SLUS528A – MARCH 2002 – REVISED AUGUST 2002

DUAL-SLOT PCI HOT-PLUG POWER CONTROLLER

FEATURES

- **12-V, –12-V, 3.3-V, 5-V Main Power Switching and Auxiliary 3.3-V Power Switching**
- **12-V, –12-V And Auxiliary 3.3-V Power FETs**
- **Hot-Swap Protection and Control of All Supplies**
- **Overcurrent Protection for All Supplies**
- **Isolation of Any Load Fault in One Slot from Any Other Slot**
- **Undervoltage Monitoring for the Main 12-V, 3.3-V, 5-V and Auxiliary 3.3-V Supplies**
- **Power Fault Latching**
- **Overtemperature Shutdown**
- **Slot Status Readout with Open-Drain LED Drivers**
- **Mechanical Switch Inputs for Attention Request and Electrical Interlock**
- **Serial Interface for Power Control, Power Status, Slot Control and Slot Status**
- **Compatible With 33-MHz, 66-MHz, and 133-MHz Bus Speeds**
- **Compliant To PCI And PCI-X Hot Plug Specifications**
- **One TPS2340A Supports Two Slots**

DESCRIPTION

The TPS2340A contains main supply power control, auxiliary supply power control, power FETs for 12 V, –12 V and auxiliary 3.3 V supplies, and a serial interface for communications with and control of slots. Each TPS2340A contains supply control and switching for two slots.

The main power control circuits start with all supplies off and hold all supplies off until power to the TPS2340A is valid on all positive supplies. When power is requested via the serial interface, the control circuit applies constant current to the gates of the power FETs, allowing each FET to ramp load voltage linearly. Each supply can be programmed for a desired ramp rate by selecting a gate capacitor for the power FET for that supply. The power control circuits also monitor load current and latch off that slot if the load current exceeds a programmed maximum value. In addition, once the 12-V, the 5-V, and the 3.3-V FETs are fully enhanced, the load voltage is monitored. If load voltage drops out of specification after these FETs are fully enhanced, the slot latches off. This provides another level of protection from load fault.

The auxiliary power control circuit switches, ramps, and monitors 3.3-V auxiliary power to each slot. The auxiliary control circuit also controls data switches that connect slot interrupts (power management event [PME] outputs) to the main interrupt PME bus after 3.3-V auxiliary supply is connected. PME is disconnected when a board is turned off or faulted.

Each TPS2340A contains power FETs for 12 V at 500 mA, –12 V at 100 mA, and auxiliary 3.3 V at 375 mA for each slot. These power FETs are short-circuit protected, slew rate controlled, and over-temperature protected.

The serial interface communicates with a slot controller using a synchronous serial protocol. The interface communicates with the slot, status LEDs, and mechanical switches with individual, dedicated lines. The interface operates from 3.3-V power but inputs are 5-V tolerant. Status LED drivers are capable of driving 24-mA LEDs via integrated open-drain MOSFETs. Mechanical switch inputs have internal pull-up and hysteresis buffers. The serial interface controls slot power, bus connection, and LED outputs, and monitors board capability, power fault, and switch input status.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Input voltage range:	P12VIN	–0.5 V to 15 V
	M12VIN	–15.0 V to 0.5 V
	All others	–0.5 V to 6 V
Output voltage range:	P12VO, 5V3VG	–0.5 V to V_{P12VIN} +0.5 V
	P12VG	–0.5 V to 28 V
	M12VO, M12VG	V_{M12VIN}–0.5 V to 0.5 V
Output current pulse:	P12VO (DC internally limited)	4 A
	M12VO	0.8 A
Operating virtual temperature range, T_J		–40°C to 85°C
Storage temperature range, T_{stg}		–55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are respect to DGND.

electrical characteristics over recommended operating temperature range, P12VINA = P12VINB = 12 V, V5IN = 5 V, DIGVCC = 3.3 V, M12VINA = M12VINB = –12 V, 3VAUXI = 3.3 V, all outputs unloaded, T_A = T_J (unless otherwise noted)

5-V/3.3-V Supply

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$5V_{OC}$ input threshold voltage	R_{OCSET} = 6.04 kΩ	43	53	63	mV
5VISA, 5VISB voltage fault threshold	After P12VG and 5V3VG good	4.16	4.65	4.92	V
5VISA, 5VISB voltage fault minimum captured pulse			75	135	ns
5VSA input bias current	PWRENx = high	–100		100	µA
5VISA, 5VISB input bias current	PWRENx = high	100	250	500	µA
5VISA, 5VISB bleed current	PWRENx = low, 5VISx = 5 V	5	10	20	mA
$3V_{OC}$ Input threshold voltage	R_{OCSET} = 6.04 kΩ	53	63	72	mV
3VISA, 3VISB voltage fault threshold	After P12VG and 5V3VG good	2.64	2.86	3.08	V
3VISA, 3VISB voltage fault minimum captured pulse time			75	135	ns
3VSA, 3VSB input bias current	PWRENx = high	–100		100	µA
3VISA, 3VISB input bias current	PWRENx = high	100	250	500	µA
3VISA, 3VISB bleed current	PWRENx = low, 5VISx = 5 V	5	10	20	mA
5V3VGA, 5V3VGB charge current		–25	–20	–14.5	µA
5V3VGA, 5V3VGB discharge current			200		mA
5V3VGA, 5V3VGB good threshold	P12VIN = 12V	9.5	11	11.5	V
5V3VGA, 5V3VGB turn-off time	C_{5V3VG} = 0.022 µF, 5V3VG falling from 90% to 10%		1	3.5	µs

electrical characteristics over recommended operating temperature range, P12VINA = P12VINB = 12 V, V5IN = 5 V, DIGVCC = 3.3 V, M12VINA = M12VINB = –12 V, 3VAUXI = 3.3 V, all outputs unloaded, $T_A = T_J$ (unless otherwise noted) (continued)

12-V Supply

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
+12-V Internal NMOS on-resistance	PWREN = HIGH, I_D = 0.5 A, $T_A = T_J$ = 25°C		0.18	0.3	Ω
	PWREN = HIGH, I_D = 0.5 A			0.4	Ω
–12-V Internal NMOS on-resistance	PWREN = HIGH, I_D = 0.1 A, $T_A = T_J$ = 25°C		0.5	0.75	Ω
	PWREN = HIGH, I_D = 0.1 A			0.9	
+12-V overcurrent threshold	R_{OCSET} = 6.04 kΩ	0.83	1.00	1.17	A
–12-V overcurrent threshold	R_{OCSET} = 6.04 kΩ	0.12	0.19	0.25	
P12VOA, P12VOB fault threshold voltage	After P12VG and 5V3VG good	9.50	10.80	11.15	V
P12VOA, P12VOB voltage fault minimum captured pulse time			75	135	ns
M12VGA, M12VGB gate charge current		–25	–20	–14.5	µA
M12VGA, M12VGB gate discharge current			200		mA
P12VGA, P12VGB, charge current	Derived from charge pump	1.0	4.0	8.5	µA
P12VGA, P12VGB, discharge current			100		mA
P12VGA, P12VGB good threshold	P12VIN = 12 V	19	20.5	22	V
Turn-on time	PWREN = HIGH to M12VO = –10.4 V, C_{M12VG} = 0.022 µF, R_L = 120 Ω, C_{M12VO} = 50 µF		15	20	ms
	PWREN = HIGH to P12VO = 11.4 V, C_{12PVG} = 0.022 µF, R_L = 24 Ω, C_{P12VO} = 200 µF		60	75	
Turn-off time	PWREN = LOW to P12VO = 0.6 V, CP12VG = 0.022 µF		1.5	3.5	µs
	PWREN = LOW to M12VO = –0.6 V, CM12VG = 0.022 µF		1.5	3.5	µs
M12VO bleed current			–20	–5	mA
P12VO bleed current		5	10		

input/output control

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
P12VIN supply current	P12VIN = 12 V		1	2	mA
V5IN supply current	V5IN = 5 V		1.00	2.75	
DIGVCC supply current	DIGVCC = 3.3 V		500	2000	µA
M12VIN supply current	M12VIN –12 V		250	2000	
3VAUXI supply current	3VAUXI = 3.3 V		200	2000	
Overcurrent fault response time			500	960	ns
DIGVCC start-up threshold voltage		2.60	2.80	2.95	V
DIGVCC stop threshold voltage		2.40	2.55	2.80	
V5IN start-up threshold voltage		4.2	4.4	4.6	
V5IN stop threshold voltage		3.8	4.0	4.4	
P12VIN start-up threshold voltage		10.2	10.3	11.2	
P12VIN stop threshold voltage		9.5	9.4	10.6	

electrical characteristics over recommended operating temperature range, P12VINA = P12VINB = 12 V, V5IN = 5 V, DIGVCC = 3.3 V, M12VINA = M12VINB = –12 V, 3VAUXI = 3.3 V, all outputs unloaded, $T_A = T_J$ (unless otherwise noted) (continued)

noise filter

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Ignored spike from overcurrent			250		ns
Latched spike from overcurrent			500		ns

3.3 V AUX and PME

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
3VAUXx overcurrent shutdown		0.95	1.15	1.40	A
3VAUXI to 3VAUXx on-resistance	I_{3VAUXx} = –500 mA		300	425	mΩ
3VAUXI undervoltage lockout		1.9	2.2	2.9	V
3VAUXx turn-on slew rate			1.6	3.3	V/ms
3VAUXx turn-on time from SWx	from SWx < 0.8 V, C_{3VAUXx} = 150 μF		3	5	ms
3VAUXx turn-off time from SWx	from SWx > 2.0 V		2.5	7.0	
3VAUXx turn-off time from Faultx	from 3VAUXx overcurrent fault detected		5	10	μs
PMEx turn-on time from 3VAUXx	from 3VAUXx > 3.0 V, C_{3VAUXx} = 150 μF	6	10	17	ms
PMEx turn-off time from SWx	from SWx > 2.0 V,		2	4	μs
PMEx turn-off time from Faultx	from 3VAUXx overcurrent fault detected		2	4	μs
PMEx switch on-resistance	from SWx < 0.8 V, I_D = 10 mA, $T_A = T_J$ = 25°C		5	10	Ω

ac switching characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{MAX} operating clock frequency	$0 \le T_A \le 70°C$	0		10	MHz
SIDO t_{CO} clock to output time	C_L = 50 pF, $0 \le T_A \le 70°C$	0		15	ns
SIDI, $\overline{\text{SIL}}$ t_{SU} setup to clock time	$0 \le T_A \le 70°C$	15			
SODI, t_{SU} setup to clock time	$0 \le T_A \le 70°C$	15			
SODI, t_H hold time	$0 \le T_A \le 70°C$	0		15	
All outputs t_{CO} clock to output time	$\overline{\text{BUSENx}}$, SIDO: C_L = 50 pF, $\overline{\text{RESETx}}$: C_L = 35 pF, All other outputs: C_L = 25 pF, $0 \le T_A \le 70°C$,			20	
Recommended input rise and fall times	10% to 90% of VCC, all digital inputs except $\overline{\text{SWx}}$, $\overline{\text{BUTTONx}}$, PGOOD, $\overline{\text{PRSNT1x}}$, and $\overline{\text{PRSNT2x}}$	0.2		1	

electrical characteristics over recommended operating temperature range, P12VINA = P12VINB = 12 V, V5IN = 5 V, DIGVCC = 3.3 V, M12VINA = M12VINB = –12 V, 3VAUXI = 3.3 V, all outputs unloaded, $T_A = T_J$ (unless otherwise noted) (continued)

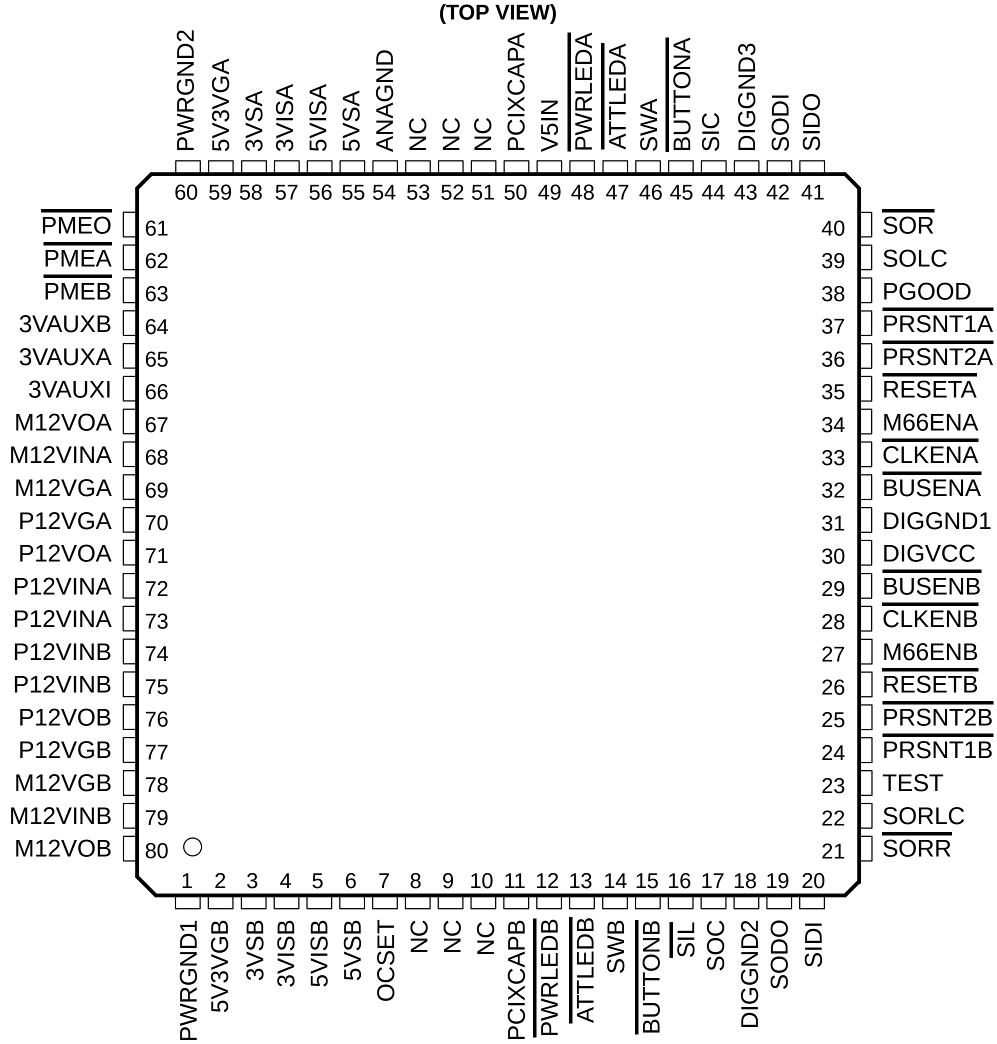
dc electrical characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input threshold voltage (SIL, SOC, SIDI, SORR, SORLC, TEST, M66EN, SOLC, SOR, SODI, SIC)		0.8	1.4	2.0	V
High–level input threshold voltage (SWA, SWB, BUTTONA, BUTTONB, PRSNT1A, PRSNT2A, PRSNT1B, PRSNT2B, PGOOD)		2.0	2.4	2.8	V
Low-level input threshold voltage (SWA, SWB, BUTTONA, BUTTONB, PRSNT1A, PRSNT2A, PRSNT1B, PRSNT2B)		0.8	1.2	1.6	V
Low-level input threshold voltage (PGOOD)		0.1	0.4	0.8	V
Input hysteresis (SWA, SWB, BUTTONA, BUTTONB, PRSNT1A, PRSNT2A, PRSNT1B, PRSNT2B)		0.4	1.0	1.6	V
Input hysteresis (PGOOD)		1.5	2.0	2.5	V
High-level output voltage (BUSENA, BUSENB)	I_L = –8 mA	2.4	2.8		V
Low-level output voltage (BUSENA, BUSENB)	I_L = 16 mA		0.2	0.5	V
Low-level output voltage (PWRLEDA, PWRLEDB, ATTLEDA, ATTLEDB)	I_L = 24 mA		0.4	0.8	V
Low-level output voltage (all other outputs)	I_L = 4 mA		0.2	0.5	V
3.3 V pull-up resistor impedance (inputs pulled up to 3.3 V)		30		200	kΩ
5 V pull-up resistor impedance (inputs pulled up to 5 V)		30		200	kΩ
Pull-down resistor impedance (inputs with pull-down)		30		200	kΩ
PCIXCAPA, PCIXCAPB resistor for 133 MHz	Open circuit recommended	30			kΩ
PCIXCAPA, PCIXCAPB resistor for 66 MHz	10 kΩ connection to DIGGND recommended	6		14	kΩ
PCIXCAPA, PCIXCAPB resistor for 33 MHz	0 kΩ connection to DIGGND recommended			1	kΩ

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, P12VINA, P12VINB	10.8	13.2	V
Input voltage, V5IN	4.75	5.25	V
Input voltage, DIGVCC	3.1	3.5	V
Input voltage, M12VINA, M12VINB	–13.2	–10.8	V
Input voltage, 3VAUXI	3.1	3.5	V
Load current, PWRLEDA, PWRLEDB, ATTLEDA, ATTLEDB	0	24	mA
Load current, P12VOA, P12VOB	0	500	mA
Load current, M12VOA, M12VOB	0	100	mA
Load current, 3VAUXA, 3VAUXB	0	375	mA

PFP PACKAGE
(TOP VIEW)



AVAILABLE OPTIONS

T_A	PACKAGE
	HTQFP (PFP)
–40°C to 85°C	TPS2340APFP

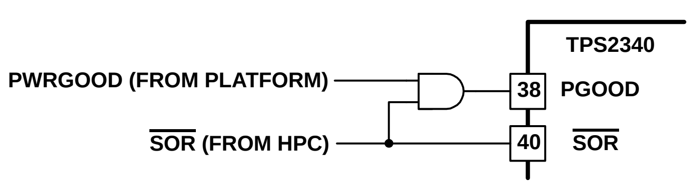
Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
3VAUXI	66	I	3.3Vaux voltage supply input. A 0.1-µF bypass capacitor to PWRGND is recommended.
3VAUXA	65	O	3.3Vaux voltage supply outputs. A 0.01-µF bypass capacitor to PWRGND is recommended.
3VAUXB	64	O	
3VISA	57	I	Connect to the load side of the sense resistor. See definition for 3VS. This pin has a switched FET to ground to discharge any output load capacitance when the output is turned off. A 0.01-µF bypass capacitor to ANAGND is recommended.
3VISB	4	I	
3VSA	58	I	Connect to the source side of the 3.3-V FET switch. This pin in conjunction with the 3VIS pin sense the current to the 3.3-V load by sensing the voltage drop across a sense resistor. A 0.01-µF bypass capacitor to ANAGND is recommended.
3VSB	3	I	
5V3VGA	59	O	Gate drive for the 5-V and 3.3-V FET switches. Ramp rate is programmed by external capacitance connected from this pin to PWRGND. The capacitor is charged with a 20-µA current source and discharged with a switch. The output UV circuitry is disabled until the voltage on this pin is greater than 11 V and the voltage on P12VGx is greater than 20 V.
5V3VGB	2	O	
5VISA	56	I	Connect to the load side of the sense resistor. See definition for 5VS. 5VIS is also used to sense the output voltage for the 5-V UV circuit. This pin has a switched FET to ground to discharge any output load capacitance when the output is turned off. A 0.01-µF bypass capacitor to ANAGND is recommended.
5VISB	5	I	
5VSA	55	I	Connect to the source of the 5-V FET switch. This pin in conjunction with the 5VIS pin senses the current to the 5V load by sensing the voltage drop across the sense resistor. A 0.01-µF bypass capacitor to ANAGND is recommended.
5VSB	6	I	
ANAGND	54	–	Ground pin for the low level analog section
$\overline{\text{ATTLEDA}}$	47	O	$\overline{\text{ATTLEDx}}$ is a high-current, low-true, open-drain output with a 100-kΩ pull-up resistor to V5IN.
$\overline{\text{ATTLEDB}}$	13	O	
$\overline{\text{BUSENA}}$	32	O	Output-to-bus enable FET switches. These outputs typically enable PCI clocks to the PCI connector.
$\overline{\text{BUSENB}}$	29	O	
$\overline{\text{BUTTONA}}$	45	I	PCI hot-plut attention notification (momentary) button inputs. Low indicates attention. These input have hysteresis and a 100-kΩ pull-up to DIGVCC, requiring only a capacitor to ground for debouncing mechanical noise.
$\overline{\text{BUTTONB}}$	15	I	
$\overline{\text{CLKENA}}$	33	O	Output-to-clock enable FET switches. These outputs typically enable PCI clocks to the PCI connector.
$\overline{\text{CLKENB}}$	28	O	
DIGVCC	30	I	Power pin for the digital section, connect to 3.3 V. A 0.1-µF bypass capacitor from DIGVCC to DIGGND is recommended.
DIGGND1	31	–	Ground pins for the digital section.
DIGGND2	18	–	
DIGGND3	43	–	
M12VGA	69	O	A capacitor connected from this pin to M12VO programs the ramp rate of the 12-V switched output. The capacitor is charged with a 20-µA current source and discharged with a switch.
M12VGB	78	O	
M12VINA	68	I	–12-V input voltage to the device and the –12-V power FET. M12VINA and M12VINB must be tied together and are internally connected by a high-resistance path. The tab on the back of the package is also connected to M12VIN. A 0.1-µF bypass capacitor from M12VIN to PWRGND is recommended.
M12VINB	79	I	
M12VOA	67	O	–12-V Switched output. This pin has a switched FET to ground to discharge any output load capacitance when the output is turned off. A 0.01-µF bypass capacitor to PWRGND is recommended.
M12VOB	80	O	
M66ENA	34	I	PCI 66MHz–capable bit for slot A. This pin has a 100-kΩ pull-up to 3VISA. This pin is typically tied to the PCI connector.
M66ENB	27	I	PCI 66MHz–capable bit for slot B. This pin has a 100-kΩ pull-up to 3VISB. This pin is typically tied to the PCI connector.
OCSET	7	I	A resistor connected between this pin and ANAGND sets the overcurrent threshold of the 4 FET switches. The +12-V and –12-V switches are set for the maximum permissible currents per the PCI specification when a 1%, 6.04-kΩ resistor is used. A 0.1-µF bypass capacitor from OCSET to ANAGND is recommended.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
P12VGA	70	O	Gate drive for the 12-V internal N-channel MOSFET for slot A. Connect a capacitor from this pin to PWRGND to program the ramp rate. The capacitor is charged with a 5–µA current source and discharged with a switch. The output undervoltage circuitry is disabled until the voltage on this pin is greater than 20 V and the voltage on 5V3VGA is greater than 11 V.
P12VGB	77	O	Gate drive for the 12-V internal N-channel MOSFET for slot B. Connect a capacitor from this pin to PWRGND to program the ramp rate. The capacitor is charged with a 5-µA current source and discharged with a switch. The output undervoltage circuitry is disabled until the voltage on this pin is greater than 20 V and the voltage on 5V3VGB is greater than 11 V.
P12VINA	72	I	12-V input to the device and the 12-V power FET for slot A. A 0.1-µF bypass capacitor from P12VINA to PWRGND is recommended.
	73	I	
P12VINB	75	I	12-V input to the device and the 12-V power FET for slot B. A 0.1-µF bypass capacitor from P12VINB to PWRGND is recommended.
	74	I	
P12VOA	71	O	12-V switched output for slot A. This pin has a switched FET to ground to discharge any output load capacitance when the output is turned off. A 0.01-µF bypass capacitor to PWRGND is recommended.
P12VOB	76	O	12-V switched output fo rslot B. This pin has a switched FET to ground to discharge any output load capacitance when the output is turned off. A 0.01-µF bypass capacitor to PWRGND is recommended.
PCIXCAPA	50	I	PCI–X capable bit. To select 133-MHz PCI–X mode, leave PCIXCAPx floating. For 66-MHz PCI–X mode, pull down PCIXCAPx with one or two 10-kΩ resistors. For 33-MHz PCI 2.2 mode, ground PCIXCAPx. This pin has a 10-kΩ pull–up resistor to DIGVCC. This pin is typically tied to the PCI connector.
PCIXCAPB	11	I	
PGOOD	38	I	Power good input. PGOOD has hysteresis so that it can be used as a power-on reset, driven from a slow-rising RC. PGOOD also has a 100-kΩ pull-up to DIGVCC. A logic path in the TPS2340A prevents the input data state machine from being reset when $\overline{\text{SOR}}$ asserts. This can be corrected with an external AND gate, which causes PGOOD to be de-asserted whenever $\overline{\text{SOR}}$ is asserted. (See Note 1.)
$\overline{\text{PMEA}}$	62	I	$\overline{\text{PME}}$ input from slot A. These signals comply with PCI Power Management Spec 1.1. $\overline{\text{PMEA}}$ has a 200-kΩ pull-up to the appropriate switched 3VAUX for precharging. This pin is typically tied to the PCI connector.
$\overline{\text{PMEB}}$	63	I	$\overline{\text{PME}}$ input from slot B. These signals comply with PCI Power Management Spec 1.1. $\overline{\text{PMEB}}$ has a 200-kΩ pull-up to the appropriate switched 3VAUX for precharging. This pin is typically tied to the PCI connector.
$\overline{\text{PMEO}}$	61	O	$\overline{\text{PME}}$ output from the device. This signal is an open-drain output and complies with PCI Power Management Specification 1.1 $\overline{\text{PME}}$ definition.
$\overline{\text{PRSNT1A}}$	37	I	PCI presence detect bit 1. This input has hysteresis and a 100-kΩ pull-up to DIGVCC, requiring only a capacitor to ground for debouncing mechanical noise. This pin is typically tied to the PCI connector.
$\overline{\text{PRSNT1B}}$	24	I	
$\overline{\text{PRSNT2A}}$	36	I	PCI–presence detect bit 2. This input has hysteresis and a 100-kΩ pull–up to DIGVCC, requiring only a capacitor to ground for debouncing mechanical noise. This pin is typically tied to the PCI connector.
$\overline{\text{PRSNT2B}}$	25	I	
PWRGND1	1	–	Ground pin for the power analog section.
PWRGND2	60	–	
$\overline{\text{PWRLEDA}}$	48	O	In normal operation, output-to-power indicator PCI hot-plug status LED. In test mode, indicates the state of the internal signal PWRENx, the power FET control signal. $\overline{\text{PWRLEDx}}$ is a high-current, low-true open-drain output with a 100-kΩ pull-up resistor.
$\overline{\text{PWRLEDB}}$	12	O	

NOTE 1: PGOOD input: diagram:

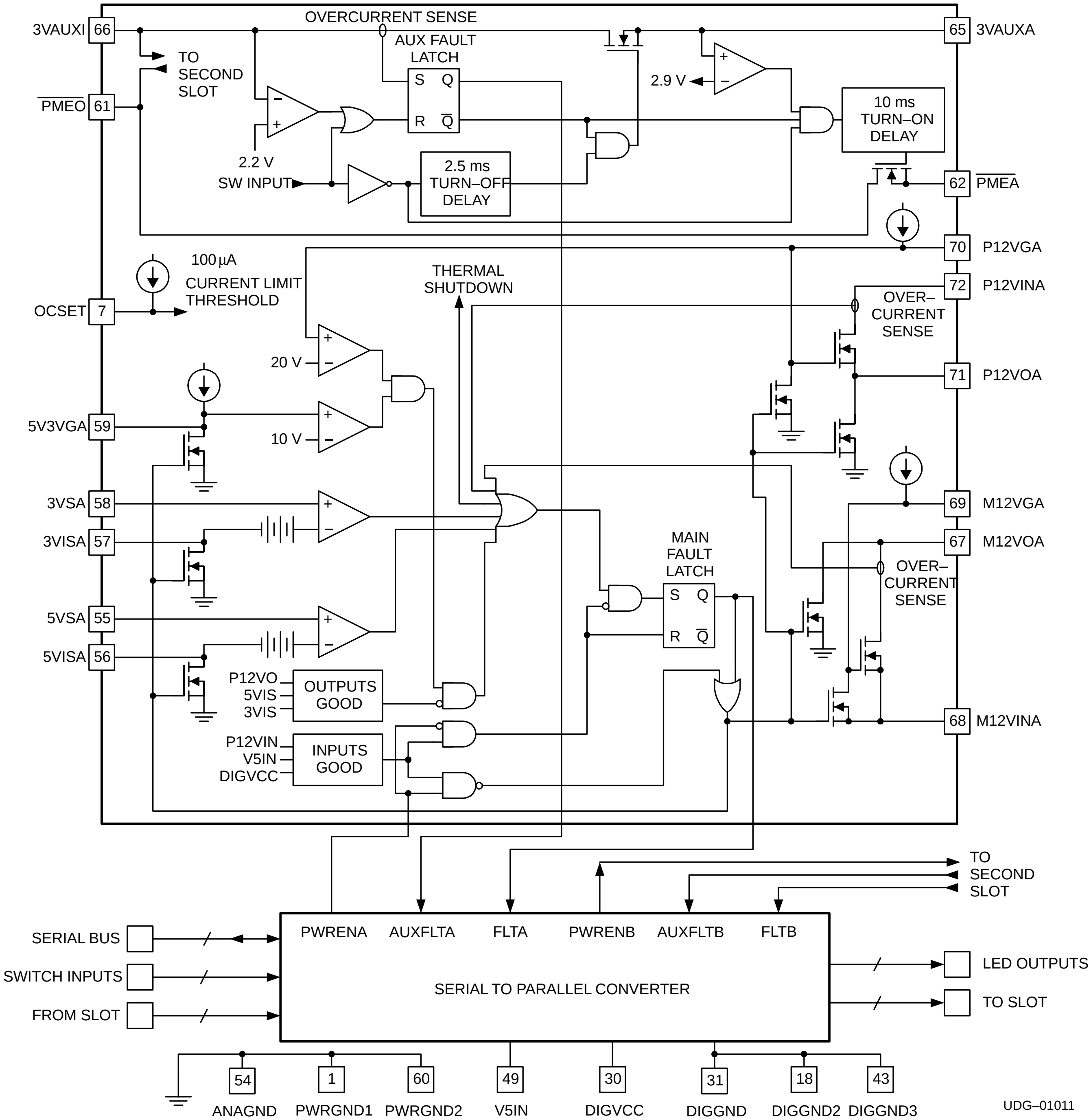


UDG–01126

Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
$\overline{\text{RESETA}}$	35	O	PCI $\overline{\text{RESET}}$ signal to slot A. Conforms to PCI 2.2 local bus specification for 3.3-V signaling. This pin is typically tied to the PCI connector.
$\overline{\text{RESETB}}$	26	O	PCI $\overline{\text{RESET}}$ signal to slot B. Conforms to PCI 2.2 local bus specification for 3.3-V signaling. This pin is typically tied to the PCI connector.
SIC	44	I	Serial input clock. Shift serial data into device one bit position on rising edge.
SIDI	20	I	Serial input data Input. The serial shift register input from a down-stream TPS2340.
SIDO	41	I/O	Serial input data output. The serial shift register output to the PCI hot-plug controller or the up-stream TPS2340. When PGOOD is low, SIDO is undriven and pulled up to DIGVCC with a 100-kΩ resistor. During the rising edge of PGOOD, the TPS2340A latches SIDO as MODE0.
$\overline{\text{SIL}}$	16	I	Serial input load. Pulse low to synchronously parallel load external serial input shift registers on the next rising edge of SIC.
SOC	17	I	Serial output clock. Shift serial output data into parallel output registers one bit position on rising edge.
SODI	42	I	Serial output data input. Serial output data shifted into parallel output registers.
SODO	19	I/O	Serial output data output. Serial output data shifted to the down-stream TPS2340. When PGOOD is low, SODO is undriven and pulled up to DIGVCC with a 100-kΩ resistor. During the rising edge of PGOOD, the TPS2340A latches SODO as MODE1.
SOLC	39	I	Serial output latch clock. Latch parallel register data on rising edge.
SORLC	22	I	Serial output reset latch clock. Latch parallel register data on rising edge (PCI $\overline{\text{RESET}}$ latches only).
$\overline{\text{SOR}}$	40	I	Serial output reset. Clears parallel register data.
$\overline{\text{SORR}}$	21	I	Serial output reset reset. Clears parallel register data (PCI $\overline{\text{RESET}}$ latches only).
SWA	46	I	Slot A switch input. Low indicates the slot is populated. This input has hysteresis and a 100-kΩ pull-up to 3VAUXI, requiring only a capacitor to ground for debouncing mechanical noise. For testing purposes, pulling SWA to 5 V enables the slot main power and disables the slot auxilliary power, bypassing the serial interface.
SWB	14	I	Slot B switch input. Low indicates the slot is populated. This input has hysteresis and a 100-kΩ pull-up to 3VAUXI, requiring only a capacitor to ground for debouncing mechanical noise. For testing purposes, pulling SWB to 5 V enables the slot main power and disables the slot auxilliary power, bypassing the serial interface.
TEST	23	I	When asserted on the rising edge of PGOOD, device enters test modes based on the states of the MODE pins. See *In–Circuit Test* section of the datasheet. When asserted after PGOOD is asserted, maps the Pwrenx and ANDed Faultx internal signals to $\overline{\text{PWRLED}}$ and $\overline{\text{ATTLED}}$ pins for test purposes. TEST has a 100-kΩ pull-down resistor to ground.
V5IN	49	I	5-V input to the device. A 0.1-µF bypass capacitor from V5IN to PWRGND is recommended.

functional block diagram



APPLICATION INFORMATION

Figure 1 shows three TPS2340A devices cascaded in a system to control six PCI or PCI–X hot-plug slots. A hot-plug controller communicates with three TPS2340A devices over a nine-signal serial bus. Three signals are used to gather status information from the slots, and six signals are used to control the slots. In this bus, seven of the nine signals are connected in parallel. The remaining signals facilitate a cascaded bus and are comprised of the signal pair SIDI/SIDO and SODI/SODO. The SIDO signal drives the PCI hot-plug controller serial input data pin or the SIDI pin of another up–stream TPS2340. The SODI signal is driven by the PCI hot-plug controller and is cascaded down to the next TPS2340A via the SODO signal.

The SIDO and SODO outputs are dual-function pins that also serve as mode-select pins upon the rising edge of PGOOD. See *Digital Circuits* section for more details.

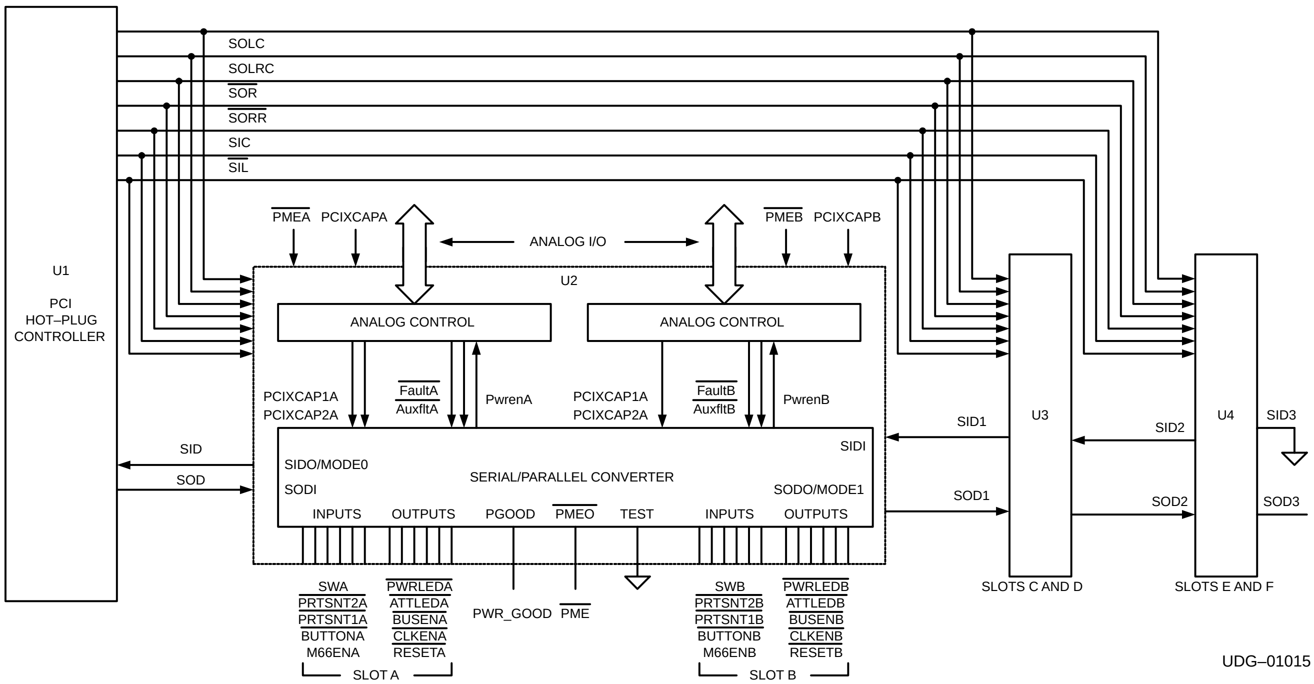


Figure 1. Hot-Plug System Block Diagram

analog circuits

power controller

The functional block diagram shows the TPS2340A with detailed information on the analog functions. For clarity, circuits for only one slot are shown in detail.

3.3-V auxiliary supply (3.3-Vaux) support

In today’s hot-plug systems, a 3.3Vaux rail remains live while the system power is shut down to allow implementation of the PCI Power Management Specification, version 1.1. The TPS2340A provides a 3.3-Vaux input pin that is monitored for undervoltage and generates a 3.3-Vaux supply pin for each hot-plug slot that is monitored for overcurrent. These supply pins are switched by the slot-specific SWx slot switch inputs. When the slot switch is opened, the slot-specific 3.3-Vaux supply is disabled to allow safe removal of the adapter card. When the slot switch is closed (SWx grounded), the slot-specific 3.3-Vaux supply is restored.

APPLICATION INFORMATION

power cycling and $\overline{\text{PME}}$

The PCI Power Management Specification defines a signal called $\overline{\text{PME}}$ (power management event) to allow power management events to be communicated back to the system. The TPS2340A provides a slot-specific $\overline{\text{PMEx}}$ input and a gated $\overline{\text{PMEO}}$ output pin that is monitored by the system. The gated $\overline{\text{PMEO}}$ output is controlled by the SWx slot switch similar to the 3.3-Vaux supply pins described above, but with a delay during connection as shown below. The purpose of the delay is to ensure that 3.3-Vaux power is stable to the slot before connecting the $\overline{\text{PMEx}}$ signal. (If the device were to observe the $\overline{\text{PMEx}}$ signal while 3.3-Vaux power was still ramping up, a false trigger could result.)

The 3.3-Vaux circuitry provides short-circuit fault detection. In the event of a fault, the slot 3.3-Vaux and $\overline{\text{PME}}$ signals are immediately disconnected. The fault state is latched internally in the TPS2340A and is cleared by opening the SWx slot switch or by the removal of the 3.3-Vaux power supplying the TPS2340.

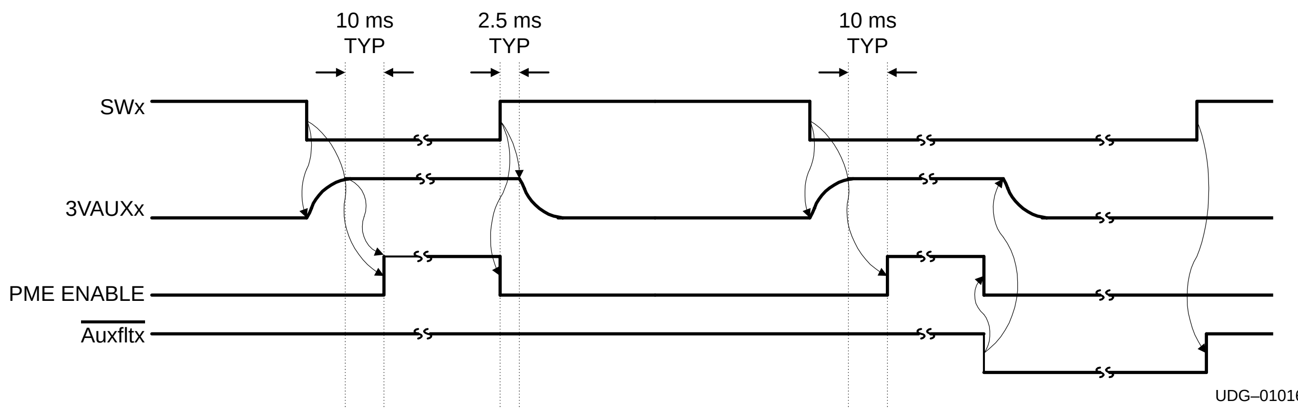


Figure 2. 3.3Vaux and $\overline{\text{PME}}$ Gating

When SWx is closed, 3VAUXx power is immediately applied to the slot with controlled slew rate, minimizing inrush current into 3VAUXx bypass capacitors. After 3VAUXx power is above threshold, a delay timer starts. At the end of the delay timer cycle, the $\overline{\text{PMEx}}$ switches close, allowing connection of the $\overline{\text{PMEx}}$ signal to the $\overline{\text{PMEO}}$ output. When multiple TPS2340A devices are used in a system, the $\overline{\text{PMEO}}$ output pins can be connected to the same node, creating a *wired–OR* $\overline{\text{PME}}$ bus that can be connected to a system interrupt input.

When SWx is opened or if there is a power fault on channel x, the $\overline{\text{PMEx}}$ switch for that channel is immediately opened and the 3VAUXx power for that channel is removed. Although these events happen at approximately the same time, the 3VAUXx power should remain high until the $\overline{\text{PMEx}}$ switch is open so that falling 3VAUXx power doesn't cause a nuisance $\overline{\text{PMEx}}$ interrupt. To insure that 3VAUXx remains high during a power fault, 3VAUXx should have a bypass capacitance of at least 20 µF. If the capacitor is not available on the inserted card, it should be provided on the system board.

APPLICATION INFORMATION

fault handling

When PGOOD is asserted (main power is valid), the serial interface is available for use. At this time, $\overline{\text{Auxflt}}$ and $\overline{\text{Faultx}}$ (i.e. $\overline{\text{Faultx}}$ = $\overline{\text{Pwrfltx}}$ • $\overline{\text{Auxflt}}$) signals are present in the registers and can be read back over the serial interface.

When PGOOD is deasserted (main power is not valid), the serial interface is inactive, so the TPS2340A provides an alternate path for observing the $\overline{\text{Auxfltx}}$ signals. In this case, $\overline{\text{Auxfltx}}$ is presented on the $\overline{\text{ATTLEDx}}$ open-drain output, so 3Vaux faults can be observed. Systems that do not require $\overline{\text{Auxfltx}}$ indications when main power is off should use main power to supply current to the attention LEDs.

In addition, when TEST is asserted after PGOOD has changed from 0 to 1, the AND of $\overline{\text{Pwrfltx}}$ and $\overline{\text{Auxfltx}}$ is present on the $\overline{\text{ATTLEDx}}$ open-drain output, so the attention LEDs can be used to report any faults on each channel.

After PGOOD is asserted with TEST deasserted and the voltage on the SWx pin is greater than V_{DIGVCC} but less than V_{V5IN}, $\overline{\text{ATTLEDx}}$ follows the fault status of the main power fault ($\overline{\text{Pwrfltx}}$). If the SWx input is pulled to V_{V5IN} potential, that slot becomes immediately enabled independent of serial interface status and $\overline{\text{ATTLEDx}}$ follows the fault status of the main power fault ($\overline{\text{Pwrfltx}}$).

Table 1. Fault Reporting Using $\overline{\text{ATTLED}}$

SWx	PGOOD	TEST	$\overline{\text{ATTLEDx}}$
< V_{DIGVCC}	0	x	$\overline{\text{Auxfltx}}$
< V_{DIGVCC}	1	1	$\overline{\text{Pwrfltx}}$ • $\overline{\text{Auxfltx}}$
> V_{DIGVCC}, < V_{V5IN}	1	0	$\overline{\text{Pwrfltx}}$
= V_{V5IN}	x	x	$\overline{\text{Pwrfltx}}$

PCI–XCAP resolution

Add-in cards indicate their PCI-X mode and frequency capabilities by connection of the PCI-XCAP pin. The TPS2340A utilizes a three-level comparator to resolve the PCI-XCAP input so as to decode operating mode and generate the PCI-XCAP2 and PCI-XCAP1 internal signals. With PCI-XCAP open, the TPS2340A selects PCI-X 133-MHz operation. PCI-X 66-MHz operation is selected by a 10-kΩ pull-down resistor on PCI-XCAP. With PCI-XCAP grounded, conventional PCI-2.2 operation is selected. This decoding conforms to the standard PCI-X specification for PCI-XCAP resolution.

Table 2. PCI-XCAP Pin State Resolution

PCI-XCAP	PCI-XCAP2	PCI-XCAP1	DESCRIPTION
GND	0	0	Conventional PCI 2.2 operation
10-kΩ Pull-down Resistor	0	1	PCI-X 66-MHz operation
Open Circuit	1	1	PCI-X 133-MHz operation

APPLICATION INFORMATION

thermal shutdown

Under normal operating conditions, the power dissipation in the TPS2340A is low enough that junction temperature (T_J) is not more than 15°C above air temperature. However, in the case of a load that exceeds PCI specifications but remains under the TPS2340A current-limit threshold, power dissipation can be higher. To prevent any damage from an out-of-specification load or severe rise in ambient temperature, the TPS2340A contains two independent thermal shutdown circuits, one for each slot’s main supplies.

The highest power dissipation in the TPS2340A is from the 12-V power FET so the TPS2340A temperature sense elements are integrated closely with these FETs. These sensors indicate when the temperature at these transistors exceeds approximately 150°C, either due to average TPS2340A power dissipation, 12-V power FET power dissipation, or a combination of both.

When excessive junction temperature is detected on one slot, that slot fault latch is set and remains set until junction temperature drops by approximately 10°C and the slot is turned off, then on again through the serial interface. The other slot is not affected by this event. Also, 3.3-Vaux is not affected by thermal events.

digital circuits

The TPS2340A implements two independent slots of hot-plug power management. In addition, the TPS2340A contains digital circuits to allow communication between these two slots and the system’s hot-plug controller. Also, the TPS2340A contains inputs for connection to mechanical switches and outputs for driving indicator LEDs to directly communicate with users and service.

This digital logic implements a serial-to-parallel converter that accepts data from the serial interface and presents that data to each slot. Data from the serial interface drives the Pwrenx internal main power control signal. Additional data from the serial interface includes $\overline{\text{BUSENx}}$ and $\overline{\text{CLKENx}}$ outputs to activate bus switches, $\overline{\text{RESETx}}$ outputs to allow reset to each slot, and $\overline{\text{ATTLEDx}}$ and $\overline{\text{PWRLEDx}}$ outputs to indicate slot status to users.

The serial-to-parallel converter also accepts data from the slot and sends that data back on the serial interface. Data to the serial interface includes SWx and $\overline{\text{BUTTONx}}$ switch state, $\overline{\text{PRSNTnx}}$ bits, M66ENx and PCI–XCAPx bits to indicate board type, and internal fault signals $\overline{\text{Auxfltx}}$ and $\overline{\text{Faultx}}$.

When the digital circuits are operating in *normal* mode, the serial interface is enabled and controls the slots. The TPS2340A also operates in various test modes, allowing board testing and system development.

Each TPS2340A controls two PCI/PCI–X slots. For systems requiring more than two slots, additional TPS2340A devices can be cascaded without requiring an additional hot-plug controller. To maintain system reliability and data integrity at full speed, bus length is often limited to six PCI slots. When higher speed PCI–X protocols are active, bus length may be limited to even fewer active slots. However, the TPS2340A is not limited in cascade capability or bus length.

APPLICATION INFORMATION

power on configuration

Table 3. lists the various modes of operation and the proper pin states that are necessary to achieve these modes. The shaded rows indicate test modes.

Table 3. Power On Configuration

PGOOD	TEST	SODO/MODE1	SIDO/MODE0	OPERATING MODE
$\uparrow$	0	1	1	Operational mode
$\uparrow$	1	0	0	NAND tree test mode
$\uparrow$	1	0	1	Tri–state test mode (all pins tri–stated)
$\uparrow$	1	1	X	Reserved
$\uparrow$	0	0	X	Reserved
$\uparrow$	0	X	0	Reserved
1	1	SODO	SIDO	Normal operation, but Pwrenx driven on $\overline{\text{PWRLEDx}}$, $\overline{\text{Faultx}}$ driven on $\overline{\text{ATTLEDx}}$.
1	0	SODO	SIDO	Normal operation

NOTE: X = Don’t care, x = slot A or B

operational mode functional description

When both mode pins are 1 and the test pin is 0, on the rising edge of PGOOD, the TPS2340A enters operational mode. In this mode, the PCI hot-plug controller is able to address multiple TPS2340A ICs and multiple slots. Input status for all slots is grouped into four channels that can be requested by the PCI hot-plug controller.

channel selection

The PCI hot-plug controller indicates to the TPS2340A which channel to read back via signaling on the $\overline{\text{SIL}}$ pin. The $\overline{\text{SIL}}$ pin asserts low for one SIC clock to indicate a *start* bit, followed by three SIC clocks of channel address information in the order of channel address LSB followed by channel address MSB and a reserved bit. So as an example, if the hot-plug controller desires to read non-interrupt capable input data from the TPS2340A (channel 01 binary), the $\overline{\text{SIL}}$ sequence is shown in Table 3.

Table 4. Input Channel Selection Example – Channel 01 Selected

CLOCK	$\overline{\text{SIL}}$ STATUS
0	Start bit (low)
1	Channel address LSB (high)
2	Channel address MSB (low)
3	Reserved (high)
4 – 47	High

APPLICATION INFORMATION

operational mode input channel address grouping

Table 5. lists the functions assigned to the channel addresses.

Table 5. Operational Mode Channel Address Grouping

CHANNEL ADDRESS	FUNCTIONAL CHANNEL GROUP
00	Interrupt capable inputs
01	Non–interrupt capable inputs
10	Diagnostic data #1
11	Diagnostic data #2

As devices are cascaded, SIDI pin data is received from devices down-stream and passes through the device, shift-register style, to eventually reach the SIDO pin and the PCI hot-plug controller. The data contained in each input channel group is described in Tables 6, 7, 8, and 9.

Table 6. Channel 00 Data Group – Interrupt Capable Inputs

BIT NUMBER	FUNCTION
0	Slot A SW (1 = interlock A open)
1	Slot A button state (1 = button A pushed)
2	Slot A power fault state ($\overline{\text{PwrfltA}}$ & $\overline{\text{AuxfltA}}$)
3	Slot A $\overline{\text{PRSNT2}}$
4	Slot A $\overline{\text{PRSNT1}}$
5	Reserved
6	Reserved
7	Reserved
8	Slot B SW
9	Slot B button state
10	Slot B power fault state ($\overline{\text{PwrfltB}}$ & $\overline{\text{AuxfltB}}$)
11	Slot B $\overline{\text{PRSNT2}}$
12	Slot B $\overline{\text{PRSNT1}}$
13	Reserved
14	Reserved
15	Reserved
16…47	SIDI pin data for slots C, D, E and F follows

APPLICATION INFORMATION

Table 7. Channel 01 Data Group – Non–Interrupt Capable Inputs

BIT NUMBER	FUNCTION
0	Slot A M66EN
1	Slot A PCI–XCAP1
2	Slot A PCI–XCAP2
3	Slot A Aux Power Fault state ($\overline{\text{AuxfltA}}$)
4	Reserved
5	Reserved
6	Reserved
7	Reserved
8	Slot B M66EN
9	Slot B PCI–XCAP1
10	Slot B PCI–XCAP2
11	Slot B Aux Power Fault state ($\overline{\text{AuxfltB}}$)
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16…47	SIDI pin data for slots C, D, E and F follows

Table 8. Channel 10 Data Group – Diagnostic Channel #1

BIT NUMBER	FUNCTION
0	Device Present 1 = Power controller is present 0 = Power controller is not installed
1	Slot A Pwren state
2	Slot A $\overline{\text{CLKEN}}$ state (0 = clock enabled)
3	Slot A $\overline{\text{BUSEN}}$ state (0 = bus enabled)
4	Slot A $\overline{\text{PCIRST}}$ state (0 = reset asserted)
5	Slot A $\overline{\text{PWRLED}}$ state (1 = power LED on)
6	Slot A $\overline{\text{ATTLED}}$ state (1 = attention LED on)
7	Reserved
8	Device Present 1 = Power controller is present 0 = Power controller is not installed
9	Slot B Pwren state
10	Slot B $\overline{\text{CLKEN}}$ state
11	Slot B $\overline{\text{BUSEN}}$ state
12	Slot B $\overline{\text{PCIRST}}$ state
13	Slot B $\overline{\text{PWRLED}}$ state
14	Slot B $\overline{\text{ATTLED}}$ state
15	Reserved
16…47	SIDI pin data for slots C, D, E and F follows

Table 9. Channel 11 Data Group – Diagnostic Channel #2

BIT NUMBER	FUNCTION
0	Slot A latched Mode 0 bit state. This bit is latched at PGOOD
1	Slot A latched Mode 1 bit state. This bit is latched at PGOOD.
2	Must be set to 1.
3	Reserved
4	Reserved
5	Reserved
6	Reserved
7	Reserved
8	Slot B latched Mode 0 bit state. This bit is latched at PGOOD.
9	Slot B latched Mode 1 bit state. This bit is latched at PGOOD.
10	Must be set to 1.
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16…47	SIDI pin data for slots C, D, E and F follows

Figure 3. illustrates the input scan chain timing for operational mode.

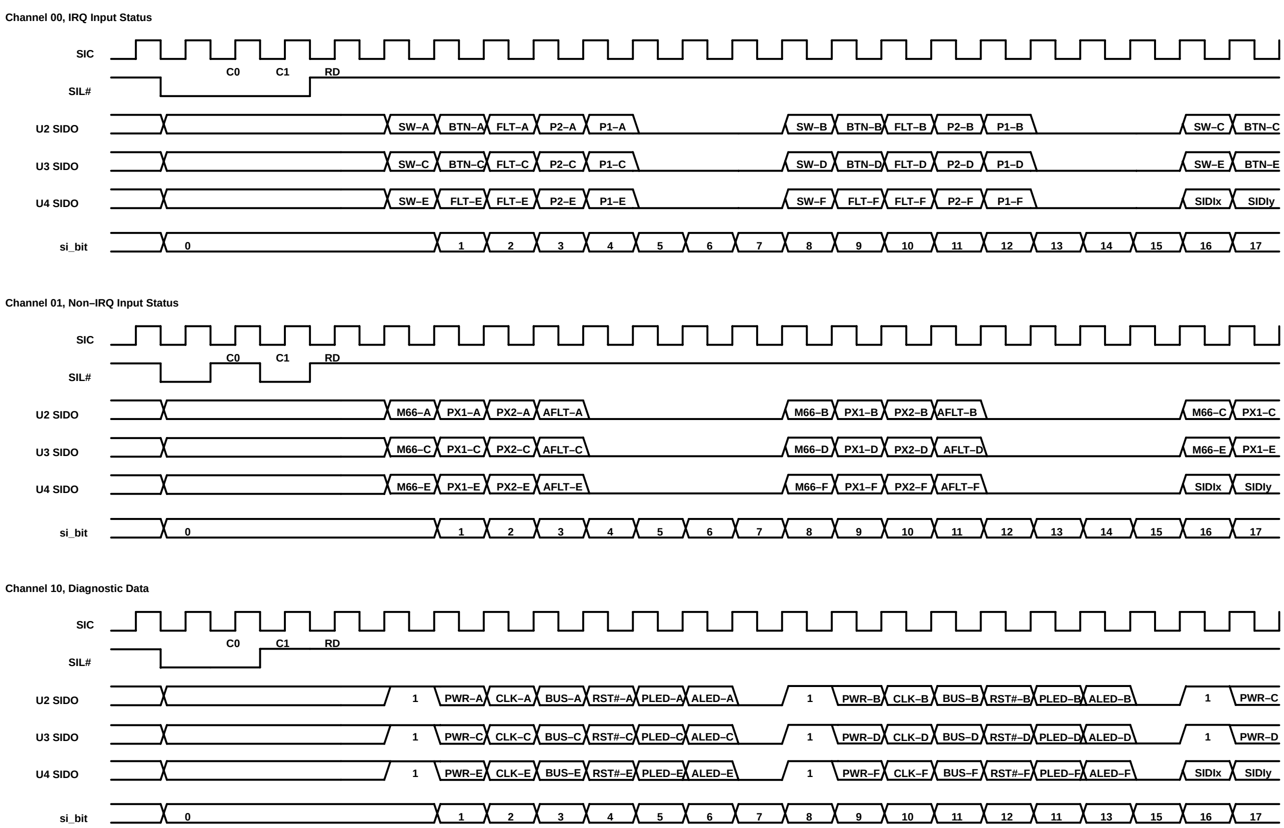


Figure 3. Serial Input Data Timing

APPLICATION INFORMATION

Similar to input data, serial output data has been ordered to facilitate cascading TPS2340A devices. Assuming a six-slot implementation, as input data arrives in the order of slot A first, followed by data for slots B through F, output data is delivered in reverse order, slot F data first, then data for slots E through A. For a PCI hot-plug controller that supports 6 slots, 48 bits (8 per slot) are shifted out by the controller any time a slot control state needs to be changed. At the conclusion of a shift-out process, output data for slots A and B is contained in the device (electrically) closest to the PCI hot-plug controller. Output data for each slot is delivered in the bit order described in Table 10.

Table 10. Operational Mode Output Data Bit Order

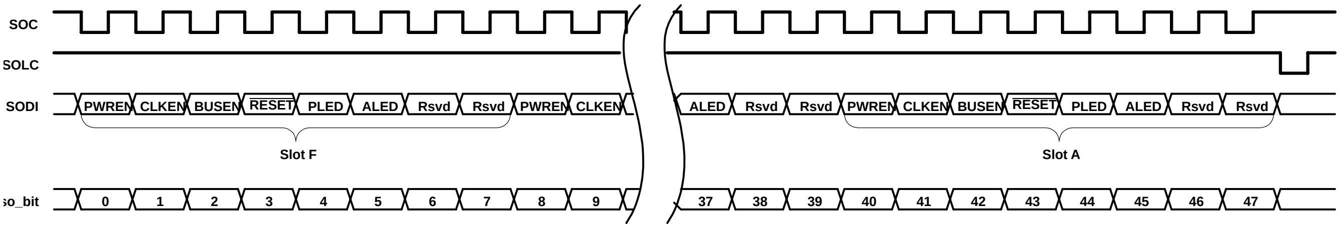
BIT NUMBER	FUNCTION
0	Slot F Pwren state (1 = turn on power)
1	Slot F CLKEN state (1 = enable the clock)
2	Slot F BUSEN state (1 = enable the bus)
3	Slot F $\overline{\text{PCIRST}}$ state (0 = assert $\overline{\text{PCIRST}}$)
4	Slot F PWRLED state (1 = turn on power LED)
5	Slot F ATTLED state (1 = turn on attention LED)
6	Reserved
7	Reserved
8	Slot E Pwren state
9	Slot E CLKEN state
10	Slot E BUSEN state
11	Slot E $\overline{\text{PCIRST}}$ state
12	Slot E PWRLED state
13	Slot E ATTLED state
14	Reserved
15	Reserved
16…47	SODO pin data for slots D, C, B and A follows

The output data for the six slots is shifted out using the SOC clock. After the appropriate data pattern is established in the shift registers, this data is parallel clocked into registers via latch clocks. These registers drive the output pins and controls. The SOLC pin serves as the latch clock for the Pwrenx, $\overline{\text{BUSENx}}$, $\overline{\text{CLKENx}}$, $\overline{\text{PWRLEDx}}$, and $\overline{\text{ATTLEDx}}$ outputs.

The SORLC pin serves as the latch clock for the $\overline{\text{RESETx}}$ pins. Two latch clocks are used so that the PCI bus timing requirements between $\overline{\text{REQ64}}$, $\overline{\text{TRDY}}$, $\overline{\text{DEVSEL}}$, and $\overline{\text{STOP}}$ and the slot’s $\overline{\text{RST}}$ signal can be more easily controlled by the hot-plug controller.

If a fault occurs, as indicated by the assertion of the $\overline{\text{Faultx}}$ signal (where $\overline{\text{Faultx}}$ = $\overline{\text{Pwrfltx}}$ and $\overline{\text{Auxfltx}}$), the $\overline{\text{RESETx}}$ pin asynchronously asserts and the $\overline{\text{CLKENx}}$ and $\overline{\text{BUSENx}}$ pins are asynchronously deasserted.

APPLICATION INFORMATION



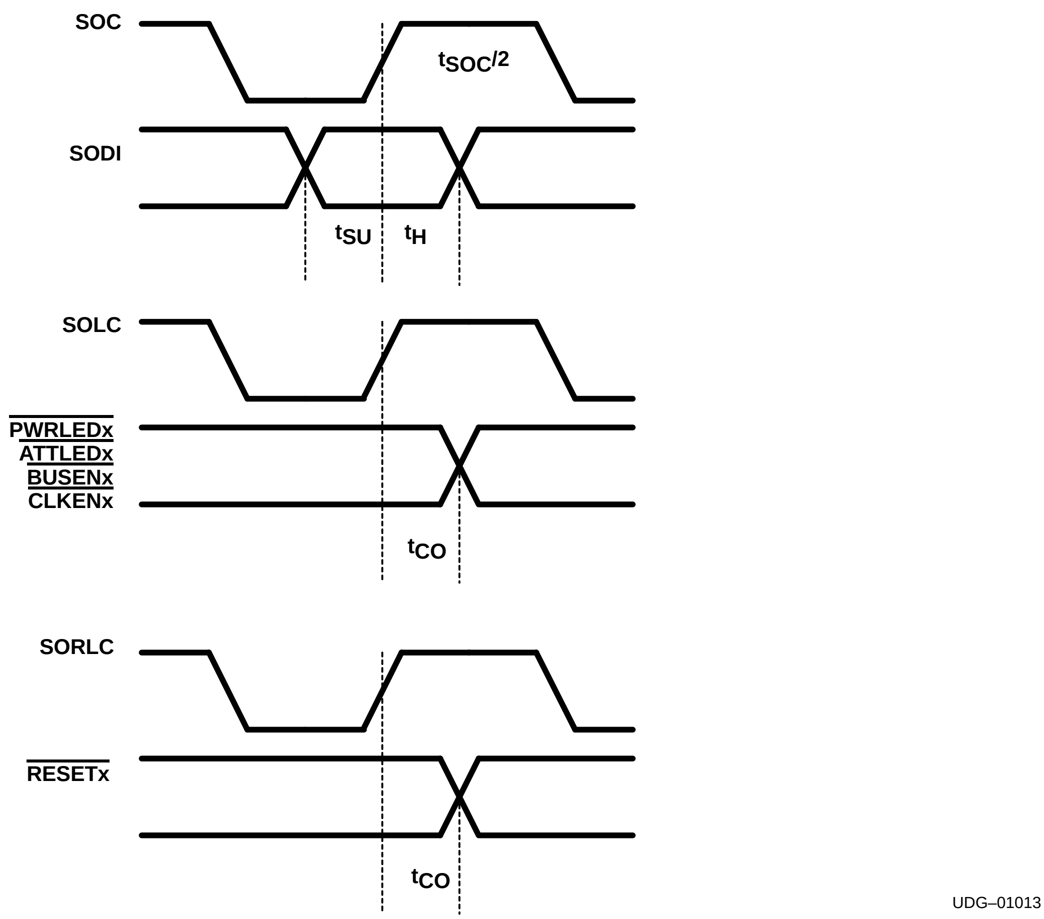


Figure 4. Serial Output Data Timing

APPLICATION INFORMATION

package information

The TPS2340A dissipates very little heat under normal operating conditions. However, when the TPS2340A is used with a load that exceeds PCI specifications either due to a fault or a specification violation, power dissipation increases as the square of load current. To allow reliable operation with high power dissipation, the TPS2340A is packaged in a PowerPAD™ molded quad flat pack with heat-conducting tab on the underside. This package offers thermal resistance from junction to case of approximately 8°C/W. In a typical layout, thermal resistance from junction to ambient is approximately 35°C/W.

For optimum heat conduction and system reliability, the heat-conducting tab should be soldered directly to a 10-mm square copper area on the circuit board tied to M12VIN voltage potential. To increase heat conduction, add plated vias to the copper area directly under the part and connect these vias to copper planes around 100% of their perimeter. These vias conduct heat away from the top layer of the circuit board and into other layers and should not use *thermal reliefs* (also known as *thermals* or *webs*). To prevent solder wicking into the vias, the vias should either be drilled to a size small enough to allow complete filling of the vias during hole plating or should be covered by solder mask on the back of the circuit board.

The TPS2340A TQFP–80 package conforms to JEDEC MS–026. For more information on the PowerPAD package, consult TI PowerPAD Technical Brief (SLMA002).

device testability

Table 11. Test Mode Configuration

PGOOD	TEST	SODO/MODE1	SIDO/MODE0	OPERATING MODE
↑	0	MODE1	MODE0	Normal operation mode, latch MODE inputs
1	0	SODO	SIDO	Normal operation mode, drive SODO and SIDO
↑	1	0	0	NAND tree test mode
↑	1	0	1	Tri–state test mode (all pins tri-stated)
↑	1	1	X	Reserved
1	1	SODO	SIDO	Normal operation, but Pwrenx driven on $\overline{\text{PWRLEDx}}$, $\overline{\text{Faultx}}$ driven on $\overline{\text{ATTLEDx}}$.

NOTE: X = Don’t care, x = slot A or B; shaded cells signify test modes.

When TEST is asserted *after* PGOOD is asserted, the device enters a run-time test mode. When this test mode is enabled, the slot-specific $\overline{\text{PWRLEDx}}$ output asserts when the slot’s internal Pwrenx signal is asserted. Similarly, the $\overline{\text{ATTLEDx}}$ output asserts when the corresponding ANDed slot $\overline{\text{Faultx}}$ signal is asserted.

APPLICATION INFORMATION

NAND tree test

All bi-directional pins are tri-stated for input mode during the NAND Tree test except SIDO. All inputs except TEST should be forced low then forced high, one signal at a time, in the order listed below. The TEST pin is the last signal in the chain and is forced high then low. The NAND result is driven on the SIDO output pin as shown in the timing diagram in Figure 5.

Table 12. NAND Tree Order

	NAND TREE ORDER	PIN NO.
1	SIDI	20
2	SODO	19
3	SWA	46
4	SWB	14
5	$\overline{\text{PRSNT1A}}$	37
6	$\overline{\text{PRSNT1B}}$	24
7	$\overline{\text{PRSNT2A}}$	36
8	$\overline{\text{PRSNT2B}}$	25
9	$\overline{\text{BUTTONA}}$	45
10	$\overline{\text{BUTTONB}}$	15
11	M66ENA	34
12	M66ENB	27
13	PCI–XCAPA	50
14	PCI–XCAPB	11
15	SODI	42
16	SOC	17
17	$\overline{\text{SOR}}$	40
18	$\overline{\text{SORR}}$	21
19	SOLC	39
20	SORLC	22
21	$\overline{\text{BUSENA}}$	32
22	$\overline{\text{BUSENB}}$	29
23	$\overline{\text{CLKENA}}$	33
24	$\overline{\text{CLKENB}}$	28
25	$\overline{\text{RESETA}}$	35
26	$\overline{\text{RESETB}}$	26
27	$\overline{\text{PWRLEDA}}$	48
28	$\overline{\text{PWRLEDB}}$	12
29	$\overline{\text{ATTLEDA}}$	47
30	$\overline{\text{ATTLEDB}}$	13
31	$\overline{\text{SIL}}$	16
32	SIC	44
33	TEST	23

APPLICATION INFORMATION

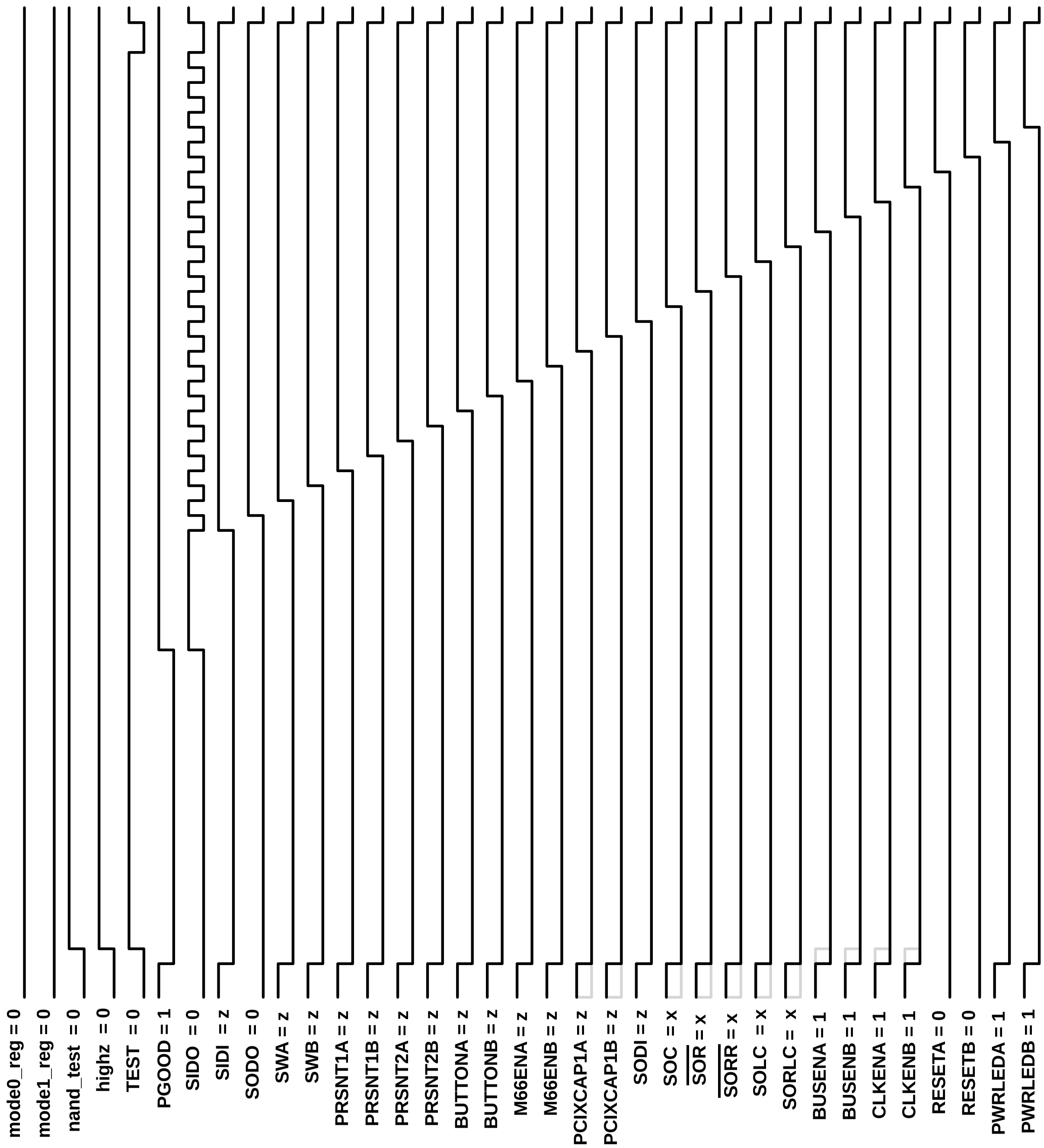


Figure 5. NAND Tree Representative Waveforms

The TPS2340A is initialized by a low-to-high transition of the PGOOD pin. The following table indicates the electrical power-on state of each slot's output pins.

Table 13. NAND Tree Order

OUTPUT PIN	POWER-ON STATE
$\overline{\text{PWRLED}}$x	1
$\overline{\text{ATTLED}}$x	1
$\overline{\text{BUSEN}}$x	1
$\overline{\text{CLKEN}}$x	1
$\overline{\text{RESET}}$x	0

The TPS2340A supports tri-state and NAND–tree test functions.

package dimensions

This package has an exposed copper heat-conducting pad on the bottom of the mold. This pad is approximately 6 mm^2, with maximum dimensions 6.07 mm $\times$ 6.07 mm

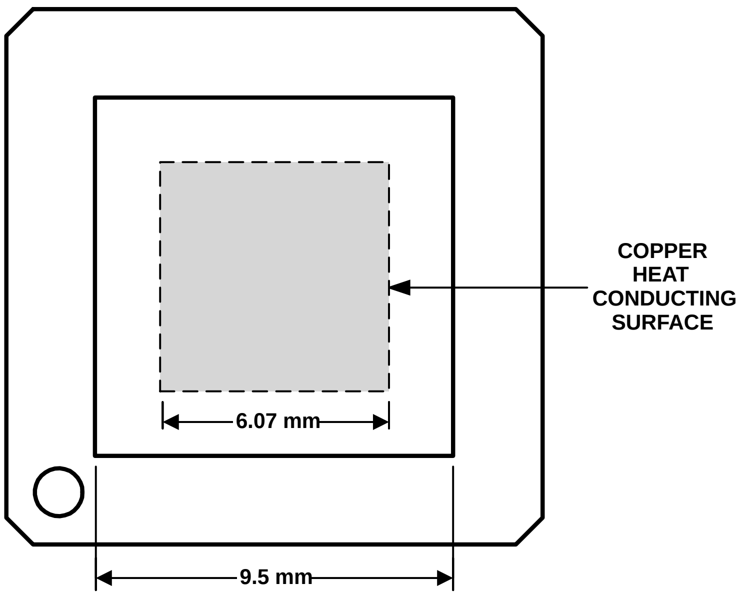
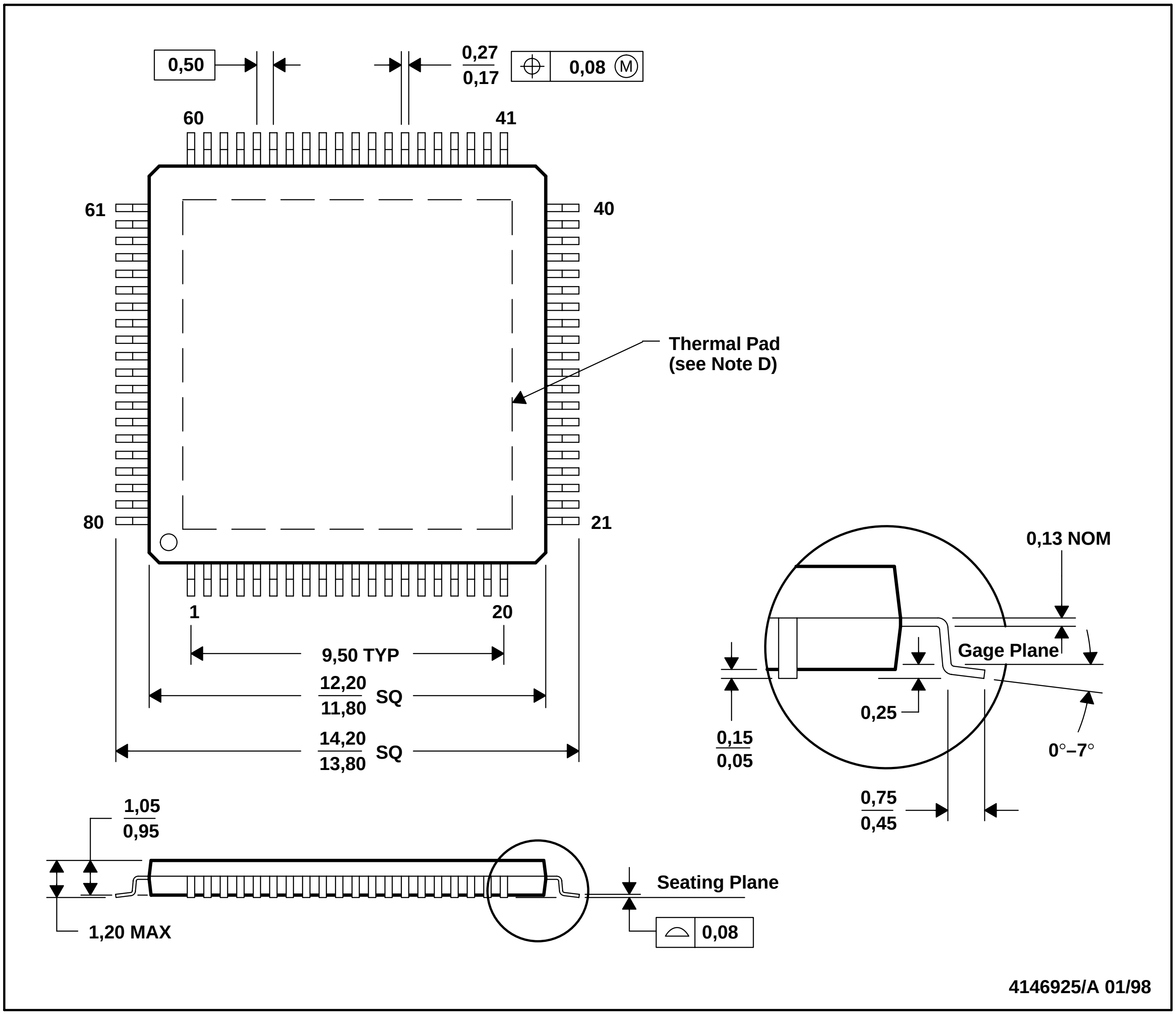


Figure 6. PowerPAD Package Details Bottom View

PFP (S-PQFP-G80) **PowerPAD™ PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MS-026

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TPS2340APFP	ACTIVE	HTQFP	PFP	80	96	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TPS2340APFPG4	ACTIVE	HTQFP	PFP	80	96	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TPS2340APFPR	ACTIVE	HTQFP	PFP	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TPS2340APFPRG4	ACTIVE	HTQFP	PFP	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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