

MC74HC1G32

Single 2-Input OR Gate

The MC74HC1G32 is a high speed CMOS 2-input OR gate fabricated with silicon gate CMOS technology.

The internal circuit is composed of multiple stages, including a buffer output which provides high noise immunity and stable output.

The MC74HC1G32 output drive current is 1/2 compared to MC74HC series.

- High Speed: $t_{PD} = 7$ ns (Typ) at $V_{CC} = 5$ V
- Low Power Dissipation: $I_{CC} = 1$ μ A (Max) at $T_A = 25^\circ\text{C}$
- High Noise Immunity
- Balanced Propagation Delays ($t_{pLH} = t_{pHL}$)
- Symmetrical Output Impedance ($I_{OH} = I_{OL} = 2$ mA)
- Chip Complexity: FET = 44

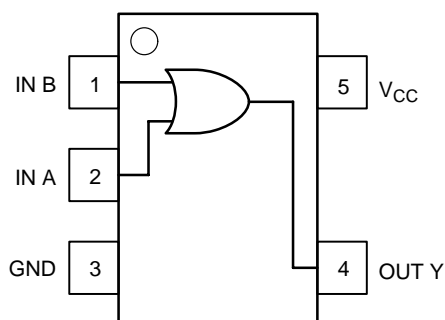


Figure 1. Pinout

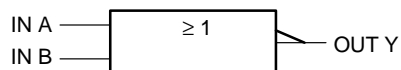
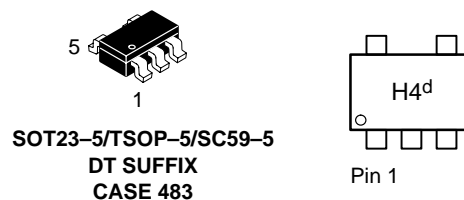
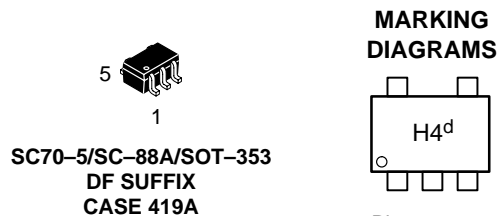


Figure 2. Logic Symbol



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d = Date Code

PIN ASSIGNMENT	
1	IN B
2	IN A
3	GND
4	OUT Y
5	V_{CC}

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

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MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	-0.5 to +7.0	V
V _{IN}	DC Input Voltage	-0.5 to V _{CC} + 0.5	V
V _{OUT}	DC Output Voltage	-0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	±20	mA
I _{OK}	DC Output Diode Current	±20	mA
I _{OUT}	DC Output Sink Current	±12.5	mA
I _{CC}	DC Supply Current per Supply Pin	±25	mA
T _{STG}	Storage Temperature Range	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T _J	Junction Temperature Under Bias	+150	°C
θ _{JA}	Thermal Resistance	SC70-5/SC-88A/SOT-353 (Note 1) SOT23-5/TSOP-5/SC59-5 350 230	°C/W
P _D	Power Dissipation in Still Air at 85°C	SC70-5/SC-88A/SOT-353 SOT23-5/TSOP-5/SC59-5 150 200	mW
MSL	Moisture Sensitivity	Level 1	
F _R	Flammability Rating	Oxygen Index: 28 to 34 UL 94 V-0 @ 0.125 in	
V _{ESD}	ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4) >2000 >200 N/A	V
I _{LATCH-UP}	Latch-Up Performance	Above V _{CC} and Below GND at 125°C (Note 5) ±500	mA

Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 20 ounce copper trace with no air flow.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage	2.0	6.0	V	
V _{IN}	DC Input Voltage	0.0	V _{CC}	V	
V _{OUT}	DC Output Voltage	0.0	V _{CC}	V	
T _A	Operating Temperature Range	-55	+125	°C	
t _r , t _f	Input Rise and Fall Time	V _{CC} = 2.0 V V _{CC} = 3.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0 0	1000 600 500 400	ns

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

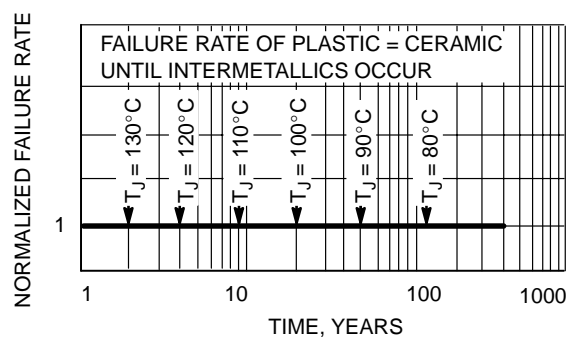


Figure 3. Failure Rate vs. Time Junction Temperature

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V _{CC} (V)	T _A = 25°C			T _A ≤ 85°C		-55°C ≤ T _A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	Minimum High-Level Input Voltage		2.0	1.5			1.5		1.5		V
			3.0	2.1			2.1		2.1		
			4.5	3.15			3.15		3.15		
			6.0	4.20			4.20		4.20		
V _{IL}	Maximum Low-Level Input Voltage		2.0			0.5		0.5		0.5	V
			3.0			0.9		0.9		0.9	
			4.5			1.35		1.35		1.35	
			6.0			1.80		1.80		1.80	
V _{OH}	Minimum High-Level Output Voltage V _{IN} = V _{IH} or V _{IL}	V _{IN} = V _{IH} or V _{IL} I _{OH} = -20 μA	2.0	1.9	2.0		1.9		1.9		V
			3.0	2.9	3.0		2.9		2.9		
		4.5	4.4	4.5		4.4		4.4			
		6.0	5.9	6.0		5.9		5.9			
V _{OL}	Maximum Low-Level Output Voltage V _{IN} = V _{IH} or V _{IL}	V _{IN} = V _{IH} or V _{IL} I _{OL} = 20 μA	2.0		0.0	0.1		0.1		0.1	V
			3.0		0.0	0.1		0.1		0.1	
		4.5		0.0	0.1		0.1		0.1		
		6.0		0.0	0.1		0.1		0.1		
V _{OL}	Maximum Low-Level Output Voltage V _{IN} = V _{IH} or V _{IL}	V _{IN} = V _{IH} or V _{IL} I _{OL} = 2 mA I _{OL} = 2.6 mA	4.5		0.17	0.26		0.33		0.40	
			6.0		0.18	0.26		0.33		0.40	
I _{IN}	Maximum Input Leakage Current	V _{IN} = 6.0 V or GND	6.0			±0.1		±1.0		±1.0	μA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND	6.0			1.0		10		40	μA

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 6.0 ns)

Symbol	Parameter	Test Conditions	T _A = 25°C			T _A ≤ 85°C		-55°C ≤ T _A ≤ 125°C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A or B to \bar{Y}	V _{CC} = 5.0 V C _L = 15 pF		3.5	15		20		25	ns
		V _{CC} = 2.0 V C _L = 50 pF		20	100		125		155	
		V _{CC} = 3.0 V		12	27		35		90	
		V _{CC} = 4.5 V		8	20		25		35	
		V _{CC} = 6.0 V		7	17		21		26	
t _{TLH} , t _{THL}	Output Transition Time	V _{CC} = 5.0 V C _L = 15 pF		3	10		15		20	ns
		V _{CC} = 2.0 V C _L = 50 pF		25	125		155		200	
		V _{CC} = 3.0 V		16	35		45		60	
		V _{CC} = 4.5 V		11	25		31		38	
		V _{CC} = 6.0 V		9	21		26		32	
C _{IN}	Maximum Input Capacitance			5	10		10		10	pF
C _{PD}	Power Dissipation Capacitance (Note 6)	Typical @ 25°C, V _{CC} = 5.0 V							pF	
		10								

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

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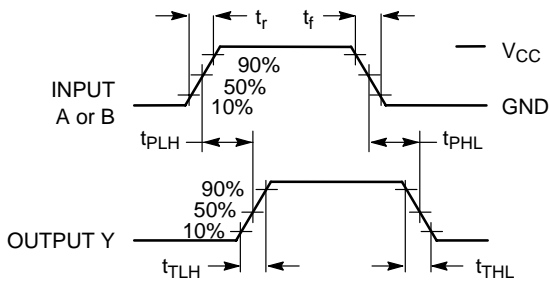
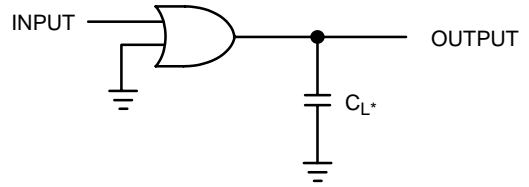


Figure 4. Switching Waveforms



*Includes all probe and jig capacitance.
A 1-MHz square input wave is recommended for propagation delay tests.

Figure 5. Test Circuit

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature						Package Type (Name/SOT#/Common Name)	Tape and Reel Size
	Logic Circuit Indicator	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape and Reel Suffix		
MC74HC1G32DFT1	MC	74	HC1G	32	DF	T1	SC70-5/SC-88A/SOT-353	178 mm (7 in) 3000 Unit
MC74HC1G32DFT2	MC	74	HC1G	32	DF	T2	SC70-5/SC-88A/SOT-353	178 mm (7 in) 3000 Unit
MC74HC1G32DTT1	MC	74	HC1G	32	DT	T1	SOT23-5/TSOP-5/SC59-5	178 mm (7 in) 3000 Unit

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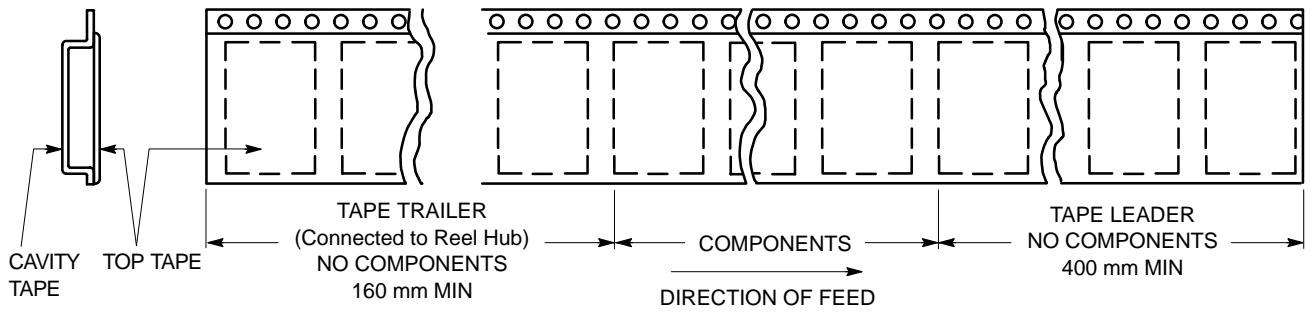


Figure 6. Tape Ends for Finished Goods

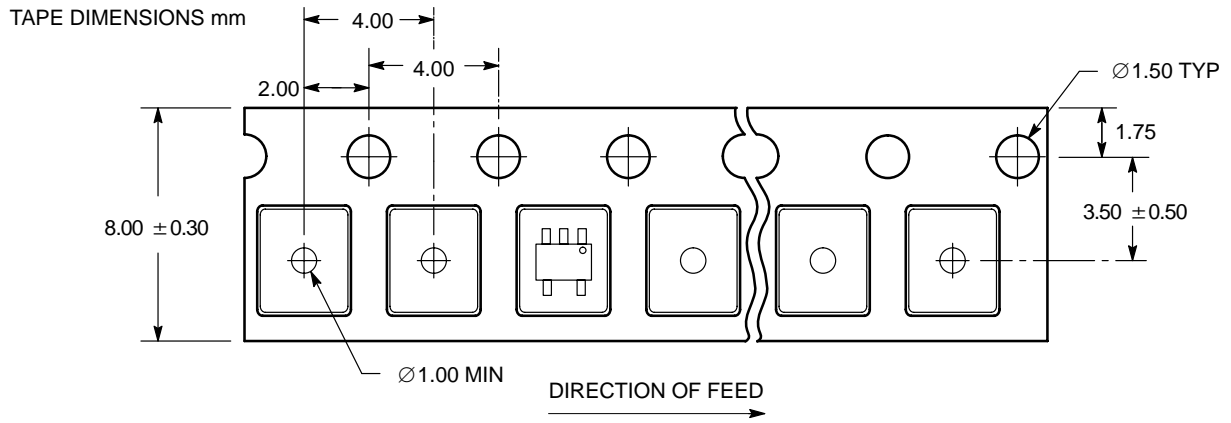


Figure 7. DFT1 Reel Configuration/Orientation

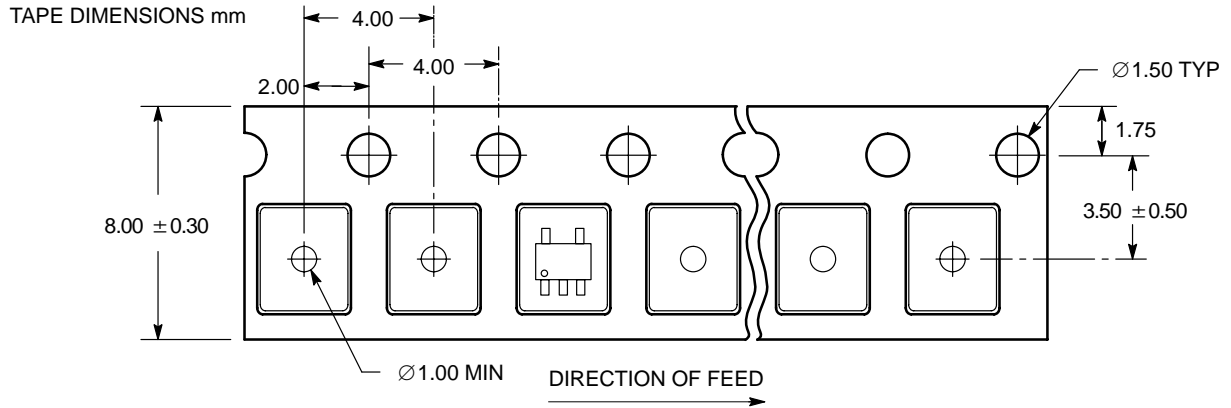


Figure 8. DFT2/DTT1 Reel Configuration/Orientation

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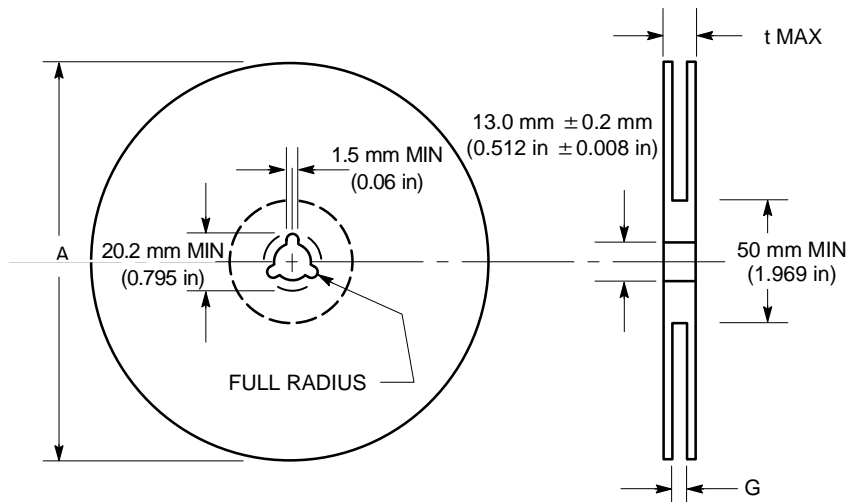


Figure 9. Reel Dimensions

REEL DIMENSIONS

Tape Size	T and R Suffix	A Max	G	t Max
8 mm	T1, T2	178 mm (7 in)	8.4 mm, +1.5 mm, -0.0 (0.33 in +0.059 in, -0.00)	14.4 mm (0.56 in)

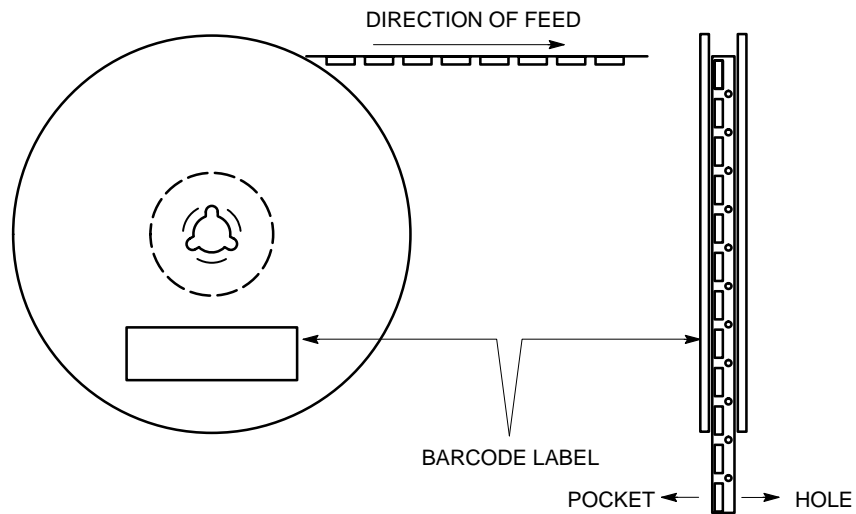
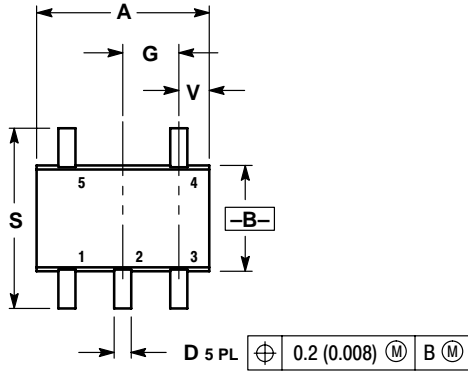


Figure 10. Reel Winding Direction

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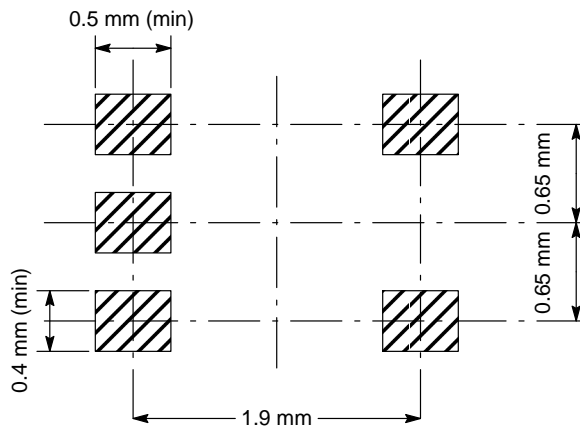
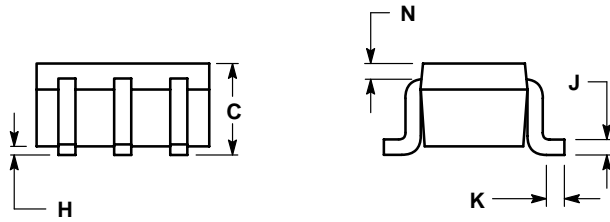
PACKAGE DIMENSIONS

SC70-5/SC-88A/SOT-353
 DF SUFFIX
 5-LEAD PACKAGE
 CASE 419A-01
 ISSUE E



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

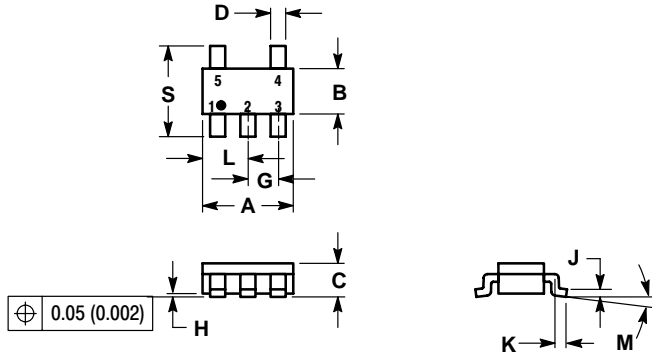
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20
V	0.012	0.016	0.30	0.40



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PACKAGE DIMENSIONS

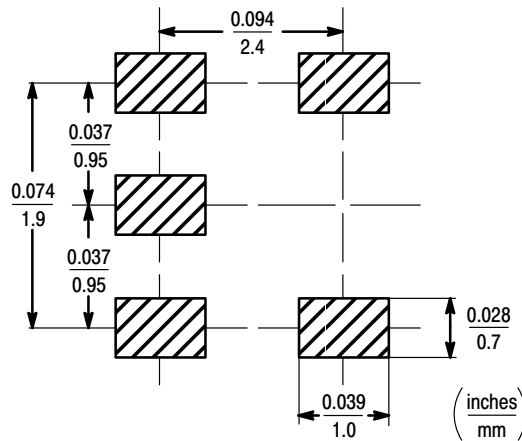
SOT23-5/TSOP-5/SC59-5
DT SUFFIX
5-LEAD PACKAGE
CASE 483-01
ISSUE B




NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.05	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0°	10°	0°	10°
S	2.50	3.00	0.0985	0.1181



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