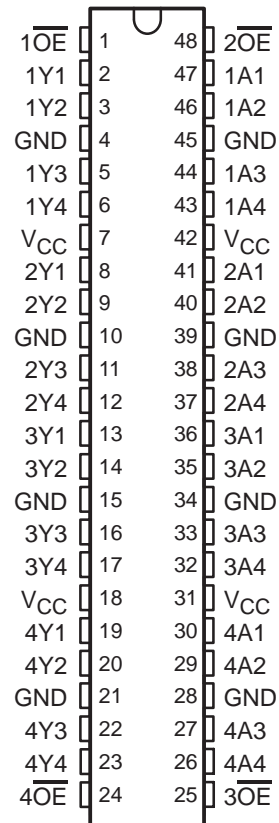


# SN74LVCH162244A 16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCAS545K – OCTOBER 1995 – REVISED OCTOBER 2003

- Member of the Texas Instruments Widebus™ Family
- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 4.4 ns at 3.3 V
- Output Ports Have Equivalent 26- $\Omega$  Series Resistors, So No External Resistors Are Required
- Typical  $V_{OLP}$  (Output Ground Bounce) <0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) >2 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V  $V_{CC}$ )
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

DL, DGG, OR DGV PACKAGE  
(TOP VIEW)



## description/ordering information

This 16-bit buffer/driver is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74LVCH162244A is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides true outputs and symmetrical active-low output-enable ( $\overline{OE}$ ) inputs.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP – DL	Tube	SN74LVCH162244ADL	LVCH162244A
		Tape and reel	SN74LVCH162244ADLR	
	TSSOP – DGG	Tape and reel	SN74LVCH162244AGR	LVCH162244A
	TVSOP – DGV	Tape and reel	SN74LVCH162244AVR	LN2244A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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## 16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

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### description/ordering information (continued)

The outputs, which are designed to sink up to 12 mA, include equivalent 26-Ω resistors to reduce overshoot and undershoot.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

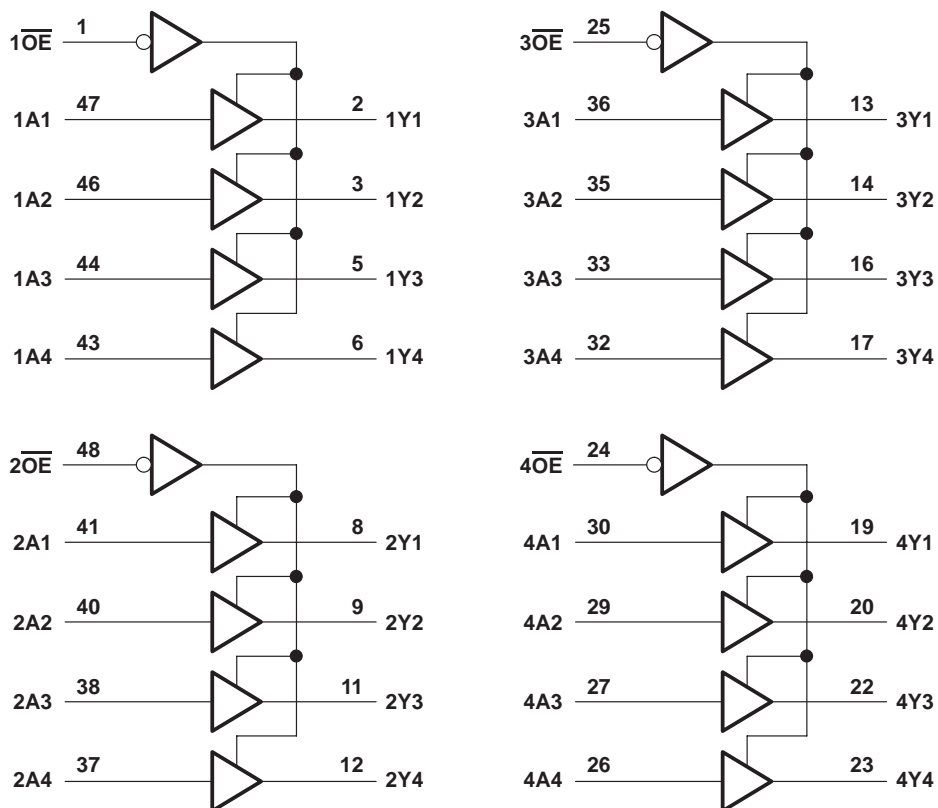
To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

FUNCTION TABLE  
(each 4-bit buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

### logic diagram (positive logic)



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## 16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	–0.5 V to 6.5 V
Input voltage range, $V_I$ (see Note 1) .....	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1) .....	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, $V_O$ (see Notes 1 and 2) .....	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	–50 mA
Continuous output current, $I_O$ .....	±50 mA
Continuous current through each $V_{CC}$ or GND .....	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DGG package .....	70°C/W
DGV package .....	58°C/W
DL package .....	63°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The value of  $V_{CC}$  is provided in the recommended operating conditions table.  
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
$V_{CC}$ Supply voltage	Operating	1.65	3.6	V
	Data retention only	1.5		
$V_{IH}$ High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V	1.7		
	$V_{CC} = 2.7$ V to 3.6 V	2		
$V_{IL}$ Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V		$0.35 \times V_{CC}$	V
	$V_{CC} = 2.3$ V to 2.7 V		0.7	
	$V_{CC} = 2.7$ V to 3.6 V		0.8	
$V_I$ Input voltage		0	5.5	V
$V_O$ Output voltage	High or low state	0	$V_{CC}$	V
	3-state	0	5.5	
$I_{OH}$ High-level output current	$V_{CC} = 1.65$ V		–2	mA
	$V_{CC} = 2.3$ V		–4	
	$V_{CC} = 2.7$ V		–8	
	$V_{CC} = 3$ V		–12	
$I_{OL}$ Low-level output current	$V_{CC} = 1.65$ V		2	mA
	$V_{CC} = 2.3$ V		4	
	$V_{CC} = 2.7$ V		8	
	$V_{CC} = 3$ V		12	
$\Delta t/\Delta v$ Input transition rise or fall rate			10	ns/V
$T_A$ Operating free-air temperature		–40	85	°C

NOTE 4: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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**16-BIT BUFFER/DRIVER**  
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP†	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = -100 μA	1.65 V to 3.6 V	V <sub>CC</sub> -0.2			V
	I <sub>OH</sub> = -2 mA	1.65 V	1.2			
	I <sub>OH</sub> = -4 mA	2.3 V	1.7			
		2.7 V	2.2			
	I <sub>OH</sub> = -6 mA	3 V	2.4			
	I <sub>OH</sub> = -8 mA	2.7 V	2			
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V			0.2	V
	I <sub>OL</sub> = 2 mA	1.65 V			0.45	
	I <sub>OL</sub> = 4 mA	2.3 V			0.7	
		2.7 V			0.4	
	I <sub>OL</sub> = 6 mA	3 V			0.55	
	I <sub>OL</sub> = 8 mA	2.7 V			0.6	
I <sub>I</sub>	V <sub>I</sub> = 0 to 5.5 V	3.6 V			±5	μA
I <sub>I(hold)</sub>	V <sub>I</sub> = 0.58 V	1.65 V	‡			μA
	V <sub>I</sub> = 1.07 V	1.65 V	‡			
	V <sub>I</sub> = 0.7 V	2.3 V	45			
	V <sub>I</sub> = 1.7 V	2.3 V	-45			
	V <sub>I</sub> = 0.8 V	3 V	75			
	V <sub>I</sub> = 2 V	3 V	-75			
	V <sub>I</sub> = 0 to 3.6 V§	3.6 V			±500	
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0			±10	μA
I <sub>OZ</sub>	V <sub>O</sub> = 0 to 5.5 V	3.6 V			±10	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	I <sub>O</sub> = 0			20	μA
	3.6 V ≤ V <sub>I</sub> ≤ 5.5 V¶				20	
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V			500	μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V			5.5	pF
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V			6	pF

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

‡ This information was not available at the time of publication.

§ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

¶ This applies in the disabled state only.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	1	10.2	1	6.4	1	5.6	1.1	4.4	ns
t <sub>en</sub>	$\overline{OE}$	Y	1	14.8	1	8.2	1	6.9	1	5.5	ns
t <sub>dis</sub>	$\overline{OE}$	Y	1	12.3	1	7.1	1	6.8	1.8	6.3	ns



**SN74LVCH162244A**  
**16-BIT BUFFER/DRIVER**  
**WITH 3-STATE OUTPUTS**

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**operating characteristics,  $T_A = 25^\circ\text{C}$**

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	UNIT
			TYP	TYP	TYP	
C <sub>pd</sub>	Power dissipation capacitance per buffer/driver	Outputs enabled	†	†	35	pF
		Outputs disabled	†	†	4	

† This information was not available at the time of publication.



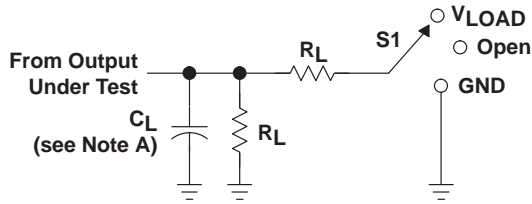
# SN74LVCH162244A

## 16-BIT BUFFER/DRIVER

### WITH 3-STATE OUTPUTS

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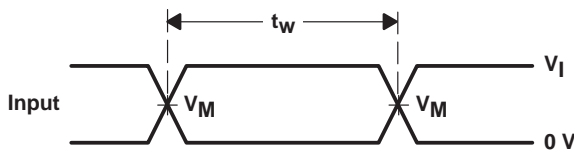
#### PARAMETER MEASUREMENT INFORMATION



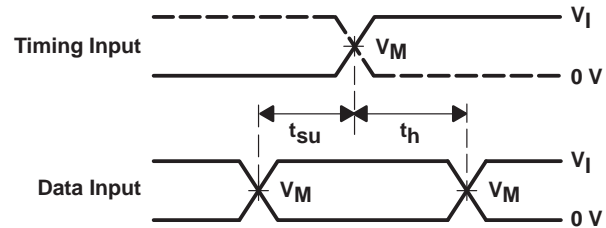
LOAD CIRCUIT

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

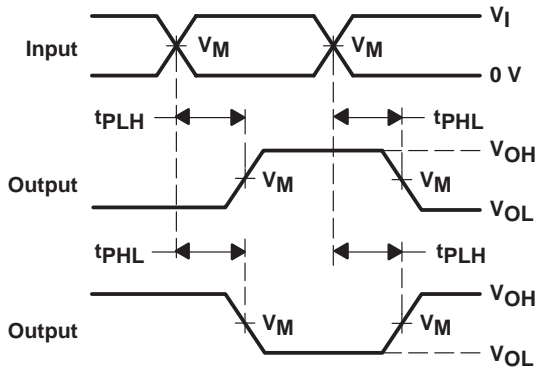
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V



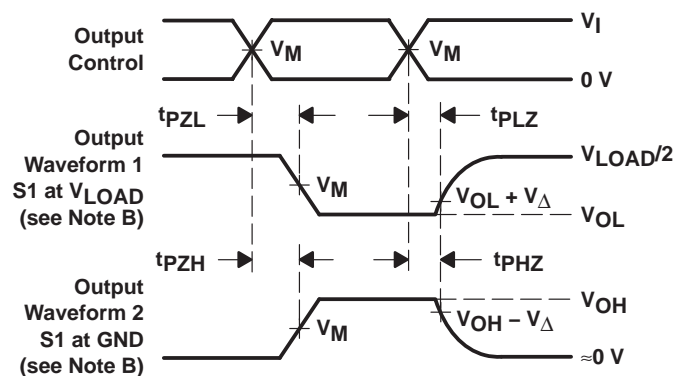
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

DL (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MO-118



DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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