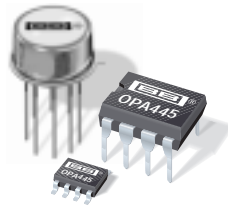




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OPA445

High Voltage FET-Input OPERATIONAL AMPLIFIER

FEATURES

- WIDE-POWER SUPPLY RANGE: $\pm 10V$ to $\pm 45V$
- HIGH SLEW RATE: $15V/\mu s$
- LOW INPUT BIAS CURRENT: $10pA$
- STANDARD-PINOUT TO-99, DIP, AND SURFACE-MOUNT PACKAGES

APPLICATIONS

- TEST EQUIPMENT
- HIGH-VOLTAGE REGULATORS
- POWER AMPLIFIERS
- DATA ACQUISITION
- SIGNAL CONDITIONING
- AUDIO
- PIEZO DRIVERS

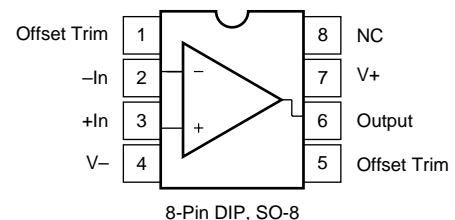
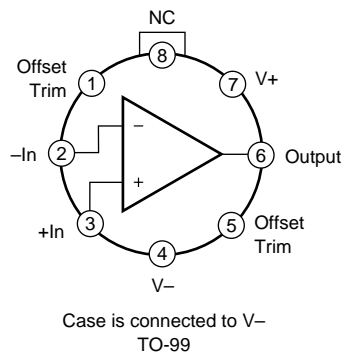
DESCRIPTION

The OPA445 is a monolithic operational amplifier capable of operation from power supplies up to $\pm 45V$ and output currents of $15mA$. It is useful in a wide variety of applications requiring high output voltage or large common-mode voltage swings.

The OPA445's high slew rate provides wide power-bandwidth response, which is often required for high-voltage applications. FET input circuitry allows the use of high-impedance feedback networks, thus mini-

mizing their output loading effects. Laser trimming of the input circuitry yields low input offset voltage and drift.

The OPA445 is available in standard pin-out TO-99, DIP-8, and SO-8 surface-mount packages. It is fully specified from $-25^{\circ}C$ to $+85^{\circ}C$ and operates from $-55^{\circ}C$ to $+125^{\circ}C$. A SPICE macromodel is available for design analysis.



SPECIFICATIONS

At $T_A = +25^\circ\text{C}$, $V_S = \pm 40\text{V}$, and $R_L = 5\text{k}\Omega$, unless otherwise specified.

Boldface limits apply over the specified temperature range, $T_A = -25^\circ\text{C}$ to $+85^\circ\text{C}$. $V_S = \pm 40\text{V}$.

PARAMETER	CONDITIONS	OPA445BM			OPA445AP, AU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE Input Offset Voltage vs Temperature vs Power Supply	V_{OS} V_{OS}/dT PSRR $V_{CM} = 0, I_O = 0$ $T_A = -25^\circ\text{C}$ to $+85^\circ\text{C}$ $V_S = \pm 10\text{V}$ to $\pm 45\text{V}$		± 1 ± 10 4	± 3 100		± 1.5 **	± 5 **	mV $\mu\text{V}/^\circ\text{C}$ $\mu\text{V}/\text{V}$
INPUT BIAS CURRENT⁽¹⁾ Input Bias Current Over Specified Temperature Range Input Offset Current Over Specified Temperature Range	I_B $V_{CM} = 0\text{V}$ I_{OS} $V_{CM} = 0\text{V}$		± 10 ± 4	± 50 ± 10 ± 20 ± 5		* *	± 100 ± 20 ± 40 ± 10	pA nA pA nA
NOISE Input Voltage Noise Density, $f = 1\text{kHz}$ Current Noise Density, $f = 1\text{kHz}$	e_n i_n		15 6			* *		$\text{nV}/\sqrt{\text{Hz}}$ $\text{fA}/\sqrt{\text{Hz}}$
INPUT VOLTAGE RANGE Common-Mode Voltage Range Common-Mode Rejection Over Specified Temperature Range	V_{CM} CMRR $V_S = \pm 40\text{V}$ $V_{CM} = -35\text{V}$ to $+35\text{V}$		(V-)+5 80 80	95	(V+)-5	* * *	* *	V dB dB
INPUT IMPEDANCE Differential Common-Mode			$10^{13} \parallel 1$ $10^{14} \parallel 3$			* *		$\Omega \parallel \text{pF}$ $\Omega \parallel \text{pF}$
OPEN-LOOP GAIN, DC Open-Loop Voltage Gain Over Specified Temperature Range	A_{OL} $V_O = -35\text{V}$ to $+35\text{V}$		100 97	110		* *		dB dB
FREQUENCY RESPONSE Gain Bandwidth Product Slew Rate Full Power Bandwidth Rise Time Overshoot Total Harmonic Distortion + Noise	GBW SR $V_O = 70\text{Vp-p}$ $V_O = 70\text{Vp-p}$ $V_O = \pm 200\text{mV}$ $G = +1, Z_L = 5\text{k}\Omega \parallel 50\text{pF}$ THD+N $f = 1\text{kHz}, V_O = 3.5\text{Vrms}, G = 1$ $f = 1\text{kHz}, V_O = 10\text{Vrms}, G = 1$		5 23	2 15 70 100 35 0.0002 0.00008		* * * * * *	* * * * * *	MHz $\text{V}/\mu\text{s}$ kHz ns % % %
OUTPUT Voltage Output Over Specified Temperature Range Current Output Output Resistance, Open Loop Short Circuit Current Capacitive Load Drive	V_O I_O R_O I_{SC} C_{LOAD} $V_O = \pm 28\text{V}$ dc		(V-)+5 (V-)+5 ± 15		(V+)-5 (V+)-5	* * *	* * * * *	V V mA Ω mA
POWER SUPPLY Specified Operating Range Operating Voltage Range Quiescent Current	V_S I_Q $I_O = 0$		± 10	± 40 ± 4.2	± 45 ± 4.7	* *	* *	V V mA
TEMPERATURE RANGE Specification Range Operating Range Storage Range Thermal Resistance TO-99 8-Pin DIP SO-8 Surface-Mount	θ_{JA}		-25 -55 -65		+85 +125 +125	* * -55	* * +125	$^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$

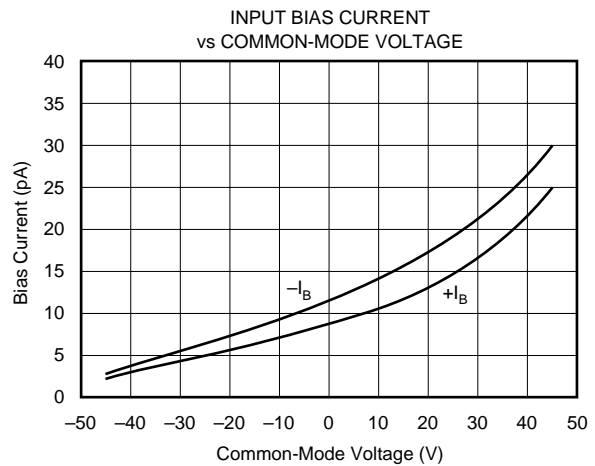
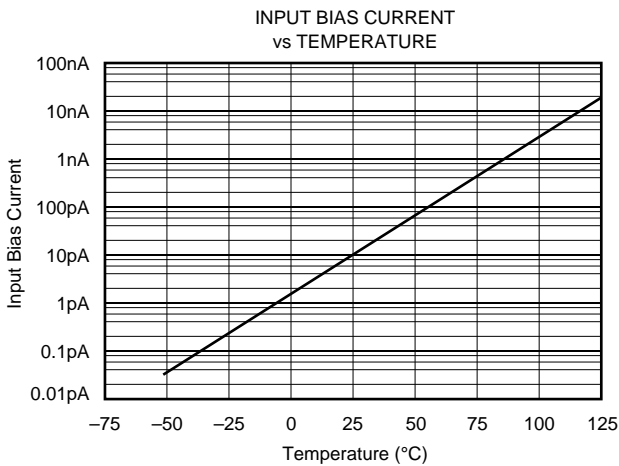
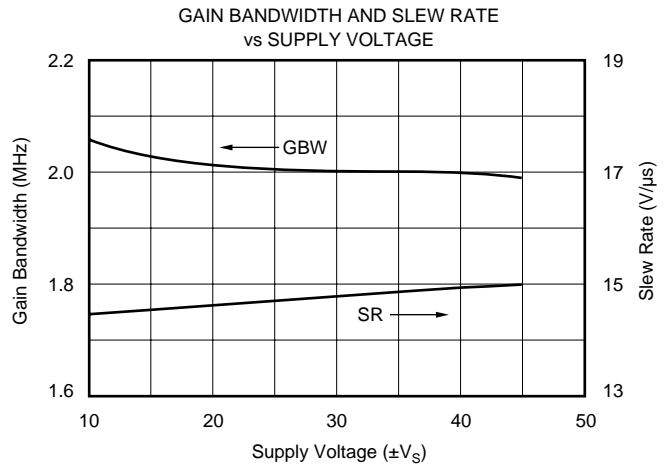
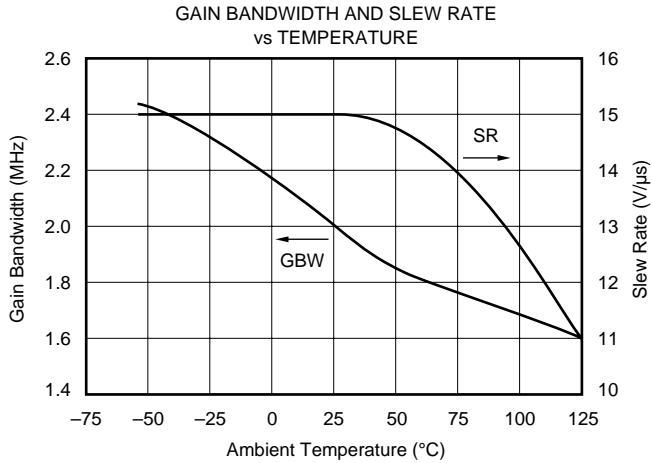
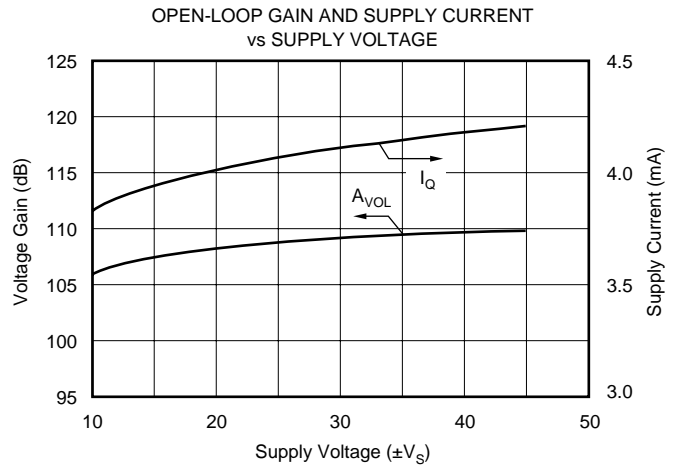
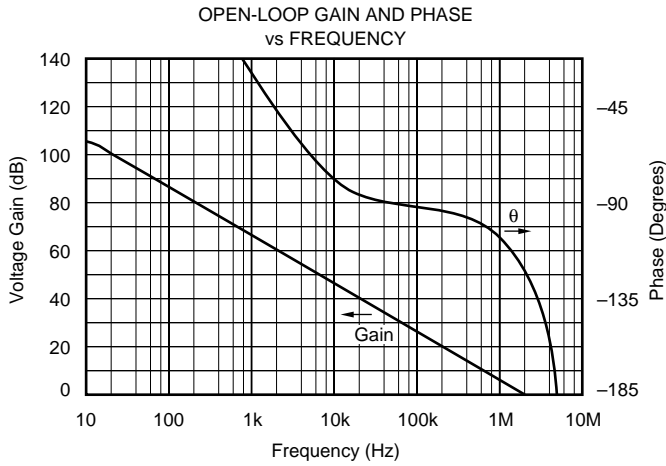
* Specifications same as OPA445BM.

NOTE: (1) High-speed test at $T_J = +25^\circ\text{C}$. (2) See "Small-Signal Overshoot vs Load Capacitance" in the Typical Performance Curves section.

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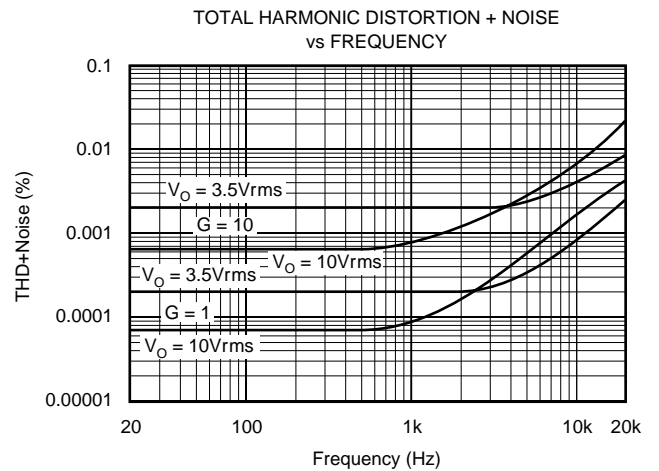
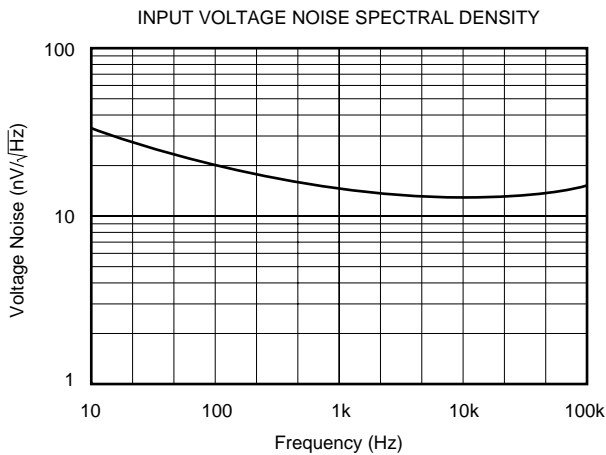
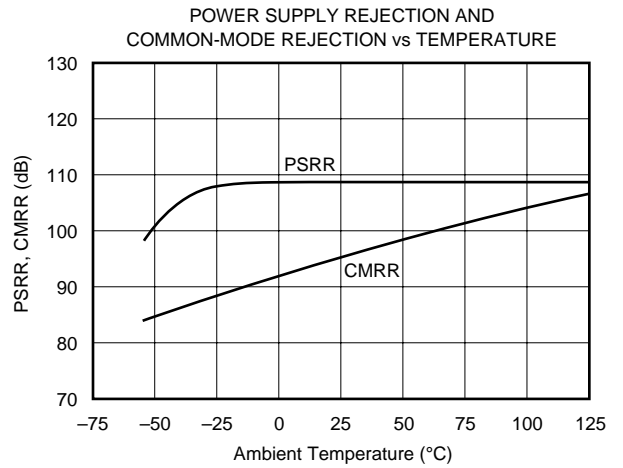
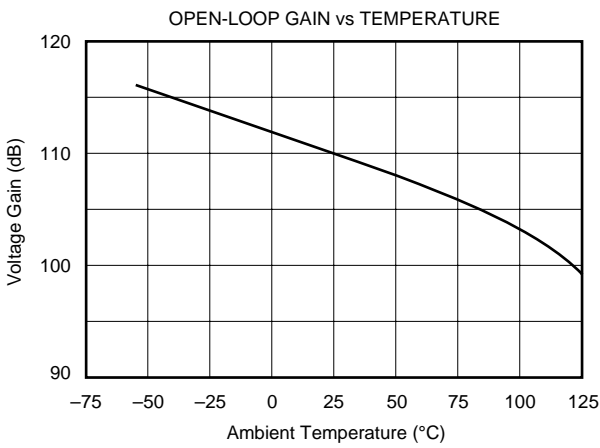
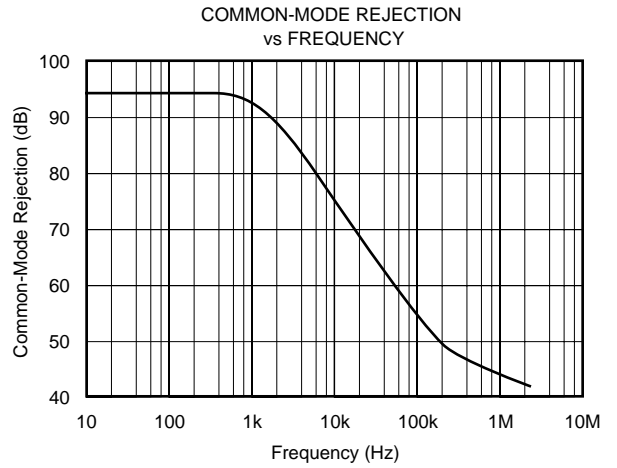
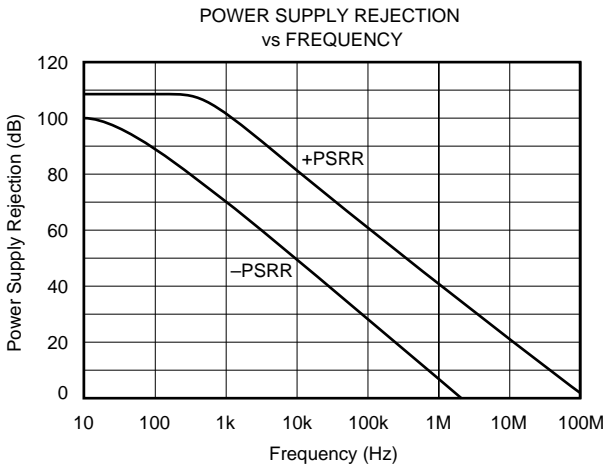
TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$, $V_S = \pm 40\text{V}$, unless otherwise noted.



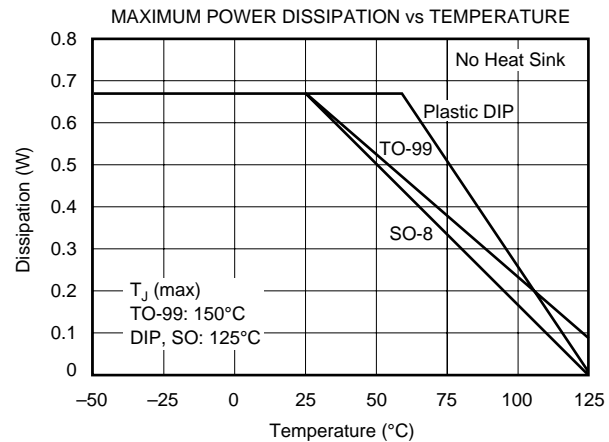
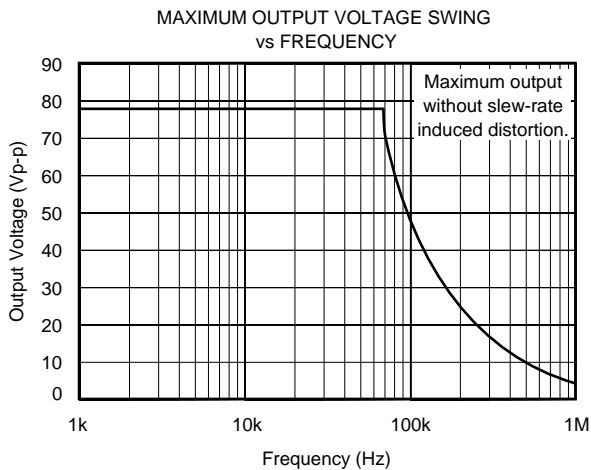
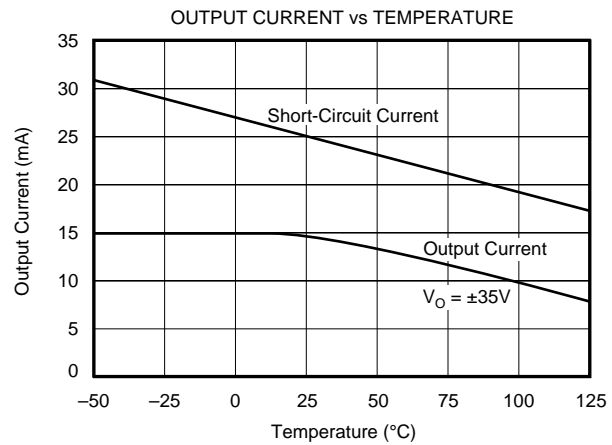
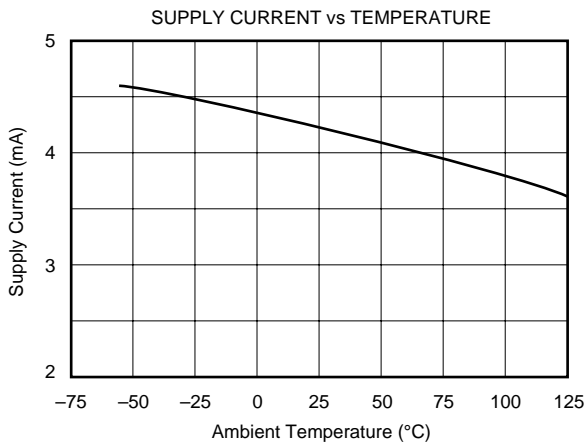
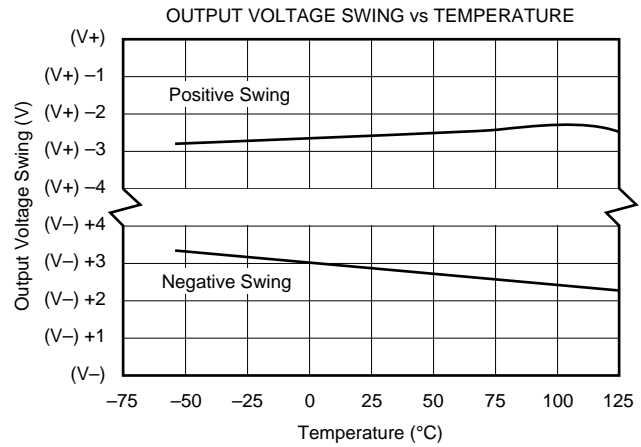
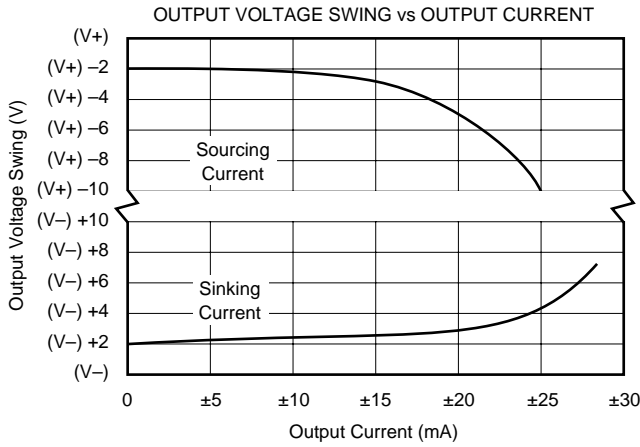
TYPICAL PERFORMANCE CURVES (Cont.)

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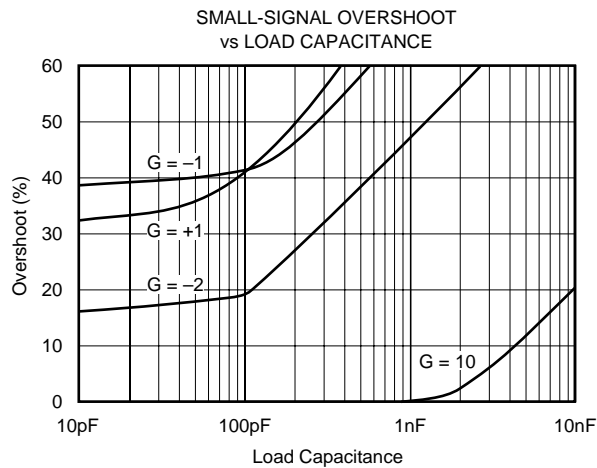
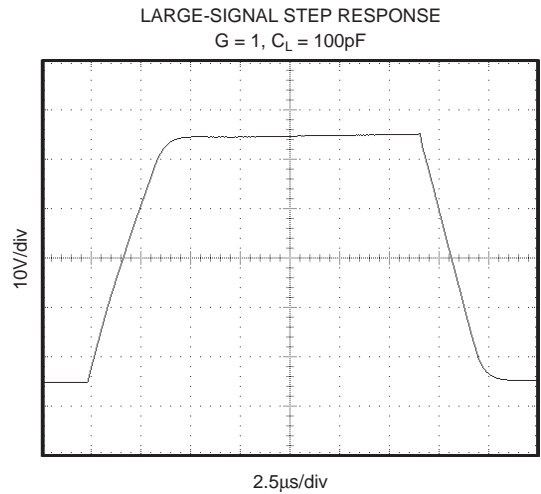
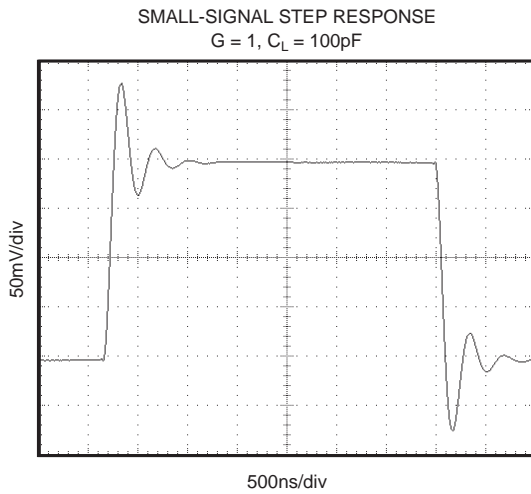
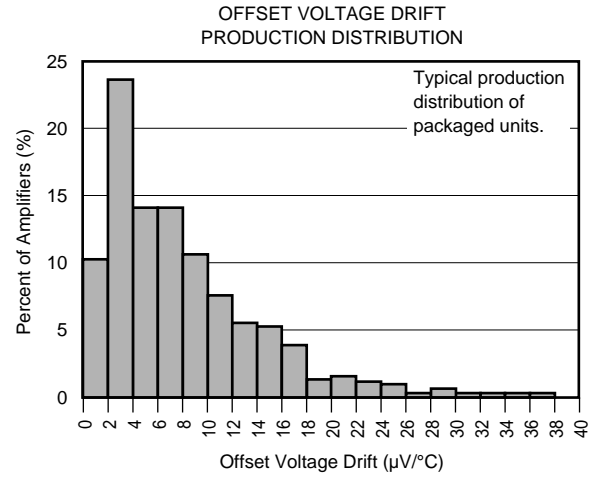
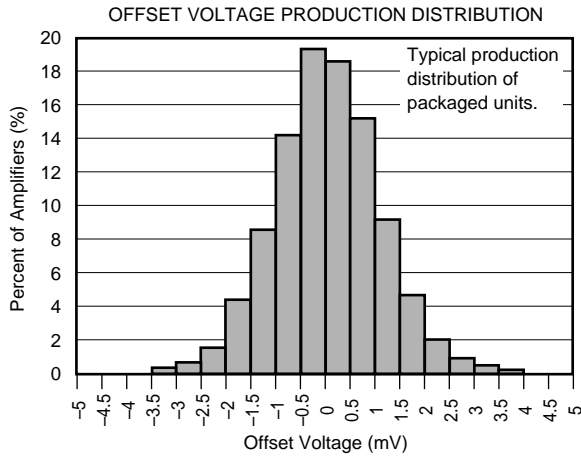
TYPICAL PERFORMANCE CURVES (Cont.)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 40\text{V}$, unless otherwise noted.



TYPICAL PERFORMANCE CURVES (Cont.)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 40\text{V}$, unless otherwise noted.



APPLICATION INFORMATION

Figure 1 shows the OPA445 connected as a basic non-inverting amplifier. The OPA445 can be used in virtually any op amp configuration.

Power supply terminals should be bypassed with 0.1µF capacitors, or greater, near the power supply pins. Be sure that the capacitors are appropriately rated for the power supply voltage used.

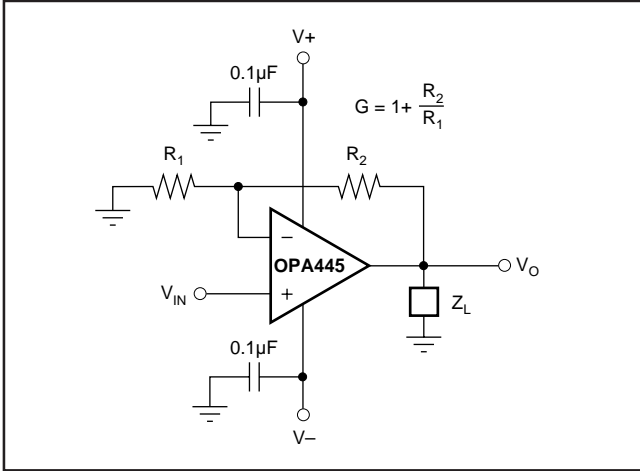


FIGURE 1. Offset Voltage Trim.

POWER SUPPLIES

The OPA445 may be operated from power supplies up to ±45V or a total of 90V with excellent performance. Most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in the typical performance curves.

Some applications do not require equal positive and negative output voltage swing. Power supply voltages do not need to be equal. The OPA445 can operate with as little as 20V between the supplies and with up to 90V between the supplies. For example, the positive supply could be set to 80V with the negative supply at -10V, or vice-versa.

OFFSET VOLTAGE TRIM

The OPA445 provides offset voltage trim connections on pins 1 and 5. Offset voltage can be adjusted by connecting a potentiometer as shown in Figure 2. This adjustment should be used only to null the offset of the op amp, not to adjust system offset or offset produced by the signal source. Nulling system offset could degrade the offset voltage drift behavior of the op amp. While it is not possible to predict the exact change in drift, the effect is usually small.

SAFE OPERATING AREA

Stress on the output transistors is determined both by the output current and by the output voltage across the conducting output transistors, $V_S - V_O$. The power dissipated by the

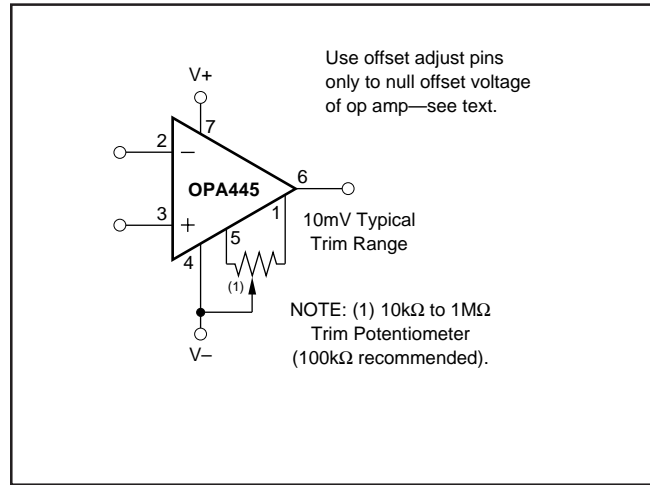


FIGURE 2. Offset Voltage Trim.

output transistor is equal to the product of the output current and the voltage across the conducting transistor, $V_S - V_O$. The Safe Operating Area (SOA curve, Figures 3, 4, and 5) shows the permissible range of voltage and current. The curves shown represent devices soldered to a circuit board with no heat sink. Increasing printed circuit trace area or the use of a heat sink (TO-99 package) can significantly reduce thermal resistance (θ), resulting in increased output current for a given output voltage (see “Heat Sink” text).

The safe output current decreases as $V_S - V_O$ increases. Output short-circuits are a very demanding case for SOA. A short-circuit to ground forces the full power supply voltage (V_+ or V_-) across the conducting transistor and produces a typical output current of 25mA. With ±40V power supplies, this creates an internal dissipation of 1W. This exceeds the maximum rating and is not recommended. If operation in this region is unavoidable, a heat sink is required. For further insight on SOA, consult Application Bulletin AB-039.

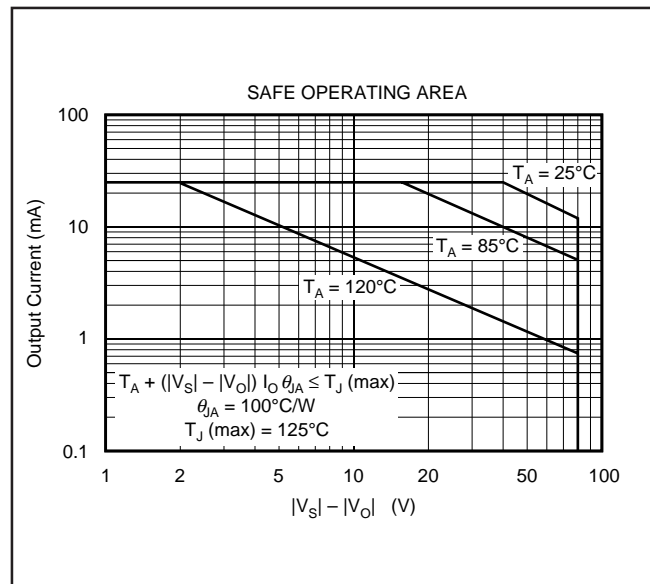


FIGURE 3. 8-Pin DIP Safe Operating Area.

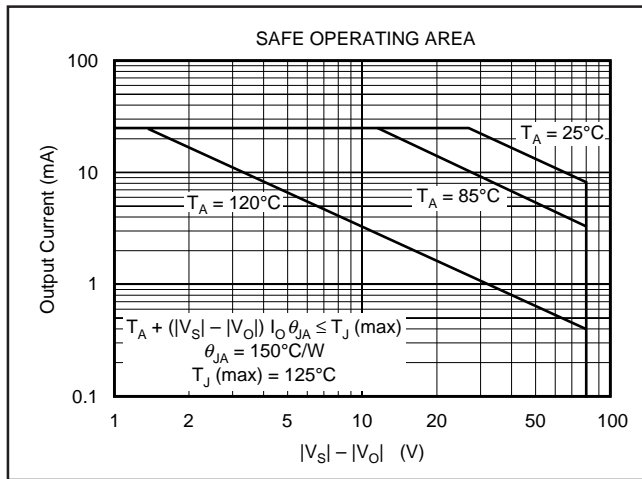


FIGURE 4. SO-8 Safe Operating Area.

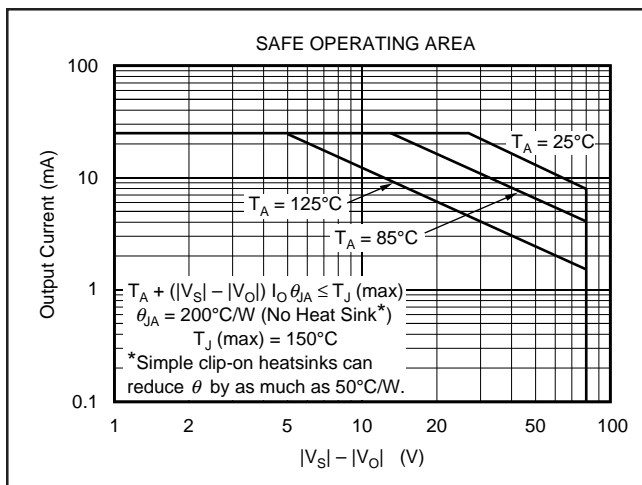


FIGURE 5. TO-99 Safe Operating Area.

POWER DISSIPATION

Power dissipation depends on power supply, signal, and load conditions. For dc signals, power dissipation is equal to the product of the output current times the voltage across the conducting output transistor, $P_D = I_L (V_S - V_O)$. Power dissipation can be minimized by using the lowest possible power supply voltage necessary to assure the required output voltage swing.

For resistive loads, the maximum power dissipation occurs at a dc output voltage of one-half the power supply voltage. Dissipation with ac signals is lower. Application Bulletin AB-039 explains how to calculate or measure dissipation with unusual loads or signals.

The OPA445 can supply output currents of 15mA and larger. This would present no problem for a standard op amp operating from $\pm 15V$ supplies. With high supply voltages, however, internal power dissipation of the op amp can be quite large. Operation from a single power supply (or unbalanced power supplies) can produce even larger power dissipation since a large voltage is impressed across the conducting output transistor. Applications with large power dissipation may require a heat sink.

HEAT SINKING

Power dissipated in the OPA445 will cause the junction temperature to rise. For reliable operation junction temperature should be limited to 125°C, maximum (150°C for TO-99 package). Some applications will require a heat sink to assure that the maximum operating junction temperature is not exceeded. In addition, the junction temperature should be kept as low as possible for increased reliability. Junction temperature can be determined according to the following equation:

$$T_J = T_A + P_D \theta_{JA}$$

Package thermal resistance, θ_{JA} , is affected by mounting techniques and environments. Poor air circulation and use of sockets can significantly increase thermal resistance. Best thermal performance is achieved by soldering the op amp into a circuit board with wide printed circuit traces to allow greater conduction through the op amp leads. Simple clip-on heat sinks (such as Thermalloy 2257) can reduce the thermal resistance of the TO-99 metal package by as much as 50°C/W. For additional information on determining heat sink requirements, consult Applications Bulletin AB-038.

CAPACITIVE LOADS

The dynamic characteristics of the OPA445 have been optimized for commonly encountered gains, loads, and operating conditions. The combination of low closed-loop gain and capacitive load will decrease the phase margin and may lead to gain peaking or oscillations. Figure 6 shows a circuit which preserves phase margin with capacitive load. The circuit does not suffer a voltage drop due to load current, however, input impedance is reduced at high frequencies. Consult Application Bulletin AB-028 for details of analysis techniques and application circuits.

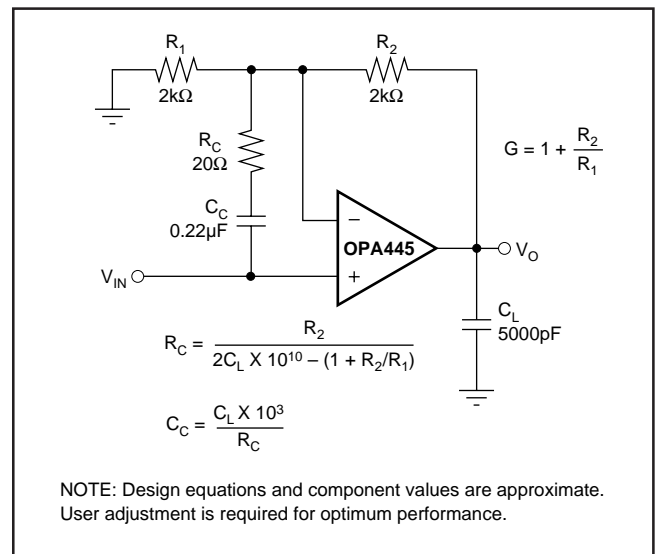


FIGURE 6. Driving Large Capacitive Loads.

INCREASING OUTPUT CURRENT

In those applications where the 15mA of output current is not sufficient to drive the required load, output current can be increased by connecting two or more OPA445s in parallel as shown in Figure 7. Amplifier A1 is the “master” amplifier and may be configured in virtually an op amp circuit. Amplifier A2, the “slave”, is configured as a unity gain buffer. Alternatively, external output transistors can be used to boost output current. The circuit in Figure 8 is capable of supplying output currents up to 1A.

INPUT PROTECTION

The inputs of conventional FET-input op amps should be protected against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. This can occur if the input voltage exceeds the power supplies or there is an input voltage with $V_S = 0V$. Protection is easily accomplished with a resistor in series with the input. Care should be taken because the resistance in series with the input capacitance may affect stability. Many input signals are inherently current-limited, therefore, a limiting resistor may not be required.

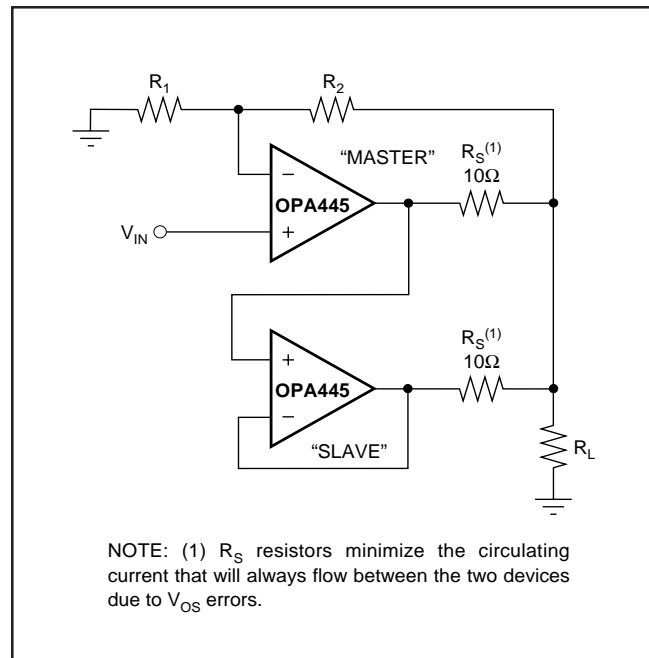


FIGURE 7. Parallel Amplifiers Increase Output Current Capability.

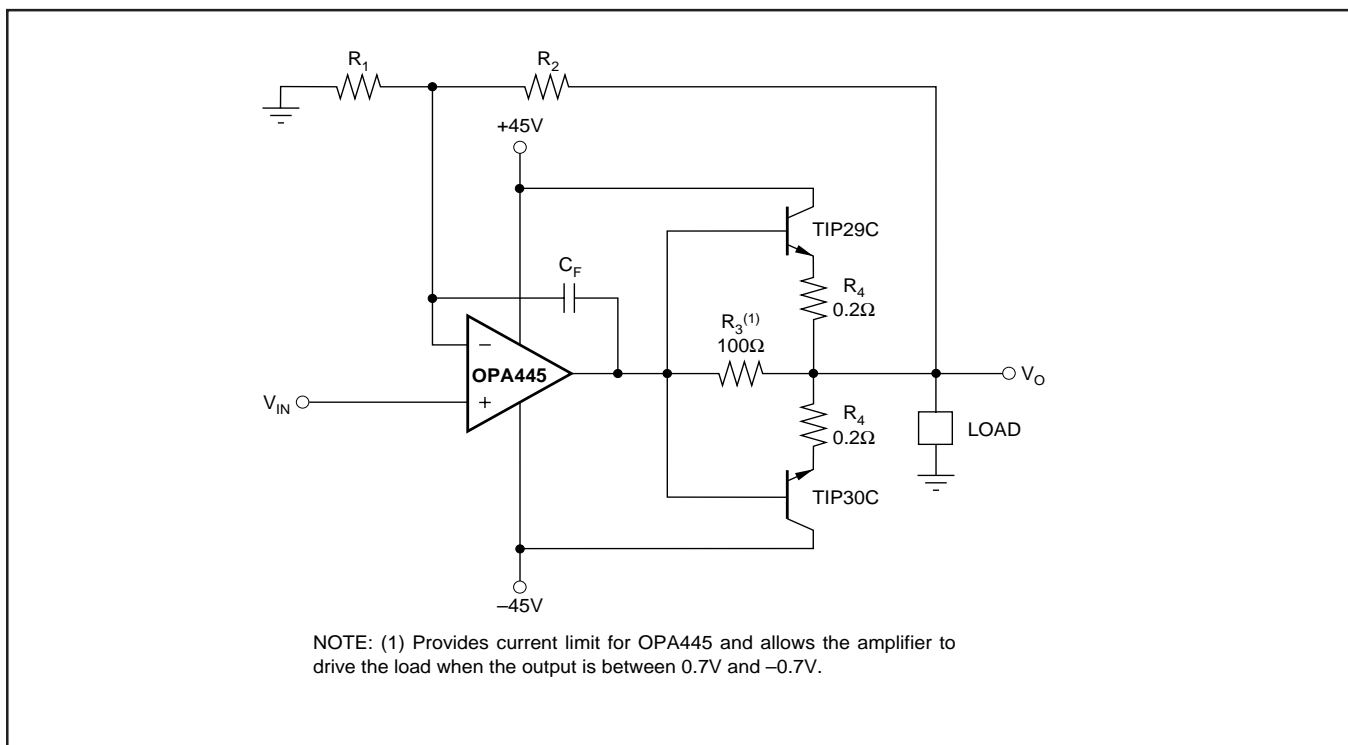


FIGURE 8. External Output Transistors Boost Output Current up to 1 Amp.

TYPICAL APPLICATIONS

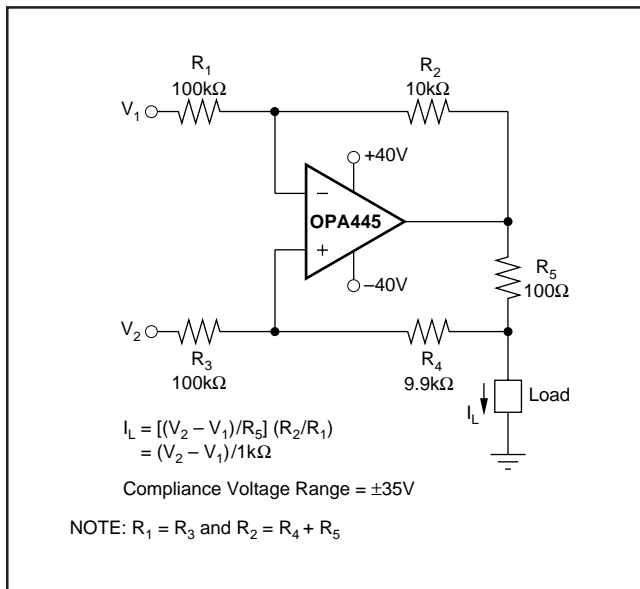


FIGURE 9. Voltage-to-Current Converter.

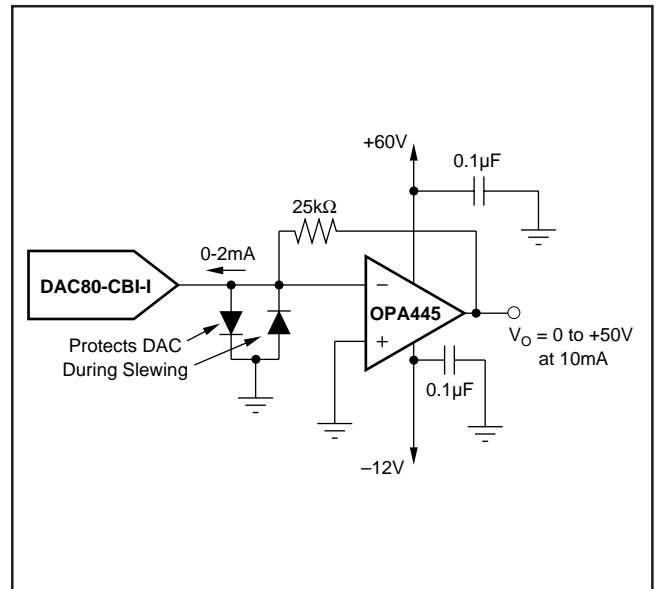


FIGURE 10. Programmable Voltage Source.

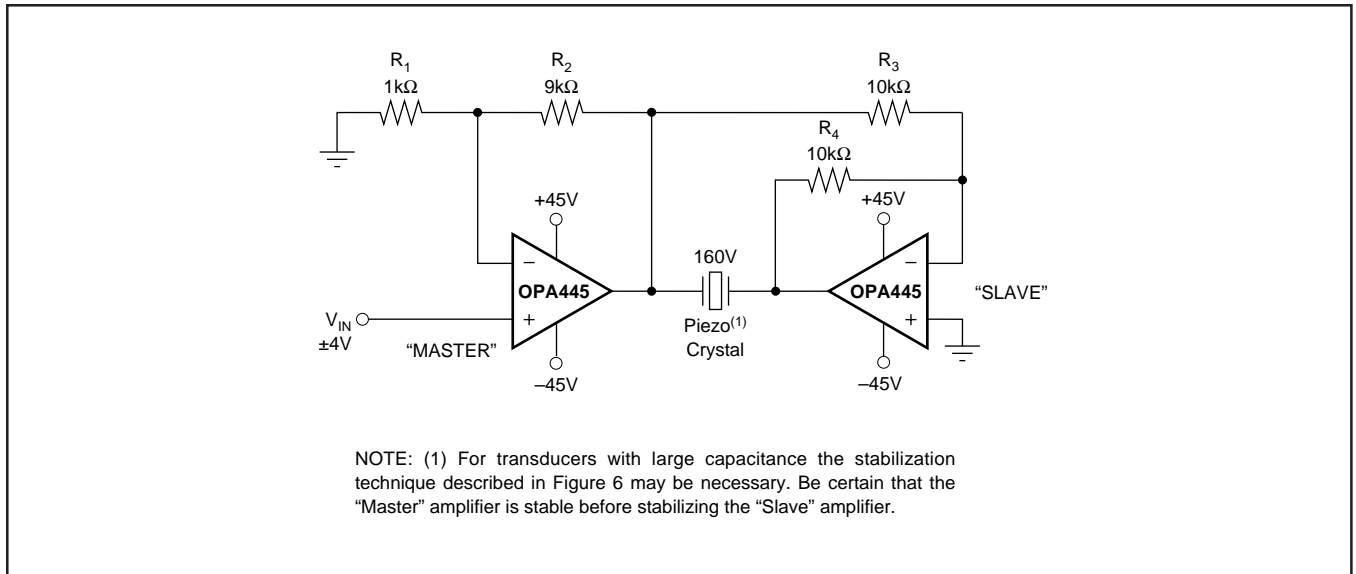


FIGURE 11. Bridge Circuit Doubles Voltage for Piezo Crystals.