# MCP23016

## 16-Bit I²C™ I/O Expander

### Features

- 16-bit remote bidirectional I/O port
  - 16 I/O pins default to 16 inputs
- Fast I²C bus clock frequency (0 - 400 kbits/s)
- Three hardware address pins allow use of up to eight devices
- High current drive capability per I/O: ±25 mA
- Open-drain interrupt output on input change
- Interrupt port capture register
- Internal Power-On Reset (POR)
- Polarity inversion register to configure the polarity of the input port data
- Compatible with most microcontrollers
- Available temperature range:
  - Industrial (I): -40°C to +85°C

### CMOS Technology

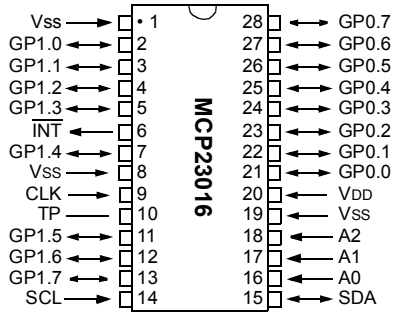
- Operating Supply Voltage: 2.0V to 5.5V
- Low standby current

### Packages

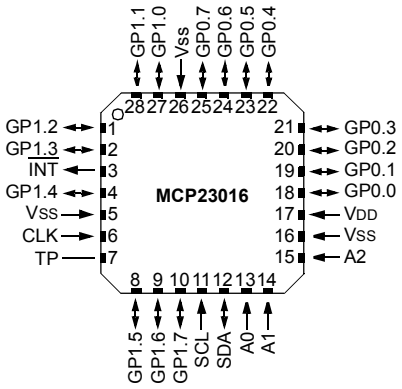
- 28-pin PDIP, 300 mil; 28-pin SOIC, 300 mil
- 28-pin SSOP, 209 mil; 28-pin QFN, 6x6 mm

### Package Types

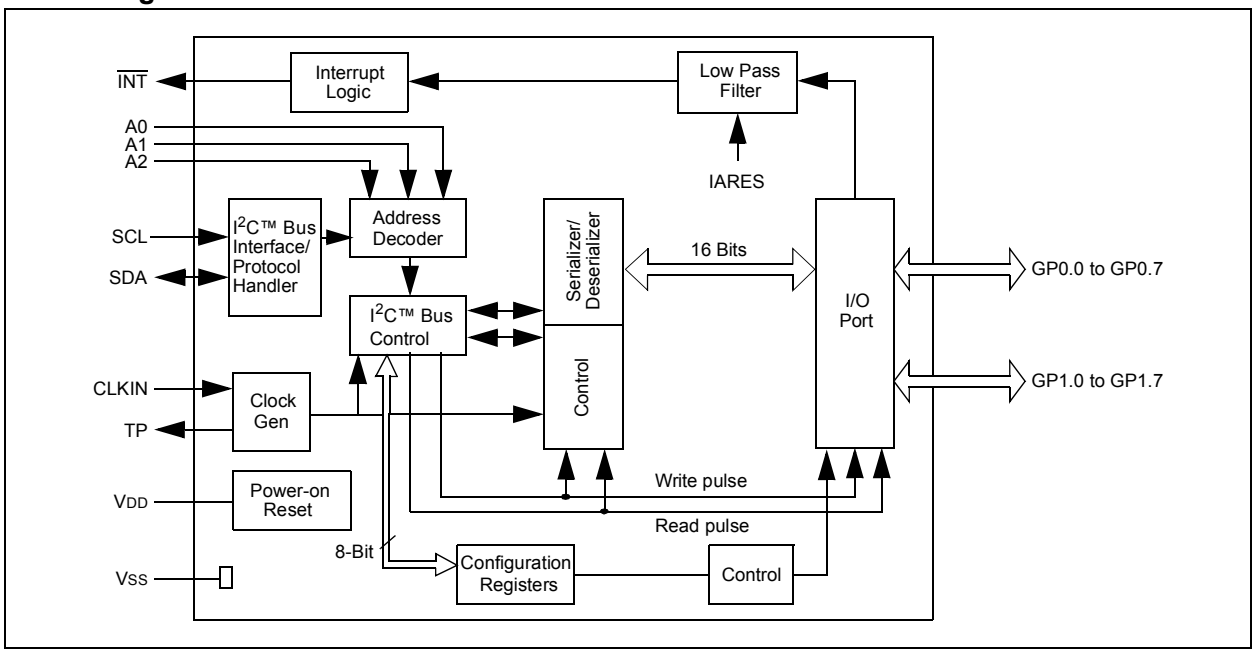
**PDIP, SOIC, SSOP**




**QFN**




### Block Diagram



**NOTES:**

## 1.0 DEVICE OVERVIEW

The MCP23016 device provides 16-bit, general purpose parallel I/O expansion for $I^2C$ bus applications.

This device includes high-current drive capability, low supply current and individual I/O configuration. I/O expanders provide a simple solution when additional I/Os are needed for ACPI, power switches, sensors, push buttons, LEDs and so on.

The MCP23016 consists of multiple 8-bit configuration registers for input, output and polarity selection. The system master can enable the I/Os as either inputs or outputs by writing the I/O configuration bits. The data for each input or output is kept in the corresponding input or output register. The polarity of the read register can be inverted with the polarity inversion register. (See Section 1.7.3, “Input Polarity Registers”) All registers can be read by the system master.

The open-drain interrupt output is activated when any input state differs from its corresponding input port register state. This is used to indicate to the system master that an input state has changed. The interrupt capture register captures port value at this time. The Power-on Reset sets the registers to their default values and initializes the device state machine.

Three device inputs (A0 - A2) determine the $I^2C$ address and allows up to eight I/O Expander devices to share the same $I^2C$ bus.

### 1.1 Pin Descriptions

**TABLE 1-1: PINOUT DESCRIPTION**

| Pin Name | PDIP, SOIC, SSOP Pin No. | QFN Pin No. | I/O/P Type | Buffer Type | Description |
|---|---|---|---|---|---|
| CLK | 9 | 6 | I | ST | Clock source input |
| TP | 10 | 7 | O | — | Test Pin (This pin must be left floating) |
| GP1.0 | 2 | 27 | I/O | TTL | D0 digital input/output for GP1 |
| GP1.1 | 3 | 28 | I/O | TTL | D1 digital input/output for GP1 |
| GP1.2 | 4 | 1 | I/O | TTL | D2 digital input/output for GP1 |
| GP1.3 | 5 | 2 | I/O | TTL | D3 digital input/output for GP1 |
| GP1.4 | 7 | 4 | I/O | TTL | D4 digital input/output for GP1 |
| GP1.5 | 11 | 8 | I/O | ST | D5 digital input/output for GP1 |
| GP1.6 | 12 | 9 | I/O | ST | D6 digital input/output for GP1 |
| GP1.7 | 13 | 10 | I/O | ST | D7 digital input/output for GP1 |
| GP0.0 | 21 | 18 | I/O | TTL | D0 digital input/output for GP0 |
| GP0.1 | 22 | 19 | I/O | TTL | D1 digital input/output for GP0 |
| GP0.2 | 23 | 20 | I/O | TTL | D2 digital input/output for GP0 |
| GP0.3 | 24 | 21 | I/O | TTL | D3 digital input/output for GP0 |
| GP0.4 | 25 | 22 | I/O | TTL | D4 digital input/output for GP0 |
| GP0.5 | 26 | 23 | I/O | TTL | D5 digital input/output for GP0 |
| GP0.6 | 27 | 24 | I/O | TTL | D6 digital input/output for GP0 |
| GP0.7 | 28 | 25 | I/O | TTL | D7 digital input/output for GP0 |
| SCL | 14 | 11 | I | ST | Serial clock input |
| SDA | 15 | 12 | I/O | ST | Serial data I/O |
| $\overline{INT}$ | 6 | 3 | O | OD | Interrupt output |
| A0 | 16 | 13 | I | ST | Address input 1 |
| A1 | 17 | 14 | I | ST | Address input 2 |
| A2 | 18 | 15 | I | ST | Address input 3 |
| $V_{SS}$ | 1, 8, 19 | 5, 16, 26 | P | — | Ground reference for logic and I/O pins |
| $V_{DD}$ | 20 | 17 | P | — | Positive supply for logic and I/O pins |

## 1.2 Power-on Reset (POR)

The on-chip POR circuit holds the chip in RESET until VDD has reached a high enough level to deactivate the POR circuit (i.e., release RESET). A maximum rise time for VDD is specified in the electrical specifications.

When the device starts normal operation (exits the RESET condition), device operating parameters (voltage, frequency, temperature) must be met to ensure proper operation.

## 1.3 Power-up Timer (PWRT)

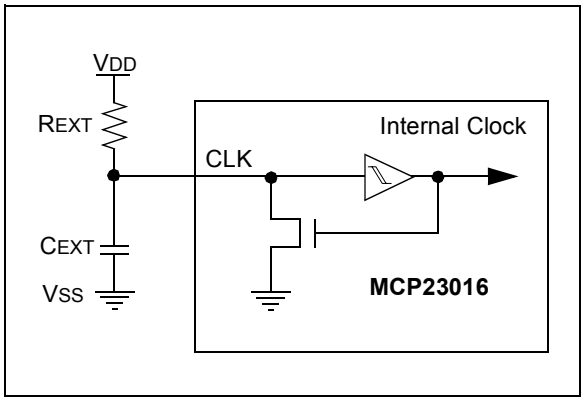
The Power-up Timer provides a 72 ms nominal time-out on power-up, keeping the device in RESET, allowing VDD to rise to an acceptable level.

The power-up time delay will vary from chip-to-chip due to VDD, temperature and process variation. See Table 2-4 for details (TPWRT, parameter 3).

## 1.4 Clock Generator

The MCP23016 uses an external RC circuit to determine the internal clock speed. The user must connect R and C to the MCP23016, as shown in Figure 1-1.

**FIGURE 1-1: CLOCK CONFIGURATION**




A 1 MHz (typ.) internal clock is needed for the device to function properly. The internal clock can be measured on the TP pin. Recommended REXT and CEXT values are shown in Table 1-2.

| **Note:** | Set IARES = 1 to measure the clock output on TP. |
|---|---|

**TABLE 1-2: RECOMMENDED VALUES**

| REXT | CEXT |
|---|---|
| 3.9 kΩ | 33 pF |

## 1.5 I²C Bus Interface/ Protocol Handler

This block manages the functionality of the I²C bus interface and protocol handling. The MCP23016 supports the following commands:

**TABLE 1-3: COMMAND BYTE TO REGISTER RELATIONSHIP**

| Command Byte | Result |
|---|---|
| 0h | Access to GP0 |
| 1h | Access to GP1 |
| 2h | Access to OLAT0 |
| 3h | Access to OLAT1 |
| 4h | Access to IPOL0 |
| 5h | Access to IPOL1 |
| 6h | Access to IODIR0 |
| 7h | Access to IODIR1 |
| 8h | Access to INTCAP0 (Read-Only) |
| 9h | Access to INTCAP1 (Read-Only) |
| Ah | Access to IOCON0 |
| Bh | Access to IOCON1 |

## 1.6 Address Decoder

The last three LSb of the 7-bit address are user-defined (see Table 1-4). Three hardware pins (<A2:A0>) define these bits.

**TABLE 1-4: DEVICE ADDRESS**

| | | | | | | |
|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | A2 | A1 | A0 |

## 1.7 Register Block

The register block contains the Configuration registers and Port registers, as shown Table 1-5.

**TABLE 1-5: REGISTER SUMMARY**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR |
|---|---|---|---|---|---|---|---|---|---|
| **Port Registers** | | | | | | | | | |
| GP0 | GP0.7 | GP0.6 | GP0.5 | GP0.4 | GP0.3 | GP0.2 | GP0.1 | GP0.0 | 0000 0000 |
| GP1 | GP1.7 | GP1.6 | GP1.5 | GP1.4 | GP1.3 | GP1.2 | GP1.1 | GP0.0 | 0000 0000 |
| OLAT0 | OL0.7 | OL0.6 | OL0.5 | OL0.4 | OL0.3 | OL0.2 | OL0.1 | OL0.0 | 0000 0000 |
| OLAT1 | OL1.7 | OL1.6 | OL1.5 | OL1.4 | OL1.3 | OL1.2 | OL1.1 | OL1.0 | 0000 0000 |
| **Configuration Registers** | | | | | | | | | |
| IPOL0 | IGP0.7 | IGP0.6 | IGP0.5 | IGP0.4 | IGP0.3 | IGP0.2 | IGP0.1 | IGP0.0 | 0000 0000 |
| IPOL1 | IGP1.7 | IGP1.6 | IGP1.5 | IGP1.4 | IGP1.3 | IGP1.2 | IGP1.1 | IGP1.0 | 0000 0000 |
| IODIR0 | IOD0.7 | IOD0.6 | IOD0.5 | IOD0.4 | IOD0.3 | IOD0.2 | IOD0.1 | IOD0.0 | 1111 1111 |
| IODIR1 | IOD1.7 | IOD1.6 | IOD1.5 | IOD1.4 | IOD1.3 | IOD1.2 | IOD1.1 | IOD1.0 | 1111 1111 |
| INTCAP0 | ICP0.7 | ICP0.6 | ICP0.5 | ICP0.4 | ICP0.3 | ICP0.2 | ICP0.1 | ICP0.0 | xxxx xxxx |
| INTCAP1 | ICP1.7 | ICP1.6 | ICP1.5 | ICP1.4 | ICP1.3 | ICP1.2 | ICP1.1 | ICP1.0 | xxxx xxxx |
| IOCON0 | — | — | — | — | — | — | — | IARES | ---- ---0 |
| IOCON1 | — | — | — | — | — | — | — | IARES | ---- ---0 |

Legend: '1' bit is set, '0' bit is cleared, x = unknown, — = unimplemented.

### 1.7.1 DATA PORT REGISTERS

Two registers provide access to the two GPIO ports:

- GP0 (provides access to data port GP0)
- GP1 (provides access to data port GP1)

A read from this register provides status on pins of these ports. A write to these registers will modify the output latch registers (OLAT0, OLAT1) and data output.

**REGISTER 1-1: GP0 - GENERAL PURPOSE I/O PORT REGISTER 0**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| GP0.7 | GP0.6 | GP0.5 | GP0.4 | GP0.3 | GP0.2 | GP0.1 | GP0.0 |
| bit 7 | | | | | | | bit 0 |

bit 7-0 **GP0.0:GP0.7**: Reflects the logic level on the pins.
1 = Logic '1'
0 = Logic '0'

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

**REGISTER 1-2: GP1 - GENERAL PURPOSE I/O PORT REGISTER 1**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| GP1.7 | GP1.6 | GP1.5 | GP1.4 | GP1.3 | GP1.2 | GP1.1 | GP1.0 |
| bit 7 | | | | | | | bit 0 |

bit 7-0 **GP1.0:GP1.7**: Reflects the logic level on the pins.
1 = Logic '1'
0 = Logic '0'

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

### 1.7.2 OUTPUT LATCH REGISTERS

Two registers provide access to the two port output latches:

- OLAT0 (provides access to the output latch for port GP0)
- OLAT1 (provides access to the output latch for port GP1)

A read from these registers results in a read of the latch that controls the output and not the actual port. A write to these registers updates the output latch that controls the output.

**REGISTER 1-3: OLAT0 - OUTPUT LATCH REGISTER 0**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| OL0.7 | OL0.6 | OL0.5 | OL0.4 | OL0.3 | OL0.2 | OL0.1 | OL0.0 |
| bit 7 | | | | | | | bit 0 |

bit 7-0 **OL0.0:O0.7**: Reflects the logic level on the output latch.
1 = Logic '1'
0 = Logic '0'

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

**REGISTER 1-4: OLAT1 - OUTPUT LATCH REGISTER 1**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| OL1.7 | OL1.6 | OL1.5 | OL1.4 | OL1.3 | OL1.2 | OL1.1 | OL1.0 |
| bit 7 | | | | | | | bit 0 |

bit 7-0 **OL1.0:O1.7**: Reflects the logic level on the output latch.
1 = Logic '1'
0 = Logic '0'

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

### 1.7.3 INPUT POLARITY REGISTERS

These registers allow the user to configure the polarity of the input port data (GP0 and GP1). If a bit in this register is set, the corresponding input port (GPn) data bit polarity will be inverted.

- IPOL0 (controls the polarity of GP0)
- IPOL1 (controls the polarity of GP1)

**REGISTER 1-5: IPOL0 - INPUT POLARITY PORT REGISTER 0**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| IGP0.7 | IGP0.6 | IGP0.5 | IGP0.4 | IGP0.3 | IGP0.2 | IGP0.1 | IGP0.0 |
| bit 7 | | | | | | | bit 0 |

bit 7-0 **IGP0.0:IGP0.7**: Controls the polarity inversion for the input pins
1 = Corresponding GP0 bit is inverted
0 = Corresponding GP0 bit is not inverted

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

**REGISTER 1-6: IPOL1 - INPUT POLARITY PORT REGISTER 1**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| IGP1.7 | IGP1.6 | IGP1.6 | IGP1.4 | IGP1.3 | IGP1.2 | IGP1.1 | IGP1.0 |
| bit 7 | | | | | | | bit 0 |

bit 7-0 **IGP1.0:IGP1.7**: Controls the polarity inversion for the input pins
1 = Corresponding GP1 bit is inverted
0 = Corresponding GP1 bit is not inverted

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

### 1.7.4 I/O DIRECTION REGISTERS

Two registers control the direction of data I/O:

- IODIR0 (controls GP0)
- IODIR1 (controls GP1)

When a bit in these registers is set, the corresponding pin becomes an input; otherwise, it becomes an output. At Power-on Reset, the device ports are configured as inputs.

**REGISTER 1-7: IODIR0 - I/O DIRECTION REGISTER 0**

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| IOD0.7 | IOD0.6 | IOD0.5 | IOD0.4 | IOD0.3 | IOD0.2 | IOD0.1 | IOD0.0 |
| bit 7 | | | | | | | bit 0 |

bit 7-0 **IOD0.0:IO0.7:** Controls the direction of data I/O
1 = Input
0 = Output

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

**REGISTER 1-8: IODIR1 - I/O DIRECTION REGISTER 1**

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| IOD1.7 | IOD1.6 | IOD1.5 | IOD1.4 | IOD1.3 | IOD1.2 | IOD1.1 | IOD1.0 |
| bit 7 | | | | | | | bit 0 |

bit 7-0 **IOD1.0:IO1.7:** Controls the direction of data I/O
1 = Input
0 = Output

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

### 1.7.5 INTERRUPT CAPTURE REGISTERS

Two registers contain the value of the port that generated the interrupt:

- INTCAP0 contains the value of GP0 at time of GP0 change interrupt
- INTCAP1 contains the value of GP1 at time of GP1 change interrupt

These registers are 'read-only' registers (A write to these registers is ignored).

**REGISTER 1-9: INTCAP0 - INTERRUPT CAPTURED VALUE FOR PORT REGISTER 0**

| R-x | R-x | R-x | R-x | R-x | R-x | R-x | R-x |
|---|---|---|---|---|---|---|---|
| ICP0.7 | ICP0.6 | ICP0.5 | ICP0.4 | ICP0.3 | ICP0.2 | ICP0.1 | ICP0.0 |
| bit 7 | | | | | | | bit 0 |

bit 7-0 **ICP0.0:ICP0.7:** Reflects the logic level on the GP0 pins at the time of interrupt due to pin change
1 = Logic '1'
0 = Logic '0'

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

**REGISTER 1-10: INTCAP1 - INTERRUPT CAPTURED VALUE FOR PORT REGISTER 1**

| R-x | R-x | R-x | R-x | R-x | R-x | R-x | R-x |
|---|---|---|---|---|---|---|---|
| ICP1.7 | ICP1.6 | ICP1.5 | ICP1.4 | ICP1.3 | ICP1.2 | ICP1.1 | ICP1.0 |
| bit 7 | | | | | | | bit 0 |

bit 7-0 **ICP1.0:ICP1.7:** Reflects the logic level on the GP1 pins at the time of interrupt due to pin change
1 = Logic '1'
0 = Logic '0'

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

### 1.7.6 I/O EXPANDER CONTROL REGISTER

- IOCON0 controls the functionality of the MCP23016.

The IARES (Interrupt Activity Resolution) bit controls the sampling frequency of the GP port pins. The higher the sampling frequency, the higher the device current requirements. If this bit is '0' (default), the maximum time to detect the activity on the port is 32 ms (max.), which results in lower standby current. If this bit is '1', the maximum time to detect activity on the port is 200 µsec. (max.), and results in higher standby current.

**REGISTER 1-11: IOCON0 - I/0 EXPANDER CONTROL REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | IARES |
| bit 7 | | | | | | | bit 0 |

bit 1-7 **Unimplemented bit:** Read as '0'

bit 0 **IARES: Interrupt Activity Resolution**
1 = Fast sample rate
0 = Normal sample rate

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

**IOCON1** is a shadow register for IOCON0. Access to IOCON1 results in access to IOCON0.

## 1.8 Serializer/Deserializer

The Serializer/Deserializer block converts and transfers data between the $I^2C$ bus and GPIO.

## 1.9 Interrupt Logic

The MCP23016 asserts the open-drain interrupt output ($\overline{INT}$) low when one of the port pins changes state. Only those pins that are configured as an input can cause an interrupt. Pins defined as an output have no effect on $\overline{INT}$. The interrupt will remain active until a read from either the port (GPn) on which the interrupt occurred or the INTCAPn register is performed. If the input returns to its previous state before a read operation, it will reset the interrupt and the $\overline{INT}$ pin output will tri-state. Each 8-bit port is read separately, so reading GP0 or INTCAP0 will not clear the interrupt generated by GP1 or INTCAP1, and vice versa.

Input change activity on each port will generate an interrupt and the value of the particular port will be captured and copied into INTCAP0/INTCAP1. The INTCAPn registers are only updated when an interrupt occurs on $\overline{INT}$. These values will stay unchanged until the user clears the interrupt by reading the port or the INTCAPn register.

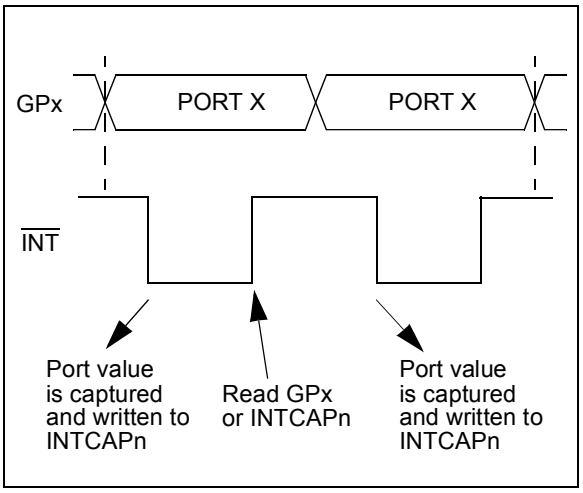
If the input port value changes back to normal before a user-read, the $\overline{INT}$ output will be reset. However, the INTCAP0/INTCAP1 will still contain the value of the port at the interrupt change. If the port value changes again, it will re-activate the interrupt and the new value will be captured.

The first interrupt on change event following an interrupt RESET will result in a capture event. Any further change event that occurs before the interrupt is reset will not result in a capture event.

### 1.9.1 INTERRUPT EVENT DETECTION

The IARES bit controls the resolution for detecting an interrupt on change event. If this bit is '0' (default), the maximum time for detecting a change of event is high, which results in lower standby current. If this bit is '1', it takes less time for scanning the activity on the port and results in higher standby current.

**FIGURE 1-2: READING PORTX AFTER INTERRUPT EVENT**



### 1.9.2 WRITING THE REGISTERS

To write to an MCP23016 register, the Master $I^2C$ device needs to follow the requirements, as illustrated in Figure 1-3. First, the device is selected by sending the slave address and setting the R/$\overline{W}$ bit to logic '0'. The command byte is sent after the address and determines which register will be written. Table 1-3 shows the relationship of the command byte and register.

The MCP23016 has twelve 8-bit registers. They are configured to operate as six 16-bit register pairs, supporting the device's 16-bit port. These pairs are formed based on their functions (e.g. GP0 and GP1 are grouped together). The $I^2C$ commands apply to one register pair to provide faster access. The first data byte following a command byte is written into the register pointed to by the command byte, while the second data is written into another register in the same pair. For example, if the first byte is sent to OLAT1 (command byte 03h), the next data byte will be written into the second register of that pair, OLAT0. If the first byte is written to OLAT0 (command byte 02h), then the second byte will be written to OLAT1.

There is no limitation on the number of data bytes in one write transmission. Figure 1-4 shows the case of multiple byte writes in one write operation. In this case, the multiple writes are made to the same data pair.

| **Note:** | The bus must remain free until after the ninth clock pulse for a minimum of 12 µs (see Table 2-5 and Figure 2-4). |
|---|---|

**FIGURE 1-3: WRITE TO CONFIGURATION REGISTERS (CASE 1)**

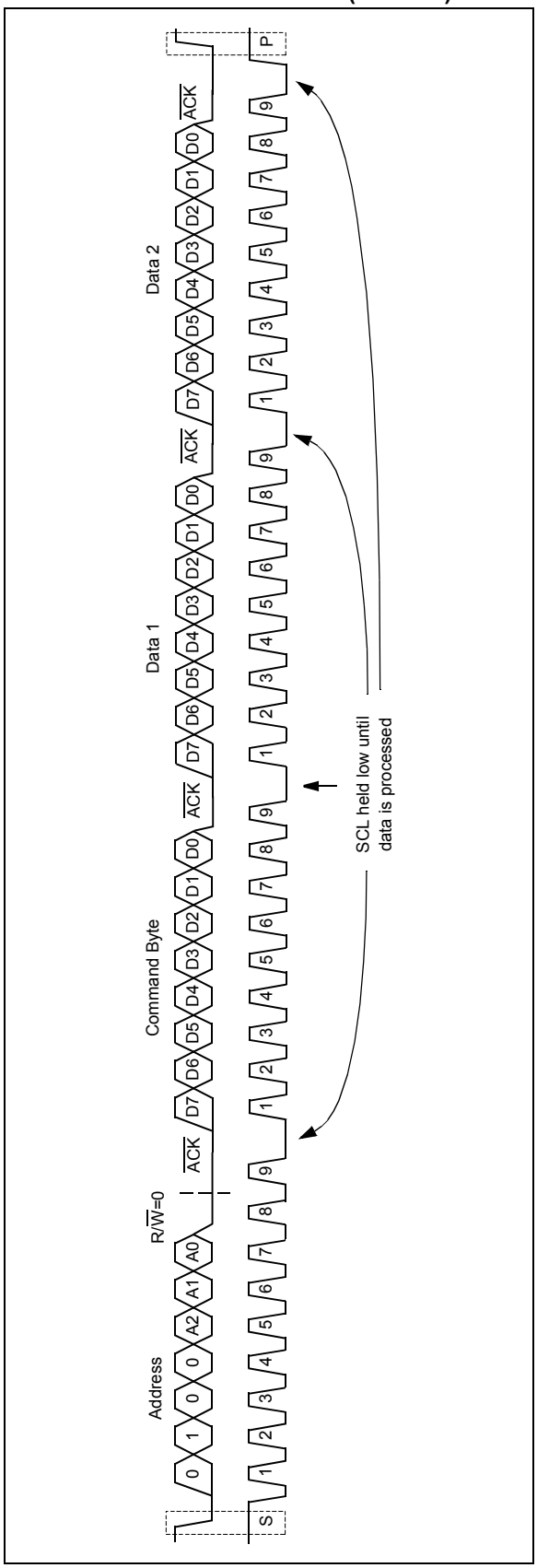


**FIGURE 1-4: WRITE TO CONFIGURATION REGISTERS (CASE 2)**

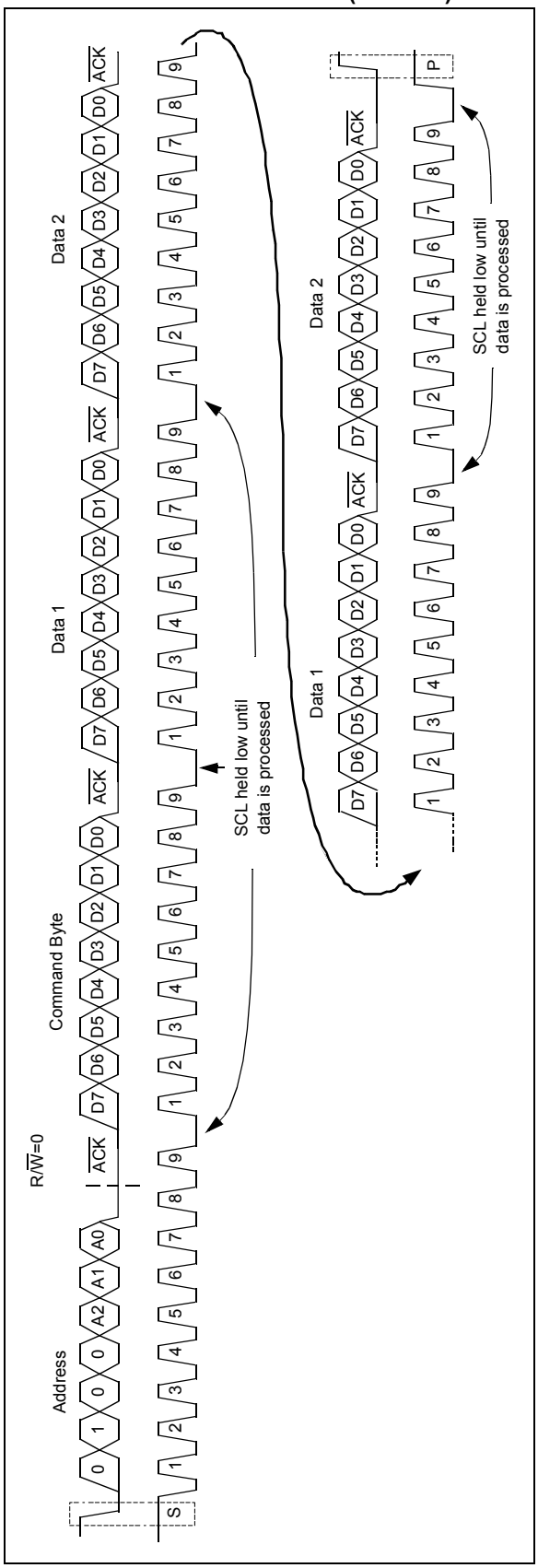
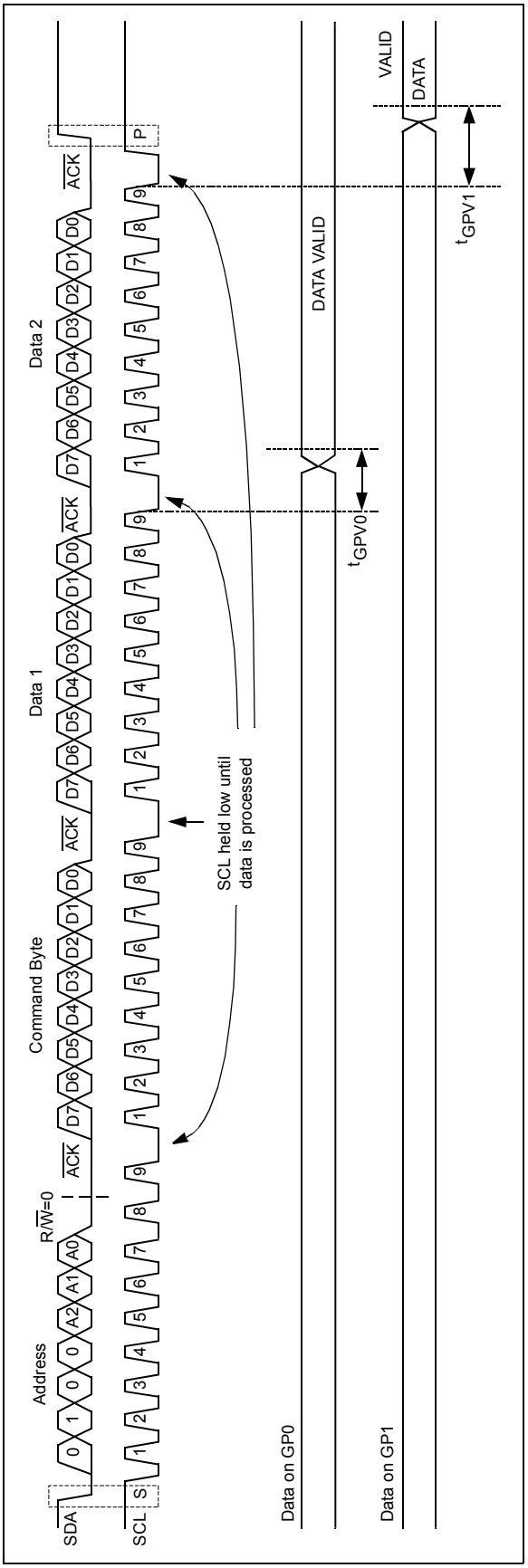



**FIGURE 1-5: WRITE TO OUTPUT PORTS**



### 1.9.3 READING THE REGISTERS

To read an MCP23016 register, the Master needs to follow the requirements shown in Figure 1-6. First, the device is selected by sending the slave address and setting the R/$\overline{W}$ bit to logic '0'. The command byte is sent after the address and determines which register will be read. A restart condition is generated and the device address is sent again with the R/$\overline{W}$ bit set to logic '1'. The data register defined by the command byte will be sent first, followed by the other register in the register pair. The logic for register selection is the same as explained in Write mode (Section 1.9.2, "Writing the Registers").

The falling edge of the ninth clock initiates the register read action. The SCL clock will be held low while the data is read from the register and is transferred to the $I^2C$ bus control block by the Serializer/Deserializer block.

The MCP23016 holds the clock low after the falling edge of the ninth clock pulse. The configuration registers, or port control registers, are read and the value is stored. Finally, the clock is released to enable the next transmission.

There is no limitation on the number of data bytes in one read transmission. Figure 1-8 shows the case of multiple byte read in one read operation. In this case, the multiple writes are made to the same data pair.

| **Note:** | The bus must remain free until after the ninth clock pulse for a minimum of 12 µs (see Table 2-5 and Figure 2-4). |
|---|---|

**FIGURE 1-6: READ FROM CONFIGURATION REGISTER**

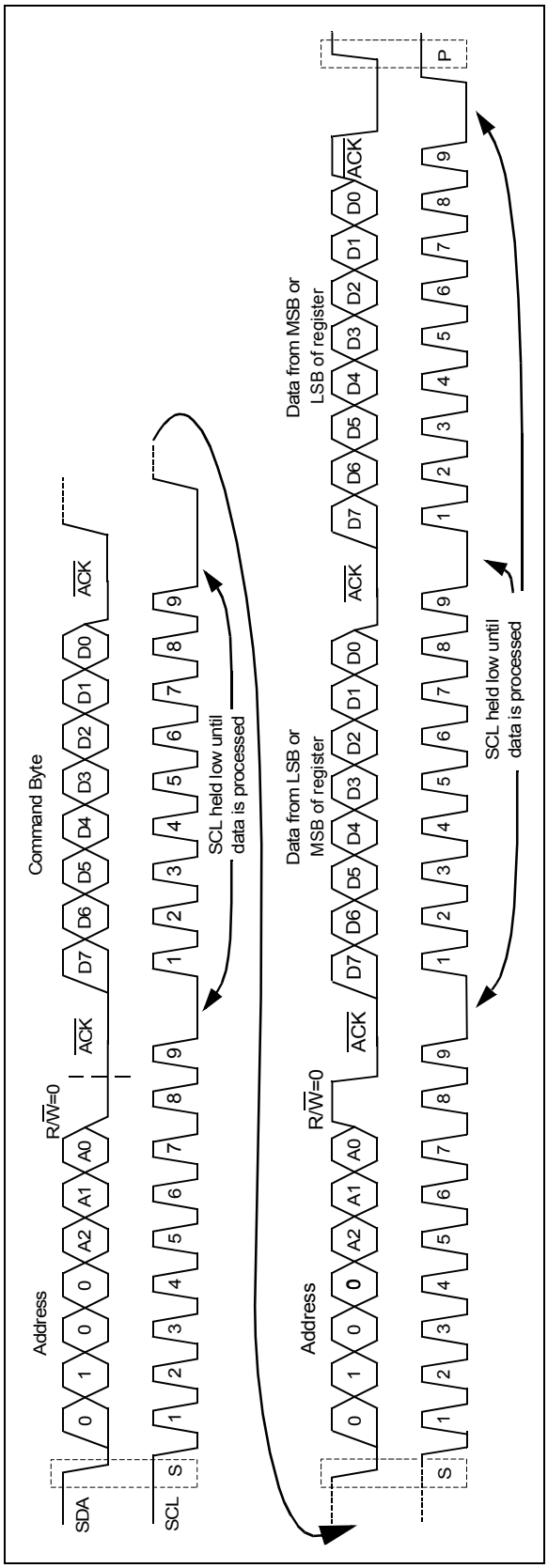


**FIGURE 1-7: READ FROM INPUT PORTS (CASE 1)**

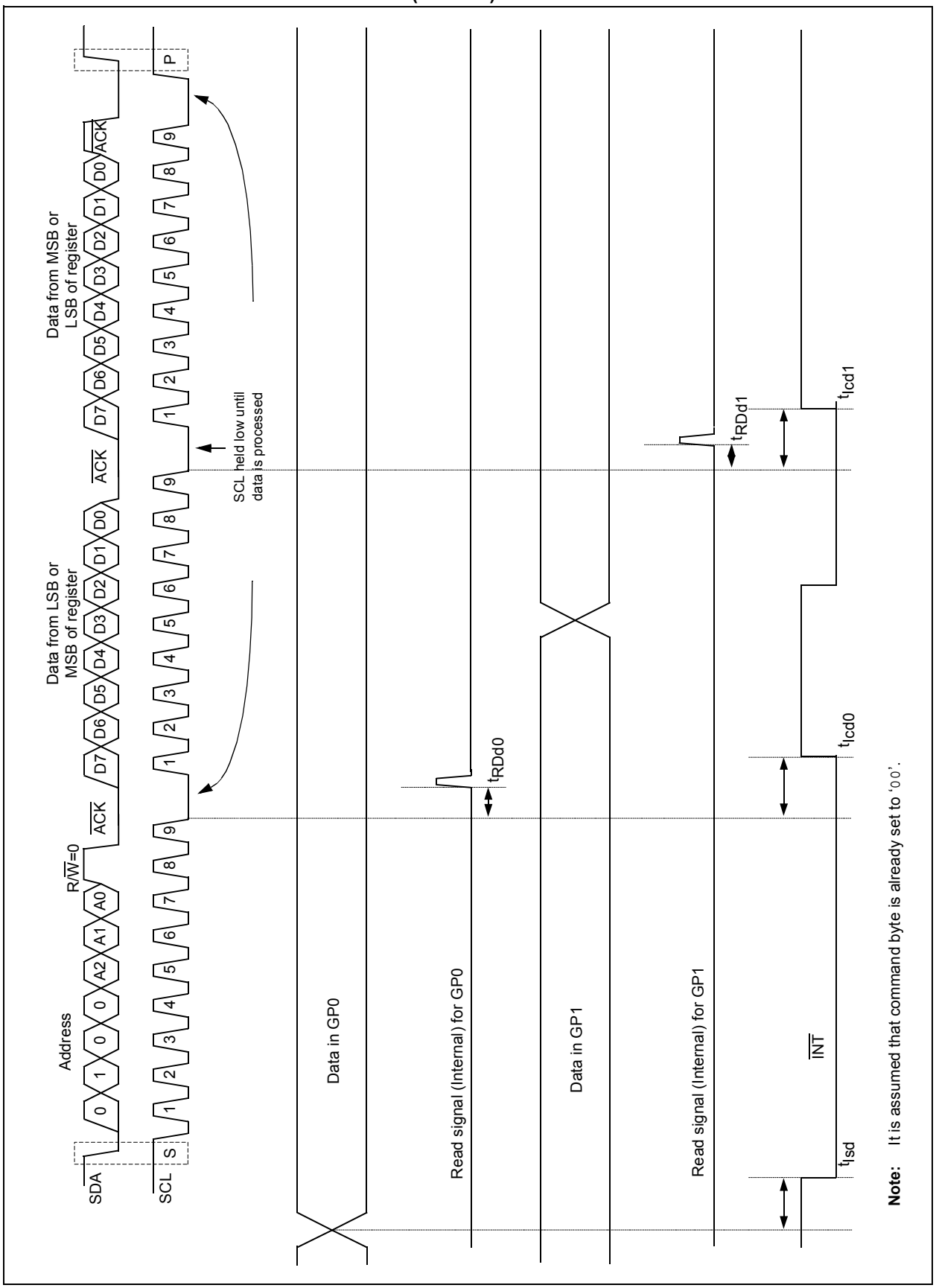
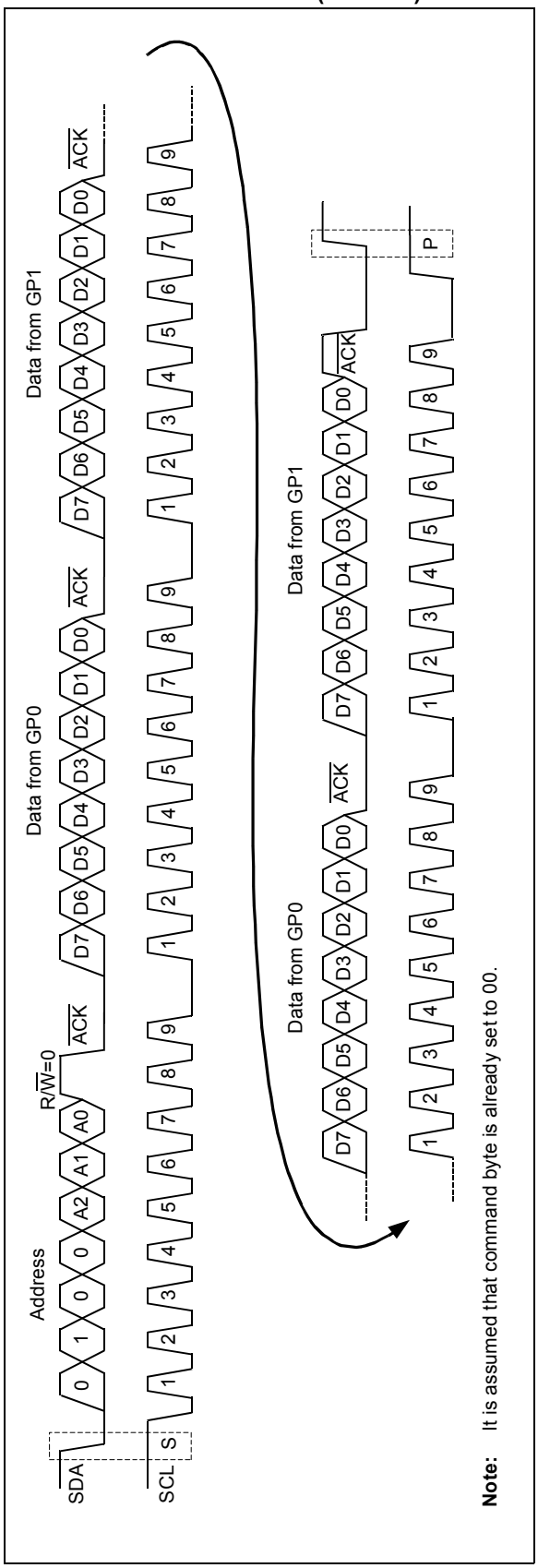


**FIGURE 1-8: READ FROM INPUT PORTS (CASE 2)**



**NOTES:**

## 2.0 ELECTRICAL CHARACTERISTICS

**Absolute Maximum Ratings †**

Ambient temperature under bias ..... -55 to +125°C

Storage temperature ..... -65°C to +150°C

Voltage on any pin with respect to $V_{SS}$ ..... -0.3V to ($V_{DD}$ + 0.3V)

Voltage on $V_{DD}$ with respect to $V_{SS}$ ..... -0.3V to +6.5V

Total power dissipation **(Note 1)** ..... 1.0 W

Maximum current out of $V_{SS}$ pin ..... 300 mA

Maximum current into $V_{DD}$ pin ..... 250 mA

Input clamp current, $I_{IK}$ ($V_I$ < 0, or $V_I$ > $V_{DD}$) ..... ± 20 mA

Output clamp current, $I_{OK}$ ($V_O$ < 0, or $V_O$ > $V_{DD}$) ..... ± 20 mA

Maximum output current sunk by any I/O pin ..... 25 mA

Maximum output current sourced by any I/O pin ..... 25 mA

Maximum current sunk by combined PORTS ..... 200 mA

Maximum current sourced by combined PORTS ..... 200 mA

**Note 1:** Power dissipation is calculated as follows:

$$Pdis = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$$

**† NOTICE:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

## 2.1 DC Characteristics

**TABLE 2-1: DC CHARACTERISTICS**

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for industrial | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Characteristic** | **Sym** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| D001 | Supply Voltage | VDD | 2.0 | — | 5.5 | V | |
| D002 | Standby Current | IDD | — | 0.4 | | mA | IARES = 1 |
| D003 | Standby Current | IPD | — | 25 | | µA | IARES = 0 |
| | **Input Low Voltage** | | | | | | |
| | I/O ports | VIL | | | | | |
| D004 | TTL buffer | | VSS | — | 0.15 VDD | V | For entire VDD range |
| D004A | | | VSS | — | 0.8V | | 4.5V ≤ VDD ≤ 5.5V |
| D005 | Schmitt Trigger buffer | | VSS | — | 0.2 VDD | V | |
| | **Input High Voltage** | | | | | | |
| | I/O ports | VIH | | — | | | |
| D006 | TTL buffer | | 2.0 | — | VDD | V | 4.5V ≤ VDD ≤ 5.5V |
| D006A | | | 0.25 VDD + 0.8V | — | VDD | V | For entire VDD range |
| D007 | Schmitt Trigger buffer | | 0.8 VDD | — | VDD | V | For entire VDD range |
| | **Input Leakage Current** | | | | | | |
| D008 | I/O ports | IIL | — | — | ±1.0 | µA | Vss ≤ VPIN ≤ VDD, Pin at hi-impedance |
| D009 | CLK | | — | — | ±5.0 | µA | Vss ≤ VPIN ≤ VDD |
| D010 | VDD start voltage to ensure internal POR signal | VPOR | — | VSS | — | V | |
| D011 | VDD rise rate to ensure internal POR signal | SVDD | 0.05 | - | — | V/ms | **Note 1** |
| | DC Trip Point | VTPOR | 1.5 | 1.7 | 1.9 | V | DC Slow Ramp |
| D011 | VDD rise rate to ensure internal POR signal with PWRT enabled | SVDD | 0.05 | — | — | V/ms | **Note 1** |
| | DC Current Draw | IPOR | — | 5.0 | — | µA | At 5.0V (1 µ/Volt typical) |

**Note 1:** These parameters are characterized but not tested.

**2:** Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**3:** Standby current is measured with all I/O in hi-impedance state and tied to VDD and VSS.

**4:** For RC CLK, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2 REXT (mA) with REXT in kohm.

**5:** Negative current is defined as coming out of the pin.

**FIGURE 2-1: RESPONSE TIME**

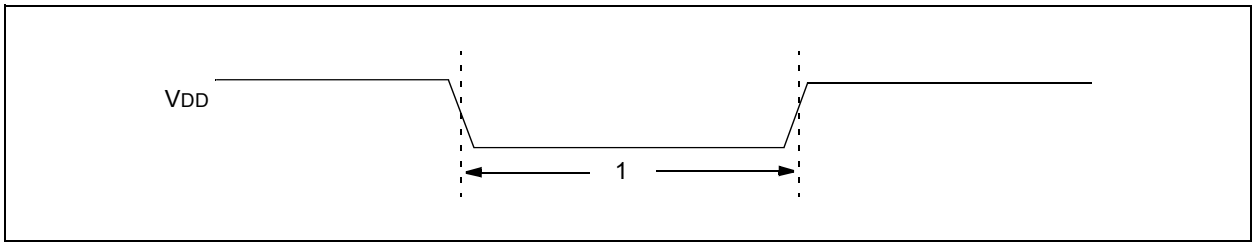



**TABLE 2-2: RESPONSE TIME**

| Parameter No. | Symbol | Characteristic | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 1 | | Response Time | 100 | — | — | ns | Minimum time where a VDD transition from 5.0V to 0.0V to 5.0V will cause a RESET. All times less than 100 ns will be filtered. |

**FIGURE 2-2: TEST POINT CLOCK TIMING**

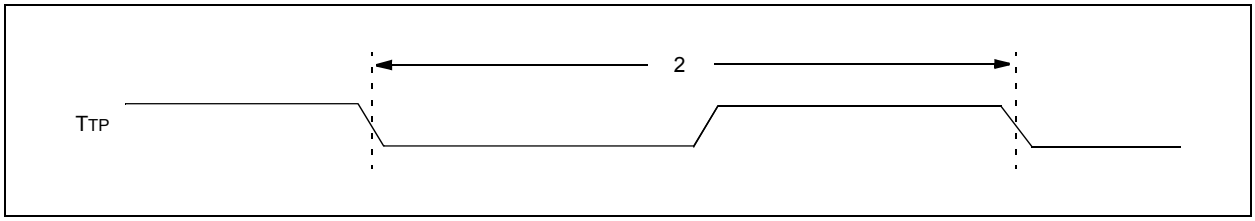



**TABLE 2-3: TEST POINT CLOCK TIMING**

| Parameter No. | Symbol | Characteristic | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | FTP | TP pin Frequency | — | 1.0 | — | MHz | Measured at TP pin, IARES = '1'. |
| 2 | TTP | TP pin CLK Period | — | 1.0 | — | µs | Measured at TP pin, IARES = '1'. |

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**TABLE 2-4: POWER-UP TIMER REQUIREMENTS**

| Parameter No. | Symbol | Characteristic | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 3 | TPWRT | Power-up Timer Period | — | 72 | — | ms | |

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**FIGURE 2-3: I²C™ BUS START/STOP BITS TIMING**

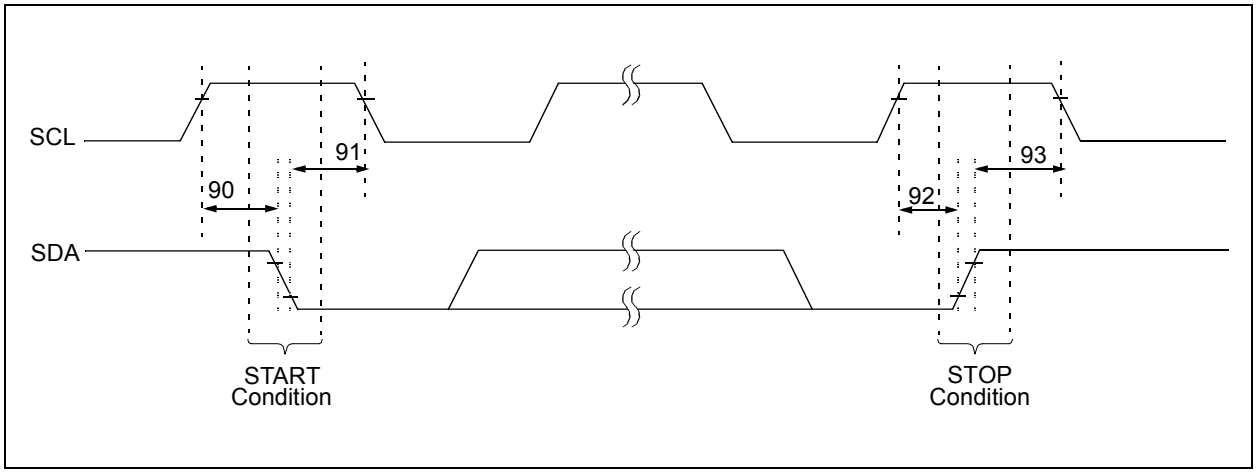



**TABLE 2-5: I²C BUS START/STOP BITS REQUIREMENTS**

| Param No. | Symbol | Characteristic | | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| 90 | TSU:STA | START condition Setup time | 100 kHz mode | 4700 | — | — | ns | Only relevant for Repeated START condition **(Note 1)** |
| | | | 400 kHz mode | 600 | — | — | | |
| 91 | THD:STA | START condition Hold time | 100 kHz mode | 4000 | — | — | ns | After this period, the first clock pulse is generated **(Note 1)** |
| | | | 400 kHz mode | 600 | — | — | | |
| 92 | TSU:STO | STOP condition Setup time | 100 kHz mode | 4700 | — | — | ns | |
| | | | 400 kHz mode | 600 | — | — | | |
| 93 | THD:STO | STOP condition Hold time | 100 kHz mode | 4000 | — | — | ns | |
| | | | 400 kHz mode | 600 | — | — | | |

**Note 1:** These parameters are characterized but not tested.

**FIGURE 2-4: I²C™ BUS DATA TIMING**

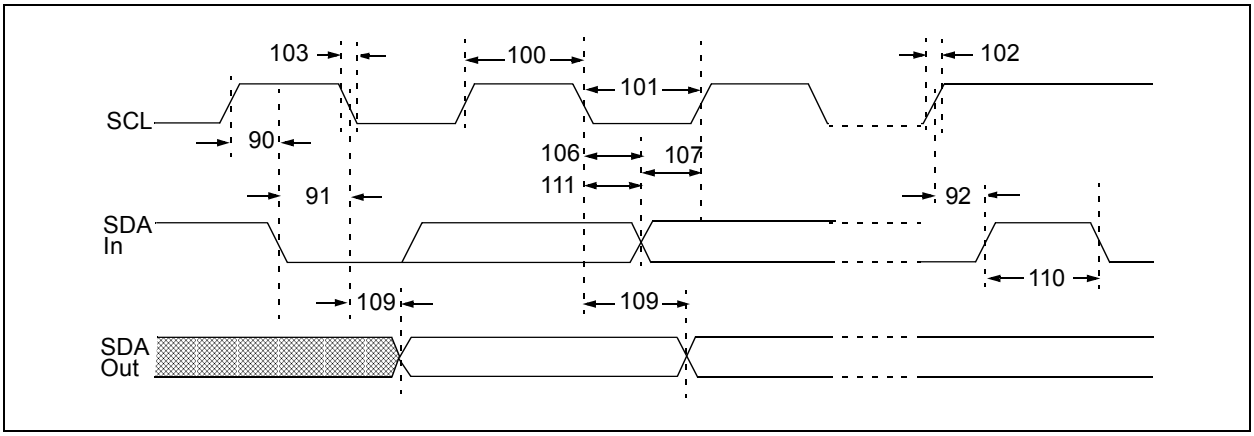


**TABLE 2-6: I²C™ BUS DATA REQUIREMENTS**

| Param No. | Symbol | Characteristic | | Min | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 100 | THIGH | Clock High Time | 100 kHz mode | 4.0 | — | µs | **(Note 1)** |
| | | | 400 kHz mode | 0.6 | — | µs | |
| 101 | TLOW | Clock Low Time | 100 kHz mode | 4.7 | — | µs | **(Note 1)** |
| | | | 400 kHz mode | 1.3 | — | µs | |
| 102 | TR | SDA and SCL Rise Time | 100 kHz mode | — | 1000 | ns | **(Note 1)** |
| | | | 400 kHz mode | 20 + 0.1 CB | 300 | ns | CB is specified to be from 10 - 400 pF |
| 103 | TF | SDA and SCL Fall Time | 100 kHz mode | — | 300 | ns | **(Note 1)** |
| | | | 400 kHz mode | 20 + 0.1 CB | 300 | ns | CB is specified to be from 10 - 400 pF |
| 90 | TSU:STA | START Condition Setup Time | 100 kHz mode | 4.7 | — | µs | Only relevant for repeated START condition **(Note 1)** |
| | | | 400 kHz mode | 0.6 | — | µs | |
| 91 | THD:STA | START Condition Hold Time | 100 kHz mode | 4.0 | — | µs | After this period, the first clock pulse is generated **(Note 1)** |
| | | | 400 kHz mode | 0.6 | — | µs | |
| 106 | THD:DAT | Data Input Hold Time | 100 kHz mode | 0 | — | ns | **(Note 1)** |
| | | | 400 kHz mode | 0 | 0.9 | µs | |
| 107 | TSU:DAT | Data Input Setup Time | 100 kHz mode | 250 | — | ns | **(Note 1) (Note 3)** |
| | | | 400 kHz mode | 100 | — | ns | |
| 92 | TSU:STO | STOP Condition Setup Time | 100 kHz mode | 4.7 | — | µs | **(Note 1)** |
| | | | 400 kHz mode | 0.6 | — | µs | |
| 109 | TAA | Output Valid from Clock | 100 kHz mode | — | 3500 | ns | **(Note 1) (Note 2)** |
| | | | 400 kHz mode | — | — | ns | |
| 110 | TBUF | Bus Free Time | 100 kHz mode | 4.7 | — | µs | Time the bus must be free before a new transmission can start **(Note 1)** |
| | | | 400 kHz mode | 1.3 | — | µs | |
| | CB | Bus Capacitive Loading | | — | 400 | pF | |
| 111 | TWAIT | Clock wait time after ninth pulse. | 100 kHz mode | 12 µs | — | µs | Time the bus must remain free after the ninth clock pulse before a new transmission can start. |
| | | | 400 kHz mode | 12 µs | — | µs | |

**Note 1:** These parameters are characterized but not tested.

**2:** As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

**3:** A Fast mode (400 kHz) I²C bus device can be used in a Standard mode (100 kHz) I²C bus system, but the requirement TSU:DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line TR max.+TSU:DAT = 1000 + 250 = 1250 ns (according to the Standard mode I²C bus specification), before the SCL line is released.

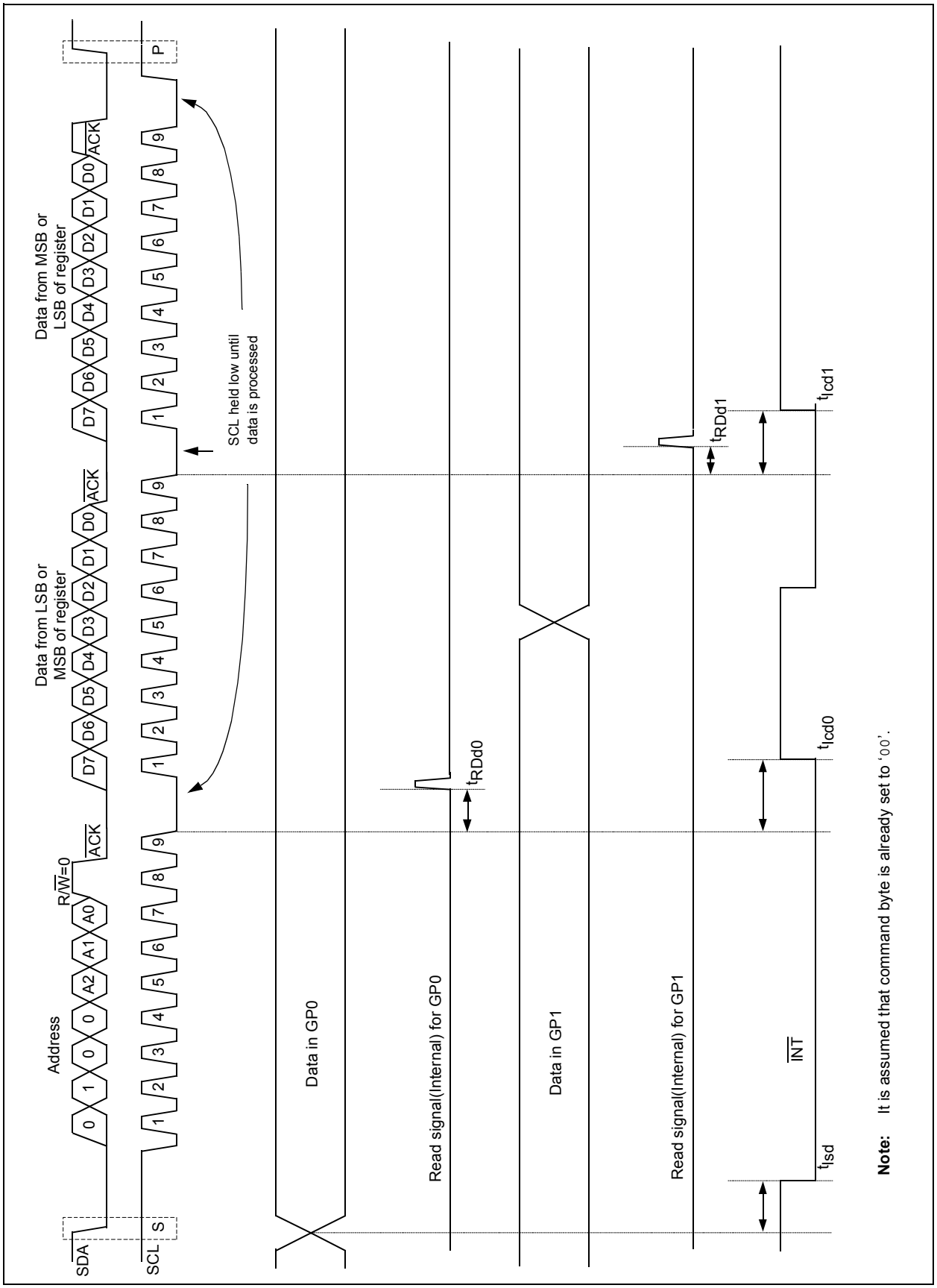
 

**TABLE 2-7: GP0 AND GP1 TIMING REQUIREMENTS**

| Param No. | Symbol | Characteristic | Min | Typ. | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | $t_{GPV0}$ | GP0 output data valid time | — | 40 | — | µs | TP = 1 MHz |
| | $t_{GPV1}$ | GP1 output data valid time | — | 50 | — | µs | |
| | $t_{RDD0}$ | GP0 data read delay time | — | 40 | — | µs | |
| | $t_{RDD1}$ | GP1 data read delay time | — | 50 | — | µs | |
| | $t_{ISD0}$ | GP0 Interrupt set delay time | — | — | 200 | µs | IARES = 1, TP = 1 MHz |
| | | | — | — | 32 | ms | IARES = 0, TP = 1 MHz |
| | $t_{ISD1}$ | GP1 Interrupt set delay time | — | — | 200 | µs | IARES = 1, TP = 1 MHz |
| | | | — | — | 32 | ms | IARES = 0, TP = 1 MHz |
| | $t_{LCD0}$ | GP0 Interrupt clear delay time (for read) | — | 100 | — | µs | TP = 1 MHz |
| | $t_{LCD1}$ | GP1 Interrupt clear delay time (for read) | — | 100 | — | µs | |

**Note 1:** These parameters are characterized but not tested.

**FIGURE 2-5: GP0 AND GP1 PORT TIMINGS**

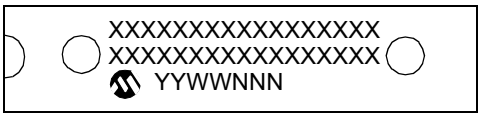


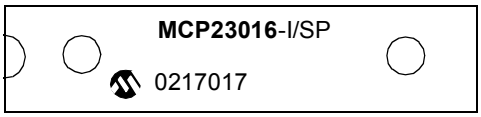
## 3.0 PACKAGE INFORMATION

### 3.1 Package Marking Information

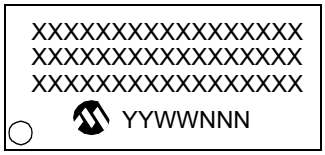
**28-Lead PDIP (Skinny DIP)**



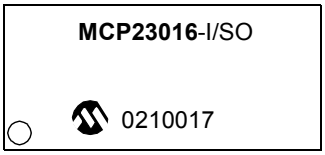

**Example:**




**28-Lead SOIC**

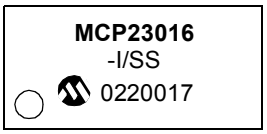



**Example:**




**28-Lead SSOP**


**Example:**




**28-Lead QFN**

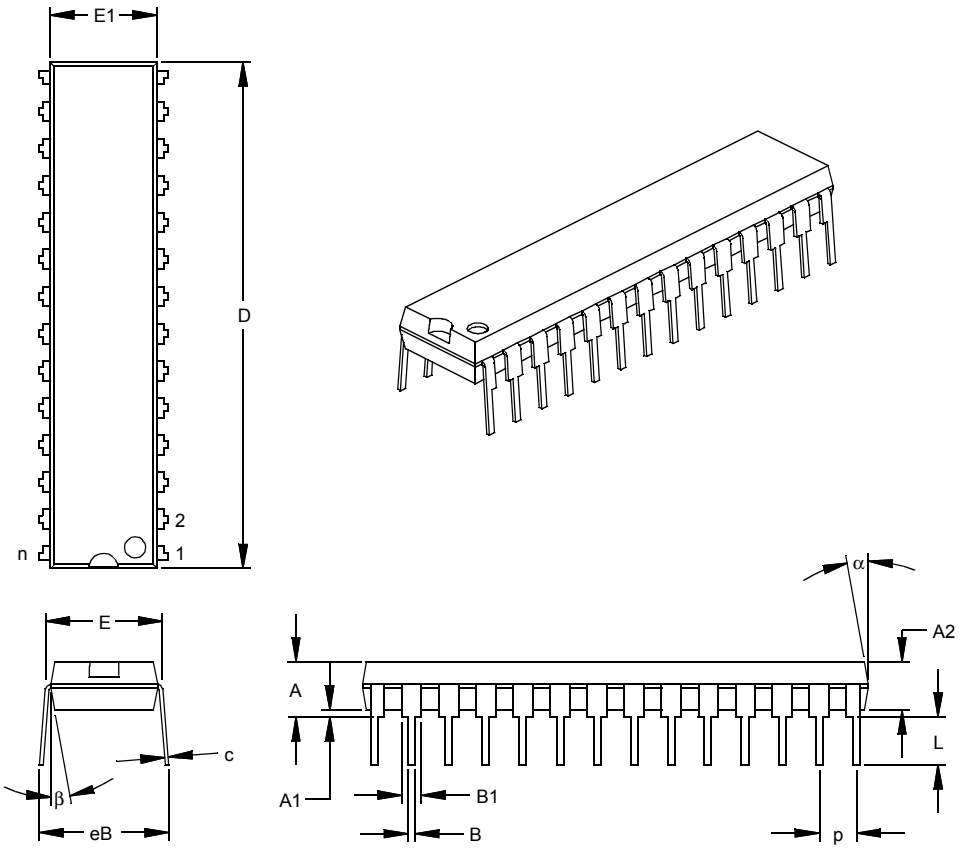

**Example:**


| | | |
|---|---|---|
| **Legend:** | XX...X | Customer specific information* |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard marking consists of Microchip part number, year code, week code, and traceability code. Please check with your Microchip Sales Office.

### 28-Lead Skinny Plastic Dual In-line (SP) – 300 mil (PDIP)

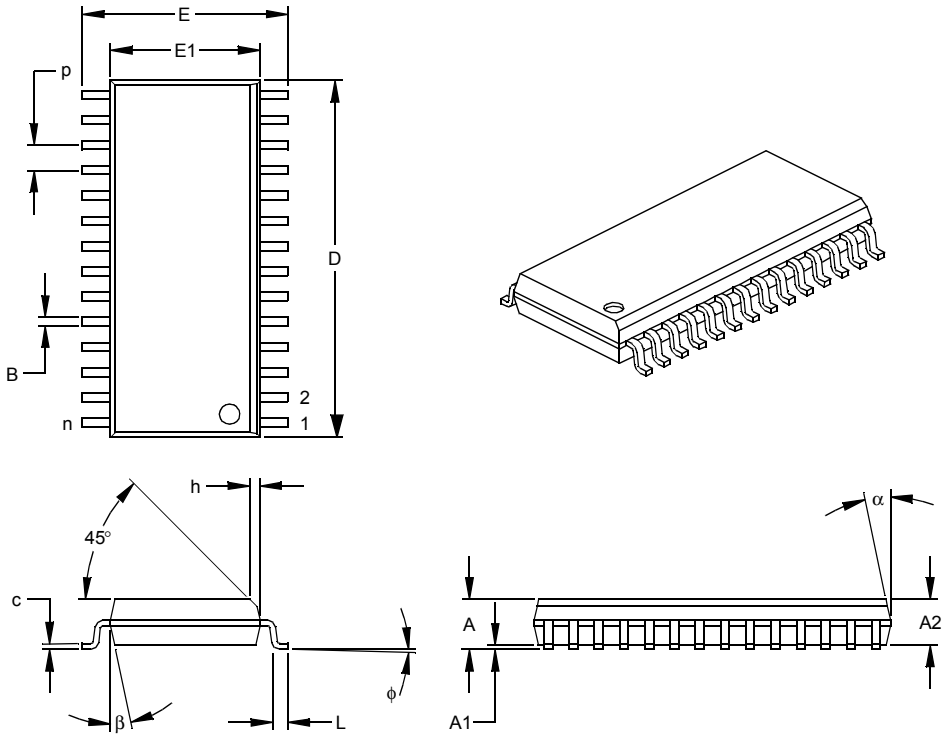



| Units | | INCHES* | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 28 | | | 28 | |
| Pitch | p | | .100 | | | 2.54 | |
| Top to Seating Plane | A | .140 | .150 | .160 | 3.56 | 3.81 | 4.06 |
| Molded Package Thickness | A2 | .125 | .130 | .135 | 3.18 | 3.30 | 3.43 |
| Base to Seating Plane | A1 | .015 | | | 0.38 | | |
| Shoulder to Shoulder Width | E | .300 | .310 | .325 | 7.62 | 7.87 | 8.26 |
| Molded Package Width | E1 | .275 | .285 | .295 | 6.99 | 7.24 | 7.49 |
| Overall Length | D | 1.345 | 1.365 | 1.385 | 34.16 | 34.67 | 35.18 |
| Tip to Seating Plane | L | .125 | .130 | .135 | 3.18 | 3.30 | 3.43 |
| Lead Thickness | c | .008 | .012 | .015 | 0.20 | 0.29 | 0.38 |
| Upper Lead Width | B1 | .040 | .053 | .065 | 1.02 | 1.33 | 1.65 |
| Lower Lead Width | B | .016 | .019 | .022 | 0.41 | 0.48 | 0.56 |
| Overall Row Spacing § | eB | .320 | .350 | .430 | 8.13 | 8.89 | 10.92 |
| Mold Draft Angle Top | α | 5 | 10 | 15 | 5 | 10 | 15 |
| Mold Draft Angle Bottom | β | 5 | 10 | 15 | 5 | 10 | 15 |

* Controlling Parameter
§ Significant Characteristic
Notes:
Dimension D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MO-095
Drawing No. C04-070

## 28-Lead Plastic Small Outline (SO) – Wide, 300 mil (SOIC)

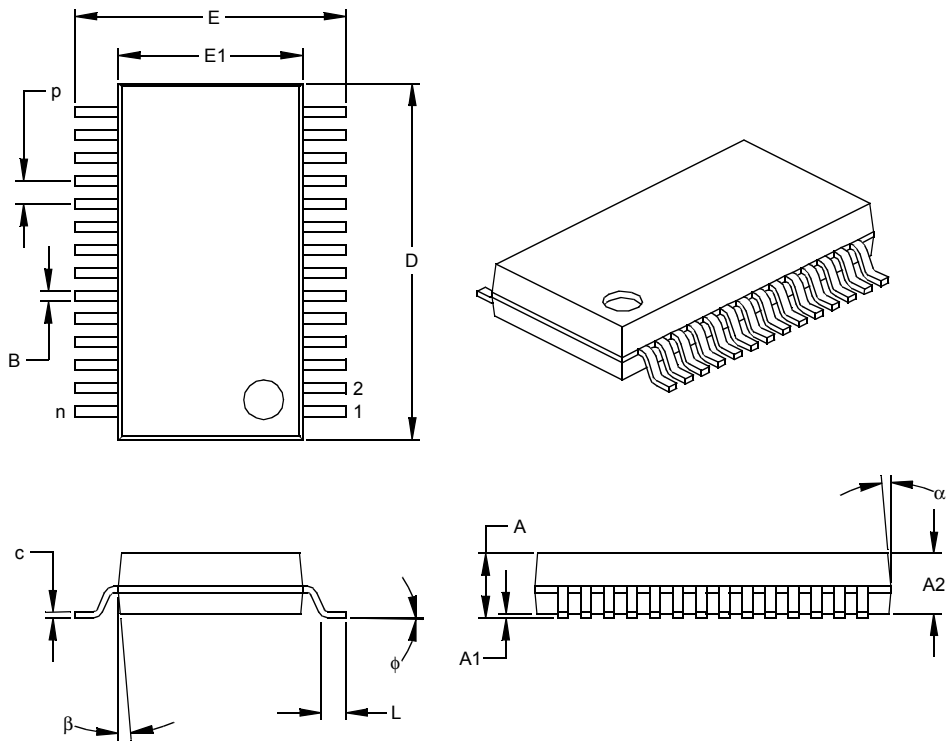



| Units | | INCHES* | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 28 | | | 28 | |
| Pitch | p | | .050 | | | 1.27 | |
| Overall Height | A | .093 | .099 | .104 | 2.36 | 2.50 | 2.64 |
| Molded Package Thickness | A2 | .088 | .091 | .094 | 2.24 | 2.31 | 2.39 |
| Standoff § | A1 | .004 | .008 | .012 | 0.10 | 0.20 | 0.30 |
| Overall Width | E | .394 | .407 | .420 | 10.01 | 10.34 | 10.67 |
| Molded Package Width | E1 | .288 | .295 | .299 | 7.32 | 7.49 | 7.59 |
| Overall Length | D | .695 | .704 | .712 | 17.65 | 17.87 | 18.08 |
| Chamfer Distance | h | .010 | .020 | .029 | 0.25 | 0.50 | 0.74 |
| Foot Length | L | .016 | .033 | .050 | 0.41 | 0.84 | 1.27 |
| Foot Angle Top | φ | 0 | 4 | 8 | 0 | 4 | 8 |
| Lead Thickness | c | .009 | .011 | .013 | 0.23 | 0.28 | 0.33 |
| Lead Width | B | .014 | .017 | .020 | 0.36 | 0.42 | 0.51 |
| Mold Draft Angle Top | α | 0 | 12 | 15 | 0 | 12 | 15 |
| Mold Draft Angle Bottom | β | 0 | 12 | 15 | 0 | 12 | 15 |

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-013
Drawing No. C04-052

### 28-Lead Plastic Shrink Small Outline (SS) – 209 mil, 5.30 mm (SSOP)



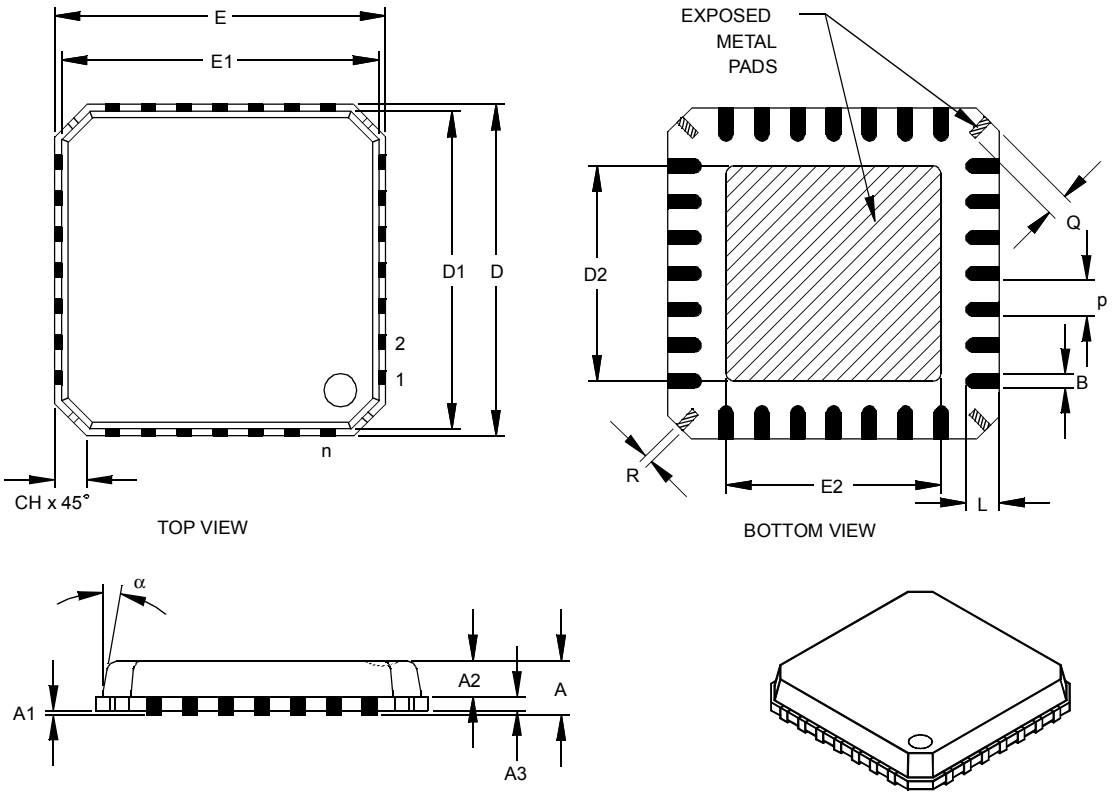

| Units | | INCHES | | | MILLIMETERS* | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 28 | | | 28 | |
| Pitch | p | | .026 | | | 0.65 | |
| Overall Height | A | .068 | .073 | .078 | 1.73 | 1.85 | 1.98 |
| Molded Package Thickness | A2 | .064 | .068 | .072 | 1.63 | 1.73 | 1.83 |
| Standoff § | A1 | .002 | .006 | .010 | 0.05 | 0.15 | 0.25 |
| Overall Width | E | .299 | .309 | .319 | 7.59 | 7.85 | 8.10 |
| Molded Package Width | E1 | .201 | .207 | .212 | 5.11 | 5.25 | 5.38 |
| Overall Length | D | .396 | .402 | .407 | 10.06 | 10.20 | 10.34 |
| Foot Length | L | .022 | .030 | .037 | 0.56 | 0.75 | 0.94 |
| Lead Thickness | c | .004 | .007 | .010 | 0.10 | 0.18 | 0.25 |
| Foot Angle | ϕ | 0 | 4 | 8 | 0.00 | 101.60 | 203.20 |
| Lead Width | B | .010 | .013 | .015 | 0.25 | 0.32 | 0.38 |
| Mold Draft Angle Top | α | 0 | 5 | 10 | 0 | 5 | 10 |
| Mold Draft Angle Bottom | β | 0 | 5 | 10 | 0 | 5 | 10 |

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-150
Drawing No. C04-073

## 28-Lead Plastic Quad Flat No Leads Package (ML) 6x6 mm Body (QFN)



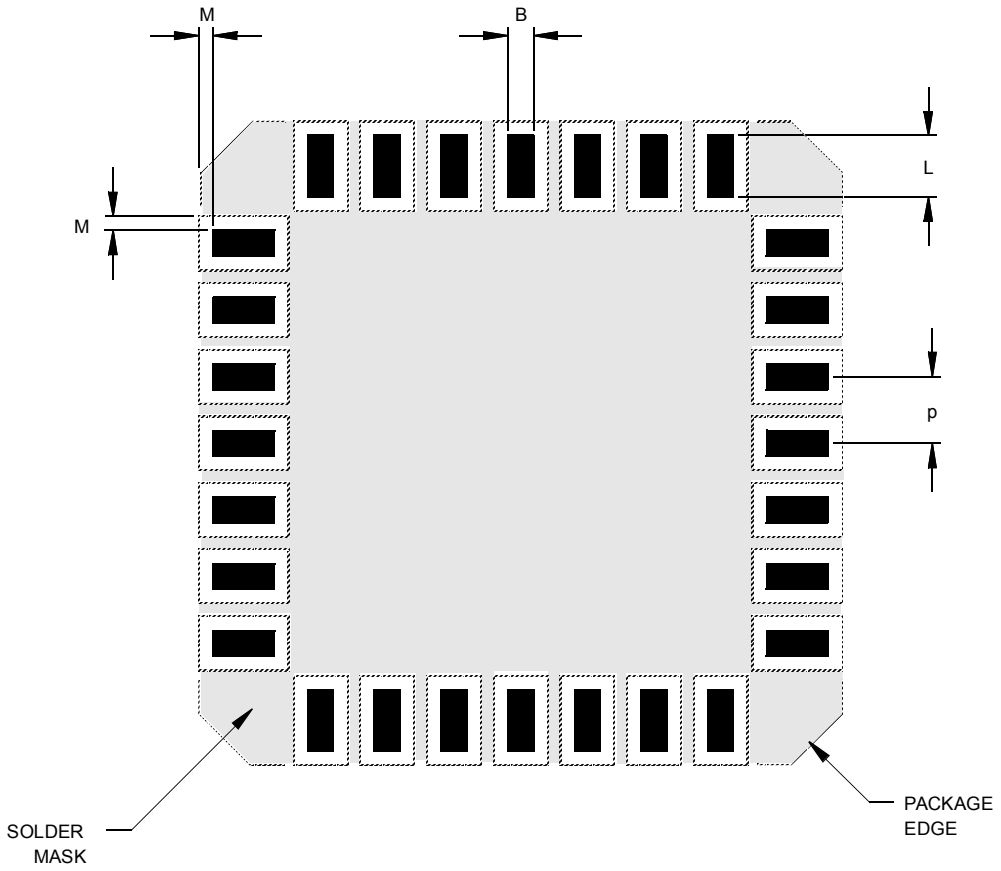

| Units | | INCHES | | | MILLIMETERS* | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 28 | | | 28 | |
| Pitch | p | | .026 BSC | | | 0.65 BSC | |
| Overall Height | A | | .033 | .039 | | 0.85 | 1.00 |
| Molded Package Thickness | A2 | | .026 | .031 | | 0.65 | 0.80 |
| Standoff | A1 | .000 | .0004 | .002 | 0.00 | 0.01 | 0.05 |
| Base Thickness | A3 | | .008 REF. | | | 0.20 REF. | |
| Overall Width | E | | .236 BSC | | | 6.00 BSC | |
| Molded Package Width | E1 | | .226 BSC | | | 5.75 BSC | |
| Exposed Pad Width | E2 | .140 | .146 | .152 | 3.55 | 3.70 | 3.85 |
| Overall Length | D | | .236 BSC | | | 6.00 BSC | |
| Molded Package Length | D1 | | .226 BSC | | | 5.75 BSC | |
| Exposed Pad Length | D2 | .140 | .146 | .152 | 3.55 | 3.70 | 3.85 |
| Lead Width | B | .009 | .011 | .014 | 0.23 | 0.28 | 0.35 |
| Lead Length | L | .020 | .024 | .030 | 0.50 | 0.60 | 0.75 |
| Tie Bar Width | R | .005 | .007 | .010 | 0.13 | 0.17 | 0.23 |
| Tie Bar Length | Q | .012 | .016 | .026 | 0.30 | 0.40 | 0.65 |
| Chamfer | CH | .009 | .017 | .024 | 0.24 | 0.42 | 0.60 |
| Mold Draft Angle Top | α | | | 12° | | | 12° |

* Controlling Parameter

**Notes:** Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC equivalent: pending

Drawing No. C04-114

### 28-Lead Plastic Quad Flat No Leads Package (ML) 6x6 mm Body (QFN) (Continued)




| Units | | INCHES | | | MILLIMETERS* | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Pitch | p | .026 BSC | | | 0.65 BSC | | |
| Pad Width | B | .009 | .011 | .014 | 0.23 | 0.28 | 0.35 |
| Pad Length | L | .020 | .024 | .030 | 0.50 | 0.60 | 0.75 |
| Pad to Solder Mask | M | .005 | | .006 | 0.13 | | 0.15 |

*Controlling Parameter

Drawing No. C04-2114

## APPENDIX A: REVISION HISTORY

### Revision A (December 2002)

Original data sheet for MCP23016 device.

**NOTES:**

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information (e.g., on pricing or delivery) refer to the factory or the listed sales office.

| PART NO. | X | /XX |
|---|---|---|
| Device | Temperature Range | Package |

| | | |
|---|---|---|
| Device: | MCP23016: 16-Bit I2C I/O Expander | |
| Temperature Range: | I | = -40°C to +85°C |
| Package: | SP | = Plastic DIP (300 mil Body), 28-lead |
| | SO | = Plastic SOIC, Wide (300 mil Body), 28-lead |
| | SS | = Plastic SOIC, (209 mil, 5.30mm), 28-lead |
| | ML | = Plastic Quad, Flat No Leads (QFN), 28-lead |

**Examples:**

a) MCP23016-I/P: Industrial Temperature, PDIP package.

b) MCP23016-I/SO: Industrial Temperature, SOIC package.

c) MCP23016-I/SS: Industrial Temperature, SOIC package.

d) MCP23016-I/ML: Industrial Temperature, QFN package.

### Sales and Support

**Data Sheets**
Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

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**NOTES:**

 

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- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products.



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2355 West Chandler Blvd.
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**Kokomo**
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Tel: 765-864-8360 Fax: 765-864-8387

**Los Angeles**
18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1888 Fax: 949-263-1338

**San Jose**
Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

**Toronto**
6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699 Fax: 905-673-6509

## ASIA/PACIFIC

**Australia**
Microchip Technology Australia Pty Ltd
Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

**China - Beijing**
Microchip Technology Consulting (Shanghai) Co., Ltd., Beijing Liaison Office
Unit 915
Bei Hai Wan Tai Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100 Fax: 86-10-85282104

**China - Chengdu**
Microchip Technology Consulting (Shanghai) Co., Ltd., Chengdu Liaison Office
Rm. 2401, 24th Floor,
Ming Xing Financial Tower
No. 88 TIDU Street
Chengdu 610016, China
Tel: 86-28-86766200 Fax: 86-28-86766599

**China - Fuzhou**
Microchip Technology Consulting (Shanghai) Co., Ltd., Fuzhou Liaison Office
Unit 28F, World Trade Plaza
No. 71 Wusi Road
Fuzhou 350001, China
Tel: 86-591-7503506 Fax: 86-591-7503521

**China - Shanghai**
Microchip Technology Consulting (Shanghai) Co., Ltd.
Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

**China - Shenzhen**
Microchip Technology Consulting (Shanghai) Co., Ltd., Shenzhen Liaison Office
Rm. 1315, 13/F, Shenzhen Kerry Centre,
Renminnan Lu
Shenzhen 518001, China
Tel: 86-755-82350361 Fax: 86-755-82366086

**China - Hong Kong SAR**
Microchip Technology Hongkong Ltd.
Unit 901-6, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200 Fax: 852-2401-3431

**India**
Microchip Technology Inc.
India Liaison Office
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaugnessey Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

**Japan**
Microchip Technology Japan K.K.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471- 6166 Fax: 81-45-471-6122

**Korea**
Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea 135-882
Tel: 82-2-554-7200 Fax: 82-2-558-5934

**Singapore**
Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-6334-8870 Fax: 65-6334-8850

**Taiwan**
Microchip Technology (Barbados) Inc.,
Taiwan Branch
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

## EUROPE

**Austria**
Microchip Technology Austria GmbH
Durisolstrasse 2
A-4600 Wels
Austria
Tel: 43-7242-2244-399
Fax: 43-7242-2244-393

**Denmark**
Microchip Technology Nordic ApS
Regus Business Centre
Lautrup hoj 1-3
Ballerup DK-2750 Denmark
Tel: 45 4420 9895 Fax: 45 4420 9910

**France**
Microchip Technology SARL
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - ler Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

**Germany**
Microchip Technology GmbH
Steinheilstrasse 10
D-85737 Ismaning, Germany
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

**Italy**
Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Taurus 1 V. Le Colleoni 1
20041 Agrate Brianza
Milan, Italy
Tel: 39-039-65791-1 Fax: 39-039-6899883

**United Kingdom**
Microchip Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44 118 921 5869 Fax: 44-118 921-5820

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