# Stratix Device Handbook, Volume 1

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# Contents

## Section I. Stratix Device Family Data Sheet

### Chapter 1. Introduction

### Chapter 2. Stratix Architecture

## Chapter 3. Configuration & Testing

## Chapter 4. DC & Switching Characteristics

## Chapter 5. Reference & Ordering Information

## Index

# Chapter Revision Dates

The chapters in this book, *Stratix Device Handbook, Volume 1*, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

Chapter 1. Introduction
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Chapter 2. Stratix Architecture
Revised: *April 2003*
Part number: *S51002-1.0*

Chapter 3. Configuration & Testing
Revised: *April 2003*
Part number: *S51003-1.0*

Chapter 4. DC & Switching Characteristics
Revised: *May 2003*
Part number: *S51004-1.1*

Chapter 5. Reference & Ordering Information
Revised: *April 2003*
Part number: *S51005-1.0*

# About this Handbook

This handbook provides comprehensive information about the Altera® Stratix family of devices.

## How to Find Information

You can find more information in the following ways:

- The Adobe Acrobat Find feature, which searches the text of a PDF document. Click the binoculars toolbar icon to open the Find dialog box.
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***Note to table:***

(1) You can also contact your local Altera sales office or sales representative.

# Typographic Conventions

This document uses the typographic conventions shown below.

| Visual Cue | Meaning |
|---|---|
| **Bold Type with Initial Capital Letters** | Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: **Save As** dialog box. |
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| *Italic type* | Internal timing parameters and variables are shown in italic type. Examples: $t_{PIA}$, $n + 1$.<br>Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: <*file name*>, <*project name*>**.pof** file. |
| Initial Capital Letters | Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu. |
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| 1., 2., 3., and<br>a., b., c., etc. | Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure. |
| ■ ● • | Bullets are used in a list of items when the sequence of the items is not important. |
| ✓ | The checkmark indicates a procedure that consists of one step only. |
| ☞ | The hand points to information that requires special attention. |
| ↵ | The angled arrow indicates you should press the Enter key. |
| 👣 | The feet direct you to more information on a particular topic. |

# Section I. Stratix Device Family Data Sheet

This section provides designers with the data sheet specifications for Stratix devices. They contain feature definitions of the internal architecture, configuration and JTAG boundary-scan testing information, DC operating conditions, AC timing parameters, a reference to power consumption, and ordering information for Stratix devices.

This section contains the following chapters:

- Chapter 1. Introduction
- Chapter 2. Stratix Architecture
- Chapter 3. Configuration & Testing
- Chapter 4. DC & Switching Characteristics
- Chapter 5. Reference & Ordering Information

## Revision History

The table below shows the revision history for Chapters 1 through 5.

| Chapter(s) | Date / Version | Changes Made |
|---|---|---|
| 1 | April 2003<br>v1.0 | Updated internal and external timing information. Added the "Maximum Input & Output Clock Rates" section. |
| 2 | April 2003<br>v1.0 | Updated internal and external timing information. Added the "Maximum Input & Output Clock Rates" section. |
| 3 | April 2003<br>v1.0 | Updated internal and external timing information. Added the "Maximum Input & Output Clock Rates" section. |
| 4 | May 2003<br>v1.1 | Updated high-speed I/O specification timing. |
|  | April 2003<br>v1.0 | Updated internal and external timing information. Added the "Maximum Input & Output Clock Rates" section. |
| 5 | April 2003<br>v1.0 | Updated internal and external timing information. Added the "Maximum Input & Output Clock Rates" section. |

# 1. Introduction

S51001-1.0

Chapter 1, Introduction, replaces the Stratix Family Data Sheet.

## Introduction

The Stratix™ family of FPGAs is based on a 1.5-V, 0.13-µm, all-layer copper SRAM process, with densities up to 114,140 logic elements (LEs) and up to 10 Mbits of RAM. Stratix devices offer up to 28 digital signal processing (DSP) blocks with up to 224 (9-bit × 9-bit) embedded multipliers, optimized for DSP applications that enable efficient implementation of high-performance filters and multipliers. Stratix devices support various I/O standards and also offer a complete clock management solution with its hierarchical clock structure with up to 420-MHz performance and up to 12 phase-locked loops (PLLs).

The following shows the main sections in the Stratix Device Family Data Sheet:

## Features

The Stratix family offers the following features:

- 10,570 to 114,140 LEs; see Table 1–1.
- Up to 10,118,016 RAM bits (1,264,752 bytes) available without reducing logic resources
- TriMatrix™ memory consisting of three RAM block sizes to implement true dual-port memory and first-in first-out (FIFO) buffers
- High-speed DSP blocks provide dedicated implementation of multipliers (at up to 250 MHz), multiply-accumulate functions, and finite impulse response (FIR) filters
- Up to 16 global clocks with 22 clocking resources per device region
- Up to 12 PLLs (four enhanced PLLs and eight fast PLLs) per device provide spread spectrum, programmable bandwidth, clock switch-over, real-time PLL reconfiguration, and advanced multiplication and phase shifting
- Support for numerous single-ended and differential I/O standards
- High-speed differential I/O support on up to 116 channels with up to 80 channels optimized for 840 megabits per second (Mbps)
- Support for high-speed networking and communications bus standards including RapidIO, UTOPIA IV, CSIX, HyperTransport™ technology, 10G Ethernet XSBI, SPI-4 Phase 2 (POS-PHY Level 4), and SFI-4
- Terminator™ technology provides on-chip termination for differential and single-ended I/O pins with impedance matching
- Support for high-speed external memory, including zero bus turnaround (ZBT) SRAM, quad data rate (QDR and QDRII) SRAM, double data rate (DDR) SDRAM, DDR fast cycle RAM (FCRAM), and single data rate (SDR) SDRAM
- Support for multiple intellectual property megafunctions from Altera MegaCore® functions and Altera Megafunction Partners Program (AMPP℠) megafunctions
- Support for remote configuration updates

*Table 1–1. Stratix Device Features — EP1S10, EP1S20, EP1S25, EP1S30*

| Feature | EP1S10 | EP1S20 | EP1S25 | EP1S30 |
|---|---|---|---|---|
| LEs | 10,570 | 18,460 | 25,660 | 32,470 |
| M512 RAM blocks (32 × 18 bits) | 94 | 194 | 224 | 295 |
| M4K RAM blocks (128 × 36 bits) | 60 | 82 | 138 | 171 |
| M-RAM blocks (4K × 144 bits) | 1 | 2 | 2 | 4 |
| Total RAM bits | 920,448 | 1,669,248 | 1,944,576 | 3,317,184 |
| DSP blocks | 6 | 10 | 10 | 12 |
| Embedded multipliers *(1)* | 48 | 80 | 80 | 96 |
| PLLs | 6 | 6 | 6 | 10 |
| Maximum user I/O pins | 426 | 586 | 706 | 726 |

*Table 1–2. Stratix Device Features — EP1S40, EP1S60, EP1S80*

| Feature | EP1S40 | EP1S60 | EP1S80 |
|---|---|---|---|
| LEs | 41,250 | 57,120 | 79,040 |
| M512 RAM blocks (32 × 18 bits) | 384 | 574 | 767 |
| M4K RAM blocks (128 × 36 bits) | 183 | 292 | 364 |
| M-RAM blocks (4K × 144 bits) | 4 | 6 | 9 |
| Total RAM bits | 3,423,744 | 5,215,104 | 7,427,520 |
| DSP blocks | 14 | 18 | 22 |
| Embedded multipliers *(1)* | 112 | 144 | 176 |
| PLLs | 12 | 12 | 12 |
| Maximum user I/O pins | 822 | 1,022 | 1,238 |

***Note to Tables 1–1 and 1–2:***

(1) This parameter lists the total number of 9 × 9-bit multipliers for each device. For the total number of 18 × 18-bit multipliers per device, divide the total number of 9 × 9-bit multipliers by 2. For the total number of 36 × 36-bit multipliers per device, divide the total number of 9 × 9-bit multipliers by 8.

Stratix devices are available in space-saving FineLine BGA™ and ball-grid array (BGA) packages (see Tables 1–3 through 1–5). All Stratix devices support vertical migration within the same package (e.g., the designer can migrate between the EP1S10, EP1S20, and EP1S25 devices in the 672-pin BGA package). Vertical migration means that designers can migrate to devices whose dedicated pins, configuration pins, and power pins are the same for a given package across device densities. For I/O pin migration across densities, the designer must cross reference the available I/O pins using the device pin-outs for all planned densities of a given package type to identify which I/O pins are migratable. The Quartus® II software can automatically cross reference and place all pins except differential pins for migration when given a device migration list. The designer must use the pin-outs for each device to verify the differential placement migration. A future version of the Quartus II software will support differential pin migration.

*Table 1–3. Stratix Package Options & I/O Pin Counts*

| Device | 672-Pin BGA | 956-Pin BGA | 484-Pin FineLine BGA | 672-Pin FineLine BGA | 780-Pin FineLine BGA | 1,020-Pin FineLine BGA | 1,508-Pin FineLine BGA |
|---|---|---|---|---|---|---|---|
| EP1S10 | 345 | | 335 | 345 | 426 | | |
| EP1S20 | 426 | | 361 | 426 | 586 | | |
| EP1S25 | 473 | | | 473 | 597 | 706 | |
| EP1S30 | | 683 | | | 597 | 726 | |
| EP1S40 | | 683 | | | 615 | 773 | 822 |
| EP1S60 | | 683 | | | | 773 | 1,022 |
| EP1S80 | | 683 | | | | 773 | 1,203 |

*Note to Table 1–3:*

(1) All I/O pin counts include 20 dedicated clock input pins (clk[15..0], clk0n, clk2n, clk9n, and clk11n) that can be used for data inputs.

*Table 1–4. Stratix BGA Package Sizes*

| Dimension | 672 Pin | 956 Pin |
|---|---|---|
| Pitch (mm) | 1.27 | 1.27 |
| Area (mm$^2$) | 1,225 | 1,600 |
| Length × width (mm × mm) | 35 × 35 | 40 × 40 |

**Table 1–5. Stratix FineLine BGA Package Sizes**

| Dimension | 484 Pin | 672 Pin | 780 Pin | 1,020 Pin | 1,508 Pin | 1,923 Pin |
|---|---|---|---|---|---|---|
| Pitch (mm) | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 |
| Area (mm$^2$) | 529 | 729 | 841 | 1,089 | 1,600 | 2,025 |
| Length × width (mm × mm) | 23 × 23 | 27 × 27 | 29 × 29 | 33 × 33 | 40 × 40 | 45 × 45 |

Stratix devices are available in up to three speed grades, -5, -6, and -7, with -5 being the fastest. Table 1–6 shows Stratix device speed-grade offerings.

**Table 1–6. Stratix Device Speed Grades**

| Device | 672-Pin BGA | 956-Pin BGA | 484-Pin FineLine BGA | 672-Pin FineLine BGA | 780-Pin FineLine BGA | 1,020-Pin FineLine BGA | 1,508-Pin FineLine BGA | 1,923-Pin FineLine BGA |
|---|---|---|---|---|---|---|---|---|
| EP1S10 | -6, -7 | | -5, -6, -7 | -6, -7 | -5, -6, -7 | | | |
| EP1S20 | -6, -7 | | -5, -6, -7 | -6, -7 | -5, -6, -7 | | | |
| EP1S25 | -6, -7 | | | -6, -7 | -5, -6, -7 | -5, -6, -7 | | |
| EP1S30 | | -5, -6, -7 | | | -5, -6, -7 | -5, -6, -7 | | |
| EP1S40 | | -5, -6, -7 | | | | -5, -6, -7 | -5, -6, -7 | |
| EP1S60 | | -6, -7 | | | | -6, -7 | -6, -7 | |
| EP1S80 | | -6, -7 | | | | | -6, -7 | *(1)* |

*Note to Table 1–6:*

(1) Contact Altera Applications for up to date information on availability for these devices.

# 2. Stratix Architecture

S51002-1.0

Chapter 2, Stratix Architecture, replaces the Stratix Family Data Sheet.

## Functional Description

Stratix devices contain a two-dimensional row- and column-based architecture to implement custom logic. A series of column and row interconnects of varying length and speed provides signal interconnects between logic array blocks (LABs), memory block structures, and DSP blocks.

The logic array consists of LABs, with 10 logic elements (LEs) in each LAB. An LE is a small unit of logic providing efficient implementation of user logic functions. LABs are grouped into rows and columns across the device.

M512 RAM blocks are simple dual-port memory blocks with 512 bits plus parity (576 bits). These blocks provide dedicated simple dual-port or single-port memory up to 18-bits wide at up to 318 MHz. M512 blocks are grouped into columns across the device in between certain LABs.

M4K RAM blocks are true dual-port memory blocks with 4K bits plus parity (4,608 bits). These blocks provide dedicated true dual-port, simple dual-port, or single-port memory up to 36-bits wide at up to 291 MHz. These blocks are grouped into columns across the device in between certain LABs.

M-RAM blocks are true dual-port memory blocks with 512K bits plus parity (589,824 bits). These blocks provide dedicated true dual-port, simple dual-port, or single-port memory up to 144-bits wide at up to 269 MHz. Several M-RAM blocks are located individually or in pairs within the device’s logic array.

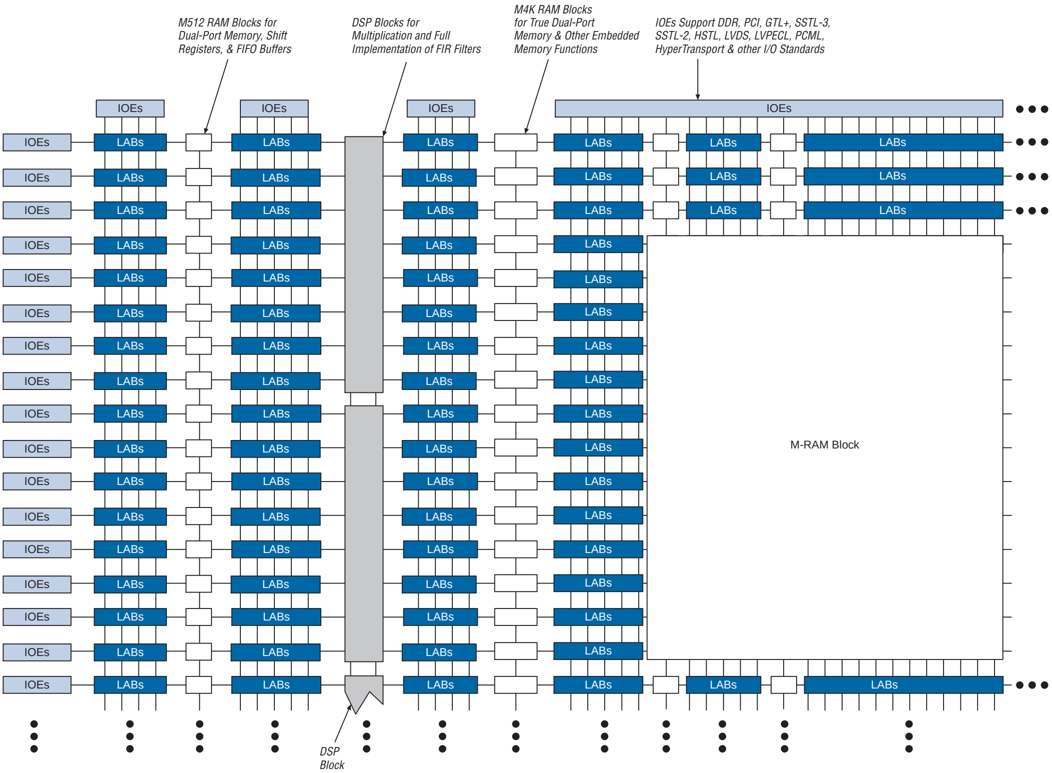
Digital signal processing (DSP) blocks can implement up to either eight full-precision 9 × 9-bit multipliers, four full-precision 18 × 18-bit multipliers, or one full-precision 36 × 36-bit multiplier with add or subtract features. These blocks also contain 18-bit input shift registers for digital signal processing applications, including FIR and infinite impulse response (IIR) filters. DSP blocks are grouped into two columns in each device.

Each Stratix device I/O pin is fed by an I/O element (IOE) located at the end of LAB rows and columns around the periphery of the device. I/O pins support numerous single-ended and differential I/O standards. Each IOE contains a bidirectional I/O buffer and six registers for registering input, output, and output-enable signals. When used with dedicated clocks, these registers provide exceptional performance and interface support with external memory devices such as DDR SDRAM, FCRAM, ZBT, and QDR SRAM devices.

High-speed serial interface channels support transfers at up to 840 Mbps using LVDS, LVPECL, 3.3-V PCML, or HyperTransport technology I/O standards.

Figure 2–1 shows an overview of the Stratix device.

***Figure 2–1. Stratix Block Diagram***



The number of M512 RAM, M4K RAM, and DSP blocks varies by device along with row and column numbers and M-RAM blocks. Table 2–1 lists the resources available in Stratix devices.

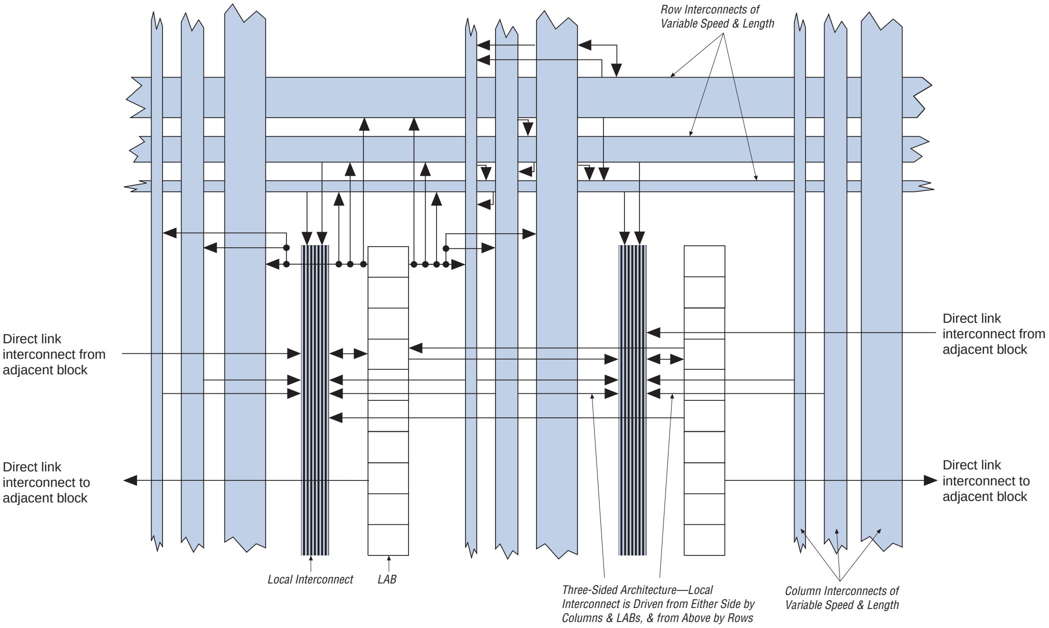
*Table 2–1. Stratix Device Resources*

| Device | M512 RAM Columns/Blocks | M4K RAM Columns/Blocks | M-RAM Blocks | DSP Block Columns/Blocks | LAB Columns | LAB Rows |
|---|---|---|---|---|---|---|
| EP1S10 | 4 / 94 | 2 / 60 | 1 | 2 / 6 | 40 | 30 |
| EP1S20 | 6 / 194 | 2 / 82 | 2 | 2 / 10 | 52 | 41 |
| EP1S25 | 6 / 224 | 3 / 138 | 2 | 2 / 10 | 62 | 46 |
| EP1S30 | 7 / 295 | 3 / 171 | 4 | 2 / 12 | 67 | 57 |
| EP1S40 | 8 / 384 | 3 / 183 | 4 | 2 / 14 | 77 | 61 |
| EP1S60 | 10 / 574 | 4 / 292 | 6 | 2 / 18 | 90 | 73 |
| EP1S80 | 11 / 767 | 4 / 364 | 9 | 2 / 22 | 101 | 91 |

## Logic Array Blocks

Each LAB consists of 10 LEs, LE carry chains, LAB control signals, local interconnect, LUT chain, and register chain connection lines. The local interconnect transfers signals between LEs in the same LAB. LUT chain connections transfer the output of one LE's LUT to the adjacent LE for fast sequential LUT connections within the same LAB. Register chain connections transfer the output of one LE's register to the adjacent LE's register within an LAB. The Quartus II Compiler places associated logic within an LAB or adjacent LABs, allowing the use of local, LUT chain, and register chain connections for performance and area efficiency. Figure 2–2 shows the Stratix LAB.

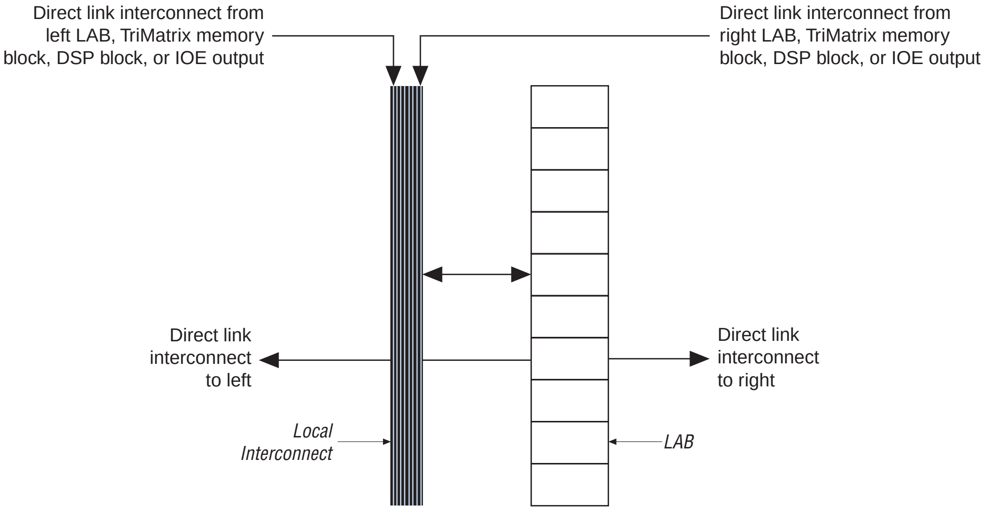
*Figure 2–2. Stratix LAB Structure*



## LAB Interconnects

The LAB local interconnect can drive LEs within the same LAB. The LAB local interconnect is driven by column and row interconnects and LE outputs within the same LAB. Neighboring LABs, M512 RAM blocks, M4K RAM blocks, or DSP blocks from the left and right can also drive an LAB's local interconnect through the direct link connection. The direct link connection feature minimizes the use of row and column interconnects, providing higher performance and flexibility. Each LE can drive 30 other LEs through fast local and direct link interconnects. Figure 2–3 shows the direct link connection.

*Figure 2–3. Direct Link Connection*



## LAB Control Signals

Each LAB contains dedicated logic for driving control signals to its LEs. The control signals include two clocks, two clock enables, two asynchronous clears, synchronous clear, asynchronous preset/load, synchronous load, and add/subtract control signals. This gives a maximum of 10 control signals at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

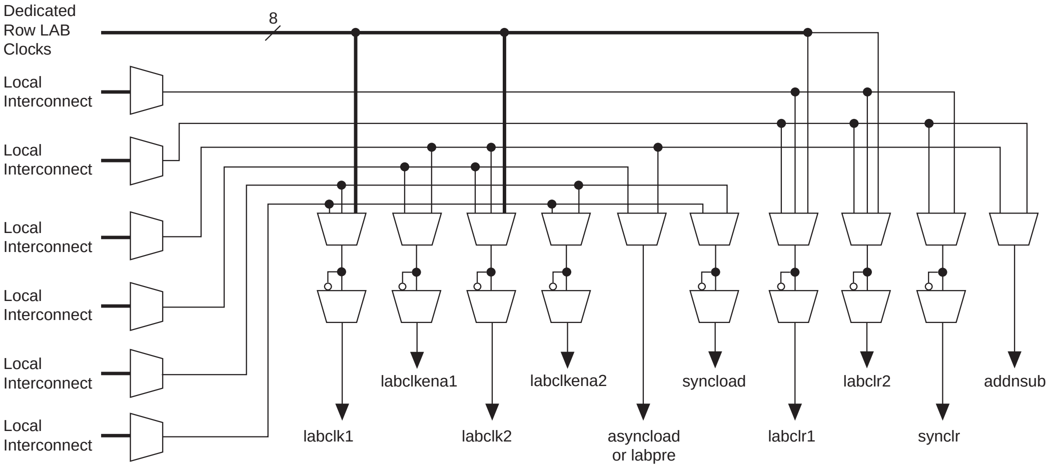
Each LAB can use two clocks and two clock enable signals. Each LAB's clock and clock enable signals are linked. For example, any LE in a particular LAB using the `labclk1` signal will also use `labclkena1`. If the LAB uses both the rising and falling edges of a clock, it also uses both LAB-wide clock signals. De-asserting the clock enable signal will turn off the LAB-wide clock.

Each LAB can use two asynchronous clear signals and an asynchronous load/preset signal. The asynchronous load acts as a preset when the asynchronous load data input is tied high.

With the LAB-wide `addnsub` control signal, a single LE can implement a one-bit adder and subtractor. This saves LE resources and improves performance for logic functions such as DSP correlators and signed multipliers that alternate between addition and subtraction depending on data.

The LAB row clocks [7..0] and LAB local interconnect generate the LAB-wide control signals. The MultiTrack™ interconnect's inherent low skew allows clock and control signal distribution in addition to data. Figure 2–4 shows the LAB control signal generation circuit.

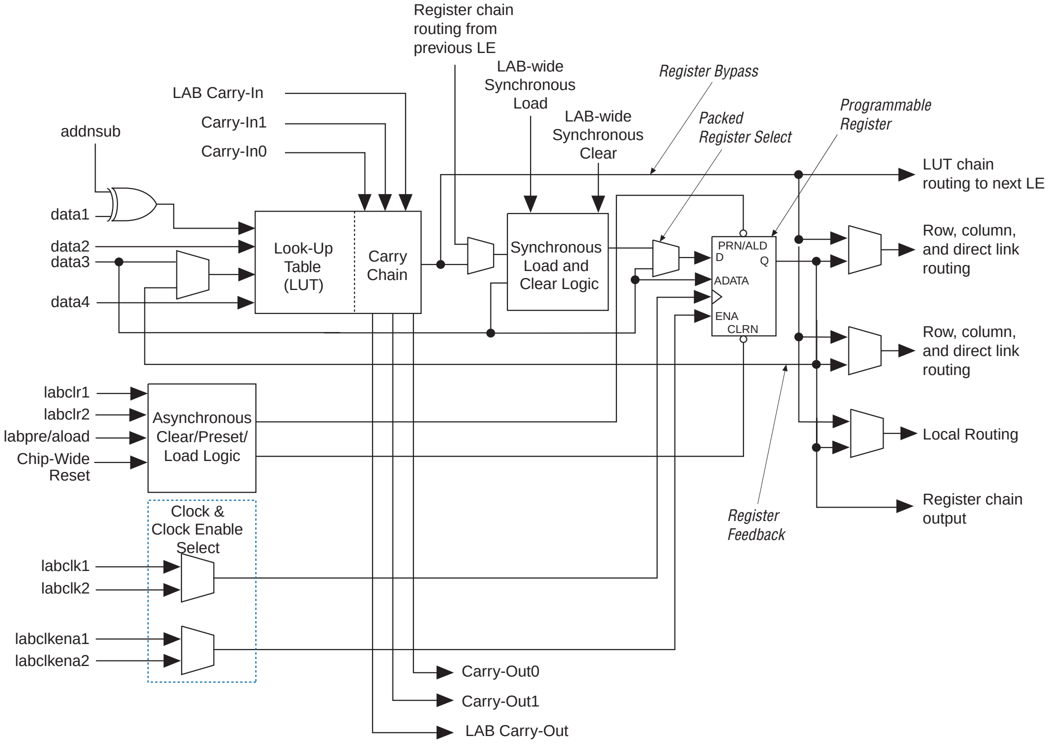
*Figure 2–4. LAB-Wide Control Signals*



## Logic Elements

The smallest unit of logic in the Stratix architecture, the LE, is compact and provides advanced features with efficient logic utilization. Each LE contains a four-input LUT, which is a function generator that can implement any function of four variables. In addition, each LE contains a programmable register and carry chain with carry select capability. A single LE also supports dynamic single bit addition or subtraction mode selectable by an LAB-wide control signal. Each LE drives all types of interconnects: local, row, column, LUT chain, register chain, and direct link interconnects. See Figure 2–5.

***Figure 2–5. Stratix LE***



Each LE's programmable register can be configured for D, T, JK, or SR operation. Each register has data, true asynchronous load data, clock, clock enable, clear, and asynchronous load/preset inputs. Global signals, general-purpose I/O pins, or any internal logic can drive the register's clock and clear control signals. Either general-purpose I/O pins or internal logic can drive the clock enable, preset, asynchronous load, and asynchronous data. The asynchronous load data input comes from the `data3` input of the LE. For combinatorial functions, the register is bypassed and the output of the LUT drives directly to the outputs of the LE.

Each LE has three outputs that drive the local, row, and column routing resources. The LUT or register output can drive these three outputs independently. Two LE outputs drive column or row and direct link routing connections and one drives local interconnect resources. This allows the LUT to drive one output while the register drives another output. This feature, called register packing, improves device utilization because the device can use the register and the LUT for unrelated functions. Another special packing mode allows the register output to feed back into the LUT of the same LE so that the register is packed with its own fan-out LUT. This provides another mechanism for improved fitting. The LE can also drive out registered and unregistered versions of the LUT output.

## LUT Chain & Register Chain

In addition to the three general routing outputs, the LEs within an LAB have LUT chain and register chain outputs. LUT chain connections allow LUTs within the same LAB to cascade together for wide input functions. Register chain outputs allow registers within the same LAB to cascade together. The register chain output allows an LAB to use LUTs for a single combinatorial function and the registers to be used for an unrelated shift register implementation. These resources speed up connections between LABs while saving local interconnect resources. See "MultiTrack Interconnect" on page 2–14 for more information on LUT chain and register chain connections.

## addnsub Signal

The LE's dynamic adder/subtractor feature saves logic resources by using one set of LEs to implement both an adder and a subtractor. This feature is controlled by the LAB-wide control signal `addnsub`. The `addnsub` signal sets the LAB to perform either A + B or A – B. The LUT computes addition, and subtraction is computed by adding the two's complement of the intended subtractor. The LAB-wide signal converts to two's complement by inverting the B bits within the LAB and setting carry-in = 1 to add one to the least significant bit (LSB). The LSB of an adder/subtractor must be placed in the first LE of the LAB, where the LAB-wide `addnsub` signal automatically sets the carry-in to 1. The Quartus II Compiler automatically places and uses the adder/subtractor feature when using adder/subtractor parameterized functions.

## LE Operating Modes

The Stratix LE can operate in one of the following modes:

- Normal mode
- Dynamic arithmetic mode

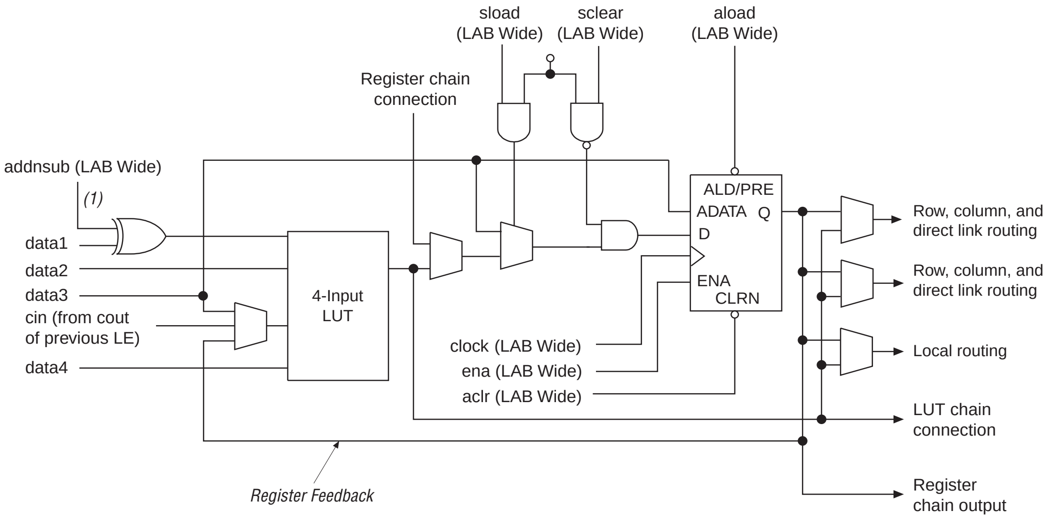
Each mode uses LE resources differently. In each mode, eight available inputs to the LE—the four data inputs from the LAB local interconnect; `carry-in0` and `carry-in1` from the previous LE; the LAB carry-in from the previous carry-chain LAB; and the register chain connection—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes. The `addnsub` control signal is allowed in arithmetic mode.

The Quartus II software, in conjunction with parameterized functions such as library of parameterized modules (LPM) functions, automatically chooses the appropriate mode for common functions such as counters, adders, subtractors, and arithmetic functions. If required, the designer can also create special-purpose functions that specify which LE operating mode to use for optimal performance.

### *Normal Mode*

The normal mode is suitable for general logic applications and combinatorial functions. In normal mode, four data inputs from the LAB local interconnect are inputs to a four-input LUT (see Figure 2–6). The Quartus II Compiler automatically selects the carry-in or the `data3` signal as one of the inputs to the LUT. Each LE can use LUT chain connections to drive its combinatorial output directly to the next LE in the LAB. Asynchronous load data for the register comes from the `data3` input of the LE. LEs in normal mode support packed registers.

***Figure 2–6. LE in Normal Mode***



*Note to Figure 2–6:*

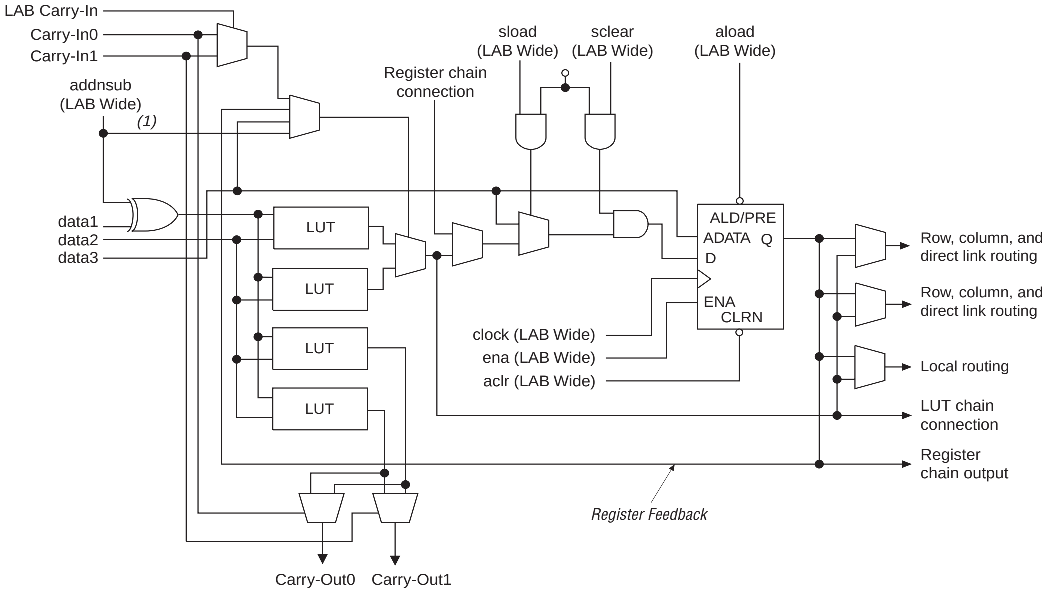
(1) This signal is only allowed in normal mode if the LE is at the end of an adder/subtractor chain.

### *Dynamic Arithmetic Mode*

The dynamic arithmetic mode is ideal for implementing adders, counters, accumulators, wide parity functions, and comparators. An LE in dynamic arithmetic mode uses four 2-input LUTs configurable as a dynamic adder/subtractor. The first two 2-input LUTs compute two summations based on a possible carry-in of 1 or 0; the other two LUTs generate carry outputs for the two chains of the carry select circuitry. As shown in Figure 2–7, the LAB carry-in signal selects either the `carry-in0` or `carry-in1` chain. The selected chain's logic level in turn determines which parallel sum is generated as a combinatorial or registered output. For example, when implementing an adder, the sum output is the selection of two possible calculated sums: `data1` + `data2` + `carry-in0` or `data1` + `data2` + `carry-in1`. The other two LUTs use the `data1` and `data2` signals to generate two possible carry-out signals—one for a carry of 1 and the other for a carry of 0. The `carry-in0` signal acts as the carry select for the `carry-out0` output and `carry-in1` acts as the carry select for the `carry-out1` output. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The dynamic arithmetic mode also offers clock enable, counter enable, synchronous up/down control, synchronous clear, synchronous load, and dynamic adder/subtractor options. The LAB local interconnect data inputs generate the counter enable and synchronous up/down control signals. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. The Quartus II software automatically places any registers that are not used by the counter into other LABs. The `addnsub` LAB-wide signal controls whether the LE acts as an adder or subtractor.

*Figure 2–7. LE in Dynamic Arithmetic Mode*



*Note to Figure 2–7:*

(1) The `addnsub` signal is tied to the carry input for the first LE of a carry chain only.

### *Carry-Select Chain*

The carry-select chain provides a very fast carry-select function between LEs in arithmetic mode. The carry-select chain uses the redundant carry calculation to increase the speed of carry functions. The LE is configured to calculate outputs for a possible carry-in of 1 and carry-in of 0 in parallel. The `carry-in0` and `carry-in1` signals from a lower-order bit feed forward into the higher-order bit via the parallel carry chain and feed into both the LUT and the next portion of the carry chain. Carry-select chains can begin in any LE within an LAB.

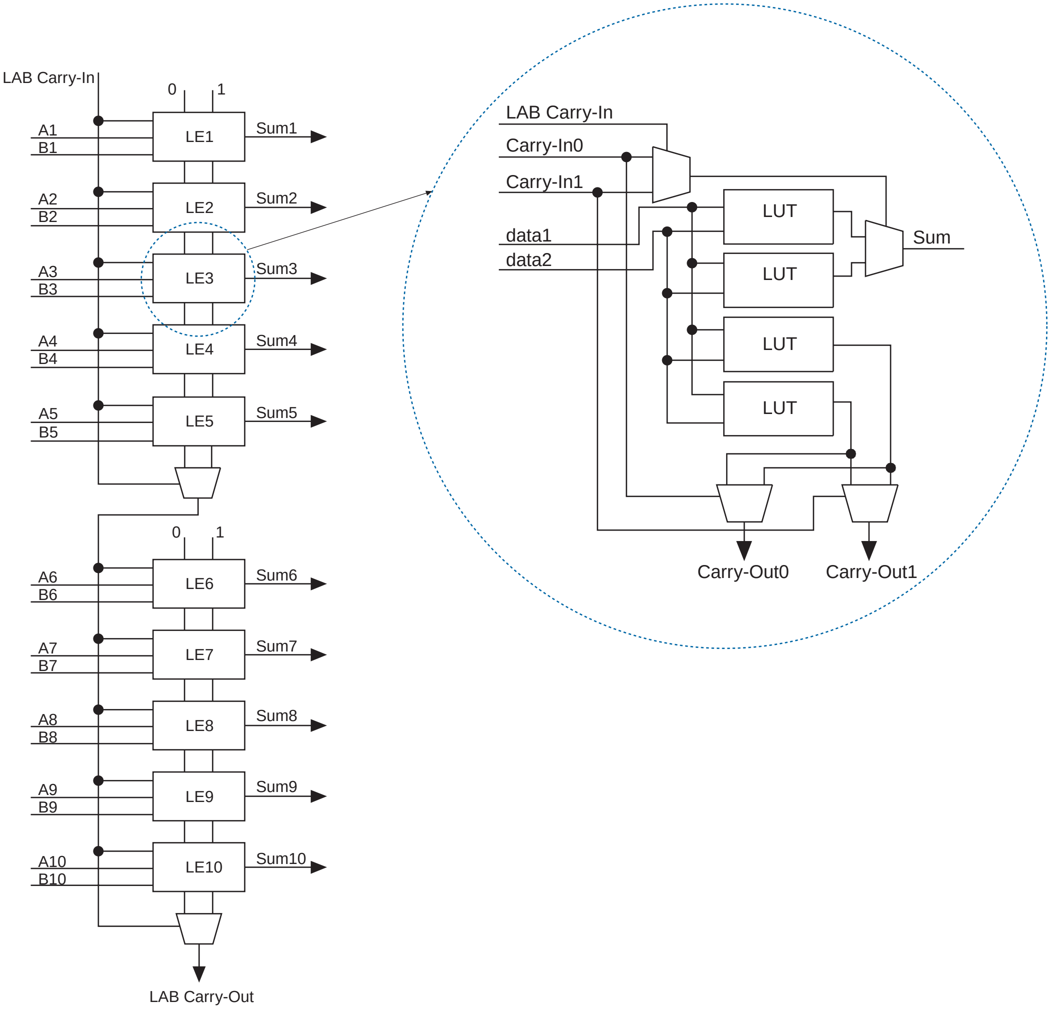
The speed advantage of the carry-select chain is in the parallel pre-computation of carry chains. Since the LAB carry-in selects the precomputed carry chain, not every LE is in the critical path. Only the propagation delay between LAB carry-in generation (LE 5 and LE 10) are now part of the critical path. This feature allows the Stratix architecture to implement high-speed counters, adders, multipliers, parity functions, and comparators of arbitrary width.

Figure 2–8 shows the carry-select circuitry in an LAB for a 10-bit full adder. One portion of the LUT generates the sum of two bits using the input signals and the appropriate carry-in bit; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT generates carry-out bits. An LAB-wide carry in bit selects which chain is used for the addition of given inputs. The carry-in signal for each chain, `carry-in0` or `carry-in1`, selects the carry-out to carry forward to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is fed to local, row, or column interconnects.

The Quartus II Compiler automatically creates carry chain logic during design processing, or the designer can create it manually during design entry. Parameterized functions such as LPM functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II Compiler creates carry chains longer than 10 LEs by linking LABs together automatically. For enhanced fitting, a long carry chain runs vertically allowing fast horizontal connections to TriMatrix memory and DSP blocks. A carry chain can continue as far as a full column.

*Figure 2–8. Carry Select Chain*



## Clear & Preset Logic Control

LAB-wide signals control the logic for the register′s clear and preset signals. The LE directly supports an asynchronous clear and preset function. The register preset is achieved through the asynchronous load of a logic high. The direct asynchronous preset does not require a NOT-gate push-back technique. Stratix devices support simultaneous preset/

asynchronous load, and clear signals. An asynchronous clear signal takes precedence if both signals are asserted simultaneously. Each LAB supports up to two clears and one preset signal.

In addition to the clear and preset ports, Stratix devices provide a chip-wide reset pin (`DEV_CLRn`) that resets all registers in the device. An option set before compilation in the Quartus II software controls this pin. This chip-wide reset overrides all other control signals.

## MultiTrack Interconnect

In the Stratix architecture, connections between LEs, TriMatrix memory, DSP blocks, and device I/O pins are provided by the MultiTrack interconnect structure with DirectDrive™ technology. The MultiTrack interconnect consists of continuous, performance-optimized routing lines of different lengths and speeds used for inter- and intra-design block connectivity. The Quartus II Compiler automatically places critical design paths on faster interconnects to improve design performance.

DirectDrive technology is a deterministic routing technology that ensures identical routing resource usage for any function regardless of placement within the device. The MultiTrack interconnect and DirectDrive technology simplify the integration stage of block-based designing by eliminating the re-optimization cycles that typically follow design changes and additions.

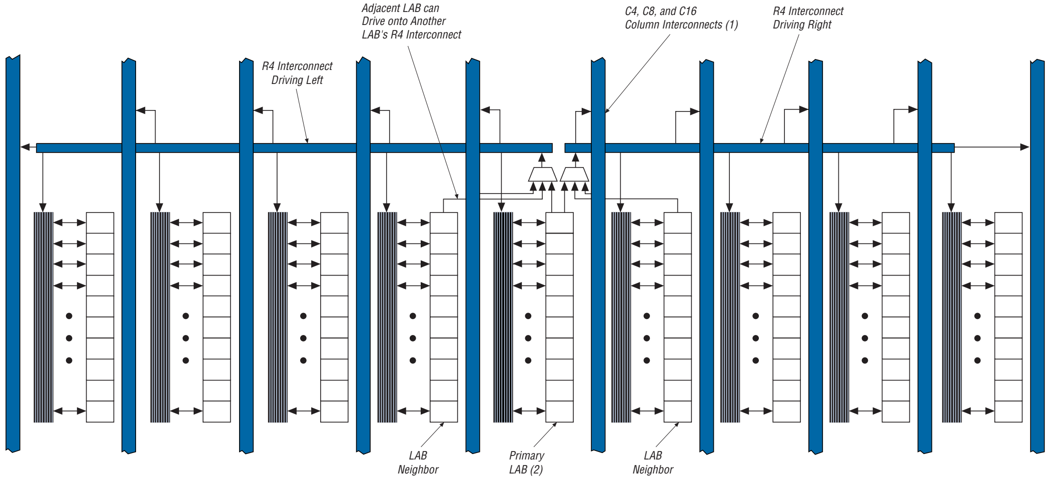
The MultiTrack interconnect consists of row and column interconnects that span fixed distances. A routing structure with fixed length resources for all devices allows predictable and repeatable performance when migrating through different device densities. Dedicated row interconnects route signals to and from LABs, DSP blocks, and TriMatrix memory within the same row. These row resources include:

- Direct link interconnects between LABs and adjacent blocks.
- R4 interconnects traversing four blocks to the right or left.
- R8 interconnects traversing eight blocks to the right or left.
- R24 row interconnects for high-speed access across the length of the device.

The direct link interconnect allows an LAB, DSP block, or TriMatrix memory block to drive into the local interconnect of its left and right neighbors and then back into itself. Only one side of a M-RAM block interfaces with direct link and row interconnects. This provides fast communication between adjacent LABs and/or blocks without using row interconnect resources.

The R4 interconnects span four LABs, three LABs and one M512 RAM block, two LABs and one M4K RAM block, or two LABs and one DSP block to the right or left of a source LAB. These resources are used for fast row connections in a four-LAB region. Every LAB has its own set of R4 interconnects to drive either left or right. Figure 2–9 shows R4 interconnect connections from an LAB. R4 interconnects can drive and be driven by DSP blocks and RAM blocks and horizontal IOEs. For LAB interfacing, a primary LAB or LAB neighbor can drive a given R4 interconnect. For R4 interconnects that drive to the right, the primary LAB and right neighbor can drive on to the interconnect. For R4 interconnects that drive to the left, the primary LAB and its left neighbor can drive on to the interconnect. R4 interconnects can drive other R4 interconnects to extend the range of LABs they can drive. R4 interconnects can also drive C4 and C16 interconnects for connections from one row to another. Additionally, R4 interconnects can drive R24 interconnects.

***Figure 2–9. R4 Interconnect Connections***



*Notes to Figure 2–9:*
(1) C4 interconnects can drive R4 interconnects.
(2) This pattern is repeated for every LAB in the LAB row.

The R8 interconnects span eight LABs, M512 or M4K RAM blocks, or DSP blocks to the right or left from a source LAB. These resources are used for fast row connections in an eight-LAB region. Every LAB has its own set of R8 interconnects to drive either left or right. R8 interconnect connections between LABs in a row are similar to the R4 connections shown in Figure 2–9, with the exception that they connect to eight LABs to the right or left, not four. Like R4 interconnects, R8 interconnects can drive and be driven by all types of architecture blocks. R8 interconnects can drive other R8 interconnects to extend their range as well as C8 interconnects for row-to-row connections. One R8 interconnect is faster than two R4 interconnects connected together.

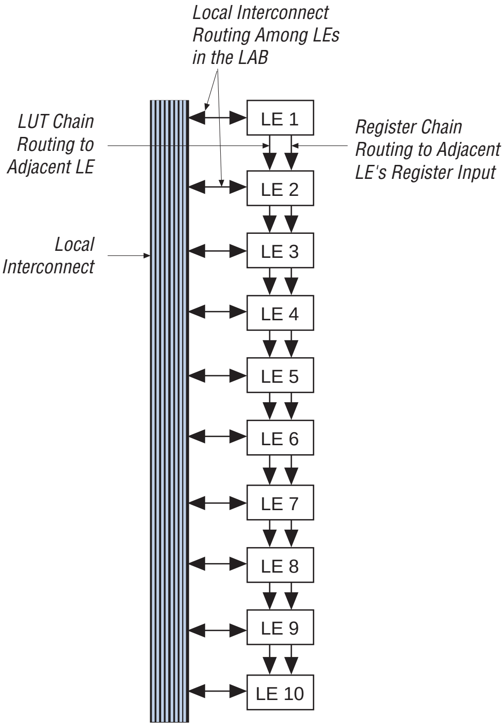
R24 row interconnects span 24 LABs and provide the fastest resource for long row connections between LABs, TriMatrix memory, DSP blocks, and IOEs. The R24 row interconnects can cross M-RAM blocks. R24 row interconnects drive to other row or column interconnects at every fourth LAB and do not drive directly to LAB local interconnects. R24 row interconnects drive LAB local interconnects via R4 and C4 interconnects. R24 interconnects can drive R24, R4, C16, and C4 interconnects.

The column interconnect operates similarly to the row interconnect and vertically routes signals to and from LABs, TriMatrix memory, DSP blocks, and IOEs. Each column of LABs is served by a dedicated column interconnect, which vertically routes signals to and from LABs, TriMatrix memory and DSP blocks, and horizontal IOEs. These column resources include:

- LUT chain interconnects within an LAB
- Register chain interconnects within an LAB
- C4 interconnects traversing a distance of four blocks in up and down direction
- C8 interconnects traversing a distance of eight blocks in up and down direction
- C16 column interconnects for high-speed vertical routing through the device

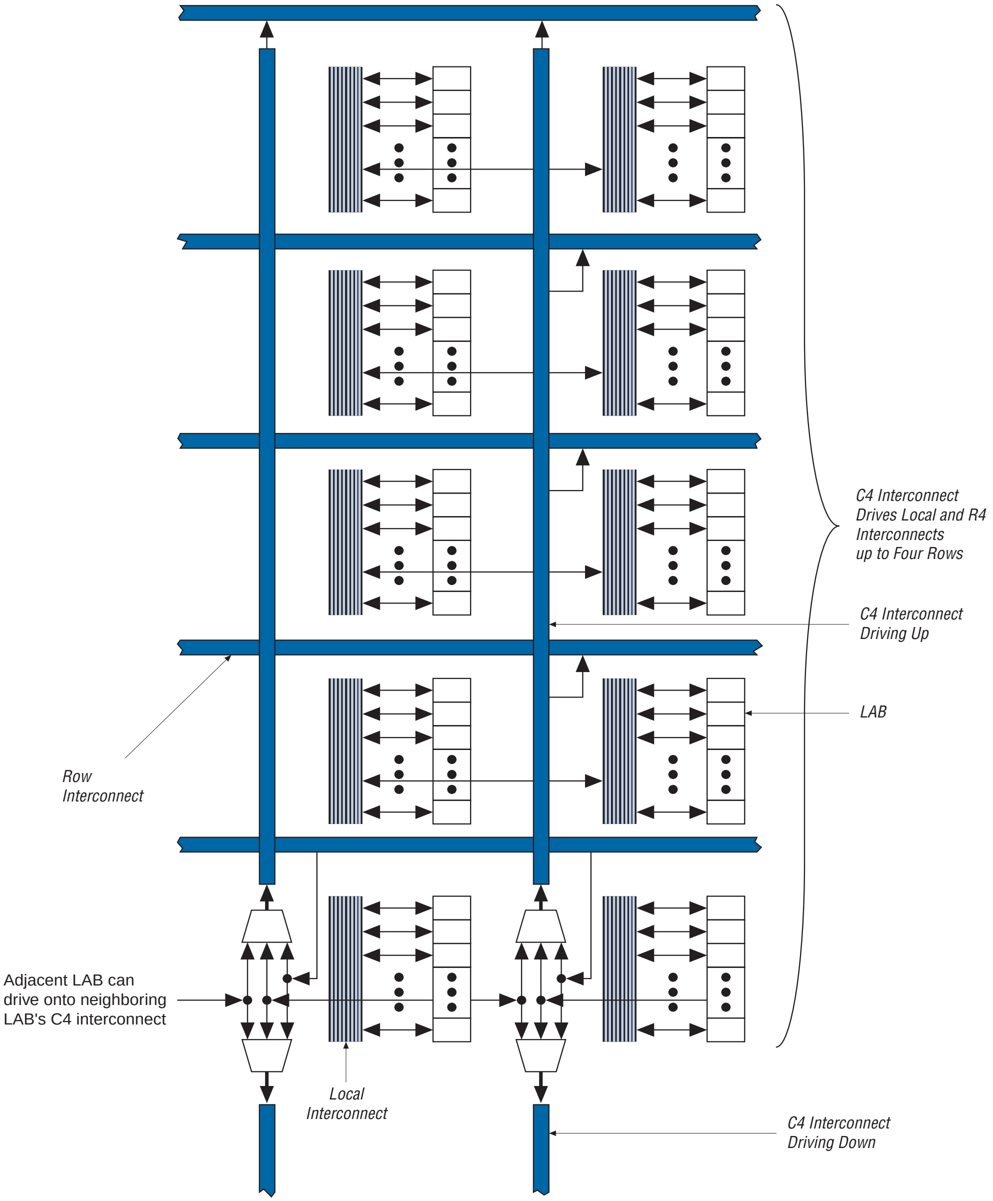
Stratix devices include an enhanced interconnect structure within LABs for routing LE output to LE input connections faster using LUT chain connections and register chain connections. The LUT chain connection allows the combinatorial output of an LE to directly drive the fast input of the LE right below it, bypassing the local interconnect. These resources can be used as a high-speed connection for wide fan-in functions from LE 1 to LE 10 in the same LAB. The register chain connection allows the register output of one LE to connect directly to the register input of the next LE in the LAB for fast shift registers. The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. Figure 2–10 shows the LUT chain and register chain interconnects.

*Figure 2–10. LUT Chain & Register Chain Interconnects*



The C4 interconnects span four LABs, M512, or M4K blocks up or down from a source LAB. Every LAB has its own set of C4 interconnects to drive either up or down. Figure 2–11 shows the C4 interconnect connections from an LAB in a column. The C4 interconnects can drive and be driven by all types of architecture blocks, including DSP blocks, TriMatrix memory blocks, and vertical IOEs. For LAB interconnection, a primary LAB or its LAB neighbor can drive a given C4 interconnect.
C4 interconnects can drive each other to extend their range as well as drive row interconnects for column-to-column connections.

*Figure 2–11. C4 Interconnect Connections* *Note (1)*



*Note to Figure 2–11:*

(1) Each C4 interconnect can drive either up or down four rows.

C8 interconnects span eight LABs, M512, or M4K blocks up or down from a source LAB. Every LAB has its own set of C8 interconnects to drive either up or down. C8 interconnect connections between the LABs in a column are similar to the C4 connections shown in Figure 2–11 with the exception that they connect to eight LABs above and below. The C8 interconnects can drive and be driven by all types of architecture blocks similar to C4 interconnects. C8 interconnects can drive each other to extend their range as well as R8 interconnects for column-to-column connections. C8 interconnects are faster than two C4 interconnects.

C16 column interconnects span a length of 16 LABs and provide the fastest resource for long column connections between LABs, TriMatrix memory blocks, DSP blocks, and IOEs. C16 interconnects can cross M-RAM blocks and also drive to row and column interconnects at every fourth LAB. C16 interconnects drive LAB local interconnects via C4 and R4 interconnects and do not drive LAB local interconnects directly.

All embedded blocks communicate with the logic array similar to LAB-to-LAB interfaces. Each block (i.e., TriMatrix memory and DSP blocks) connects to row and column interconnects and has local interconnect regions driven by row and column interconnects. These blocks also have direct link interconnects for fast connections to and from a neighboring LAB. All blocks are fed by the row LAB clocks, `labclk[7..0]`.

Table 2–2 shows the Stratix device's routing scheme.

*Table 2–2. Stratix Device Routing Scheme*

| Source | Destination | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | LUT Chain | Register Chain | Local Interconnect | Direct Link Interconnect | R4 Interconnect | R8 Interconnect | R24 Interconnect | C4 Interconnect | C8 Interconnect | C16 Interconnect | LE | M512 RAM Block | M4K RAM Block | M-RAM Block | DSP Blocks | Column IOE | Row IOE |
| LUT Chain | | | | | | | | | | | ✓ | | | | | | |
| Register Chain | | | | | | | | | | | ✓ | | | | | | |
| Local Interconnect | | | | | | | | | | | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Direct Link Interconnect | | | ✓ | | | | | | | | | | | | | | |
| R4 Interconnect | | | ✓ | | ✓ | | ✓ | ✓ | | ✓ | | | | | | | |
| R8 Interconnect | | | ✓ | | | ✓ | | | ✓ | | | | | | | | |
| R24 Interconnect | | | | | ✓ | | ✓ | ✓ | | ✓ | | | | | | | |
| C4 Interconnect | | | ✓ | | ✓ | | | ✓ | | | | | | | | | |
| C8 Interconnect | | | ✓ | | | ✓ | | | ✓ | | | | | | | | |
| C16 Interconnect | | | | | ✓ | | ✓ | ✓ | | ✓ | | | | | | | |
| LE | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | ✓ | ✓ | | | | | | | | |
| M512 RAM Block | | | ✓ | ✓ | ✓ | ✓ | | ✓ | ✓ | | | | | | | | |
| M4K RAM Block | | | ✓ | ✓ | ✓ | ✓ | | ✓ | ✓ | | | | | | | | |
| M-RAM Block | | | | | | | | ✓ | ✓ | | | | | | | | |
| DSP Blocks | | | ✓ | ✓ | ✓ | ✓ | | ✓ | ✓ | | | | | | | | |
| Column IOE | | | | ✓ | | | | ✓ | ✓ | ✓ | | | | | | | |
| Row IOE | | | | ✓ | | ✓ | ✓ | ✓ | ✓ | ✓ | | | | | | | |

## TriMatrix Memory

TriMatrix memory consists of three types of RAM blocks: M512, M4K, and M-RAM blocks. Although these memory blocks are different, they can all implement various types of memory with or without parity, including true dual-port, simple dual-port, and single-port RAM, ROM, and FIFO buffers. Table 2–3 shows the size and features of the different RAM blocks.

*Table 2–3. TriMatrix Memory Features (Part 1 of 2)*

| Memory Feature | M512 RAM Block (32 × 18 Bits) | M4K RAM Block (128 × 36 Bits) | M-RAM Block (4K × 144 Bits) |
|---|---|---|---|
| Maximum performance | *(1)* | *(1)* | *(1)* |
| True dual-port memory | | ✓ | ✓ |
| Simple dual-port memory | ✓ | ✓ | ✓ |
| Single-port memory | ✓ | ✓ | ✓ |
| Shift register | ✓ | ✓ | |
| ROM | ✓ | ✓ | *(2)* |
| FIFO buffer | ✓ | ✓ | ✓ |
| Byte enable | | ✓ | ✓ |
| Parity bits | ✓ | ✓ | ✓ |
| Mixed clock mode | ✓ | ✓ | ✓ |
| Memory initialization | ✓ | ✓ | |
| Simple dual-port memory mixed width support | ✓ | ✓ | ✓ |
| True dual-port memory mixed width support | | ✓ | ✓ |
| Power-up conditions | Outputs cleared | Outputs cleared | Outputs unknown |
| Register clears | Input and output reigsters | Input and output registers | Output registers |
| Mixed-port read-during-write | Unknown output/old data | Unknown output/old data | Unknown output |

*Table 2–3. TriMatrix Memory Features (Part 2 of 2)*

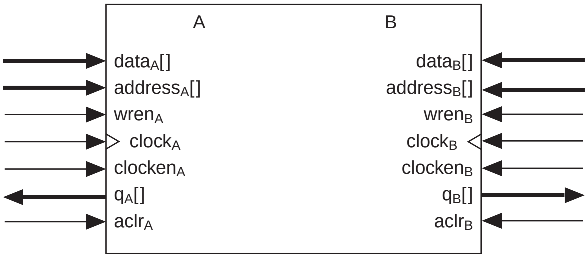
| Memory Feature | M512 RAM Block (32 × 18 Bits) | M4K RAM Block (128 × 36 Bits) | M-RAM Block (4K × 144 Bits) |
|---|---|---|---|
| Configurations | 512 × 1<br>256 × 2<br>128 × 4<br>64 × 8<br>64 × 9<br>32 × 16<br>32 × 18 | 4K × 1<br>2K × 2<br>1K × 4<br>512 × 8<br>512 × 9<br>256 × 16<br>256 × 18<br>128 × 32<br>128 × 36 | 64K × 8<br>64K × 9<br>32K × 16<br>32K × 18<br>16K × 32<br>16K × 36<br>8K × 64<br>8K × 72<br>4K × 128<br>4K × 144 |

*Notes to Table 2–3:*
(1) See Table 4–35 for maximum performance information.
(2) The M-RAM block does not support memory initializations. However, the M-RAM block can emulate a ROM function using a dual-port RAM bock. The Stratix device must write to the dual-port memory once and then disable the write-enable ports afterwards.

## Memory Modes

TriMatrix memory blocks include input registers that synchronize writes and output registers to pipeline designs and improve system performance. M4K and M-RAM memory blocks offer a true dual-port mode to support any combination of two-port operations: two reads, two writes, or one read and one write at two different clock frequencies. Figure 2–12 shows true dual-port memory.

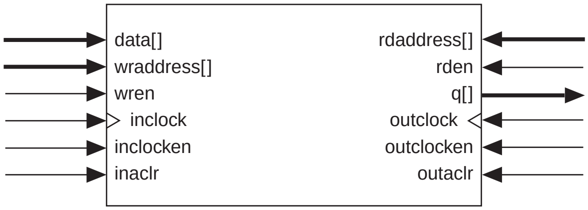
*Figure 2–12. True Dual-Port Memory Configuration*



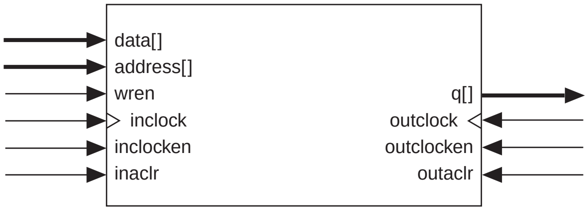
In addition to true dual-port memory, the memory blocks support simple dual-port and single-port RAM. Simple dual-port memory supports a simultaneous read and write and can either read old data before the write occurs or just read the don’t care bits. Single-port memory supports non-simultaneous reads and writes, but the `q[]` port will output the data once it has been written to the memory (if the outputs are not registered) or after the next rising edge of the clock (if the outputs are registered). For more information, see Chapter 3, Using TriMatrix Embedded Memory Blocks in Stratix & Stratix GX Devices of the *Stratix Device Handbook, Volume 2*. Figure 2–13 shows these different RAM memory port configurations for TriMatrix memory.

***Figure 2–13. Simple Dual-Port & Single-Port Memory Configurations***

**Simple Dual-Port Memory**



**Single-Port Memory** *(1)*



***Note to Figure 2–13:***

(1) Two single-port memory blocks can be implemented in a single M4K block as long as each of the two independent block sizes is equal to or less than half of the M4K block size.

The memory blocks also enable mixed-width data ports for reading and writing to the RAM ports in dual-port RAM configuration. For example, the memory block can be written in ×1 mode at port A and read out in ×16 mode from port B.

TriMatrix memory architecture can implement fully synchronous RAM by registering both the input and output signals to the RAM block. All TriMatrix memory block inputs are registered providing synchronous write cycles. In synchronous operation, the memory block generates its own self-timed strobe write enable (`WREN`) signal derived from the global or regional clock. In contrast, a circuit using asynchronous RAM must generate the RAM `WREN` signal while ensuring its data and address signals meet setup and hold time specifications relative to the `WREN` signal. The output registers can be bypassed. Pseudo-asynchronous reading is possible in the simple dual-port mode of M512 and M4K RAM blocks by clocking the read enable and read address registers on the negative clock edge and bypassing the output registers.

Two single-port memory blocks can be implemented in a single M4K block as long as each of the two independent block sizes is equal to or less than half of the M4K block size.

The Quartus II software automatically implements larger memory by combining multiple TriMatrix memory blocks. For example, two 256 × 16-bit RAM blocks can be combined to form a 256 × 32-bit RAM block. Memory performance does not degrade for memory blocks using the maximum number of words available in one memory block. Logical memory blocks using less than the maximum number of words use physical blocks in parallel, eliminating any external control logic that would increase delays. To create a larger high-speed memory block, the Quartus II software automatically combines memory blocks with LE control logic.

### Parity Bit Support

The memory blocks support a parity bit for each byte. The parity bit, along with internal LE logic, can implement parity checking for error detection to ensure data integrity. Designers can also use parity-size data words to store user-specified control bits. In the M4K and M-RAM blocks, byte enables are also available for data input masking during write operations.

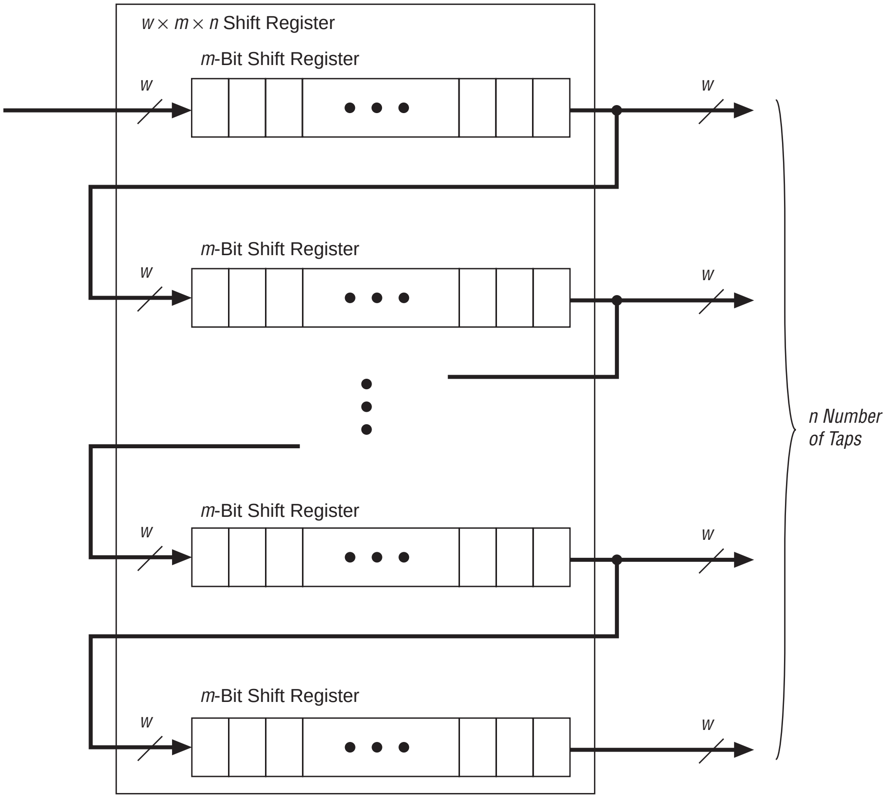
### Shift Register Support

The designer can configure embedded memory blocks to implement shift registers for DSP applications such as pseudo-random number generators, multi-channel filtering, auto-correlation, and cross-correlation functions. These and other DSP applications require local data storage, traditionally implemented with standard flip-flops, which can quickly consume many logic cells and routing resources for large shift registers. A more efficient alternative is to use embedded memory as a shift register block, which saves logic cell and routing resources and provides a more efficient implementation with the dedicated circuitry.

The size of a $w \times m \times n$ shift register is determined by the input data width ($w$), the length of the taps ($m$), and the number of taps ($n$). The size of a $w \times m \times n$ shift register must be less than or equal to the maximum number of memory bits in the respective block: 576 bits for the M512 RAM block and 4,608 bits for the M4K RAM block. The total number of shift register outputs (number of taps $n \times$ width $w$) must be less than the maximum data width of the RAM block (18 for M512 blocks, 36 for M4K blocks). To create larger shift registers, the memory blocks are cascaded together.

Data is written into each address location at the falling edge of the clock and read from the address at the rising edge of the clock. The shift register mode logic automatically controls the positive and negative edge clocking to shift the data in one clock cycle. Figure 2–14 shows the TriMatrix memory block in the shift register mode.

*Figure 2–14. Shift Register Memory Configuration*



## Memory Block Size

TriMatrix memory provides three different memory sizes for efficient application support. The large number of M512 blocks are ideal for designs with many shallow first-in first-out (FIFO) buffers. M4K blocks provide additional resources for channelized functions that do not require large amounts of storage. The M-RAM blocks provide a large single block of RAM ideal for data packet storage. The different-sized blocks allow Stratix devices to efficiently support variable-sized memory in designs.

The Quartus II software automatically partitions the user-defined memory into the embedded memory blocks using the most efficient size combinations. The designer can also manually assign the memory to a specific block size or a mixture of block sizes.

### M512 RAM Block

The M512 RAM block is a simple dual-port memory block and is useful for implementing small FIFO buffers, DSP, and clock domain transfer applications. Each block contains 576 RAM bits (including parity bits). M512 RAM blocks can be configured in the following modes:

- Simple dual-port RAM
- Single-port RAM
- FIFO
- ROM
- Shift register

When configured as RAM or ROM, the designer can use an initialization file to pre-load the memory contents.

The memory address depths and output widths can be configured as 512 × 1, 256 × 2, 128 × 4, 64 × 8 (64 × 9 bits with parity), and 32 × 16 (32 × 18 bits with parity). Mixed-width configurations are also possible, allowing different read and write widths. Table 2–4 summarizes the possible M512 RAM block configurations.

*Table 2–4. M512 RAM Block Configurations (Simple Dual-Port RAM) (Part 1 of 2)*

| Read Port | Write Port | | | | | | |
|---|---|---|---|---|---|---|---|
| | 512 × 1 | 256 × 2 | 128 × 4 | 64 × 8 | 32 × 16 | 64 × 9 | 32 × 18 |
| 512 × 1 | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| 256 × 2 | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| 128 × 4 | ✓ | ✓ | ✓ | | ✓ | | |
| 64 × 8 | ✓ | ✓ | | ✓ | | | |
| 32 × 16 | ✓ | ✓ | ✓ | | ✓ | | |

*Table 2–4. M512 RAM Block Configurations (Simple Dual-Port RAM) (Part 2 of 2)*

| Read Port | Write Port | | | | | | |
|---|---|---|---|---|---|---|---|
| | 512 × 1 | 256 × 2 | 128 × 4 | 64 × 8 | 32 × 16 | 64 × 9 | 32 × 18 |
| 64 × 9 | | | | | | ✓ | |
| 32 × 18 | | | | | | | ✓ |

When the M512 RAM block is configured as a shift register block, a shift register of size up to 576 bits is possible.

The M512 RAM block can also be configured to support serializer and deserializer applications. By using the mixed-width support in combination with DDR I/O standards, the block can function as a SERDES to support low-speed serial I/O standards using global or regional clocks. See "I/O Structure" on page 2–101 for details on dedicated SERDES in Stratix devices.

M512 RAM blocks can have different clocks on its inputs and outputs. The `wren`, `datain`, and write address registers are all clocked together from one of the two clocks feeding the block. The read address, `rden`, and output registers can be clocked by either of the two clocks driving the block. This allows the RAM block to operate in read/write or input/output clock modes. Only the output register can be bypassed. The eight `labclk` signals or local interconnect can drive the `inclock`, `outclock`, `wren`, `rden`, `inclr`, and `outclr` signals. Because of the advanced interconnect between the LAB and M512 RAM blocks, LEs can also control the `wren` and `rden` signals and the RAM clock, clock enable, and asynchronous clear signals. Figure 2–15 shows the M512 RAM block control signal generation logic.

The RAM blocks within Stratix devices have local interconnects to allow LEs and interconnects to drive into RAM blocks. The M512 RAM block local interconnect is driven by the R4, R8, C4, C8, and direct link interconnects from adjacent LABs. The M512 RAM blocks can communicate with LABs on either the left or right side through these row interconnects or with LAB columns on the left or right side with the column interconnects. Up to 10 direct link input connections to the M512 RAM block are possible from the left adjacent LABs and another 10 possible from the right adjacent LAB. M512 RAM outputs can also connect to left and right LABs through 10 direct link interconnects. The M512 RAM block has equal opportunity for access and performance to and from LABs on either its left or right side. Figure 2–16 shows the M512 RAM block to logic array interface.

*Figure 2–15. M512 RAM Block Control Signals*

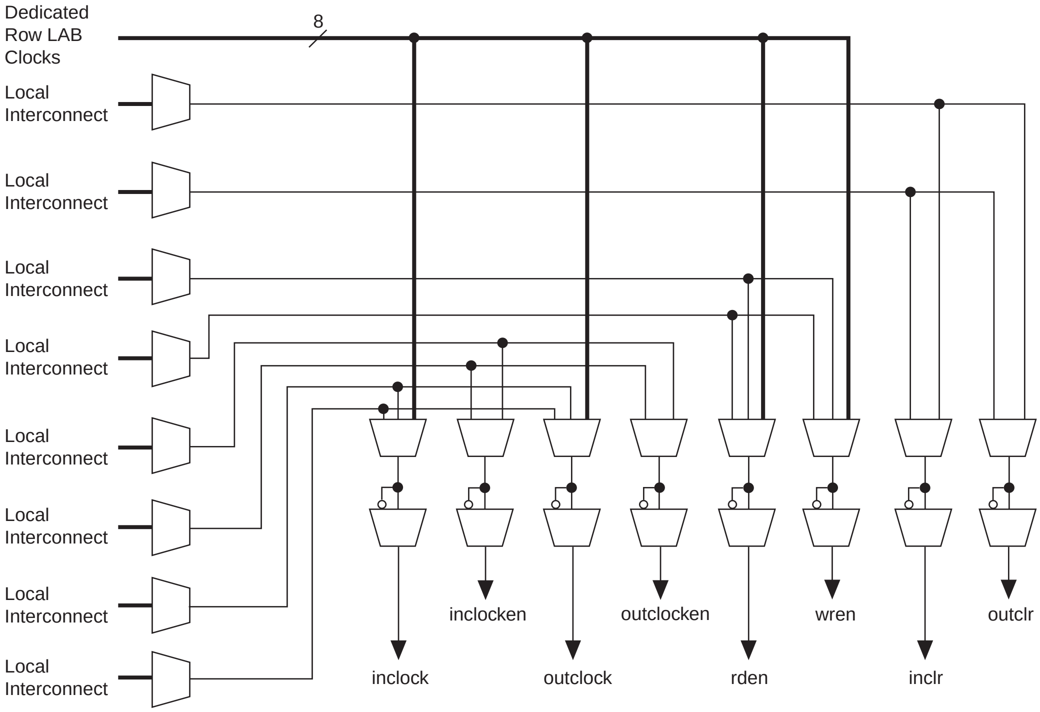
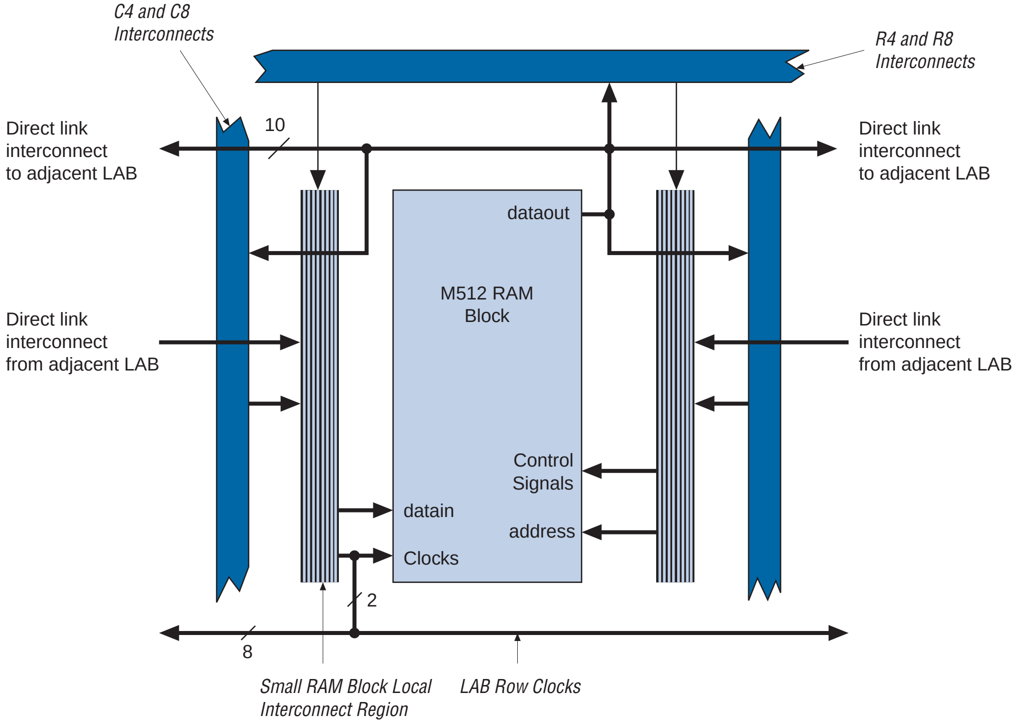


*Figure 2–16. M512 RAM Block LAB Row Interface*



### *M4K RAM Blocks*

The M4K RAM block includes support for true dual-port RAM. The M4K RAM block is used to implement buffers for a wide variety of applications such as storing processor code, implementing lookup schemes, and implementing larger memory applications. Each block contains 4,608 RAM bits (including parity bits). M4K RAM blocks can be configured in the following modes:

- True dual-port RAM
- Simple dual-port RAM
- Single-port RAM
- FIFO
- ROM
- Shift register

When configured as RAM or ROM, the designer can use an initialization file to pre-load the memory contents.

The memory address depths and output widths can be configured as 4,096 × 1, 2,048 × 2, 1,024 × 4, 512 × 8 (or 512 × 9 bits), 256 × 16 (or 256 × 18 bits), and 128 × 32 (or 128 × 36 bits). The 128 × 32- or 36-bit configuration is not available in the true dual-port mode. Mixed-width configurations are also possible, allowing different read and write widths. Tables 2–5 and 2–6 summarize the possible M4K RAM block configurations.

***Table 2–5. M4K RAM Block Configurations (Simple Dual-Port)***

| Read Port | Write Port | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | **4K × 1** | **2K × 2** | **1K × 4** | **512 × 8** | **256 × 16** | **128 × 32** | **512 × 9** | **256 × 18** | **128 × 36** |
| 4K × 1 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| 2K × 2 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| 1K × 4 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| 512 × 8 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| 256 × 16 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| 128 × 32 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| 512 × 9 | | | | | | | ✓ | ✓ | ✓ |
| 256 × 18 | | | | | | | ✓ | ✓ | ✓ |
| 128 × 36 | | | | | | | ✓ | ✓ | ✓ |

***Table 2–6. M4K RAM Block Configurations (True Dual-Port)***

| Port A | Port B | | | | | | |
|---|---|---|---|---|---|---|---|
| | **4K × 1** | **2K × 2** | **1K × 4** | **512 × 8** | **256 × 16** | **512 × 9** | **256 × 18** |
| 4K × 1 | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| 2K × 2 | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| 1K × 4 | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| 512 × 8 | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| 256 × 16 | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| 512 × 9 | | | | | | ✓ | ✓ |
| 256 × 18 | | | | | | ✓ | ✓ |

When the M4K RAM block is configured as a shift register block, the designer can create a shift register up to 4,608 bits ($w \times m \times n$).

M4K RAM blocks support byte writes when the write port has a data width of 16, 18, 32, or 36 bits. The byte enables allow the input data to be masked so the device can write to specific bytes. The unwritten bytes retain the previous written value. Table 2–7 summarizes the byte selection.

*Table 2–7. Byte Enable for M4K Blocks* *Notes (1), (2)*

| byteena[3..0] | datain ×18 | datain ×36 |
|---|---|---|
| [0] = 1 | [8..0] | [8..0] |
| [1] = 1 | [17..9] | [17..9] |
| [2] = 1 | – | [26..18] |
| [3] = 1 | – | [35..27] |

*Notes to Table 2–7:*

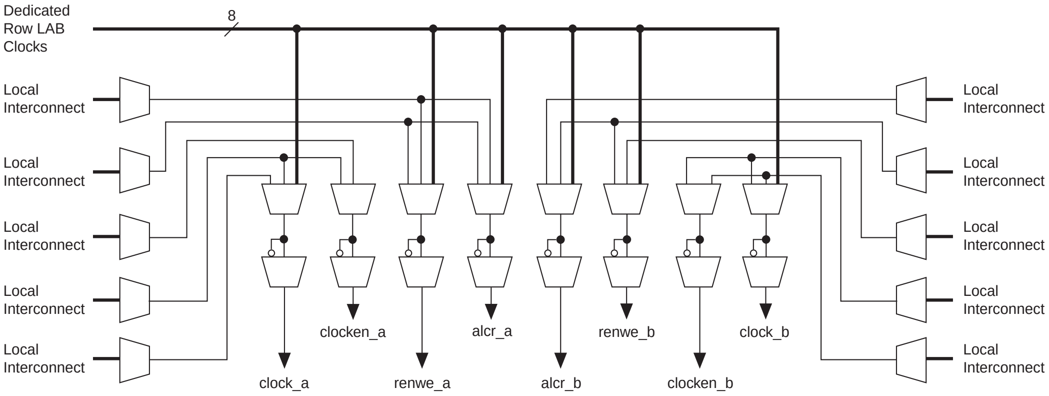
(1) Any combination of byte enables is possible.

(2) Byte enables can be used in the same manner with 8-bit words, i.e., in ×16 and ×32 modes.

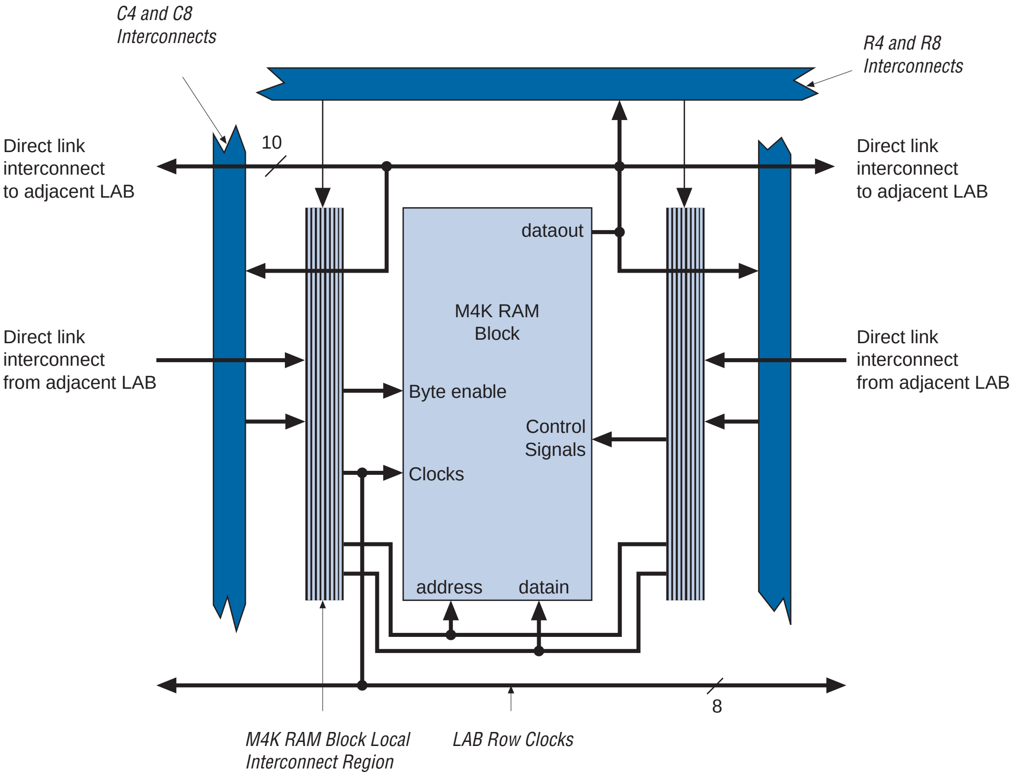
The M4K RAM blocks allow for different clocks on their inputs and outputs. Either of the two clocks feeding the block can clock M4K RAM block registers (`renwe`, address, byte enable, `datain`, and output registers). Only the output register can be bypassed. The eight `labclk` signals or local interconnects can drive the control signals for the A and B ports of the M4K RAM block. LEs can also control the `clock_a`, `clock_b`, `renwe_a`, `renwe_b`, `clr_a`, `clr_b`, `clocken_a`, and `clocken_b` signals, as shown in Figure 2–17.

The R4, R8, C4, C8, and direct link interconnects from adjacent LABs drive the M4K RAM block local interconnect. The M4K RAM blocks can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 10 direct link input connections to the M4K RAM Block are possible from the left adjacent LABs and another 10 possible from the right adjacent LAB. M4K RAM block outputs can also connect to left and right LABs through 10 direct link interconnects each. Figure 2–18 shows the M4K RAM block to logic array interface.

### Figure 2–17. M4K RAM Block Control Signals



### Figure 2–18. M4K RAM Block LAB Row Interface



### *M-RAM Block*

The largest TriMatrix memory block, the M-RAM block, is useful for applications where a large volume of data must be stored on-chip. Each block contains 589,824 RAM bits (including parity bits). The M-RAM block can be configured in the following modes:

- True dual-port RAM
- Simple dual-port RAM
- Single-port RAM
- FIFO

The designer cannot use an initialization file to initialize the contents of a M-RAM block. All M-RAM block contents power up to an undefined value. Only synchronous operation is supported in the M-RAM block, so all inputs are registered. Output registers can be bypassed. The memory address and output width can be configured as 64K × 8 (or 64K × 9 bits), 32K × 16 (or 32K × 18 bits), 16K × 32 (or 16K × 36 bits), 8K × 64 (or 8K × 72 bits), and 4K × 128 (or 4K × 144 bits). The 4K × 128 configuration is unavailable in true dual-port mode because there are a total of 144 data output drivers in the block. Mixed-width configurations are also possible, allowing different read and write widths. Tables 2–8 and 2–9 summarizes the possible M-RAM block configurations:

*Table 2–8. M-RAM Block Configurations (Simple Dual-Port)*

| Read Port | Write Port | | | | |
|---|---|---|---|---|---|
| | 64K × 9 | 32K × 18 | 16K × 36 | 8K × 72 | 4K × 144 |
| 64K × 9 | ✓ | ✓ | ✓ | ✓ | |
| 32K × 18 | ✓ | ✓ | ✓ | ✓ | |
| 16K × 36 | ✓ | ✓ | ✓ | ✓ | |
| 8K × 72 | ✓ | ✓ | ✓ | ✓ | |
| 4K × 144 | | | | | ✓ |

*Table 2–9. M-RAM Block Configurations (True Dual-Port)*

| Port A | Port B | | | |
|---|---|---|---|---|
| | 64K × 9 | 32K × 18 | 16K × 36 | 8K × 72 |
| 64K × 9 | ✓ | ✓ | ✓ | ✓ |
| 32K × 18 | ✓ | ✓ | ✓ | ✓ |
| 16K × 36 | ✓ | ✓ | ✓ | ✓ |
| 8K × 72 | ✓ | ✓ | ✓ | ✓ |

The read and write operation of the memory is controlled by the `WREN` signal, which sets the ports into either read or write modes. There is no separate read enable (`RE`) signal.

Writing into RAM is controlled by both the `WREN` and byte enable (`byteena`) signals for each port. The default value for the `byteena` signal is high, in which case writing is controlled only by the `WREN` signal. The byte enables are available for the ×18, ×36, and ×72 modes. In the ×144 simple dual-port mode, the two sets of `byteena` signals (`byteena_a` and `byteena_b`) are combined to form the necessary 16 byte enables. Table 2–10 and Table 2–11 summarize the byte selection.

*Table 2–10. Byte Enable for M-RAM Blocks* *Notes (1), (2)*

| byteena[3..0] | datain ×18 | datain ×36 | datain ×72 |
|---|---|---|---|
| [0] = 1 | [8..0] | [8..0] | [8..0] |
| [1] = 1 | [17..9] | [17..9] | [17..9] |
| [2] = 1 | – | [26..18] | [26..18] |
| [3] = 1 | – | [35..27] | [35..27] |
| [4] = 1 | – | – | [44..36] |
| [5] = 1 | – | – | [53..45] |
| [6] = 1 | – | – | [62..54] |
| [7] = 1 | – | – | [71..63] |

*Table 2–11. M-RAM Combined Byte Selection for ×144 Mode Notes (1), (2)*

| byteena[15..0] | datain ×144 |
|---|---|
| [0] = 1 | [8..0] |
| [1] = 1 | [17..9] |
| [2] = 1 | [26..18] |
| [3] = 1 | [35..27] |
| [4] = 1 | [44..36] |
| [5] = 1 | [53..45] |
| [6] = 1 | [62..54] |
| [7] = 1 | [71..63] |
| [8] = 1 | [80..72] |
| [9] = 1 | [89..81] |
| [10] = 1 | [98..90] |
| [11] = 1 | [107..99] |
| [12] = 1 | [116..108] |
| [13] = 1 | [125..117] |
| [14] = 1 | [134..126] |
| [15] = 1 | [143..135] |

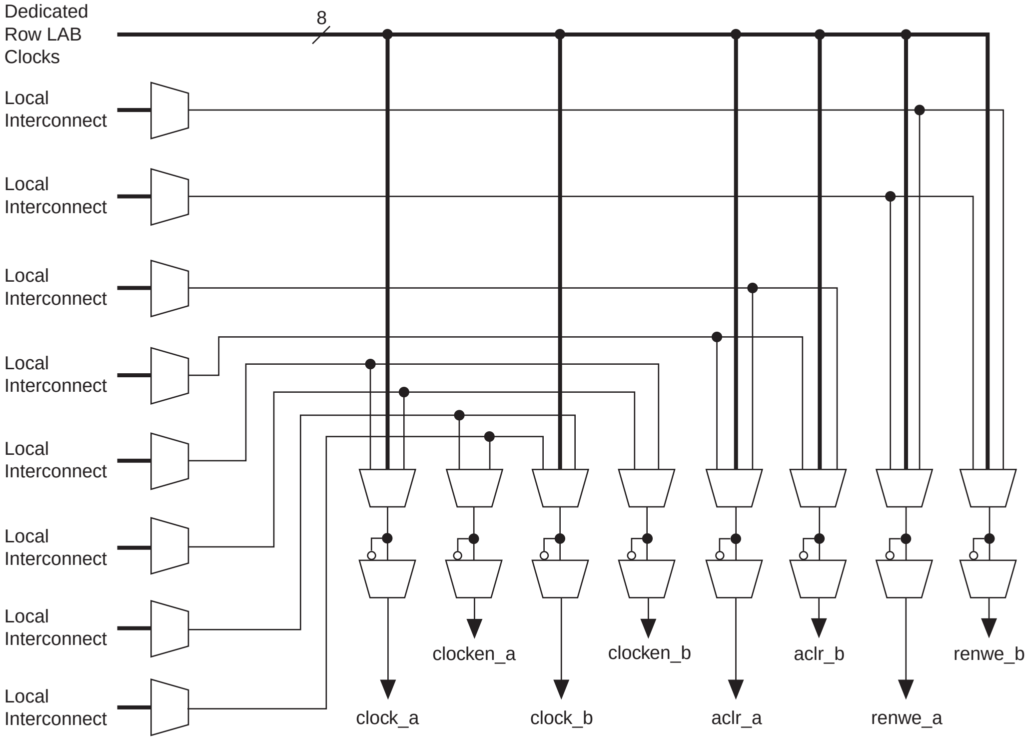
*Notes to Tables 2–10 and 2–11:*

(1) Any combination of byte enables is possible.

(2) Byte enables can be used in the same manner with 8-bit words, i.e., in ×16, ×32, ×64, and ×128 modes.

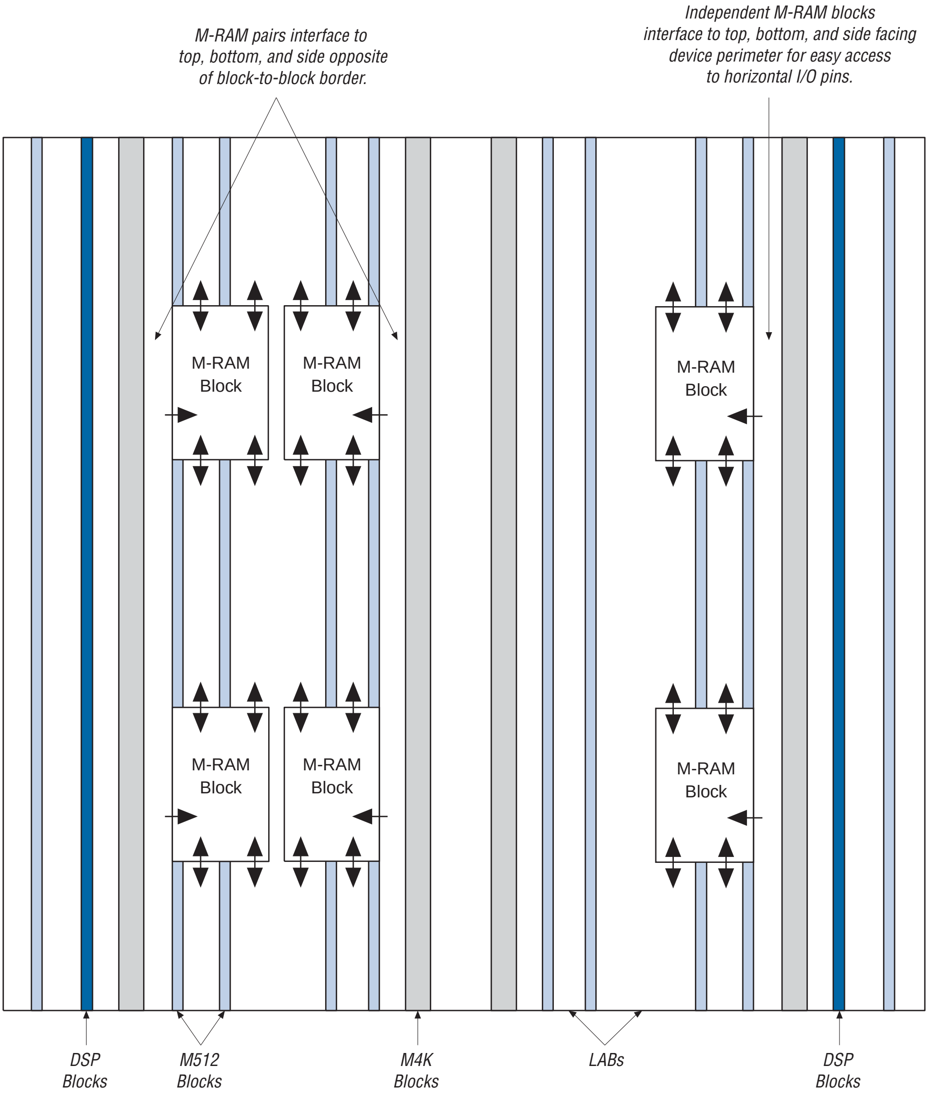
Similar to all RAM blocks, M-RAM blocks can have different clocks on their inputs and outputs. All input registers—`renwe`, `datain`, address, and byte enable registers—are clocked together from either of the two clocks feeding the block. The output register can be bypassed. The eight `labclk` signals or local interconnect can drive the control signals for the A and B ports of the M-RAM block. LEs can also control the `clock_a`, `clock_b`, `renwe_a`, `renwe_b`, `clr_a`, clr_b, `clocken_a`, and `clocken_b` signals as shown in Figure 2–19.

*Figure 2–19. M-RAM Block Control Signals*



One of the M-RAM block's horizontal sides drive the address and control signal (clock, renwe, byteena, etc.) inputs. Typically, the horizontal side closest to the device perimeter contains the interfaces. The one exception is when two M-RAM blocks are paired next to each other. In this case, the side of the M-RAM block opposite the common side of the two blocks contains the input interface. The top and bottom sides of any M-RAM block contain data input and output interfaces to the logic array. The top side has 72 data inputs and 72 data outputs for port B, and the bottom side has another 72 data inputs and 72 data outputs for port A. Figure 2–20 shows an example floorplan for the EP1S60 device and the location of the M-RAM interfaces.

***Figure 2–20. EP1S60 Device with M-RAM Interface Locations*** *Note (1)*

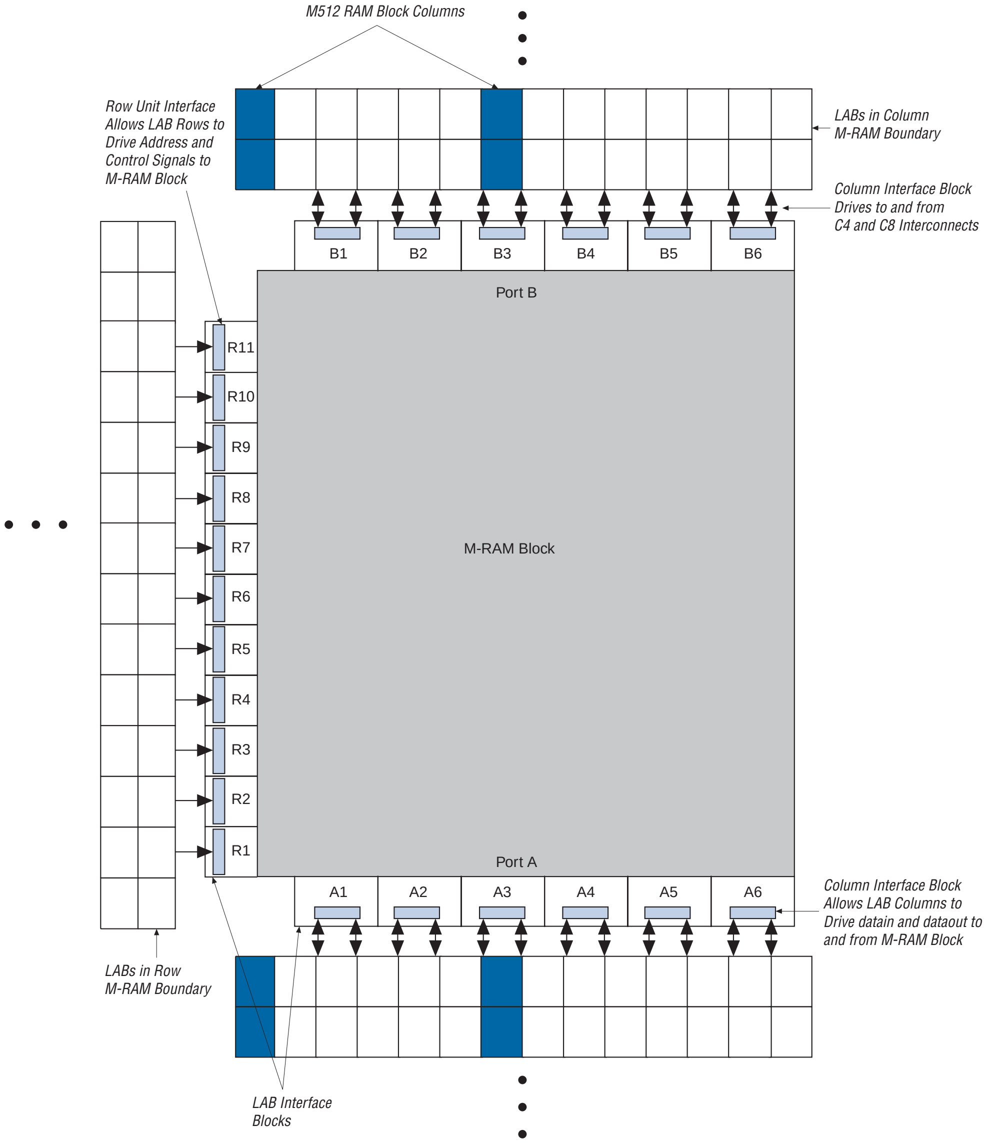


*Note to Figure 2–20:*

(1) Device shown is an EP1S60 device. The number and position of M-RAM blocks varies in other devices.

The M-RAM block local interconnect is driven by the R4, R8, C4, C8, and direct link interconnects from adjacent LABs. For independent M-RAM blocks, up to 10 direct link address and control signal input connections to the M-RAM block are possible from the left adjacent LABs for M-RAM blocks facing to the left, and another 10 possible from the right adjacent LABs for M-RAM blocks facing to the right. For column interfacing, every M-RAM column unit connects to the right and left column lines, allowing each M-RAM column unit to communicate directly with three columns of LABs. Figures 2–21 through 2–23 show the interface between the M-RAM block and the logic array.

**Figure 2–21. Left-Facing M-RAM to Interconnect Interface** *Notes (1), (2)*



*Notes to Figure 2–21:*

(1) Only R24 and C16 interconnects cross the M-RAM block boundaries.

(2) The right-facing M-RAM block has interface blocks on the right side, but none on the left. B1 to B6 and A1 to A6 orientation is clipped across the vertical axis for right-facing M-RAM blocks.

*Figure 2–22. M-RAM Row Unit Interface to Interconnect*

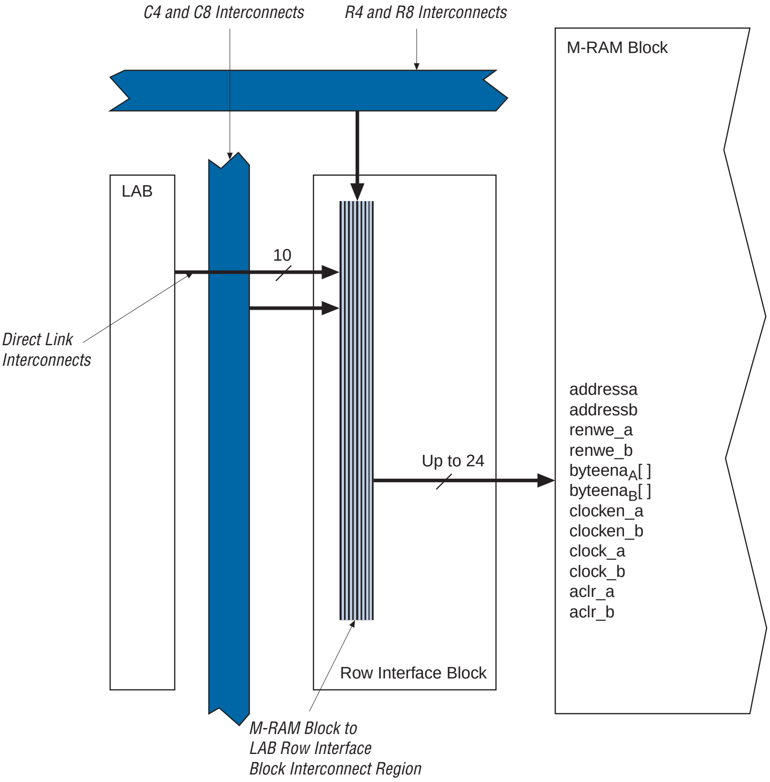


***Figure 2–23. M-RAM Column Unit Interface to Interconnect***

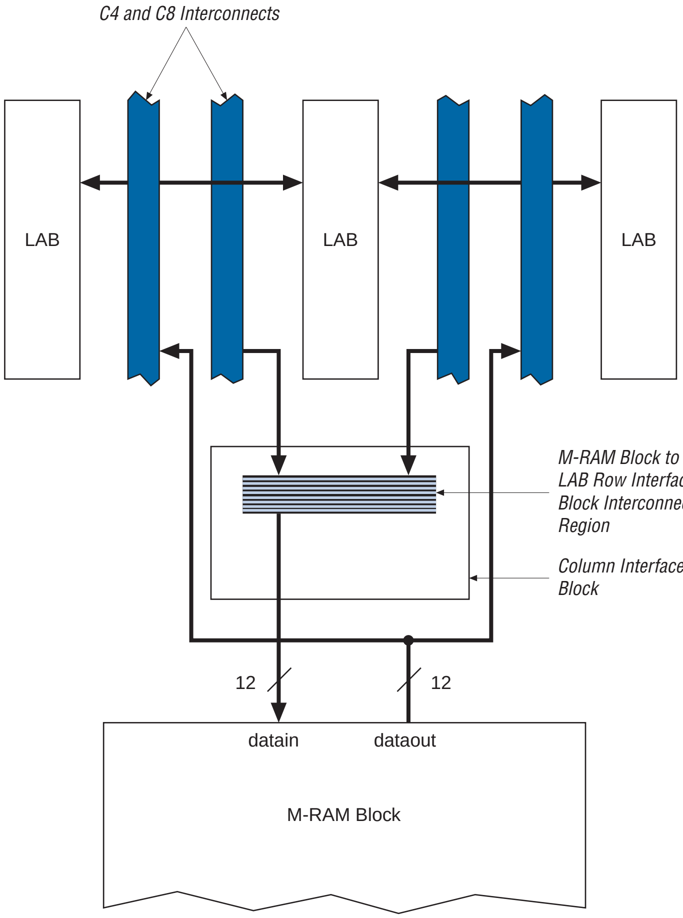


Table 2–12 shows the input and output data signal connections for the column units (B1 to B6 and A1 to A6). It also shows the address and control signal input connections to the row units (R1 to R11).

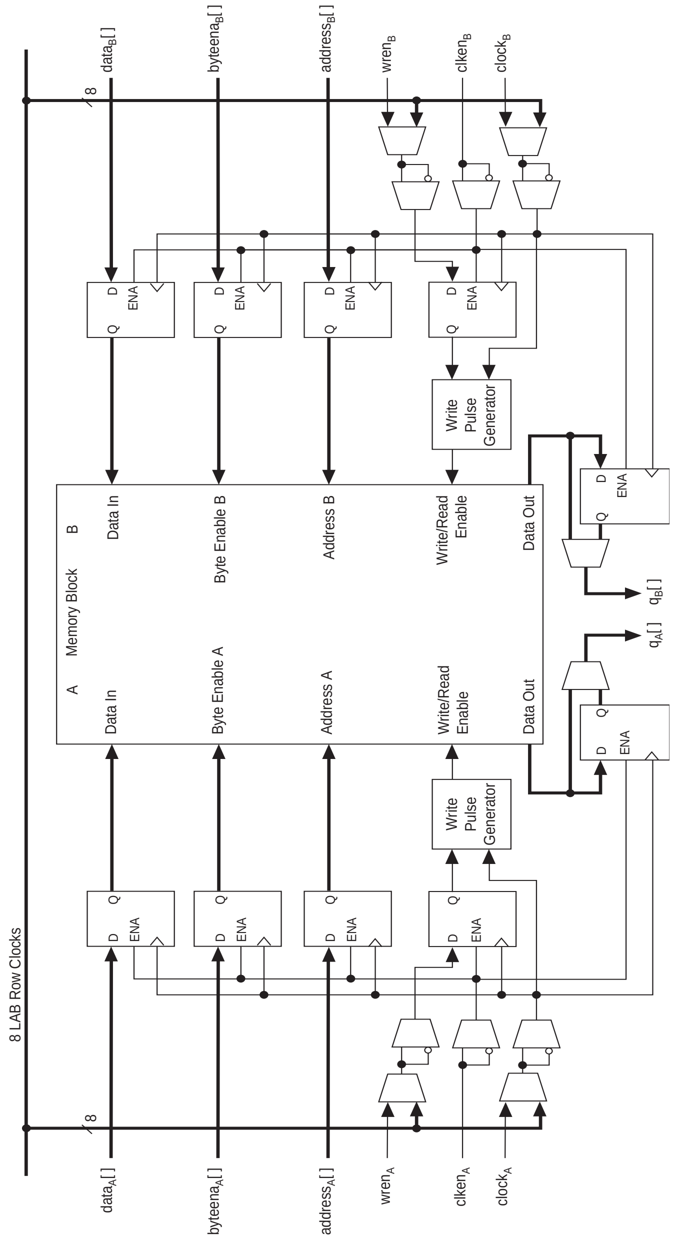
*Table 2–12. M-RAM Row & Column Interface Unit Signals*

| Unit Interface Block | Input SIgnals | Output Signals |
|---|---|---|
| R1 | addressa[7..0] | |
| R2 | addressa[15..8] | |
| R3 | byte_enable_a[7..0]<br>renwe_a | |
| R4 | - | |
| R5 | - | |
| R6 | clock_a<br>clocken_a<br>clock_b<br>clocken_b | |
| R7 | - | |
| R8 | - | |
| R9 | byte_enable_b[7..0]<br>renwe_b | |
| R10 | addressb[15..8] | |
| R11 | addressb[7..0] | |
| B1 | datain_b[71..60] | dataout_b[71..60] |
| B2 | datain_b[59..48] | dataout_b[59..48] |
| B3 | datain_b[47..36] | dataout_b[47..36] |
| B4 | datain_b[35..24] | dataout_b[35..24] |
| B5 | datain_b[23..12] | dataout_b[23..12] |
| B6 | datain_b[11..0] | dataout_b[11..0] |
| A1 | datain_a[71..60] | dataout_a[71..60] |
| A2 | datain_a[59..48] | dataout_a[59..48] |
| A3 | datain_a[47..36] | dataout_a[47..36] |
| A4 | datain_a[35..24] | dataout_a[35..24] |
| A5 | datain_a[23..12] | dataout_a[23..12] |
| A6 | datain_a[11..0] | dataout_a[11..0] |

### Independent Clock Mode

The memory blocks implement independent clock mode for true dual-port memory. In this mode, a separate clock is available for each port (ports A and B). Clock A controls all registers on the port A side, while clock B controls all registers on the port B side. Each port, A and B, also supports independent clock enables and asynchronous clear signals for port A and B registers. Figure 2–24 shows a TriMatrix memory block in independent clock mode.

*Figure 2–24. Independent Clock Mode* Note (1)



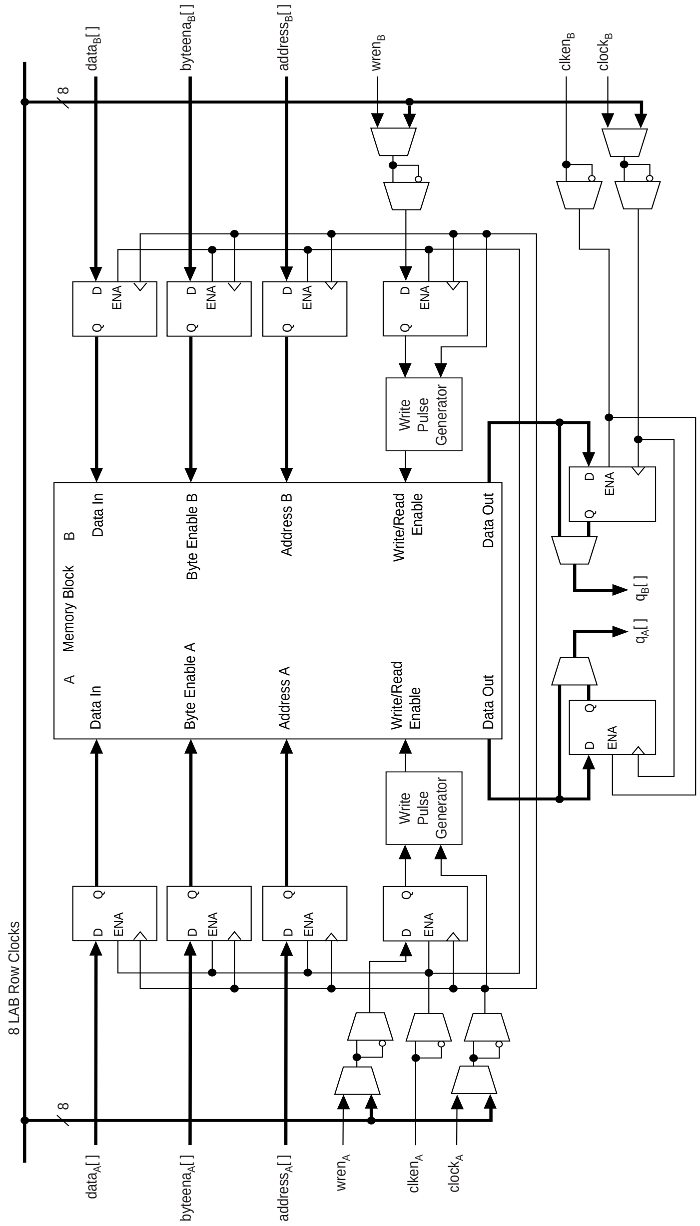
*Note to Figure 2–24:*

(1) All registers shown have asynchronous clear ports.

## Input/Output Clock Mode

Input/output clock mode can be implemented for both the true and simple dual-port memory modes. On each of the two ports, A or B, one clock controls all registers for inputs into the memory block: data input, `wren`, and address. The other clock controls the block's data output registers. Each memory block port, A or B, also supports independent clock enables and asynchronous clear signals for input and output registers. Figures 2–25 and 2–26 show the memory block in input/output clock mode.

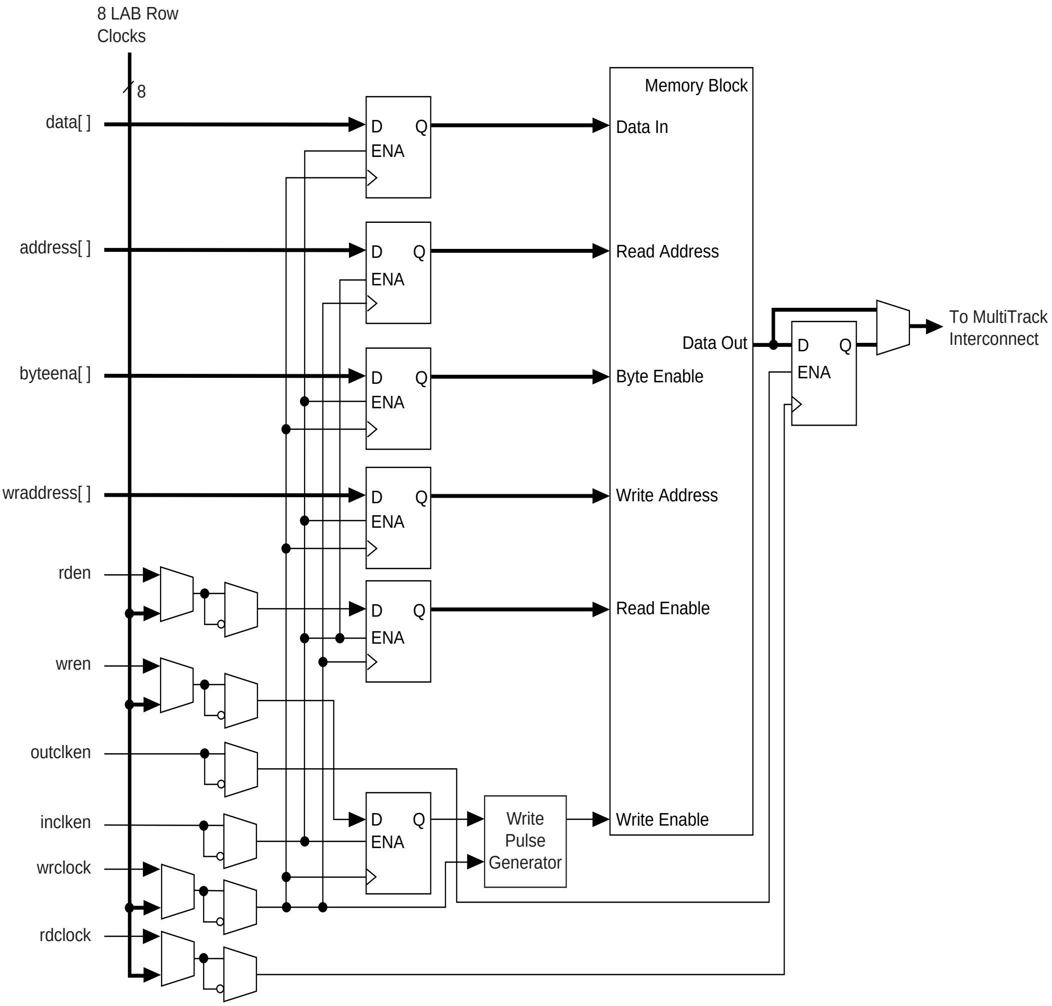
**Figure 2–25. Input/Output Clock Mode in True Dual-Port Mode** Note (1)



*Note to Figure 2–25:*

(1) All registers shown have asynchronous clear ports.

*Figure 2–26. Input/Output Clock Mode in Simple Dual-Port Mode* Note (1)



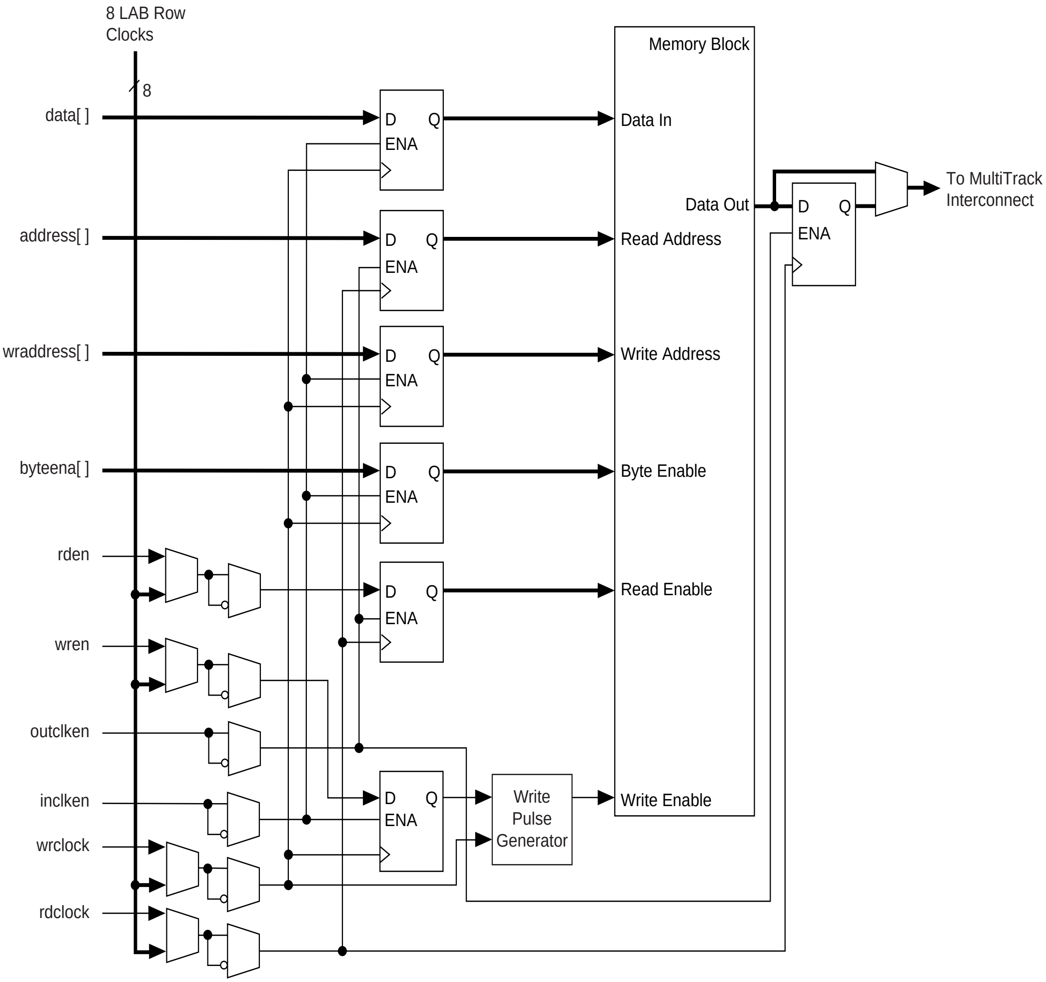
*Note to Figure 2–26:*

(1) All registers shown except the `rden` register have asynchronous clear ports.

## Read/Write Clock Mode

The memory blocks implement read/write clock mode for simple dual-port memory. The designer can use up to two clocks in this mode. The write clock controls the block's data inputs, `wraddress`, and `wren`. The read clock controls the data output, `rdaddress`, and `rden`. The memory blocks support independent clock enables for each clock and asynchronous clear signals for the read- and write-side registers. Figure 2–27 shows a memory block in read/write clock mode.

***Figure 2–27. Read/Write Clock Mode in Simple Dual-Port Mode*** *Note (1)*



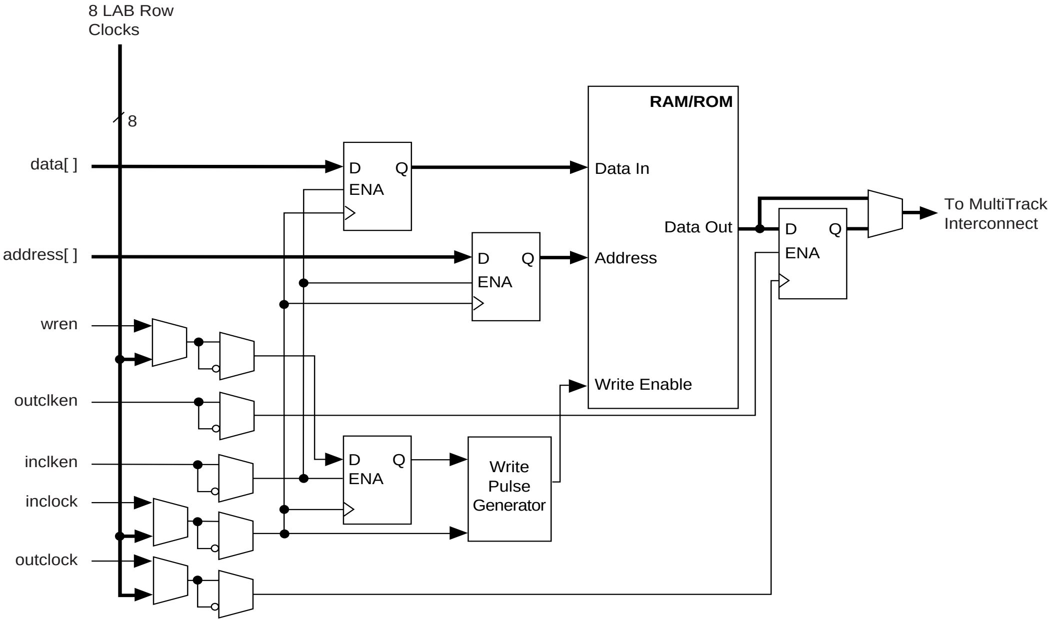
*Note to Figure 2–27:*

(1) All registers shown except the `rden` register have asynchronous clear ports.

### Single-Port Mode

The memory blocks also support single-port mode, used when simultaneous reads and writes are not required. See Figure 2–28. A single block in a memory block can support up to two single-port mode RAM blocks in the M4K RAM blocks if each RAM block is less than or equal to 2K bits in size.

*Figure 2–28. Single-Port Mode*



## Digital Signal Processing Block

The most commonly used DSP functions are finite impulse response (FIR) filters, complex FIR filters, infinite impulse response (IIR) filters, fast Fourier transform (FFT) functions, direct cosine transform (DCT) functions, and correlators. All of these blocks have the same fundamental building block: the multiplier. Additionally, some applications need specialized operations such as multiply-add and multiply-accumulate operations. Stratix devices provide DSP blocks to meet the arithmetic requirements of these functions.

Each Stratix device has two columns of DSP blocks to efficiently implement DSP functions faster than LE-based implementations. Larger Stratix devices have more DSP blocks per column (see Table 2–13). Each DSP block can be configured to support up to:

- Eight 9 × 9-bit multipliers
- Four 18 × 18-bit multipliers
- One 36 × 36-bit multiplier

As indicated, the Stratix DSP block can support one 36 × 36-bit multiplier in a single DSP block. This is true for any matched sign multiplications (either unsigned by unsigned or signed by signed), but the capabilities for dynamic and mixed sign multiplications are handled differently. The following list provides the largest functions that can fit into a single DSP block.

- 36 × 36-bit unsigned by unsigned multiplication
- 36 × 36-bit signed by signed multiplication
- 35 × 36-bit unsigned by signed multiplication
- 36 × 35-bit signed by unsigned multiplication
- 36 × 35-bit signed by dynamic sign multiplication
- 35 × 36-bit dynamic sign by signed multiplication
- 35 × 36-bit unsigned by dynamic sign multiplication
- 36 × 35-bit dynamic sign by unsigned multiplication
- 35 × 35-bit dynamic sign multiplication when the sign controls for each operand are different
- 36 × 36-bit dynamic sign multiplication when the same sign control is used for both operands

☞ This list only shows functions that can fit into a single DSP block. Multiple DSP blocks can support larger multiplication functions.

Figure 2–29 shows one of the columns with surrounding LAB rows.

*Figure 2–29. DSP Blocks Arranged in Columns*

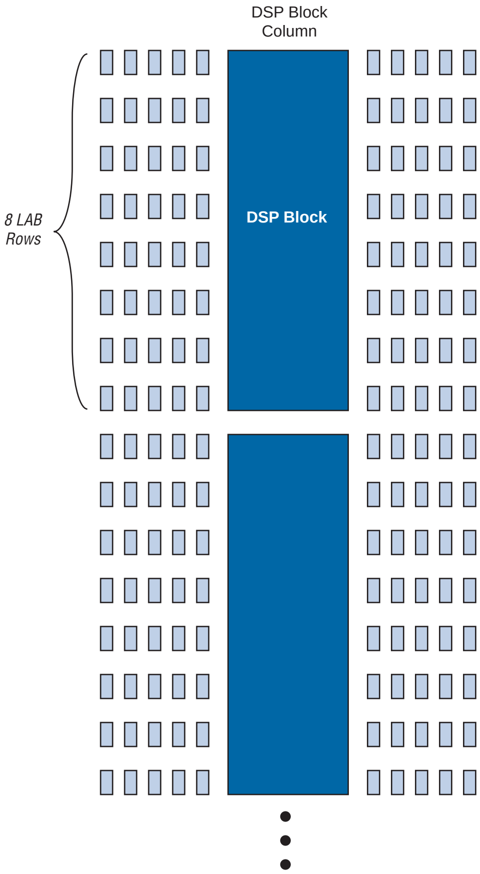


Table 2–13 shows the number of DSP blocks in each Stratix device.

*Table 2–13. DSP Blocks in Stratix Devices* Note (1), (2)

| Device | DSP Blocks | Total 9 × 9 Multipliers | Total 18 × 18 Multipliers | Total 36 × 36 Multipliers |
|---|---|---|---|---|
| EP1S10 | 6 | 48 | 24 | 6 |
| EP1S20 | 10 | 80 | 40 | 10 |
| EP1S25 | 10 | 80 | 40 | 10 |
| EP1S30 | 12 | 96 | 48 | 12 |
| EP1S40 | 14 | 112 | 56 | 14 |
| EP1S60 | 18 | 144 | 72 | 18 |
| EP1S80 | 22 | 176 | 88 | 22 |

*Notes to Table 2–13:*

(1) Each device has either the number of 9 × 9-, 18 × 18-, or 36 × 36-bit multipliers shown. The total number of multipliers for each device is not the sum of all the multipliers.

(2) The number of supported multiply functions shown is based on signed/signed or unsigned/unsigned implementations.

DSP block multipliers can optionally feed an adder/subtractor or accumulator within the block depending on the configuration. This makes routing to LEs easier, saves LE routing resources, and increases performance, because all connections and blocks are within the DSP block. Additionally, the DSP block input registers can efficiently implement shift registers for FIR filter applications.

Figure 2–30 shows the top-level diagram of the DSP block configured for 18 × 18-bit multiplier mode. Figure 2–31 shows the 9 × 9-bit multiplier configuration of the DSP block.

*Figure 2–30. DSP Block Diagram for 18 × 18-Bit Configuration*

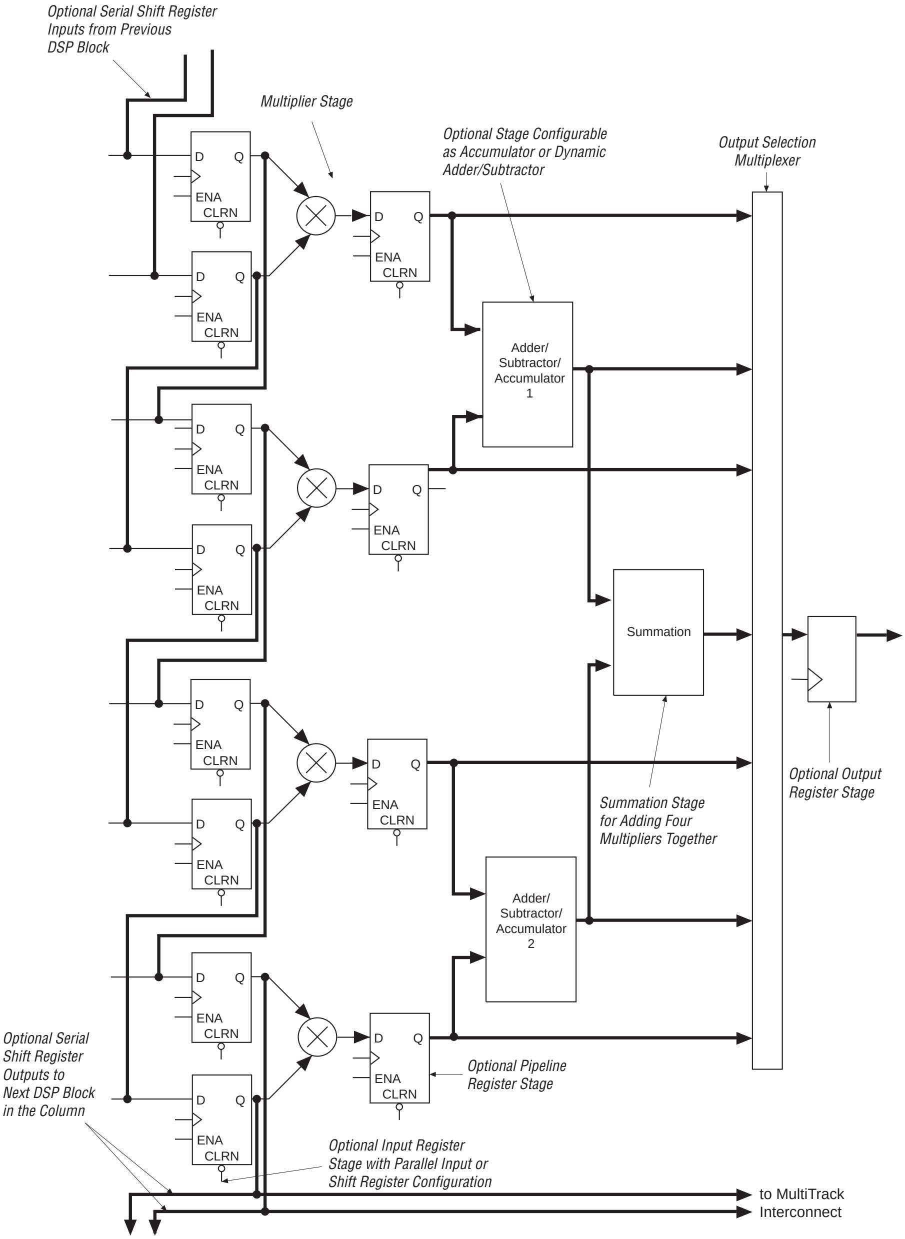
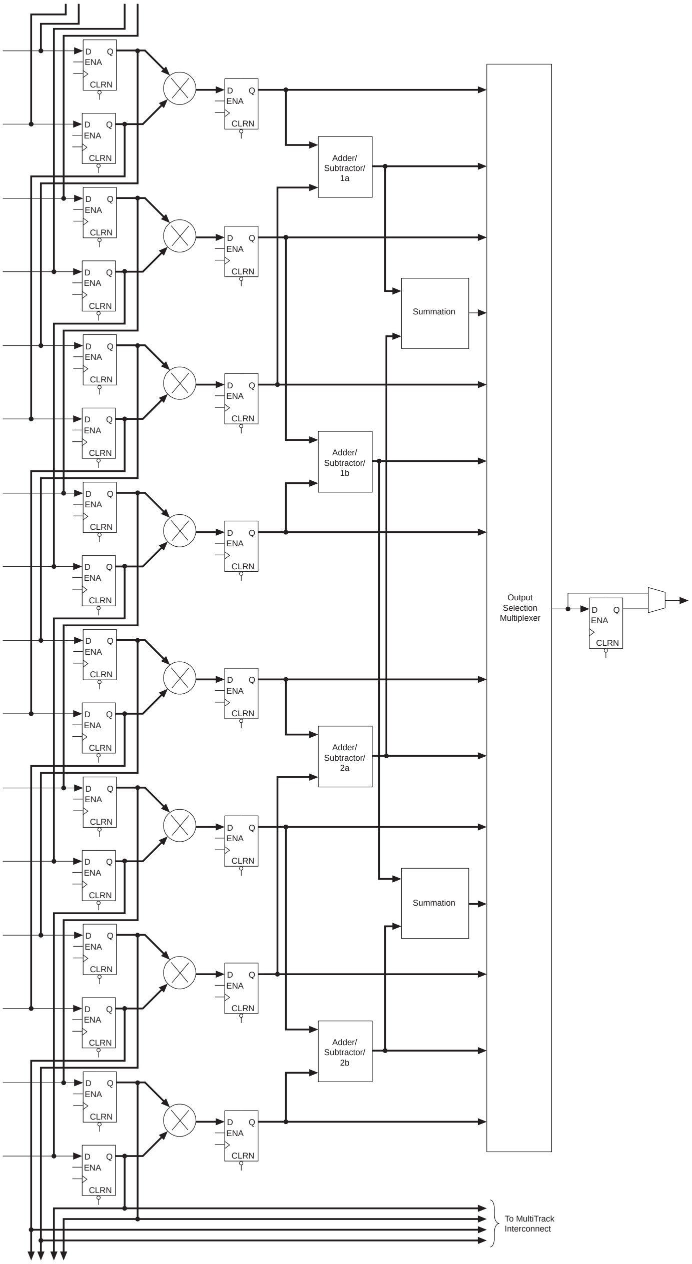


Figure 2–31. DSP Block Diagram for 9 × 9-Bit Configuration



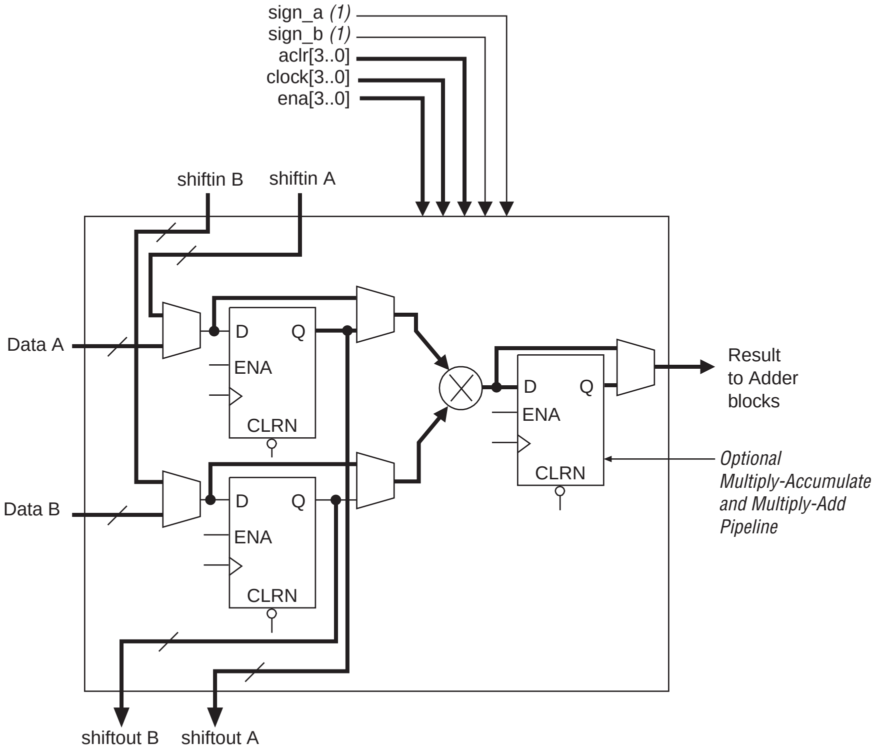
The DSP block consists of the following elements:

- Multiplier block
- Adder/output block

## Multiplier Block

The DSP block multiplier block consists of the input registers, a multiplier, and pipeline register for pipelining multiply-accumulate and multiply-add/subtract functions as shown in Figure 2–32.

*Figure 2–32. Multiplier Sub-Block within Stratix DSP Block*



*Note to Figure 2–32:*

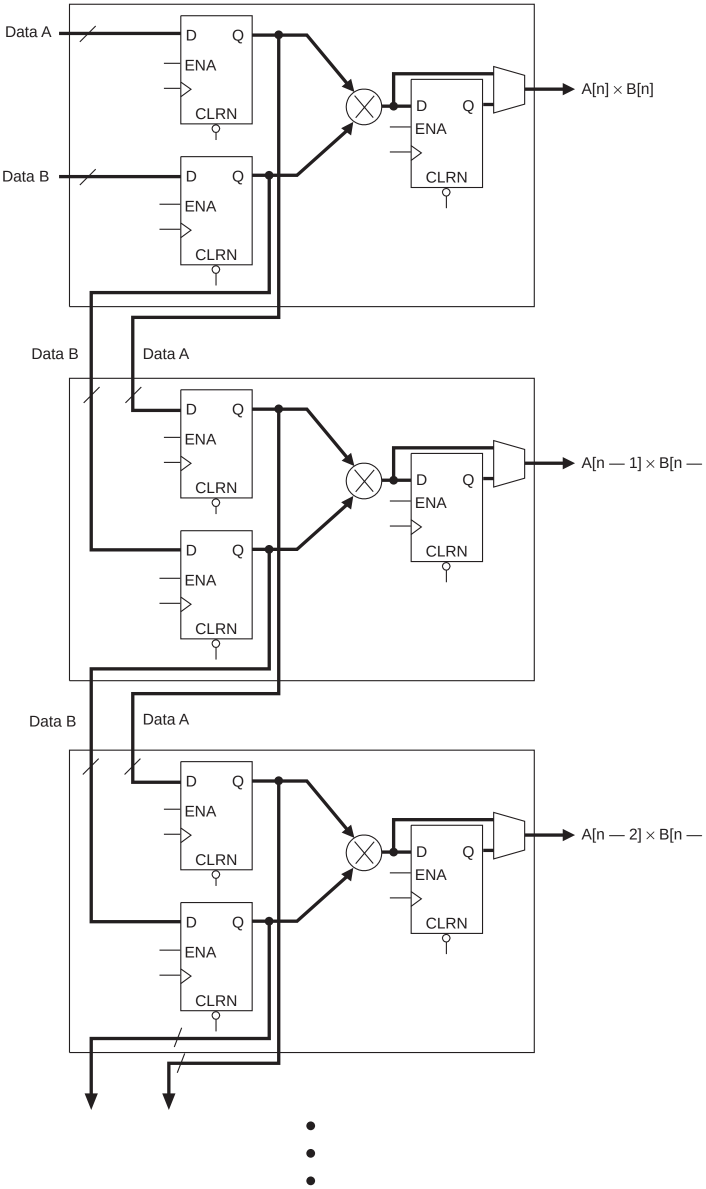
(1) These signals can be unregistered or registered once to match data path pipelines if required.

### *Input Registers*

A bank of optional input registers is located at the input of each multiplier and multiplicand inputs to the multiplier. When these registers are configured for parallel data inputs, they are driven by regular routing resources. Designers can use a clock signal, asynchronous clear signal, and a clock enable signal to independently control each set of A and B inputs for each multiplier in the DSP block. Designers select these control signals from a set of four different `clock[3..0]`, `aclr[3..0]`, and `ena[3..0]` signals that drive the entire DSP block.

Designers can also configure the input registers for a shift register application. In this case, the input registers feed the multiplier and drive two dedicated shift output lines: `shiftoutA` and `shiftoutB`. The shift outputs of one multiplier block directly feed the adjacent multiplier block in the same DSP block (or the next DSP block) as shown in Figure 2–33, to form a shift register chain. This chain can terminate in any block, i.e., designers can create any length of shift register chain up to 224 registers. The designer can use the input shift registers for FIR filter applications. One set of shift inputs can provide data for a filter, and the other are coefficients that are optionally loaded in serial or parallel. When implementing 9 × 9- and 18 × 18-bit multipliers, the designer does not need to implement external shift registers in LAB LEs. The designer implements all the filter circuitry within the DSP block and its routing resources, saving LE and general routing resources for general logic. External registers are needed for shift register inputs when using 36 × 36-bit multipliers.

**Figure 2–33. Multiplier Sub-Blocks Using Input Shift Register Connections** *Note (1)*



*Note to Figure 2–33:*

(1) Either Data A or Data B input can be set to a parallel input for constant coefficient multiplication.

Table 2–14 shows the summary of input register modes for the DSP block.

*Table 2–14. Input Register Modes*

| Register Input Mode | 9 × 9 | 18 × 18 | 36 × 36 |
|---|---|---|---|
| Parallel input | ✓ | ✓ | ✓ |
| Shift register input | ✓ | ✓ | |

### *Multiplier*

The multiplier supports 9 × 9-, 18 × 18-, or 36 × 36-bit multiplication. Each DSP block supports eight possible 9 × 9-bit or smaller multipliers. There are four multiplier blocks available for multipliers larger than 9 × 9 bits but smaller than 18 × 18 bits. There is one multiplier block available for multipliers larger than 18 × 18 bits but smaller than or equal to 36 × 36 bits. The ability to have several small multipliers is useful in applications such as video processing. Large multipliers greater than 18 × 18 bits are useful for applications such as the mantissa multiplication of a single-precision floating-point number.

The multiplier operands can be signed or unsigned numbers, where the result is signed if either input is signed as shown in Table 2–15. The `sign_a` and `sign_b` signals provide dynamic control of each operand's representation: a logic 1 indicates the operand is a signed number, a logic 0 indicates the operand is an unsigned number. These sign signals affect all multipliers and adders within a single DSP block and designers can register them to match the data path pipeline. The multipliers are full precision (i.e., 18 bits for the 18-bit multiply, 36-bits for the 36-bit multiply, etc.) regardless of whether `sign_a` or `sign_b` set the operands as signed or unsigned numbers.

*Table 2–15. Multiplier Signed Representation*

| Data A | Data B | Result |
|---|---|---|
| Unsigned | Unsigned | Unsigned |
| Unsigned | Signed | Signed |
| Signed | Unsigned | Signed |
| Signed | Signed | Signed |

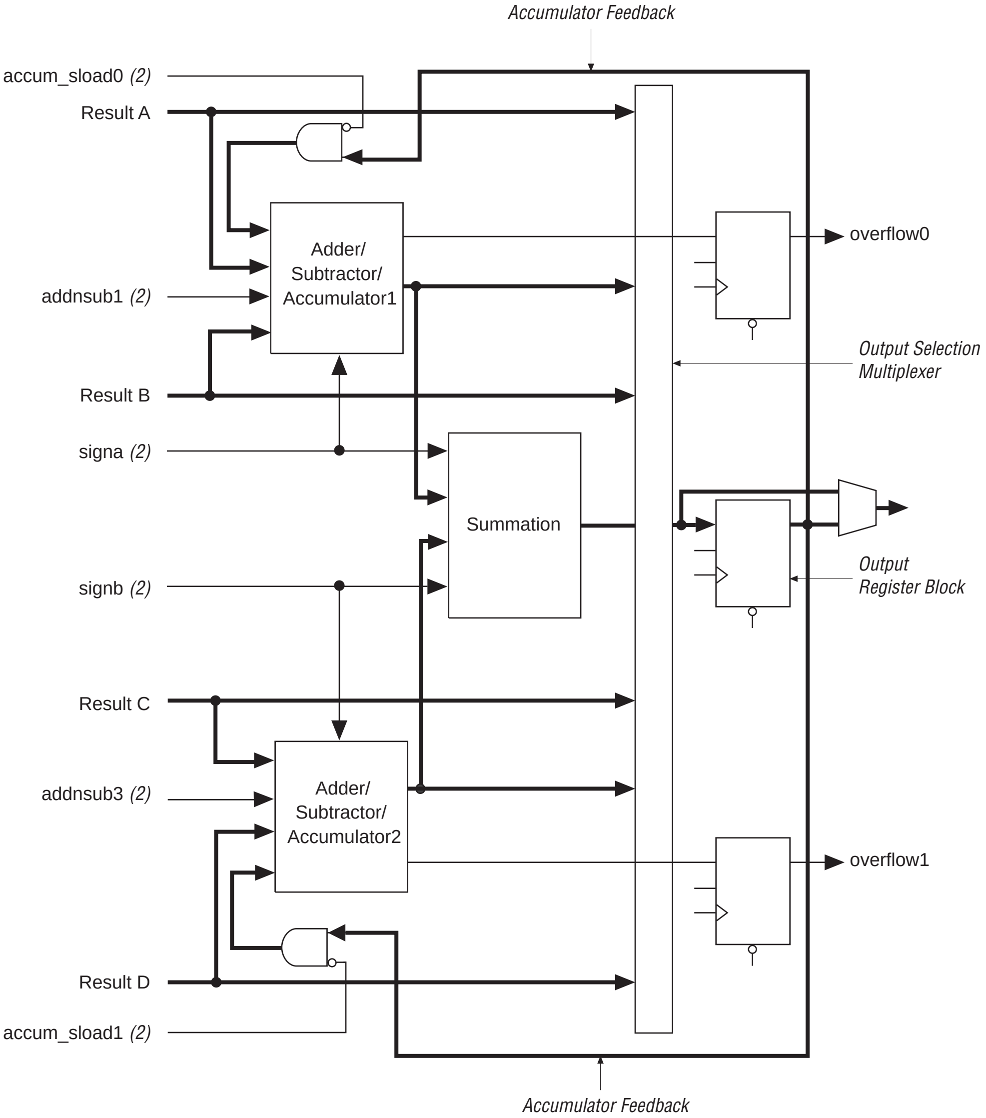
### *Pipeline/Post Multiply Register*

The output of 9 × 9- or 18 × 18-bit multipliers can optionally feed a register to pipeline multiply-accumulate and multiply-add/subtract functions. For 36 × 36-bit multipliers, this register will pipeline the multiplier function.

## Adder/Output Blocks

The result of the multiplier sub-blocks are sent to the adder/output block which consist of an adder/subtractor/accumulator unit, summation unit, output select multiplexer, and output registers. The results are used to configure the adder/output block as a pure output, accumulator, a simple two-multiplier adder, four-multiplier adder, or final stage of the 36-bit multiplier. The designer can configure the adder/output block to use output registers in any mode, and must use output registers for the accumulator. The system cannot use adder/output blocks independently of the multiplier. Figure 2–34 shows the adder and output stages.

***Figure 2–34. Adder/Output Blocks*** *Note (1)*



*Notes to Figure 2–34:*

(1) Adder/output block shown in Figure 2–34 is in 18 × 18-bit mode. In 9 × 9-bit mode, there are four adder/subtractor blocks and two summation blocks.

(2) These signals are either not registered, registered once, or registered twice to match the data path pipeline.

### *Adder/Subtractor/Accumulator*

The adder/subtractor/accumulator is the first level of the adder/output block and can be used as an accumulator or as an adder/subtractor.

#### Adder/Subtractor

Each adder/subtractor/accumulator block can perform addition or subtraction using the `addnsub` independent control signal for each first-level adder in 18 × 18-bit mode. There are two `addnsub[1..0]` signals available in a DSP block for any configuration. For 9 × 9-bit mode, one `addnsub[1..0]` signal controls the top two one-level adders and another `addnsub[1..0]` signal controls the bottom two one-level adders. A high `addnsub` signal indicates addition, and a low signal indicates subtraction. The `addnsub` control signal can be unregistered or registered once or twice when feeding the adder blocks to match data path pipelines.

The `signa` and `signb` signals serve the same function as the multiplier block `signa` and `signb` signals. The only difference is that these signals can be registered up to two times. These signals are tied to the same `signa` and `signb` signals from the multiplier and must be connected to the same clocks and control signals.

#### Accumulator

When configured for accumulation, the adder/output block output feeds back to the accumulator as shown in Figure 2–34. The `accum_sload[1..0]` signal synchronously loads the multiplier result to the accumulator output. This signal can be unregistered or registered once or twice. Additionally, the `overflow` signal indicates the accumulator has overflowed or underflowed in accumulation mode. This signal is always registered and must be externally latched in LEs if the design requires a latched `overflow` signal.

### *Summation*

The output of the adder/subtractor/accumulator block feeds to an optional summation block. This block sums the outputs of the DSP block multipliers. In 9 × 9-bit mode, there are two summation blocks providing the sums of two sets of four 9 × 9-bit multipliers. In 18 × 18-bit mode, there is one summation providing the sum of one set of four 18 × 18-bit multipliers.

### *Output Selection Multiplexer*

The outputs from the various elements of the adder/output block are routed through an output selection multiplexer. Based on the DSP block operational mode and user settings, the multiplexer selects whether the output from the multiplier, the adder/subtractor/accumulator, or summation block feeds to the output.

### *Output Registers*

Optional output registers for the DSP block outputs are controlled by four sets of control signals: `clock[3..0]`, `aclr[3..0]`, and `ena[3..0]`. Output registers can be used in any mode.

## Modes of Operation

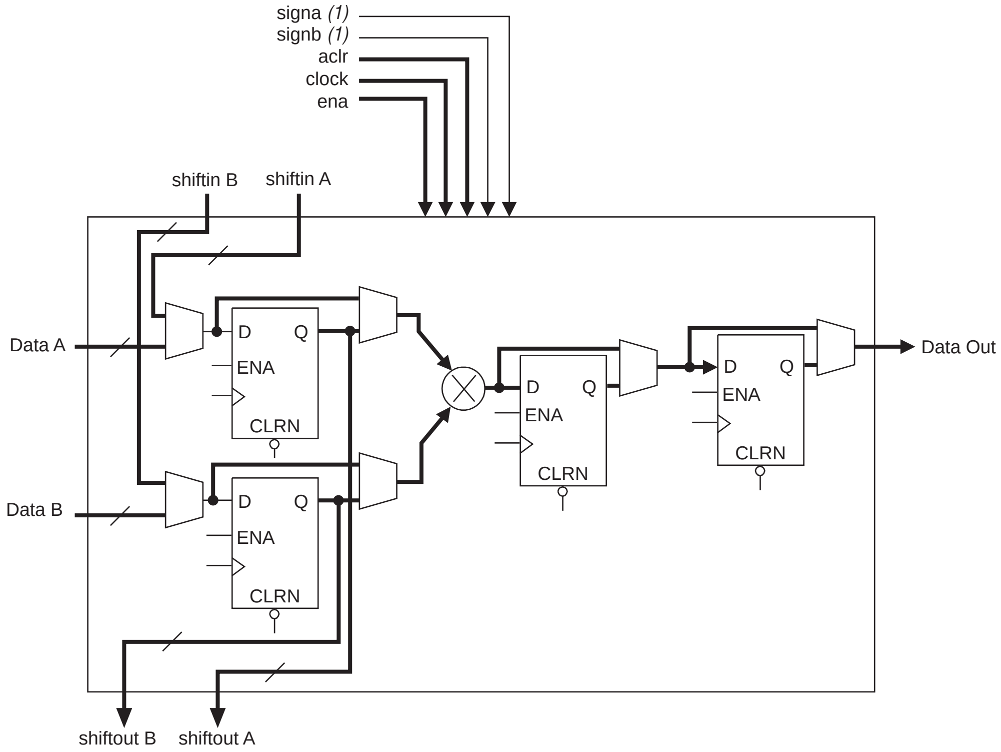
The adder, subtractor, and accumulate functions of a DSP block have four modes of operation:

- Simple multiplier
- Multiply-accumulator
- Two-multipliers adder
- Four-multipliers adder

### *Simple Multiplier Mode*

In simple multiplier mode, the DSP block drives the multiplier sub-block result directly to the output with or without an output register. Up to four 18 × 18-bit multipliers or eight 9 × 9-bit multipliers can drive their results directly out of one DSP block. See Figure 2–35.

*Figure 2–35. Simple Multiplier Mode*

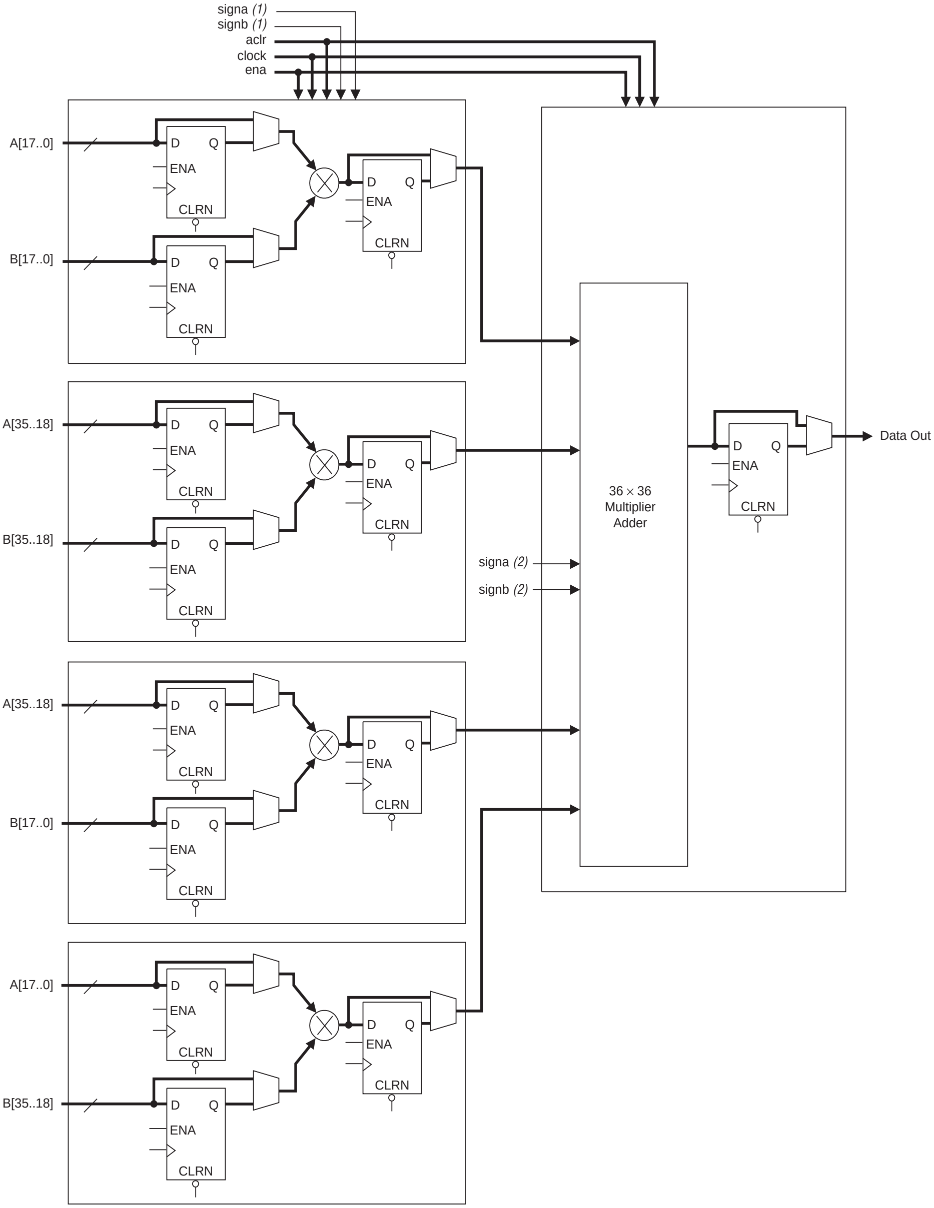


*Note to Figure 2–35:*

(1) These signals are not registered or registered once to match the data path pipeline.

DSP blocks can also implement one 36 × 36-bit multiplier in multiplier mode. DSP blocks use four 18 × 18-bit multipliers combined with dedicated adder and internal shift circuitry to achieve 36-bit multiplication. The input shift register feature is not available for the 36 × 36-bit multiplier. In 36 × 36-bit mode, the device can use the register that is normally a multiplier-result-output register as a pipeline stage for the 36 × 36-bit multiplier. Figure 2–36 shows the 36 × 36-bit multiply mode.

*Figure 2–36. 36 × 36 Multiply Mode*



*Notes to Figure 2–36:*

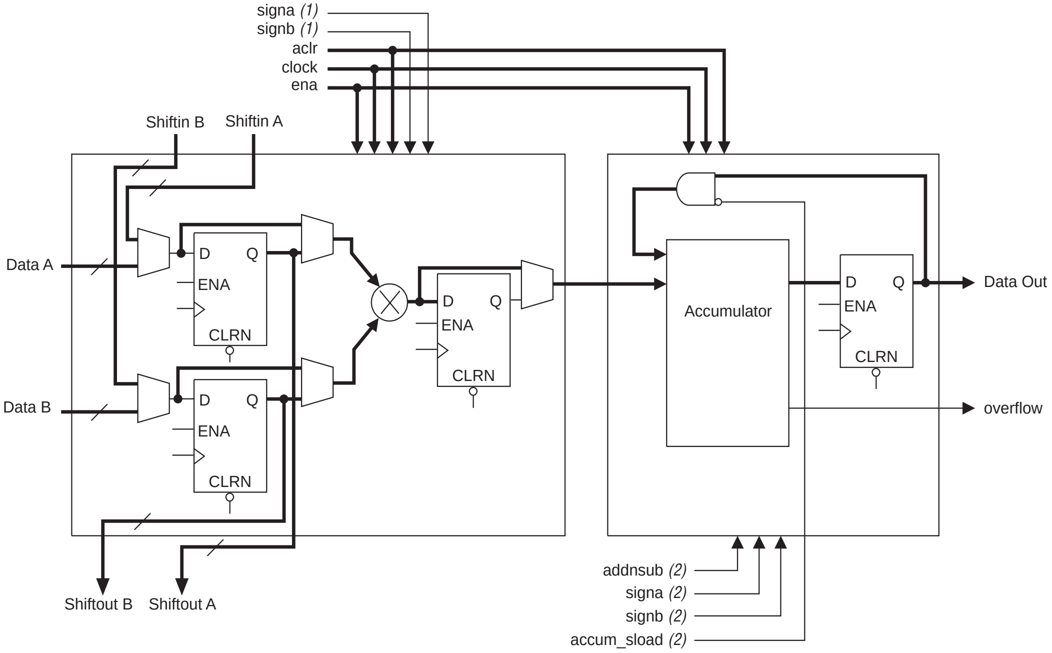
(1) These signals are not registered or registered once to match the pipeline.

(2) These signals are not registered, registered once, or registered twice for latency to match the pipeline.

### *Multiply-Accumulator Mode*

In multiply-accumulator mode (see Figure 2–37), the DSP block drives multiplied results to the adder/subtractor/accumulator block configured as an accumulator. A designer can implement one or two multiply-accumulators up to 18 × 18 bits in one DSP block. The first and third multiplier sub-blocks are unused in this mode, since only one multiplier can feed one of two accumulators. The multiply-accumulator output can be up to 52 bits—a maximum of a 36-bit result with 16 bits of accumulation. The `accum_sload` and `overflow` signals are only available in this mode. The `addnsub` signal can set the accumulator for decimation and the `overflow` signal will indicate underflow condition.

**Figure 2–37. Multiply-Accumulate Mode**



*Notes to Figure 2–37:*

(1) These signals are not registered or registered once to match the data path pipeline.

(2) These signals are not registered, registered once, or registered twice for latency to match the data path pipeline.

### *Two-Multipliers Adder Mode*

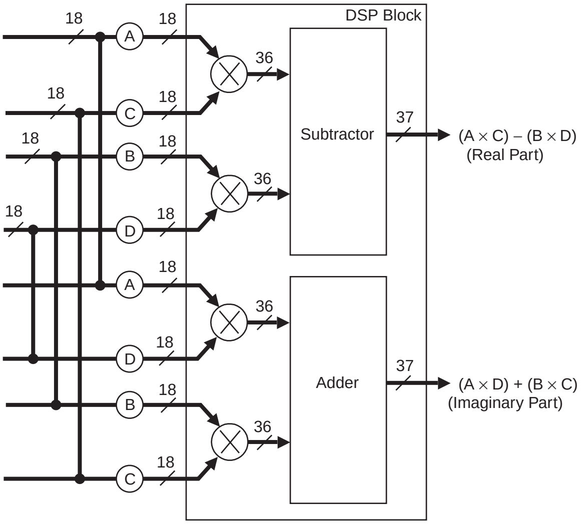
The two-multipliers adder mode uses the adder/subtractor/accumulator block to add or subtract the outputs of the multiplier block, which is useful for applications such as FFT functions and complex FIR filters. A single DSP block can implement two sums or differences from two 18 × 18-bit multipliers each or four sums or differences from two 9 × 9-bit multipliers each.

Designers can use the two-multipliers adder mode for complex multiplications, which are written as:

$$(a + jb) \times (c + jd) = [(a \times c) - (b \times d)] + j \times [(a \times d) + (b \times c)]$$

The two-multipliers adder mode allows a single DSP block to calculate the real part [(a × c) – (b × d)] using one subtractor and the imaginary part [(a × d) + (b × c)] using one adder, for data widths up to 18 bits. Two complex multiplications are possible for data widths up to 9 bits using four adder/subtractor/accumulator blocks. Figure 2–38 shows an 18-bit two-multipliers adder.

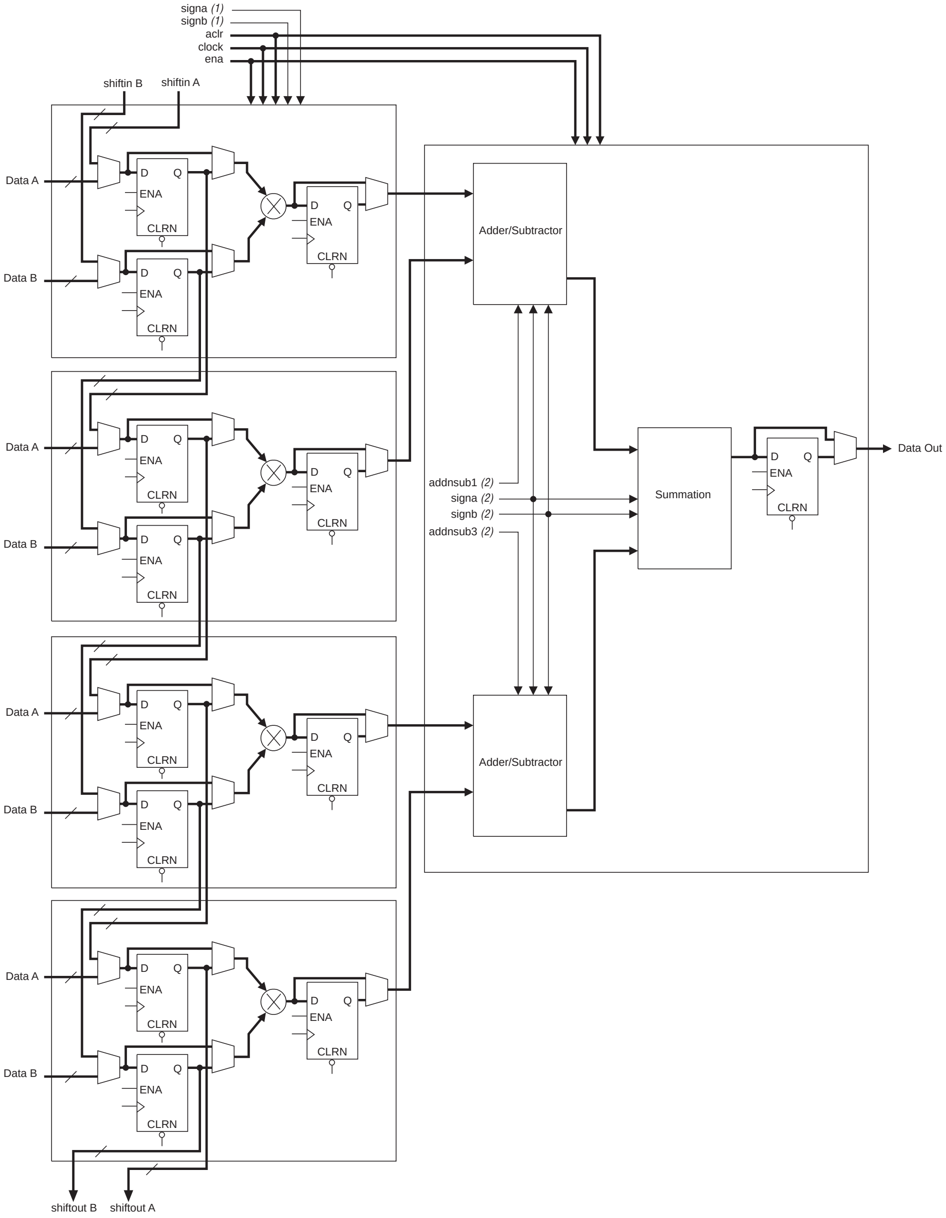
*Figure 2–38. Two-Multipliers Adder Mode Implementing Complex Multiply*



### Four-Multipliers Adder Mode

In the four-multipliers adder mode, the DSP block adds the results of two first -stage adder/subtractor blocks. One sum of four 18 × 18-bit multipliers or two different sums of two sets of four 9 × 9-bit multipliers can be implemented in a single DSP block. The product width for each multiplier must be the same size. The four-multipliers adder mode is useful for FIR filter applications. Figure 2–39 shows the four multipliers adder mode.

*Figure 2–39. Four-Multipliers Adder Mode*



*Notes to Figure 2–39:*

(1) These signals are not registered or registered once to match the data path pipeline.

(2) These signals are not registered, registered once, or registered twice for latency to match the data path pipeline.

For FIR filters, the DSP block combines the four-multipliers adder mode with the shift register inputs. One set of shift inputs contains the filter data, while the other holds the coefficients loaded in serial or parallel. The input shift register eliminates the need for shift registers external to the DSP block (i.e., implemented in LEs). This architecture simplifies filter design since the DSP block implements all of the filter circuitry.

One DSP block can implement an entire 18-bit FIR filter with up to four taps. For FIR filters larger than four taps, DSP blocks can be cascaded with additional adder stages implemented in LEs.

Table 2–16 shows the different number of multipliers possible in each DSP block mode according to size. These modes allow the DSP blocks to implement numerous applications for DSP including FFTs, complex FIR, FIR, and 2D FIR filters, equalizers, IIR, correlators, matrix multiplication and many other functions.

*Table 2–16. Multiplier Size & Configurations per DSP block*

| DSP Block Mode | 9 × 9 | 18 × 18 | 36 × 36 (1) |
|---|---|---|---|
| Multiplier | Eight multipliers with eight product outputs | Four multipliers with four product outputs | One multiplier with one product output |
| Multiply-accumulator | Two multiply and accumulate (52 bits) | Two multiply and accumulate (52 bits) | – |
| Two-multipliers adder | Four sums of two multiplier products each | Two sums of two multiplier products each | – |
| Four-multipliers adder | Two sums of four multiplier products each | One sum of four multiplier products each | – |

*Note to Table 2–16:*

(1) The number of supported multiply functions shown is based on signed/signed or unsigned/unsigned implementations.

## DSP Block Interface

Stratix device DSP block outputs can cascade down within the same DSP block column. Dedicated connections between DSP blocks provide fast connections between the shift register inputs to cascade the shift register chains. The designer can cascade DSP blocks for 9 × 9- or 18 × 18-bit FIR filters larger than four taps, with additional adder stages implemented in LEs. If the DSP block is configured as 36 × 36 bits, the adder, subtractor, or accumulator stages are implemented in LEs. Each DSP block can route the shift register chain out of the block to cascade two full columns of DSP blocks.

The DSP block is divided into eight block units that interface with eight LAB rows on the left and right. Each block unit can be considered half of an 18 × 18-bit multiplier sub-block with 18 inputs and 18 outputs. A local interconnect region is associated with each DSP block. Like an LAB, this interconnect region can be fed with 10 direct link interconnects from the LAB to the left or right of the DSP block in the same row. All row and column routing resources can access the DSP block's local interconnect region. The outputs also work similarly to LAB outputs as well. Nine outputs from the DSP block can drive to the left LAB through direct link interconnects and nine can drive to the right LAB though direct link interconnects. All 18 outputs can drive to all types of row and column routing. Outputs can drive right- or left-column routing. Figures 2–40 and 2–41 show the DSP block interfaces to LAB rows.

**Figure 2–40. DSP Block Interconnect Interface**

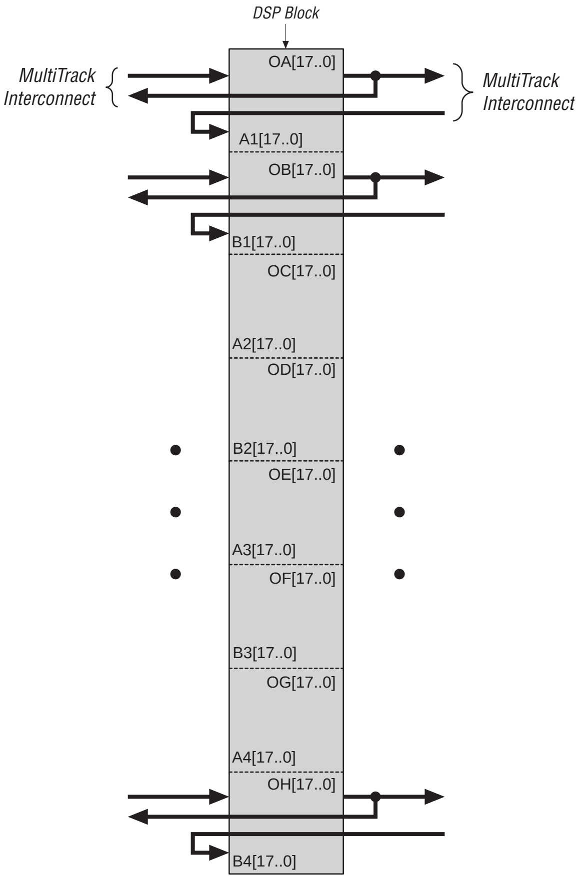
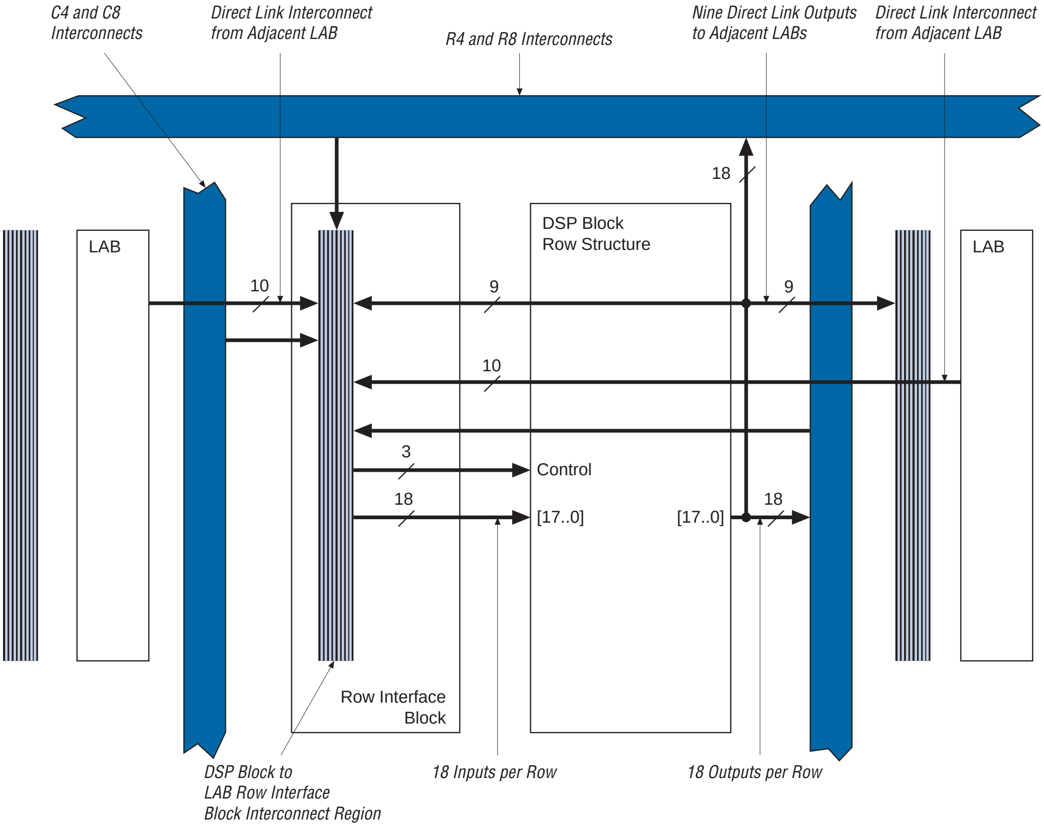


*Figure 2–41. DSP Block Interface to Interconnect*



A bus of 18 control signals feeds the entire DSP block. These signals include `clock[0..3]` clocks, `aclr[0..3]` asynchronous clears, `ena[1..4]` clock enables, `signa`, `signb` signed/unsigned control signals, `addnsub1` and `addnsub3` addition and subtraction control signals, and `accum_sload[0..1]` accumulator synchronous loads. The clock signals are routed from LAB row clocks and are generated from specific LAB rows at the DSP block interface. The LAB row source for control signals, data inputs, and outputs is shown in Table 2–17.

*Table 2–17. DSP Block Signal Sources & Destinations*

| LAB Row at Interface | Control Signals Generated | Data Inputs | Data Outputs |
|---|---|---|---|
| 1 | `signa` | `A1[17..0]` | `OA[17..0]` |
| 2 | `aclr0`<br>`accum_sload0` | `B1[17..0]` | `OB[17..0]` |
| 3 | `addnsub1`<br>`clock0`<br>`ena0` | `A2[17..0]` | `OC[17..0]` |
| 4 | `aclr1`<br>`clock1`<br>`ena1` | `B2[17..0]` | `OD[17..0]` |
| 5 | `aclr2`<br>`clock2`<br>`ena2` | `A3[17..0]` | `OE[17..0]` |
| 6 | `sign_b`<br>`clock3`<br>`ena3` | `B3[17..0]` | `OF[17..0]` |
| 7 | `clear3`<br>`accum_sload1` | `A4[17..0]` | `OG[17..0]` |
| 8 | `addnsub3` | `B4[17..0]` | `OH[17..0]` |

# PLLs & Clock Networks

Stratix devices provide a hierarchical clock structure and multiple PLLs with advanced features. The large number of clocking resources in combination with the clock synthesis precision provided by enhanced and fast PLLs provides a complete clock management solution.

## Global & Hierarchical Clocking

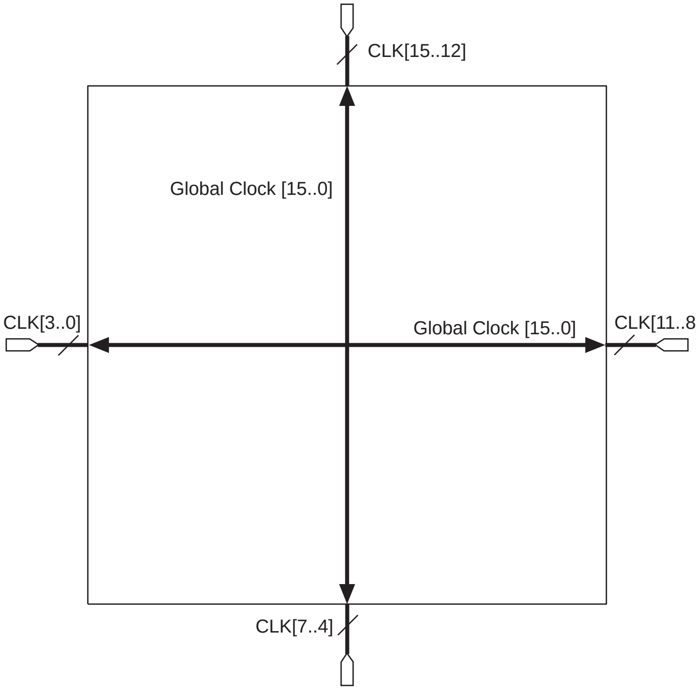
Stratix devices provide 16 dedicated global clock networks, 16 regional clock networks (four per device quadrant), and 8 dedicated fast regional clock networks. These clocks are organized into a hierarchical clock structure that allows for up to 22 clocks per device region with low skew and delay. This hierarchical clocking scheme provides up to 48 unique clock domains within Stratix devices.

There are 16 dedicated clock pins (`CLK[15..0]`) to drive either the global or regional clock networks. Four clock pins drive each side of the device, as shown in Figures 2–42 and 2–43. Enhanced and fast PLL outputs can also drive the global and regional clock networks.

### *Global Clock Network*

These clocks drive throughout the entire device, feeding all device quadrants. The global clock networks can be used as clock sources for all resources within the device—IOEs, LEs, DSP blocks, and all memory blocks. These resources can also be used for control signals, such as clock enables and synchronous or asynchronous clears fed from the external pin. The global clock networks can also be driven by internal logic for internally generated global clocks and asynchronous clears, clock enables, or other control signals with large fanout. Figure 2–42 shows the 16 dedicated `CLK` pins driving global clock networks.

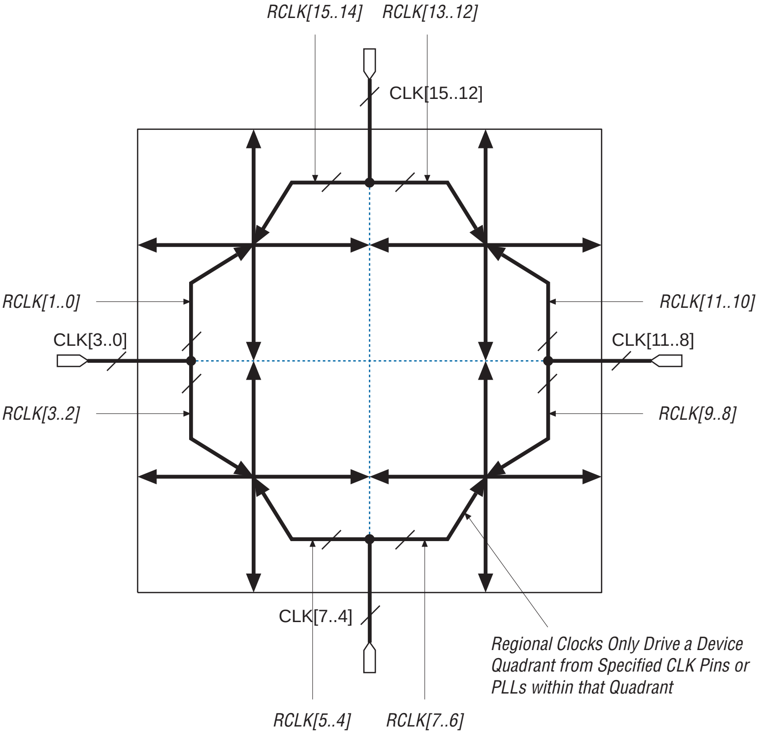
***Figure 2–42. Global Clocking***



### Regional Clock Network

There are four regional clock networks `RCLK[3..0]` within each quadrant of the Stratix device that are driven by the same dedicated `CLK[15..0]` input pins or from PLL outputs. The regional clock networks only pertain to the quadrant they drive into. The regional clock networks provide the lowest clock delay and skew for logic contained within a single quadrant. The `CLK` clock pins symmetrically drive the `RCLK` networks within a particular quadrant, as shown in Figure 2–43.

**Figure 2–43. Regional Clocks**

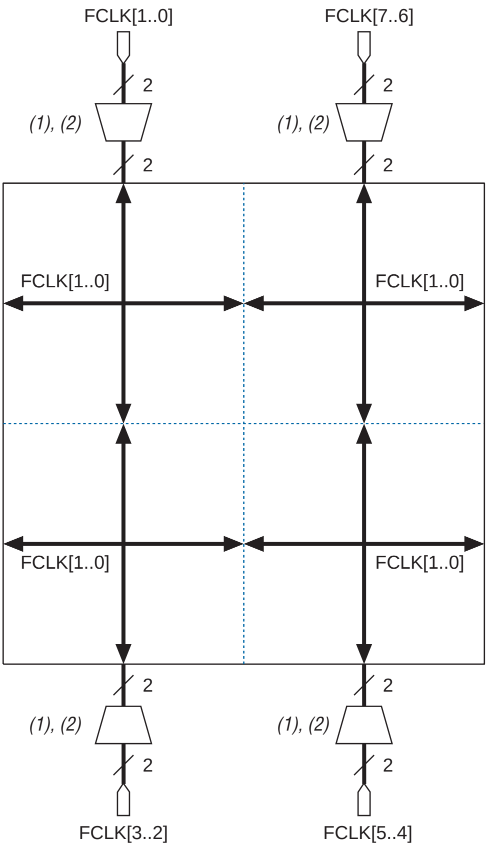


Regional Clocks Only Drive a Device Quadrant from Specified CLK Pins or PLLs within that Quadrant

### Fast Regional Clock Network

In EP1S25, EP1S20, and EP1S10 devices, there are two fast regional clock networks, `FCLK[1..0]`, within each quadrant, fed by input pins that can connect to fast regional clock networks (see Figure 2–44). In EP1S30 and larger devices, there are two fast regional clock networks within each half-quadrant (see Figure 2–45). Dual-purpose `FCLK` pins drive the fast clock networks. All devices have eight `FCLK` pins to drive fast regional clock networks. Any I/O pin can drive a clock or control signal onto any fast regional clock network with the addition of a delay. This signal is driven via the I/O interconnect.

*Figure 2–44. EP1S25, EP1S20 & EP1S10 Device Fast Clock Pin Connections to Fast Regional Clocks*

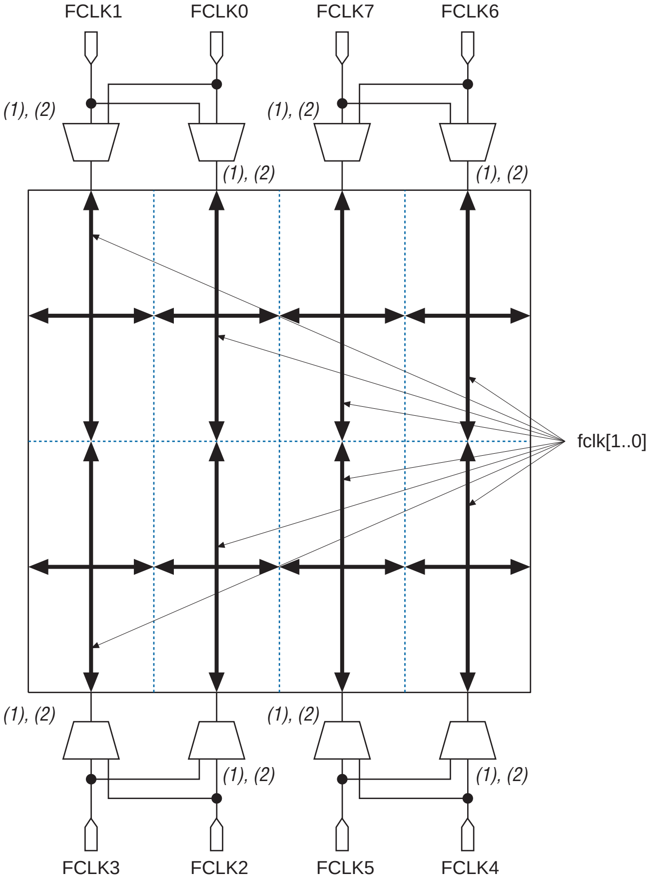


*Notes to Figure 2–44:*

(1) This is a set of two multiplexers.

(2) In addition to the `FCLK` pin inputs, there is also an input from the I/O interconnect.

*Figure 2–45. EP1S30 Device Fast Regional Clock Pin Connections to Fast Regional Clocks*



*Notes to Figure 2–45:*

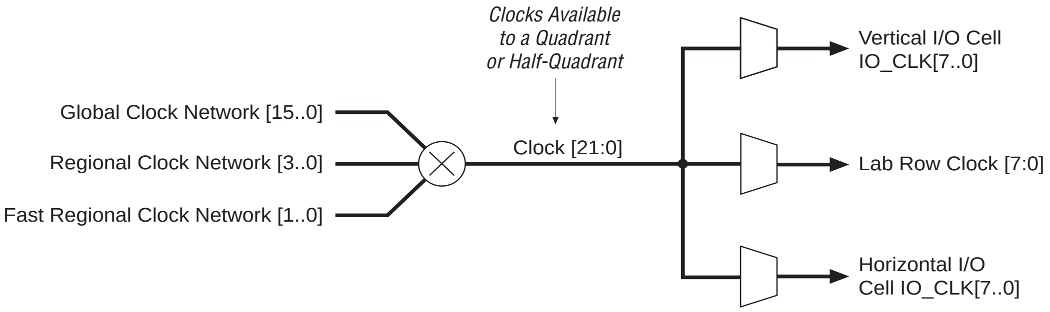
(1) This is a set of two multiplexers.

(2) In addition to the `FCLK` pin inputs, there is also an input from the I/O interconnect.

## Combined Resources

Within each region, there are 22 distinct dedicated clocking resources consisting of 16 global clock lines, four regional clock lines, and two fast regional clock lines. Multiplexers are used with these clocks to form eight bit busses to drive LAB row clocks, column IOE clocks, or row IOE clocks. Another multiplexer is used at the LAB level to select two of the eight row clocks to feed the LE registers within the LAB. See Figure 2–46.

*Figure 2–46. Regional Clock Bus*



IOE clocks have horizontal and vertical block regions that are clocked by eight I/O clock signals chosen from the 22 quadrant or half-quadrant clock resources. Figures 2–47 and 2–48 show the quadrant and half-quadrant relationship to the I/O clock regions, respectively. The vertical regions (column pins) have less clock delay than the horizontal regions (row pins).

*Figure 2–47. EP1S10, EP1S20 & EP1S25 Device I/O Clock Groups*

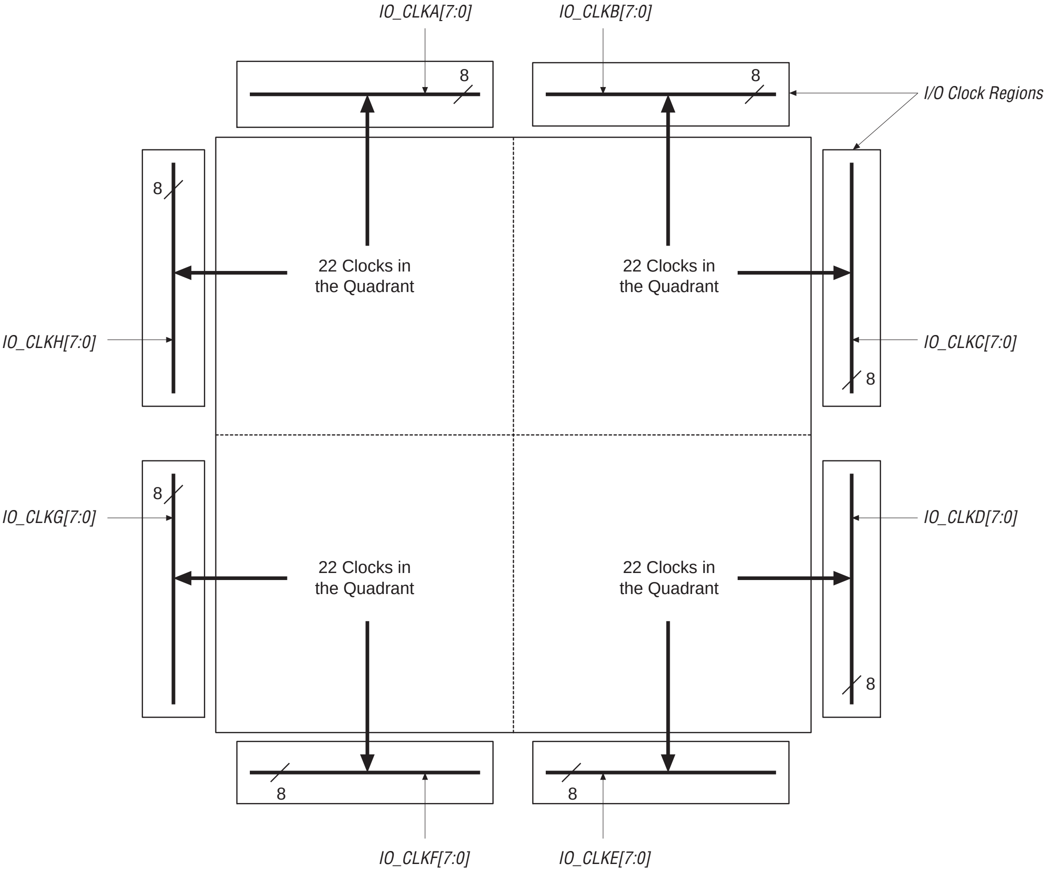
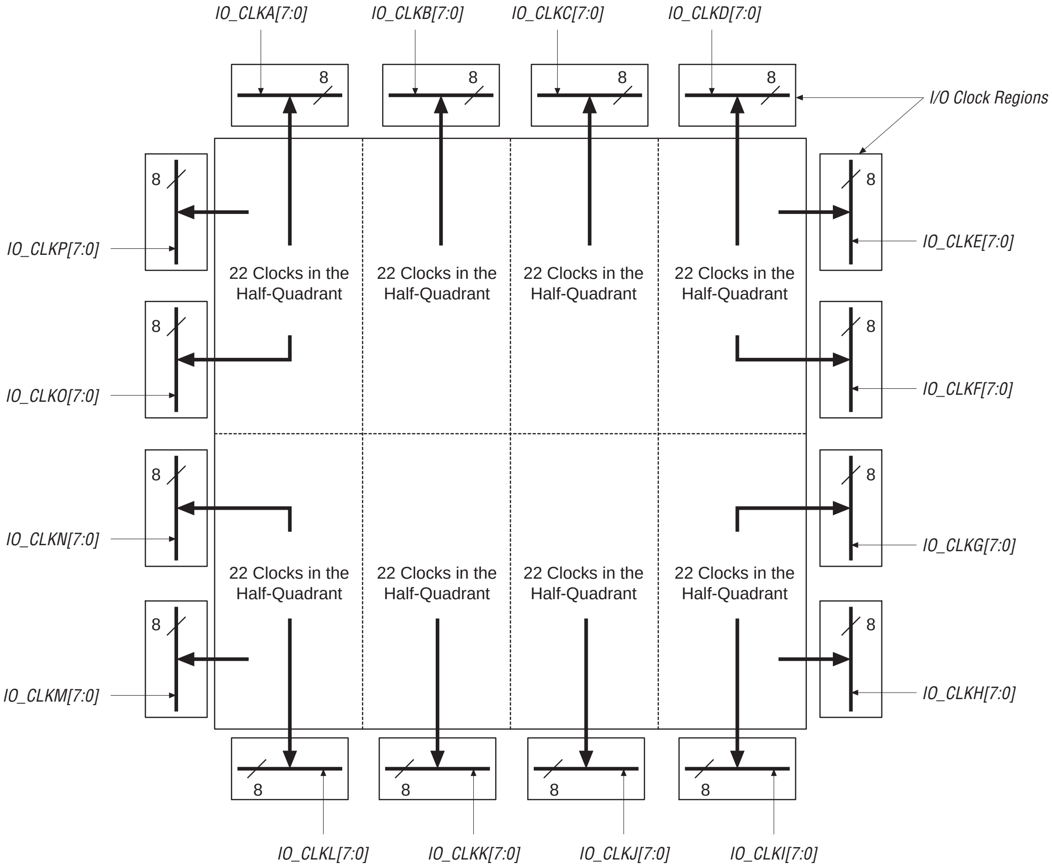


*Figure 2–48. EP1S30, EP1S40, EP1S60, EP1S80 Device I/O Clock Groups*



Designers can use the Quartus II software to control whether a clock input pin is either global, regional, or fast regional. The Quartus II software automatically selects the clocking resources if not specified.

## Enhanced & Fast PLLs

Stratix devices provide robust clock management and synthesis using up to four enhanced PLLs and eight fast PLLs. These PLLs increase performance and provide advanced clock interfacing and clock-frequency synthesis. With features such as clock switchover, spread spectrum clocking, programmable bandwidth, phase and delay control, and PLL reconfiguration, the Stratix device's enhanced PLLs provide designers with complete control of their clocks and system timing. The fast PLLs provide general purpose clocking with multiplication and phase shifting as well as high-speed outputs for high-speed differential I/O support. Enhanced and fast PLLs work together with the Stratix high-speed I/O and advanced clock architecture to provide significant improvements in system performance and bandwidth.

The Quartus II software enables the PLLs and their features without requiring any external devices. Tables 2–18 and 2–19 show the PLLs available for each Stratix device, respectively, and their type.

*Table 2–18. Stratix Device PLL Availability*

| Device | Fast PLLs | | | | | | | | Enhanced PLLs | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 7 | 8 | 9 | 10 | 5 *(1)* | 6 *(1)* | 11 *(2)* | 12 *(2)* |
| EP1S10 | ✓ | ✓ | ✓ | ✓ | | | | | ✓ | ✓ | | |
| EP1S20 | ✓ | ✓ | ✓ | ✓ | | | | | ✓ | ✓ | | |
| EP1S25 | ✓ | ✓ | ✓ | ✓ | | | | | ✓ | ✓ | | |
| EP1S30 | ✓ | ✓ | ✓ | ✓ | ✓ *(3)* | ✓ *(3)* | ✓ *(3)* | ✓ *(3)* | ✓ | ✓ | | |
| EP1S40 | ✓ | ✓ | ✓ | ✓ | ✓ *(3)* | ✓ *(3)* | ✓ *(3)* | ✓ *(3)* | ✓ | ✓ | ✓ | ✓ |
| EP1S60 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| EP1S80 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

***Notes to Table 2–18:***

(1) PLLs 5 and 6 each have eight single-ended outputs or four differential outputs.
(2) PLLs 11 and 12 each have one single-ended output.
(3) EP1S30 and EP1S40 devices do not support these PLLs in the 780-pin FineLine BGA® package.

*Table 2–19. Stratix Device PLL Availability*

| Device | Fast PLLs | | | | Enhanced PLLs | | | |
|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 7 | 8 | 5 | 6 | 11 | 12 |
| EP1S10C | ✓ | ✓ | | | ✓ | ✓ | | |
| EP1S10D | ✓ | ✓ | | | ✓ | ✓ | | |
| EP1S25C | ✓ | ✓ | | | ✓ | ✓ | | |
| EP1S25D | ✓ | ✓ | | | ✓ | ✓ | | |
| EP1S25F | ✓ | ✓ | | | ✓ | ✓ | | |
| EP1S40D | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| EP1S40G | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

Table 2–20 shows the enhanced PLL and fast PLL features in Stratix devices.

*Table 2–20. Stratix PLL Features*

| Feature | Enhanced PLL | Fast PLL |
|---|---|---|
| Clock multiplication and division | *m*/(*n* × post-scale counter) *(1)* | *m*/(post-scale counter) *(2)* |
| Phase shift | Down to 156.25-ps increments *(3)*, *(4)* | Down to 125-ps increments *(3)*, *(4)* |
| Delay shift | 250-ps increments for ±3 ns | |
| Clock switchover | ✓ | |
| PLL reconfiguration | ✓ | |
| Programmable bandwidth | ✓ | |
| Spread spectrum clocking | ✓ | |
| Programmable duty cycle | ✓ | ✓ |
| Number of internal clock outputs | 6 | 3 *(5)* |
| Number of external clock outputs | Four differential/eight singled-ended or one single-ended *(6)* | *(7)* |
| Number of feedback clock inputs | 2 *(8)* | |

***Notes to Table 2–20:***

(1) For enhanced PLLs, *m*, *n*, and post-scale counters range from 1 to 512.

(2) For fast PLLs, *m*, *n*, and post-scale counters range from 1 to 32.

(3) The smallest phase shift is determined by the voltage controlled oscillator (VCO) period divided by 8.

(4) For degree increments, Stratix devices can shift all output frequencies in increments of at least 45°. Smaller degree increments are possible depending on the frequency and divide parameters.

(5) PLLs 7, 8, 9, and 10 have two output ports per PLL. PLLs 1, 2, 3, and 4 have three output ports per PLL.

(6) Every Stratix device has two enhanced PLLs (PLLs 5 and 6) with either eight single-ended outputs or four differential outputs each. Two additional enhanced PLLs (PLLs 11 and 12) in EP1S80, EP1S60, EP1S40 devices each have one single-ended output.

(7) Fast PLLs can drive to any I/O pin as an external clock. For high-speed differential I/O pins, the device uses a data channel to generate `txclkout`.

(8) Every Stratix device has two enhanced PLLs with one single-ended or differential external feedback input per PLL.

Figure 2–49 shows a top-level diagram of the Stratix device and PLL floorplan.

*Figure 2–49. PLL Locations*

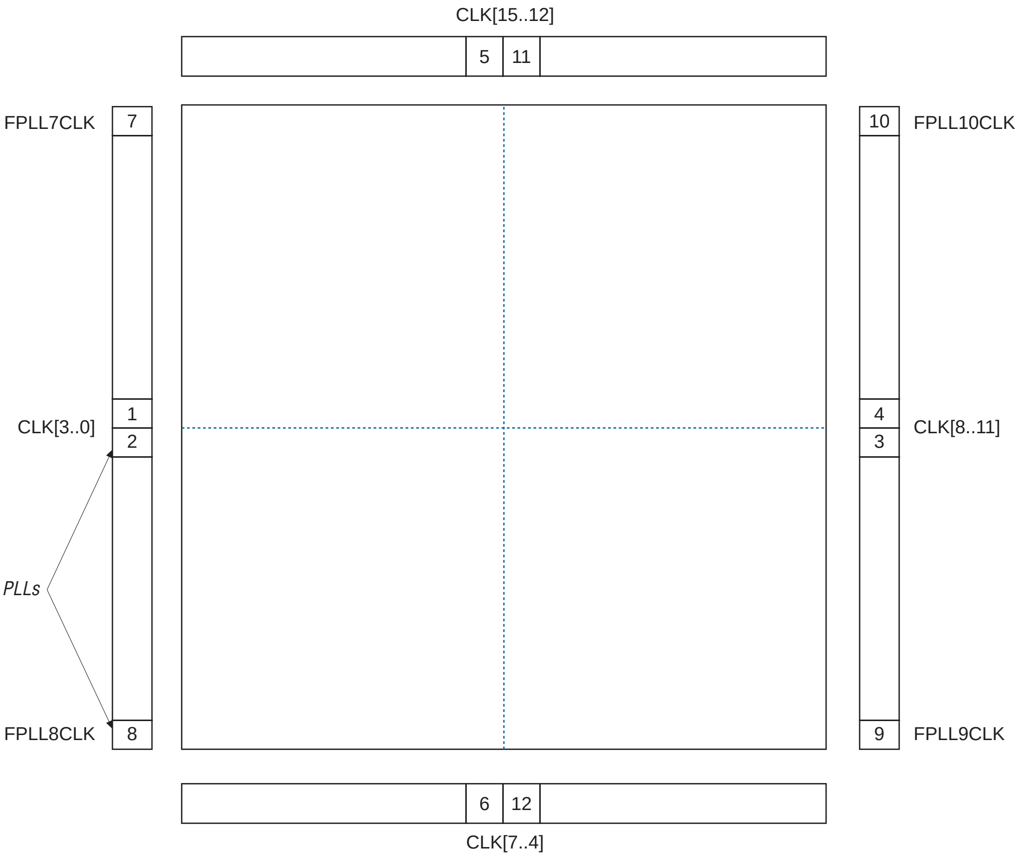
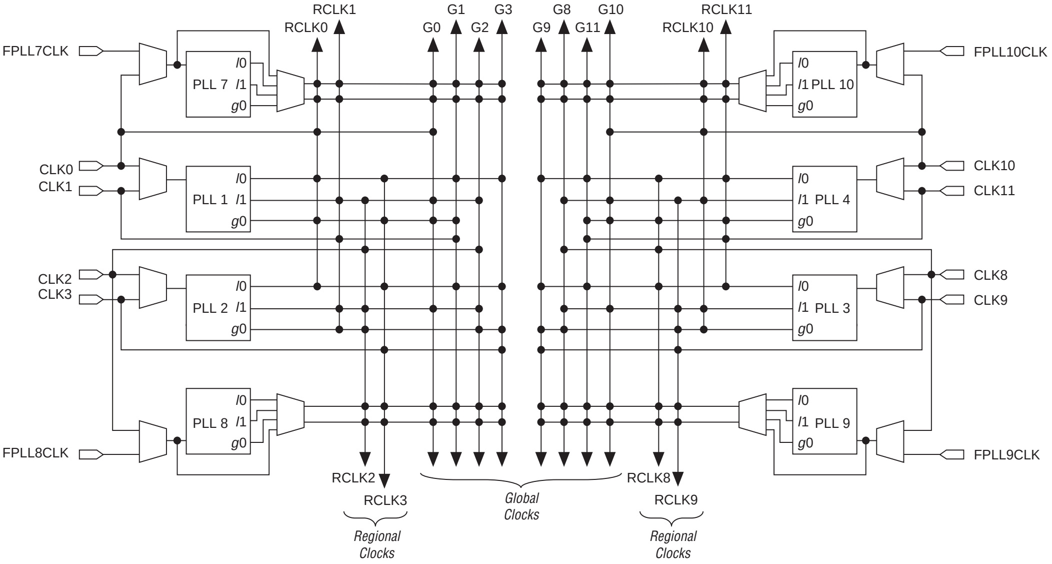


Figure 2–50 shows the global and regional clocking from the PLL outputs and the CLK pins.

*Figure 2–50. Global & Regional Clock Connections from Side Pins & Fast PLL Outputs* Note (1)



*Notes to Figure 2–50:*

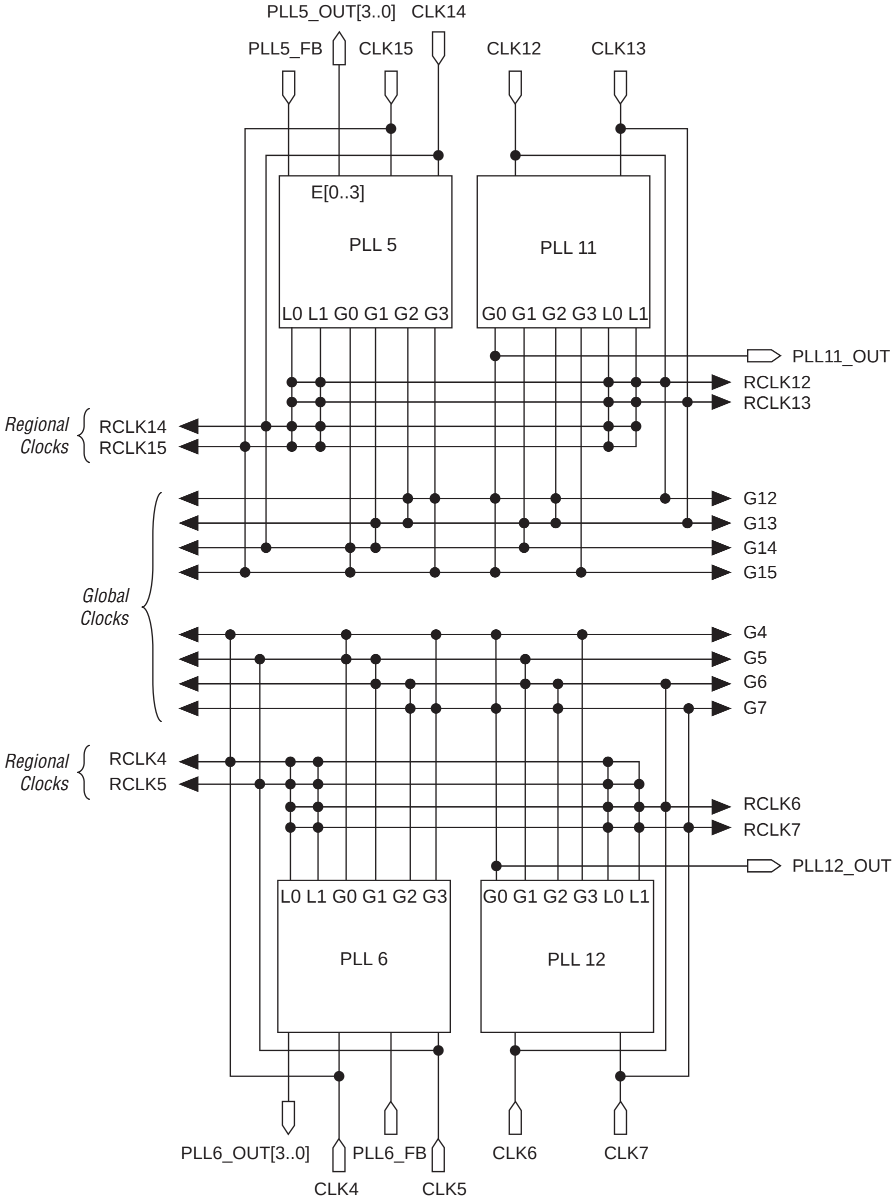
(1) PLLs 1 to 4 and 7 to 10 are fast PLLs. PLLs 5, 6, 11, and 12 are enhanced PLLs.

(2) The global or regional clocks in a fast PLL's quadrant can drive the fast PLL input. A pin or other PLL must drive the global or regional source. The source cannot be driven by internally generated logic before driving the fast PLL.

(3) PLLs 3, 4, 9, and 10 are used for the HSSI block in Stratix devices and are not available for this use.

Figure 2–51 shows the global and regional clocking from enhanced PLL outputs and top `CLK` pins.

*Figure 2–51. Global & Regional Clock Connections from Top Clock Pins & Enhanced PLL Outputs* *Note (1)*



*Notes to Figure 2–51:*

(1) PLLs 1 to 4 and 7 to 10 are fast PLLs. PLLs 5, 6, 11, and 12 are enhanced PLLs.

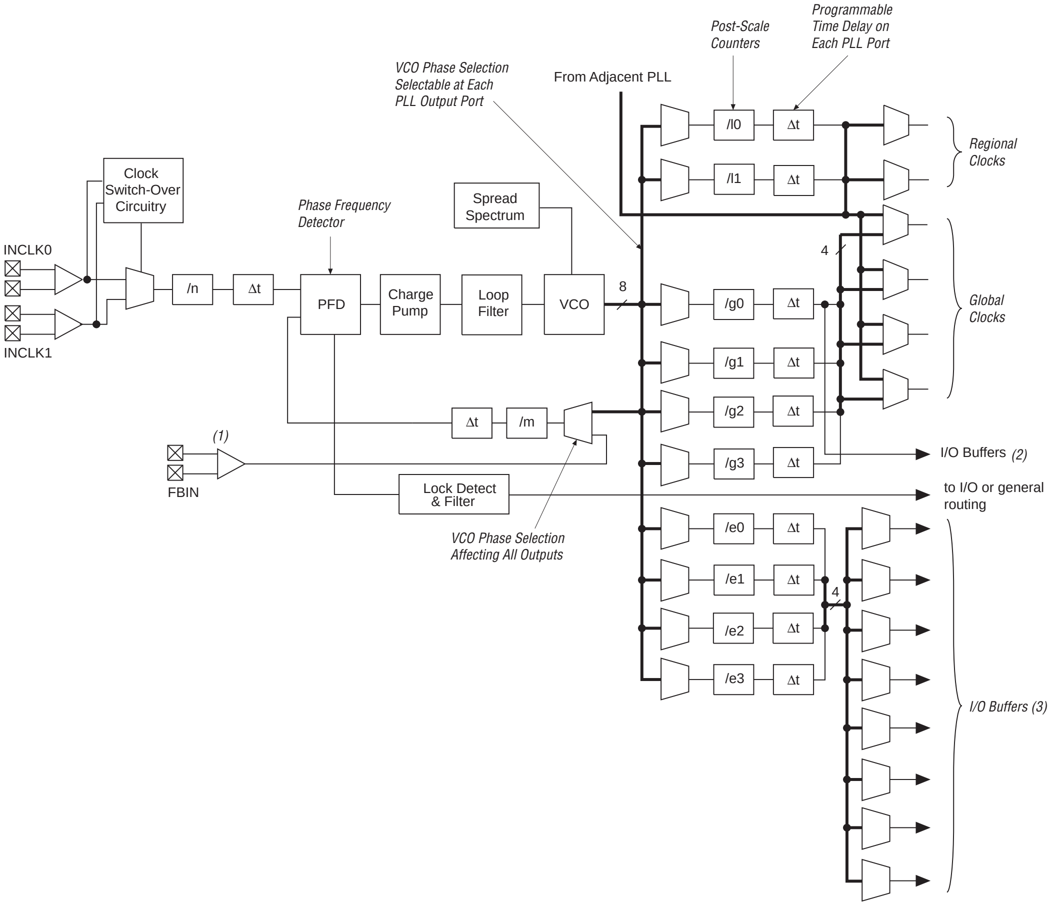
(2) `CLK4`, `CLK6`, `CLK12`, and `CLK14` feed the corresponding PLL's `inclk0` port.

(3) `CLK5`, `CLK7`, `CLK13`, and `CLK15` feed the corresponding PLL's `inclk1` port.

## Enhanced PLLs

Stratix devices contain up to four enhanced PLLs with advanced clock management features. Figure 2–52 shows a diagram of the enhanced PLL.

*Figure 2–52. Stratix Enhanced PLL*



*Notes to Figure 2–52:*

(1) External feedback is available in PLLs 5 and 6.
(2) This single-ended external output is available from the *g*0 counter for PLLs 11 and 12.
(3) These four counters and external outputs are available in PLLs 5 and 6.
(4) This connection is only available on EP1S40 and larger Stratix devices. For example, PLLs 5 and 11 are adjacent and PLLs 6 and 12 are adjacent.

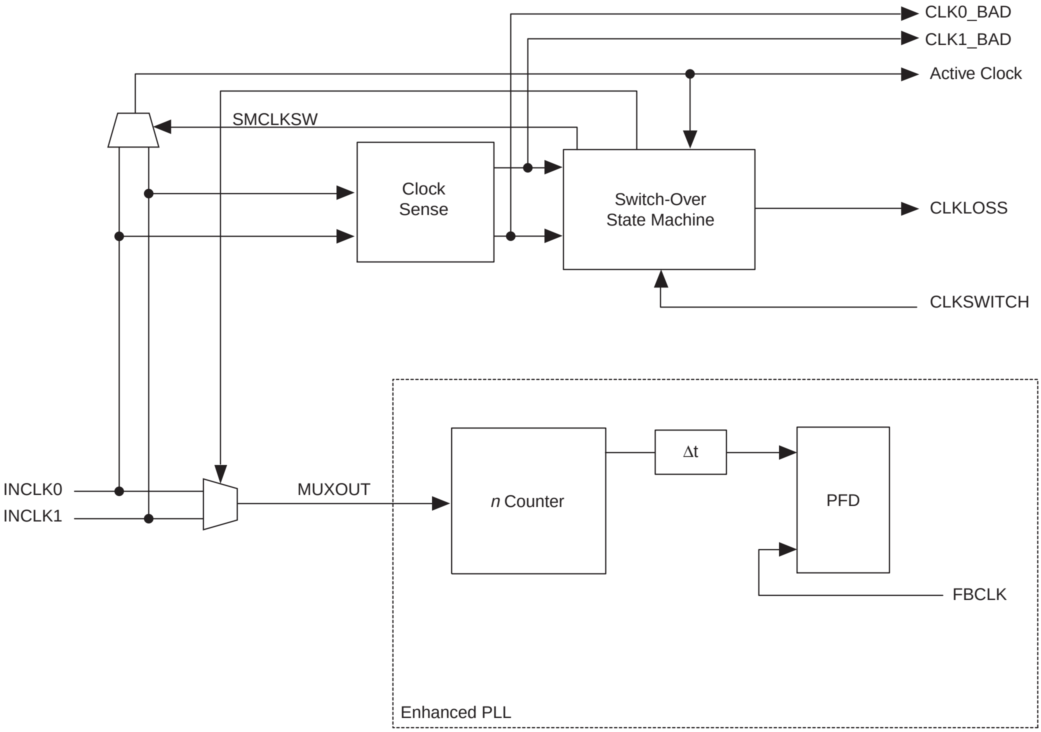
### Clock Multiplication & Division

Each Stratix device enhanced PLL provides clock synthesis for PLL output ports using $m/(n \times \text{post-scale counter})$ scaling factors. The input clock is divided by a pre-scale divider, $n$, and is then multiplied by the $m$ feedback factor. The control loop drives the VCO to match $f_{IN} \times (m/n)$. Each output port has a unique post-scale counter that divides down the high-frequency VCO. For multiple PLL outputs with different frequencies, the VCO is set to the least common multiple of the output frequencies that meets its frequency specifications. Then, the post-scale dividers scale down the output frequency for each output port. For example, if output frequencies required from one PLL are 33 and 66 MHz, set the VCO to 330 MHz (the least common multiple in the VCO's range). There is one pre-scale divider, $n$, and one multiply divider, $m$, per PLL, with a range of 1 to 512 on each. There are two post-scale dividers ($l$) for regional clock output ports, four counters ($g$) for global clock output ports, and up to four counters ($e$) for external clock outputs, all ranging from 1 to 512. The Quartus II software automatically chooses the appropriate scaling factors according to the input frequency, multiplication, and division values entered.

### Clock Switchover

To effectively develop high-reliability network systems, clocking schemes must support multiple clocks to provide redundancy. For this reason, Stratix device enhanced PLLs support a flexible clock switchover capability. Figure 2–53 shows a block diagram of the switchover circuit. The switchover circuit is configurable, so the designer can define how to implement it. Clock-sense circuitry automatically switches from the primary to secondary clock for PLL reference when the primary clock signal is not present.

*Figure 2–53. Clock Switchover Circuitry*



*Note to Figure 2–53:*
(1) PFD: phase frequency detector.

There are two possible ways to use the clock switch-over feature.

- Designers can use automatic switch-over circuitry for switching between inputs of the same frequency. For example, in applications that require a redundant clock with the same frequency as the primary clock, the switchover state machine generates a signal that controls the multiplexer select input on the bottom of Figure 2–53. In this case, the secondary clock becomes the reference clock for the PLL.

- Designers can use the `clkswitch` input for user- or system-controlled switch conditions. This is possible for same-frequency switchover or to switch between inputs of different frequencies. For example, if `inclk0` is 66 MHz and `inclk1` is 100 MHz, the designer must control the switchover because the automatic clock-sense circuitry cannot monitor primary and secondary clock frequencies with a frequency difference of more than ±20%. This feature is useful when clock sources can originate from multiple cards on the backplane, requiring a system-controlled switchover between frequencies of operation. The designer can use `clkswitch` together with the lock signal to trigger the switch from a clock that is running but becomes unstable and cannot be locked onto.

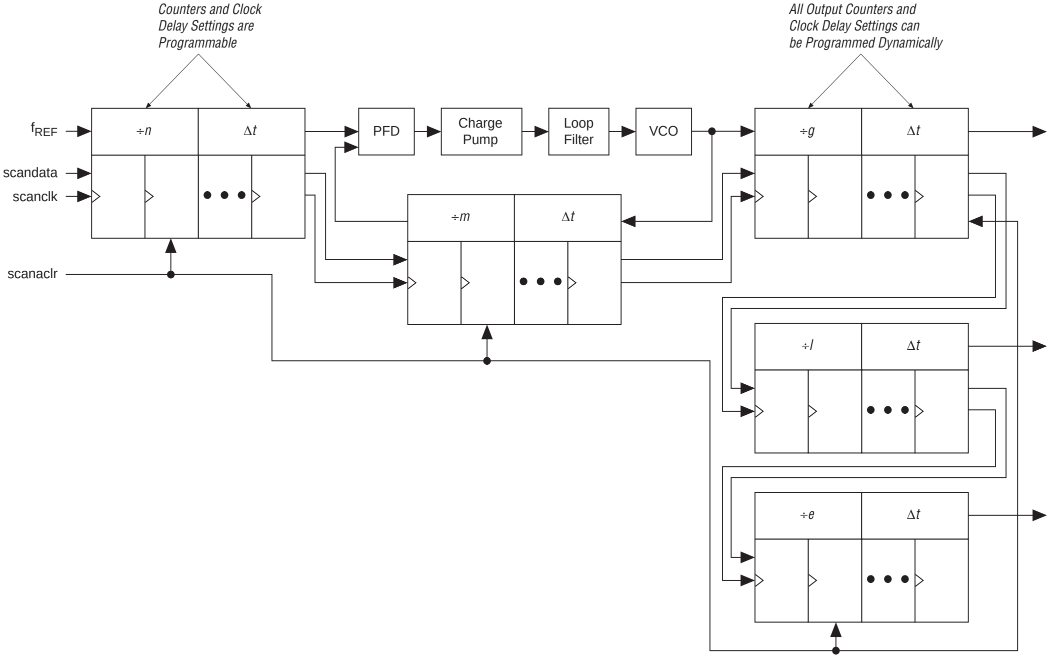
During switch over, the PLL VCO continues to run and will either slow down or speed up, generating frequency drift on the PLL outputs. The clock switchover transitions without any glitches. After the switch, there is a finite resynchronization period to lock onto new clock as the VCO ramps up. The exact amount of time it takes for the PLL to relock relates to the PLL configuration and may be adjusted by using the programmable bandwidth feature of the PLL. The preliminary specification for the maximum time to relock is 100 µs.

### *PLL Reconfiguration*

The PLL reconfiguration feature enables system logic to change Stratix device enhanced PLL counters and delay elements without reloading a Programmer Object File (**.pof**). This provides considerable flexibility for frequency synthesis, allowing real-time PLL frequency and output clock delay variation. The designer can sweep the PLL output frequencies and clock delay in prototype environments. The PLL reconfiguration feature can also dynamically or intelligently control system clock speeds or $t_{CO}$ delays in end systems.

Clock delay elements at each PLL output port implement variable delay. Figure 2–54 shows a diagram of the overall dynamic PLL control feature for the counters and the clock delay elements. The configuration time is less than 20 µs for the enhanced PLL using a input shift clock rate of 25 MHz. The charge pump, loop filter components, and phase shifting using VCO phase taps cannot be dynamically adjusted.

***Figure 2–54. Dynamically Programmable Counters & Delays in Stratix Device Enhanced PLLs***



PLL reconfiguration data is shifted into serial registers from the logic array or external devices. The PLL input shift data uses a reference input shift clock. Once the last bit of the serial chain is clocked in, the register chain is synchronously loaded into the PLL configuration bits. The shift circuitry also provides an asynchronous clear for the serial registers.

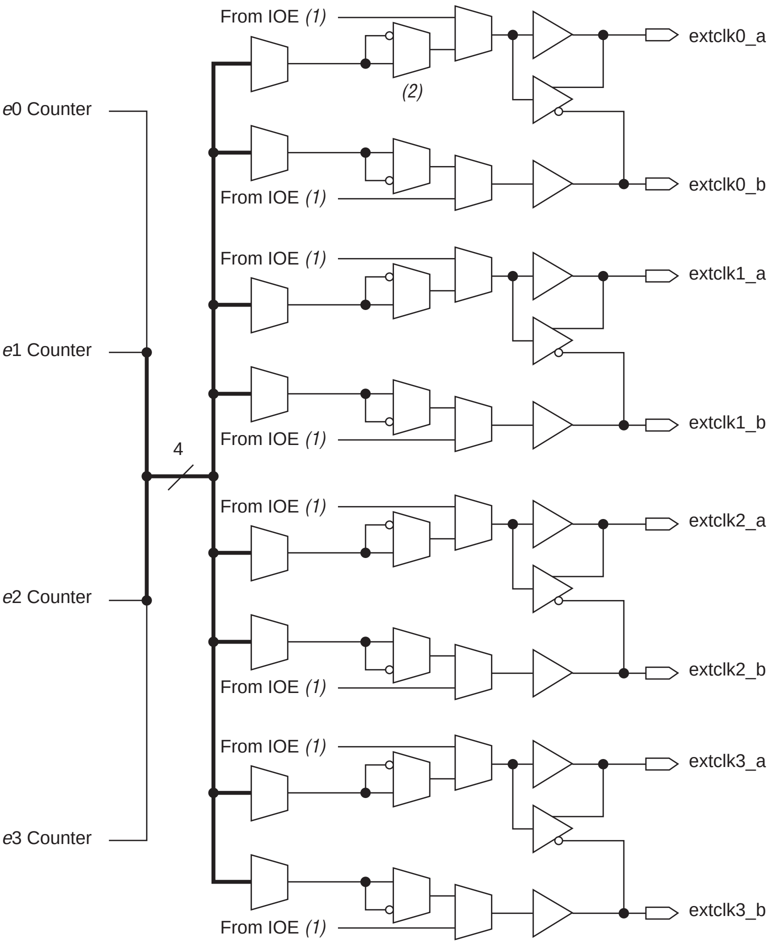
### *Programmable Bandwidth*

The designer has advanced control of the PLL bandwidth using the programmable control of the PLL loop characteristics, including loop filter and charge pump. The PLL's bandwidth is a measure of its ability to track the input clock and jitter. A high-bandwidth PLL can quickly lock onto a reference clock and react to any changes in the clock. It also will allow a wide band of input jitter spectrum to pass to the output. A low-bandwidth PLL will take longer to lock, but it will attenuate all high-frequency jitter components. The Quartus II software can adjust PLL characteristics to achieve the desired bandwidth. The programmable bandwidth is tuned by varying the charge pump current, loop filter resistor value, high frequency capacitor value, and *m* counter value. Designers can manually adjust these values if desired. Bandwidth is programmable from 200 kHz to 1.5 MHz.

### External Clock Outputs

Enhanced PLLs 5 and 6 each support up to eight single-ended clock outputs (or four differential pairs). See Figure 2–55.

*Figure 2–55. External Clock Outputs for PLLs 5 & 6*



*Notes to Figure 2–55:*

(1) The design can use each external clock output pin as a general-purpose output pin from the logic array. These pins are multiplexed with IOE outputs.

(2) Two single-ended outputs are possible per output counter—either two outputs of the same frequency and phase or one shifted 180°.

(3) EP1S10, EP1S20, and EP1S25 devices in 672-pin BGA and 484- and 672-pin FineLine BGA packages only have two pairs of external clocks (i.e., `pll_out0p`, `pll_out0n`, `pll_out1p`, and `pll_out1n`).

Any of the four external output counters can drive the single-ended or differential clock outputs for PLLs 5 and 6. This means one counter or frequency can drive all output pins available from PLL 5 or PLL 6. Each pair of output pins (four pins total) has dedicated `VCC` and `GND` pins to reduce the output clock's overall jitter by providing improved isolation from switching I/O pins.

For PLLs 5 and 6, each pin of a single-ended output pair can either be in phase or 180° out of phase. The clock output pin pairs support the same I/O standards as standard output pins (in the top and bottom banks) as well as LVDS, LVPECL, 3.3-V PCML, HyperTransport technology, differential HSTL, and differential SSTL. Table 2–21 shows which I/O standards the enhanced PLL clock pins support. When in single-ended or differential mode, the two outputs operate off the same power supply. Both outputs use the same standards in single-ended mode to maintain performance. Designers can also use the external clock output pins as user output pins if external enhanced PLL clocking is not needed.

*Table 2–21. I/O Standards Supported for Enhanced PLL Pins (Part 1 of 2)*

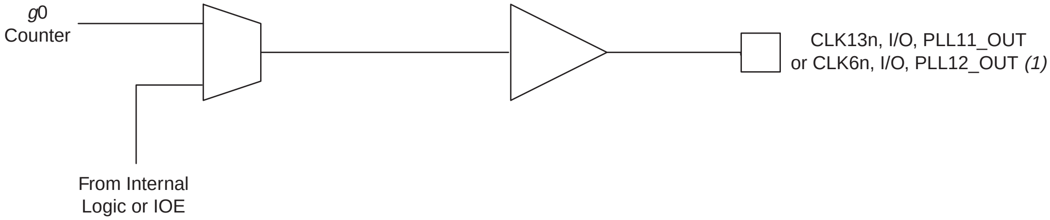
| I/O Standard | Input | | | Output |
|---|---|---|---|---|
| | INCLK | FBIN | PLLENABLE | EXTCLK |
| LVTTL | ✓ | ✓ | ✓ | ✓ |
| LVCMOS | ✓ | ✓ | ✓ | ✓ |
| 2.5 V | ✓ | ✓ | | ✓ |
| 1.8 V | ✓ | ✓ | | ✓ |
| 1.5 V | ✓ | ✓ | | ✓ |
| 3.3-V PCI | ✓ | ✓ | | ✓ |
| 3.3-V PCI-X 1.0 | ✓ | ✓ | | ✓ |
| LVPECL | ✓ | ✓ | | ✓ |
| 3.3-V PCML | ✓ | ✓ | | ✓ |
| LVDS | ✓ | ✓ | | ✓ |
| HyperTransport technology | ✓ | ✓ | | ✓ |
| Differential HSTL | ✓ | | | ✓ |
| Differential SSTL | | | | ✓ |
| 3.3-V GTL | ✓ | ✓ | | ✓ |
| 3.3-V GTL+ | ✓ | ✓ | | ✓ |
| 1.5-V HSTL class I | ✓ | ✓ | | ✓ |
| 1.5-V HSTL class II | ✓ | ✓ | | ✓ |
| 1.8-V HSTL class I | ✓ | ✓ | | ✓ |

*Table 2–21. I/O Standards Supported for Enhanced PLL Pins (Part 2 of 2)*

| I/O Standard | Input | | | Output |
|---|---|---|---|---|
| | INCLK | FBIN | PLLENABLE | EXTCLK |
| 1.8-V HSTL class II | ✓ | ✓ | | ✓ |
| SSTL-18 class I | ✓ | ✓ | | ✓ |
| SSTL-18 class II | ✓ | ✓ | | ✓ |
| SSTL-2 class I | ✓ | ✓ | | ✓ |
| SSTL-2 class II | ✓ | ✓ | | ✓ |
| SSTL-3 class I | ✓ | ✓ | | ✓ |
| SSTL-3 class II | ✓ | ✓ | | ✓ |
| AGP (1× and 2×) | ✓ | ✓ | | ✓ |
| CTT | ✓ | ✓ | | ✓ |

Enhanced PLLs 11 and 12 support one single-ended output each (see Figure 2–56). These outputs do not have their own `VCC` and `GND` signals. Therefore, to minimize jitter, do not place switching I/O pins next to this output pin.

*Figure 2–56. External Clock Outputs for Enhanced PLLs 11 & 12*



*Note to Figure 2–56:*

(1) For PLL 11, this pin is `CLK13n`; for PLL 12 this pin is `CLK7n`.

Stratix devices can drive any enhanced PLL driven through the global clock or regional clock network to any general I/O pin as an external output clock. The jitter on the output clock is not guaranteed for these cases.

### Clock Feedback

The following four feedback modes in Stratix device enhanced PLLs allow multiplication and/or phase and delay shifting:

- Zero delay buffer: The external clock output pin is phase-aligned with the clock input pin for zero delay.
- External feedback: The external feedback input pin, `FBIN`, is phase-aligned with the clock input, `CLK`, pin. Aligning these clocks allows the designer to remove clock delay and skew between devices. This mode is only possible for PLLs 5 and 6. PLLs 5 and 6 each support feedback for one of the dedicated external outputs, either one single-ended or one differential pair. In this mode, one *e* counter feeds back to the PLL `FBIN` input, becoming part of the feedback loop.
- Normal mode: If an internal clock is used in this mode, it is phase-aligned to the input clock pin. The external clock output pin will have a phase delay relative to the clock input pin if connected in this mode. The designer defines which internal clock output from the PLL should be phase-aligned to the internal clock pin.
- No compensation: In this mode, the PLL will not compensate for any clock networks or external clock outputs.

### *Phase & Delay Shifting*

Stratix device enhanced PLLs provide advanced programmable phase and clock delay shifting. These parameters are set in the Quartus II software.

#### Phase Delay

The Quartus II software automatically sets the phase taps and counter settings according to the phase shift entry. The designer enters a desired phase shift and the Quartus II software automatically sets the closest setting achievable. This type of phase shift is not reconfigurable during system operation. For phase shifting, enter a phase shift (in degrees or time units) for each PLL clock output port or for all outputs together in one shift. Designers can select phase-shifting values in time units with a resolution of 156.25 to 416.66 ps. This resolution is a function of frequency input and the multiplication and division factors (i.e., it is a function of the VCO period), with the finest step being equal to an eighth (×0.125) of the VCO period. Each clock output counter can choose a different phase of the VCO period from up to eight taps for individual fine step selection. Also, each clock output counter can use a unique initial count setting to achieve individual coarse shift selection in steps of one VCO period. The combination of coarse and fine shifts allows phase shifting for the entire input clock period.

The equation to determine the precision of the phase shifting in degrees is: 45° ÷ post-scale counter value. Therefore, the maximum step size is 45°, and smaller steps are possible depending on the multiplication and division ratio necessary on the output counter port.

This type of phase shift provides the highest precision since it is the least sensitive to process, supply, and temperature variation.

### Clock Delay

In addition to the phase shift feature, the ability to fine tune the Δt clock delay provides advanced time delay shift control on each of the four PLL outputs. There are time delays for each post-scale counter (*e*, *g*, or *l*) from the PLL, the *n* counter, and *m* counter. Each of these can shift in 250-ps increments for a range of 3.0 ns. The *m* delay shifts all outputs earlier in time, while *n* delay shifts all outputs later in time. Individual delays on post-scale counters (*e*, *g*, and *l*) provide positive delay for each output. Table 2–22 shows the combined delay for each output for normal or zero delay buffer mode where $\Delta t_e$, $\Delta t_g$, or $\Delta t_l$ is unique for each PLL output.

The $t_{OUTPUT}$ for a single output can range from –3 ns to +6 ns. The total delay shift difference between any two PLL outputs, however, must be less than ±3 ns. For example, shifts on two outputs of –1 and +2 ns is allowed, but not –1 and +2.5 ns because these shifts would result in a difference of 3.5 ns. If the design uses external feedback, the $\Delta t_e$ delay will remove delay from outputs, represented by a negative sign (see Table 2–22). This effect occurs because the $\Delta t_e$ delay is then part of the feedback loop.

Table 2–22. Output Clock Delay for Enhanced PLLs

| Normal or Zero Delay Buffer Mode | External Feedback Mode |
|---|---|
| $\Delta t_{eOUTPUT} = \Delta t_n - \Delta t_m + \Delta t_e$<br>$\Delta t_{gOUTPUT} = \Delta t_n - \Delta t_m + \Delta t_g$<br>$\Delta t_{lOUTPUT} = \Delta t_n - \Delta t_m + \Delta t_l$ | $\Delta t_{eOUTPUT} = \Delta t_n - \Delta t_m - \Delta t_e$ (1)<br>$\Delta t_{gOUTPUT} = \Delta t_n - \Delta t_m + \Delta t_g$<br>$\Delta t_{lOUTPUT} = \Delta t_n - \Delta t_m + \Delta t_l$ |

*Note to Table 2–22:*

(1) $\Delta t_e$ removes delay from outputs in external feedback mode.

The variation due to process, voltage, and temperature is about ±15% on the delay settings. PLL reconfiguration can control the clock delay shift elements, but not the VCO phase shift multiplexers, during system operation.

### Spread-Spectrum Clocking

Stratix device enhanced PLLs use spread-spectrum technology to reduce electromagnetic interference generation from a system by distributing the energy over a broader frequency range. The enhanced PLL typically provides 0.5% down spread modulation using a triangular profile. The modulation frequency is programmable. Enabling spread-spectrum for a PLL affects all of its outputs.

### Lock Detect

The lock output indicates that there is a stable clock output signal in phase with the reference clock. The locked port can drive the logic array or an output pin.

If the input clock stops and causes the PLL to lose lock, then the PLL must be reset for correct phase shift operation.

See the *Stratix FPGA Errata Sheet* for more information on implementing the gated lock signal in your design.

### Programmable Duty Cycle

The programmable duty cycle allows enhanced PLLs to generate clock outputs with a variable duty cycle. This feature is supported on each enhanced PLL post-scale counter (*g*0..*g*3, *l*0..*l*3, *e*0..*e*3). The duty cycle setting is achieved by a low and high time count setting for the post-scale dividers. The Quartus II software uses the frequency input and the required multiply or divide rate to determine the duty cycle choices.

### Advanced Clear & Enable Control

There are several control signals for clearing and enabling PLLs and their outputs. The designer can use these signals to control PLL resynchronization and gate PLL output clocks for low-power applications.

The `pllenable` pin is a dedicated pin that enables/disables PLLs. When the `pllenable` pin is low, the clock output ports are driven by `GND` and all the PLLs go out of lock. When the `pllenable` pin goes high again, the PLLs relock and resynchronize to the input clocks. The designer can choose which PLLs are controlled by the `pllenable` signal by connecting the `pllenable` input port of the `altpll` megafunction to the common `pllenable` input pin.

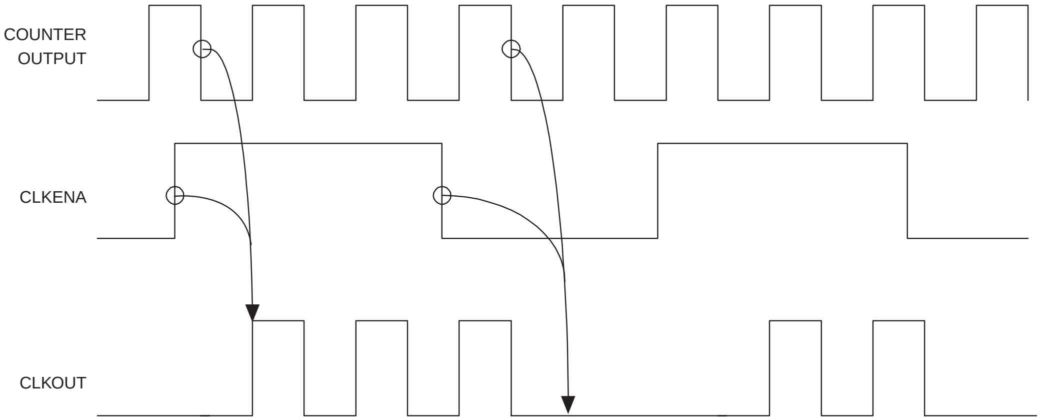
The `areset` signals are reset/resynchronization inputs for each PLL. The device input pins or logic elements (LEs) can drive these input signals. When driven high, the PLL counters will reset, clearing the PLL output and placing the PLL out of lock. The VCO will set back to its nominal setting (~700 MHz). When driven low again, the PLL will resynchronize to its input as it relocks. If the target VCO frequency is below this nominal frequency, then the output frequency will start at a higher value than desired as the PLL locks. If the system cannot tolerate this, the `clkena` signal can disable the output clocks until the PLL locks.

The `pfdena` signals control the phase frequency detector (PFD) output with a programmable gate. If the designer disables the PFD, the VCO will operate at its last set value of control voltage and frequency with some long-term drift to a lower frequency. The system will continue running when the PLL goes out of lock or the input clock is disabled. By maintaining the last locked frequency, the system has time to store its current settings before shutting down. Designers can either use their own control signal or `clkloss` or gated `locked` status signals to trigger `pdfena`.

The `clkena` signals control the enhanced PLL regional and global outputs. Each regional and global output port has its own `clkena` signal. The `clkena` signals synchronously disable or enable the clock at the PLL output port by gating the outputs of the *g* and *l* counters. The `clkena` signals are registered on the falling edge of the counter output clock to enable or disable the clock without glitches. Figure 2–57 shows the waveform example for a PLL clock port enable. The PLL can remain locked independent of the `clkena` signals since the loop-related counters are not affected. This feature is useful for applications that require a low power or sleep mode. Upon re-enabling, the PLL does not need a resynchronization or relock period. The `clkena` signal can also disable clock outputs if the system is not tolerant to frequency overshoot during resynchronization.

The `extclkena` signals work in the same way as the `clkena` signals, but they control the external clock output counters (*e*0, *e*1, *e*2, and *e*3). Upon re-enabling, the PLL does not need a resynchronization or relock period unless the PLL is using external feedback mode. In order to lock in external feedback mode, the external output must drive the board trace back to the `FBIN` pin.

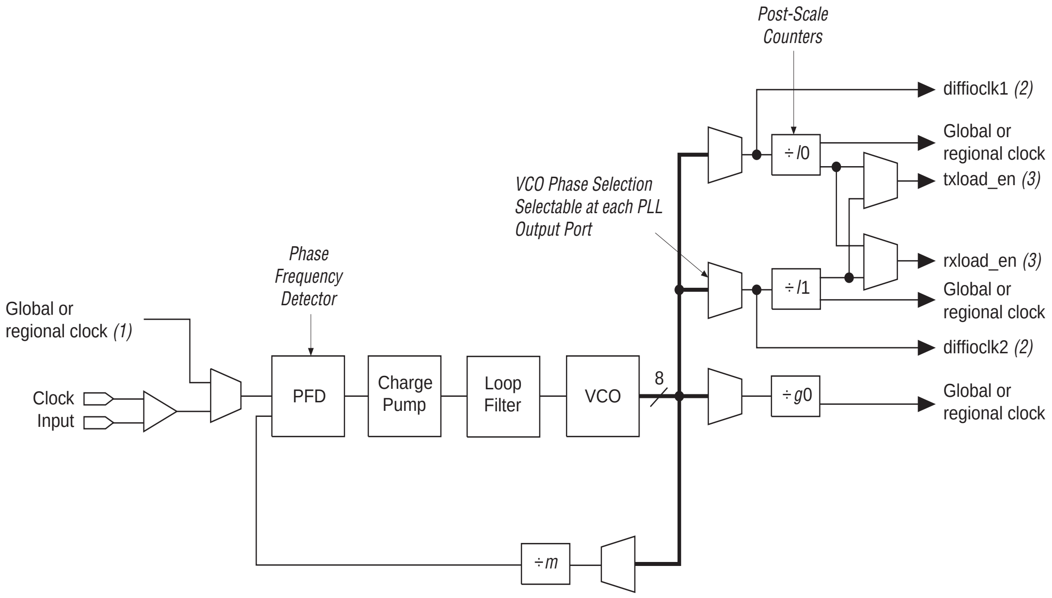
*Figure 2–57. extclkena Signals*



## Fast PLLs

Stratix devices contain up to eight fast PLLs with high-speed serial interfacing ability, along with general-purpose features. Figure 2–58 shows a diagram of the fast PLL.

*Figure 2–58. Stratix Device Fast PLL*



*Notes to Figure 2–58:*

(1) The global or regional clock input can be driven by an output from another PLL or a pin-driven global or regional clock. It cannot be driven by internally-generated global signals.

(2) In high-speed differential I/O support mode, this high-speed PLL clock feeds the SERDES. Stratix devices only support one rate of data transfer per fast PLL in high-speed differential I/O support mode.

(3) This signal is a high-speed differential I/O support SERDES control signal.

### Clock Multiplication & Division

Stratix device enhanced PLLs provide clock synthesis for PLL output ports using $m$/(post scaler) scaling factors. The input clock is multiplied by the $m$ feedback factor. Each output port has a unique post scale counter to divide down the high-frequency VCO. There is one multiply divider, $m$, per fast PLL with a range of 1 to 32. There are two post scale L dividers for regional and/or LVDS interface clocks, and $g0$ counter for global clock output port; all range from 1 to 32.

In the case of a high-speed differential interface, the designer can set the output counter to 1 to allow the high-speed VCO frequency to drive the SERDES.

### *External Clock Inputs*

Each fast PLL supports single-ended or differential inputs for source synchronous transmitters or for general-purpose use. Source-synchronous receivers support differential clock inputs. The fast PLL inputs are fed by `CLK[0..3]`, `CLK[8..11]`, and `FPLL[7..10]CLK` pins, as shown in Figure 2–50 on page 2–82.

Table 2–23 shows the I/O standards supported by fast PLL input pins.

***Table 2–23. Fast PLL Port I/O Standards (Part 1 of 2)***

| I/O Standard | Input | |
|---|---|---|
| | INCLK | PLLENABLE |
| LVTTL | ✓ | ✓ |
| LVCMOS | ✓ | ✓ |
| 2.5 V | ✓ | |
| 1.8 V | ✓ | |
| 1.5 V | ✓ | |
| 3.3-V PCI | | |
| 3.3-V PCI-X 1.0 | | |
| LVPECL | ✓ | |
| 3.3-V PCML | ✓ | |
| LVDS | ✓ | |
| HyperTransport technology | ✓ | |
| Differential HSTL | | |
| Differential SSTL | | |
| 3.3-V GTL | ✓ | |
| 3.3-V GTL+ | ✓ | |
| 1.5-V HSTL class I | ✓ | |
| 1.5-V HSTL class II | ✓ | |
| 1.8-V HSTL class I | ✓ | |
| 1.8-V HSTL class II | ✓ | |
| SSTL-18 class I | ✓ | |
| SSTL-18 class II | ✓ | |
| SSTL-2 class I | ✓ | |

*Table 2–23. Fast PLL Port I/O Standards (Part 2 of 2)*

| I/O Standard | Input | |
|---|---|---|
| | INCLK | PLLENABLE |
| SSTL-2 class II | ✓ | |
| SSTL-3 class I | ✓ | |
| SSTL-3 class II | ✓ | |
| AGP (1× and 2×) | ✓ | |
| CTT | ✓ | |

Table 2–24 shows the performance on each of the fast PLL clock inputs when using LVDS, LVPECL, 3.3-V PCML, or HyperTransport technology.

*Table 2–24. LVDS Performance on Fast PLL Input*

| Fast PLL Clock Input | Maximum Input Frequency (MHz) |
|---|---|
| CLK0, CLK2, CLK9, CLK11, FPLL7CLK, FPLL8CLK, FPLL9CLK, FPLL10CLK | 717 *(1)* |
| CLK1, CLK3, CLK8, CLK10 | 462 |

*Note to Table 2–24:*

(1) HyperTransport technology supports 400-MHz input frequency. See "Maximum Input & Output Clock Rates" on page 4–63

### External Clock Outputs

Each fast PLL supports differential or single-ended outputs for source-synchronous transmitters or for general-purpose external clocks. There are no dedicated external clock output pins. Any I/O pin can be driven by the fast PLL global or regional outputs as an external output pin. The I/O standards supported by any particular bank determines what standards are possible for an external clock output driven by the fast PLL in that bank.

### Phase Shifting

Stratix device fast PLLs have advanced clock shift capability that enables programmable phase shifts. Designers can enter a phase shift (in degrees or time units) for each PLL clock output port or for all outputs together in one shift. Designers can perform phase shifting in time units with a resolution range of 125 to 416.66 ps. This resolution is a function of the VCO period, with the finest step being equal to an eighth (×0.125) of the VCO period.

### *Control Signals*

The fast PLL has the same `lock` output, `pllenable` input, and `areset` input control signals as the enhanced PLL.

If the input clock stops and causes the PLL to lose lock, then the PLL must be reset for correct phase shift operation.

For more information on high-speed differential I/O support, see "High-Speed Differential I/O Support" on page 2–137.

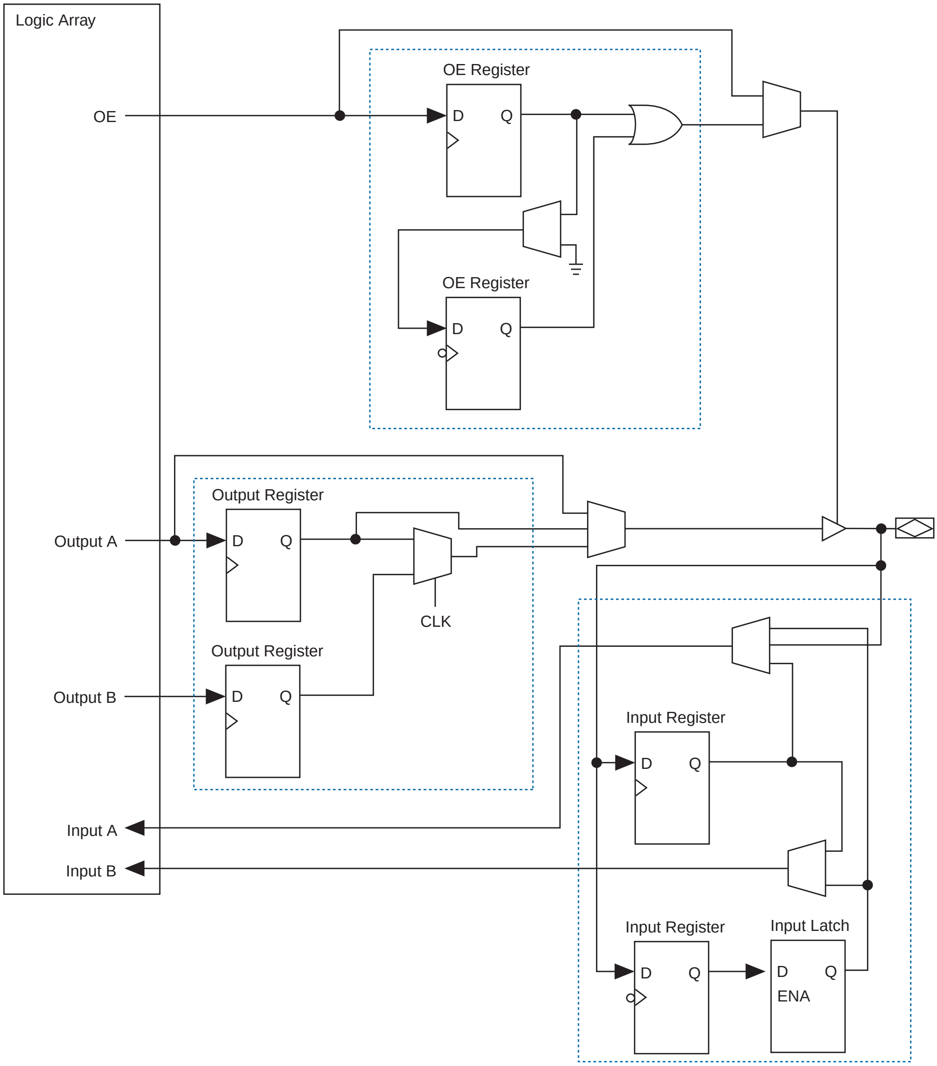
## I/O Structure

IOEs provide many features, including:

- Dedicated differential and single-ended I/O buffers
- 3.3-V, 64-bit, 66-MHz PCI compliance
- 3.3-V, 64-bit, 133-MHz PCI-X 1.0 compliance
- Joint Test Action Group (JTAG) boundary-scan test (BST) support
- Driver impedance matching
- On-chip termination for differential and single-ended standards
- Programmable pull-up during configuration
- Output drive strength control
- Slew-rate control
- Tri-state buffers
- Bus-hold circuitry
- Programmable pull-up resistors
- Programmable input and output delays
- Open-drain outputs
- DQ and DQS I/O pins

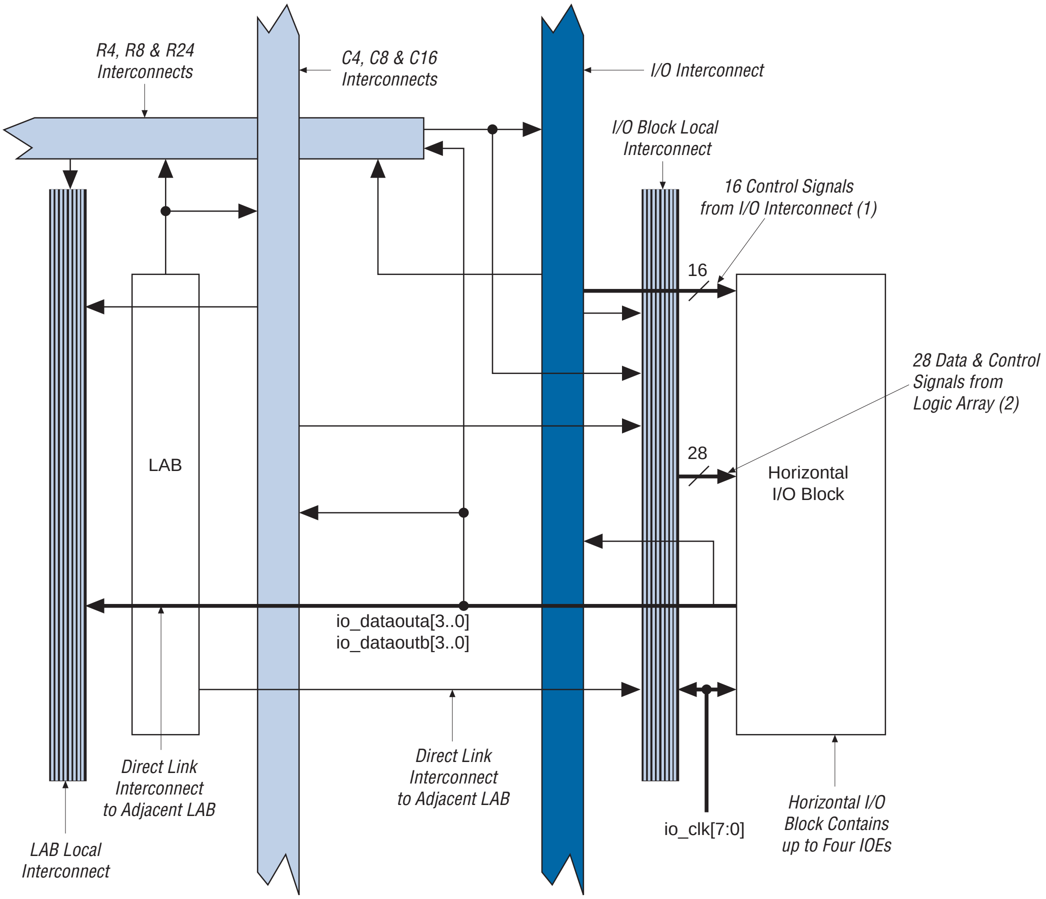
The IOE in Stratix devices contains a bidirectional I/O buffer, six registers, and a latch for a complete embedded bidirectional single data rate or DDR transfer. Figure 2–59 shows the Stratix IOE structure. The IOE contains two input registers (plus a latch), two output registers, and two output enable registers. The design can use both input registers and the latch to capture DDR input and both output registers to drive DDR outputs. Additionally, the design can use the output enable (OE) register for fast clock-to-output enable timing. The negative edge-clocked OE register is used for DDR SDRAM interfacing. The Quartus II software automatically duplicates a single OE register that controls multiple output or bidirectional pins.

*Figure 2–59. Stratix IOE Structure*



The IOEs are located in I/O blocks around the periphery of the Stratix device. There are up to four IOEs per row I/O block and six IOEs per column I/O block. The row I/O blocks drive row, column, or direct link interconnects. The column I/O blocks drive column interconnects. Figure 2–60 shows how a row I/O block connects to the logic array. Figure 2–61 shows how a column I/O block connects to the logic array.

*Figure 2–60. Row I/O Block Connection to the Interconnect*

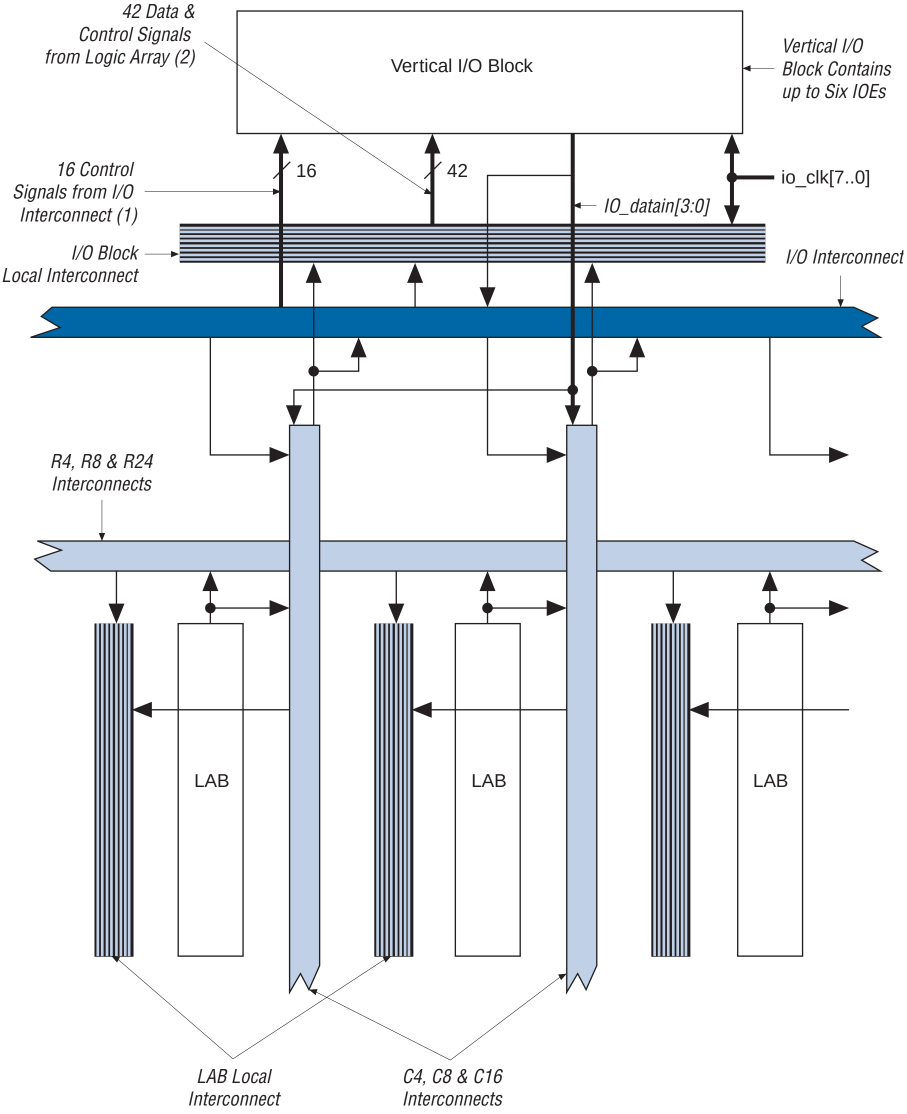


*Notes to Figure 2–60:*

(1) The 16 control signals are composed of four output enables `io_boe[3..0]`, four clock enables `io_bce[3..0]`, four clocks `io_clk[3..0]`, and four clear signals `io_bclr[3..0]`.

(2) The 28 data and control signals consist of eight data out lines: four lines each for DDR applications `io_dataouta[3..0]` and `io_dataoutb[3..0]`, four output enables `io_coe[3..0]`, four input clock enables `io_cce_in[3..0]`, four output clock enables `io_cce_out[3..0]`, four clocks `io_cclk[3..0]`, and four clear signals `io_cclr[3..0]`.

*Figure 2–61. Column I/O Block Connection to the Interconnect*



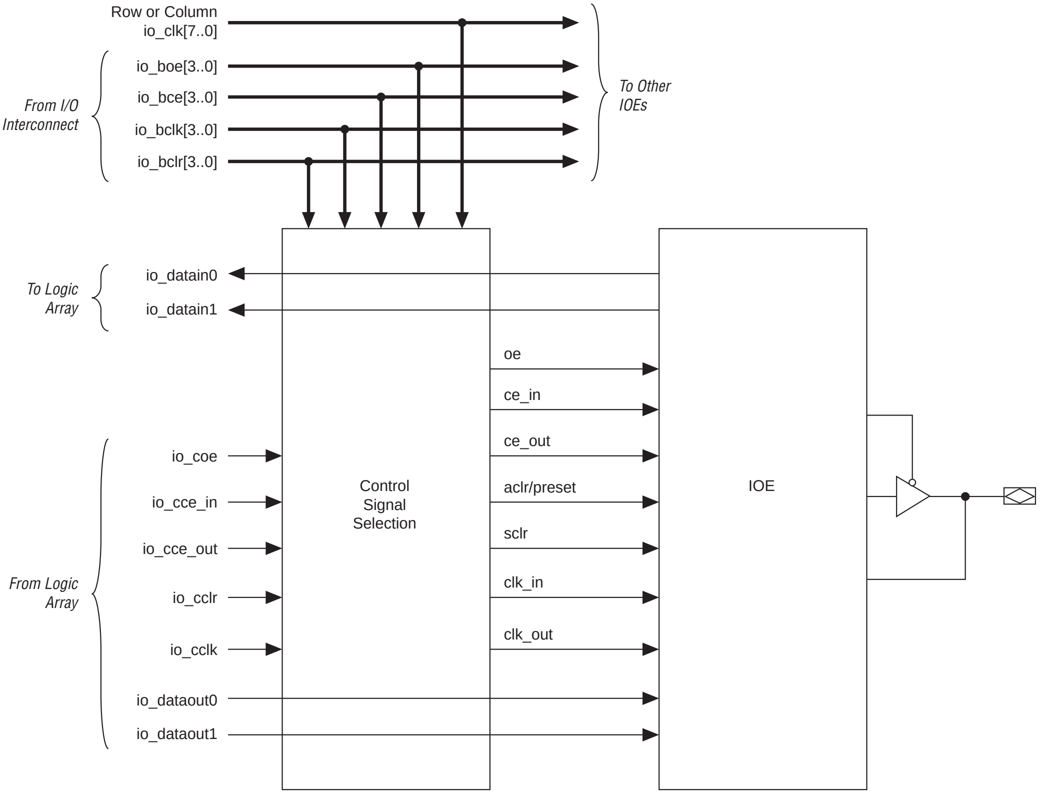
*Notes to Figure 2–61:*

(1) The 16 control signals are composed of four output enables `io_boe[3..0]`, four clock enables `io_bce[3..0]`, four clocks `io_bclk[3..0]`, and four clear signals `io_bclr[3..0]`.

(2) The 42 data and control signals consist of 12 data out lines; six lines each for DDR applications `io_dataouta[5..0]` and `io_dataoutb[5..0]`, six output enables `io_coe[5..0]`, six input clock enables `io_cce_in[5..0]`, six output clock enables `io_cce_out[5..0]`, six clocks `io_cclk[5..0]`, and six clear signals `io_cclr[5..0]`.

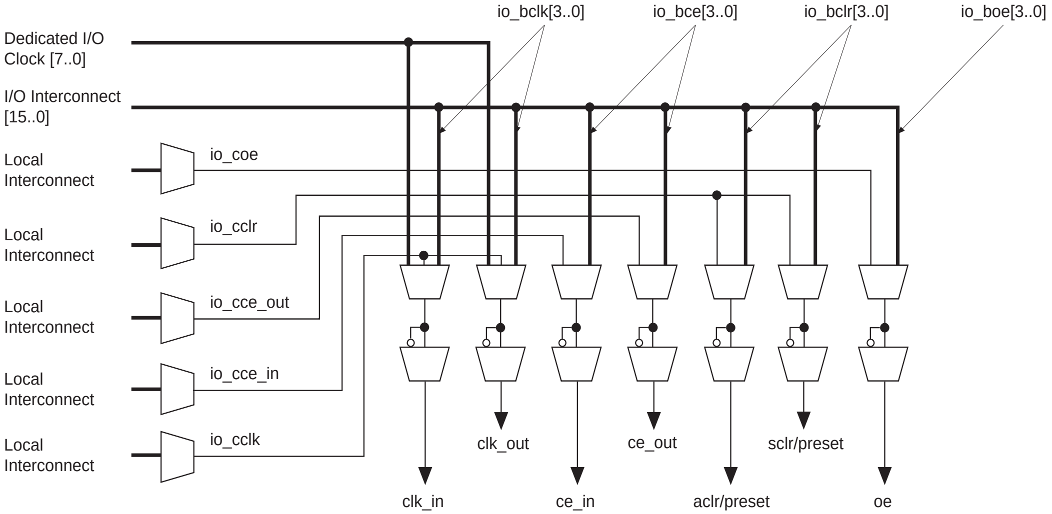
Stratix devices have an I/O interconnect similar to the R4 and C4 interconnect to drive high-fanout signals to and from the I/O blocks. There are 16 signals that drive into the I/O blocks composed of four output enables `io_boe[3..0]`, four clock enables `io_bce[3..0]`, four clocks `io_bclk[3..0]`, and four clear signals `io_bclr[3..0]`. The pin's `datain` signals can drive the IO interconnect, which in turn drives the logic array or other I/O blocks. In addition, the control and data signals can be driven from the logic array, providing a slower but more flexible routing resource. The row or column IOE clocks, `io_clk[7..0]`, provide a dedicated routing resource for low-skew, high-speed clocks. I/O clocks are generated from regional, global, or fast regional clocks (see "PLLs & Clock Networks" on page 2–71). Figure 2–62 illustrates the signal paths through the I/O block.

***Figure 2–62. Signal Path through the I/O Block***



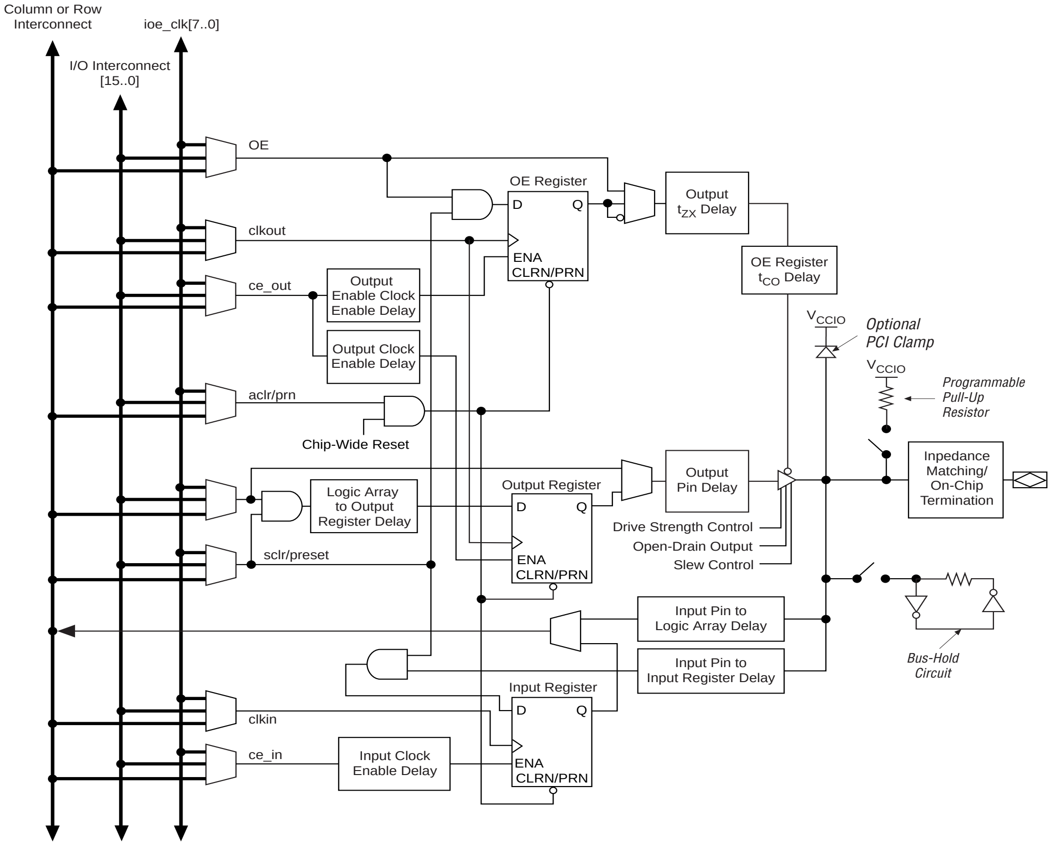
Each IOE contains its own control signal selection for the following control signals: `oe`, `ce_in`, `ce_out`, `aclr/preset`, `sclr/preset`, `clk_in`, and `clk_out`. Figure 2–63 illustrates the control signal selection.

*Figure 2–63. Control Signal Selection per IOE*



In normal bidirectional operation, the input register can be used for input data requiring fast setup times. The input register can have its own clock input and clock enable separate from the OE and output registers. The output register can be used for data requiring fast clock-to-output performance. The OE register can be used for fast clock-to-output enable timing. The OE and output register share the same clock source and the same clock enable source from local interconnect in the associated LAB, dedicated I/O clocks, and the column and row interconnects. Figure 2–64 shows the IOE in bidirectional configuration.

**Figure 2–64. Stratix IOE in Bidirectional I/O Configuration** Note (1)



*Note to Figure 2–64:*

(1) All input signals to the IOE can be inverted at the IOE.

The Stratix device IOE includes programmable delays that can be activated to ensure zero hold times, input IOE register-to-logic array register transfers, or logic array-to-output IOE register transfers.

A path in which a pin directly drives a register may require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinatorial logic may not require the delay. Programmable delays exist for decreasing input-pin-to-logic-array and IOE input register delays. The Quartus II Compiler can program these delays to automatically minimize setup time while providing a zero hold time. Programmable delays can increase the register-to-pin delays for output and/or output enable registers. A programmable delay exists to increase the $t_{ZX}$ delay to the output pin, which is required for ZBT interfaces. Table 2–25 shows the programmable delays for Stratix devices.

*Table 2–25. Stratix Programmable Delay Chain*

| Programmable Delays | Quartus II Logic Option |
|---|---|
| Input pin to logic array delay | Decrease input delay to internal cells |
| Input pin to input register delay | Decrease input delay to input register |
| Output pin delay | Increase delay to output pin |
| Output enable register $t_{CO}$ delay | Increase delay to output enable pin |
| Output $t_{ZX}$ delay | Increase $t_{ZX}$ delay to output pin |
| Output clock enable delay | Increase output clock enable delay |
| Input clock enable delay | Increase input clock enable delay |
| Logic array to output register delay | Decrease input delay to output register |
| Output enable clock enable delay | Increase output enable clock enable delay |

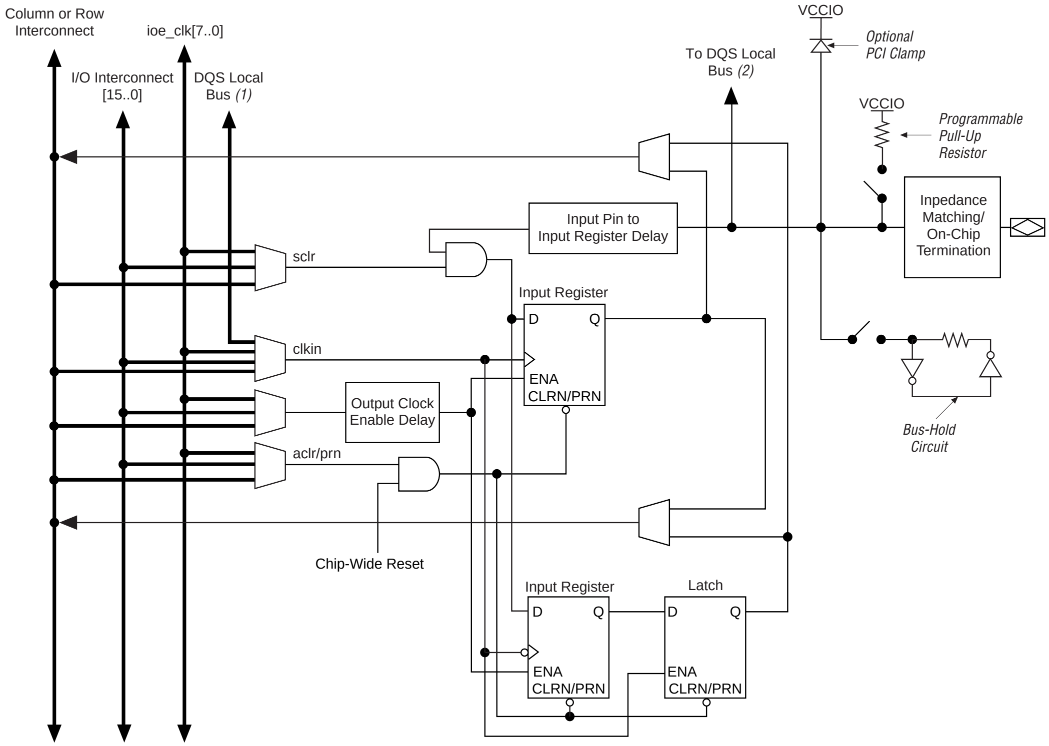
The IOE registers in Stratix devices share the same source for clear or preset. The designer can program preset or clear for each individual IOE. The designer can also program the registers to power up high or low after configuration is complete. If programmed to power up low, an asynchronous clear can control the registers. If programmed to power up high, an asynchronous preset can control the registers. This feature prevents the inadvertent activation of another device’s active-low input upon power-up. If one register in an IOE uses a preset or clear signal then all registers in the IOE must use that same signal if they require preset or clear. Additionally a synchronous reset signal is available to the designer for the IOE registers.

## Double-Data Rate I/O Pins

Stratix devices have six registers in the IOE, which support DDR interfacing by clocking data on both positive and negative clock edges. The IOEs in Stratix devices support DDR inputs, DDR outputs, and bidirectional DDR modes.

When using the IOE for DDR inputs, the two input registers clock double rate input data on alternating edges. An input latch is also used within the IOE for DDR input acquisition. The latch holds the data that is present during the clock high times. This allows both bits of data to be synchronous with the same clock edge (either rising or falling). Figure 2–65 shows an IOE configured for DDR input.

*Figure 2–65. Stratix IOE in DDR Input I/O Configuration* *Note (1)*



*Notes to Figure 2–65:*

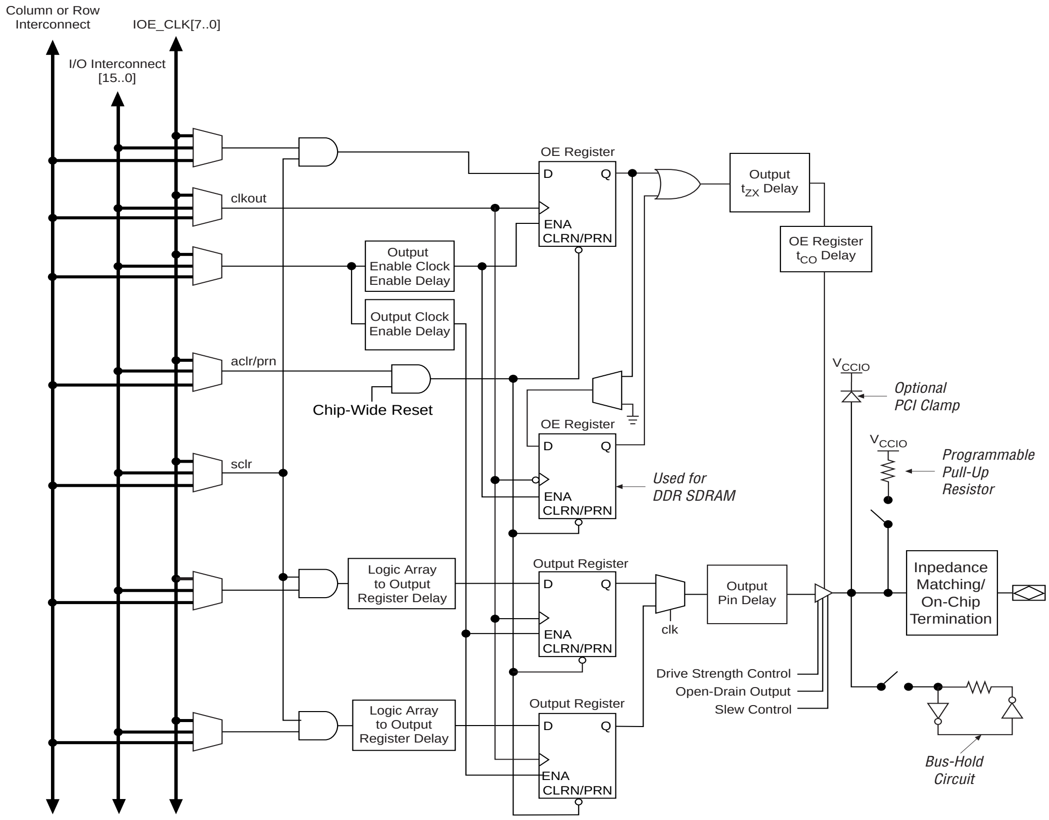
(1) All input signals to the IOE can be inverted at the IOE.

(2) This signal connection is only allowed on dedicated DQ function pins.

(3) This signal is for dedicated DQS function pins only.

When using the IOE for DDR outputs, the two output registers are configured to clock two data paths from LEs on rising clock edges. These output registers are multiplexed by the clock to drive the output pin at a ×2 rate. One output register clocks the first bit out on the clock high time, while the other output register clocks the second bit out on the clock low time. Figure 2–66 shows the IOE configured for DDR output.

**Figure 2–66. Stratix IOE in DDR Output I/O Configuration** *Note (1)*



*Note to Figure 2–66:*

(1) All input signals to the IOE can be inverted at the IOE.

The Stratix IOE operates in bidirectional DDR mode by combining the DDR input and DDR output configurations. Stratix device I/O pins transfer data on a DDR bidirectional bus to support DDR SDRAM. The negative-edge-clocked OE register holds the OE signal inactive until the falling edge of the clock. This is done to meet DDR SDRAM timing requirements.

## External RAM Interfacing

Stratix devices support DDR SDRAM and fast cycle RAM (FCRAM) at up to 200 MHz through dedicated phase-shift circuitry, QDR and QDRII SRAM interfaces up to 167 MHz, and ZBT SRAM interfaces at up to

200 MHz. Stratix devices also provide preliminary support for reduced latency DRAM at rates up to 250 MHz through the dedicated phase-shift circuitry.

☞ In addition to the required signals for external memory interfacing, Stratix devices offer the optional clock enable signal. When the clock enable signal is used, the output register updates with new values. The output registers hold their old values when the clock enable signal is disabled.

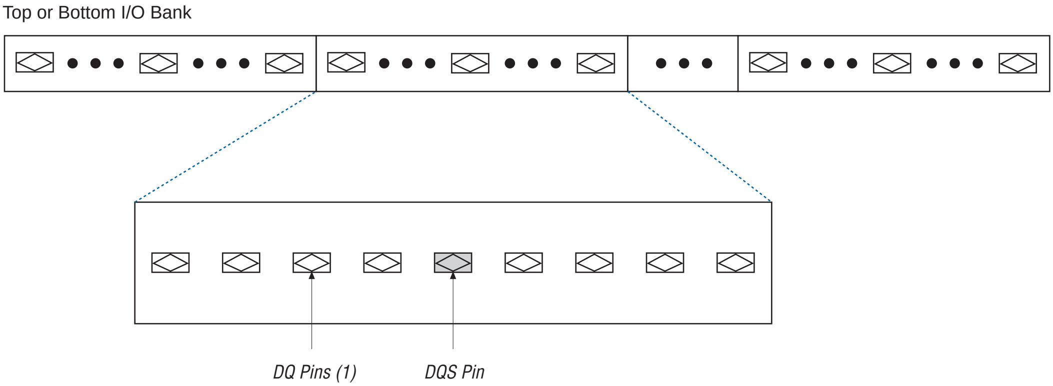
To find out more about the DDR SDRAM specification, see the JEDEC web site (www.jedec.org). For information on memory controller megafunctions for Stratix devices, see the Altera web site (www.altera.com).

### DDR SDRAM & FCRAM

In addition to six I/O registers in the IOE for interfacing to these high-speed memory interfaces, Stratix devices also have dedicated circuitry for interfacing with DDR SDRAM and FCRAM. In every Stratix device, the I/O banks at the top (I/O banks 3 and 4) and bottom (I/O banks 7 and 8) of the device support DDR SDRAM and FCRAM I/O pins. These pins support DQS signals with DQ bus modes of ×8, ×16, or ×32.

For ×8 mode, there are up to 20 groups of programmable DQS and DQ pins—10 groups in I/O banks 3 and 4 and 10 groups in I/O banks 7 and 8. The EP1S10 device supports up to 16 groups total. See Table 2–26. Each group consists of one DQS pin and a set of eight DQ pins (see Figure 2–67). Each DQS pin drives the set of eight DQ pins within that group.

*Figure 2–67. Stratix Device DQ & DQS Groups in ×8 Mode*



*Note to Figure 2–67:*

(1) There are at least eight `DQ` pins per group. Some devices may have more.

For ×16 mode, there are up to eight groups of programmable DQS and DQ pins—four groups in I/O banks 3 and 4, and four groups in I/O banks 7 and 8. The EP1S20 device supports seven ×16 groups. The EP1S10 device does not support ×16 mode. All other devices support the full eight groups. See Table 2–26. Each group consists of one DQS and 16 DQ pins. In ×16 mode, `DQST1`, `DQST3`, `DQST6`, and `DQST8` pins on the top side of the device, and `DQSB1`, `DQSB3`, `DQSB6`, and `DQSB8` pins on the bottom side of the device are dedicated DQS pins. The `DQST2`, `DQST7`, `DQSB2`, and `DQSB7` pins are dedicated DQS pins for ×32 mode. You can use any of the column I/O pins for the DM signals.

☞ If the Stratix device interfaces with a x16 memory device that uses two DQS pins and each DQS pin drives eight DQ pins, the Stratix device must use two sets of x8 groups. Similarly, if the Stratix device interfaces with a x32 memory device that uses four DQS pins and each DQS pin drives eight DQ pins, the Stratix device must use four sets of the x8 groups. The Stratix device's x16 mode means that there is one DQS pin for 16 DQ pins and the Stratix device's x32 mode means that there is only one DQS pin driving all 32 DQ pins..

A compensated delay element on each DQS pin allows for either a 90° (for DDR SDRAM) or a 72° (for FCRAM) phase shift, which automatically aligns input DQS synchronization signals with the data window of their corresponding DQ data signals. The DQS signals drive a local DQS bus within the top and bottom I/O banks. This DQS bus is an additional resource to the I/O clocks and is used to clock DQ input registers with the DQS signal.

*Table 2–26. DQS & DQ Bus Mode Support Note (1)*

| Device | Package | Number of ×8 Groups | Number of ×16 Groups | Number of ×32 Groups |
|---|---|---|---|---|
| EP1S10 | 672-pin BGA<br>672-pin FineLine BGA | 12 *(2)* | 0 | 0 |
| | 484-pin FineLine BGA<br>780-pin FineLine BGA | 16 *(3)* | 0 | 4 |
| EP1S20 | 484-pin FineLine BGA | 18 *(4)* | 7 | 4 |
| | 672-pin BGA<br>672-pin FineLine BGA | 16 *(3)* | 7 *(5)* | 4 |
| | 780-pin FineLine BGA | 20 | 7 *(5)* | 4 |
| EP1S25 | 672-pin BGA<br>672-pin FineLine BGA | 16 *(3)* | 8 | 4 |
| | 780-pin FineLine BGA<br>1,020-pin FineLine BGA | 20 | 8 | 4 |
| EP1S30 | 956-pin BGA<br>780-pin FineLine BGA<br>1,020-pin FineLine BGA | 20 | 8 | 4 |
| EP1S40 | 956-pin BGA<br>1,020-pin FineLine BGA<br>1,508-pin FineLine BGA | 20 | 8 | 4 |
| EP1S60 | 956-pin BGA<br>1,020-pin FineLine BGA<br>1,508-pin FineLine BGA | 20 | 8 | 4 |
| EP1S80 | 956-pin BGA<br>1,508-pin FineLine BGA<br>1,923-pin FineLine BGA | 20 | 8 | 4 |

***Notes to Table 2–26:***

(1) See Chapter 4, Using Selectable I/O Standards in Stratix & Stratix GX Devices of the *Stratix Device Handbook, Volume 2* for $V_{REF}$ guidelines.

(2) These packages have six groups in I/O banks 3 and 4 and six groups in I/O banks 7 and 8.

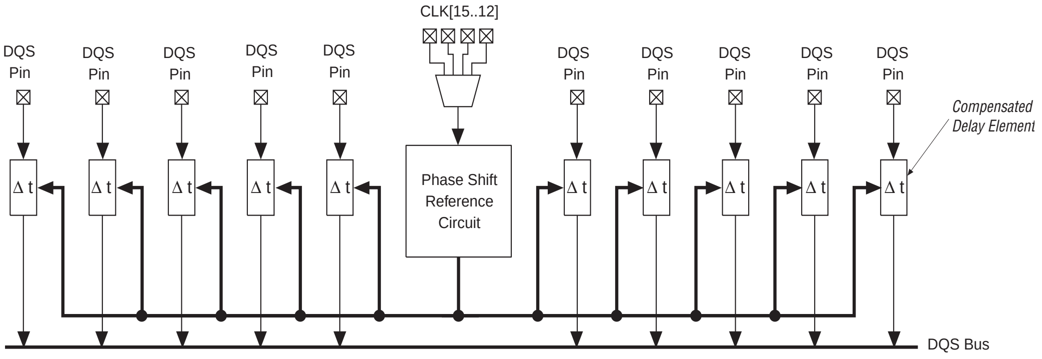
(3) These packages have eight groups in I/O banks 3 and 4 and eight groups in I/O banks 7 and 8.

(4) This package has nine groups in I/O banks 3 and 4 and nine groups in I/O banks 7 and 8.

(5) These packages have three groups in I/O banks 3 and 4 and four groups in I/O banks 7 and 8.

A single phase shifting reference circuit is located on the top and bottom of the Stratix device. This circuit is driven by a system reference clock through the `CLK` pins that is the same frequency as the DQS signal. Clock pins `CLK12p` to `CLK15p` feed the phase circuitry on the top of the device and clock pins `CLK4p` to `CLK7p` feed the phase circuitry on the bottom of the device. The phase shifting reference circuit on the top of the device controls the compensated delay elements for all ten DQS pins located at the top of the device. The phase shifting reference circuit on the bottom of the device controls the compensated delay elements for all ten DQS pins located on the bottom of the device. All ten delay elements (DQS signals) on either the top or bottom of the device shift by the same degree amount. For example, all ten DQS pins on the top of the device can be shifted by 90° and all ten DQS pins on the bottom of the device can be shifted by 72°. The reference circuit requires a maximum of 256 system reference clock cycles to set the correct phase on the DQS delay elements. Figure 2–68 illustrates the phase shift reference circuit control of each DQS delay shift on the top of the device. This same circuit is duplicated on the bottom of the device.

***Figure 2–68. Phase Shift Reference Circuit Control of DQS Delay***



*Note to Figure 2–68:*

(1) This circuit is repeated on the bottom of the device with the `CLK[4..7]` pins as possible inputs to the reference circuit.

These dedicated circuits combined with enhanced PLL clocking and phase shift ability provide a complete hardware solution for interfacing to high-speed memory.

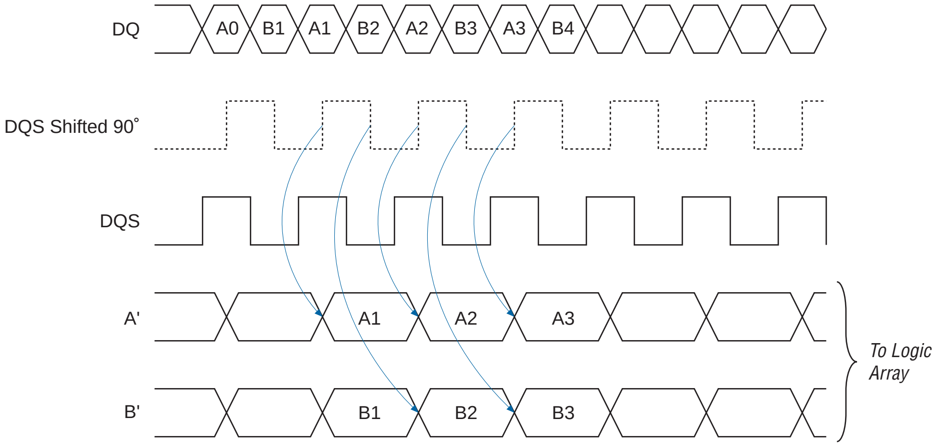
When reading from the DDR SDRAM or FCRAM, the DQS signal coming into the Stratix device is edge-aligned with the DQ pins. The dedicated circuitry center-aligns the DQS signal with respect to the DQ signals and the shifted DQS bus drives the clock input of the DDR input registers. The DDR input registers bring the data from the DQ signals to the device. The system clock is used to clock the DQS output enable and output paths. The –90° shifted clock is used to clock the DQ output enable and output paths. See Chapter 8, Double Data Rate I/O Signaling in Stratix & Stratix GX Devices of the *Stratix Device Handbook, Volume 2*. To meet 200 MHz performance for DDR SDRAM and FCRAM interfaces the following guidelines should be used:

- The number of DQ pins on each side of an associated DQS pin must be the same
- Resynchronize the incoming data to the logic array clock using successive LE registers or FIFO buffers
- LE registers must be placed in the LAB adjacent to the DQ I/O pin column it is fed by

The Stratix device can use either the rising or falling edge of the system clock to resynchronize the DQ signals. For more information, see the *DDR SDRAM Controller MegaCore Function User Guide*.

The DQS and DQ pins in the Stratix devices output SSTL-2 class II-compliant signals. Stratix devices also can drive differential SSTL-2 class II signals on the output clock pins. Figure 2–69 shows how the data is sampled using the shifted DQS signals.

***Figure 2–69. Input Timing Diagram in DDR Mode***



***Note to Figure 2–69***

(1) DQS and DQ signals are both inputs. The DQS signal is externally edge-aligned with the data DQ signal.

When writing to the DDR SDRAM/FCRAM, the DQS signal must be center-aligned with the DQ pins. Two PLL outputs are needed to generate the DQS signal and to clock the DQ pins. The DQS are clocked by the 1× PLL output, while the DQ pins are clocked by the 270° phase-shifted 1× PLL output. Figure 2–70 shows the DQS and DQ output timing diagram.

*Figure 2–70. Output TIming Diagram in DDR Mode*

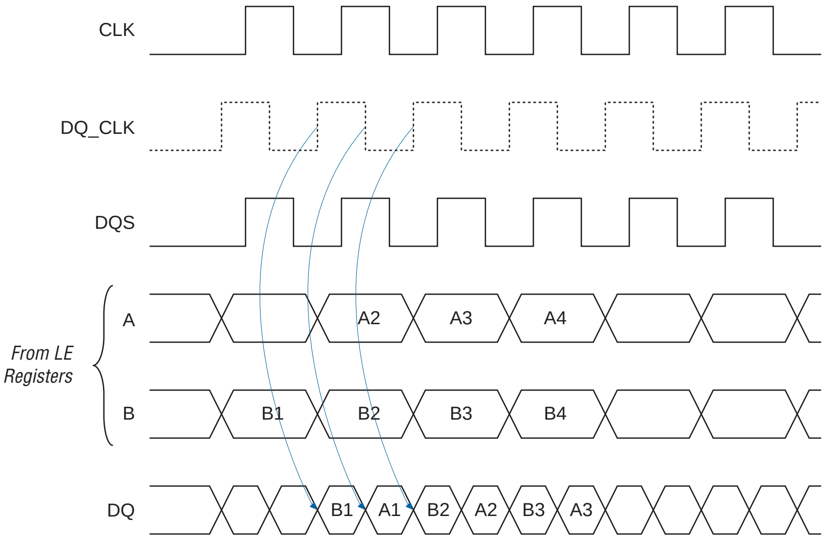
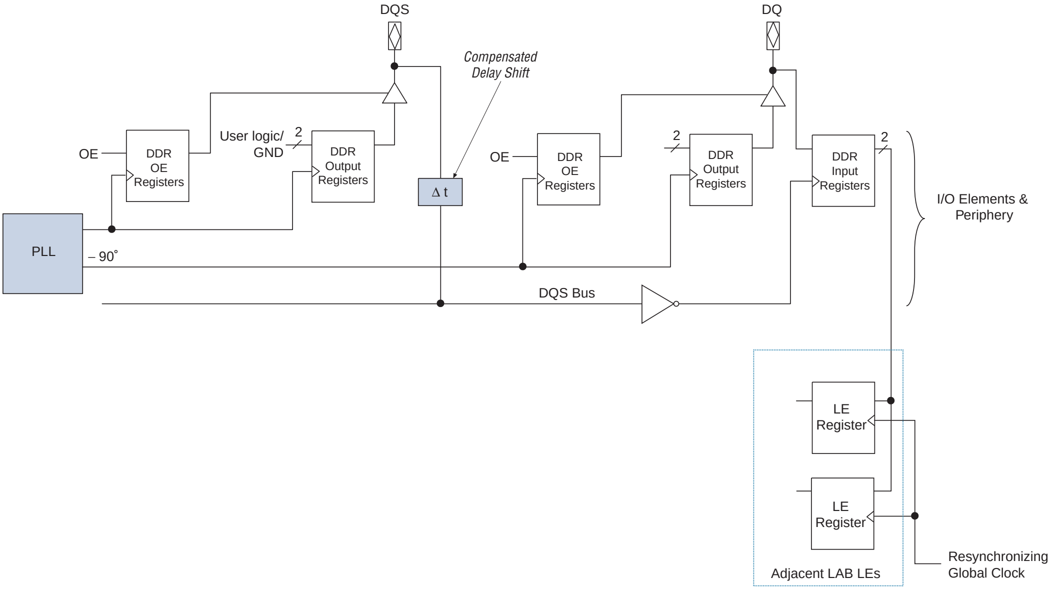


Figure 2–71 illustrates DDR SDRAM and FCRAM interfacing from the I/O through the dedicated circuitry to the logic array. When the DQS pin acts as an input strobe, the dedicated circuitry shifts the incoming DQS pin by either 90° or 72° and clock the DDR input registers. Due to the DDR input registers architecture in Stratix, the shifted DQS signal must be inverted. The DDR registers output is sent to two LE registers to be synchronized with the system clock. When the DQS pin acts as the output strobe, the 1× clock output from the PLL generates the DQS signal, while the shifted 1× PLL clock output clocks the DQ pins. The resynchronizing global clock in Figure 2–71 is usually the non-phase-shifted clock from the PLL output. If the PLL generating the DQ and DQS clocks uses a clock other than the 1× clock, the PLL output must go off-chip and then back onto the chip for use as the input reference clock.

*Figure 2–71. DDR SDRAM Interfacing*



For more information on DDR signaling, refer to Chapter 8, Double Data Rate I/O Signaling in Stratix & Stratix GX Devices of the *Stratix Device Handbook, Volume 2*. and the *DDR SDRAM Controller MegaCore Function User Guide*.

Table 2–27 and Figure 2–72 show the DDR read mode timing parameters.

*Table 2–27. 200-MHz DDR SDRAM Read AC Timing Specifications*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{DV}$ | DQ and DQS output valid time | 1.5 | | ns |
| $t_{DQSQ}$ | DQ to DQS skew | | 0.4 | ns |
| $t_{HSKEW}$ | Data hold skew factor | | 0.6 | ns |
| $t_{EXT}$ | Board skew | –0.3 | 0.3 | ns |
| $t_{SD}$ | Strobe delay | 0.7 | 1.6 | ns |

*Figure 2–72. DDR Read Mode Timing Parameters*

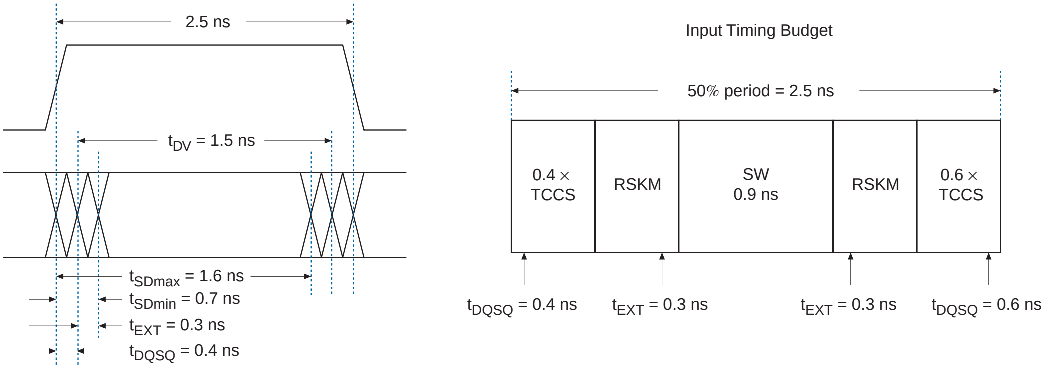


Table 2–28 and Figure 2–73 show the DDR SDRAM write mode timing parameters.

*Table 2–28. 200-MHz DDR SDRAM Write AC Timing Specifications*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{DQSH}$ | DQS high input pulse width | 1.75 | | ns |
| $t_{DQSL}$ | DQS low input pulse width | 1.75 | | ns |
| $t_{DIPW}$ | DQ input pulse width | 1.50 | | ns |
| $t_{DS}$ | Data input setup time from DQS | 0.40 | | ns |
| $t_{DH}$ | Data input hold time from DQS | 0.40 | | ns |
| $t_{CKSKEW}$ | CLK input crossing point voltage | $0.5 \times V_{CCIO} - 0.2$ | $0.5 \times V_{CCIO} + 0.2$ | V |

*Figure 2–73. DDR Write Mode Timing Parameters*

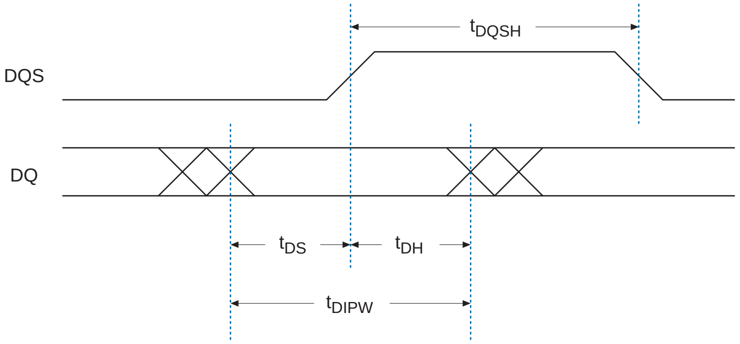
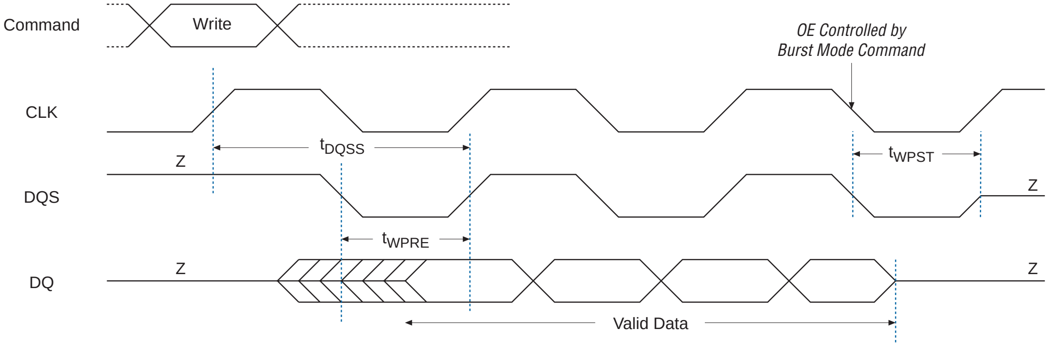


Table 2–29 and Figure 2–74 show the DDR write mode output enable timing parameters.

*Table 2–29. 200-MHz DDR SDRAM Write Mode OE Timing Specifications*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{DQSS}$ | Write to first DQS latching | 3.75 | 6.25 | ns |
| $t_{WPRE}$ | Write preamble | 1.25 |  | ns |
| $t_{WPST}$ | Write postamble | 2.00 | 3.00 | ns |

*Figure 2–74. DDR Read Mode Timing Parameters*



Tables 2–30 through 2–32 and Figure 2–75 show the DDR FCRAM timing specifications.

*Table 2–30. 200-MHz DDR FCRAM Read AC Timing Specifications*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{DV}$ | DQ and DQS output valid time | 1.12 | | ns |
| $t_{DQSQ}$ | DQ to DQS skew | | 0.38 | ns |
| $t_{HSKEW}$ | Data hold skew factor | | 0.90 | ns |
| $t_{EXT}$ | Board skew | –0.30 | 0.30 | ns |
| $t_{SD}$ | Strobe delay | 0.68 | 1.30 | ns |

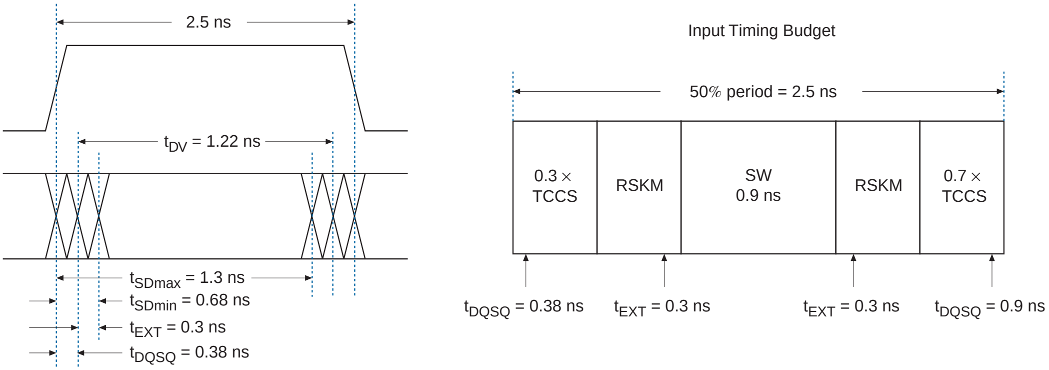
*Table 2–31. 200-MHz DDR FCRAM Write AC Timing Specifications*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{DSP}$ | DQS high input pulse width | 1.75 | | ns |
| $t_{DQSL}$ | DQS low input pulse width | 1.75 | | ns |
| $t_{DIPW}$ | DQ input pulse width | 1.50 | | ns |
| $t_{DS}$ | Data input setup time from DQS | 0.40 | | ns |
| $t_{DH}$ | Data input hold time from DQS | 0.40 | | ns |

*Table 2–32. 200-MHz DDR FCRAM Write Mode OE Timing Specifications*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{DQSS}$ | Write to first DQS latching | 3.75 | 6.25 | ns |
| $t_{WPRE}$ | Write preamble | 1.25 | | ns |
| $t_{WPST}$ | Write postamble | 2.00 | 3.00 | ns |

*Figure 2–75. DDR FCRAM Timing*



## *RLDRAM I & II*

Reduced latency DRAM (RLDRAM) I and II also use DDR signaling to transfer data into and out of the memory.

RLDRAM I uses a pair of DQS pins, one at 180 degree phase shift with respect to the other. Since Stratix devices do not have differential DQS pins, the DQS# signal is ignored. The DQS itself is only used when the Stratix device reads from the RLDRAM I device because the Stratix device uses the RLDRAM clocks for writing to the RLDRAM.

RLDRAM II uses two separate, free-running, unidirectional data strobes (`DKx/DKx#` and `QKx/QKx#`) for writing to, and reading from the RLDRAM II device. The `QKx` strobes should be routed to the DQS pins on the Stratix device. The `QKx#` strobes should be ignored since Stratix devices do not have differential DQS pins. The Stratix device can generate the `DKx/DKx#` strobes with the enhanced PLL's differential clock outputs. This implementation will give the strobes the best jitter performance.

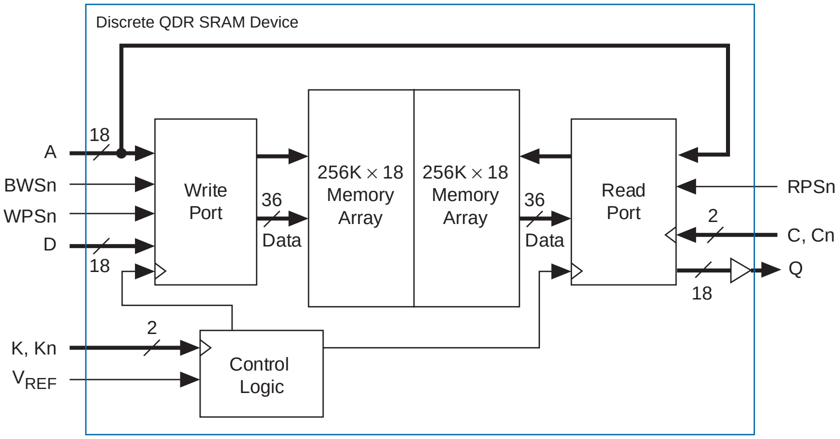
RLDRAM I and II use the 1.8-V HSTL I/O standard. Stratix devices support operation up to 200 MHz.

For more information on Stratix device support for RLDRAM I and II, contact Altera Applications.

## *QDR & QDR II SRAM*

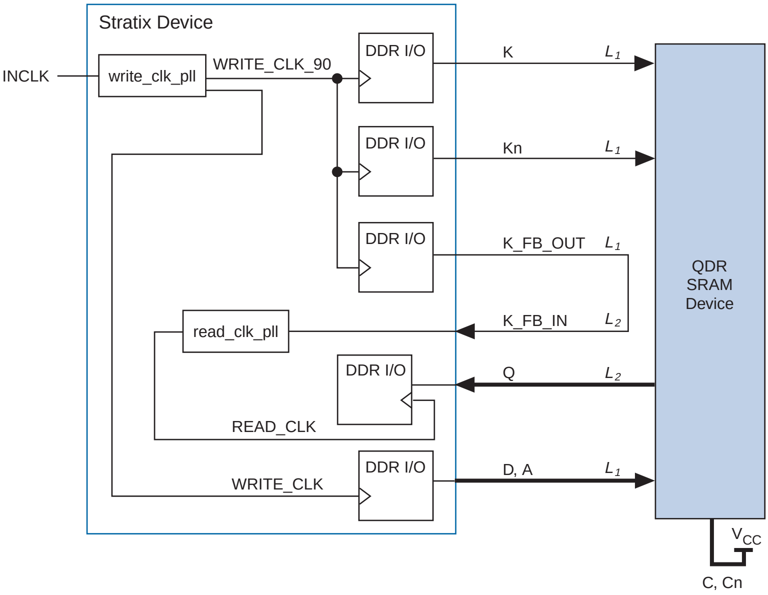
QDR SRAM provides independent read and write ports that eliminate bus turnaround. The memory uses two sets of clocks: `K` and `Kn` for write access, and `C` and `Cn` for read accesses, where `Kn` and `Cn` are the inverse of the `K` and `C` clocks, respectively. You can use differential HSTL I/O pins to drive the QDR SRAM clock into the Stratix device. The separate write data and read data ports permit a transfer rate up to four words on every cycle through the DDR circuitry. Stratix devices also offer on-chip termination resistor to implement the required termination scheme for the 1.5-V HSTL I/O standard. Stratix devices support both burst-of-2 and burst-of-4 QDR SRAM architectures, with clock cycles up to 167 MHz using the 1.5-V HSTL class I or class II I/O standard. Figure 2–76 shows the block diagram for QDR SRAM burst-of-2 architecture.

***Figure 2–76. QDR SRAM Block diagram for Burst-Of-2 Architecture***



Stratix devices utilize the DDR I/O circuitry for the input and output data bus and the `K` and `Kn` output clock signals. Figure 2–77 shows QDR SRAM interfacing from the I/O pin using the DDR I/O circuitry. Stratix devices also support QDR II SRAM at higher clock speeds since the timing requirements for QDR II SRAM are not as strict as QDR SRAM. Altera offers a QDR SRAM Controller Reference Design that can be modified to interface with multiple QDR SRAM devices.

*Figure 2–77. QDR SRAM Interfacing*



Go to www.qdrsram.com for the QDR SRAM specifications. For more information on QDR SRAM Interfaces in Stratix devices, see Chapter 2, QDR SRAM Controller Reference Design for Stratix & Stratix GX Devices of the *Stratix Device Handbook, Volume 2*.

Tables 2–33 and 2–34 and Figure 2–78 show QDR SRAM timing specifications for Stratix devices.

*Table 2–33. 1.5-V HSTL Class I & II 166-MHz QDR AC Timing Specifications*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{CO}$ | `CLK` to valid signal delay | 0.8 | 2.2 | ns |
| $t_{SU}$ | Input setup time to `CLK` |  | 0.0 | ns |
| $t_{HD}$ | Input hold time to `CLK` |  | 0.7 | ns |

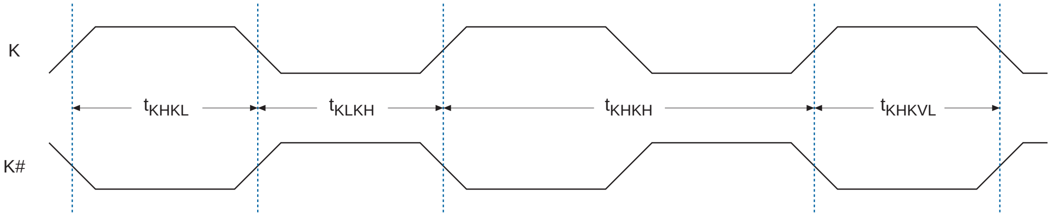
*Table 2–34. 166-MHz QDR Clock Timing Specifications*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{KHKH}$ | Clock cycle time | 6.0 | | ns |
| $t_{KHKL}$ | Clock high time | 2.4 | | ns |
| $t_{KLKH}$ | Clock low time | 2.4 | | ns |
| $t_{KHK\#H}$ *(1)* | Clock K/C rising to clock K#/C# rising | 2.7 | 3.3 | ns |

*Note to Table 2–34:*

(1) The maximum clock skew between K/C to clock K#/C# is 300 ps.

*Figure 2–78. QDR Clock Skew*



## Zero Bus Turnaround SRAM Interface Support

In addition to DDR SDRAM support, Stratix device I/O pins can also interface with ZBT SRAM devices at up to 200 MHz. ZBT SRAM blocks eliminate dead bus cycles when turning a bidirectional bus around between reads and writes or between writes and reads. ZBT allows for 100% bus utilization because ZBT SRAM can be read or written on every clock cycle. Bus contention can occur when shifting from a write cycle to a read cycle or vice versa with no idle cycles in between. ZBT SRAM allows small amounts of bus contention. Bus contention will not damage Stratix device I/O drivers, but it will increase the power dissipation. To avoid bus contention, the output clock-to-low-impedance time ($t_{ZX}$) must be greater than the clock-to-high-impedance time ($t_{XZ}$). Stratix devices can meet ZBT $t_{CO}$ and $t_{SU}$ timing requirements by controlling phase delay in clocks to the OE/output and input registers using an enhanced PLL. Figure 2–79 shows a flow-through ZBT SRAM operation where the A1 and A3 are read addresses and A2 and A4 are write addresses. For pipelined ZBT SRAM operation, data is delayed by another clock cycle. Stratix devices support up to 200-MHz ZBT SRAM operation using the 2.5-V or 3.3-V LVTTL I/O standard.

*Figure 2–79. $t_{ZX}$ & $t_{XZ}$ Timing Diagram*

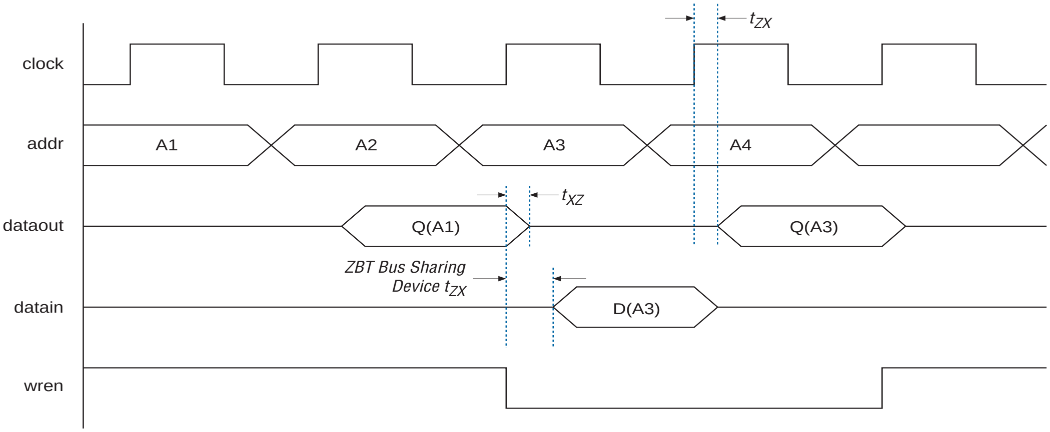


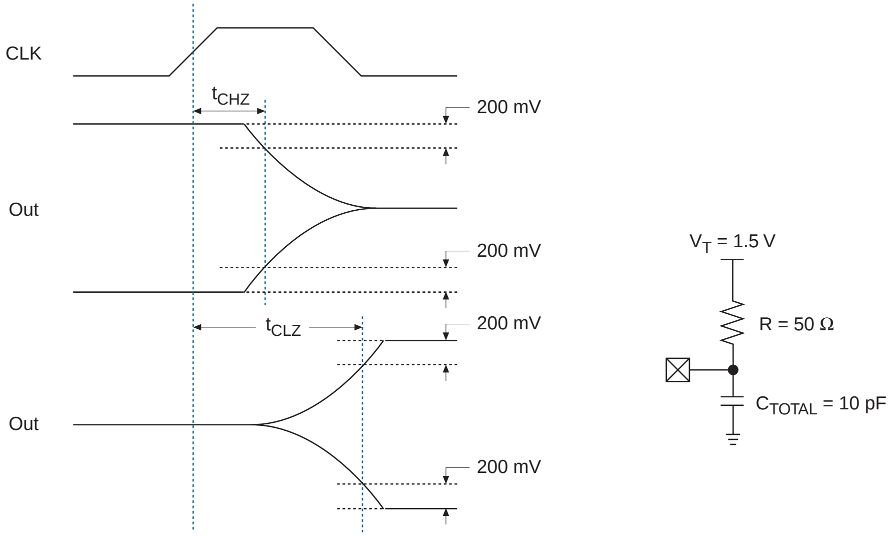
Table 2–35 and Figure 2–80 show the ZBT timing specifications for Stratix devices.

*Table 2–35. 200-MHz ZBT AC Timing Specifications Notes (1), (2)*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CCINT}$ | Logic array supply voltage | 1.425 | 1.575 | V |
| $V_{CCIO}$ | Output supply voltage | 3.135/<br>2.375 | 3.465/<br>2.625 | V |
| $t_{CO}$ | `CLK` to signal valid delay | 0.5 | 3.5 | ns |
| $t_{SU}$ | Input setup time to `CLK` | | 1.8 | ns |
| $t_{CLZ}$ | `CLK` to low impedance *(3)* | 2.2 | 3.5 | ns |
| $t_{CHZ}$ | `CLK` to high impedance *(3)* | 0.5 | 1.5 | ns |
| $t_{HD}$ | Input hold time to `CLK` | | 1.5 | ns |
| $t_A$ | Operating temperature | 0 | 70 | °C |

***Notes to Table 2–35:***
(1) Load for ZBT $t_{CO}$ ($C_L$ = 10 pF).
(2) PLL jitter, PLL time step resolution, and `CLK` skew are included.
(3) $V_{CCIO}$ variation is 3.3 V/2.5 V ±5%.

*Figure 2–80. ZBT Turn-On & Turn-Off Timing*



## Programmable Drive Strength

The output buffer for each Stratix device I/O pin has a programmable drive strength control for certain I/O standards. The LVTTL and LVCMOS standard has several levels of drive strength that the user can control. SSTL-3 class I and II, SSTL-2 class I and II, HSTL class I and II, and 3.3-V GTL+ support a minimum setting, the lowest drive strength that guarantees the $I_{OH}/I_{OL}$ of the standard. Using minimum settings provides signal slew rate control to reduce system noise and signal overshoot.

Table 2–36 shows the possible settings for the I/O standards with drive strength control.

*Table 2–36. Programmable Drive Strength*

| I/O Standard | $I_{OH}$ / $I_{OL}$ Current Strength Setting (mA) |
|---|---|
| 3.3-V LVTTL | 24 *(1)*, 16, 12, 8, 4 |
| 3.3-V LVCMOS | 24 *(2)*, 12 *(1)*, 8, 4, 2 |
| 2.5-V LVTTL/LVCMOS | 16 *(1)*, 12, 8, 2 |
| 1.8-V LVTTL/LVCMOS | 12 *(1)*, 8, 2 |
| 1.5-V LVCMOS | 8 *(1)*, 4, 2 |

***Notes to Table 2–36:***

(1) This is the Quartus II software default current setting.

(2) I/O banks 1, 2, 5, and 6 do not support this setting.

## Open-Drain Output

Stratix devices provide an optional open-drain (equivalent to an open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write-enable signals) that can be asserted by any of several devices.

## Slew-Rate Control

The output buffer for each Stratix device I/O pin has a programmable output slew-rate control that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay to rising and falling edges. Each I/O pin has an individual slew-rate control, allowing the designer to specify the slew rate on a pin-by-pin basis. The slew-rate control affects both the rising and falling edges.

## Bus Hold

Each Stratix device I/O pin provides an optional bus-hold feature. The bus-hold circuitry can weakly hold the signal on an I/O pin at its last-driven state. Since the bus-hold feature holds the last-driven state of the pin until the next input signal is present, you do not need an external pull-up or pull-down resistor to hold a signal level when the bus is tri-stated.

The bus-hold circuitry also pulls undriven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. The designer can select this feature individually for each I/O pin. The bus-hold output will drive no higher than $V_{CCIO}$ to prevent overdriving signals. If the bus-hold feature is enabled, the programmable pull-up option cannot be used. Disable the bus-hold feature when using open-drain outputs with the GTL+ I/O standard or when the I/O pin has been configured for differential signals.

The bus-hold circuitry uses a resistor with a nominal resistance ($R_{BH}$) of approximately 7 kΩ to weakly pull the signal level to the last-driven state. Table 4–31 on page 4–15 gives the specific sustaining current driven through this resistor and overdrive current used to identify the next-driven input level. This information is provided for each $V_{CCIO}$ voltage level.

The bus-hold circuitry is active only after configuration. When going into user mode, the bus-hold circuit captures the value on the pin present at the end of configuration.

## Programmable Pull-Up Resistor

Each Stratix device I/O pin provides an optional programmable pull-up resistor during user mode. If you enable this feature for an I/O pin, the pull-up resistor (typically 25 kΩ) weakly holds the output to the $V_{CCIO}$ level of the output pin's bank.

## Advanced I/O Standard Support

Stratix device IOEs support the following I/O standards:

- LVTTL
- LVCMOS
- 1.5 V
- 1.8 V
- 2.5 V
- 3.3-V PCI
- 3.3-V PCI-X 1.0
- 3.3-V AGP (1× and 2×)
- LVDS
- LVPECL
- 3.3-V PCML
- HyperTransport
- Differential HSTL (on input/output clocks only)
- Differential SSTL (on output column clock pins only)
- GTL/GTL+
- 1.5-V HSTL class I and II

- 1.8-V HSTL Class I and II
- SSTL-3 class I and II
- SSTL-2 class I and II
- SSTL-18 class I and II
- CTT

Table 2–37 describes the I/O standards supported by Stratix devices.

**Table 2–37. Stratix Supported I/O Standards**

| I/O Standard | Type | Input Reference Voltage ($V_{REF}$) (V) | Output Supply Voltage ($V_{CCIO}$) (V) | Board Termination Voltage ($V_{TT}$) (V) |
|---|---|---|---|---|
| LVTTL | Single-ended | N/A | 3.3 | N/A |
| LVCMOS | Single-ended | N/A | 3.3 | N/A |
| 2.5 V | Single-ended | N/A | 2.5 | N/A |
| 1.8 V | Single-ended | N/A | 1.8 | N/A |
| 1.5 V | Single-ended | N/A | 1.5 | N/A |
| 3.3-V PCI | Single-ended | N/A | 3.3 | N/A |
| 3.3-V PCI-X 1.0 | Single-ended | N/A | 3.3 | N/A |
| LVDS | Differential | N/A | 3.3 | N/A |
| LVPECL | Differential | N/A | 3.3 | N/A |
| 3.3-V PCML | Differential | N/A | 3.3 | N/A |
| HyperTransport | Differential | N/A | 2.5 | N/A |
| Differential HSTL *(1)* | Differential | 0.75 | 1.5 | 0.75 |
| Differential SSTL *(2)* | Differential | 1.25 | 2.5 | 1.25 |
| GTL | Voltage-referenced | 0.8 | N/A | 1.20 |
| GTL+ | Voltage-referenced | 1.0 | N/A | 1.5 |
| 1.5-V HSTL class I and II | Voltage-referenced | 0.75 | 1.5 | 0.75 |
| 1.8-V HSTL class I and II | Voltage-referenced | 0.9 | 1.8 | 0.9 |
| SSTL-18 class I and II | Voltage-referenced | 0.90 | 1.8 | 0.90 |
| SSTL-2 class I and II | Voltage-referenced | 1.25 | 2.5 | 1.25 |
| SSTL-3 class I and II | Voltage-referenced | 1.5 | 3.3 | 1.5 |
| AGP (1× and 2×) | Voltage-referenced | 1.32 | 3.3 | N/A |
| CTT | Voltage-referenced | 1.5 | 3.3 | 1.5 |

*Notes to Table 2–37:*

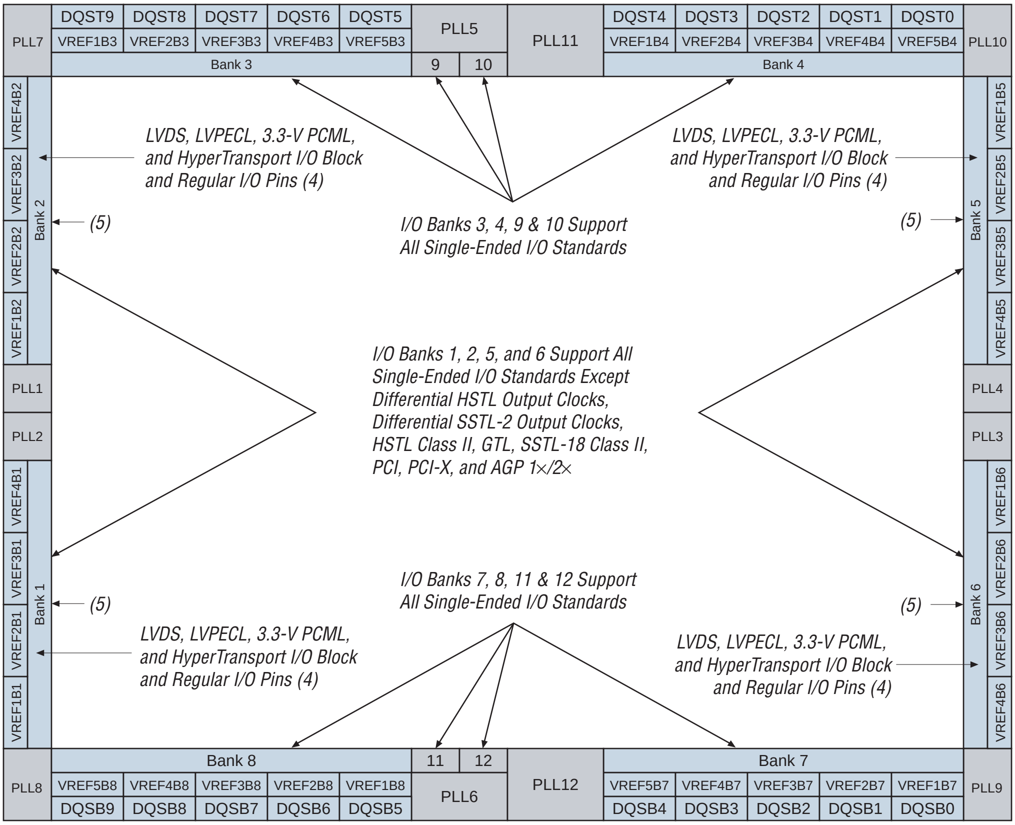
(1) This I/O standard is only available on input and output clock pins.

(2) This I/O standard is only available on output column clock pins.

For more information on I/O standards supported by Stratix devices, see Chapter 4, Using Selectable I/O Standards in Stratix & Stratix GX Devices of the *Stratix Device Handbook, Volume 2*.

Stratix devices contain eight I/O banks in addition to the four enhanced PLL external clock out banks, as shown in Figure 2–81. The four I/O banks on the right and left of the device contain circuitry to support high-speed differential I/O for LVDS, LVPECL, 3.3-V PCML, and HyperTransport inputs and outputs. These banks support all I/O standards listed in Table 2–37 except PCI I/O pins or PCI-X 1.0, GTL, SSTL-18 Class II, and HSTL Class II outputs. The top and bottom I/O banks support all single-ended I/O standards. Additionally, Stratix devices support four enhanced PLL external clock output banks, allowing clock output capabilities such as differential support for SSTL and HSTL. Table 2–38 shows I/O standard support for each I/O bank.

**Figure 2–81. Stratix I/O Banks** Notes (1), (2), (3)



*Notes to Figure 2–81:*

1. (1) Figure 2–81 is a top view of the silicon die. This will correspond to a top-down view for non-flip-chip packages, but will be a reverse view for flip-chip packages.
2. (2) Figure 2–81 is a graphic representation only. Refer to the pin list and the Quartus II software for exact locations.
3. (3) Banks 9 through 12 are enhanced PLL external clock output banks.
4. (4) If the high-speed differential I/O pins are not used for high-speed differential signaling, they can support all of the I/O standards except HSTL class I and II, GTL, SSTL-18 Class II, PCI, PCI-X 1.0, and AGP 1×/2×.
5. (5) You can only place single-ended input pads four or more pads away from a differential pad. You can only place single-ended output/bidirectional pads five or more pads away from a differential pad. Use the **Show Pads** view in the Quartus II Floorplan Editor to locate these pads. The Quartus II software will give an error message for illegal output or bidirectional pin placement next to a high-speed differential I/O pin.

Table 2–38 shows I/O standard support for each I/O bank.

*Table 2–38. I/O Support by Bank (Part 1 of 2)*

| I/O Standard | Top & Bottom Banks (3, 4, 7 & 8) | Left & Right Banks (1, 2, 5 & 6) | Enhanced PLL External Clock Output Banks (9, 10, 11 & 12) |
|---|---|---|---|
| LVTTL | ✓ | ✓ | ✓ |
| LVCMOS | ✓ | ✓ | ✓ |
| 2.5 V | ✓ | ✓ | ✓ |
| 1.8 V | ✓ | ✓ | ✓ |
| 1.5 V | ✓ | ✓ | ✓ |
| 3.3-V PCI | ✓ |  | ✓ |
| 3.3-V PCI-X 1.0 | ✓ |  | ✓ |
| LVPECL |  | ✓ |  |
| 3.3-V PCML |  | ✓ |  |
| LVDS |  | ✓ |  |
| HyperTransport technology |  | ✓ |  |
| Differential HSTL (clock inputs) | ✓ | ✓ |  |
| Differential HSTL (clock outputs) |  |  | ✓ |
| Differential SSTL (clock outputs) |  |  | ✓ |
| 3.3-V GTL | ✓ | *(1)* | ✓ |
| 3.3-V GTL+ | ✓ | ✓ | ✓ |
| 1.5-V HSTL class I | ✓ | ✓ | ✓ |
| 1.5-V HSTL class II | ✓ | *(1)* | ✓ |
| 1.8-V HSTL class I | ✓ | ✓ | ✓ |
| 1.8-V HSTL class II | ✓ | *(1)* | ✓ |
| SSTL-18 class I | ✓ | ✓ | ✓ |
| SSTL-18 class II | ✓ | *(1)* | ✓ |
| SSTL-2 class I | ✓ | ✓ | ✓ |
| SSTL-2 class II | ✓ | ✓ | ✓ |
| SSTL-3 class I | ✓ | ✓ | ✓ |

*Table 2–38. I/O Support by Bank (Part 2 of 2)*

| I/O Standard | Top & Bottom Banks (3, 4, 7 & 8) | Left & Right Banks (1, 2, 5 & 6) | Enhanced PLL External Clock Output Banks (9, 10, 11 & 12) |
|---|---|---|---|
| SSTL-3 class II | ✓ | ✓ | ✓ |
| AGP (1× and 2×) | ✓ | *(1)* | ✓ |
| CTT | ✓ | ✓ | ✓ |

***Note to Table 2–38:***

(1) These I/O standards are only supported for input pins.

Each I/O bank has its own `VCCIO` pins. A single device can support 1.5-, 1.8-, 2.5-, and 3.3-V interfaces; each bank can support a different standard independently. Each bank also has dedicated `VREF` pins to support any one of the voltage-referenced standards (such as SSTL-3) independently.

Each I/O bank can support multiple standards with the same $V_{CCIO}$ for input and output pins. Each bank can support one voltage-referenced I/O standard. For example, when $V_{CCIO}$ is 3.3 V, a bank can support LVTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs.

## Terminator Technology

Terminator technology provides on-chip parallel and differential termination (LVDS I/O Standard) and impedance matching (series termination) to reduce reflections and maintain signal integrity. Terminator technology simplifies board design by minimizing the number of external termination resistors required. These resistors can be placed inside the package, eliminating small stubs that can still lead to reflections. Additionally, the terminator technology provides constant calibration of the internal resistor values after configuration and during normal operation via two external reference resistors. The constant calibration allows the termination resistors to compensate for process, temperature, and voltage variation, providing a robust termination scheme. There is one set of reference resistors for each I/O bank.

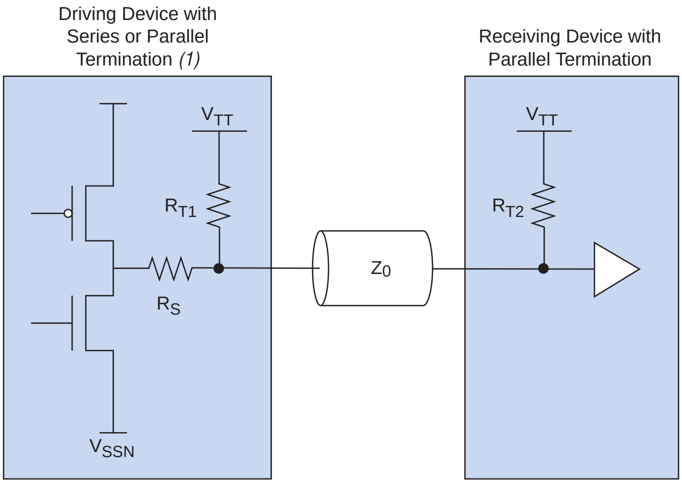
Three types of termination are available in the device:

- Series Termination ($R_S$) and Impedance Matching
- Parallel Termination ($R_T$)
- Differential Termination ($R_D$) for LVDS

Stratix devices support series termination for SSTL-3 and SSTL-2 signals to meet SSTL specifications. Stratix devices also support driver impedance matching through series termination for LVTTL and LVCMOS signals to match the impedance of the transmission lines, typically 25 or 50 Ω. When used with the output drivers, the terminator technology sets the output driver impedance to 25 or 50 Ω as specified by the external reference resistors, resulting in significantly reduced reflections.

Parallel termination is supported for SSTL-3, SSTL-2, HSTL, GTL, GTL+, and CTT signals as defined by the respective I/O standards. Figure 2–82 illustrates the possible termination schemes for single-ended I/O pins.

***Figure 2–82. Termination Schemes for Single-Ended I/O Pins***

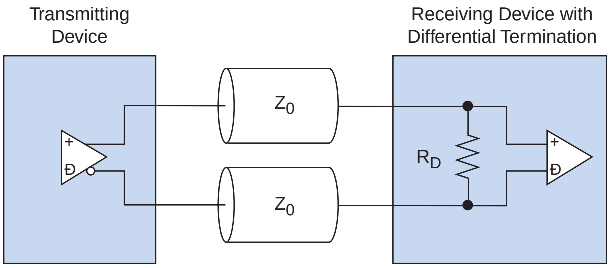


*Note to Figure 2–82:*

(1) In the transmitting device, only one type of termination: series or parallel termination is possible. For standards that require both terminations, such as SSTL 2 Class II, an external parallel termination resistor must be provided.

Stratix devices support differential termination with a 100-Ω resistor for LVDS signals. Figure 2–83 shows the device with differential termination.

*Figure 2–83. Differential LVDS Input On-Chip Termination*



Terminator technology can only support one type of termination per I/O bank, although some different I/O standards can be mixed within a given I/O bank. I/O banks at the top and bottom of the device support series termination and impedance matching and parallel termination. I/O banks on the left and right side of the device support series termination and impedance matching and LVDS far-end differential termination. Each I/O bank utilizing on-chip termination must connect two external reference resistors, $R_{UP}$ and $R_{DN}$, to the designated pins in the I/O bank. The designer sets which pins are terminated and match the reference resistors. After configuration and during normal operation, the device periodically samples the external resistor values and updates the internal resistor values. Table 2–39 shows the Terminator technology support within each I/O bank.

*Table 2–39. Terminator Technology Support by I/O Banks*

| Terminator Technology Support | Top & Bottom Banks (3, 4, 7 & 8) | Left & Right Banks (1, 2, 5 & 6) |
|---|---|---|
| Series termination | ✓ | ✓ |
| Impedance matching (LVTTL/LVCMOS) | ✓ | ✓ |
| Parallel termination *(1)* | ✓ | |
| Differential termination *(2)*, *(3)* | | ✓ |

***Notes to Table 2–39:***

(1) Clock pins `CLK[0..3]` and `CLK[8..11]` do not support parallel termination.

(2) Clock pins `CLK0`, `CLK2`, `CLK9`, `CLK11`, and pins `FPLL[7..10]CLK` do not support differential termination.

(3) Differential termination is only supported for LVDS as it requires 3.3-V `VCCIO`.

Table 2–40 summarizes the external resistor values required for Terminator technology.

*Table 2–40. External Resistor Values*

| Parameter | $R_{UP}$ | $R_{DN}$ |
|---|---|---|
| Series termination | 250 Ω | 250 Ω |
| Impedance matching (LVTTL/LVCMOS) | 250 Ω / 500 Ω | 250 Ω / 500 Ω |
| Parallel termination *(1)* | 1,000 Ω | 1,000 Ω |
| Differential termination | *(2)* | *(2)* |

***Notes to Table 2–40:***

(1) Stratix devices support parallel termination on the top and bottom I/O banks only.

(2) No external resistor is necessary.

## MultiVolt I/O Interface

The Stratix architecture supports the MultiVolt I/O interface feature, which allows Stratix devices in all packages to interface with systems of different supply voltages.

The Stratix `VCCINT` pins must always be connected to a 1.5-V power supply. With a 1.5-V $V_{CCINT}$ level, input pins are 1.5-V, 1.8-V, 2.5-V, and 3.3-V tolerant. The `VCCIO` pins can be connected to either a 1.5-V, 1.8-V, 2.5-V, or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (i.e., when `VCCIO` pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems). When `VCCIO` pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems.

Table 2–41 summarizes Stratix MultiVolt I/O support.

**Table 2–41. Stratix MultiVolt I/O Support** *Note (1)*

| $V_{CCIO}$ (V) | Input Signal | | | | | Output Signal | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | 1.5 V | 1.8 V | 2.5 V | 3.3 V | 5.0 V | 1.5 V | 1.8 V | 2.5 V | 3.3 V | 5.0 V |
| 1.5 | ✓ | ✓ | ✓ *(2)* | ✓ *(2)* | | ✓ | | | | |
| 1.8 | ✓ *(2)* | ✓ | ✓ *(2)* | ✓ *(2)* | | ✓ *(3)* | ✓ | | | |
| 2.5 | | | ✓ | ✓ | | ✓ *(3)* | ✓ *(3)* | ✓ | | |
| 3.3 | | | ✓ *(2)* | ✓ | ✓ *(4)* | ✓ *(3)* | ✓ *(3)* | ✓ *(3)* | ✓ | ✓ |

*Notes to Table 2–41:*

(1) To drive inputs higher than $V_{CCIO}$ but less than 4.1 V, disable the PCI clamping diode. However, to drive 5.0-V inputs to the device, enable the PCI clamping diode to prevent $V_I$ from rising above 4.1 V.

(2) The pin current may be slightly higher than the default value. Contact Altera Applications for details.

(3) Although $V_{CCIO}$ specifies the voltage necessary for the Stratix device to drive out, a receiving device powered at a different level can still interface with the Stratix device if it has inputs that tolerate the $V_{CCIO}$ value.

(4) Stratix devices can be 5.0-V tolerant with the use of an external resistor and the internal PCI clamp diode.

## High-Speed Differential I/O Support

Stratix devices contain dedicated circuitry for supporting differential standards at speeds up to 840 Mbps. The following differential I/O standards are supported in the Stratix device: LVDS, LVPECL, HyperTransport, and 3.3-V PCML.

There are four dedicated high-speed PLLs in the EP1S10 to EP1S25 devices and eight dedicated high-speed PLLs in the EP1S30 to EP1S80 devices to multiply reference clocks and drive high-speed differential SERDES channels.

Table 2–42 sshows the number of channels and fast PLLs in EP1S10, EP1S20, and EP1S25 devices. Tables 2–43 through 2–46 show this information for EP1S30, EP1S40, EP1S60, and EP1S80 devices.

***Table 2–42. EP1S10, EP1S20 & EP1S25 Device Differential Channels (Part 1 of 2)*** *Note (1)*

| Device | Package | Transmitter/ Receiver | Total Channels | Maximum Speed (Mbps) | Center Fast PLLs | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | PLL 1 | PLL 2 | PLL 3 | PLL 4 |
| EP1S10 | 484-pin FineLine BGA | Transmitter *(2)* | 20 | 840 | 5 | 5 | 5 | 5 |
| | | | | 462 *(3)* | 10 | 10 | 10 | 10 |
| | | Receiver | 20 | 840 | 5 | 5 | 5 | 5 |
| | | | | 462 *(3)* | 10 | 10 | 10 | 10 |
| | 672-pin FineLine BGA | Transmitter *(2)* | 36 | 462 *(4)* | 9 | 9 | 9 | 9 |
| | | | | 462 *(3)* | 18 | 18 | 18 | 18 |
| | | Receiver | 36 | 462 *(4)* | 9 | 9 | 9 | 9 |
| | | | | 462 *(3)* | 18 | 18 | 18 | 18 |
| | 780-pin FineLine BGA | Transmitter *(2)* | 44 | 840 | 11 | 11 | 11 | 11 |
| | | | | 462 *(3)* | 22 | 22 | 22 | 22 |
| | | Receiver | 44 | 840 | 11 | 11 | 11 | 11 |
| | | | | 462 *(3)* | 22 | 22 | 22 | 22 |
| EP1S20 | 484-pin FineLine BGA | Transmitter *(2)* | 24 | 840 | 6 | 6 | 6 | 6 |
| | | | | 462 *(3)* | 12 | 12 | 12 | 12 |
| | | Receiver | 20 | 840 | 5 | 5 | 5 | 5 |
| | | | | 462 *(3)* | 10 | 10 | 10 | 10 |
| | 672-pin FineLine BGA | Transmitter *(2)* | 48 | 462 *(4)* | 12 | 12 | 12 | 12 |
| | | | | 462 *(3)* | 24 | 24 | 24 | 24 |
| | | Receiver | 50 | 462 *(4)* | 13 | 12 | 12 | 13 |
| | | | | 462 *(3)* | 25 | 25 | 25 | 25 |
| | 780-pin FineLine BGA | Transmitter *(2)* | 66 | 840 | 17 | 16 | 16 | 17 |
| | | | | 462 *(3)* | 33 | 33 | 33 | 33 |
| | | Receiver | 66 | 840 | 17 | 16 | 16 | 17 |
| | | | | 462 *(3)* | 33 | 33 | 33 | 33 |

*Table 2–42. EP1S10, EP1S20 & EP1S25 Device Differential Channels (Part 2 of 2) Note (1)*

| Device | Package | Transmitter/ Receiver | Total Channels | Maximum Speed (Mbps) | Center Fast PLLs | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | PLL 1 | PLL 2 | PLL 3 | PLL 4 |
| EP1S25 | 672-pin FineLine BGA | Transmitter *(2)* | 56 | 462 *(4)* | 14 | 14 | 14 | 14 |
| | | | | 462 *(3)* | 28 | 28 | 28 | 28 |
| | | Receiver | 58 | 462 *(4)* | 14 | 15 | 15 | 14 |
| | | | | 462 *(3)* | 29 | 29 | 29 | 29 |
| | 780-pin FineLine BGA | Transmitter *(2)* | 70 | 840 | 18 | 17 | 17 | 18 |
| | | | | 462 *(3)* | 35 | 35 | 35 | 35 |
| | | Receiver | 66 | 840 | 17 | 16 | 16 | 17 |
| | | | | 462 *(3)* | 33 | 33 | 33 | 33 |
| | 1,020-pin FineLine BGA | Transmitter *(2)* | 78 | 840 | 19 | 20 | 20 | 19 |
| | | | | 462 *(3)* | 39 | 39 | 39 | 39 |
| | | Receiver | 78 | 840 | 19 | 20 | 20 | 19 |
| | | | | 462 *(3)* | 39 | 39 | 39 | 39 |

*Notes to Table 2–42:*

(1) Table 2–42 shows two different number of channels depending on the channel speed. For example, in the 484-pin FineLine BGA EP1S10 device, PLL 1 can drive a maximum of five channels at 840 Mbps or a maximum of 10 channels at 462 Mbps. The Quartus II software may also merge receiver and transmitter PLLs when a receiver is driving a transmitter. In this case, one fast PLL can drive both the maximum numbers of receiver and transmitter channels.

(2) The number of channels listed includes the transmitter clock output (`tx_outclock`) channel. You can use an extra data channel if you need a DDR clock.

(3) These channels span across two banks per side of the device. When a center fast PLL drives the opposite bank on the same side of the device, the other center fast PLL cannot drive any differential channels on the device. For example, if PLL 1 in a 484-pin FineLine BGA EP1S10 device drives 10 channels at 462 Mbps, PLL 2 cannot drive any differential channels. Similar restrictions apply to PLLs 3 and 4.

(4) 672-pin packages only support up to 462 Mbps. These values show the channels available for each PLL without crossing another bank.

**Table 2–43. EP1S30 Differential Channels** *Note (1)*

| Package | Transmitter/ Receiver | Total Channels | Maximum Speed (Mbps) | Center Fast PLLs | | | | Corner Fast PLLs *(2)*, *(7)* | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | PLL1 | PLL2 | PLL3 | PLL4 | PLL7 | PLL8 | PLL9 | PLL10 |
| 780-pin FineLine BGA | Transmitter *(3)* | 70 | 840 | 18 | 17 | 17 | 18 | *(5)* | *(5)* | *(5)* | *(5)* |
| | | | 462 *(4)* | 35 | 35 | 35 | 35 | *(5)* | *(5)* | *(5)* | *(5)* |
| | Receiver | 66 | 840 | 17 | 16 | 16 | 17 | *(5)* | *(5)* | *(5)* | *(5)* |
| | | | 462 *(4)* | 33 | 33 | 33 | 33 | *(5)* | *(5)* | *(5)* | *(5)* |
| 956-pin FineLine BGA | Transmitter *(3)* | 80 (2) *(6)* | 840 | 19 | 20 | 20 | 19 | 20 | 20 | 20 | 20 |
| | | | 462 *(4)* | 39 | 39 | 39 | 39 | 20 | 20 | 20 | 20 |
| | Receiver | 80 (2) *(6)* | 840 | 20 | 20 | 20 | 20 | 19 | 20 | 20 | 19 |
| | | | 462 *(4)* | 40 | 40 | 40 | 40 | 19 | 20 | 20 | 19 |
| 1,020-pin FineLine BGA | Transmitter *(3)* | 80 (2) *(6)* | 840 | 20 | 20 | 20 | 20 | 20 | 20 | 20 | 20 |
| | | | 462 *(4)* | 40 | 40 | 40 | 40 | 20 | 20 | 20 | 20 |
| | Receiver | 80 (2) *(6)* | 840 | 20 | 20 | 20 | 20 | 20 | 20 | 20 | 20 |
| | | | 462 *(4)* | 40 | 40 | 40 | 40 | 20 | 20 | 20 | 20 |

**Table 2–44. EP1S40 Differential Channels (Part 1 of 2)** *Note (1)*

| Package | Transmitter/ Receiver | Total Channels | Maximum Speed (Mbps) | Center Fast PLLs | | | | Corner Fast PLLs *(2)*, *(7)* | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | PLL1 | PLL2 | PLL3 | PLL4 | PLL7 | PLL8 | PLL9 | PLL10 |
| 780-pin FineLine BGA | Transmitter *(3)* | 68 | 840 | 18 | 16 | 16 | 18 | *(5)* | *(5)* | *(5)* | *(5)* |
| | | | 462 *(4)* | 34 | 34 | 34 | 34 | *(5)* | *(5)* | *(5)* | *(5)* |
| | Receiver | 66 | 840 | 17 | 16 | 16 | 17 | *(5)* | *(5)* | *(5)* | *(5)* |
| | | | 462 *(4)* | 33 | 33 | 33 | 33 | *(5)* | *(5)* | *(5)* | *(5)* |
| 956-pin FineLine BGA | Transmitter *(3)* | 80 | 840 | 18 | 17 | 17 | 18 | 20 | 20 | 20 | 20 |
| | | | 462 *(4)* | 35 | 35 | 35 | 35 | 20 | 20 | 20 | 20 |
| | Receiver | 80 | 840 | 20 | 20 | 20 | 20 | 18 | 17 | 17 | 18 |
| | | | 462 *(4)* | 40 | 40 | 40 | 40 | 18 | 17 | 17 | 18 |
| 1,020-pin FineLine BGA | Transmitter *(3)* | 80 (10) *(6)* | 840 | 20 | 20 | 20 | 20 | 20 | 20 | 20 | 20 |
| | | | 462 *(4)* | 40 | 40 | 40 | 40 | 20 | 20 | 20 | 20 |
| | Receiver | 80 (10) *(6)* | 840 | 20 | 20 | 20 | 20 | 20 | 20 | 20 | 20 |
| | | | 462 *(4)* | 40 | 40 | 40 | 40 | 20 | 20 | 20 | 20 |

*Table 2–44. EP1S40 Differential Channels (Part 2 of 2) Note (1)*

| Package | Transmitter/ Receiver | Total Channels | Maximum Speed (Mbps) | Center Fast PLLs | | | | Corner Fast PLLs *(2), (7)* | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | PLL1 | PLL2 | PLL3 | PLL4 | PLL7 | PLL8 | PLL9 | PLL10 |
| 1,508-pin FineLine BGA | Transmitter *(3)* | 80<br>(10) *(6)* | 840 | 20 | 20 | 20 | 20 | 20 | 20 | 20 | 20 |
| | | | 462 *(4)* | 40 | 40 | 40 | 40 | 20 | 20 | 20 | 20 |
| | Receiver | 80<br>(10) *(6)* | 840 | 20 | 20 | 20 | 20 | 20 | 20 | 20 | 20 |
| | | | 462 *(4)* | 40 | 40 | 40 | 40 | 20 | 20 | 20 | 20 |

*Table 2–45. EP1S60 Differential Channels Note (1)*

| Package | Transmitter/ Receiver | Total Channels | Maximum Speed (Mbps) | Center Fast PLLs | | | | Corner Fast PLLs *(2), (7)* | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | PLL1 | PLL2 | PLL3 | PLL4 | PLL7 | PLL8 | PLL9 | PLL10 |
| 956-pin FineLine BGA | Transmitter *(3)* | 80 | 840 | 12 | 10 | 10 | 12 | 20 | 20 | 20 | 20 |
| | | | 462 *(4)* | 40 | 40 | 40 | 40 | 20 | 20 | 20 | 20 |
| | Receiver | 80 | 840 | 20 | 20 | 20 | 20 | 12 | 10 | 10 | 12 |
| | | | 462 *(4)* | 22 | 22 | 22 | 22 | 12 | 10 | 10 | 12 |
| 1,020-pin FineLine BGA | Transmitter *(3)* | 80<br>(12) *(6)* | 840 | 14 | 14 | 14 | 14 | 20 | 20 | 20 | 20 |
| | | | 462 *(4)* | 28 | 28 | 28 | 28 | 20 | 20 | 20 | 20 |
| | Receiver | 80<br>(10) *(6)* | 840 | 20 | 20 | 20 | 20 | 14 | 13 | 13 | 14 |
| | | | 462 *(4)* | 40 | 40 | 40 | 40 | 14 | 13 | 13 | 14 |
| 1,508-pin FineLine BGA | Transmitter *(3)* | 80<br>(36) *(6)* | 840 | 20 | 20 | 20 | 20 | 20 | 20 | 20 | 20 |
| | | | 462 *(4)* | 40 | 40 | 40 | 40 | 20 | 20 | 20 | 20 |
| | Receiver | 80<br>(36) *(6)* | 840 | 20 | 20 | 20 | 20 | 20 | 20 | 20 | 20 |
| | | | 462 *(4)* | 40 | 40 | 40 | 40 | 20 | 20 | 20 | 20 |

***Table 2–46. EP1S80 Differential Channels*** *Note (1)*

| Package | Transmitter/ Receiver | Total Channels | Maximum Speed (Mbps) | Center Fast PLLs | | | | Corner Fast PLLs *(2)* | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | **PLL1** | **PLL2** | **PLL3** | **PLL4** | **PLL7** | **PLL8** | **PLL9** | **PLL10** |
| 956-pin FineLine BGA | Transmitter *(3)* | 80 (40) *(6)* | 840 | 10 | 10 | 10 | 10 | 20 | 20 | 20 | 20 |
| | | | 462 *(4)* | 20 | 20 | 20 | 20 | 20 | 20 | 20 | 20 |
| | Receiver | 80 | 840 | 20 | 20 | 20 | 20 | 10 | 10 | 10 | 10 |
| | | | 462 *(4)* | 40 | 40 | 40 | 40 | 10 | 10 | 10 | 10 |
| 1,020-pin FineLine BGA | Transmitter *(3)* | 92 (12) *(6)* | 840 | 12 | 14 | 14 | 12 | 20 | 20 | 20 | 20 |
| | | | 462 *(4)* | 26 | 26 | 26 | 26 | 20 | 20 | 20 | 20 |
| | Receiver | 90 (10) *(6)* | 840 | 20 | 20 | 20 | 20 | 10 | 10 | 10 | 10 |
| | | | 462 *(4)* | 40 | 40 | 40 | 40 | 12 | 13 | 13 | 12 |
| 1,508-pin FineLine BGA | Transmitter *(3)* | 80 (72) *(6)* | 840 | 20 | 20 | 20 | 20 | 20 | 20 | 20 | 20 |
| | | | 462 *(4)* | 40 | 40 | 40 | 40 | 28 | 28 | 28 | 28 |
| | Receiver | 80 (56) *(6)* | 840 | 20 | 20 | 20 | 20 | 20 | 20 | 20 | 20 |
| | | | 462 *(4)* | 40 | 40 | 40 | 40 | 24 | 24 | 24 | 24 |

*Notes to Tables 2–43 through 2–46*

(1) This table shows two different number of channels depending on the channel speed. For example, in the 780-pin FineLine BGA EP1S30 device, PLL 1 can drive a maximum of 18 channels at 840 Mbps or a maximum of 35 channels at 462 Mbps. The Quartus II software may also merge transmitter and receiver PLLs when a receiver is driving a transmitter. In this case, one fast PLL can drive both the maximum numbers of receiver and transmitter channels.

(2) Some of the channels accessible by the center fast PLL and the channels accessible by the corner fast PLL overlap. Therefore, the total number of channels is not the addition of the number of channels accessible by PLLs 1, 2, 3, and 4 with the number of channels accessible by PLLs 7, 8, 9, and 10. For more information on which channels overlap, contact Altera Applications.

(3) The numbers of channels listed include the transmitter clock output (`tx_outclock`) channel. You can use an extra data channel if you need a DDR clock.

(4) When a center fast PLL drives the opposite bank on the same side of the device, the other center fast PLL cannot drive any differential channels on the device. For example, if PLL 1 in a 484-pin FineLine BGA EP1S10 device drives 10 channels at 462 Mbps, PLL 2 cannot drive any differential channels. Similar restrictions apply to PLLs 3 and 4.

(5) PLLs 7, 8, 9, and 10 are not available in this device.

(6) The number in parentheses is the number of slow-speed channels, guaranteed to operate at up to 462 Mbps. These channels are independent of the high-speed differential channels. For the location of these channels, contact Altera Applications.

(7) The corner fast PLLs in this device support a preliminary data rate of 462 Mbps. Contact Altera Applications for more information.

The high-speed differential I/O circuitry supports the following high speed I/O interconnect standards and applications:

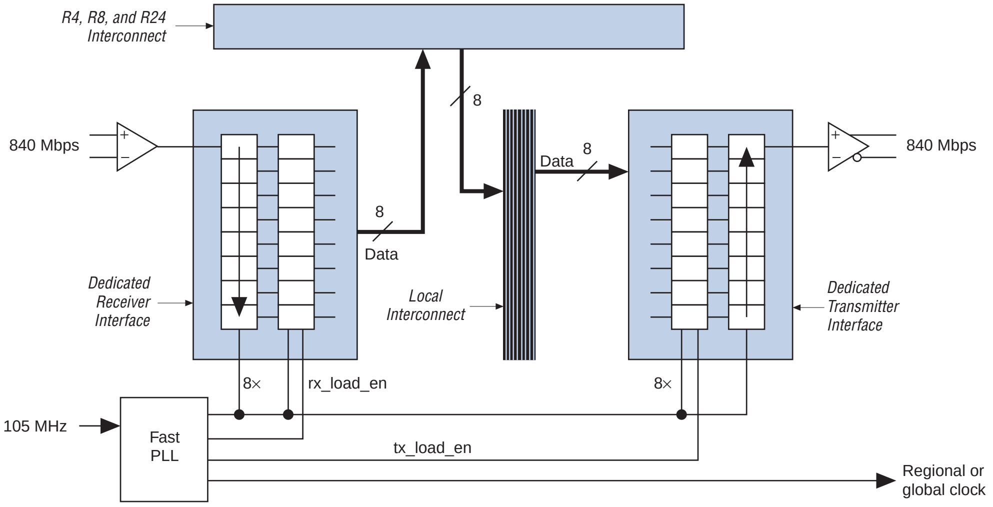
- UTOPIA IV
- SPI-4 Phase 2 (POS-PHY Level 4)
- SFI-4

- 10G Ethernet XSBI
- RapidIO
- HyperTransport

## Dedicated Circuitry

Stratix devices support source-synchronous interfacing with LVDS, LVPECL, 3.3-V PCML, or HyperTransport signaling at up to 840 Mbps. Stratix devices can transmit or receive serial channels along with a low-speed or high-speed clock. The receiving device PLL multiplies the clock by a integer factor W (W = 1 through 32). For example, a HyperTransport application where the data rate is 800 Mbps and the clock rate is 400 MHz would require that W be set to 2. The SERDES factor J determines the parallel data width to deserialize from receivers or to serialize for transmitters. The SERDES factor J can be set to 4, 7, 8, or 10 and does not have to equal the PLL clock-multiplication W value. For a J factor of 1, the Stratix device bypasses the SERDES block. For a J factor of 2, the Stratix device bypasses the SERDES block, and the DDR input and output registers are used in the IOE.

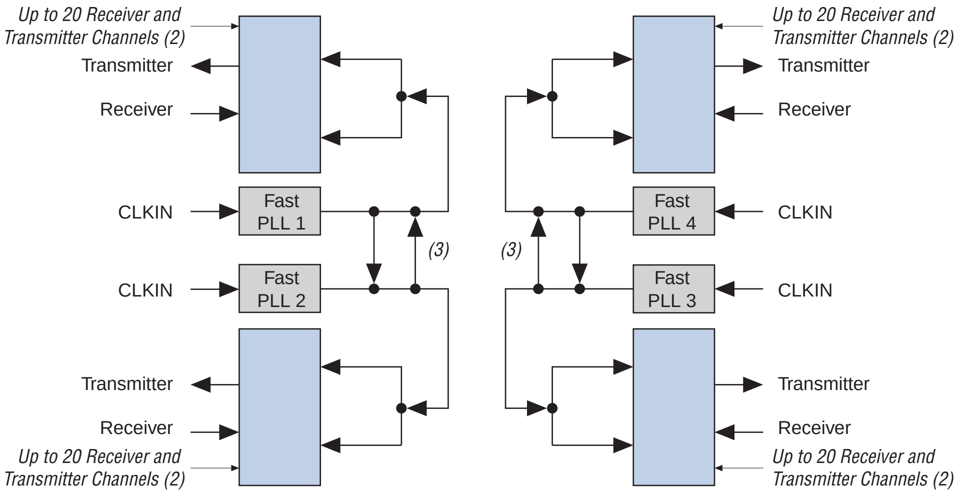
*Figure 2–84. High-Speed Differential I/O Receiver / Transmitter Interface Example*



An external pin or global or regional clock can drive the fast PLLs, which can output up to three clocks: two multiplied high-speed differential I/O clocks to drive the SERDES block and/or external pin, and a low-speed clock to drive the logic array.

The Quartus II MegaWizard Plug-In Manager only allows you to implement up to 20 receiver or 20 transmitter channels for each fast PLL. These channels operate at up to 840 Mbps. The receiver and transmitter channels are interleaved such that each I/O bank on the left and right side of the device has one receiver channel and one transmitter channel per LAB row. Figure 2–85 shows the fast PLL and channel layout in EP1S10, EP1S20, and EP1S25 devices. Figure 2–86 shows the fast PLL and channel layout in the EP1S30 to EP1S80 devices.

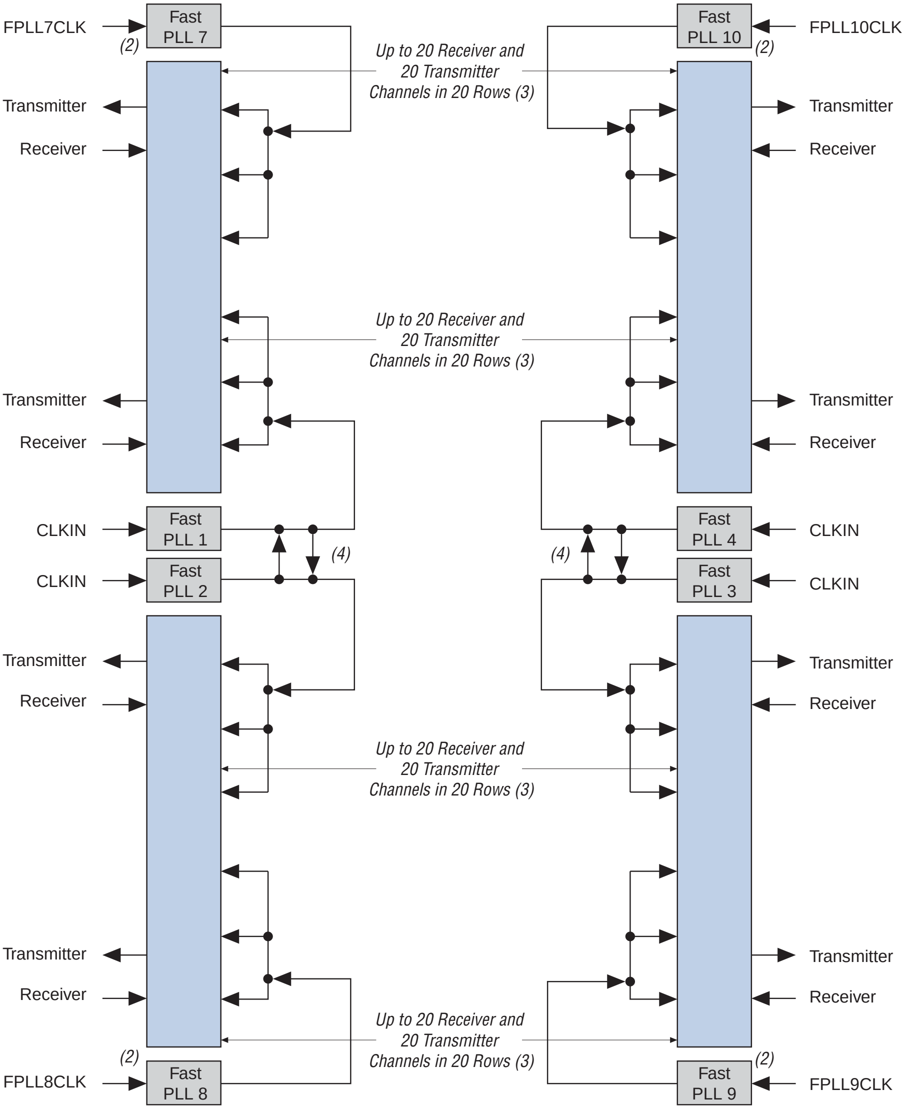
*Figure 2–85. Fast PLL & Channel Layout in the EP1S10, EP1S20 or EP1S25 Devices* *Note (1)*



*Notes to Figure 2–85:*

(1) Wire-bond packages only support up to 462 Mbps until characterization shows otherwise.
(2) See Table 2–42 for the number of channels each device supports.
(3) There is a multiplexer here to select the PLL clock source. If a PLL uses this multiplexer to clock channels outside of its bank quadrant, those clocked channels support up to 462 Mbps. For example, if PLL 2 clocks PLL 1's channel region, then those channels support up to 462 Mbps.

***Figure 2–86. Fast PLL & Channel Layout in the EP1S30 to EP1S80 Devices*** *Note (1)*



*Notes to Figure 2–86:*

(1) Wire-bond packages only support up to 462 Mbps until characterization shows otherwise.

(2) For EP1S80 devices, the fast PLLs located at the corners of the device support up to 462 Mbps.

(3) See Tables 2–43 through 2–46 for the number of channels each device supports.

(4) There is a multiplexer here to select the PLL clock source. If a PLL uses this multiplexer to clock channels outside of its bank quadrant, those clocked channels support up to 462 Mbps. For example, if PLL 2 clocks PLL 1's channel region, then those channels support up to 462 Mbps.

The transmitter external clock output is transmitted on a data channel. The `txclk` pin for each bank is located in between data transmitter pins. For ×1 clocks (e.g., 622 Mbps, 622 MHz), the high-speed PLL clock bypasses the SERDES to drive the output pins. For half-rate clocks (e.g., 622 Mbps, 311 MHz) or any other even-numbered factor such as 1/4, 1/7, 1/8, or 1/10, the SERDES automatically generates the clock in the Quartus II software.

For systems that require more than four or eight high-speed differential I/O clock domains, a SERDES bypass implementation is possible using IOEs.

### Byte Alignment

For high-speed source synchronous interfaces such as POS-PHY 4, XSBI, RapidIO, and HyperTransport, the source synchronous clock rate is not a byte- or SERDES-rate multiple of the data rate. Byte alignment is necessary for these protocols since the source synchronous clock does not provide a byte or word boundary since the clock is one half the data rate, not one eighth. The Stratix device's high-speed differential I/O circuitry provides dedicated data realignment circuitry for user-controlled byte boundary shifting. This simplifies designs while saving LE resources. An input signal to each fast PLL can stall deserializer parallel data outputs by one bit period. The designer can use an LE-based state machine to signal the shift of receiver byte boundaries until a specified pattern is detected to indicate byte alignment.

## Power Sequencing & Hot Socketing

Because Stratix devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. Therefore, the `VCCIO` and `VCCINT` power supplies may be powered in any order.

Signals can be driven into Stratix devices before and during power up without damaging the device. In addition, Stratix devices do not drive out during power up. Once operating conditions are reached and the device is configured, Stratix devices operate as specified by the user.

# 3. Configuration & Testing

S51003-1.0

Chapter 3, Configuration & Testing, replaces the Stratix Family Data Sheet.

## IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All Stratix devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1a-1990 specification. JTAG boundary-scan testing can be performed either before or after, but not during configuration. Stratix devices can also use the JTAG port for configuration together with either the Quartus II software or hardware using either Jam Files (**.jam**) or Jam Byte-Code Files (**.jbc**).

Stratix devices support IOE I/O standard setting reconfiguration through the JTAG BST chain. The JTAG chain can update the I/O standard for all input and output pins any time before or during user mode through the `CONFIG_IO` instruction. Designers can use this ability for JTAG testing before configuration when some of the Stratix pins drive or receive from other devices on the board using voltage-referenced standards. Since the Stratix device may not be configured before JTAG testing, the I/O pins may not be configured for appropriate electrical standards for chip-to-chip communication. Programming those I/O standards via JTAG allows designers to fully test I/O connection to other devices.

The enhanced PLL reconfiguration bits are part of the JTAG chain before configuration and after power-up. After device configuration, the PLL reconfiguration bits are not part of the JTAG chain.

The JTAG pins support 1.5-V/1.8-V or 2.5-V/3.3-V I/O standards. The `TDO` pin voltage is determined by the $V_{CCIO}$ of the bank where it resides. The `VCCSEL` pin selects whether the JTAG inputs are 1.5-V, 1.8-V, 2.5-V, or 3.3-V compatible.

Stratix devices also use the JTAG port to monitor the logic operation of the device with the SignalTap embedded logic analyzer. Stratix devices support the JTAG instructions shown in Table 3–1.

*Table 3–1. Stratix JTAG Instructions*

| JTAG Instruction | Instruction Code | Description |
|---|---|---|
| `SAMPLE/PRELOAD` | `00 0000 0101` | Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap embedded logic analyzer. |
| `EXTEST` *(1)* | `00 0000 0000` | Allows the external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins. |
| `BYPASS` | `11 1111 1111` | Places the 1-bit bypass register between the `TDI` and `TDO` pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation. |
| `USERCODE` | `00 0000 0111` | Selects the 32-bit USERCODE register and places it between the `TDI` and `TDO` pins, allowing the USERCODE to be serially shifted out of `TDO`. |
| `IDCODE` | `00 0000 0110` | Selects the IDCODE register and places it between `TDI` and `TDO`, allowing the IDCODE to be serially shifted out of `TDO`. |
| `HIGHZ` *(1)* | `00 0000 1011` | Places the 1-bit bypass register between the `TDI` and `TDO` pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins. |
| `CLAMP` *(1)* | `00 0000 1010` | Places the 1-bit bypass register between the `TDI` and `TDO` pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding I/O pins to a state defined by the data in the boundary-scan register. |
| ICR instructions | | Used when configuring an Stratix device via the JTAG port with a MasterBlaster™, ByteBlasterMV™, or ByteBlaster™ II download cable, or when using a Jam File or Jam Byte-Code File via an embedded processor or JRunner. |
| `PULSE_NCONFIG` | `00 0000 0001` | Emulates pulsing the `nCONFIG` pin low to trigger reconfiguration even though the physical pin is unaffected. |
| `CONFIG_IO` | `00 0000 1101` | Allows configuration of I/O standards through the JTAG chain for JTAG testing. Can be executed before, after, or during configuration. Stops configuration if executed during configuration. Once issued, the `CONFIG_IO` instruction will hold `nSTATUS` low to reset the configuration device. `nSTATUS` is held low until the device is reconfigured. |
| SignalTap instructions | | Monitors internal device operation with the SignalTap II embedded logic analyzer. |

*Note to Table 3–1:*

(1) Bus hold and weak pull-up resistor features override the high-impedance state of `HIGHZ`, `CLAMP`, and `EXTEST`.

The Stratix device instruction register length is 10 bits and the USERCODE register length is 32 bits. Tables 3–2 and 3–3 show the boundary-scan register length and device IDCODE information for Stratix devices.

*Table 3–2. Stratix Boundary-Scan Register Length*

| Device | Boundary-Scan Register Length |
|---|---|
| EP1S10 | 1,317 |
| EP1S20 | 1,797 |
| EP1S25 | 2,157 |
| EP1S30 | 2,253 |
| EP1S40 | 2,529 |
| EP1S60 | 3,129 |
| EP1S80 | 3,777 |

*Table 3–3. 32-Bit Stratix Device IDCODE*

| Device | IDCODE (32 Bits) *(2)* | | | |
|---|---|---|---|---|
| | Version (4 Bits) | Part Number (16 Bits) | Manufacturer Identity (11 Bits) | LSB (1 Bit) *(3)* |
| EP1S10 | `0000` | `0010 0000 0000 0001` | `000 0110 1110` | `1` |
| EP1S20 | `0000` | `0010 0000 0000 0010` | `000 0110 1110` | `1` |
| EP1S25 | `0000` | `0010 0000 0000 0011` | `000 0110 1110` | `1` |
| EP1S30 | `0000` | `0010 0000 0000 0100` | `000 0110 1110` | `1` |
| EP1S40 | `0000` | `0010 0000 0000 0101` | `000 0110 1110` | `1` |
| EP1S60 | `0000` | `0010 0000 0000 0110` | `000 0110 1110` | `1` |
| EP1S80 | `0000` | `0010 0000 0000 0111` | `000 0110 1110` | `1` |

***Notes to Tables 3–2 and 3–3:***

(1) Contact Altera Applications for up-to-date information on this device.

(2) The most significant bit (MSB) is on the left.

(3) The IDCODE's least significant bit (LSB) is always 1.

Figure 3–1 shows the timing requirements for the JTAG signals.

*Figure 3–1. Stratix JTAG Waveforms*

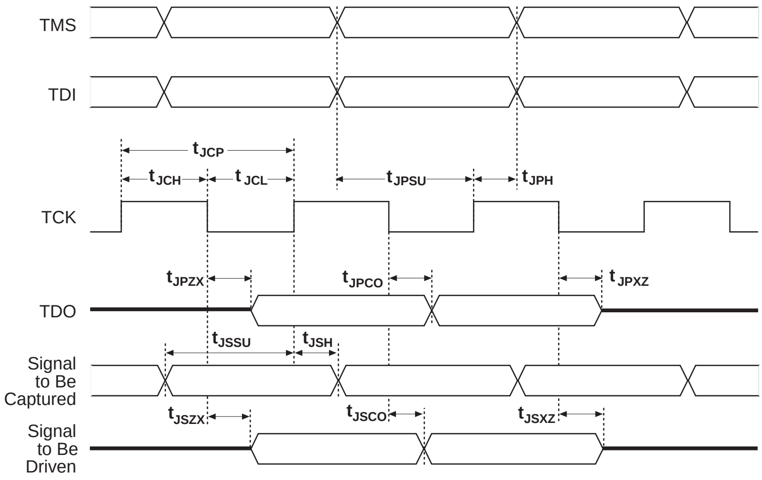


Table 3–4 shows the JTAG timing parameters and values for Stratix devices.

*Table 3–4. Stratix JTAG Timing Parameters & Values*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{JCP}$ | `TCK` clock period | 100 | | ns |
| $t_{JCH}$ | `TCK` clock high time | 50 | | ns |
| $t_{JCL}$ | `TCK` clock low time | 50 | | ns |
| $t_{JPSU}$ | JTAG port setup time | 20 | | ns |
| $t_{JPH}$ | JTAG port hold time | 45 | | ns |
| $t_{JPCO}$ | JTAG port clock to output | | 25 | ns |
| $t_{JPZX}$ | JTAG port high impedance to valid output | | 25 | ns |
| $t_{JPXZ}$ | JTAG port valid output to high impedance | | 25 | ns |
| $t_{JSSU}$ | Capture register setup time | 20 | | ns |
| $t_{JSH}$ | Capture register hold time | 45 | | ns |
| $t_{JSCO}$ | Update register clock to output | | 35 | ns |
| $t_{JSZX}$ | Update register high impedance to valid output | | 35 | ns |
| $t_{JSXZ}$ | Update register valid output to high impedance | | 35 | ns |

For more information on JTAG, see the following documents:

- *AN 39: IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices*
- *Jam Programming & Test Language Specification*

## SignalTap Embedded Logic Analyzer

Stratix devices feature the SignalTap embedded logic analyzer, which monitors design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry. A designer can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages, such as FineLine BGA packages, because it can be difficult to add a connection to a pin during the debugging process after a board is designed and manufactured.

## Configuration

The logic, circuitry, and interconnects in the Stratix architecture are configured with CMOS SRAM elements. Stratix devices are reconfigurable and are 100% tested prior to shipment. As a result, the designer does not have to generate test vectors for fault coverage purposes, and can instead focus on simulation and design verification. In addition, the designer does not need to manage inventories of different ASIC designs. Stratix devices can be configured on the board for the specific functionality required.

Stratix devices are configured at system power-up with data stored in an Altera serial configuration device or provided by a system controller. Altera offers in-system programmability (ISP)-capable configuration devices that configure Stratix devices via a serial data stream. Stratix devices can be configured in under 100 ms using 8-bit parallel data at 100 MHz. The Stratix device's optimized interface allows microprocessors to configure it serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat Stratix devices as memory and configure them by writing to a virtual memory location, making reconfiguration easy. After a Stratix device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Real-time changes can be made during system operation, enabling innovative reconfigurable computing applications.

### Operating Modes

The Stratix architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called command mode. Normal device operation is called user mode.

SRAM configuration elements allow Stratix devices to be reconfigured in-circuit by loading new configuration data into the device. With real-time reconfiguration, the device is forced into command mode with a device pin. The configuration process loads different configuration data, reinitializes the device, and resumes user-mode operation. Designers can perform in-field upgrades by distributing new configuration files either within the system or remotely.

`PORSEL` is a dedicated input pin used to select POR delay times of 2 ms or 100 ms during power-up. When the `PORSEL` pin is connected to ground, the POR time is 100 ms; when the `PORSEL` pin is connected to $V_{CC}$, the POR time is 2 ms.

The `nIO_PULLUP` pin enables a built-in weak pull-up resistor to pull all user I/O pins to $V_{CCIO}$ before and during device configuration. If `nIO_PULLUP` is connected to $V_{CC}$ during configuration, the weak pull-ups on all user I/O pins are disabled. If connected to ground, the pull-ups are enabled during configuration. The `nIO_PULLUP` pin can be pulled to 1.5, 1.8, 2.5, or 3.3 V for a logic level high.

`VCCSEL` is a dedicated input that is used to choose whether all dedicated configuration and JTAG input pins can accept 1.5 V/1.8 V or 2.5 V/3.3 V during configuration. A logic low sets 3.3 V/2.5 V, and a logic high sets 1.8 V/1.5 V. `VCCSEL` affects the following pins: `TDI`, `TMS`, `TCK`, `TRST`, `MSEL0`, `MSEL1`, `MSEL2`, `nCONFIG`, `nCE`, `DCLK`, `PLL_ENA`, `CONF_DONE`, `nSTATUS`. The `VCCSEL` pin can be pulled to 1.5, 1.8, 2.5, or 3.3 V for a logic level high.

The $V_{CCSEL}$ signal does not control any of the dual-purpose pins, including the dual-purpose configuration pins. During configuration, the output buffers of dual-purpose pins will drive out a 1.5-V TTL compatible signal while the input buffers will receive 3.3-V TTL. After configuration, the dual-purpose pins inherit the I/O standards specified in the design.

The VCCSEL signal does not control the dual-purpose configuration pins such as the `DATA[7..0]` and PPA pins (`nWS`, `nRS`, `CS`, `nCS`, and `RDYnBSY`). During configuration, these dual-purpose pins will drive out voltage levels corresponding to the $V_{CCIO}$ supply voltage that powers the I/O bank containing the pin. After configuration, the dual-purpose pins use I/O standards specified in the user design.

`TDO` and `nCEO` drive out at the same voltages as the $V_{CCIO}$ supply that powers the I/O bank containing the pin. Users must select the $V_{CCIO}$ supply for bank containing `TDO` accordingly. For example, when using the ByteBlasterMV cable, the $V_{CCIO}$ for the bank containing `TDO` must be powered up at 3.3 V.

## Configuring Stratix FPGAs with JRunner

JRunner is a software driver that configures Altera FPGAs, including Stratix FPGAs, through the ByteBlaster II or ByteBlasterMV cables in JTAG mode. The programming input file supported is in Raw Binary File (**.rbf**) format. JRunner also requires a Chain Description File (**.cdf**) generated by the Quartus II software. JRunner is targeted for embedded JTAG configuration. The source code is developed for the Windows NT operating system (OS), but can be customized to run on other platforms. For more information on the JRunner software driver, see the JRunner Software Driver: An Embedded Solution to the JTAG Configuration White Paper and the source files on the Altera web site (www.altera.com).

## Configuration Schemes

Designers can load the configuration data for a Stratix device with one of five configuration schemes (see Table 3–5), chosen on the basis of the target application. Designers can use a configuration device, intelligent controller, or the JTAG port to configure a Stratix device. A configuration device can automatically configure a Stratix device at system power-up.

Multiple Stratix devices can be configured in any of five configuration schemes by connecting the configuration enable (`nCE`) and configuration enable output (`nCEO`) pins on each device.

*Table 3–5. Data Sources for Configuration*

| Configuration Scheme | Data Source |
|---|---|
| Configuration device | Enhanced or EPC2 configuration device |
| Passive serial (PS) | MasterBlaster, ByteBlasterMV, or ByteBlaster II download cable or serial data source |
| Passive parallel asynchronous (PPA) | Parallel data source |
| Fast passive parallel | Parallel data source |
| JTAG | MasterBlaster, ByteBlasterMV, or ByteBlaster II download cable, a microprocessor with a Jam or JBC file, or JRunner |

## Partial Reconfiguration

The enhanced PLLs within the Stratix device family support partial reconfiguration of their multiply, divide, and time delay settings without reconfiguring the entire device. Designers can use either serial data from the logic array or regular I/O pins to program the PLL's counter settings in a serial chain. This option provides considerable flexibility for frequency synthesis, allowing real-time variation of the PLL frequency and delay. The rest of the device is functional while reconfiguring the PLL. See "Enhanced PLLs" on page 2–84 for more information on Stratix PLLs.

## Remote Update Configuration Modes

Stratix devices also support remote configuration using an Altera enhanced configuration device (e.g., EPC16, EPC8, and EPC4 devices) with page mode selection. Factory configuration data is stored in the default page of the configuration device. This is the default configuration which contains the design required to control remote updates and handle or recover from errors. The designer writes the factory configuration once into the flash memory or configuration device. Remote update data can update any of the remaining pages of the configuration device. If there is an error or corruption in a remote update configuration, the configuration device reverts back to the factory configuration information.

There are two remote configuration modes: remote and local configuration. Designers can use the remote update configuration mode for all three configuration modes: serial, parallel synchronous, and parallel asynchronous. Configuration devices (e.g., EPC16 devices) only support serial and parallel synchronous modes. Asynchronous parallel mode allows remote updates when an intelligent host is used to configure the Stratix device. This host must support page mode settings similar to an EPC16 device.

### *Remote Update Mode*

When the Stratix device is first powered up in remote update programming mode, it loads the configuration located at page address "`000`." The factory configuration should always be located at page address "`000`," and should never be remotely updated. The factory configuration contains the required logic to perform the following operations:

- Determine the page address/load location for the next application's configuration data
- Recover from a previous configuration error

- Receive new configuration data and write it into the configuration device

The factory configuration is the default and takes control if an error occurs while loading the application configuration.

While in the factory configuration, the factory-configuration logic performs the following operations:

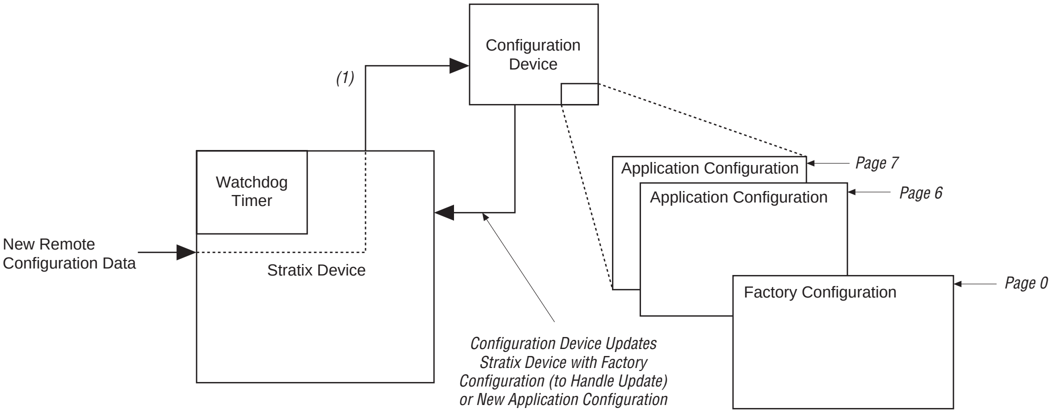
- Loads a remote update-control register to determine the page address of the new application configuration
- Determines whether to enable a user watchdog timer for the application configuration
- Determines what the watchdog timer setting should be if it is enabled

The user watchdog timer is a counter that must be continually reset within a specific amount of time in the user mode of an application configuration to ensure that valid configuration occurred during a remote update. Only valid application configurations designed for remote update can reset the user watchdog timer in user mode. If a valid application configuration does not reset the user watchdog timer in a specific amount of time, the timer updates a status register and loads the factory configuration. The user watchdog timer is automatically disabled for factory configurations.

If an error occurs in loading the application configuration, the configuration logic writes a status register to specify the cause of the error. Once this occurs, the Stratix device automatically loads the factory configuration, which reads the status register and determines the reason for reconfiguration. Based on the reason, the factory configuration will take appropriate steps and will write the remote update control register to specify the next application configuration page to be loaded.

When the Stratix device successfully loads the application configuration, it enters into user mode. The Stratix device then executes the main application of the user. Intellectual property (IP), such as a Nios® embedded processor, can help the Stratix device determine when remote update is coming. The Nios embedded processor or user logic receives incoming data, writes it to the configuration device, and loads the factory configuration. The factory configuration will read the remote update status register and determine the valid application configuration to load. Figure 3–2 shows the Stratix remote update. Figure 3–3 shows the transition diagram for remote update mode.

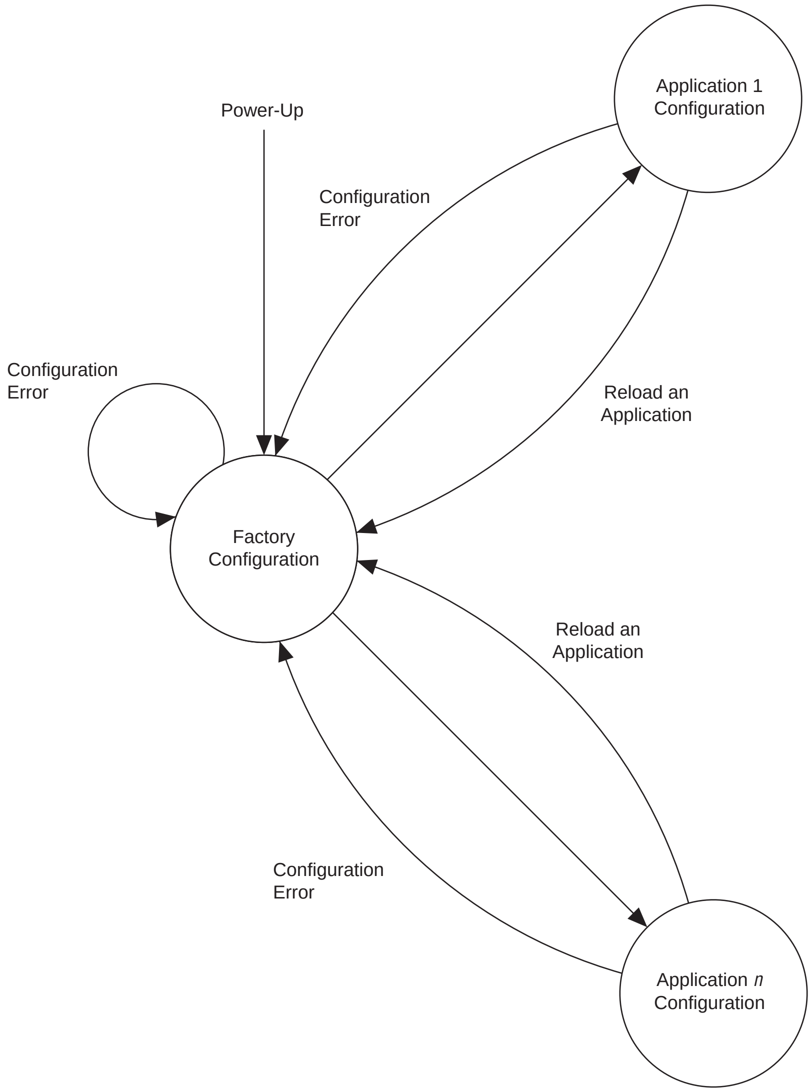
*Figure 3–2. Stratix Device Remote Update*



*Note to Figure 3–2:*

(1) When the Stratix device is configured with the factory configuration, it can handle update data from EPC16, EPC8, or EPC4 configuration device pages and point to the next page in the configuration device.

*Figure 3–3. Remote Update Transition Diagram* *Notes (1), (2)*



*Notes to Figure 3–3:*

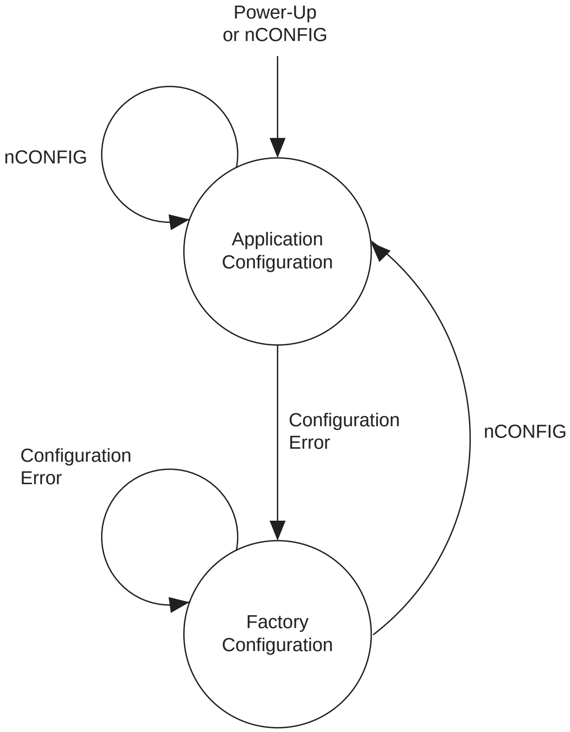
(1) Remote update of Application Configuration is controlled by a Nios embedded processor or user logic programmed in the Factory or Application configurations.

(2) Up to seven pages can be specified allowing up to seven different configuration applications.

### *Local Update Mode*

Local update mode is a simplified version of the remote update. This feature is intended for simple systems that need to load a single application configuration immediately upon power up without loading the factory configuration first. Local update designs have only one application configuration to load, so it does not require a factory configuration to determine which application configuration to use. Figure 3–4 shows the transition diagram for local update mode.

***Figure 3–4. Local Update Transition Diagram***



## Temperature Sensing Diode

Stratix devices include a diode-connected transistor for use as a temperature sensor in power management. This diode is used with an external digital thermometer device such as a MAX1617A or MAX1619 from MAXIM Integrated Products. These devices steer bias current through the Stratix diode, measuring forward voltage and converting this reading to temperature in the form of an 8-bit signed number (7 bits plus sign). The external device's output represents the package temperature of the Stratix device and can be used for intelligent power management.

The diode requires two pins (`tempdiodep` and `tempdioden`) on the Stratix device to connect to the external temperature-sensing device, as shown in Figure 3–5. The temperature sensing diode is a passive element and therefore can be used before the Stratix device is powered.

*Figure 3–5. External Temperature-Sensing Diode*

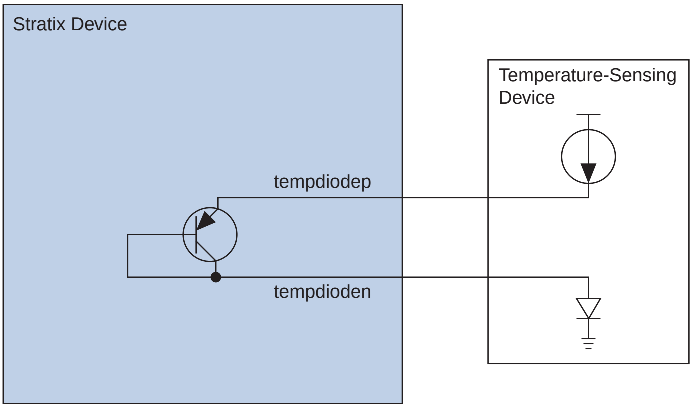


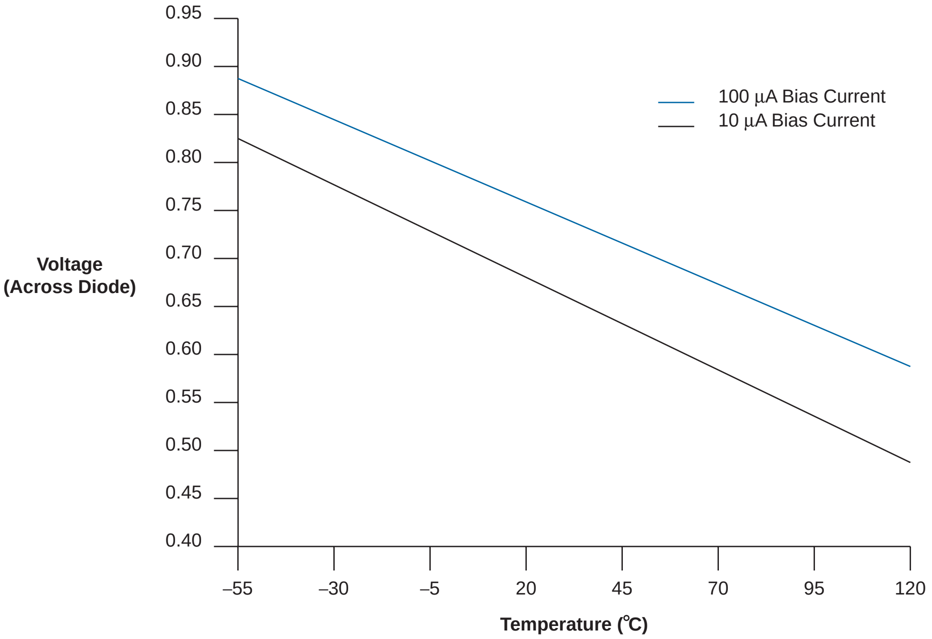
Table 3–6 shows the specifications for bias voltage and current of the Stratix temperature sensing diode.

*Table 3–6. Temperature-Sensing Diode Electrical Characteristics*

| Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|
| $I_{BIAS}$ high | 80 | 100 | 120 | µA |
| $I_{BIAS}$ low | 8 | 10 | 12 | µA |
| $V_{BP} - V_{BN}$ | 0.3 | | 0.9 | V |
| $V_{BN}$ | | 0.7 | | V |
| Series resistance | | | 3 | W |

The temperature-sensing diode works for the entire operating range shown in Figure 3–6.

*Figure 3–6. Temperature vs. Temperature-Sensing Diode Voltage*



# 4. DC & Switching Characteristics

S51004-1.1

Chapter 4, DC & Switching Characteristics, replaces the Stratix Family Data Sheet.

## Operating Conditions

Stratix devices are offered in both commercial and industrial grades. However, industrial-grade devices may have limited speed-grade availability.

Tables 4–1 through 4–32 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 1.5-V Stratix devices.

*Table 4–1. Stratix Device Absolute Maximum Ratings* *Notes (1), (2)*

| Symbol | Parameter | Conditions | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage | With respect to ground | –0.5 | 2.4 | V |
| $V_{CCIO}$ | | | –0.5 | 4.6 | V |
| $V_I$ | DC input voltage *(3)* | | –0.5 | 4.6 | V |
| $I_{OUT}$ | DC output current, per pin | | –25 | 40 | mA |
| $T_{STG}$ | Storage temperature | No bias | –65 | 150 | °C |
| $T_J$ | Junction temperature | BGA packages under bias | | 135 | °C |

*Table 4–2. Stratix Device Recommended Operating Conditions (Part 1 of 2)*

| Symbol | Parameter | Conditions | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | *(4)* | 1.425 | 1.575 | V |
| $V_{CCIO}$ | Supply voltage for output buffers, 3.3-V operation | *(4)*, *(5)* | 3.00 (3.135) | 3.60 (3.465) | V |
| | Supply voltage for output buffers, 2.5-V operation | *(4)* | 2.375 | 2.625 | V |
| | Supply voltage for output buffers, 1.8-V operation | *(4)* | 1.71 | 1.89 | V |
| | Supply voltage for output buffers, 1.5-V operation | *(4)* | 1.4 | 1.6 | V |
| $V_I$ | Input voltage | *(3)*, *(6)* | –0.5 | 4.1 | V |

*Table 4–2. Stratix Device Recommended Operating Conditions (Part 2 of 2)*

| Symbol | Parameter | Conditions | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_J$ | Operating junction temperature | For commercial use | 0 | 85 | °C |
| | | For industrial use | –40 | 100 | °C |
| $t_R$ | Input rise time | | | 40 | ns |
| $t_F$ | Input fall time | | | 40 | ns |

*Table 4–3. Stratix Device DC Operating Conditions* *Note (7)*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $I_I$ | Input pin leakage current | $V_I = V_{CCIOmax}$ to 0 V *(8)* | –10 | | 10 | µA |
| $I_{OZ}$ | Tri-stated I/O pin leakage current | $V_O = V_{CCIOmax}$ to 0 V *(8)* | –10 | | 10 | µA |
| $I_{CC0}$ | $V_{CC}$ supply current (standby) (All memory blocks in power-down mode) | $V_I$ = ground, no load, no toggling inputs | | | | mA |
| $R_{CONF}$ | Value of I/O pin pull-up resistor before and during configuration | $V_{CCIO}$ = 3.0 V *(9)* | 20 | | 50 | kΩ |
| | | $V_{CCIO}$ = 2.375 V *(9)* | 30 | | 80 | kΩ |
| | | $V_{CCIO}$ = 1.71 V *(9)* | 60 | | 150 | kΩ |

*Table 4–4. LVTTL Specifications*

| Symbol | Parameter | Conditions | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 3.0 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | 1.7 | 4.1 | V |
| $V_{IL}$ | Low-level input voltage | | –0.5 | 0.7 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –4 to –24 mA *(10)* | 2.4 | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 4 to 24 mA *(10)* | | 0.45 | V |

### Table 4–5. LVCMOS Specifications

| Symbol | Parameter | Conditions | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 3.0 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | 1.7 | 4.1 | V |
| $V_{IL}$ | Low-level input voltage | | –0.5 | 0.7 | V |
| $V_{OH}$ | High-level output voltage | $V_{CCIO}$ = 3.0,<br>$I_{OH}$ = –0.1 mA | $V_{CCIO}$ – 0.2 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CCIO}$ = 3.0,<br>$I_{OL}$ = 0.1 mA | | 0.2 | V |

### Table 4–6. 2.5-V I/O Specifications

| Symbol | Parameter | Conditions | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 2.375 | 2.625 | V |
| $V_{IH}$ | High-level input voltage | | 1.7 | 4.1 | V |
| $V_{IL}$ | Low-level input voltage | | –0.5 | 0.7 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –0.1 mA | 2.1 | | V |
| | | $I_{OH}$ = –1 mA | 2.0 | | V |
| | | $I_{OH}$ = –2 to –16 mA *(10)* | 1.7 | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 0.1 mA | | 0.2 | V |
| | | $I_{OL}$ = 1 mA | | 0.4 | V |
| | | $I_{OL}$ = 2 to 16 mA *(10)* | | 0.7 | V |

### Table 4–7. 1.8-V I/O Specifications

| Symbol | Parameter | Conditions | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 1.65 | 1.95 | V |
| $V_{IH}$ | High-level input voltage | | 0.65 × $V_{CCIO}$ | 2.25 | V |
| $V_{IL}$ | Low-level input voltage | | –0.3 | 0.35 × $V_{CCIO}$ | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –2 to –8 mA *(10)* | $V_{CCIO}$ – 0.45 | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 2 to 8 mA *(10)* | | 0.45 | V |

### Table 4–8. 1.5-V I/O Specifications

| Symbol | Parameter | Conditions | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage |  | 1.4 | 1.6 | V |
| $V_{IH}$ | High-level input voltage |  | 0.65 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | V |
| $V_{IL}$ | Low-level input voltage |  | –0.3 | 0.35 × $V_{CCIO}$ | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –2 mA *(10)* | 0.75 × $V_{CCIO}$ |  | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 2 mA *(10)* |  | 0.25 × $V_{CCIO}$ | V |

***Notes to Tables 4–1 through 4–8:***

(1) See the *Operating Requirements for Altera Devices Data Sheet*.

(2) Conditions beyond those listed in Table 4–1 may cause permanent damage to a device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse affects on the device.

(3) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2 V or overshoot to 4.6 V for input currents less than 100 mA and periods shorter than 20 ns.

(4) Maximum $V_{CC}$ rise time is 100 ms, and $V_{CC}$ must rise monotonically.

(5) $V_{CCIO}$ maximum and minimum conditions for LVPECL, LVDS, and 3.3-V PCML are shown in parentheses.

(6) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before $V_{CCINT}$ and $V_{CCIO}$ are powered.

(7) Typical values are for $T_A$ = 25°C, $V_{CCINT}$ = 1.5 V, and $V_{CCIO}$ = 1.5 V, 1.8 V, 2.5 V, and 3.3 V.

(8) This value is specified for normal device operation. The value may vary during power-up. This applies for all $V_{CCIO}$ settings (3.3, 2.5, 1.8, and 1.5 V)

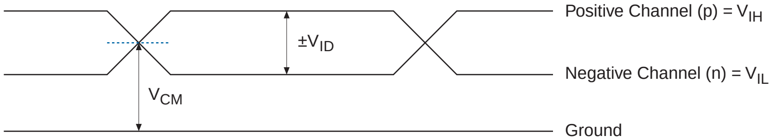
(9) Pin pull-up resistance values will lower if an external source drives the pin higher than $V_{CCIO}$.

(10) Drive strength is programmable according to values in Table 2–36 on page 2–127.

Figures 4–1 and 4–2 show receiver input and transmitter output waveforms, respectively, for all differential I/O standards (LVDS, 3.3-V PCML, LVPECL, and HyperTransport technology).

### Figure 4–1. Receiver Input Waveforms for Differential I/O Standards

**Single-Ended Waveform**



**Differential Waveform**

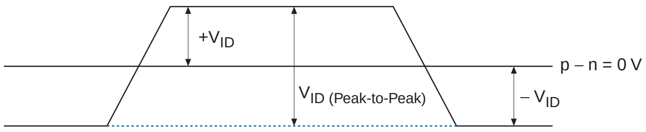
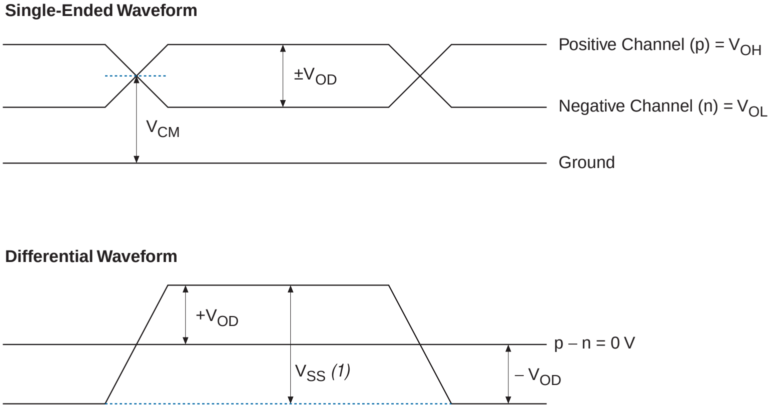


Figure 4–2. Transmitter Output Waveforms for Differential I/O Standards



*Note to Figure 4–2:*

(1) $V_{SS}$: steady-state differential output voltage.

Table 4–9. 3.3-V LVDS I/O Specifications (Part 1 of 2)

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | I/O supply voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{ID}$ | Input differential voltage swing | 0.1 V < $V_{CM}$ < 1.1 V<br>*J* = 1 through 10 | 300 | | 1,000 | mV |
| | | 1.1 V ≤ $V_{CM}$ ≤ 1.6 V<br>*J* = 1 | 200 | | 1,000 | mV |
| | | 1.1 V ≤ $V_{CM}$ ≤ 1.6 V<br>*J* = 2 through10 | 100 | | 1,000 | mV |
| | | 1.6 V < $V_{CM}$ < 1.8 V<br>*J* = 1 through 10 | 300 | | 1,000 | mV |

***Table 4–9. 3.3-V LVDS I/O Specifications (Part 2 of 2)***

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{ICM}$ | Input common mode voltage | LVDS<br>$0.3\text{ V} < V_{ID} < 1.0\text{ V}$<br>$J = 1$ through 10 | 100 | | 1,100 | mV |
| | | LVDS<br>$0.3\text{ V} < V_{ID} < 1.0\text{ V}$<br>$J = 1$ through 10 | 1,600 | | 1,800 | mV |
| | | LVDS<br>$0.2\text{ V} < V_{ID} < 1.0\text{ V}$<br>$J = 1$ | 1,100 | | 1,600 | mV |
| | | LVDS<br>$0.1\text{ V} < V_{ID} < 1.0\text{ V}$<br>$J = 2$ through 10 | 1,100 | | 1,600 | mV |
| $V_{OD}$ *(1)* | Output differential voltage | $R_L = 100\ \Omega$ | 250 | 375 | 550 | mV |
| $\Delta V_{OD}$ | Change in $V_{OD}$ between high and low | $R_L = 100\ \Omega$ | | | 50 | mV |
| $V_{OCM}$ | Output common mode voltage | $R_L = 100\ \Omega$ | 1,125 | 1,200 | 1,375 | mV |
| $\Delta V_{OCM}$ | Change in $V_{OCM}$ between high and low | $R_L = 100\ \Omega$ | | | 50 | mV |
| $R_L$ | Receiver differential input resistor | | 90 | 100 | 110 | $\Omega$ |

*Table 4–10. 3.3-V PCML Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | I/O supply voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{ID}$ | Input differential voltage swing | | 300 | | 600 | mV |
| $V_{ICM}$ | Input common mode voltage | | 1.5 | | 3.465 | V |
| $V_{OD}$ | Output differential voltage | | 300 | 370 | 500 | mV |
| $\Delta$ $V_{OD}$ | Change in $V_{OD}$ between high and low | | | | 50 | mV |
| $V_{OCM}$ | Output common mode voltage | | 2.5 | 2.85 | 3.3 | V |
| $\Delta$ $V_{OCM}$ | Change in $V_{OCM}$ between high and low | | | | 50 | mV |
| $V_T$ | Output termination voltage | | | $V_{CCIO}$ | | V |
| $R_1$ | Output external pull-up resistors | | 45 | 50 | 55 | Ω |
| $R_2$ | Output external pull-up resistors | | 45 | 50 | 55 | Ω |

*Table 4–11. LVPECL Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | I/O supply voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{ID}$ | Input differential voltage swing | | 300 | | 1,000 | mV |
| $V_{ICM}$ | Input common mode voltage | | 1 | | 2 | V |
| $V_{OD}$ | Output differential voltage | $R_L$ = 100 Ω | 525 | 700 | 970 | mV |
| $V_{OCM}$ | Output common mode voltage | $R_L$ = 100 Ω | 1.5 | 1.7 | 1.9 | V |
| $R_L$ | Receiver differential input resistor | | 90 | 100 | 110 | Ω |

*Table 4–12. HyperTransport Technology Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | I/O supply voltage | | 2.375 | 2.5 | 2.625 | V |
| $V_{ID}$ | Input differential voltage swing | | 300 | | 900 | mV |
| $V_{ICM}$ | Input common mode voltage | | 300 | | 900 | mV |
| $V_{OD}$ | Output differential voltage | $R_L = 100\ \Omega$ | 380 | 485 | 820 | mV |
| $\Delta V_{OD}$ | Change in $V_{OD}$ between high and low | $R_L = 100\ \Omega$ | | | 50 | mV |
| $V_{OCM}$ | Output common mode voltage | $R_L = 100\ \Omega$ | 440 | 650 | 780 | mV |
| $\Delta V_{OCM}$ | Change in $V_{OCM}$ between high and low | $R_L = 100\ \Omega$ | | | 50 | mV |
| $R_L$ | Receiver differential input resistor | | 90 | 100 | 110 | Ω |

*Table 4–13. 3.3-V PCI Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 3.0 | 3.3 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | $0.5 \times V_{CCIO}$ | | $V_{CCIO} + 0.5$ | V |
| $V_{IL}$ | Low-level input voltage | | –0.5 | | $0.3 \times V_{CCIO}$ | V |
| $V_{OH}$ | High-level output voltage | $I_{OUT} = -500\ \mu A$ | $0.9 \times V_{CCIO}$ | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OUT} = 1{,}500\ \mu A$ | | | $0.1 \times V_{CCIO}$ | V |

| *Table 4–14. PCI-X 1.0 Specifications* | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Minimum** | **Typical** | **Maximum** | **Unit** |
| $V_{CCIO}$ | Output supply voltage | | 3.0 | | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | $0.5 \times V_{CCIO}$ | | $V_{CCIO} + 0.5$ | V |
| $V_{IL}$ | Low-level input voltage | | –0.5 | | $0.35 \times V_{CCIO}$ | V |
| $V_{IPU}$ | Input pull-up voltage | | $0.7 \times V_{CCIO}$ | | | V |
| $V_{OH}$ | High-level output voltage | $I_{OUT} = -500\ \mu A$ | $0.9 \times V_{CCIO}$ | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OUT} = 1{,}500\ \mu A$ | | | $0.1 \times V_{CCIO}$ | V |

| *Table 4–15. GTL+ I/O Specifications* | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Minimum** | **Typical** | **Maximum** | **Unit** |
| $V_{TT}$ | Termination voltage | | 1.35 | 1.5 | 1.65 | V |
| $V_{REF}$ | Reference voltage | | 0.88 | 1.0 | 1.12 | V |
| $V_{IH}$ | High-level input voltage | | $V_{REF} + 0.1$ | | | V |
| $V_{IL}$ | Low-level input voltage | | | | $V_{REF} - 0.1$ | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL} = 34$ mA *(3)* | | | 0.65 | V |

| *Table 4–16. GTL I/O Specifications* | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Minimum** | **Typical** | **Maximum** | **Unit** |
| $V_{TT}$ | Termination voltage | | 1.14 | 1.2 | 1.26 | V |
| $V_{REF}$ | Reference voltage | | 0.74 | 0.8 | 0.86 | V |
| $V_{IH}$ | High-level input voltage | | $V_{REF} + 0.05$ | | | V |
| $V_{IL}$ | Low-level input voltage | | | | $V_{REF} - 0.05$ | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL} = 40$ mA *(3)* | | | 0.4 | V |

*Table 4–17. SSTL-18 Class I Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 1.65 | 1.8 | 1.95 | V |
| $V_{REF}$ | Reference voltage | | 0.8 | 0.9 | 1.0 | V |
| $V_{TT}$ | Termination voltage | | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 | V |
| $V_{IH(DC)}$ | High-level DC input voltage | | $V_{REF}$ + 0.125 | | | V |
| $V_{IL(DC)}$ | Low-level DC input voltage | | | | $V_{REF}$ – 0.125 | V |
| $V_{IH(AC)}$ | High-level AC input voltage | | $V_{REF}$ + 0.275 | | | V |
| $V_{IL(AC)}$ | Low-level AC input voltage | | | | $V_{REF}$ – 0.275 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –6.7 mA *(3)* | $V_{TT}$ + 0.475 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 6.7 mA *(3)* | | | $V_{TT}$ – 0.475 | V |

*Table 4–18. SSTL-18 Class II Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 1.65 | 1.8 | 1.95 | V |
| $V_{REF}$ | Reference voltage | | 0.8 | 0.9 | 1.0 | V |
| $V_{TT}$ | Termination voltage | | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 | V |
| $V_{IH(DC)}$ | High-level DC input voltage | | $V_{REF}$ + 0.125 | | | V |
| $V_{IL(DC)}$ | Low-level DC input voltage | | | | $V_{REF}$ – 0.125 | V |
| $V_{IH(AC)}$ | High-level AC input voltage | | $V_{REF}$ + 0.275 | | | V |
| $V_{IL(AC)}$ | Low-level AC input voltage | | | | $V_{REF}$ – 0.275 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –13.4 mA *(3)* | $V_{TT}$ + 0.630 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 13.4 mA *(3)* | | | $V_{TT}$ – 0.630 | V |

### Table 4–19. SSTL-2 Class I Specifications

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 2.375 | 2.5 | 2.625 | V |
| $V_{TT}$ | Termination voltage | | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 | V |
| $V_{REF}$ | Reference voltage | | 1.15 | 1.25 | 1.35 | V |
| $V_{IH}$ | High-level input voltage | | $V_{REF}$ + 0.18 | | 3.0 | V |
| $V_{IL}$ | Low-level input voltage | | –0.3 | | $V_{REF}$ – 0.18 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –8.1 mA *(3)* | $V_{TT}$ + 0.57 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 8.1 mA *(3)* | | | $V_{TT}$ – 0.57 | V |

### Table 4–20. SSTL-2 Class II Specifications

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 2.3 | 2.5 | 2.7 | V |
| $V_{TT}$ | Termination voltage | | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 | V |
| $V_{REF}$ | Reference voltage | | 1.15 | 1.25 | 1.35 | V |
| $V_{IH}$ | High-level input voltage | | $V_{REF}$ + 0.18 | | $V_{CCIO}$ + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | | –0.3 | | $V_{REF}$ – 0.18 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –16.4 mA *(3)* | $V_{TT}$ + 0.76 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 16.4 mA *(3)* | | | $V_{TT}$ – 0.76 | V |

### Table 4–21. SSTL-3 Class I Specifications

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 3.0 | 3.3 | 3.6 | V |
| $V_{TT}$ | Termination voltage | | $V_{REF}$ – 0.05 | $V_{REF}$ | $V_{REF}$ + 0.05 | V |
| $V_{REF}$ | Reference voltage | | 1.3 | 1.5 | 1.7 | V |
| $V_{IH}$ | High-level input voltage | | $V_{REF}$ + 0.2 | | $V_{CCIO}$ + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | | –0.3 | | $V_{REF}$ – 0.2 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –8 mA *(3)* | $V_{TT}$ + 0.6 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 8 mA *(3)* | | | $V_{TT}$ – 0.6 | V |

### Table 4–22. SSTL-3 Class II Specifications

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 3.0 | 3.3 | 3.6 | V |
| $V_{TT}$ | Termination voltage | | $V_{REF} - 0.05$ | $V_{REF}$ | $V_{REF} + 0.05$ | V |
| $V_{REF}$ | Reference voltage | | 1.3 | 1.5 | 1.7 | V |
| $V_{IH}$ | High-level input voltage | | $V_{REF} + 0.2$ | | $V_{CCIO} + 0.3$ | V |
| $V_{IL}$ | Low-level input voltage | | –0.3 | | $V_{REF} - 0.2$ | V |
| $V_{OH}$ | High-level output voltage | $I_{OH} = -16$ mA *(3)* | $V_{TT} + 0.8$ | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL} = 16$ mA *(3)* | | | $V_{TT} - 0.8$ | V |

### Table 4–23. 3.3-V AGP 2× Specifications

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 3.15 | 3.3 | 3.45 | V |
| $V_{REF}$ | Reference voltage | | $0.39 \times V_{CCIO}$ | | $0.41 \times V_{CCIO}$ | V |
| $V_{IH}$ | High-level input voltage *(4)* | | $0.5 \times V_{CCIO}$ | | $V_{CCIO} + 0.5$ | V |
| $V_{IL}$ | Low-level input voltage *(4)* | | | | $0.3 \times V_{CCIO}$ | V |
| $V_{OH}$ | High-level output voltage | $I_{OUT} = -0.5$ mA | $0.9 \times V_{CCIO}$ | | 3.6 | V |
| $V_{OL}$ | Low-level output voltage | $I_{OUT} = 1.5$ mA | | | $0.1 \times V_{CCIO}$ | V |

### Table 4–24. 3.3-V AGP 1× Specifications

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 3.15 | 3.3 | 3.45 | V |
| $V_{IH}$ | High-level input voltage *(4)* | | $0.5 \times V_{CCIO}$ | | $V_{CCIO} + 0.5$ | V |
| $V_{IL}$ | Low-level input voltage *(4)* | | | | $0.3 \times V_{CCIO}$ | V |
| $V_{OH}$ | High-level output voltage | $I_{OUT} = -0.5$ mA | $0.9 \times V_{CCIO}$ | | 3.6 | V |
| $V_{OL}$ | Low-level output voltage | $I_{OUT} = 1.5$ mA | | | $0.1 \times V_{CCIO}$ | V |

### Table 4–25. 1.5-V HSTL Class I Specifications (Part 1 of 2)

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 1.4 | 1.5 | 1.6 | V |
| $V_{REF}$ | Input reference voltage | | 0.68 | 0.75 | 0.9 | V |
| $V_{TT}$ | Termination voltage | | 0.7 | 0.75 | 0.8 | V |

*Table 4–25. 1.5-V HSTL Class I Specifications (Part 2 of 2)*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ (DC) | DC high-level input voltage | | $V_{REF}$ + 0.1 | | | V |
| $V_{IL}$ (DC) | DC low-level input voltage | | –0.3 | | $V_{REF}$ – 0.1 | V |
| $V_{IH}$ (AC) | AC high-level input voltage | | $V_{REF}$ + 0.2 | | | V |
| $V_{IL}$ (AC) | AC low-level input voltage | | | | $V_{REF}$ – 0.2 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = 8 mA *(3)* | $V_{CCIO}$ – 0.4 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OH}$ = –8 mA *(3)* | | | 0.4 | V |

*Table 4–26. 1.5-V HSTL Class II Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 1.4 | 1.5 | 1.6 | V |
| $V_{REF}$ | Input reference voltage | | 0.68 | 0.75 | 0.9 | V |
| $V_{TT}$ | Termination voltage | | 0.7 | 0.75 | 0.8 | V |
| $V_{IH}$ (DC) | DC high-level input voltage | | $V_{REF}$ + 0.1 | | | V |
| $V_{IL}$ (DC) | DC low-level input voltage | | –0.3 | | $V_{REF}$ – 0.1 | V |
| $V_{IH}$ (AC) | AC high-level input voltage | | $V_{REF}$ + 0.2 | | | V |
| $V_{IL}$ (AC) | AC low-level input voltage | | | | $V_{REF}$ – 0.2 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = 16 mA *(3)* | $V_{CCIO}$ – 0.4 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OH}$ = –16 mA *(3)* | | | 0.4 | V |

*Table 4–27. 1.8-V HSTL Class I Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 1.65 | 1.80 | 1.95 | V |
| $V_{REF}$ | Input reference voltage | | 0.70 | 0.90 | 0.95 | V |
| $V_{TT}$ | Termination voltage | | | $V_{CCIO}$ × 0.5 | | V |
| $V_{IH}$ (DC) | DC high-level input voltage | | $V_{REF}$ + 0.1 | | | V |
| $V_{IL}$ (DC) | DC low-level input voltage | | –0.5 | | $V_{REF}$ – 0.1 | V |
| $V_{IH}$ (AC) | AC high-level input voltage | | $V_{REF}$ + 0.2 | | | V |
| $V_{IL}$ (AC) | AC low-level input voltage | | | | $V_{REF}$ – 0.2 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = 8 mA *(3)* | $V_{CCIO}$ – 0.4 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OH}$ = –8 mA *(3)* | | | 0.4 | V |

***Table 4–28. 1.8-V HSTL Class II Specifications***

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 1.65 | 1.80 | 1.95 | V |
| $V_{REF}$ | Input reference voltage | | 0.70 | 0.90 | 0.95 | V |
| $V_{TT}$ | Termination voltage | | | $V_{CCIO}$ × 0.5 | | V |
| $V_{IH}$ (DC) | DC high-level input voltage | | $V_{REF}$ + 0.1 | | | V |
| $V_{IL}$ (DC) | DC low-level input voltage | | –0.5 | | $V_{REF}$ – 0.1 | V |
| $V_{IH}$ (AC) | AC high-level input voltage | | $V_{REF}$ + 0.2 | | | V |
| $V_{IL}$ (AC) | AC low-level input voltage | | | | $V_{REF}$ – 0.2 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = 16 mA *(3)* | $V_{CCIO}$ – 0.4 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OH}$ = –16 mA *(3)* | | | 0.4 | V |

***Table 4–29. 1.5-V Differential HSTL Specifications***

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | I/O supply voltage | | 1.4 | 1.5 | 1.6 | V |
| $V_{DIF}$ (DC) | DC input differential voltage | | 0.2 | | | V |
| $V_{CM}$ (DC) | DC common mode input voltage | | 0.68 | | 0.9 | V |
| $V_{DIF}$ (AC) | AC differential input voltage | | 0.4 | | | V |

***Table 4–30. CTT I/O Specifications***

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 3.0 | 3.3 | 3.6 | V |
| $V_{TT}/V_{REF}$ | Termination and input reference voltage | | 1.35 | 1.5 | 1.65 | V |
| $V_{IH}$ | High-level input voltage | | $V_{REF}$ + 0.2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | $V_{REF}$ – 0.2 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –8 mA | $V_{REF}$ + 0.4 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 8 mA | | | $V_{REF}$ – 0.4 | V |
| $I_O$ | Output leakage current (when output is high *Z*) | GND ð $V_{OUT}$ ð $V_{CCIO}$ | –10 | | 10 | µA |

**Table 4–31. Bus Hold Parameters**

| Parameter | Conditions | $V_{CCIO}$ Level | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | 1.5 V | | 1.8 V | | 2.5 V | | 3.3 V | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Low sustaining current | $V_{IN} > V_{IL}$ (maximum) | | | 30 | | 50 | | 70 | | μA |
| High sustaining current | $V_{IN} < V_{IH}$ (minimum) | | | –30 | | –50 | | –70 | | μA |
| Low overdrive current | $0 V < V_{IN} < V_{CCIO}$ | | | | 200 | | 300 | | 500 | μA |
| High overdrive current | $0 V < V_{IN} < V_{CCIO}$ | | | | –200 | | –300 | | –500 | μA |

**Table 4–32. Stratix Device Capacitance** *Note (5)*

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| $C_{IOTB}$ | Input capacitance on I/O pins in I/O banks 3, 4, 7, and 8. | | 11.5 | | pF |
| $C_{IOLR}$ | Input capacitance on I/O pins in I/O banks 1, 2, 5, and 6, including high-speed differential receiver and transmitter pins. | | 8.2 | | pF |
| $C_{CLKTB}$ | Input capacitance on top/bottom clock input pins: `CLK[4:7]` and `CLK[12:15]`. | | 11.5 | | pF |
| $C_{CLKLR}$ | Input capacitance on left/right clock inputs: `CLK1`, `CLK3`, `CLK8`, `CLK10`. | | 7.8 | | pF |
| $C_{CLKLR+}$ | Input capacitance on left/right clock inputs: `CLK0`, `CLK2`, `CLK9`, and `CLK11`. | | 4.4 | | pF |

***Notes to Tables 4–9 through 4–32:***

(1) When `tx_outclock` port of `altlvds_tx` megafunction is 717 MHz, $V_{OD(min)}$ = 235 mV on the output clock pin.

(2) Pin pull-up resistance values will lower if an external source drives the pin higher than $V_{CCIO}$.

(3) Drive strength is programmable according to values in Table 2–36 on page 2–127.

(4) $V_{REF}$ specifies the center point of the switching range.

(5) Capacitance is sample-tested only. Capacitance is measured using time-domain reflections (TDR). Measurement accuracy is within ±0.5 pF.

## Power Consumption

Altera offers two ways to calculate power for a design: the Altera web power calculator and the PowerGauge™ feature in the Quartus II software.

The interactive power calculator on the Altera web site is typically used prior to designing the FPGA in order to get a magnitude estimate of the device power. The Quartus II software PowerGauge feature allows designers to apply test vectors against their design for more accurate power consumption modeling.

In both cases, these calculations should only be used as an estimation of power, not as a specification.

Stratix devices require a certain amount of power-up current to successfully power up because of the small process geometry on which they are fabricated.

Table 4–33 shows the maximum power-up current ($I_{CCINT}$) required to power a Stratix device. This specification is for commercial operating conditions. Measurments were performed with an isolated Stratix device on the board to characterize the power-up current of an isolated device. Decoupling capacitors were not used in this measurement. To factor in the current for decoupling capacitors, sum up the current for each capacitor using the following equation:

$I = C\,(dV/dt)$

If the regulator or power supply minimum output current is more than the Stratix device requires, then the device may consume more current than the maximum current listed in Table 4–33. However, the device does not require any more current to successfully power up than what is listed in Table 4–33.

*Table 4–33. Stratix Power-Up Current ($I_{CCINT}$) Requirements*

| Device | Power-Up Current Requirement | | Unit |
|---|---|---|---|
| | Typ | Max | |
| EP1S10 | 250 | 700 | mA |
| EP1S20 | 400 | 1,200 | mA |
| EP1S25 | 500 | 1,500 | mA |
| EP1S30 | 550 | 1,900 | mA |
| EP1S40 | 650 | 2,300 | mA |
| EP1S60 | 800 | 2,600 | mA |
| EP1S80 | 1,000 | 3,000 | mA |

The exact amount of current consumed varies according to the process, temperature, and power ramp rate. Stratix devices typically require less current during power up than shown in Table 4–33. The user-mode current during device operation is generally higher than the power-up current.

The duration of the $I_{CCINT}$ power-up requirement depends on the $V_{CCINT}$ voltage supply rise time. The power-up current consumption drops when the $V_{CCINT}$ supply reaches approximately 0.75 V.

# Timing Model

The DirectDrive technology and MultiTrack interconnect ensure predictable performance, accurate simulation, and accurate timing analysis across all Stratix device densities and speed grades. This section describes and specifies the performance, internal, external, and PLL timing specifications.

All specifications are representative of worst-case supply voltage and junction temperature conditions.

## Preliminary & Final Timing

Timing models can have either preliminary or final status. The Quartus II software issues an informational message during the design compilation if the timing models are preliminary. Table 4–34 shows the status of the Stratix device timing models.

Preliminary status means the timing model is subject to change. Initially, timing numbers are created using simulation results, process data, and other known parameters. These tests are used to make the preliminary numbers as close to the actual timing parameters as possible.

Final timing numbers are based on actual device operation and testing. These numbers reflect the actual performance of the device under worst-case voltage and junction temperature conditions.

*Table 4–34. Stratix Device Timing Model Status*

| Device | Preliminary | Final |
|---|---|---|
| EP1S10 | | ✓ |
| EP1S20 | | ✓ |
| EP1S25 | | ✓ |
| EP1S30 | | ✓ |
| EP1S40 | | ✓ |
| EP1S60 | ✓ | |
| EP1S80 | ✓ | |

## Performance

Table 4–35 shows Stratix performance for some common designs. All performance values were obtained with Quartus II software compilation of LPM, or MegaCore functions for the FIR and FFT designs.

*Table 4–35. Stratix Performance (Part 1 of 3)* *Note (1)*

| Resource Used | Design Size & Function | Mode | Resources Used | | | Performance (MHz) | | |
|---|---|---|---|---|---|---|---|---|
| | | | LEs | TriMatrix Memory Blocks | DSP Blocks | -5 Speed Grade | -6 Speed Grade | -7 Speed Grade |
| LE | 16-to-1 multiplexer *(2)* | | 22 | 0 | 0 | 346.74 | 302.84 | 263.71 |
| | 32-to-1 multiplexer *(2)* | | 46 | 0 | 0 | 265.18 | 233.04 | 207.16 |
| | 16-bit counter | | 16 | 0 | 0 | 422.11 | 422.11 | 390.01 |
| | 64-bit counter | | 64 | 0 | 0 | 316.05 | 293.16 | 255.42 |
| TriMatrix memory M512 block | RAM 32 × 18 bit *(2)* | Simple dual-port | 0 | 1 | 0 | 317.76 | 277.62 | 241.48 |
| | FIFO 32 × 18 bit *(2)* | | 30 | 1 | 0 | 319.18 | 278.86 | 242.54 |

*Table 4–35. Stratix Performance (Part 2 of 3) Note (1)*

| Resource Used | Design Size & Function | Mode | Resources Used | | | Performance (MHz) | | |
|---|---|---|---|---|---|---|---|---|
| | | | LEs | TriMatrix Memory Blocks | DSP Blocks | -5 Speed Grade | -6 Speed Grade | -7 Speed Grade |
| TriMatrix memory M4K block | RAM 128 × 36 bit *(2)* | Simple dual-port | 0 | 1 | 0 | 290.86 | 255.55 | 222.27 |
| | RAM 256 × 18 bit *(2)* | True dual-port | 0 | 1 | 0 | 290.86 | 255.55 | 222.27 |
| | FIFO 128 × 36 bit *(2)* | | 34 | 1 | 0 | 280.42 | 255.55 | 222.27 |
| TriMatrix memory M-RAM block | RAM 4K × 144 bit *(2)* | Simple dual-port | 0 | 1 | 0 | 255.85 | 233.06 | 194.06 |
| | | Single port | 0 | 1 | 0 | 255.85 | 233.06 | 194.06 |
| | | True dual-port | 0 | 1 | 0 | 269.83 | 237.69 | 206.82 |
| | RAM 8K × 72 bit *(2)* | Simple dual-port | 0 | 1 | 0 | 275.86 | 223.13 | 194.02 |
| | | Single port | 0 | 1 | 0 | 278.88 | 243.21 | 211.49 |
| | | True dual-port | 0 | 1 | 0 | 269.84 | 237.74 | 206.73 |
| | RAM 16K × 36 bit *(2)* | Simple dual-port | 0 | 1 | 0 | 269.84 | 237.74 | 206.73 |
| | | Single port | 0 | 1 | 0 | 280.64 | 254.36 | 221.17 |
| | | True dual-port | 0 | 1 | 0 | 275.84 | 244.56 | 212.66 |
| | RAM 32K × 18 bit *(2)* | Simple dual-port | 0 | 1 | 0 | 275.84 | 244.56 | 212.66 |
| | | Single port | 0 | 1 | 0 | 275.84 | 244.56 | 212.66 |
| | | True dual-port | 0 | 1 | 0 | 287.83 | 253.33 | 220.29 |
| | RAM 64K × 9 bit *(2)* | Simple dual-port | 0 | 1 | 0 | 287.83 | 253.33 | 220.29 |
| | | Single port | 0 | 1 | 0 | 287.83 | 253.33 | 220.29 |

*Table 4–35. Stratix Performance (Part 3 of 3)* *Note (1)*

| Resource Used | Design Size & Function | Mode | Resources Used | | | Performance (MHz) | | |
|---|---|---|---|---|---|---|---|---|
| | | | LEs | TriMatrix Memory Blocks | DSP Blocks | -5 Speed Grade | -6 Speed Grade | -7 Speed Grade |
| DSP block | 9 × 9-bit multiplier *(3)* | | 0 | 0 | 1 | 335.00 | 293.94 | 255.68 |
| | 18 × 18-bit multiplier *(3)* | | 0 | 0 | 1 | 278.78 | 237.41 | 206.52 |
| | 36 × 36-bit multiplier *(3)*, *(5)* | | 0 | 0 | 1 | 148.25 | 134.71 | 117.16 |
| | 36 × 36-bit multiplier *(4)*, *(5)* | | 0 | 0 | 1 | 278.78 | 237.41 | 206.52 |
| | 18-bit, 4-tap FIR filter | | 0 | 0 | 1 | 278.78 | 237.41 | 206.52 |
| Multiple resources | 8-bit, 16-tap parallel FIR filter | | 58 | 0 | 4 | 146.41 | 133.35 | 115.14 |
| | 8-bit, 1,024-point FFT function | | 870 | 5 *(6)* | 1 | 239.46 | 229.46 | 201.40 |

*Notes to Table 4–35:*

(1) These design performance numbers were obtained using the Quartus II software.
(2) This application uses registered inputs and outputs.
(3) This application uses registered input and output stages within the DSP block.
(4) This application uses registered input, pipeline, and output stages within the DSP block.
(5) This is for a signed/signed or unsigned/unsigned case.
(6) This design uses M4K TriMatrix memory blocks.

## Internal Timing Parameters

Internal timing parameters are specified on a speed grade basis independent of device density. Tables 4–36 through 4–42 describe the Stratix device internal timing microparameters for LEs, IOEs, TriMatrix memory structures, DSP blocks, and MultiTrack interconnects.

*Table 4–36. LE Internal Timing Microparameter Descriptions*

| Symbol | Parameter |
|---|---|
| $t_{SU}$ | LE register setup time before clock |
| $t_{H}$ | LE register hold time after clock |
| $t_{CO}$ | LE register clock-to-output delay |
| $t_{LUT}$ | LE combinatorial LUT delay for data-in to data-out |
| $t_{CLR}$ | Minimum clear pulse width |
| $t_{PRE}$ | Minimum preset pulse width |
| $t_{CLKHL}$ | Minimum clock high or low time |

*Table 4–37. IOE Internal Timing Microparameter Descriptions*

| Symbol | Parameter |
|---|---|
| $t_{SU}$ | IOE input and output register setup time before clock |
| $t_{H}$ | IOE input and output register hold time after clock |
| $t_{CO}$ | IOE input and output register clock-to-output delay |
| $t_{PIN2COMBOUT\_R}$ | Row input pin to IOE combinatorial output |
| $t_{PIN2COMBOUT\_C}$ | Column input pin to IOE combinatorial output |
| $t_{COMBIN2PIN\_R}$ | Row IOE data input to combinatorial output pin |
| $t_{COMBIN2PIN\_C}$ | Column IOE data input to combinatorial output pin |
| $t_{CLR}$ | Minimum clear pulse width |
| $t_{PRE}$ | Minimum preset pulse width |
| $t_{CLKHL}$ | Minimum clock high or low time |

*Table 4–38. DSP Block Internal Timing Microparameter Descriptions*

| Symbol | Parameter |
|---|---|
| $t_{SU}$ | Input, pipeline, and output register setup time before clock |
| $t_{H}$ | Input, pipeline, and output register hold time after clock |
| $t_{CO}$ | Input, pipeline, and output register clock-to-output delay |
| $t_{INREG2PIPE9}$ | Input Register to DSP Block pipeline register in 9 × 9-bit mode |
| $t_{INREG2PIPE18}$ | Input Register to DSP Block pipeline register in 18 × 18-bit mode |
| $t_{PIPE2OUTREG2ADD}$ | DSP Block Pipeline Register to output register delay in Two-Multipliers Adder mode |
| $t_{PIPE2OUTREG4ADD}$ | DSP Block Pipeline Register to output register delay in Four-Multipliers Adder mode |
| $t_{PD9}$ | Combinatorial input to output delay for 9 × 9 |
| $t_{PD18}$ | Combinatorial input to output delay for 18 × 18 |
| $t_{PD36}$ | Combinatorial input to output delay for 36 × 36 |
| $t_{CLR}$ | Minimum clear pulse width |
| $t_{CLKHL}$ | Minimum clock high or low time |

*Table 4–39. M512 Block Internal Timing MicroparameterDescriptions*

| Symbol | Parameter |
|---|---|
| $t_{M512RC}$ | Synchronous read cycle time |
| $t_{M512WC}$ | Synchronous write cycle time |
| $t_{M512WERESU}$ | Write or read enable setup time before clock |
| $t_{M512WEREH}$ | Write or read enable hold time after clock |
| $t_{M512DATASU}$ | Data setup time before clock |
| $t_{M512DATAH}$ | Data hold time after clock |
| $t_{M512WADDRSU}$ | Write address setup time before clock |
| $t_{M512WADDRH}$ | Write address hold time after clock |
| $t_{M512RADDRSU}$ | Read address setup time before clock |
| $t_{M512RADDRH}$ | Read address hold time after clock |
| $t_{M512DATACO1}$ | Clock-to-output delay when using output registers |
| $t_{M512DATACO2}$ | Clock-to-output delay without output registers |
| $t_{M512CLKHL}$ | Minimum clock high or low time |
| $t_{M512CLR}$ | Minimum clear pulse width |

*Table 4–40. M4K Block Internal Timing Microparameter Descriptions*

| Symbol | Parameter |
|---|---|
| $t_{M4KRC}$ | Synchronous read cycle time |
| $t_{M4KWC}$ | Synchronous write cycle time |
| $t_{M4KWERESU}$ | Write or read enable setup time before clock |
| $t_{M4KWEREH}$ | Write or read enable hold time after clock |
| $t_{M4KBESU}$ | Byte enable setup time before clock |
| $t_{M4KBEH}$ | Byte enable hold time after clock |
| $t_{M4KDATAASU}$ | A port data setup time before clock |
| $t_{M4KDATAAH}$ | A port data hold time after clock |
| $t_{M4KADDRASU}$ | A port address setup time before clock |
| $t_{M4KADDRAH}$ | A port address hold time after clock |
| $t_{M4KDATABSU}$ | B port data setup time before clock |
| $t_{M4KDATABH}$ | B port data hold time after clock |
| $t_{M4KADDRBSU}$ | B port address setup time before clock |
| $t_{M4KADDRBH}$ | B port address hold time after clock |
| $t_{M4KDATACO1}$ | Clock-to-output delay when using output registers |
| $t_{M4KDATACO2}$ | Clock-to-output delay without output registers |
| $t_{M4KCLKHL}$ | Minimum clock high or low time |
| $t_{M4KCLR}$ | Minimum clear pulse width |

*Table 4–41. M-RAM Block Internal Timing Microparameter Descriptions (Part 1 of 2)*

| Symbol | Parameter |
|---|---|
| $t_{MRAMRC}$ | Synchronous read cycle time |
| $t_{MRAMWC}$ | Synchronous write cycle time |
| $t_{MRAMWERESU}$ | Write or read enable setup time before clock |
| $t_{MRAMWEREH}$ | Write or read enable hold time after clock |
| $t_{MRAMBESU}$ | Byte enable setup time before clock |
| $t_{MRAMBEH}$ | Byte enable hold time after clock |
| $t_{MRAMDATAASU}$ | A port data setup time before clock |
| $t_{MRAMDATAAH}$ | A port data hold time after clock |
| $t_{MRAMADDRASU}$ | A port address setup time before clock |
| $t_{MRAMADDRAH}$ | A port address hold time after clock |

*Table 4–41. M-RAM Block Internal Timing Microparameter Descriptions (Part 2 of 2)*

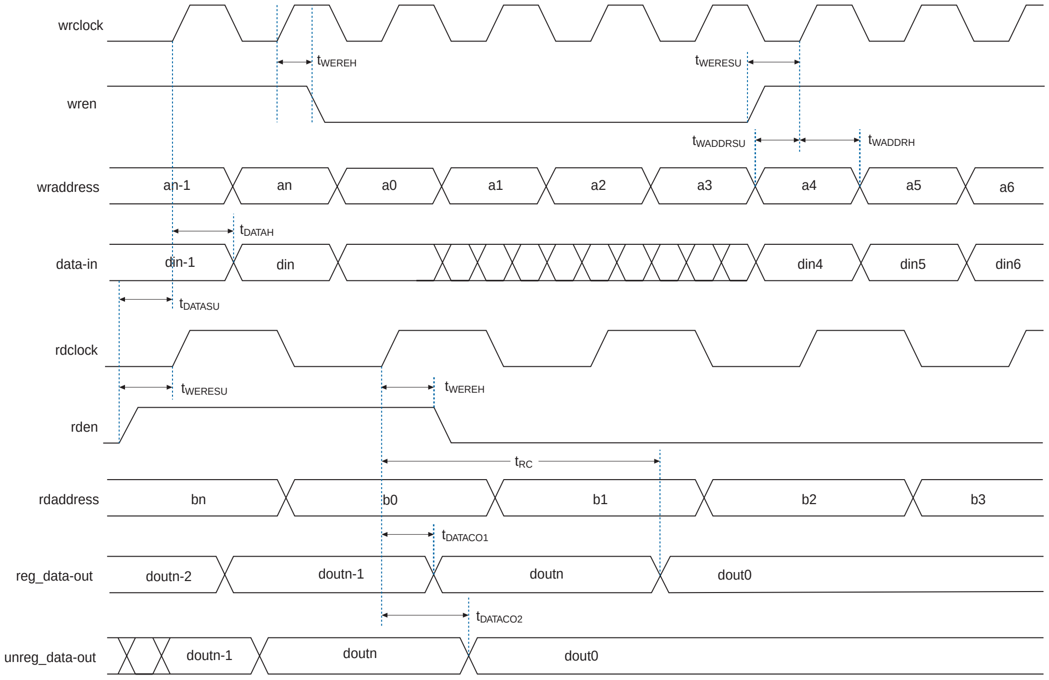
| Symbol | Parameter |
|---|---|
| $t_{MRAMDATABSU}$ | B port setup time before clock |
| $t_{MRAMDATABH}$ | B port hold time after clock |
| $t_{MRAMADDRBSU}$ | B port address setup time before clock |
| $t_{MRAMADDRBH}$ | B port address hold time after clock |
| $t_{MRAMDATACO1}$ | Clock-to-output delay when using output registers |
| $t_{MRAMDATACO2}$ | Clock-to-output delay without output registers |
| $t_{MRAMCLKHL}$ | Minimum clock high or low time |
| $t_{MRAMCLR}$ | Minimum clear pulse width |

*Table 4–42. Routing Delay Internal Timing Microparameter Descriptions*

| Symbol | Parameter |
|---|---|
| $t_{R4}$ | Delay for an R4 line with average loading; covers a distance of four LAB columns |
| $t_{R8}$ | Delay for an R8 line with average loading; covers a distance of eight LAB columns |
| $t_{R24}$ | Delay for an R24 line with average loading; covers a distance of 24 LAB columns |
| $t_{C4}$ | Delay for an C4 line with average loading; covers a distance of four LAB rows |
| $t_{C8}$ | Delay for an C8 line with average loading; covers a distance of eight LAB rows |
| $t_{C16}$ | Delay for an C16 line with average loading; covers a distance of 16 LAB rows |
| $t_{LOCAL}$ | Local interconnect delay |

Figure 4–3 shows the TriMatrix memory waveforms for the M512, M4K, and M-RAM timing parameters shown in Tables 4–39 through 4–41 above.

*Figure 4–3. Dual-Port RAM Timing Microparameter Waveform*



Internal timing parameters are specified on a speed grade basis independent of device density. Tables 4–43 through 4–48 show the internal timing microparameters for LEs, IOEs, TriMatrix memory structures, DSP blocks, and MultiTrack interconnects.

*Table 4–43. LE Internal Timing Microparameters*

| Symbol | -5 | | -6 | | -7 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 10 | | 10 | | 11 | | ps |
| $t_{H}$ | 100 | | 100 | | 114 | | ps |
| $t_{CO}$ | | 156 | | 176 | | 202 | ps |
| $t_{LUT}$ | | 366 | | 459 | | 527 | ps |
| $t_{CLR}$ | 100 | | 100 | | 114 | | ps |
| $t_{PRE}$ | 100 | | 100 | | 114 | | ps |
| $t_{CLKHL}$ | 100 | | 100 | | 114 | | ps |

*Table 4–44. IOE Internal Timing Microparameters*

| Symbol | -5 | | -6 | | -7 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 76 | | 80 | | 80 | | ps |
| $t_{H}$ | 64 | | 68 | | 68 | | ps |
| $t_{CO}$ | | 162 | | 171 | | 171 | ps |
| $t_{PIN2COMBOUT\_R}$ | | 1,038 | | 1,093 | | 1,256 | ps |
| $t_{PIN2COMBOUT\_C}$ | | 927 | | 976 | | 1,122 | ps |
| $t_{COMBIN2PIN\_R}$ | | 2,944 | | 3,099 | | 3,563 | ps |
| $t_{COMBIN2PIN\_C}$ | | 3,189 | | 3,357 | | 3,860 | ps |
| $t_{CLR}$ | 262 | | 276 | | 317 | | ps |
| $t_{PRE}$ | 262 | | 276 | | 317 | | ps |
| $t_{CLKHL}$ | 90 | | 95 | | 109 | | ps |

*Table 4–45. DSP Block Internal Timing Microparameters*

| Symbol | -5 | | -6 | | -7 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0 | | 0 | | 0 | | ps |
| $t_{H}$ | 67 | | 75 | | 86 | | ps |
| $t_{CO}$ | | 142 | | 158 | | 181 | ps |
| $t_{INREG2PIPE9}$ | | 2,613 | | 2,982 | | 3,429 | ps |
| $t_{INREG2PIPE18}$ | | 3,390 | | 3,993 | | 4,591 | ps |
| $t_{PIPE2OUTREG2ADD}$ | | 2,002 | | 2,203 | | 2,533 | ps |
| $t_{PIPE2OUTREG4ADD}$ | | 2,899 | | 3,189 | | 3,667 | ps |
| $t_{PD9}$ | | 3,709 | | 4,081 | | 4,692 | ps |
| $t_{PD18}$ | | 4,795 | | 5,275 | | 6,065 | ps |
| $t_{PD36}$ | | 7,495 | | 8,245 | | 9,481 | ps |
| $t_{CLR}$ | 450 | | 500 | | 575 | | ps |
| $t_{CLKHL}$ | 1,350 | | 1,500 | | 1,724 | | ps |

*Table 4–46. M512 Block Internal Timing Microparameters*

| Symbol | -5 | | -6 | | -7 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{M512RC}$ | | 3,340 | | 3,816 | | 4,387 | ps |
| $t_{M512WC}$ | | 3,138 | | 3,590 | | 4,128 | ps |
| $t_{M512WERESU}$ | 110 | | 123 | | 141 | | ps |
| $t_{M512WERH}$ | 34 | | 38 | | 43 | | ps |
| $t_{M512DATASU}$ | 110 | | 123 | | 141 | | ps |
| $t_{M512DATAH}$ | 34 | | 38 | | 43 | | ps |
| $t_{M512WADDRASU}$ | 110 | | 123 | | 141 | | ps |
| $t_{M512WADDRH}$ | 34 | | 38 | | 43 | | ps |
| $t_{M512RADDRASU}$ | 110 | | 123 | | 141 | | ps |
| $t_{M512RADDRH}$ | 34 | | 38 | | 43 | | ps |
| $t_{M512DATACO1}$ | | 424 | | 472 | | 541 | ps |
| $t_{M512DATACO2}$ | | 3,366 | | 3,846 | | 4,421 | ps |
| $t_{M512CLKHL}$ | 150 | | 167 | | 192 | | ps |
| $t_{M512CLR}$ | 170 | | 189 | | 217 | | ps |

*Table 4–47. M4K Block Internal Timing Microparameters (Part 1 of 2)*

| Symbol | -5 | | -6 | | -7 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{M4KRC}$ | | 3,807 | | 4,320 | | 4,967 | ps |
| $t_{M4KWC}$ | | 2,556 | | 2,840 | | 3,265 | ps |
| $t_{M4KWERESU}$ | 131 | | 149 | | 171 | | ps |
| $t_{M4KWERH}$ | 34 | | 38 | | 43 | | ps |
| $t_{M4KDATASU}$ | 131 | | 149 | | 171 | | ps |
| $t_{M4KDATAH}$ | 34 | | 38 | | 43 | | ps |
| $t_{M4KWADDRASU}$ | 131 | | 149 | | 171 | | ps |
| $t_{M4KWADDRH}$ | 34 | | 38 | | 43 | | ps |
| $t_{M4KRADDRASU}$ | 131 | | 149 | | 171 | | ps |
| $t_{M4KRADDRH}$ | 34 | | 38 | | 43 | | ps |
| $t_{M4KDATABSU}$ | 131 | | 149 | | 171 | | ps |
| $t_{M4KDATABH}$ | 34 | | 38 | | 43 | | ps |

*Table 4–47. M4K Block Internal Timing Microparameters (Part 2 of 2)*

| Symbol | -5 | | -6 | | -7 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{M4KADDRBSU}$ | 131 | | 149 | | 171 | | ps |
| $t_{M4KADDRBH}$ | 34 | | 38 | | 43 | | ps |
| $t_{M4KDATACO1}$ | | 571 | | 635 | | 729 | ps |
| $t_{M4KDATACO2}$ | | 3,984 | | 4,507 | | 5,182 | ps |
| $t_{M4KCLKHL}$ | 150 | | 167 | | 192 | | ps |
| $t_{M4KCLR}$ | 170 | | 189 | | 217 | | ps |

*Table 4–48. M-RAM Block Internal Timing Microparameters*

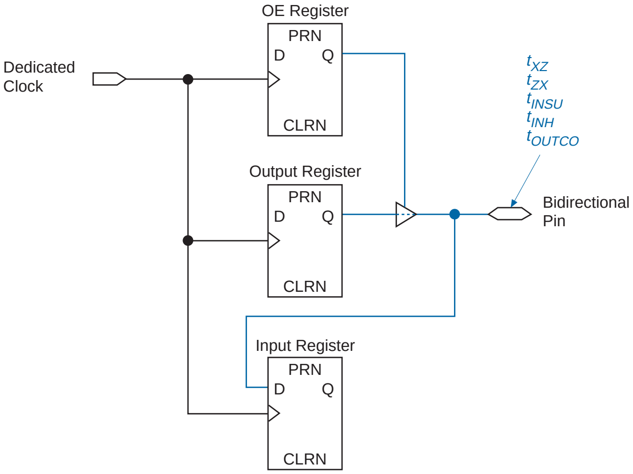
| Symbol | -5 | | -6 | | -7 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{MRAMRC}$ | | 4,364 | | 4,838 | | 5,562 | ps |
| $t_{MRAMWC}$ | | 3,654 | | 4,127 | | 4,746 | ps |
| $t_{MRAMWERESU}$ | 25 | | 25 | | 28 | | ps |
| $t_{MRAMWERH}$ | 18 | | 20 | | 23 | | ps |
| $t_{MRAMDATASU}$ | 25 | | 25 | | 28 | | ps |
| $t_{MRAMDATAH}$ | 18 | | 20 | | 23 | | ps |
| $t_{MRAMWADDRASU}$ | 25 | | 25 | | 28 | | ps |
| $t_{MRAMWADDRH}$ | 18 | | 20 | | 23 | | ps |
| $t_{MRAMRADDRASU}$ | 25 | | 25 | | 28 | | ps |
| $t_{MRAMRADDRH}$ | 18 | | 20 | | 23 | | ps |
| $t_{MRAMDATABSU}$ | 25 | | 25 | | 28 | | ps |
| $t_{MRAMDATABH}$ | 18 | | 20 | | 23 | | ps |
| $t_{MRAMADDRBSU}$ | 25 | | 25 | | 28 | | ps |
| $t_{MRAMADDRBH}$ | 18 | | 20 | | 23 | | ps |
| $t_{MRAMDATACO1}$ | | 1,038 | | 1,053 | | 1,210 | ps |
| $t_{MRAMDATACO2}$ | | 4,362 | | 4,939 | | 5,678 | ps |
| $t_{MRAMCLKHL}$ | 270 | | 300 | | 345 | | ps |
| $t_{MRAMCLR}$ | 135 | | 150 | | 172 | | ps |

Routing delays vary depending on the load on that specific routing line. The Quartus II software reports the routing delay information when running the timing analysis for a design. Contact Altera Applications for more details.

## External Timing Parameters

External timing parameters are specified by device density and speed grade. Figure 4–4 shows the timing model for bidirectional IOE pin timing. All registers are within the IOE.

*Figure 4–4. External Timing in Stratix Devices*



All external I/O timing parameters shown are for 3.3-V LVTTL I/O standard with the maximum current strength and fast slew rate. For external I/O timing using standards other than LVTTL or for different current strengths, use the I/O standard input and output delay adders in Tables 4–94 through 4–98.

Table 4–49 shows the external I/O timing parameters when using fast regional clock networks.

**Table 4–49. Stratix Fast Regional Clock External I/O Timing Parameters** *Notes (1), (2)*

| Symbol | Parameter | Conditions |
|---|---|---|
| $t_{INSU}$ | Setup time for input or bidirectional pin using column IOE input register with fast regional clock fed by `FCLK` pin | |
| $t_{INH}$ | Hold time for input or bidirectional pin using column IOE input register with fast regional clock fed by `FCLK` pin | |
| $t_{OUTCO}$ | Clock-to-output delay output or bidirectional pin using column IOE output register with fast regional clock fed by `FCLK` pin | $C_{LOAD}$ = 10 pF |
| $t_{XZ}$ | Synchronous column IOE output enable register to output pin disable delay using fast regional clock fed by `FCLK` pin | $C_{LOAD}$ = 10 pF |
| $t_{ZX}$ | Synchronous column IOE output enable register to output pin enable delay using fast regional clock fed by `FCLK` pin | $C_{LOAD}$ = 10 pF |

***Notes to Table 4–49:***

(1) These timing parameters are sample-tested only.

(2) These timing parameters are for column and row IOE pins. Designers should use the Quartus II software to verify the external timing for any pin.

Table 4–50 shows the external I/O timing parameters when using regional clock networks.

**Table 4–50. Stratix Regional Clock External I/O Timing Parameters (Part 1 of 2)** *Notes (1), (2)*

| Symbol | Parameter | Conditions |
|---|---|---|
| $t_{INSU}$ | Setup time for input or bidirectional pin using column IOE input register with regional clock fed by `CLK` pin | |
| $t_{INH}$ | Hold time for input or bidirectional pin using column IOE input register with regional clock fed by `CLK` pin | |
| $t_{OUTCO}$ | Clock-to-output delay output or bidirectional pin using column IOE output register with regional clock fed by `CLK` pin | $C_{LOAD}$ = 10 pF |

**Table 4–50. Stratix Regional Clock External I/O Timing Parameters (Part 2 of 2)** *Notes (1), (2)*

| Symbol | Parameter | Conditions |
|---|---|---|
| $t_{XZ}$ | Synchronous column IOE output enable register to output pin disable delay using regional clock fed by `CLK` pin | $C_{LOAD}$ = 10 pF |
| $t_{ZX}$ | Synchronous column IOE output enable register to output pin enable delay using regional clock fed by `CLK` pin | $C_{LOAD}$ = 10 pF |
| $t_{INSUPLL}$ | Setup time for input or bidirectional pin using column IOE input register with regional clock fed by Enhanced PLL with default phase setting | |
| $t_{INHPLL}$ | Hold time for input or bidirectional pin using column IOE input register with regional clock fed by Enhanced PLL with default phase setting | |
| $t_{OUTCOPLL}$ | Clock-to-output delay output or bidirectional pin using column IOE output register with regional clock Enhanced PLL with default phase setting | $C_{LOAD}$ = 10 pF |
| $t_{XZPLL}$ | Synchronous column IOE output enable register to output pin disable delay using regional clock fed by Enhanced PLL with default phase setting | $C_{LOAD}$ = 10 pF |
| $t_{ZXPLL}$ | Synchronous column IOE output enable register to output pin enable delay using regional clock fed by Enhanced PLL with default phase setting | $C_{LOAD}$ = 10 pF |

*Notes to Table 4–50:*

(1) These timing parameters are sample-tested only.

(2) These timing parameters are for column IOE pins. Row IOE pins are 100- to 200-ps slower depending on device, speed grade, and the specific parameter in question. Designers should use the Quartus II software to verify the external timing for any pin.

Table 4–51 shows the external I/O timing parameters when using global clock networks.

### *Table 4–51. Stratix Global Clock External I/O Timing Parameters* *Notes (1), (2)*

| Symbol | Parameter | Conditions |
|---|---|---|
| $t_{INSU}$ | Setup time for input or bidirectional pin using column IOE input register with global clock fed by `CLK` pin | |
| $t_{INH}$ | Hold time for input or bidirectional pin using column IOE input register with global clock fed by `CLK` pin | |
| $t_{OUTCO}$ | Clock-to-output delay output or bidirectional pin using column IOE output register with global clock fed by `CLK` pin | $C_{LOAD}$ = 10 pF |
| $t_{XZ}$ | Synchronous column IOE output enable register to output pin disable delay using global clock fed by `CLK` pin | $C_{LOAD}$ = 10 pF |
| $t_{ZX}$ | Synchronous column IOE output enable register to output pin enable delay using global clock fed by `CLK` pin | $C_{LOAD}$ = 10 pF |
| $t_{INSUPLL}$ | Setup time for input or bidirectional pin using column IOE input register with global clock fed by Enhanced PLL with default phase setting | |
| $t_{INHPLL}$ | Hold time for input or bidirectional pin using column IOE input register with global clock fed by enhanced PLL with default phase setting | |
| $t_{OUTCOPLL}$ | Clock-to-output delay output or bidirectional pin using column IOE output register with global clock enhanced PLL with default phase setting | $C_{LOAD}$ = 10 pF |
| $t_{XZPLL}$ | Synchronous column IOE output enable register to output pin disable delay using global clock fed by enhanced PLL with default phase setting | $C_{LOAD}$ = 10 pF |
| $t_{ZXPLL}$ | Synchronous column IOE output enable register to output pin enable delay using global clock fed by enhanced PLL with default phase setting | $C_{LOAD}$ = 10 pF |

***Notes to Table 4–51:***

(1) These timing parameters are sample-tested only.

(2) These timing parameters are for column IOE pins using a 3.3-V LVTTL, 24-mA setting. Row IOE pins are 100- to 250-ps slower depending on device, speed grade, and the specific parameter in question. Designers should use the Quartus II software to verify the external timing for any pin.

Tables 4–52 through 4–57 show the external timing parameters on column and row pins for EP1S10 devices.

*Table 4–52. EP1S10 Column Pin Fast Regional Clock External I/O Timing Parameters*

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.244 | | 2.374 | | 2.714 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 4.598 | 2.000 | 4.922 | 2.000 | 5.638 | ns |
| $t_{XZ}$ | | 4.708 | | 5.038 | | 5.770 | ns |
| $t_{ZX}$ | | 4.708 | | 5.038 | | 5.770 | ns |

*Table 4–53. EP1S10 Column Pin Regional Clock External I/O Timing Parameters*

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.114 | | 2.174 | | 2.483 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 4.728 | 2.000 | 5.078 | 2.000 | 5.818 | ns |
| $t_{XZ}$ | | 4.838 | | 5.194 | | 5.950 | ns |
| $t_{ZX}$ | | 4.838 | | 5.194 | | 5.950 | ns |
| $t_{INSUPLL}$ | 1.035 | | 0.941 | | 1.070 | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.629 | 0.500 | 2.769 | 0.500 | 3.158 | ns |
| $t_{XZPLL}$ | | 2.739 | | 2.885 | | 3.290 | ns |
| $t_{ZXPLL}$ | | 2.739 | | 2.885 | | 3.290 | ns |

*Table 4–54. EP1S10 Column Pin Global Clock External I/O Timing Parameters*

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 1.699 | | 1.748 | | 1.993 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 5.143 | 2.000 | 5.504 | 2.000 | 6.308 | ns |
| $t_{XZ}$ | | 5.253 | | 5.620 | | 6.440 | ns |
| $t_{ZX}$ | | 5.253 | | 5.620 | | 6.440 | ns |
| $t_{INSUPLL}$ | 0.988 | | 0.936 | | 1.066 | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.634 | 0.500 | 2.774 | 0.500 | 3.162 | ns |
| $t_{XZPLL}$ | | 2.744 | | 2.890 | | 3.294 | ns |
| $t_{ZXPLL}$ | | 2.744 | | 2.890 | | 3.294 | ns |

*Table 4–55. EP1S10 Row Pin Fast Regional Clock External I/O Timing Parameters*

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.177 | | 2.366 | | 2.705 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 4.973 | 2.000 | 4.989 | 2.000 | 5.485 | ns |
| $t_{XZ}$ | | 5.210 | | 5.238 | | 5.771 | ns |
| $t_{ZX}$ | | 5.210 | | 5.238 | | 5.771 | ns |

*Table 4–56. EP1S10 Row Pin Regional Clock External I/O Timing Parameters*

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.244 | | 2.413 | | 2.760 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 4.906 | 2.000 | 4.942 | 2.000 | 5.430 | ns |
| $t_{XZ}$ | | 5.143 | | 5.191 | | 5.716 | ns |
| $t_{ZX}$ | | 5.143 | | 5.191 | | 5.716 | ns |
| $t_{INSUPLL}$ | 1.126 | | 1.186 | | 1.352 | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.804 | 0.500 | 2.627 | 0.500 | 2.765 | ns |
| $t_{XZPLL}$ | | 3.041 | | 2.876 | | 3.051 | ns |
| $t_{ZXPLL}$ | | 3.041 | | 2.876 | | 3.051 | ns |

*Table 4–57. EP1S10 Row Pin Global Clock External I/O Timing Parameters*

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 1.790 | | 1.947 | | 2.223 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 5.360 | 2.000 | 5.408 | 2.000 | 5.967 | ns |
| $t_{XZ}$ | | 5.597 | | 5.657 | | 6.253 | ns |
| $t_{ZX}$ | | 5.597 | | 5.657 | | 6.253 | ns |
| $t_{INSUPLL}$ | 1.126 | | 1.186 | | 1.352 | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.804 | 0.500 | 2.627 | 0.500 | 2.765 | ns |
| $t_{XZPLL}$ | | 3.041 | | 2.876 | | 3.051 | ns |
| $t_{ZXPLL}$ | | 3.041 | | 2.876 | | 3.051 | ns |

Tables 4–58 through 4–63 show the external timing parameters on column and row pins for EP1S20 devices.

*Table 4–58. EP1S20 Column Pin Fast Regional Clock External I/O Timing Parameters*

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.113 | | 2.250 | | 2.571 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 4.671 | 2.000 | 5.002 | 2.000 | 5.730 | ns |
| $t_{XZ}$ | | 4.781 | | 5.118 | | 5.862 | ns |
| $t_{ZX}$ | | 4.781 | | 5.118 | | 5.862 | ns |

*Table 4–59. EP1S20 Column Pin Regional Clock External I/O Timing Parameters*

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 1.763 | | 1.906 | | 2.177 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 4.979 | 2.000 | 5.346 | 2.000 | 6.124 | ns |
| $t_{XZ}$ | | 5.089 | | 5.462 | | 6.256 | ns |
| $t_{ZX}$ | | 5.089 | | 5.462 | | 6.256 | ns |
| $t_{INSUPLL}$ | 0.926 | | 0.978 | | 1.112 | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.638 | 0.500 | 2.776 | 0.500 | 3.167 | ns |
| $t_{XZPLL}$ | | 2.748 | | 2.892 | | 3.299 | ns |
| $t_{ZXPLL}$ | | 2.748 | | 2.892 | | 3.299 | ns |

### Table 4–60. EP1S20 Column Pin Global Clock External I/O Timing Parameters

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 1.493 | | 1.675 | | 1.862 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 5.249 | 2.000 | 5.621 | 2.000 | 6.439 | ns |
| $t_{XZ}$ | | 5.359 | | 5.737 | | 6.571 | ns |
| $t_{ZX}$ | | 5.359 | | 5.737 | | 6.571 | ns |
| $t_{INSUPLL}$ | 0.874 | | 0.926 | | 1.103 | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.648 | 0.500 | 2.784 | 0.500 | 3.176 | ns |
| $t_{XZPLL}$ | | 2.758 | | 2.900 | | 3.308 | ns |
| $t_{ZXPLL}$ | | 2.758 | | 2.900 | | 3.308 | ns |

### Table 4–61. EP1S20 Row Pin Fast Regional Clock External I/O Timing Parameters

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 1.997 | | 2.170 | | 2.481 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 4.653 | 2.000 | 4.985 | 2.000 | 5.709 | ns |
| $t_{XZ}$ | | 4.890 | | 5.234 | | 5.995 | ns |
| $t_{ZX}$ | | 4.890 | | 5.234 | | 5.995 | ns |

*Table 4–62. EP1S20 Row Pin Regional Clock External I/O Timing Parameters*

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 1.999 | | 2.146 | | 2.456 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 4.651 | 2.000 | 5.009 | 2.000 | 5.734 | ns |
| $t_{XZ}$ | | 4.888 | | 5.258 | | 6.020 | ns |
| $t_{ZX}$ | | 4.888 | | 5.258 | | 6.020 | ns |
| $t_{INSUPLL}$ | 1.126 | | 1.186 | | 1.352 | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.304 | 0.500 | 2.427 | 0.500 | 2.765 | ns |
| $t_{XZPLL}$ | | 2.541 | | 2.676 | | 3.051 | ns |
| $t_{ZXPLL}$ | | 2.541 | | 2.676 | | 3.051 | ns |

*Table 4–63. EP1S20 Row Pin Global Clock External I/O Timing Parameters*

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 1.684 | | 1.826 | | 2.089 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 4.966 | 2.000 | 5.329 | 2.000 | 6.101 | ns |
| $t_{XZ}$ | | 5.203 | | 5.578 | | 6.387 | ns |
| $t_{ZX}$ | | 5.203 | | 5.578 | | 6.387 | ns |
| $t_{INSUPLL}$ | 1.126 | | 1.186 | | 1.352 | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.304 | 0.500 | 2.427 | 0.500 | 2.765 | ns |
| $t_{XZPLL}$ | | 2.541 | | 2.676 | | 3.051 | ns |
| $t_{ZXPLL}$ | | 2.541 | | 2.676 | | 3.051 | ns |

Tables 4–64 through 4–69 show the external timing parameters on column and row pins for EP1S25 devices.

**Table 4–64. EP1S25 Column Pin Fast Regional Clock External I/O Timing Parameters**

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.416 | | 2.615 | | 2.960 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 4.526 | 2.000 | 4.837 | 2.000 | 5.541 | ns |
| $t_{XZ}$ | | 4.636 | | 4.953 | | 5.673 | ns |
| $t_{ZX}$ | | 4.636 | | 4.953 | | 5.673 | ns |

**Table 4–65. EP1S25 Column Pin Regional Clock External I/O Timing Parameters**

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 1.713 | | 1.838 | | 2.120 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 5.229 | 2.000 | 5.614 | 2.000 | 6.432 | ns |
| $t_{XZ}$ | | 5.339 | | 5.730 | | 6.564 | ns |
| $t_{ZX}$ | | 5.339 | | 5.730 | | 6.564 | ns |
| $t_{INSUPLL}$ | 1.061 | | 1.155 | | 1.233 | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.661 | 0.500 | 2.799 | 0.500 | 3.195 | ns |
| $t_{XZPLL}$ | | 2.771 | | 2.915 | | 3.327 | ns |
| $t_{ZXPLL}$ | | 2.771 | | 2.915 | | 3.327 | ns |

*Table 4–66. EP1S25 Column Pin Global Clock External I/O Timing Parameters*

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 1.748 | | 1.883 | | 2.171 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 5.194 | 2.000 | 5.569 | 2.000 | 6.381 | ns |
| $t_{XZ}$ | | 5.304 | | 5.685 | | 6.513 | ns |
| $t_{ZX}$ | | 5.304 | | 5.685 | | 6.513 | ns |
| $t_{INSUPLL}$ | 1.088 | | 1.097 | | 1.220 | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.676 | 0.500 | 2.813 | 0.500 | 3.208 | ns |
| $t_{XZPLL}$ | | 2.786 | | 2.929 | | 3.340 | ns |
| $t_{ZXPLL}$ | | 2.786 | | 2.929 | | 3.340 | ns |

*Table 4–67. EP1S25 Row Pin Fast Regional Clock External I/O Timing Parameters*

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.371 | | 2.566 | | 2.902 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 4.479 | 2.000 | 4.789 | 2.000 | 5.488 | ns |
| $t_{XZ}$ | | 4.716 | | 5.038 | | 5.774 | ns |
| $t_{ZX}$ | | 4.716 | | 5.038 | | 5.774 | ns |

*Table 4–68. EP1S25 Row Pin Regional Clock External I/O Timing Parameters*

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 1.970 | | 2.109 | | 2.377 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 4.880 | 2.000 | 5.246 | 2.000 | 6.013 | ns |
| $t_{XZ}$ | | 5.117 | | 5.495 | | 6.299 | ns |
| $t_{ZX}$ | | 5.117 | | 5.495 | | 6.299 | ns |
| $t_{INSUPLL}$ | 1.326 | | 1.386 | | 1.552 | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.304 | 0.500 | 2.427 | 0.500 | 2.765 | ns |
| $t_{XZPLL}$ | | 2.541 | | 2.676 | | 3.051 | ns |
| $t_{ZXPLL}$ | | 2.541 | | 2.676 | | 3.051 | ns |

*Table 4–69. EP1S25 Row Pin Global Clock External I/O Timing Parameters*

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 1.963 | | 2.108 | | 2.379 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 4.887 | 2.000 | 5.247 | 2.000 | 6.011 | ns |
| $t_{XZ}$ | | 5.124 | | 5.496 | | 6.297 | ns |
| $t_{ZX}$ | | 5.124 | | 5.496 | | 6.297 | ns |
| $t_{INSUPLL}$ | 1.326 | | 1.386 | | 1.552 | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.304 | 0.500 | 2.427 | 0.500 | 2.765 | ns |
| $t_{XZPLL}$ | | 2.541 | | 2.676 | | 3.051 | ns |
| $t_{ZXPLL}$ | | 2.541 | | 2.676 | | 3.051 | ns |

Tables 4–70 through 4–75 show the external timing parameters on column and row pins for EP1S30 devices.

*Table 4–70. EP1S30 Column Pin Fast Regional Clock External I/O Timing Parameters*

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.508 | | 2.729 | | 3.108 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 5.014 | 2.000 | 5.415 | 2.000 | 6.204 | ns |
| $t_{XZ}$ | | 5.124 | | 5.531 | | 6.336 | ns |
| $t_{ZX}$ | | 5.124 | | 5.531 | | 6.336 | ns |

*Table 4–71. EP1S30 Column Pin Regional Clock External I/O Timing Parameters*

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.483 | | 2.578 | | 2.935 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 5.081 | 2.000 | 5.522 | 2.000 | 6.326 | ns |
| $t_{XZ}$ | | 5.191 | | 5.638 | | 6.458 | ns |
| $t_{ZX}$ | | 5.191 | | 5.638 | | 6.458 | ns |
| $t_{INSUPLL}$ | 0.992 | | 1.042 | | 1.166 | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.630 | 0.500 | 2.768 | 0.500 | 3.162 | ns |
| $t_{XZPLL}$ | | 2.740 | | 2.884 | | 3.294 | ns |
| $t_{ZXPLL}$ | | 2.740 | | 2.884 | | 3.294 | ns |

*Table 4–72. EP1S30 Column Pin Global Clock External I/O Timing Parameters*

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.109 | | 2.171 | | 2.467 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 5.455 | 2.000 | 5.929 | 2.000 | 6.794 | ns |
| $t_{XZ}$ | | 5.565 | | 6.045 | | 6.926 | ns |
| $t_{ZX}$ | | 5.565 | | 6.045 | | 6.926 | ns |
| $t_{INSUPLL}$ | 1.020 | | 1.065 | | 1.204 | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.602 | 0.500 | 2.745 | 0.500 | 3.124 | ns |
| $t_{XZPLL}$ | | 2.712 | | 2.861 | | 3.256 | ns |
| $t_{ZXPLL}$ | | 2.712 | | 2.861 | | 3.256 | ns |

*Table 4–73. EP1S30 Row Pin Fast Regional Clock External I/O Timing Parameters*

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.581 | | 2.771 | | 3.169 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 4.749 | 2.000 | 5.132 | 2.000 | 5.881 | ns |
| $t_{XZ}$ | | 4.986 | | 5.381 | | 6.167 | ns |
| $t_{ZX}$ | | 4.986 | | 5.381 | | 6.167 | ns |

*Table 4–74. EP1S30 Row Pin Regional Clock External I/O Timing Parameters*

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.576 | | 2.723 | | 3.118 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 4.754 | 2.000 | 5.180 | 2.000 | 5.932 | ns |
| $t_{XZ}$ | | 4.991 | | 5.429 | | 6.218 | ns |
| $t_{ZX}$ | | 4.991 | | 5.429 | | 6.218 | ns |
| $t_{INSUPLL}$ | 1.126 | | 1.186 | | 1.352 | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.304 | 0.500 | 2.427 | 0.500 | 2.765 | ns |
| $t_{XZPLL}$ | | 2.541 | | 2.676 | | 3.051 | ns |
| $t_{ZXPLL}$ | | 2.541 | | 2.676 | | 3.051 | ns |

*Table 4–75. EP1S30 Row Pin Global Clock External I/O Timing Parameters*

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.217 | | 2.332 | | 2.667 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 5.113 | 2.000 | 5.571 | 2.000 | 6.383 | ns |
| $t_{XZ}$ | | 5.350 | | 5.820 | | 6.669 | ns |
| $t_{ZX}$ | | 5.350 | | 5.820 | | 6.669 | ns |
| $t_{INSUPLL}$ | 1.126 | | 1.186 | | 1.352 | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.304 | 0.500 | 2.427 | 0.500 | 2.765 | ns |
| $t_{XZPLL}$ | | 2.541 | | 2.676 | | 3.051 | ns |
| $t_{ZXPLL}$ | | 2.541 | | 2.676 | | 3.051 | ns |

Tables 4–76 through 4–81 show the external timing parameters on column and row pins for EP1S40 devices.

**Table 4–76. EP1S40 Column Pin Fast Regional Clock External I/O Timing Parameters**

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.700 | | 2.910 | | 3.232 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 5.064 | 2.000 | 5.434 | 2.000 | 6.229 | ns |
| $t_{XZ}$ | | 5.174 | | 5.550 | | 6.361 | ns |
| $t_{ZX}$ | | 5.174 | | 5.550 | | 6.361 | ns |

**Table 4–77. EP1S40 Column Pin Regional Clock External I/O Timing Parameters**

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.467 | | 2.627 | | 3.011 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 5.255 | 2.000 | 5.673 | 2.000 | 6.501 | ns |
| $t_{XZ}$ | | 5.365 | | 5.789 | | 6.633 | ns |
| $t_{ZX}$ | | 5.365 | | 5.789 | | 6.633 | ns |
| $t_{INSUPLL}$ | 1.212 | | 1.303 | | 1.394 | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.610 | 0.500 | 2.751 | 0.500 | 3.134 | ns |
| $t_{XZPLL}$ | | 2.720 | | 2.867 | | 3.266 | ns |
| $t_{ZXPLL}$ | | 2.720 | | 2.867 | | 3.266 | ns |

*Table 4–78. EP1S40 Column Pin Global Clock External I/O Timing Parameters*

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.033 | | 2.184 | | 2.451 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 5.689 | 2.000 | 6.116 | 2.000 | 7.010 | ns |
| $t_{XZ}$ | | 5.799 | | 6.232 | | 7.142 | ns |
| $t_{ZX}$ | | 5.799 | | 6.232 | | 7.142 | ns |
| $t_{INSUPLL}$ | 1.270 | | 1.278 | | 1.466 | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.594 | 0.500 | 2.732 | 0.500 | 3.113 | ns |
| $t_{XZPLL}$ | | 2.704 | | 2.848 | | 3.245 | ns |
| $t_{ZXPLL}$ | | 2.704 | | 2.848 | | 3.245 | ns |

*Table 4–79. EP1S40 Row Pin Fast Regional Clock External I/O Timing Parameters*

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.437 | | 2.648 | | 3.029 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 4.893 | 2.000 | 5.255 | 2.000 | 6.021 | ns |
| $t_{XZ}$ | | 5.130 | | 5.504 | | 6.307 | ns |
| $t_{ZX}$ | | 5.130 | | 5.504 | | 6.307 | ns |

*Table 4–80. EP1S40 Row Pin Regional Clock External I/O Timing Parameters*

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.398 | | 2.567 | | 2.938 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 4.932 | 2.000 | 5.336 | 2.000 | 6.112 | ns |
| $t_{XZ}$ | | 5.169 | | 5.585 | | 6.398 | ns |
| $t_{ZX}$ | | 5.169 | | 5.585 | | 6.398 | ns |
| $t_{INSUPLL}$ | 1.126 | | 1.186 | | 1.352 | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.304 | 0.500 | 2.427 | 0.500 | 2.765 | ns |
| $t_{XZPLL}$ | | 2.541 | | 2.676 | | 3.051 | ns |
| $t_{ZXPLL}$ | | 2.541 | | 2.676 | | 3.051 | ns |

*Table 4–81. EP1S40 Row Pin Global Clock External I/O Timing Parameters*

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 1.965 | | 2.128 | | 2.429 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 5.365 | 2.000 | 5.775 | 2.000 | 6.621 | ns |
| $t_{XZ}$ | | 5.602 | | 6.024 | | 6.907 | ns |
| $t_{ZX}$ | | 5.602 | | 6.024 | | 6.907 | ns |
| $t_{INSUPLL}$ | 1.126 | | 1.186 | | 1.352 | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.304 | 0.500 | 2.427 | 0.500 | 2.765 | ns |
| $t_{XZPLL}$ | | 2.541 | | 2.676 | | 3.051 | ns |
| $t_{ZXPLL}$ | | 2.541 | | 2.676 | | 3.051 | ns |

Tables 4–82 through 4–87 show the external timing parameters on column and row pins for EP1S60 devices.

***Table 4–82. EP1S60 Column Pin Fast Regional Clock External I/O Timing Parameters***

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.248 | | 2.485 | | 2.841 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 5.120 | 2.000 | 4.901 | 2.000 | 5.705 | ns |
| $t_{XZ}$ | | 5.230 | | 5.617 | | 6.437 | ns |
| $t_{ZX}$ | | 5.230 | | 5.617 | | 6.437 | ns |

***Table 4–83. EP1S60 Column Pin Regional Clock External I/O Timing Parameters***

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 1.928 | | 2.118 | | 2.421 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 5.441 | 2.000 | 5.268 | 2.000 | 6.125 | ns |
| $t_{XZ}$ | | 5.551 | | 5.984 | | 6.857 | ns |
| $t_{ZX}$ | | 5.551 | | 5.984 | | 6.857 | ns |
| $t_{INSUPLL}$ | 0.961 | | 0.968 | | 1.103 | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.603 | 0.500 | 2.142 | 0.500 | 2.525 | ns |
| $t_{XZPLL}$ | | 2.713 | | 2.858 | | 3.257 | ns |
| $t_{ZXPLL}$ | | 2.713 | | 2.858 | | 3.257 | ns |

*Table 4–84. EP1S60 Column Pin Global Clock External I/O Timing Parameters*

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 1.403 | | 1.517 | | 1.732 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 6.008 | 2.000 | 5.869 | 2.000 | 6.814 | ns |
| $t_{XZ}$ | | 6.118 | | 6.585 | | 7.546 | ns |
| $t_{ZX}$ | | 6.118 | | 6.585 | | 7.546 | ns |
| $t_{INSUPLL}$ | 0.879 | | 0.931 | | 1.059 | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.643 | 0.500 | 2.179 | 0.500 | 2.569 | ns |
| $t_{XZPLL}$ | | 2.753 | | 2.895 | | 3.301 | ns |
| $t_{ZXPLL}$ | | 2.753 | | 2.895 | | 3.301 | ns |

*Table 4–85. EP1S60 Row Pin Fast Regional Clock External I/O Timing Parameters*

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.367 | | 2.561 | | 2.928 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 4.910 | 2.000 | 5.284 | 2.000 | 6.056 | ns |
| $t_{XZ}$ | | 5.147 | | 5.533 | | 6.342 | ns |
| $t_{ZX}$ | | 5.147 | | 5.533 | | 6.342 | ns |

*Table 4–86. EP1S60 Row Pin Regional Clock External I/O Timing Parameters*

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.157 | | 2.309 | | 2.644 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 5.120 | 2.000 | 5.536 | 2.000 | 6.340 | ns |
| $t_{XZ}$ | | 5.357 | | 5.785 | | 6.626 | ns |
| $t_{ZX}$ | | 5.357 | | 5.785 | | 6.626 | ns |
| $t_{INSUPLL}$ | 1.126 | | 1.186 | | 1.352 | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.304 | 0.500 | 2.427 | 0.500 | 2.765 | ns |
| $t_{XZPLL}$ | | 2.541 | | 2.676 | | 3.051 | ns |
| $t_{ZXPLL}$ | | 2.541 | | 2.676 | | 3.051 | ns |

*Table 4–87. EP1S60 Row Pin Global Clock External I/O Timing Parameters*

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 1.546 | | 1.662 | | 1.901 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 5.731 | 2.000 | 6.183 | 2.000 | 7.083 | ns |
| $t_{XZ}$ | | 5.968 | | 6.432 | | 7.369 | ns |
| $t_{ZX}$ | | 5.968 | | 6.432 | | 7.369 | ns |
| $t_{INSUPLL}$ | 1.126 | | 1.186 | | 1.352 | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.304 | 0.500 | 2.427 | 0.500 | 2.765 | ns |
| $t_{XZPLL}$ | | 2.541 | | 2.676 | | 3.051 | ns |
| $t_{ZXPLL}$ | | 2.541 | | 2.676 | | 3.051 | ns |

Tables 4–88 through 4–93 show the external timing parameters on column and row pins for EP1S80 devices.

**Table 4–88. EP1S80 Column Pin Fast Regional Clock External I/O Timing Parameters**

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.290 | | 2.531 | | 2.842 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 5.079 | 2.000 | 4.555 | 2.000 | 5.353 | ns |
| $t_{XZ}$ | | 5.189 | | 5.571 | | 6.385 | ns |
| $t_{ZX}$ | | 5.189 | | 5.571 | | 6.385 | ns |

**Table 4–89. EP1S80 Column Pin Regional Clock External I/O Timing Parameters**

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 1.939 | | 2.088 | | 2.439 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 5.430 | 2.000 | 4.954 | 2.000 | 5.807 | ns |
| $t_{XZ}$ | | 5.540 | | 5.970 | | 6.839 | ns |
| $t_{ZX}$ | | 5.540 | | 5.970 | | 6.839 | ns |
| $t_{INSUPLL}$ | 0.936 | | 0.995 | | 1.131 | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.586 | 0.500 | 1.815 | 0.500 | 2.197 | ns |
| $t_{XZPLL}$ | | 2.696 | | 2.831 | | 3.229 | ns |
| $t_{ZXPLL}$ | | 2.696 | | 2.831 | | 3.229 | ns |

### Table 4–90. EP1S80 Column Pin Global Clock External I/O Timing Parameters

| Symbol | -5 Speed Grade |  | -6 Speed Grade |  | -7 Speed Grade |  | Unit |
|---|---|---|---|---|---|---|---|
|  | Min | Max | Min | Max | Min | Max |  |
| $t_{INSU}$ | 1.225 |  | 1.330 |  | 1.516 |  | ns |
| $t_{INH}$ | 0.000 |  | 0.000 |  | 0.000 |  | ns |
| $t_{OUTCO}$ | 2.000 | 6.186 | 2.000 | 5.756 | 2.000 | 6.730 | ns |
| $t_{XZ}$ |  | 6.296 |  | 6.772 |  | 7.762 | ns |
| $t_{ZX}$ |  | 6.296 |  | 6.772 |  | 7.762 | ns |
| $t_{INSUPLL}$ | 0.921 |  | 0.931 |  | 1.110 |  | ns |
| $t_{INHPLL}$ | 0.000 |  | 0.000 |  | 0.000 |  | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.643 | 0.500 | 1.879 | 0.500 | 2.269 | ns |
| $t_{XZPLL}$ |  | 2.753 |  | 2.895 |  | 3.301 | ns |
| $t_{ZXPLL}$ |  | 2.753 |  | 2.895 |  | 3.301 | ns |

### Table 4–91. EP1S80 Row Pin Fast Regional Clock External I/O Timing Parameters

| Symbol | -5 Speed Grade |  | -6 Speed Grade |  | -7 Speed Grade |  | Unit |
|---|---|---|---|---|---|---|---|
|  | Min | Max | Min | Max | Min | Max |  |
| $t_{INSU}$ | 2.407 |  | 2.606 |  | 2.982 |  | ns |
| $t_{INH}$ | 0.000 |  | 0.000 |  | 0.000 |  | ns |
| $t_{OUTCO}$ | 2.000 | 4.870 | 2.000 | 5.239 | 2.000 | 6.002 | ns |
| $t_{XZ}$ |  | 5.107 |  | 5.488 |  | 6.288 | ns |
| $t_{ZX}$ |  | 5.107 |  | 5.488 |  | 6.288 | ns |

*Table 4–92. EP1S80 Row Pin Regional Clock External I/O Timing Parameters*

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.168 | | 2.324 | | 2.662 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 5.109 | 2.000 | 5.521 | 2.000 | 6.322 | ns |
| $t_{XZ}$ | | 5.346 | | 5.770 | | 6.608 | ns |
| $t_{ZX}$ | | 5.346 | | 5.770 | | 6.608 | ns |
| $t_{INSUPLL}$ | 1.126 | | 1.186 | | 1.352 | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.304 | 0.500 | 2.427 | 0.500 | 2.765 | ns |
| $t_{XZPLL}$ | | 2.541 | | 2.676 | | 3.051 | ns |
| $t_{ZXPLL}$ | | 2.541 | | 2.676 | | 3.051 | ns |

*Table 4–93. EP1S80 Global Clock External I/O Timing Parameters*

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 1.368 | | 1.475 | | 1.685 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 5.909 | 2.000 | 6.370 | 2.000 | 7.299 | ns |
| $t_{XZ}$ | | 6.146 | | 6.619 | | 7.585 | ns |
| $t_{ZX}$ | | 6.146 | | 6.619 | | 7.585 | ns |
| $t_{INSUPLL}$ | 1.126 | | 1.186 | | 1.352 | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.304 | 0.500 | 2.427 | 0.500 | 2.765 | ns |
| $t_{XZPLL}$ | | 2.541 | | 2.676 | | 3.051 | ns |
| $t_{ZXPLL}$ | | 2.541 | | 2.676 | | 3.051 | ns |

## External I/O Delay Parameters

External I/O delay timing parameters for I/O standard input and output adders and programmable input and output delays are specified by speed grade independent of device density.

Tables 4–94 through 4–99 show the adder delays associated with column and rowI/O pins for flip-chip and wire-bond packages. If an I/O standard is selected other than LVTTL 24 mA with a fast slew rate, add the selected delay to the external $t_{CO}$ and $t_{SU}$ I/O parameters shown in Tables 4–43 through 4–48.

*Table 4–94. Stratix I/O Standard Column Pin Input Delay Adders*

| I/O Standard | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| LVCMOS | | 0 | | 0 | | 0 | ps |
| 3.3-V LVTTL | | 0 | | 0 | | 0 | ps |
| 2.5-V LVTTL | | 30 | | 31 | | 35 | ps |
| 1.8-V LVTTL | | 150 | | 157 | | 180 | ps |
| 1.5-V LVTTL | | 210 | | 220 | | 252 | ps |
| GTL | | 220 | | 231 | | 265 | ps |
| GTL+ | | 220 | | 231 | | 265 | ps |
| 3.3-V PCI | | 0 | | 0 | | 0 | ps |
| 3.3-V PCI-X 1.0 | | 0 | | 0 | | 0 | ps |
| Compact PCI | | 0 | | 0 | | 0 | ps |
| AGP 1× | | 0 | | 0 | | 0 | ps |
| AGP 2× | | 0 | | 0 | | 0 | ps |
| CTT | | 120 | | 126 | | 144 | ps |
| SSTL-3 class I | | –30 | | –32 | | –37 | ps |
| SSTL-3 class II | | –30 | | –32 | | –37 | ps |
| SSTL-2 class I | | –70 | | –74 | | –86 | ps |
| SSTL-2 class II | | –70 | | –74 | | –86 | ps |
| SSTL-18 class I | | 180 | | 189 | | 217 | ps |
| SSTL-18 class II | | 180 | | 189 | | 217 | ps |
| 1.5-V HSTL class I | | 120 | | 126 | | 144 | ps |
| 1.5-V HSTL class II | | 120 | | 126 | | 144 | ps |
| 1.8-V HSTL class I | | 70 | | 73 | | 83 | ps |
| 1.8-V HSTL class II | | 70 | | 73 | | 83 | ps |

*Table 4–95. Stratix I/O Standard Row Pin Input Delay Adders*

| I/O Standard | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| LVCMOS | | 0 | | 0 | | 0 | ps |
| 3.3-V LVTTL | | 0 | | 0 | | 0 | ps |
| 2.5-V LVTTL | | 30 | | 31 | | 35 | ps |
| 1.8-V LVTTL | | 150 | | 157 | | 180 | ps |
| 1.5-V LVTTL | | 210 | | 220 | | 252 | ps |
| GTL | | 0 | | 0 | | 0 | ps |
| GTL+ | | 220 | | 231 | | 265 | ps |
| 3.3-V PCI | | 0 | | 0 | | 0 | ps |
| 3.3-V PCI-X 1.0 | | 0 | | 0 | | 0 | ps |
| Compact PCI | | 0 | | 0 | | 0 | ps |
| AGP 1× | | 0 | | 0 | | 0 | ps |
| AGP 2× | | 0 | | 0 | | 0 | ps |
| CTT | | 80 | | 84 | | 96 | ps |
| SSTL-3 class I | | –30 | | –32 | | –37 | ps |
| SSTL-3 class II | | –30 | | –32 | | –37 | ps |
| SSTL-2 class I | | –70 | | –74 | | –86 | ps |
| SSTL-2 class II | | –70 | | –74 | | –86 | ps |
| SSTL-18 class I | | 180 | | 189 | | 217 | ps |
| SSTL-18 class II | | 0 | | 0 | | 0 | ps |
| 1.5-V HSTL class I | | 130 | | 136 | | 156 | ps |
| 1.5-V HSTL class II | | 0 | | 0 | | 0 | ps |
| 1.8-V HSTL class I | | 70 | | 73 | | 83 | ps |
| 1.8-V HSTL class II | | 70 | | 73 | | 83 | ps |
| LVDS *(1)* | | 40 | | 42 | | 48 | ps |
| LVPECL *(1)* | | –50 | | –53 | | –61 | ps |
| 3.3-V PCML *(1)* | | 330 | | 346 | | 397 | ps |
| HyperTransport *(1)* | | 80 | | 84 | | 96 | ps |

*Table 4–96. Stratix I/O Standard Output Delay Adders for Fast Slew Rate on Column Pins (Part 1 of 2)*

| Standard | | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| LVCMOS | 2 mA | | 570 | | 599 | | 689 | ps |
| | 4 mA | | 570 | | 599 | | 689 | ps |
| | 8 mA | | 350 | | 368 | | 423 | ps |
| | 12 mA | | 130 | | 137 | | 157 | ps |
| | 24 mA | | 0 | | 0 | | 0 | ps |
| 3.3-V LVTTL | 4 mA | | 570 | | 599 | | 689 | ps |
| | 8 mA | | 350 | | 368 | | 423 | ps |
| | 12 mA | | 130 | | 137 | | 157 | ps |
| | 16 mA | | 70 | | 74 | | 85 | ps |
| | 24 mA | | 0 | | 0 | | 0 | ps |
| 2.5-V LVTTL | 2 mA | | 830 | | 872 | | 1,002 | ps |
| | 8 mA | | 250 | | 263 | | 302 | ps |
| | 12 mA | | 140 | | 147 | | 169 | ps |
| | 16 mA | | 100 | | 105 | | 120 | ps |
| 1.8-V LVTTL | 2 mA | | 420 | | 441 | | 507 | ps |
| | 8 mA | | 350 | | 368 | | 423 | ps |
| | 12 mA | | 350 | | 368 | | 423 | ps |
| 1.5-V LVTTL | 2 mA | | 1,740 | | 1,827 | | 2,101 | ps |
| | 4 mA | | 1,160 | | 1,218 | | 1,400 | ps |
| | 8 mA | | 690 | | 725 | | 833 | ps |
| GTL | | | –150 | | –157 | | –181 | ps |
| GTL+ | | | –110 | | –115 | | –133 | ps |
| 3.3-V PCI | | | –230 | | –241 | | –277 | ps |
| 3.3-V PCI-X 1.0 | | | –230 | | –241 | | –277 | ps |
| Compact PCI | | | –230 | | –241 | | –277 | ps |
| AGP 1× | | | –30 | | –31 | | –36 | ps |
| AGP 2× | | | –30 | | –31 | | –36 | ps |
| CTT | | | 50 | | 53 | | 61 | ps |
| SSTL-3 class I | | | 90 | | 95 | | 109 | ps |
| SSTL-3 class II | | | –50 | | –52 | | –60 | ps |
| SSTL-2 class I | | | 100 | | 105 | | 120 | ps |
| SSTL-2 class II | | | 20 | | 21 | | 24 | ps |
| SSTL-18 class I | | | 230 | | 242 | | 278 | ps |

*Table 4–96. Stratix I/O Standard Output Delay Adders for Fast Slew Rate on Column Pins (Part 2 of 2)*

| Standard | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| SSTL-18 class II | | 0 | | 0 | | 0 | ps |
| 1.5-V HSTL class I | | 380 | | 399 | | 459 | ps |
| 1.5-V HSTL class II | | 190 | | 200 | | 230 | ps |
| 1.8-V HSTL class I | | 380 | | 399 | | 459 | ps |
| 1.8-V HSTL class II | | 390 | | 410 | | 471 | ps |

*Table 4–97. Stratix I/O Standard Output Delay Adders for Fast Slew Rate on Row Pins (Part 1 of 2)*

| Standard | | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| LVCMOS | 2 mA | | 570 | | 599 | | 689 | ps |
| | 4 mA | | 570 | | 599 | | 689 | ps |
| | 8 mA | | 350 | | 368 | | 423 | ps |
| | 12 mA | | 130 | | 137 | | 157 | ps |
| | 24 mA | | 0 | | 0 | | 0 | ps |
| 3.3-V LVTTL | 4 mA | | 570 | | 599 | | 689 | ps |
| | 8 mA | | 350 | | 368 | | 423 | ps |
| | 12 mA | | 130 | | 137 | | 157 | ps |
| | 16 mA | | 70 | | 74 | | 85 | ps |
| | 24 mA | | 0 | | 0 | | 0 | ps |
| 2.5-V LVTTL | 2 mA | | 830 | | 872 | | 1,002 | ps |
| | 8 mA | | 250 | | 263 | | 302 | ps |
| | 12 mA | | 140 | | 147 | | 169 | ps |
| | 16 mA | | 100 | | 105 | | 120 | ps |
| 1.8-V LVTTL | 2 mA | | 1,510 | | 1,586 | | 1,824 | ps |
| | 8 mA | | 420 | | 441 | | 507 | ps |
| | 12 mA | | 350 | | 368 | | 423 | ps |
| 1.5-V LVTTL | 2 mA | | 1,740 | | 1,827 | | 2,101 | ps |
| | 4 mA | | 1,160 | | 1,218 | | 1,400 | ps |
| | 8 mA | | 690 | | 725 | | 833 | ps |
| GTL | | | 570 | | 599 | | 689 | ps |
| GTL+ | | | –110 | | –115 | | –133 | ps |
| 3.3-V PCI | | | 570 | | 599 | | 689 | ps |

*Table 4–97. Stratix I/O Standard Output Delay Adders for Fast Slew Rate on Row Pins (Part 2 of 2)*

| Standard | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| 3.3-V PCI-X 1.0 | | 570 | | 599 | | 689 | ps |
| Compact PCI | | 570 | | 599 | | 689 | ps |
| AGP 1× | | 570 | | 599 | | 689 | ps |
| AGP 2× | | 570 | | 599 | | 689 | ps |
| CTT | | 50 | | 53 | | 61 | ps |
| SSTL-3 class I | | 90 | | 95 | | 109 | ps |
| SSTL-3 class II | | –50 | | –52 | | –60 | ps |
| SSTL-2 class I | | 100 | | 105 | | 120 | ps |
| SSTL-2 class II | | 20 | | 21 | | 24 | ps |
| SSTL-18 class I | | 230 | | 242 | | 278 | ps |
| SSTL-18 class II | | 570 | | 599 | | 689 | ps |
| 1.5-V HSTL class I | | 380 | | 399 | | 459 | ps |
| 1.5-V HSTL class II | | 570 | | 599 | | 689 | ps |
| 1.8-V HSTL class I | | 380 | | 399 | | 459 | ps |
| 1.8-V HSTL class II | | 390 | | 410 | | 471 | ps |
| LVDS *(1)* | | –20 | | –21 | | –24 | ps |
| LVPECL *(1)* | | 40 | | 42 | | 48 | ps |
| PCML *(1)* | | –60 | | –63 | | –73 | ps |
| HyperTransport Technology *(1)* | | 70 | | 74 | | 85 | ps |

*Table 4–98. Stratix I/O Standard Output Delay Adders for Slow Slew Rate on Column Pins (Part 1 of 2)*

| I/O Standard | | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| LVCMOS | 2 mA | | 1,911 | | 2,011 | | 2,312 | ps |
| | 4 mA | | 1,911 | | 2,011 | | 2,312 | ps |
| | 8 mA | | 1,691 | | 1,780 | | 2,046 | ps |
| | 12 mA | | 1,471 | | 1,549 | | 1,780 | ps |
| | 24 mA | | 1,341 | | 1,412 | | 1,623 | ps |

*Table 4–98. Stratix I/O Standard Output Delay Adders for Slow Slew Rate on Column Pins (Part 2 of 2)*

| I/O Standard | | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| 3.3-V LVTTL | 4 mA | | 1,993 | | 2,097 | | 2,411 | ps |
| | 8 mA | | 1,773 | | 1,866 | | 2,145 | ps |
| | 12 mA | | 1,553 | | 1,635 | | 1,879 | ps |
| | 16 mA | | 1,493 | | 1,572 | | 1,807 | ps |
| | 24 mA | | 1,423 | | 1,498 | | 1,722 | ps |
| 2.5-V LVTTL | 2 mA | | 2,631 | | 2,768 | | 3,182 | ps |
| | 8 mA | | 2,051 | | 2,159 | | 2,482 | ps |
| | 12 mA | | 1,941 | | 2,043 | | 2,349 | ps |
| | 16 mA | | 1,901 | | 2,001 | | 2,300 | ps |
| 1.8-V LVTTL | 2 mA | | 4,632 | | 4,873 | | 5,604 | ps |
| | 8 mA | | 3,542 | | 3,728 | | 4,287 | ps |
| | 12 mA | | 3,472 | | 3,655 | | 4,203 | ps |
| 1.5-V LVTTL | 2 mA | | 6,620 | | 6,964 | | 8,008 | ps |
| | 4 mA | | 6,040 | | 6,355 | | 7,307 | ps |
| | 8 mA | | 5,570 | | 5,862 | | 6,740 | ps |
| GTL | | | 1,191 | | 1,255 | | 1,442 | ps |
| GTL+ | | | 1,231 | | 1,297 | | 1,490 | ps |
| 3.3-V PCI | | | 1,111 | | 1,171 | | 1,346 | ps |
| 3.3-V PCI-X 1.0 | | | 1,111 | | 1,171 | | 1,346 | ps |
| Compact PCI | | | 1,111 | | 1,171 | | 1,346 | ps |
| AGP 1× | | | 1,311 | | 1,381 | | 1,587 | ps |
| AGP 2× | | | 1,311 | | 1,381 | | 1,587 | ps |
| CTT | | | 1,391 | | 1,465 | | 1,684 | ps |
| SSTL-3 class I | | | 1,431 | | 1,507 | | 1,732 | ps |
| SSTL-3 class II | | | 1,291 | | 1,360 | | 1,563 | ps |
| SSTL-2 class I | | | 1,912 | | 2,013 | | 2,314 | ps |
| SSTL-2 class II | | | 1,832 | | 1,929 | | 2,218 | ps |
| SSTL-18 class I | | | 3,097 | | 3,260 | | 3,748 | ps |
| SSTL-18 class II | | | 2,867 | | 3,018 | | 3,470 | ps |
| 1.5-V HSTL class I | | | 4,916 | | 5,174 | | 5,950 | ps |
| 1.5-V HSTL class II | | | 4,726 | | 4,975 | | 5,721 | ps |
| 1.8-V HSTL class I | | | 3,247 | | 3,417 | | 3,929 | ps |
| 1.8-V HSTL class II | | | 3,257 | | 3,428 | | 3,941 | ps |

*Table 4–99. Stratix I/O Standard Output Delay Adders for Slow Slew Rate on Row Pins (Part 1 of 2)*

| I/O Standard | | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| LVCMOS | 2 mA | | 1,930 | | 2,031 | | 2,335 | ps |
| | 4 mA | | 1,930 | | 2,031 | | 2,335 | ps |
| | 8 mA | | 1,710 | | 1,800 | | 2,069 | ps |
| | 12 mA | | 1,490 | | 1,569 | | 1,803 | ps |
| 3.3-V LVTTL | 4 mA | | 1,953 | | 2,055 | | 2,363 | ps |
| | 8 mA | | 1,733 | | 1,824 | | 2,097 | ps |
| | 12 mA | | 1,513 | | 1,593 | | 1,831 | ps |
| | 16 mA | | 1,453 | | 1,530 | | 1,759 | ps |
| 2.5-V LVTTL | 2 mA | | 2,632 | | 2,769 | | 3,183 | ps |
| | 8 mA | | 2,052 | | 2,160 | | 2,483 | ps |
| | 12 mA | | 1,942 | | 2,044 | | 2,350 | ps |
| | 16 mA | | 1,902 | | 2,002 | | 2,301 | ps |
| 1.8-V LVTTL | 2 mA | | 4,537 | | 4,773 | | 5,489 | ps |
| | 8 mA | | 3,447 | | 3,628 | | 4,172 | ps |
| | 12 mA | | 3,377 | | 3,555 | | 4,088 | ps |
| 1.5-V LVTTL | 2 mA | | 6,575 | | 6,917 | | 7,954 | ps |
| | 4 mA | | 5,995 | | 6,308 | | 7,253 | ps |
| | 8 mA | | 5,525 | | 5,815 | | 6,686 | ps |
| GTL | | | 1,930 | | 2,031 | | 2,335 | ps |
| GTL+ | | | 1,250 | | 1,317 | | 1,513 | ps |
| 3.3-V PCI | | | 1,930 | | 2,031 | | 2,335 | ps |
| 3.3-V PCI-X 1.0 | | | 1,930 | | 2,031 | | 2,335 | ps |
| Compact PCI | | | 1,930 | | 2,031 | | 2,335 | ps |
| AGP 1× | | | 1,930 | | 2,031 | | 2,335 | ps |
| AGP 2× | | | 1,930 | | 2,031 | | 2,335 | ps |
| CTT | | | 1,410 | | 1,485 | | 1,707 | ps |
| SSTL-3 class I | | | 1,450 | | 1,527 | | 1,755 | ps |
| SSTL-3 class II | | | 1,310 | | 1,380 | | 1,586 | ps |
| SSTL-2 class I | | | 1,797 | | 1,892 | | 2,175 | ps |
| SSTL-2 class II | | | 1,717 | | 1,808 | | 2,079 | ps |
| SSTL-18 class I | | | 2,477 | | 2,608 | | 2,998 | ps |
| SSTL-18 class II | | | 2,817 | | 2,965 | | 3,409 | ps |
| 1.5-V HSTL class I | | | 3,629 | | 3,819 | | 4,391 | ps |

*Table 4–99. Stratix I/O Standard Output Delay Adders for Slow Slew Rate on Row Pins (Part 2 of 2)*

| I/O Standard | -5 Speed Grade |  | -6 Speed Grade |  | -7 Speed Grade |  | Unit |
|---|---|---|---|---|---|---|---|
|  | Min | Max | Min | Max | Min | Max |  |
| 1.5-V HSTL class II |  | 3,819 |  | 4,019 |  | 4,621 | ps |
| 1.8-V HSTL class I |  | 2,627 |  | 2,765 |  | 3,179 | ps |
| 1.8-V HSTL class II |  | 2,637 |  | 2,776 |  | 3,191 | ps |
| LVDS *(1)* |  | 1,340 |  | 1,411 |  | 1,622 | ps |
| LVPECL *(1)* |  | 1,400 |  | 1,474 |  | 1,694 | ps |
| 3.3-V PCML *(1)* |  | 1,300 |  | 1,369 |  | 1,573 | ps |
| HyperTransport *(1)* |  | 1,430 |  | 1,506 |  | 1,731 | ps |

***Note to Tables 4–94 through 4–99:***

(1) These parameters are only available on row I/O pins.

Tables 4–100 and 4–101 show the adder delays for the column and row IOE programmable delays. These delays are controlled with the Quartus II software options listed in the Parameter column.

*Table 4–100. Stratix IOE Programmable Delays on Column Pins (Part 1 of 2)*

| Parameter | Setting | -5 Speed Grade |  | -6 Speed Grade |  | -7 Speed Grade |  | Unit |
|---|---|---|---|---|---|---|---|---|
|  |  | Min | Max | Min | Max | Min | Max |  |
| Decrease input delay to internal cells | On |  | 2,740 |  | 3,014 |  | 3,466 | ps |
|  | Small |  | 1,870 |  | 2,057 |  | 2,365 | ps |
|  | Medium |  | 2,230 |  | 2,453 |  | 2,820 | ps |
|  | Large |  | 2,740 |  | 3,014 |  | 3,466 | ps |
| Decrease input delay to input register | On |  | 3,220 |  | 3,542 |  | 4,073 | ps |
| Decrease input delay to output register | On |  | 2,470 |  | 2,717 |  | 3,124 | ps |
| Increase delay to output pin | On |  | 377 |  | 397 |  | 457 | ps |
| Increase delay to output enable pin | On |  | 530 |  | 583 |  | 670 | ps |
| Increase output clock enable delay | On |  | 1,960 |  | 2,156 |  | 2,479 | ps |
|  | Small |  | 1,040 |  | 1,144 |  | 1,315 | ps |
|  | Large |  | 1,960 |  | 2,156 |  | 2,479 | ps |

*Table 4–100. Stratix IOE Programmable Delays on Column Pins (Part 2 of 2)*

| Parameter | Setting | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| Increase input clock enable delay | On | | 1,920 | | 2,112 | | 2,428 | ps |
| | Small | | 1,000 | | 1,100 | | 1,265 | ps |
| | Large | | 1,920 | | 2,112 | | 2,428 | ps |
| Increase output enable clock enable delay | On | | 1,960 | | 2,156 | | 2,479 | ps |
| | Small | | 1,040 | | 1,144 | | 1,315 | ps |
| | Large | | 1,960 | | 2,156 | | 2,479 | ps |
| Increase $t_{ZX}$ delay to output pin | On | | –1,112 | | –1,171 | | –1,347 | ps |

*Table 4–101. Stratix IOE Programmable Delays on Row Pins (Part 1 of 2)*

| Parameter | Setting | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| Decrease input delay to internal cells | On | | 2,740 | | 3,014 | | 3,466 | ps |
| | Small | | 1,870 | | 2,057 | | 2,365 | ps |
| | Medium | | 2,230 | | 2,453 | | 2,820 | ps |
| | Large | | 2,740 | | 3,014 | | 3,466 | ps |
| Decrease input delay to input register | On | | 3,220 | | 3,542 | | 4,073 | ps |
| Decrease input delay to output register | On | | 2,470 | | 2,717 | | 3,124 | ps |
| Increase delay to output pin | On | | 377 | | 397 | | 457 | ps |
| Increase delay to output enable pin | On | | 530 | | 583 | | 670 | ps |
| Increase output clock enable delay | On | | 1,960 | | 2,156 | | 2,479 | ps |
| | Small | | 1,040 | | 1,144 | | 1,315 | ps |
| | Large | | 1,960 | | 2,156 | | 2,479 | ps |
| Increase input clock enable delay | On | | 1,920 | | 2,112 | | 2,428 | ps |
| | Small | | 1,000 | | 1,100 | | 1,265 | ps |
| | Large | | 1,920 | | 2,112 | | 2,428 | ps |

*Table 4–101. Stratix IOE Programmable Delays on Row Pins (Part 2 of 2)*

| Parameter | Setting | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| Increase output enable clock enable delay | On | | 1,960 | | 2,156 | | 2,479 | ps |
| | Small | | 1,040 | | 1,144 | | 1,315 | ps |
| | Large | | 1,960 | | 2,156 | | 2,479 | ps |
| Increase $t_{ZX}$ delay to output pin | On | | –1,109 | | –1,168 | | –1,344 | ps |

## Maximum Input & Output Clock Rates

Tables 4–102 through 4–107 show the maximum input clock rate for column and row pins in Stratix devices.

*Table 4–102. Stratix Maximum Input Clock Rate for CLK[7..4] & CLK[15..12] Pins in Flip-Chip Packages (Part 1 of 2)*

| I/O Standard | -5 Speed Grade | -6 Speed Grade | -7 Speed Grade | Unit |
|---|---|---|---|---|
| LVTTL | 422 | 422 | 390 | MHz |
| 2.5 V | 422 | 422 | 390 | MHz |
| 1.8 V | 422 | 422 | 390 | MHz |
| 1.5 V | 422 | 422 | 390 | MHz |
| LVCMOS | 422 | 422 | 390 | MHz |
| GTL | 300 | 250 | 200 | MHz |
| GTL+ | 300 | 250 | 200 | MHz |
| SSTL-3 class I | 400 | 350 | 300 | MHz |
| SSTL-3 class II | 400 | 350 | 300 | MHz |
| SSTL-2 class I | 400 | 350 | 300 | MHz |
| SSTL-2 class II | 400 | 350 | 300 | MHz |
| SSTL-18 class I | 400 | 350 | 300 | MHz |
| SSTL-18 class II | 400 | 350 | 300 | MHz |
| 1.5-V HSTL class I | 400 | 350 | 300 | MHz |
| 1.5-V HSTL class II | 400 | 350 | 300 | MHz |
| 1.8-V HSTL class I | 400 | 350 | 300 | MHz |
| 1.8-V HSTL class II | 400 | 350 | 300 | MHz |
| 3.3-V PCI | 420 | 381 | 347 | MHz |
| 3.3-V PCI-X 1.0 | 420 | 381 | 347 | MHz |

*Table 4–102. Stratix Maximum Input Clock Rate for CLK[7..4] & CLK[15..12] Pins in Flip-Chip Packages (Part 2 of 2)*

| I/O Standard | -5 Speed Grade | -6 Speed Grade | -7 Speed Grade | Unit |
|---|---|---|---|---|
| Compact PCI | 420 | 381 | 347 | MHz |
| AGP 1× | 303 | 303 | 261 | MHz |
| AGP 2× | 303 | 303 | 261 | MHz |
| CTT | 300 | 250 | 200 | MHz |
| Differential HSTL | 400 | 350 | 300 | MHz |
| LVDS *(1)* | 645 | 645 | 622 | MHz |
| LVPECL *(1)* | 645 | 645 | 622 | MHz |
| PCML *(1)* | 300 | 275 | 275 | MHz |
| HyperTransport technology *(1)* | 500 | 500 | 450 | MHz |

*Table 4–103. Stratix Maximum Input Clock Rate for CLK[0, 2, 9, 11] Pins in Flip-Chip Packages (Part 1 of 2)*

| I/O Standard | -5 Speed Grade | -6 Speed Grade | -7 Speed Grade | Unit |
|---|---|---|---|---|
| LVTTL | 422 | 422 | 390 | MHz |
| 2.5 V | 422 | 422 | 390 | MHz |
| 1.8 V | 422 | 422 | 390 | MHz |
| 1.5 V | 422 | 422 | 390 | MHz |
| LVCMOS | 422 | 422 | 390 | MHz |
| GTL | 300 | 250 | 200 | MHz |
| GTL+ | 300 | 250 | 200 | MHz |
| SSTL-3 class I | 400 | 350 | 300 | MHz |
| SSTL-3 class II | 400 | 350 | 300 | MHz |
| SSTL-2 class I | 400 | 350 | 300 | MHz |
| SSTL-2 class II | 400 | 350 | 300 | MHz |
| SSTL-18 class I | 400 | 350 | 300 | MHz |
| SSTL-18 class II | 400 | 350 | 300 | MHz |
| 1.5-V HSTL class I | 400 | 350 | 300 | MHz |
| 1.5-V HSTL class II | 400 | 350 | 300 | MHz |
| 1.8-V HSTL class I | 400 | 350 | 300 | MHz |
| 1.8-V HSTL class II | 400 | 350 | 300 | MHz |
| 3.3-V PCI | 420 | 381 | 347 | MHz |

*Table 4–103. Stratix Maximum Input Clock Rate for CLK[0, 2, 9, 11] Pins in Flip-Chip Packages (Part 2 of 2)*

| I/O Standard | -5 Speed Grade | -6 Speed Grade | -7 Speed Grade | Unit |
|---|---|---|---|---|
| 3.3-V PCI-X 1.0 | 420 | 381 | 347 | MHz |
| Compact PCI | 420 | 381 | 347 | MHz |
| AGP 1× | 303 | 303 | 261 | MHz |
| AGP 2× | 303 | 303 | 261 | MHz |
| CTT | 300 | 250 | 200 | MHz |
| Differential HSTL | 400 | 350 | 300 | MHz |
| LVDS *(1)* | 717 | 717 | 640 | MHz |
| LVPECL *(1)* | 717 | 717 | 640 | MHz |
| PCML *(1)* | 400 | 375 | 350 | MHz |
| HyperTransport technology *(1)* | 717 | 717 | 640 | MHz |

*Table 4–104. Stratix Maximum Input Clock Rate for CLK[1, 3, 8, 10] Pins in Flip-Chip Packages (Part 1 of 2)*

| I/O Standard | -5 Speed Grade | -6 Speed Grade | -7 Speed Grade | Unit |
|---|---|---|---|---|
| LVTTL | 375 | 325 | 275 | MHz |
| 2.5 V | 375 | 325 | 275 | MHz |
| 1.8 V | 375 | 325 | 275 | MHz |
| 1.5 V | 375 | 325 | 275 | MHz |
| LVCMOS | 375 | 325 | 275 | MHz |
| GTL | 300 | 250 | 200 | MHz |
| GTL+ | 300 | 250 | 200 | MHz |
| SSTL-3 class I | 350 | 300 | 250 | MHz |
| SSTL-3 class II | 350 | 300 | 250 | MHz |
| SSTL-2 class I | 350 | 300 | 250 | MHz |
| SSTL-2 class II | 350 | 300 | 250 | MHz |
| SSTL-18 class I | 350 | 300 | 250 | MHz |
| SSTL-18 class II | 350 | 300 | 250 | MHz |
| 1.5-V HSTL class I | 350 | 300 | 250 | MHz |
| 1.5-V HSTL class II | 350 | 300 | 250 | MHz |
| 1.8-V HSTL class I | 350 | 300 | 250 | MHz |
| 1.8-V HSTL class II | 350 | 300 | 250 | MHz |

*Table 4–104. Stratix Maximum Input Clock Rate for CLK[1, 3, 8, 10] Pins in Flip-Chip Packages (Part 2 of 2)*

| I/O Standard | -5 Speed Grade | -6 Speed Grade | -7 Speed Grade | Unit |
|---|---|---|---|---|
| 3.3-V PCI | 375 | 325 | 275 | MHz |
| 3.3-V PCI-X 1.0 | 375 | 325 | 275 | MHz |
| Compact PCI | 375 | 325 | 275 | MHz |
| AGP 1× | 375 | 325 | 275 | MHz |
| AGP 2× | 375 | 325 | 275 | MHz |
| CTT | 300 | 250 | 200 | MHz |
| Differential HSTL | 350 | 300 | 250 | MHz |
| LVDS *(1)* | 500 | 422 | 311 | MHz |
| LVPECL *(1)* | 311 | 311 | 311 | MHz |
| PCML *(1)* | 275 | 250 | 175 | MHz |
| HyperTransport technology *(1)* | 350 | 350 | 350 | MHz |

*Table 4–105. Stratix Maximum Input Clock Rate for CLK[7..4] & CLK[15..12] Pins in Wire-Bond Packages (Part 1 of 2) Note (2)*

| I/O Standard | -5 Speed Grade | -6 Speed Grade | -7 Speed Grade | Unit |
|---|---|---|---|---|
| LVTTL |  | 422 | 390 | MHz |
| 2.5 V |  | 422 | 390 | MHz |
| 1.8 V |  | 422 | 390 | MHz |
| 1.5 V |  | 422 | 390 | MHz |
| LVCMOS |  | 422 | 390 | MHz |
| GTL |  | 250 | 200 | MHz |
| GTL+ |  | 250 | 200 | MHz |
| SSTL-3 class I |  | 300 | 250 | MHz |
| SSTL-3 class II |  | 300 | 250 | MHz |
| SSTL-2 class I |  | 300 | 250 | MHz |
| SSTL-2 class II |  | 300 | 250 | MHz |
| SSTL-18 class I |  | 300 | 250 | MHz |
| SSTL-18 class II |  | 300 | 250 | MHz |
| 1.5-V HSTL class I |  | 300 | 180 | MHz |
| 1.5-V HSTL class II |  | 300 | 180 | MHz |
| 1.8-V HSTL class I |  | 300 | 180 | MHz |

*Table 4–105. Stratix Maximum Input Clock Rate for CLK[7..4] & CLK[15..12] Pins in Wire-Bond Packages (Part 2 of 2) Note (2)*

| I/O Standard | -5 Speed Grade | -6 Speed Grade | -7 Speed Grade | Unit |
|---|---|---|---|---|
| 1.8-V HSTL class II | | 300 | 180 | MHz |
| 3.3-V PCI | | 381 | 347 | MHz |
| 3.3-V PCI-X 1.0 | | 381 | 347 | MHz |
| Compact PCI | | 381 | 347 | MHz |
| AGP 1× | | 303 | 261 | MHz |
| AGP 2× | | 303 | 261 | MHz |
| CTT | | 250 | 180 | MHz |
| Differential HSTL | | 300 | 180 | MHz |
| LVDS *(1)* | | 422 | 400 | MHz |
| LVPECL *(1)* | | 422 | 400 | MHz |
| PCML *(1)* | | 215 | 200 | MHz |
| HyperTransport technology *(1)* | | 422 | 400 | MHz |

*Table 4–106. Stratix Maximum Input Clock Rate for CLK[0, 2, 9, 11] Pins in Wire-Bond Packages (Part 1 of 2) Note (2)*

| I/O Standard | -5 Speed Grade | -6 Speed Grade | -7 Speed Grade | Unit |
|---|---|---|---|---|
| LVTTL | | 422 | 390 | MHz |
| 2.5 V | | 422 | 390 | MHz |
| 1.8 V | | 422 | 390 | MHz |
| 1.5 V | | 422 | 390 | MHz |
| LVCMOS | | 422 | 390 | MHz |
| GTL | | 250 | 200 | MHz |
| GTL+ | | 250 | 200 | MHz |
| SSTL-3 class I | | 350 | 300 | MHz |
| SSTL-3 class II | | 350 | 300 | MHz |
| SSTL-2 class I | | 350 | 300 | MHz |
| SSTL-2 class II | | 350 | 300 | MHz |
| SSTL-18 class I | | 350 | 300 | MHz |
| SSTL-18 class II | | 350 | 300 | MHz |
| 1.5-V HSTL class I | | 350 | 300 | MHz |
| 1.5-V HSTL class II | | 350 | 300 | MHz |

*Table 4–106. Stratix Maximum Input Clock Rate for CLK[0, 2, 9, 11] Pins in Wire-Bond Packages (Part 2 of 2)* *Note (2)*

| I/O Standard | -5 Speed Grade | -6 Speed Grade | -7 Speed Grade | Unit |
|---|---|---|---|---|
| 1.8-V HSTL class I | | 350 | 300 | MHz |
| 1.8-V HSTL class II | | 350 | 300 | MHz |
| 3.3-V PCI | | 381 | 347 | MHz |
| 3.3-V PCI-X 1.0 | | 381 | 347 | MHz |
| Compact PCI | | 381 | 347 | MHz |
| AGP 1× | | 303 | 261 | MHz |
| AGP 2× | | 303 | 261 | MHz |
| CTT | | 250 | 200 | MHz |
| Differential HSTL | | 350 | 300 | MHz |
| LVDS *(1)* | | 717 | 640 | MHz |
| LVPECL *(1)* | | 717 | 640 | MHz |
| PCML *(1)* | | 375 | 350 | MHz |
| HyperTransport technology *(1)* | | 717 | 640 | MHz |

*Table 4–107. Stratix Maximum Input Clock Rate for CLK[1, 3, 8, 10] Pins in Wire-Bond Packages (Part 1 of 2)* *Note (2)*

| I/O Standard | -5 Speed Grade | -6 Speed Grade | -7 Speed Grade | Unit |
|---|---|---|---|---|
| LVTTL | | 210 | 175 | MHz |
| 2.5 V | | 210 | 175 | MHz |
| 1.8 V | | 210 | 175 | MHz |
| 1.5 V | | 210 | 175 | MHz |
| LVCMOS | | 210 | 175 | MHz |
| GTL | | 180 | 150 | MHz |
| GTL+ | | 180 | 150 | MHz |
| SSTL-3 class I | | 200 | 185 | MHz |
| SSTL-3 class II | | 200 | 185 | MHz |
| SSTL-2 class I | | 200 | 185 | MHz |
| SSTL-2 class II | | 200 | 185 | MHz |
| SSTL-18 class I | | 200 | 185 | MHz |
| SSTL-18 class II | | 200 | 185 | MHz |
| 1.5-V HSTL class I | | 200 | 185 | MHz |

*Table 4–107. Stratix Maximum Input Clock Rate for CLK[1, 3, 8, 10] Pins in Wire-Bond Packages (Part 2 of 2) Note (2)*

| I/O Standard | -5 Speed Grade | -6 Speed Grade | -7 Speed Grade | Unit |
|---|---|---|---|---|
| 1.5-V HSTL class II | | 200 | 185 | MHz |
| 1.8-V HSTL class I | | 200 | 185 | MHz |
| 1.8-V HSTL class II | | 200 | 185 | MHz |
| 3.3-V PCI | | 210 | 175 | MHz |
| 3.3-V PCI-X 1.0 | | 210 | 175 | MHz |
| Compact PCI | | 210 | 175 | MHz |
| AGP 1× | | 210 | 175 | MHz |
| AGP 2× | | 210 | 175 | MHz |
| CTT | | 250 | 200 | MHz |
| Differential HSTL | | 200 | 185 | MHz |
| LVDS *(1)* | | 311 | 275 | MHz |
| LVPECL *(1)* | | 311 | 275 | MHz |
| PCML *(1)* | | 200 | 175 | MHz |
| HyperTransport technology *(1)* | | 311 | 275 | MHz |

***Notes to Tables 4–102 through 4–107:***

(1) These parameters are only available on row I/O pins.

(2) The -5 speed grade is not available in wire-bond packages.

Tables 4–108 through 4–111 show the maximum output clock rate for column and row pins in Stratix devices.

*Table 4–108. Stratix Maximum Output Clock Rate for PLL[5, 6, 11, 12] Pins in Flip-Chip Packages (Part 1 of 2)*

| I/O Standard | -5 Speed Grade | -6 Speed Grade | -7 Speed Grade | Unit |
|---|---|---|---|---|
| LVTTL | 350 | 300 | 250 | MHz |
| 2.5 V | 350 | 300 | 300 | MHz |
| 1.8 V | 250 | 250 | 250 | MHz |
| 1.5 V | 225 | 200 | 200 | MHz |
| LVCMOS | 350 | 300 | 250 | MHz |
| GTL | 200 | 167 | 125 | MHz |
| GTL+ | 200 | 167 | 125 | MHz |
| SSTL-3 class I | 167 | 150 | 133 | MHz |

***Table 4–108. Stratix Maximum Output Clock Rate for PLL[5, 6, 11, 12] Pins in Flip-Chip Packages (Part 2 of 2)***

| I/O Standard | -5 Speed Grade | -6 Speed Grade | -7 Speed Grade | Unit |
|---|---|---|---|---|
| SSTL-3 class II | 167 | 150 | 133 | MHz |
| SSTL-2 class I | 200 | 200 | 167 | MHz |
| SSTL-2 class II | 200 | 200 | 167 | MHz |
| SSTL-18 class I | 150 | 133 | 133 | MHz |
| SSTL-18 class II | 150 | 133 | 133 | MHz |
| 1.5-V HSTL class I | 250 | 225 | 200 | MHz |
| 1.5-V HSTL class II | 250 | 200 | 200 | MHz |
| 1.8-V HSTL class I | 250 | 225 | 200 | MHz |
| 1.8-V HSTL class II | 250 | 200 | 200 | MHz |
| 3.3-V PCI | 350 | 300 | 250 | MHz |
| 3.3-V PCI-X 1.0 | 350 | 300 | 250 | MHz |
| Compact PCI | 350 | 300 | 250 | MHz |
| AGP 1× | 350 | 300 | 250 | MHz |
| AGP 2× | 350 | 300 | 250 | MHz |
| CTT | 200 | 200 | 200 | MHz |
| Differential HSTL | 225 | 200 | 200 | MHz |
| Differential SSTL-2 *(1)* | 200 | 200 | 167 | MHz |
| LVDS *(2)* | 500 | 500 | 500 | MHz |
| LVPECL *(2)* | 500 | 500 | 500 | MHz |
| PCML *(2)* | 350 | 350 | 350 | MHz |
| HyperTransport technology *(2)* | 350 | 350 | 350 | MHz |

***Table 4–109. Stratix Maximum Output Clock Rate for PLL[1, 2, 3, 4] Pins in Flip-Chip Packages (Part 1 of 2)***

| I/O Standard | -5 Speed Grade | -6 Speed Grade | -7 Speed Grade | Unit |
|---|---|---|---|---|
| LVTTL | 400 | 350 | 300 | MHz |
| 2.5 V | 400 | 350 | 300 | MHz |
| 1.8 V | 400 | 350 | 300 | MHz |
| 1.5 V | 350 | 300 | 300 | MHz |
| LVCMOS | 350 | 300 | 300 | MHz |
| GTL | 200 | 167 | 125 | MHz |

**Table 4–109. Stratix Maximum Output Clock Rate for PLL[1, 2, 3, 4] Pins in Flip-Chip Packages (Part 2 of 2)**

| I/O Standard | -5 Speed Grade | -6 Speed Grade | -7 Speed Grade | Unit |
|---|---|---|---|---|
| GTL+ | 200 | 167 | 125 | MHz |
| SSTL-3 class I | 167 | 150 | 133 | MHz |
| SSTL-3 class II | 167 | 150 | 133 | MHz |
| SSTL-2 class I | 150 | 133 | 133 | MHz |
| SSTL-2 class II | 150 | 133 | 133 | MHz |
| SSTL-18 class I | 150 | 133 | 133 | MHz |
| SSTL-18 class II | 150 | 133 | 133 | MHz |
| HSTL class I | 250 | 225 | 200 | MHz |
| HSTL class II | 225 | 225 | 200 | MHz |
| 3.3-V PCI | 400 | 350 | 300 | MHz |
| 3.3-V PCI-X 1.0 | 400 | 350 | 300 | MHz |
| Compact PCI | 400 | 350 | 300 | MHz |
| AGP 1× | 400 | 350 | 300 | MHz |
| AGP 2× | 400 | 350 | 300 | MHz |
| CTT | 400 | 350 | 300 | MHz |
| Differential HSTL | 225 | 225 | 200 | MHz |
| Differential SSTL-2 *(1)* | 200 | 200 | 167 | MHz |
| LVDS *(2)* | 500 | 500 | 500 | MHz |
| LVPECL *(2)* | 500 | 500 | 500 | MHz |
| PCML *(2)* | 420 | 420 | 420 | MHz |
| HyperTransport technology *(2)* | 420 | 420 | 420 | MHz |

**Table 4–110. Stratix Maximum Output Clock Rate for PLL[5, 6, 11, 12] Pins in Wire-Bond Packages (Part 1 of 2)** *Note (3)*

| I/O Standard | -5 Speed Grade | -6 Speed Grade | -7 Speed Grade | Unit |
|---|---|---|---|---|
| LVTTL | | 175 | 150 | MHz |
| 2.5 V | | 175 | 150 | MHz |
| 1.8 V | | 175 | 150 | MHz |
| 1.5 V | | 175 | 150 | MHz |
| LVCMOS | | 175 | 150 | MHz |
| GTL | | 125 | 100 | MHz |

***Table 4–110. Stratix Maximum Output Clock Rate for PLL[5, 6, 11, 12] Pins in Wire-Bond Packages (Part 2 of 2)*** *Note (3)*

| I/O Standard | -5 Speed Grade | -6 Speed Grade | -7 Speed Grade | Unit |
|---|---|---|---|---|
| GTL+ | | 125 | 100 | MHz |
| SSTL-3 class I | | 110 | 90 | MHz |
| SSTL-3 class II | | 133 | 125 | MHz |
| SSTL-2 class I | | 166 | 133 | MHz |
| SSTL-2 class II | | 133 | 100 | MHz |
| SSTL-18 class I | | 110 | 100 | MHz |
| SSTL-18 class II | | 110 | 100 | MHz |
| HSTL class I | | 167 | 167 | MHz |
| HSTL class II | | 167 | 133 | MHz |
| 3.3-V PCI | | 175 | 150 | MHz |
| 3.3-V PCI-X 1.0 | | 175 | 150 | MHz |
| Compact PCI | | 175 | 150 | MHz |
| AGP 1× | | 175 | 150 | MHz |
| AGP 2× | | 175 | 150 | MHz |
| CTT | | 125 | 100 | MHz |
| Differential HSTL | | 167 | 133 | MHz |
| Differential SSTL-2 *(1)* | | 110 | 100 | MHz |
| LVDS *(2)* | | 311 | 275 | MHz |
| LVPECL *(2)* | | 311 | 275 | MHz |
| PCML *(2)* | | 250 | 200 | MHz |
| HyperTransport technology *(2)* | | 311 | 275 | MHz |

***Table 4–111. Stratix Maximum Output Clock Rate for PLL[1, 2, 3, 4] Pins in Wire-Bond Packages (Part 1 of 2)*** *Note (3)*

| I/O Standard | -5 Speed Grade | -6 Speed Grade | -7 Speed Grade | Unit |
|---|---|---|---|---|
| LVTTL | | 200 | 175 | MHz |
| 2.5 V | | 200 | 175 | MHz |
| 1.8 V | | 200 | 175 | MHz |
| 1.5 V | | 200 | 175 | MHz |
| LVCMOS | | 200 | 175 | MHz |
| GTL | | 125 | 100 | MHz |

*Table 4–111. Stratix Maximum Output Clock Rate for PLL[1, 2, 3, 4] Pins in Wire-Bond Packages (Part 2 of 2) Note (3)*

| I/O Standard | -5 Speed Grade | -6 Speed Grade | -7 Speed Grade | Unit |
|---|---|---|---|---|
| GTL+ | | 125 | 100 | MHz |
| SSTL-3 class I | | 110 | 90 | MHz |
| SSTL-3 class II | | 150 | 133 | MHz |
| SSTL-2 class I | | 90 | 80 | MHz |
| SSTL-2 class II | | 110 | 100 | MHz |
| SSTL-18 class I | | 110 | 100 | MHz |
| SSTL-18 class II | | 110 | 100 | MHz |
| 1.5-V HSTL class I | | 225 | 200 | MHz |
| 1.5-V HSTL class II | | 200 | 167 | MHz |
| 1.8-V HSTL class I | | 225 | 200 | MHz |
| 1.8-V HSTL class II | | 200 | 167 | MHz |
| 3.3-V PCI | | 200 | 175 | MHz |
| 3.3-V PCI-X 1.0 | | 200 | 175 | MHz |
| Compact PCI | | 200 | 175 | MHz |
| AGP 1× | | 200 | 175 | MHz |
| AGP 2× | | 200 | 175 | MHz |
| CTT | | 125 | 100 | MHz |
| Differential HSTL | | 200 | 167 | MHz |
| Differential SSTL-2 *(1)* | | 110 | 100 | MHz |
| LVDS *(2)* | | 400 | 311 | MHz |
| LVPECL *(1)* | | 400 | 311 | MHz |
| PCML *(1)* | | 250 | 250 | MHz |
| HyperTransport technology *(1)* | | 420 | 400 | MHz |

*Notes to Tables 4–108 through 4–111:*

(1) Differential SSTL-2 outputs are only available on column I/O pins.
(2) These parameters are only available on row I/O pins.
(3) The -5 speed grade is not available in wire-bond packages.

## High-Speed I/O Timing

Table 4–112 provides high-speed timing specifications definitions.

*Table 4–112. High-Speed Timing Specifications & Terminology*

| High-Speed Timing Specification | Terminology |
|---|---|
| $t_C$ | High-speed receiver/transmitter input and output clock period. |
| $f_{HSCLK}$ | High-speed receiver/transmitter input and output clock frequency. |
| $t_{RISE}$ | Low-to-high transmission time. |
| $t_{FALL}$ | High-to-low transmission time. |
| Timing unit interval (TUI) | The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency × Multiplication Factor) = $t_C/w$). |
| $f_{HSDR}$ | Maximum LVDS data transfer rate ($f_{HSDR}$ = 1/TUI). |
| Channel-to-channel skew (TCCS) | The timing difference between the fastest and slowest output edges, including $t_{CO}$ variation and clock skew. The clock is included in the TCCS measurement. |
| Sampling window (SW) | The period of time during which the data must be valid in order for you to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window.<br>SW = $t_{SW}$ (max) – $t_{SW}$ (min). |
| Input jitter (peak-to-peak) | Peak-to-peak input jitter on high-speed PLLs. |
| Output jitter (peak-to-peak) | Peak-to-peak output jitter on high-speed PLLs. |
| $t_{DUTY}$ | Duty cycle on high-speed transmitter output clock. |
| $t_{LOCK}$ | Lock time for high-speed transmitter and receiver PLLs. |

Tables 4–113 and 4–114 show the high-speed I/O timing for Stratix devices.

*Table 4–113. High-Speed I/O Specifications for Flip-Chip Packages (Part 1 of 2)* *Notes (1), (2)*

| Symbol | Conditions | -5 Speed Grade | | | -6 Speed Grade | | | -7 Speed Grade | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{HSCLK}$ (Clock frequency) (LVDS, LVPECL, HyperTransport technology) | $W = 10$ | 30 | | 84 | 30 | | 84 | 30 | | 62.4 | MHz |
| | $W = 8$ | 37.5 | | 105 | 37.5 | | 105 | 37.5 | | 78 | MHz |
| | $W = 7$ | 42.9 | | 120 | 42.9 | | 120 | 42.9 | | 89.14 | MHz |
| | $W = 4$ | 75 | | 210 | 75 | | 210 | 75 | | 156 | MHz |
| | $W = 2$ | 150 | | 420 | 150 | | 420 | 150 | | 231 | MHz |
| | $W = 1$ (LVDS and LVPECL only) | 300 | | 717 | 300 | | 717 | 300 | | 462 | MHz |
| $f_{HSDR}$ Device operation (LVDS, LVPECL, HyperTransport technology) | $J = 10$ | 300 | | 840 | 300 | | 840 | 300 | | 624 | Mbps |
| | $J = 8$ | 300 | | 840 | 300 | | 840 | 300 | | 624 | Mbps |
| | $J = 7$ | 300 | | 840 | 300 | | 840 | 300 | | 624 | Mbps |
| | $J = 4$ | 300 | | 840 | 300 | | 840 | 300 | | 624 | Mbps |
| | $J = 2$ | 100 | | 462 | 100 | | 462 | 100 | | 462 | Mbps |
| | $J = 1$ (LVDS and LVPECL only) | 100 | | 462 | 100 | | 462 | 100 | | 462 | Mbps |
| $f_{HSCLK}$ (Clock frequency) (PCML) | $W = 10$ | 30 | | 40 | 30 | | 40 | 30 | | 31.1 | MHz |
| | $W = 8$ | 37.5 | | 50 | 37.5 | | 50 | 37.5 | | 38.87 | MHz |
| | $W = 7$ | 42.9 | | 57.14 | 42.9 | | 57.14 | 42.9 | | 44.43 | MHz |
| | $W = 4$ | 75 | | 100 | 75 | | 100 | 75 | | 77.75 | MHz |
| | $W = 2$ | 50 | | 200 | 50 | | 200 | 50 | | 150 | MHz |
| | $W = 1$ | 100 | | 250 | 100 | | 250 | 100 | | 200 | MHz |
| $f_{HSDR}$ Device operation (PCML) | $J = 10$ | 300 | | 400 | 300 | | 400 | 300 | | 311 | Mbps |
| | $J = 8$ | 300 | | 400 | 300 | | 400 | 300 | | 311 | Mbps |
| | $J = 7$ | 300 | | 400 | 300 | | 400 | 300 | | 311 | Mbps |
| | $J = 4$ | 300 | | 400 | 300 | | 400 | 300 | | 311 | Mbps |
| | $J = 2$ | 100 | | 400 | 100 | | 400 | 100 | | 300 | Mbps |
| | $J = 1$ | 100 | | 250 | 100 | | 250 | 100 | | 200 | Mbps |
| TCCS | All | | | ±100 | | | ±100 | | | ±150 | ps |

| *Table 4–113. High-Speed I/O Specifications for Flip-Chip Packages (Part 2 of 2) Notes (1), (2)* | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Conditions** | **-5 Speed Grade** | | | **-6 Speed Grade** | | | **-7 Speed Grade** | | | **Unit** |
| | | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | |
| SW | PCML (*J* = 4, 7, 8, 10) | | | 750 | | | 750 | | | 800 | ps |
| | PCML (*J* = 2) | | | 900 | | | 900 | | | 1,200 | ps |
| | PCML (*J* = 1) | | | 1,500 | | | 1,500 | | | 1,700 | ps |
| | LVDS and LVPECL (*J* = 1) | | | 500 | | | 500 | | | 550 | ps |
| | LVDS, LVPECL, HyperTransport technology (*J* = 2 through 10) | | | 440 | | | 440 | | | 500 | ps |
| Input jitter tolerance (peak-to-peak) | All | | | 250 | | | 250 | | | 250 | ps |
| Output jitter (peak-to-peak) | All | | | 160 | | | 160 | | | 200 | ps |
| Output $t_{RISE}$ | LVDS | 80 | 110 | 120 | 80 | 110 | 120 | 80 | 110 | 120 | ps |
| | HyperTransport technology | 110 | 170 | 200 | 110 | 170 | 200 | 120 | 170 | 200 | ps |
| | LVPECL | 90 | 130 | 150 | 90 | 130 | 150 | 100 | 135 | 150 | ps |
| | PCML | 80 | 110 | 135 | 80 | 110 | 135 | 80 | 110 | 135 | ps |
| Output $t_{FALL}$ | LVDS | 80 | 110 | 120 | 80 | 110 | 120 | 80 | 110 | 120 | ps |
| | HyperTransport technology | 110 | 170 | 200 | 110 | 170 | 200 | 110 | 170 | 200 | ps |
| | LVPECL | 90 | 130 | 160 | 90 | 130 | 160 | 100 | 135 | 160 | ps |
| | PCML | 105 | 140 | 175 | 105 | 140 | 175 | 110 | 145 | 175 | ps |
| $t_{DUTY}$ | LVDS (*J* = 2 through 10) | 47.5 | 50 | 52.5 | 47.5 | 50 | 52.5 | 47.5 | 50 | 52.5 | % |
| | LVDS (*J* =1) and LVPECL, PCML, HyperTransport technology | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | % |
| $t_{LOCK}$ | All | | | 100 | | | 100 | | | 100 | µs |

*Notes for Table 4–113:*

(1) When J = 4, 7, 8, and 10, the SERDES block is used.

(2) When J = 2 or J = 1, the SERDES is bypassed.

*Table 4–114. High-Speed I/O Specifications for Wire-Bond Packages (Part 1 of 2)*

| Symbol | Conditions | -6 Speed Grade |  |  | -7 Speed Grade |  |  | Unit |
|---|---|---|---|---|---|---|---|---|
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| $f_{HSCLK}$ (clock frequency) (LVDS,LVPECL, HyperTransport technology) | W = 10 | 30 |  | 62.4 | 30 |  | 46 | MHz |
|  | W = 8 | 37.5 |  | 78 | 37.5 |  | 57.5 | MHz |
|  | W = 7 | 42.9 |  | 89.14 | 42.9 |  | 65.71 | MHz |
|  | W = 4 | 75 |  | 156 | 75 |  | 115 | MHz |
|  | W = 2 | 50 |  | 231 | 50 |  | 230 | MHz |
|  | W = 1 (LVDS and LVPECL only) | 100 |  | 311 | 100 |  | 311 | MHz |
| Device operation, $f_{HSDR}$ (LVDS,LVPECL, HyperTransport technology) | J = 10 | 300 |  | 624 | 300 |  | 460 | Mbps |
|  | J = 8 | 300 |  | 624 | 300 |  | 460 | Mbps |
|  | J = 7 | 300 |  | 624 | 300 |  | 460 | Mbps |
|  | J = 4 | 300 |  | 624 | 300 |  | 460 | Mbps |
|  | J = 2 | 100 |  | 462 | 100 |  | 460 | Mbps |
|  | J = 1 (LVDS and LVPECL only) | 100 |  | 311 | 100 |  | 270 | Mbps |
| $f_{HSCLK}$ (clock frequency) (PCML) | W = 10 | 30 |  | 31.1 |  |  |  | MHz |
|  | W = 8 | 37.5 |  | 38.87 |  |  |  | MHz |
|  | W = 7 | 42.9 |  | 44.43 |  |  |  | MHz |
|  | W = 4 | 75 |  | 77.75 |  |  |  | MHz |
|  | W = 2 | 50 |  | 150 | 50 |  | 150 | MHz |
|  | W = 1 | 100 |  | 200 | 100 |  | 200 | MHz |
| Device operation, $f_{HSDR}$ (PCML) | J = 10 | 300 |  | 311 |  |  |  | Mbps |
|  | J = 8 | 300 |  | 311 |  |  |  | Mbps |
|  | J = 7 | 300 |  | 311 |  |  |  | Mbps |
|  | J = 4 | 300 |  | 311 |  |  |  | Mbps |
|  | J = 2 | 100 |  | 300 | 100 |  | 155 | Mbps |
|  | J = 1 | 100 |  | 200 | 100 |  | 155 | Mbps |
| TCCS | All |  |  | ± 200 |  |  | ± 200 | ps |

*Table 4–114. High-Speed I/O Specifications for Wire-Bond Packages (Part 2 of 2)*

| Symbol | Conditions | -6 Speed Grade | | | -7 Speed Grade | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| SW | PCML (J = 4, 7, 8, 10) only | | | 800 | | | 800 | ps |
| | PCML (J = 2) only | | | 1,200 | | | 1,200 | ps |
| | PCML (J = 1) only | | | 1,700 | | | 1,700 | ps |
| | LVDS and LVPECL (J = 1) only | | | 550 | | | 550 | ps |
| | LVDS, LVPECL, HyperTransport technology (J = 2..10) only | | | 500 | | | 500 | ps |
| Input jitter tolerance (peak-to-peak) | All | | | 250 | | | 250 | ps |
| Output jitter (peak-to-peak) | All | | | 200 | | | 200 | ps |
| Output $t_{RISE}$ | LVDS | 80 | 110 | 120 | 80 | 110 | 120 | ps |
| | HyperTransport technology | 120 | 170 | 200 | 120 | 170 | 200 | ps |
| | LVPECL | 100 | 135 | 150 | 100 | 135 | 150 | ps |
| | PCML | 80 | 110 | 135 | 80 | 110 | 135 | ps |
| Output $t_{FALL}$ | LVDS | 80 | 110 | 120 | 80 | 110 | 120 | ps |
| | HyperTransport | 110 | 170 | 200 | 110 | 170 | 200 | ps |
| | LVPECL | 100 | 135 | 160 | 100 | 135 | 160 | ps |
| | PCML | 110 | 145 | 175 | 110 | 145 | 175 | ps |
| $t_{DUTY}$ | LVDS (J =2..10) only | 47.5 | 50 | 52.5 | 47.5 | 50 | 52.5 | % |
| | LVDS (J =1) and LVPECL, PCML, HyperTransport technology | 45 | 50 | 55 | 45 | 50 | 55 | % |
| $t_{LOCK}$ | All | | | 100 | | | 100 | us |

## PLL Timing

Tables 4–115 and 4–116 describe the Stratix device enhanced PLL specifications.

*Table 4–115. Enhanced PLL Specifications for -5 & -6 Speed Grades (Part 1 of 2)*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{IN}$ | Input clock frequency | 3 *(1)* | | 462 | MHz |
| $f_{INDUTY}$ | Input clock duty cycle | 40 | | 60 | % |
| $f_{EINDUTY}$ | External feedback clock input duty cycle | 40 | | 60 | % |
| $t_{INJITTER}$ | Input clock cycle-to-cycle jitter | | | ±200 | ps |
| $t_{EINJITTER}$ | External feedback clock cycle-to-cycle jitter | | | ±200 | ps |
| $t_{FCOMP}$ | External feedback clock compensation time *(2)* | | | 6 | ns |
| $f_{OUT}$ | PLL output frequency | 0.6 | | 462 | MHz |
| $t_{OUTDUTY}$ | Duty cycle for external clock output (when set to 50%) | 45 | | 55 | % |
| $t_{JITTER}$ | Cycle-to-cycle jitter for external or internal global or regional clock output *(3)* | | | ±100 ps or ±15 mUI, whichever is higher | ps or mUI |
| $t_{CONFIG5,6}$ | Time required to reconfigure the scan chains for PLLs 5 and 6 | | | $289/f_{SCANCLK}$ | |
| $t_{CONFIG11,12}$ | Time required to reconfigure the scan chains for PLLs 11 and 12 | | | $193/f_{SCANCLK}$ | |
| $t_{SCANCLK}$ | `scanclk` frequency *(4)* | | | 33 | MHz |
| $t_{DLOCK}$ | Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) *(5)* | *(6)* | | 100 | µs |
| $t_{LOCK}$ | Time required to lock from end of device configuration | 10 | | 1,000 | µs |
| $f_{VCO}$ | PLL internal VCO operating range | 300 | | 800 | MHz |
| $t_{LSKEW}$ | Clock skew between two external clock outputs driven by the same counter | | ±50 | | ps |
| $t_{SKEW}$ | Clock skew between two external clock outputs driven by the different counters with the same settings | | ±75 | | ps |

### *Table 4–115. Enhanced PLL Specifications for -5 & -6 Speed Grades (Part 2 of 2)*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{SS}$ | Spread spectrum modulation frequency | 30 | | 150 | kHz |
| % spread | Percentage spread for spread spectrum frequency *(7)* | 0 | 0.5 | | % |

### *Table 4–116. Enhanced PLL Specifications for -7 Speed Grade (Part 1 of 2)*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{IN}$ | Input clock frequency | 3 *(1)* | | 462 | MHz |
| $f_{INDUTY}$ | Input clock duty cycle | 40 | | 60 | % |
| $f_{EINDUTY}$ | External feedback clock input duty cycle | 40 | | 60 | % |
| $t_{INJITTER}$ | Input clock cycle-to-cycle jitter | | | ±200 | ps |
| $t_{EINJITTER}$ | External feedback clock cycle-to-cycle jitter | | | ±200 | ps |
| $t_{FCOMP}$ | External feedback clock compensation time *(2)* | | | 6 | ns |
| $f_{OUT}$ | PLL output frequency | 0.6 | | 462 | MHz |
| $t_{OUTDUTY}$ | Duty cycle for external clock output (when set to 50%) | 45 | | 55 | % |
| $t_{JITTER}$ | Cycle-to-cycle jitter for external or internal global or regional clock output *(3)* | | | ±100 ps or ±15 mUI, whichever is higher | ps or mUI |
| $t_{CONFIG5,6}$ | Time required to reconfigure the scan chains for PLLs 5 and 6 | | | $289/f_{SCANCLK}$ | |
| $t_{CONFIG11,12}$ | Time required to reconfigure the scan chains for PLLs 11 and 12 | | | $193/f_{SCANCLK}$ | |
| $t_{SCANCLK}$ | `scanclk` frequency *(4)* | | | 100 | MHz |
| $t_{DLOCK}$ | Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) *(5)* | *(6)* | | 100 | μs |
| $t_{LOCK}$ | Time required to lock from end of device configuration | 10 | | 1,000 | μs |
| $f_{VCO}$ | PLL internal VCO operating range | 300 | | 600 | MHz |
| $t_{LSKEW}$ | Clock skew between two external clock outputs driven by the same counter | | ±50 | | ps |
| $t_{SKEW}$ | Clock skew between two external clock outputs driven by the different counters with the same settings | | ±75 | | ps |

### Table 4–116. Enhanced PLL Specifications for -7 Speed Grade (Part 2 of 2)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{SS}$ | Spread spectrum modulation frequency | 30 | | 150 | kHz |
| % spread | Percentage spread for spread spectrum frequency *(7)* | 0 | 0.5 | | % |

*Notes to Table 4–115 and 4–116:*

(1) The minimum input clock frequency to the PFD ($f_{IN}/N$) must be at least 3 Mhz for Stratix and Stratix GX device enhanced PLLs.

(2) $t_{FCOMP}$ can also equal 50% of the input clock period multiplied by the pre-scale divider *n* (whichever is less).

(3) Actual jitter performance may vary based on the system configuration.

(4) This parameter is timing analyzed by the Quartus II software because the `scanclk` and `scandata` ports can be driven by the logic array.

(5) Total required time to reconfigure and lock is equal to $t_{DLOCK} + t_{CONFIG}$. If only post-scale counters and delays are changed, then $t_{DLOCK}$ is equal to 0.

(6) Lock time is a function of PLL configuration and may be significantly faster depending on bandwidth settings or feedback counter change increment.

(7) Exact, user-controllable value depends on the PLL settings.

Table 4–117 and 4–118 describe the Stratix and Stratix GX device fast PLL specifications.

### Table 4–117. Fast PLL Specifications for -5 & -6 Speed Grades (Part 1 of 2) Note (1)

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $f_{IN}$ | `CLKIN` frequency (for *m* = 1) *(2), (3)* | 300 | 717 | MHz |
| | `CLKIN` frequency (for *m* = 2 to 19) | 300/*m* | 1,000/*m* | MHz |
| | `CLKIN` frequency (for *m* = 20 to 32) | 15 | 1,000/*m* | MHz |
| $f_{OUT}$ | Output frequency for internal global or regional clock *(4)* | 9.375 | 420 | MHz |
| $f_{OUT\_EXT}$ | Output frequency for external clock *(3)* | 9.375 | 717 | MHz |
| $f_{VCO}$ | VCO operating frequency | 300 | 1,000 | MHz |
| $t_{INDUTY}$ | `CLKIN` duty cycle | 40 | 60 | % |
| $t_{INJITTER}$ | Cycle-to-cycle jitter for `CLKIN` pin | | ±200 | ps |
| $t_{DUTY}$ | Duty cycle for `DFFIO` 1× `CLKOUT` pin *(5)* | 45 | 55 | % |
| $t_{JITTER}$ | Cycle-to-cycle jitter for DIFFIO clock out *(5)* | | ±80 | ps |
| | Cycle-to-cycle jitter for internal global or regional clock | | ±100 ps or ±15 mUI, whichever is higher | ps or mUI |
| $t_{LOCK}$ | Time required for PLL to acquire lock | 10 | 100 | μs |

*Table 4–117. Fast PLL Specifications for -5 & -6 Speed Grades (Part 2 of 2) Note (1)*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| m | Multiplication factors for *m* counter *(6)* | 1 | 32 | Integer |
| *l*0, *l*1, *g*0 | Multiplication factors for *l*0, *l*1, and *g*0 counter *(6)*, *(7)* | 1 | 32 | Integer |

**Table 4–118. Fast PLL Specifications for -7 Speed Grade** *Note (1)*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $f_{IN}$ | `CLKIN` frequency (for *m* = 1) *(2)*, *(3)* | 300 | 460 | MHz |
| | `CLKIN` frequency (for *m* = 2 to 19) | 300/*m* | 700/*m* | MHz |
| | `CLKIN` frequency (for *m* = 20 to 32) | 15 | 700/*m* | MHz |
| $f_{OUT}$ | Output frequency for internal global or regional clock *(4)* | 9.375 | 420 | MHz |
| $f_{OUT\_EXT}$ | Output frequency for external clock *(3)* | 9.375 | 460 | MHz |
| $f_{VCO}$ | VCO operating frequency | 300 | 700 | MHz |
| $t_{INDUTY}$ | `CLKIN` duty cycle | 40 | 60 | % |
| $t_{INJITTER}$ | Cycle-to-cycle jitter for `CLKIN` pin | | ±200 | ps |
| $t_{DUTY}$ | Duty cycle for `DFFIO` 1× `CLKOUT` pin *(5)* | 45 | 55 | % |
| $t_{JITTER}$ | Cycle-to-cycle jitter for DIFFIO clock out *(5)* | | ±80 | ps |
| | Cycle-to-cycle jitter for internal global or regional clock | | ±100 ps or ±15 mUI, whichever is higher | ps or mUI |
| $t_{LOCK}$ | Time required for PLL to acquire lock | 10 | 100 | µs |
| m | Multiplication factors for *m* counter *(6)* | 1 | 32 | Integer |
| *l*0, *l*1, *g*0 | Multiplication factors for *l*0, *l*1, and *g*0 counter *(6)*, *(7)* | 1 | 32 | Integer |

***Notes to Table 4–117 and Table 4–118:***

(1) PLLs 3, 4, 9, and 10 on Stratix GX devices are only used for the HSSI block. These PLLs are not available for general-purpose programming.

(2) PLLs 7, 8, 9, and 10 support up to 717-MHz input clock frequency on `FPLL[7..10]clk` pins using differential standards. PLLs 1, 2, 3, and 4 support up to 717-MHz input clock frequency on the `CLK0`, `CLK2`, `CLK9`, and `CLK11` pins using differential standards. All other clock inputs support 462 MHz using differential standards. See "Maximum Input & Output Clock Rates" on page 4–63

(3) PLLs 7, 8, 9, and 10 in the EP1S80 device support up to 462-MHz input and output.

(4) When using the SERDES, high-speed differential I/O mode supports a maximum output frequency of 210 MHz to the global or regional clocks (i.e., the maximum data rate 840 Mbps divided by the smallest SERDES J factor of 4).

(5) This parameter is for high-speed differential I/O mode only.

(6) These counters have a maximum of 32 if programmed for 50/50 duty cycle. Otherwise, they have a maximum of 16.

(7) High-speed differential I/O mode supports *W* = 1 to 16 and *J* = 4, 7, 8, or 10.

# 5. Reference & Ordering Information

S51005-1.0

Chapter 5, Reference & Ordering Information, replaces the Stratix Family Data Sheet.

## Software

Stratix devices are supported by the Altera Quartus II design software, which provides a comprehensive environment for system-on-a-programmable-chip (SOPC) design. The Quartus II software includes HDL and schematic design entry, compilation and logic synthesis, full simulation and advanced timing analysis, SignalTap® II logic analyzer, and device configuration. See the *Design Software Selector Guide* for more details on the Quartus II software features.

The Quartus II software supports the Windows XP/2000/NT/98, Sun Solaris, Linux Red Hat v7.1 and HP-UX operating systems. It also supports seamless integration with industry-leading EDA tools through the NativeLink® interface.

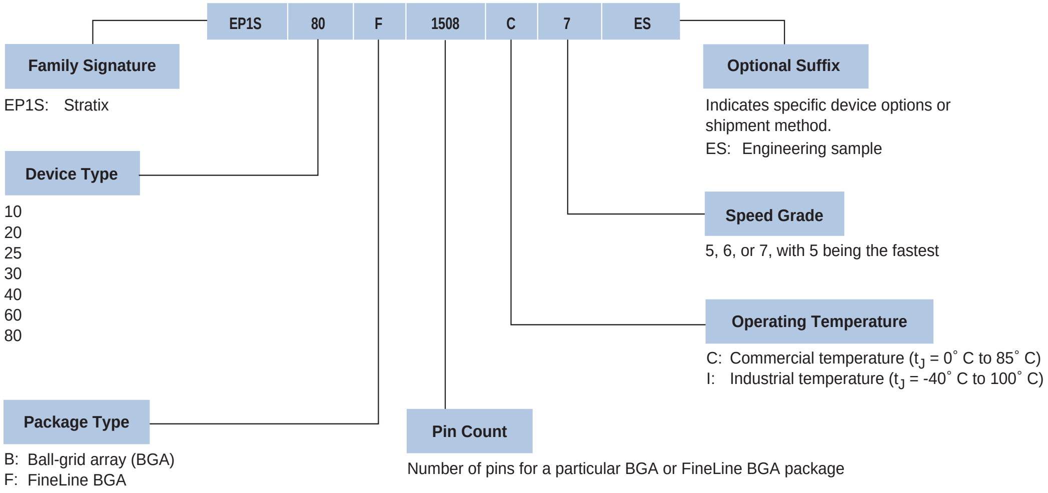
## Device Pin-Outs

Printed Device pin-outs for Stratix devices can be found in this handbook in Section II, PCB Layout Guidelines and are also available on the Altera web site at (www.altera.com).

## Ordering Information

Figure 5–1 describes the ordering codes for Stratix devices. For more information on a specific package, refer to the Chapter 8, Package Information for Stratix Devices.

*Figure 5–1. Stratix Device Packaging Ordering Information*



# Index

# Stratix Device Handbook, Volume 2

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# Contents

## Section I. Clock Management

### Chapter 1. Using General-Purpose PLLs in Stratix & Stratix GX Devices

## Section II. Memory

### Chapter 2. QDR SRAM Controller Reference Design for Stratix & Stratix GX Devices

### Chapter 3. Using TriMatrix Embedded Memory Blocks in Stratix & Stratix GX Devices

# Section III. I/O Standards

## Chapter 4. Using Selectable I/O Standards in Stratix & Stratix GX Devices

## Chapter 5. Using High-Speed Differential I/O Interfaces in Stratix Devices

## Section IV. Digital Signal Processing (DSP)

## Chapter 6. Using the DSP Blocks in Stratix & Stratix GX Devices

## Chapter 7. Implementing High-Performance DSP Functions in Stratix & Stratix GX Devices

## Section V. IP & Design Considerations

### Chapter 8. Double Data Rate I/O Signaling in Stratix & Stratix GX Devices

### Chapter 9. Using Soft Multipliers with Stratix & Stratix GX Devices

## Chapter 10. Implementing 10-Gigabit Ethernet Using Stratix Devices

## Chapter 11. Implementing SFI-4 in Stratix Devices

## Chapter 12. Transitioning APEX Designs to Stratix Devices

## Section VI. Configuration & Remote System Upgrades

### Chapter 13. Configuring Stratix & Stratix GX Devices

## Chapter 14. Using Altera Enhanced Configuration Devices

## Chapter 15. Using Remote System Configuration with Stratix & Stratix GX Devices

## Index

# Chapter Revision Dates

The chapters in this book, *Stratix Device Handbook, Volume 2*, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

Chapter 1. Using General-Purpose PLLs in Stratix & Stratix GX Devices
Revised: *April 2003*
Part number: *S52001-1.0*

Chapter 2. QDR SRAM Controller Reference Design for Stratix & Stratix GX Devices
Revised: *April 2003*
Part number: *S52002-1.0*

Chapter 3. Using TriMatrix Embedded Memory Blocks in Stratix & Stratix GX Devices
Revised: *April 2003*
Part number: *S52003-1.0*

Chapter 4. Using Selectable I/O Standards in Stratix & Stratix GX Devices
Revised: *April 2003*
Part number: *S52004-1.0*

Chapter 5. Using High-Speed Differential I/O Interfaces in Stratix Devices
Revised: *May 2003*
Part number: *S52005-1.1*

Chapter 6. Using the DSP Blocks in Stratix & Stratix GX Devices
Revised: *April 2003*
Part number: *S52006-1.0*

Chapter 7. Implementing High-Performance DSP Functions in Stratix & Stratix GX Devices
Revised: *April 2003*
Part number: *S52007-1.0*

Chapter 8. Double Data Rate I/O Signaling in Stratix & Stratix GX Devices
Revised: *April 2003*
Part number: *S52008-1.0*

Chapter 9. Using Soft Multipliers with Stratix & Stratix GX Devices
Revised: *April 2003*
Part number: *S52009-1.0*

Chapter 10. Implementing 10-Gigabit Ethernet Using Stratix Devices
Revised: *April 2003*
Part number: *S52010-1.0*

Chapter 11. Implementing SFI-4 in Stratix Devices
Revised: *April 2003*
Part number: *S52011-1.0*

Chapter 12. Transitioning APEX Designs to Stratix Devices
Revised: *April 2003*
Part number: *S52012-1.0*

Chapter 13. Configuring Stratix & Stratix GX Devices
Revised: *April 2003*
Part number: *S52013-1.0*

Chapter 14. Using Altera Enhanced Configuration Devices
Revised: *April 2003*
Part number: *S52014-1.0*

Chapter 15. Using Remote System Configuration with Stratix & Stratix GX Devices
Revised: *April 2003*
Part number: *S52015-1.0*

# About this Handbook

This handbook provides comprehensive information about the Altera® Stratix family of devices.

## How to Find Information

You can find more information in the following ways:

- The Adobe Acrobat Find feature, which searches the text of a PDF document. Click the binoculars toolbar icon to open the Find dialog box.
- Acrobat bookmarks, which serve as an additional table of contents in PDF documents.
- Thumbnail icons, which provide miniature previews of each page, provide a link to the pages.
- Numerous links, shown in green text, which allow you to jump to related information.

## How to Contact Altera

For the most up-to-date information about Altera products, go to the Altera world-wide web site at www.altera.com. For technical support on this product, go to www.altera.com/mysupport. For additional information about Altera products, consult the sources shown below.

| Information Type | USA & Canada | All Other Locations |
|---|---|---|
| Technical support | www.altera.com/mysupport/ | altera.com/mysupport/ |
| | (800) 800-EPLD (3753)<br>(7:00 a.m. to 5:00 p.m. Pacific Time) | (408) 544-7000 *(1)*<br>(7:00 a.m. to 5:00 p.m. Pacific Time) |
| Product literature | www.altera.com | www.altera.com |
| Altera literature services | lit_req@altera.com *(1)* | lit_req@altera.com *(1)* |
| Non-technical customer service | (800) 767-3753 | (408) 544-7000<br>(7:30 a.m. to 5:30 p.m. Pacific Time) |
| FTP site | ftp.altera.com | ftp.altera.com |

***Note to table:***

(1) You can also contact your local Altera sales office or sales representative.

# Section I. Clock Management

This section provides information on the different types of phase-lock loops (PLLs). The feature rich enhanced PLLs assist designers in managing clocks internally and also have the ability to drive off chip to control system-level clock networks. The fast PLLs offer general-purpose clock management with multiplication and phase shifting as well as high-speed outputs to manage the high-speed differential I/O interfaces. This chapter contains detailed information on the features, the interconnections to the core and off chip, and the specifications for both types of PLLs.

This section contains the following:

- Chapter 1, Using General-Purpose PLLs in Stratix & Stratix GX Devices

## Revision History

The table below shows the revision history for Chapter 1.

| Chapter(s) | Date / Version | Changes Made |
|---|---|---|
| 1 | April 2003<br>v1.0 | Added document to the Stratix Device Handbook. |

# 1. Using General-Purpose PLLs in Stratix & Stratix GX Devices

S52001-1.0

Chapter 1, Using General-Purpose PLLs in Stratix & Stratix GX Devices replaces *AN 200: Using PLLs in Stratix Devices*.

## Introduction

Stratix™ and Stratix GX devices have highly versatile phase-locked loops (PLLs) that provide robust clock management and synthesis for on-chip clock management, external system clock management, and high-speed I/O interfaces. There are two types of PLLs in each Stratix and Stratix GX device: enhanced PLLs and fast PLLs. Each device has up to four enhanced PLLs, which are feature-rich, general-purpose PLLs supporting advanced capabilities such as external feedback, clock switchover, phase and delay control, PLL reconfiguration, spread spectrum clocking, and programmable bandwidth. There are also up to eight fast PLLs per device, which offer general-purpose clock management with multiplication and phase shifting as well as high-speed outputs to manage the high-speed differential I/O interfaces.

The Altera® Quartus® II software enables the PLLs and their features without requiring any external devices.

Tables 1–1 and 1–2 show the PLLs available for each Stratix and Stratix GX device, respectively, and their type.

***Table 1–1. Stratix Device PLL Availability***

| Device | Fast PLLs |  |  |  |  |  |  |  | Enhanced PLLs |  |  |  |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
|  | 1 | 2 | 3 | 4 | 7 | 8 | 9 | 10 | 5 *(1)* | 6 *(1)* | 11 *(2)* | 12 *(2)* |
| EP1S10 | ✓ | ✓ | ✓ | ✓ |  |  |  |  | ✓ | ✓ |  |  |
| EP1S20 | ✓ | ✓ | ✓ | ✓ |  |  |  |  | ✓ | ✓ |  |  |
| EP1S25 | ✓ | ✓ | ✓ | ✓ |  |  |  |  | ✓ | ✓ |  |  |
| EP1S30 | ✓ | ✓ | ✓ | ✓ | ✓ *(3)* | ✓ *(3)* | ✓ *(3)* | ✓ *(3)* | ✓ | ✓ |  |  |
| EP1S40 | ✓ | ✓ | ✓ | ✓ | ✓ *(3)* | ✓ *(3)* | ✓ *(3)* | ✓ *(3)* | ✓ | ✓ | ✓ | ✓ |
| EP1S60 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| EP1S80 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

*Notes to Table 1–1:*

(1) PLLs 5 and 6 each have eight single-ended outputs or four differential outputs.

(2) PLLs 11 and 12 each have one single-ended output.

(3) EP1S30 and EP1S40 devices do not support these PLLs in the 780-pin FineLine BGA® package.

***Table 1–2. Stratix GX Device PLL Availability***

| Device | Fast PLLs |  |  |  | Enhanced PLLs |  |  |  |
|---|---|---|---|---|---|---|---|---|
|  | 1 | 2 | 7 | 8 | 5 | 6 | 11 | 12 |
| EP1S10C | ✓ | ✓ |  |  | ✓ | ✓ |  |  |
| EP1S10D | ✓ | ✓ |  |  | ✓ | ✓ |  |  |
| EP1S25C | ✓ | ✓ |  |  | ✓ | ✓ |  |  |
| EP1S25D | ✓ | ✓ |  |  | ✓ | ✓ |  |  |
| EP1S25F | ✓ | ✓ |  |  | ✓ | ✓ |  |  |
| EP1S40D | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| EP1S40G | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

Table 1–3 shows the enhanced PLL and fast PLL features in Stratix and Stratix GX devices.

*Table 1–3. Stratix & Stratix GX PLL Features*

| Feature | Enhanced PLL | Fast PLL |
|---|---|---|
| Clock multiplication and division | $m/(n \times$ post-scale counter$)$ *(1)* | $m/($post-scale counter$)$ *(2)* |
| Phase shift | Down to 156.25-ps increments *(3)*, *(4)* | Down to 125-ps increments *(3)*, *(4)* |
| Delay shift | 250-ps increments for ±3 ns | |
| Clock switchover | ✓ | |
| PLL reconfiguration | ✓ | |
| Programmable bandwidth | ✓ | |
| Spread spectrum clocking | ✓ | |
| Programmable duty cycle | ✓ | ✓ |
| Number of internal clock outputs | 6 | 3 *(5)* |
| Number of external clock outputs | Four differential/eight singled-ended or one single-ended *(6)* | *(7)* |
| Number of feedback clock inputs | 2 *(8)* | |

***Notes to Table 1–3:***

(1) For enhanced PLLs, $m$, $n$, and post-scale counters range from 1 to 512.

(2) For fast PLLs, $m$, $n$, and post-scale counters range from 1 to 32.

(3) The smallest phase shift is determined by the voltage controlled oscillator (VCO) period divided by 8.

(4) For degree increments, Stratix and Stratix GX devices can shift all output frequencies in increments of at least 45°. Smaller degree increments are possible depending on the frequency and divide parameters.

(5) PLLs 7, 8, 9, and 10 have two output ports per PLL. PLLs 1, 2, 3, and 4 have three output ports per PLL. On Stratix GX devices, PLLs 3, 4, 9, and 10 are not available for general-purpose use.

(6) Every Stratix and Stratix GX device has two enhanced PLLs (PLLs 5 and 6) with either eight single-ended outputs or four differential outputs each. Two additional enhanced PLLs (PLLs 11 and 12) in EP1S80, EP1S60, EP1S40, and EP1SGX40 devices each have one single-ended output.

(7) Fast PLLs can drive to any I/O pin as an external clock. For high-speed differential I/O pins, the device uses a data channel to generate `txclkout`.

(8) Every Stratix and Stratix GX device has two enhanced PLLs with one single-ended or differential external feedback input per PLL.

Figure 1–1 shows a top-level diagram of the Stratix device and PLL floorplan. Figure 1–2 shows a top-level diagram of the Stratix GX device and PLL floorplan. See "Clocking" on page 1–48 for more detail on PLL connections to global and regional clocks.

*Figure 1–1. Stratix PLL Locations*

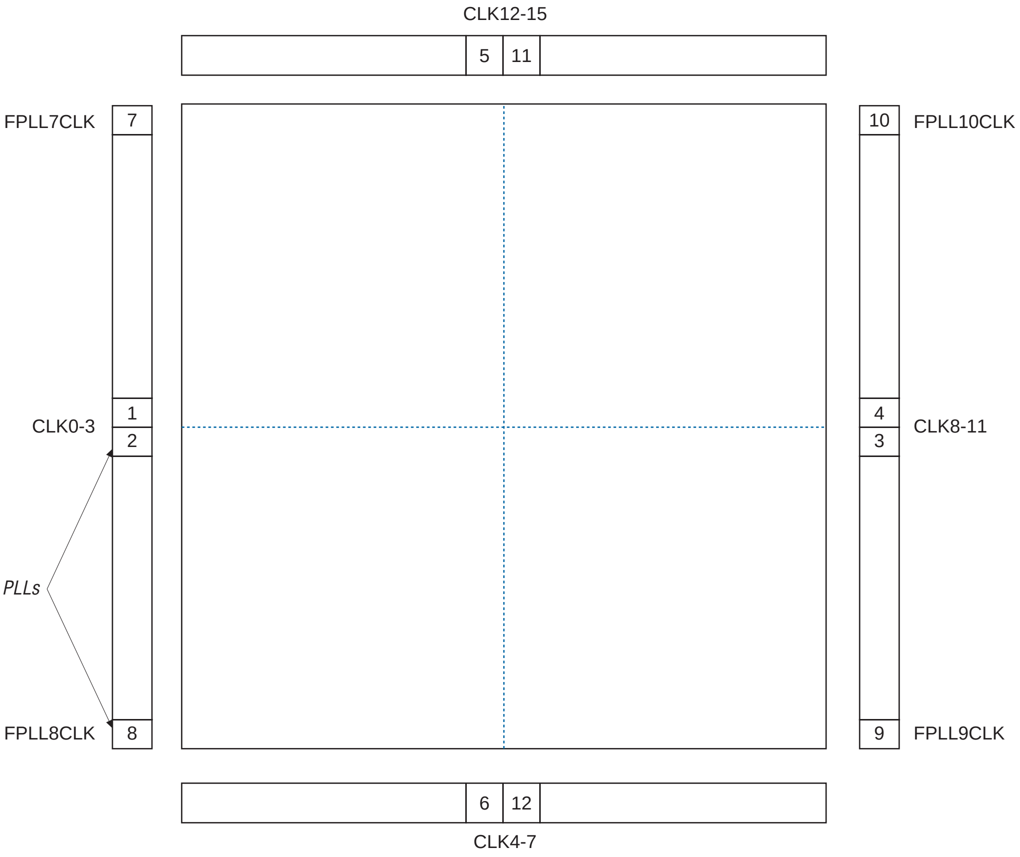
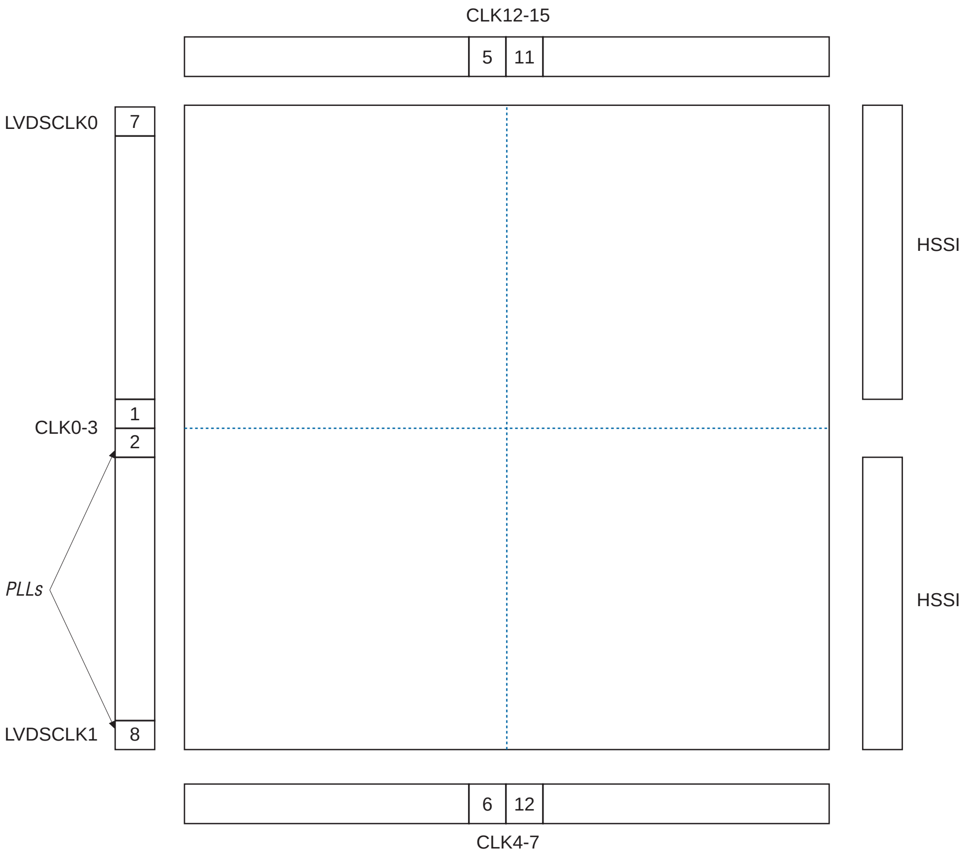


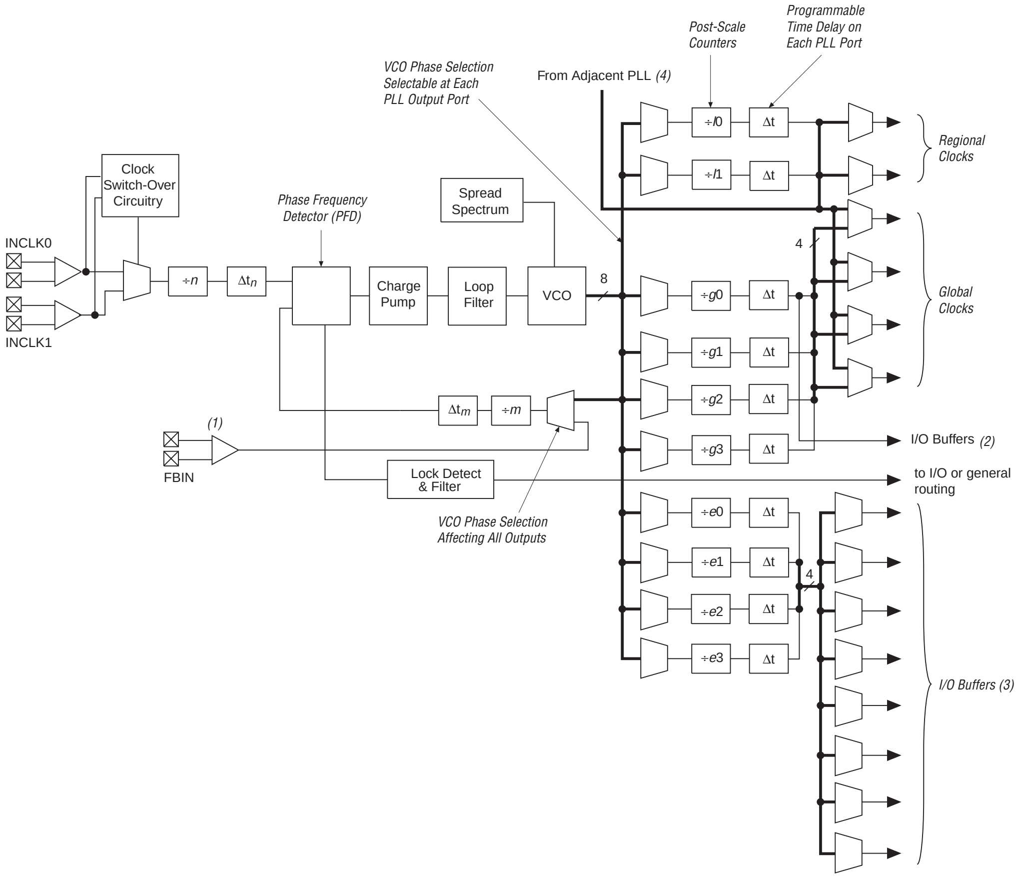
*Figure 1–2. Stratix GX PLL Locations*



## Enhanced PLLs

Stratix and Stratix GX devices contain up to four enhanced PLLs with advanced clock management features. Figure 1–3 shows a diagram of the enhanced PLL.

*Figure 1–3. Stratix & Stratix GX Enhanced PLL*



*Notes to Figure 1–3:*

(1) External feedback is available in PLLs 5 and 6.

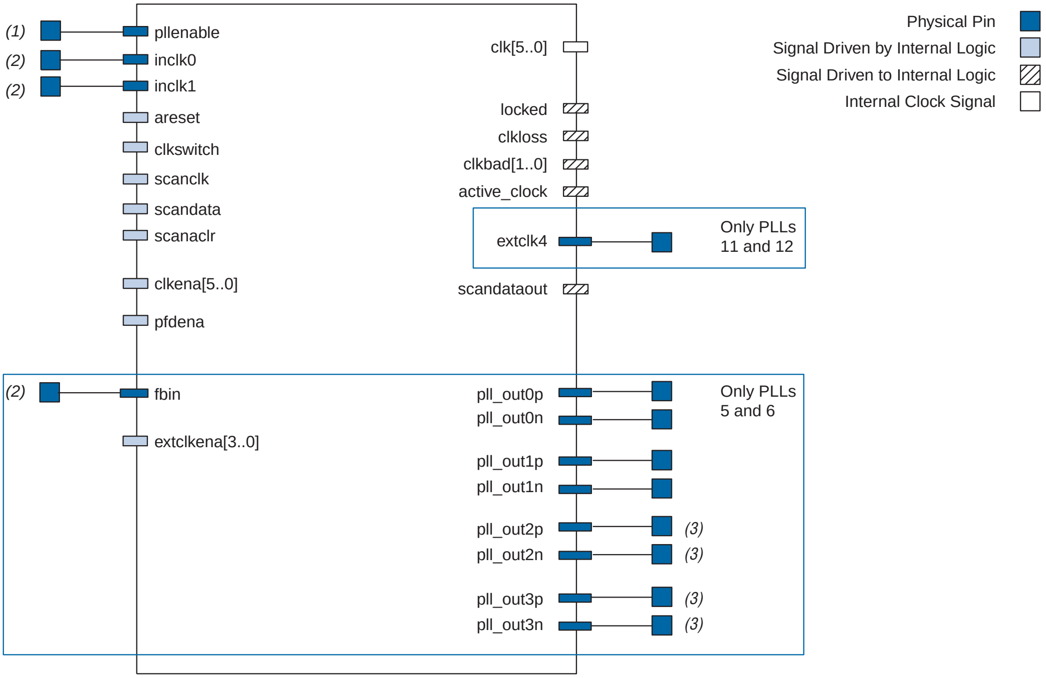
(2) This single-ended external output is available from the *g*0 counter for PLLs 11 and 12.

(3) These four counters and external outputs are available in PLLs 5 and 6.

(4) This connection is only available on EP1SGX40 Stratix GX devices and EP1S40 and larger Stratix devices. For example, PLLs 5 and 11 are adjacent and PLLs 6 and 12 are adjacent.

Figure 1–4 shows all the possible ports of the enhanced PLLs.

*Figure 1–4. Enhanced PLL Signals*



*Notes to Figure 1–4:*

(1) This input pin is shared by all enhanced and fast PLLs.

(2) These are either single-ended or differential pins.

(3) EP1S10, EP1S20, and EP1S25 devices in 672-pin ball grid array (BGA) and 484- and 672-pin FineLine BGA packages only have two pairs of external clocks (i.e., `pll_out0p`, `pll_out0n`, `pll_out1p`, and `pll_out1n`).

Table 1–4 and 1–5 describe all the enhanced PLL ports.

*Table 1–4. Enhanced PLL Input Signals*

| Port | Description | Source | Destination |
|---|---|---|---|
| `inclk[1..0]` | Primary and secondary reference clock inputs to PLL | Pin | ÷*n* counter |
| `fbin` | External feedback input to the PLL (PLLs 5 and 6 only) | Pin | Phase frequency detector (PFD) |
| `pllena` | Enable pin for enabling or disabling all or a set of PLLs—active high | Pin | General PLL control signal |
| `clkswitch` | Switch-over signal used to initiate external clock switch-over control—active high | Logic array | PLL switch-over circuit |
| `areset` | Signal used to reset the PLL which will re-synchronize all the counter outputs—active high | Logic array | General PLL control signal |
| `clkena[5..0]` | Enable clock driving regional or global clock—active high | Logic array | Clock output |
| `extclkena[3..0]` | Enable clock driving external clock (PLLs 5 and 6 only)—active high | Logic array | Clock output |
| `pfdena` | Enables the outputs from the phase frequency detector—active high | Logic array | PFD |
| `scanclk` | Serial clock signal for the real-time PLL control feature | Logic array | Reconfiguration circuit |
| `scandata` | Serial input data stream for the real-time PLL control feature | Logic array | Reconfiguration circuit |
| `scanaclr` | Serial shift register reset clearing all registers in the serial shift chain—active high | Logic array | Reconfiguration circuit |

*Table 1–5. Enhanced PLL Output Signals*

| Port | Description | Source | Destination |
|---|---|---|---|
| `clk[5..0]` | PLL outputs driving regional or global clock | PLL counter | Internal Clock |
| `pll_out[3..0]p/n` | `pll_out[3..0]` are PLL outputs driving the four differential or eight single-ended external clock output pins for PLLs 5 or 6. p or n are the positive (p) and negative (n) pins for differential pins. | PLL counter | Pin(s) |
| `extclk4` | PLL output driving external clock output pin from PLLs 11 and 12 | PLL *g*0 counter | Pin |
| `clkloss` | Signal indicating the switch-over circuit detected a switch-over condition | PLL switch-over circuit | Logic array |
| `clkbad[1..0]` | Signals indicating which reference clock is no longer toggling. `clkbad1` indicates `inclk1` status, `clkbad0` indicates `inclk0` status | PLL switch-over circuit | Logic array |
| `locked` | Lock or gated lock output from lock detect circuit—active high | PLL lock detect | Logic array |
| `activeclock` | Signal to indicate which clock (`1` = `inclk0` or `0` = `inclk1`) is driving the PLL. | PLL clock multiplexer | Logic array |
| `scandataout` | Output of the last shift register in the scan chain | PLL scan chain | Logic array |

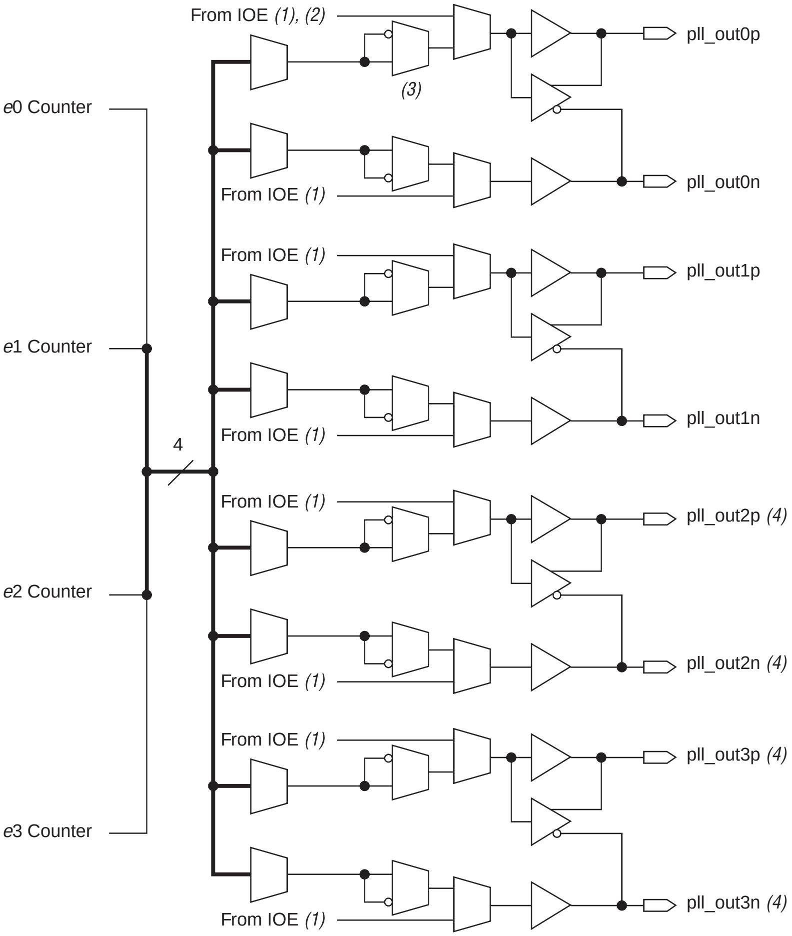
## Clock Multiplication & Division

Each Stratix and Stratix GX device enhanced PLL provides clock synthesis for PLL output ports using $m/(n \times \text{post-scale counter})$ scaling factors. The input clock is divided by a pre-scale counter, $n$, and is then multiplied by the $m$ feedback factor. The control loop drives the VCO to match $f_{IN} \times (m/n)$. Each output port has a unique post-scale counter that divides down the high-frequency VCO. For multiple PLL outputs with different frequencies, the VCO is set to the least common multiple of the output frequencies that meets its frequency specifications. Then, the post-scale counters scale down the output frequency for each output port. For example, if output frequencies required from one PLL are 33 and 66 MHz, then the Quartus II software sets the VCO to 330 MHz (the least common multiple of 33 and 66 MHz within the VCO range). There is one pre-scale counter, $n$, and one multiply counter, $m$, per PLL, with a range of 1 to 512 on each. There are two post-scale counters ($l$) for regional clock output ports, four counters ($g$) for global clock output ports, and up to four counters ($e$) for external clock outputs, all ranging from 1 to 512. The Quartus II software automatically chooses the appropriate scaling factors according to the input frequency, multiplication, and division values entered into the `altpll` MegaWizard Plug-In Manager.

## External Clock Outputs

Enhanced PLLs 5 and 6 each support up to eight single-ended clock outputs (or four differential pairs). See Figure 1–5.

*Figure 1–5. External Clock Outputs for PLLs 5 & 6*



*Notes to Figure 1–5:*

1. (1) LE: logic element.
2. (2) The design can use each external clock output pin as a general-purpose output pin from the logic array. These pins are multiplexed with IOE outputs.
3. (3) Two single-ended outputs are possible per output counter—either two outputs of the same frequency and phase or one shifted 180°.
4. (4) EP1S10, EP1S20, and EP1S25 devices in 672-pin ball grid array (BGA) and 484- and 672-pin FineLine BGA packages only have two pairs of external clocks (i.e., `pll_out0p`, `pll_out0n`, `pll_out1p`, and `pll_out1n`).

Any of the four external output counters can drive the single-ended or differential clock outputs for PLLs 5 and 6. This means one counter or frequency can drive all output pins available from PLL 5 or PLL 6. Each pair of output pins (four pins total) has dedicated `VCC` and `GND` pins to reduce the output clock's overall jitter by providing improved isolation from switching I/O pins.

For PLLs 5 and 6, each pin of a single-ended output pair can either be in phase or 180° out of phase. The Quartus II software will transfer the NOT gate in the design into the IOE to implement 180° phase with respect to the other pin in the pair. The clock output pin pairs support the same I/O standards as standard output pins (in the top and bottom banks) as well as LVDS, LVPECL, PCML, HyperTransport™ technology, differential HSTL, and differential SSTL. Table 1–6 shows which I/O standards the enhanced PLL clock pins support. When in single-ended or differential mode, one power pin supports two differential or four single-ended . Both outputs use the same standards in single-ended mode to maintain performance. Designers can also use the external clock output pins as user output pins if external enhanced PLL clocking is not needed.

The enhanced PLL can also drive out to any regular I/O pin through the global or regional clock network. The jitter on the output clock is not guaranteed for this case.

***Table 1–6. I/O Standards Supported for Enhanced PLL Pins (Part 1 of 2)***

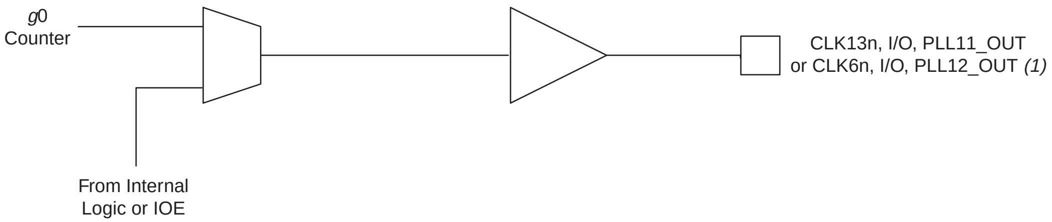
| I/O Standard | Input | | | Output |
|---|---|---|---|---|
| | INCLK | FBIN | PLLENABLE | EXTCLK |
| LVTTL | ✓ | ✓ | ✓ | ✓ |
| LVCMOS | ✓ | ✓ | ✓ | ✓ |
| 2.5 V | ✓ | ✓ | | ✓ |
| 1.8 V | ✓ | ✓ | | ✓ |
| 1.5 V | ✓ | ✓ | | ✓ |
| 3.3-V PCI | ✓ | ✓ | | ✓ |
| 3.3-V PCI-X | ✓ | ✓ | | ✓ |
| LVPECL | ✓ | ✓ | | ✓ |
| PCML | ✓ | ✓ | | ✓ |
| LVDS | ✓ | ✓ | | ✓ |
| HyperTransport technology | ✓ | ✓ | | ✓ |
| Differential HSTL | ✓ | | | ✓ |

*Table 1–6. I/O Standards Supported for Enhanced PLL Pins (Part 2 of 2)*

| I/O Standard | Input | | | Output |
|---|---|---|---|---|
| | INCLK | FBIN | PLLENABLE | EXTCLK |
| Differential SSTL | | | | ✓ |
| 3.3-V GTL | ✓ | ✓ | | ✓ |
| 3.3-V GTL+ | ✓ | ✓ | | ✓ |
| 1.5-V HSTL class I | ✓ | ✓ | | ✓ |
| 1.5-V HSTL class II | ✓ | ✓ | | ✓ |
| SSTL-18 class I | ✓ | ✓ | | ✓ |
| SSTL-18 class II | ✓ | ✓ | | ✓ |
| SSTL-2 class I | ✓ | ✓ | | ✓ |
| SSTL-2 class II | ✓ | ✓ | | ✓ |
| SSTL-3 class I | ✓ | ✓ | | ✓ |
| SSTL-3 class II | ✓ | ✓ | | ✓ |
| AGP (1× and 2×) | ✓ | ✓ | | ✓ |
| CTT | ✓ | ✓ | | ✓ |

Enhanced PLLs 11 and 12 support one single-ended output each (see Figure 1–6). These outputs do not have their own `VCC` and `GND` signals. Therefore, to minimize jitter, do not place switching I/O pins next to this output pin.

*Figure 1–6. External Clock Outputs for Enhanced PLLs 11 & 12*



*Note to Figure 1–6:*

(1) For PLL11, this pin is `CLK13n`; for PLL 12 this pin is `CLK6n`.

Stratix and Stratix GX devices can drive any enhanced PLL driven through the global clock or regional clock network to any general I/O pin as an external output clock. The jitter on the output clock is not guaranteed for these cases.

## Clock Feedback

The following three feedback modes in Stratix and Stratix GX device enhanced PLLs allow multiplication and/or phase and delay shifting:

- Zero delay buffer: The external clock output pin is phase-aligned with the clock input pin for zero delay.
- External feedback: The external feedback input pin, FBIN, is phase-aligned with the clock input, CLK, pin. Aligning these clocks allows the designer to remove clock delay and skew between devices. This mode is only possible for PLLs 5 and 6. PLLs 5 and 6 each support feedback for one of the dedicated external outputs, either one single-ended or one differential pair. In this mode, one e counter feeds back to the PLL FBIN input, becoming part of the feedback loop.
- Normal mode: If an internal clock is used in this mode, it is phase-aligned to the input clock pin. The external clock output pin will have a phase delay relative to the clock input pin if connected in this mode.

## Phase & Delay Shifting

Stratix and Stratix GX device enhanced PLLs provide advanced programmable phase and clock delay shifting. These parameters are set in the Quartus II software.

### *Phase Delay*

The Quartus II software automatically sets the phase taps and counter settings according to the phase shift entry. The designer enters a desired phase shift and the Quartus II software automatically sets the closest setting achievable. This type of phase shift is not reconfigurable during system operation. For phase shifting, enter a phase shift (in degrees or time units) for each PLL clock output port or for all outputs together in one shift. Designers can select phase-shifting values in time units with a resolution of 156.25 to 416.66 ps. This resolution is a function of frequency input and the multiplication and division factors (i.e., it is a function of the VCO period), with the finest step being equal to an eighth (×0.125) of the VCO period. Each clock output counter can choose a different phase of the VCO period from up to eight taps for individual fine step selection. Also, each clock output counter can use a unique initial count setting to achieve individual coarse shift selection in steps of one VCO period. The combination of coarse and fine shifts allows phase shifting for the entire input clock period.

The equation to determine the precision of the phase shifting in degrees is: 45° ÷ post-scale counter value. Therefore, the maximum step size is 45°, and smaller steps are possible depending on the multiplication and division ratio necessary on the output counter port.

This type of phase shift provides the highest precision since it is the least sensitive to process, supply, and temperature variation.

### Clock Delay

In addition to the phase shift feature, the ability to fine tune the Δt clock delay provides advanced time delay shift control on each of the four PLL outputs. There are time delays for each post-scale counter (*e*, *g*, or *l*) from the PLL, the *n* counter, and *m* counter. Each of these can shift in 250-ps increments for a range of 3.0 ns. The *m* delay shifts all outputs earlier in time, while *n* delay shifts all outputs later in time. Individual delays on post-scale counters (*e*, *g*, and *l*) provide positive delay for each output. Table 1–7 shows the combined delay for each output for normal or zero delay buffer mode where $\Delta t_e$, $\Delta t_g$, or $\Delta t_l$ is unique for each PLL output.

The $t_{OUTPUT}$ for a single output can range from –3 ns to +6 ns. The total delay shift difference between any two PLL outputs, however, must be less than ±3 ns. For example, shifts on two outputs of –1 and +2 ns is allowed, but not –1 and +2.5 ns because these shifts would result in a difference of 3.5 ns. If the design uses external feedback, the $\Delta t_e$ delay will remove delay from outputs, represented by a negative sign (see Table 1–7). This effect occurs because the $\Delta t_e$ delay is then part of the feedback loop.

**Table 1–7. Output Clock Delay for Enhanced PLLs**

| Normal or Zero Delay Buffer Mode | External Feedback Mode |
|---|---|
| $\Delta t_{eOUTPUT} = \Delta t_n - \Delta t_m + \Delta t_e$<br>$\Delta t_{gOUTPUT} = \Delta t_n - \Delta t_m + \Delta t_g$<br>$\Delta t_{lOUTPUT} = \Delta t_n - \Delta t_m + \Delta t_l$ | $\Delta t_{eOUTPUT} = \Delta t_n - \Delta t_m - \Delta t_e$ (1)<br>$\Delta t_{gOUTPUT} = \Delta t_n - \Delta t_m + \Delta t_g$<br>$\Delta t_{lOUTPUT} = \Delta t_n - \Delta t_m + \Delta t_l$ |

***Note to Table 1–7:***

(1) $\Delta t_e$ removes delay from outputs in external feedback mode.

The variation due to process, voltage, and temperature is about ±15% on the delay settings. PLL reconfiguration can control the clock delay shift elements, but not the VCO phase shift multiplexers, during system operation.

## Lock Detect

The lock output indicates that there is a stable clock output signal in phase with the reference clock. Without any additional circuitry, the lock signal may toggle as the PLL begins tracking the reference clock. A designer may need to gate the lock signal for use as a system control. Either a gated lock signal or an ungated lock signal from the locked port can drive the logic array or an output pin.

See the *Stratix FPGA Errata Sheet* for more information on implementing the gated lock signal in your design.

## Programmable Duty Cycle

The programmable duty cycle allows enhanced PLLs to generate clock outputs with a variable duty cycle. This feature is supported on each enhanced PLL post-scale counter (*g*0..*g*3, *l*0..*l*3, *e*0..*e*3). The duty cycle setting is achieved by a low and high time count setting for the post-scale counters. The Quartus II software uses the frequency input and the required multiply or divide rate to determine the duty cycle choices. The precision of the duty cycle is determined by the post-scale counter value chosen on an output. The precision is defined by 50% divided by the post-scale counter value. The closest value to 100% is not achievable for a given counter value. For example, if the *g*0 counter is 10, then steps of 5% are possible for duty cycle choices between 5 to 90%.

If the device uses external feedback, the designer must set the duty cycle for the counter driving off the device to 50%.

## General Advanced Clear & Enable Control

There are several control signals for clearing and enabling PLLs and their outputs. The designer can use these signals to control PLL resynchronization and gate PLL output clocks for low-power applications.

The `pllenable` pin is a dedicated pin that enables/disables PLLs. When the `pllenable` pin is low, the clock output ports are driven by `GND` and all the PLLs go out of lock. When the `pllenable` pin goes high again, the PLLs relock and resynchronize to the input clocks. The designer can choose which PLLs are controlled by the `pllenable` signal by connecting the `pllenable` input port of the `altpll` megafunction to the common `pllenable` input pin.

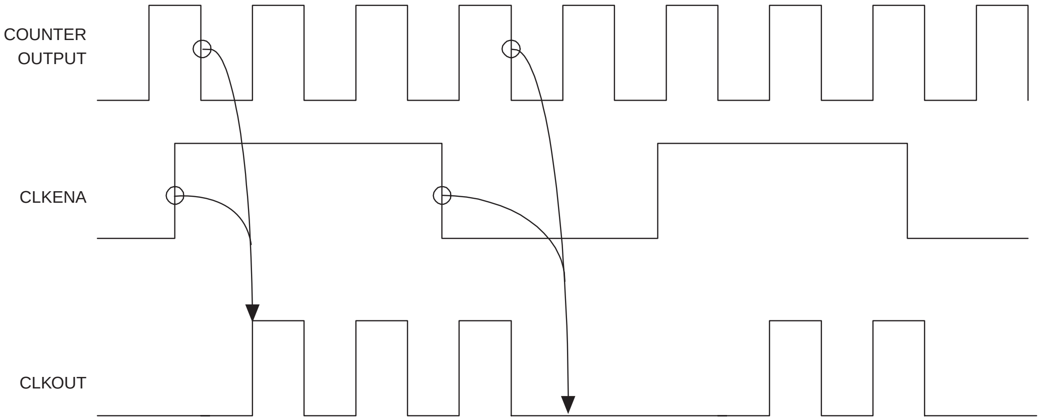
The `areset` signals are reset/resynchronization inputs for each PLL. The device input pins or logic elements (LEs) can drive these input signals. When driven high, the PLL counters will reset, clearing the PLL output and placing the PLL out of lock. The VCO will set back to its nominal setting (~700 MHz). When driven low again, the PLL will resynchronize to its input as it relocks. If the target VCO frequency is below this nominal frequency, then the output frequency will start at a higher value than desired as the PLL locks. If the system cannot tolerate this, the `clkena` signal can disable the output clocks until the PLL locks.

The `pfdena` signals control the phase frequency detector (PFD) output with a programmable gate. If the designer disables the PFD, the VCO will operate at its last set value of control voltage and frequency with some long-term drift to a lower frequency. The system will continue running when the PLL goes out of lock or the input clock is disabled. By maintaining the last locked frequency, the system has time to store its current settings before shutting down. Designers can either use their own control signal or `clkloss` or gated `locked` status signals to trigger `pdfena`.

The `clkena` signals control the enhanced PLL regional and global outputs. Each regional and global output port has its own `clkena` signal. The `clkena` signals synchronously disable or enable the clock at the PLL output port by gating the outputs of the *g* and *l* counters. The `clkena` signals are registered on the falling edge of the counter output clock to enable or disable the clock without glitches. Figure 1–7 shows the waveform example for a PLL clock port enable. The PLL can remain locked independent of the `clkena` signals since the loop-related counters are not affected. This feature is useful for applications that require a low power or sleep mode. Upon re-enabling, the PLL does not need a resynchronization or relock period. The `clkena` signal can also disable clock outputs if the system is not tolerant to frequency overshoot during resynchronization.

The `extclkena` signals work in the same way as the `clkena` signals, but they control the external clock output counters (*e*0, *e*1, *e*2, and *e*3). Upon re-enabling, the PLL does not need a resynchronization or relock period unless the PLL is using external feedback mode. In order to lock in external feedback mode, the external output must drive the board trace back to the `FBIN` pin.

*Figure 1–7. extclkena Signals*



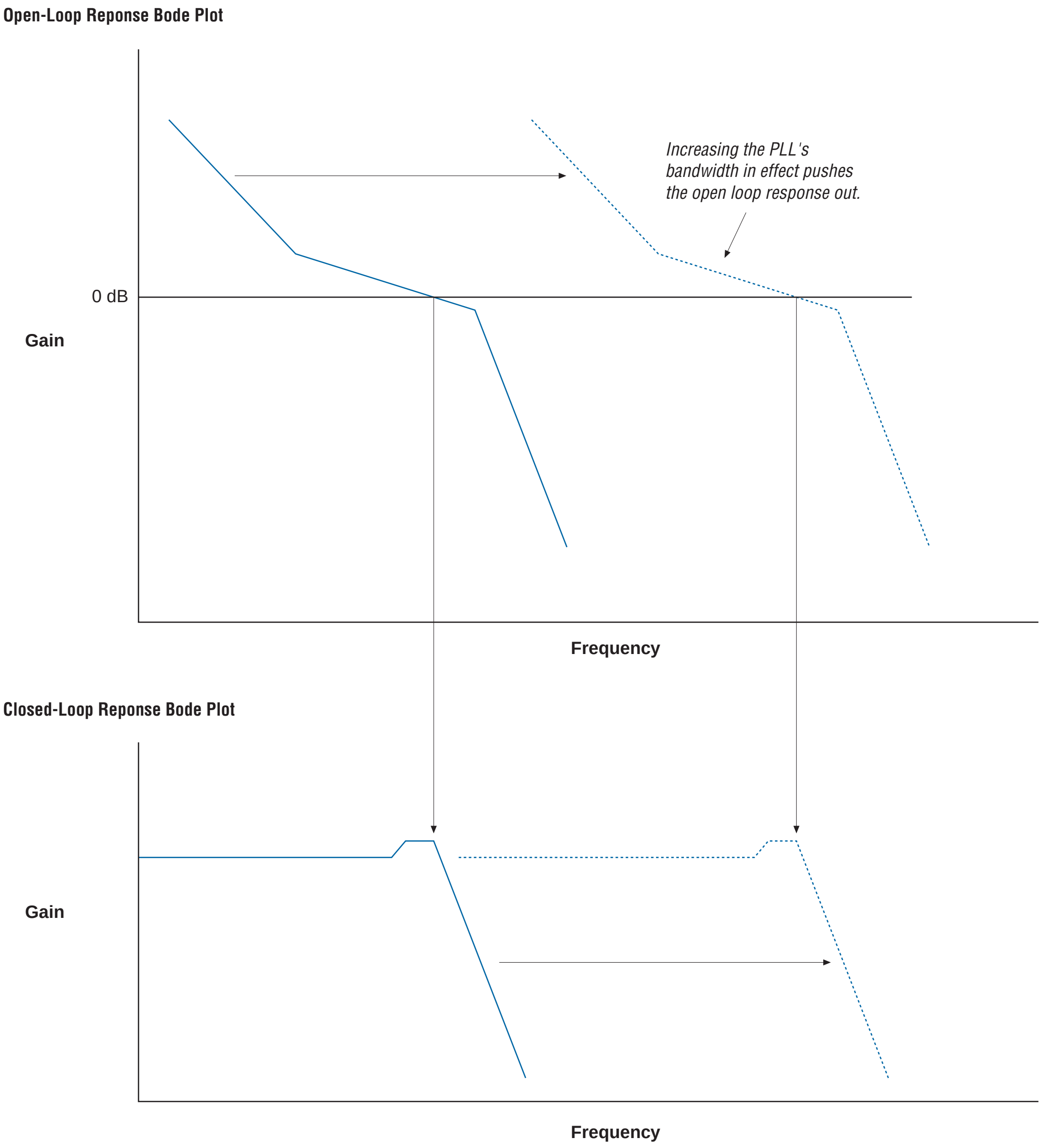
## Programmable Bandwidth

Enhanced PLLs provide advanced control of the PLL bandwidth using the programmable characteristics of the PLL loop, including loop filter and charge pump.

### *Background*

The PLL bandwidth is the measure of the PLLs ability to track the input clock and jitter. It is determined by the –3-dB frequency of the closed-loop gain in the PLL or approximately the unity gain point for open loop PLL response. As Figure 1–8 shows, these points correspond to approximately the same frequency.

*Figure 1–8. Open- & Closed-Loop Response Bode Plots*



A high-bandwidth PLL provides a fast lock time and tracks jitter on the reference clock source, passing it through to the PLL output. A low-bandwidth PLL filters out reference clock jitter, but increases lock time. Stratix device enhanced PLLs allow the designer to control the bandwidth over a finite range to customize the PLL characteristics for a particular application. Applications that require clock switch-over (such as TDMA, frequency hopping wireless, and redundant clocking) can benefit from the programmable bandwidth feature of the Stratix and Stratix GX PLLs.

The bandwidth and stability of such a system is determined by a number of factors including the charge pump current, the loop filter resistor value, the high-frequency capacitor value (in the loop filter), and the *m*-counter value. The designer can use the Quartus II software to control these factors and to set the bandwidth to the desired value within a given range.

The designer can set the bandwidth to the appropriate value to balance the need for jitter filtering and lock time. Figures 1–9 and 1–10 show the output of a low- and high-bandwidth PLL, respectively, as it locks onto the input clock.

***Figure 1–9. Low-Bandwidth PLL Lock Time***

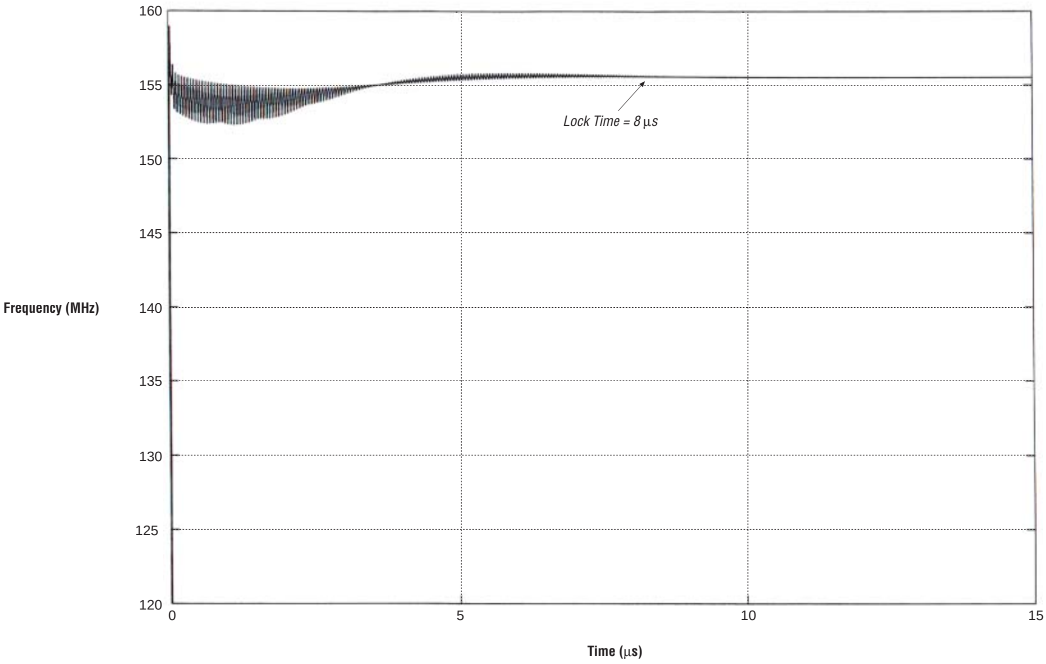
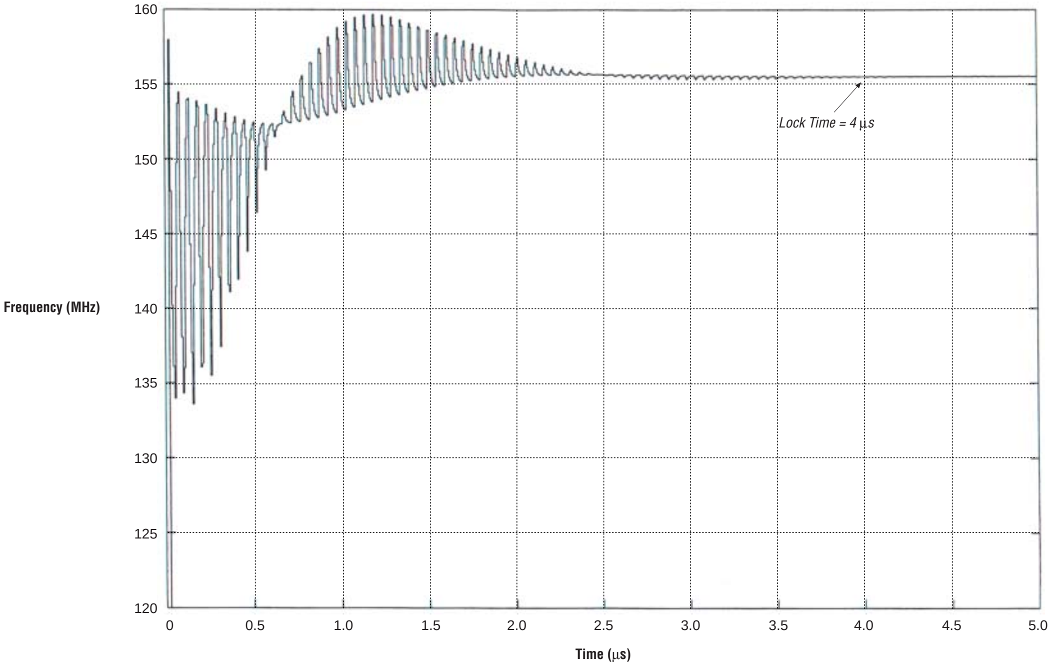


*Figure 1–10. High-Bandwidth PLL Lock Time*



A high-bandwidth PLL may benefit a system with two cascaded PLLs. If the first PLL uses spread spectrum (as user-induced jitter), the second PLL needs a high bandwidth so it can track the jitter that is feeding it. A low-bandwidth PLL may, in this case, lose lock due to the spread spectrum-induced jitter on the input clock.

A low-bandwidth PLL may benefit a system using clock switchover. When the clock switchover happens, the PLL input temporarily stops. A low-bandwidth PLL would react more slowly to changes to its input clock and take longer to drift to a lower frequency (caused by the input stopping) than a high-bandwidth PLL. Figures 1–11 and 1–12 demonstrate this property. The two plots show the effects of clock switchover with a low- or high-bandwidth PLL. When the clock switchover happens, the output of the low-bandwidth PLL (see Figure 1–11) drifts to lower frequency much slower than the high-bandwidth PLL output (see Figures 1–12).

*Figure 1–11. Effect of Low Bandwidth on Clock Switchover*

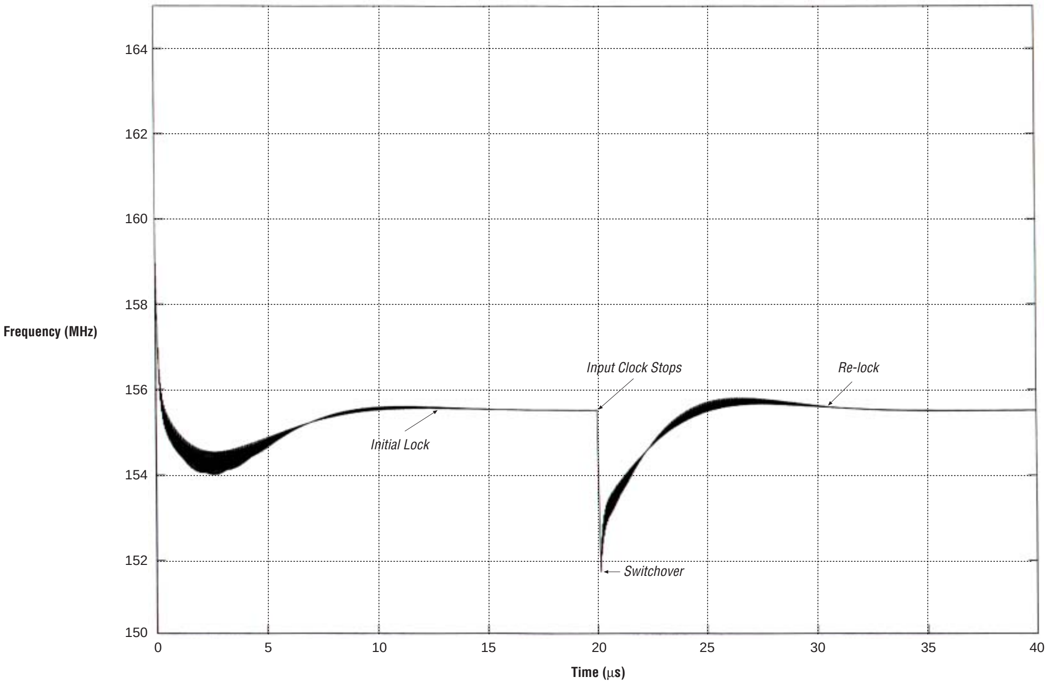
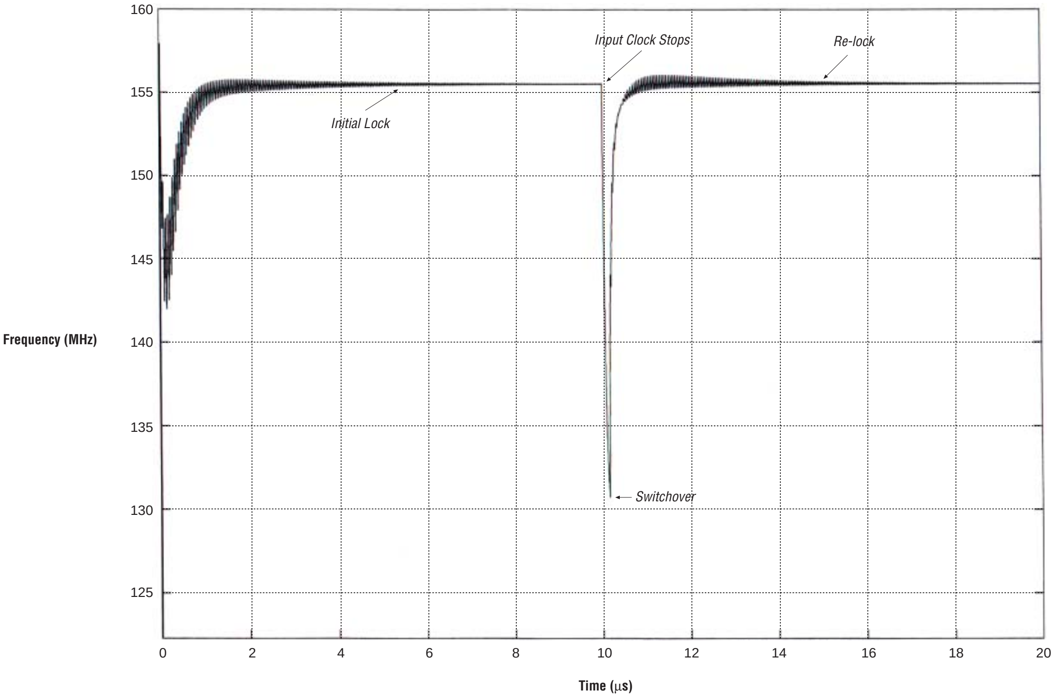


*Figure 1–12. Effect of High Bandwidth on Clock Switchover*



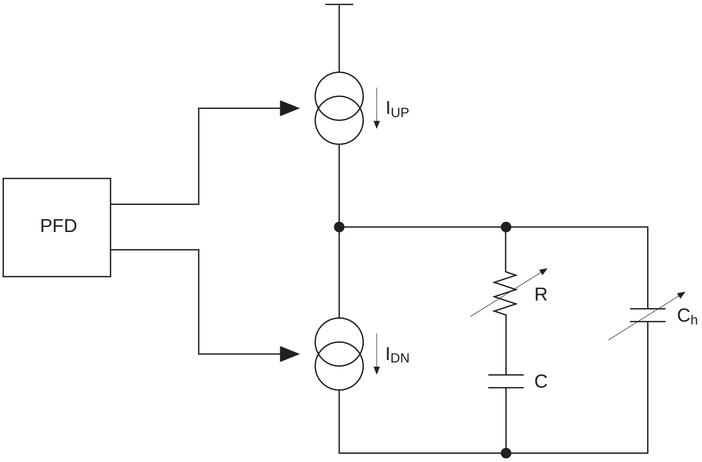
### *Implementation*

Traditionally, external components such as the VCO or loop filter control a PLL's bandwidth. Most loop filters are made up of passive components, such as resistors and capacitors, which take up unnecessary board space and increase cost. With Stratix and Stratix GX device enhanced PLLs, all the components are contained within the device to increase performance and decrease cost.

Stratix and Stratix GX device enhanced PLLs implement programmable bandwidth by giving the designer control of the charge pump current and loop filter resistor (R) and high-frequency capacitor ($C_h$) values (see Table 1–8). The Stratix and Stratix GX device enhanced PLL bandwidth ranges from approximately 200 kHz to 1.5 MHz.

The charge pump current directly affects the PLL bandwidth. The higher the charge pump current, the higher the PLL bandwidth. The designer can choose from a fixed set of values for the charge pump current. Figure 1–13 shows the loop filter and the components that designers can set via the Quartus II software.

***Figure 1–13. Loop Filter Programmable Components***



## *Software Support*

The Quartus II software provides two levels of programmable bandwidth control. The first level allows the designer to enter a value for the desired bandwidth directly into the Quartus II software using the MegaWizard™ Plug-In Manager. Alternatively, designers can set the `bandwidth` parameter in the `altpll` function to the desired bandwidth. The Quartus II software then chooses each individual bandwidth parameter to achieve the desired setting. If designs cannot achieve the desired bandwidth setting, the Quartus II software will select the closest achievable value.

An advanced level of control is also possible for precise control of the loop filter parameters. This level allows the designer to specifically select the charge pump current, loop filter resistor value, and loop filter (high frequency) capacitor value. These parameters are: charge_pump_current, loop_filter_r, and loop_filter_c. Each parameter supports the specific range of values listed in Table 1–8.

*Table 1–8. Advanced Loop Filter Parameters*

| Parameter | Values |
|---|---|
| Resistor values (kΩ) | 1, 2, 3, 4, 7, 8, 9, 10 |
| High-frequency capacitance values (pF) | 5, 10, 15, 20 |
| Charge pump current settings (µA) | 4, 10, 15, 20, 24, 30, 35, 40, 45, 50, 55, 60, 65, 70, 75, 80, 85, 90, 100, 112, 135, 148, 164, 212 |

For more information on PLL software support in the Quartus II software, see the *altpll Megafunction User Guide*.

Contact Altera Applications for more information on how the PLL parameters affect bandwidth.

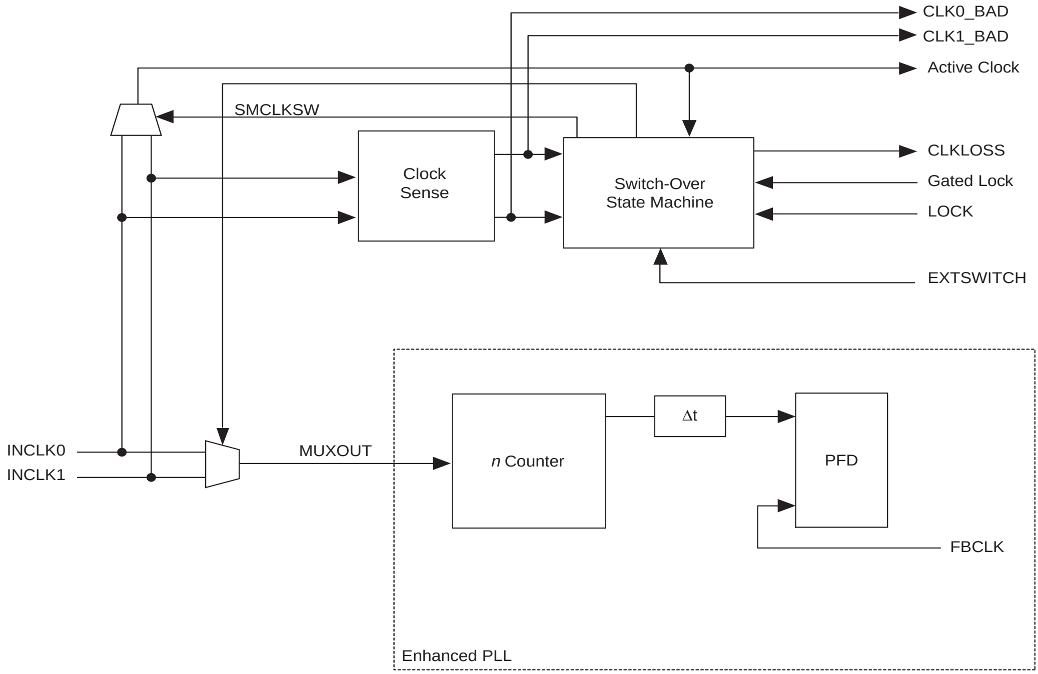
## Clock Switchover

The clock switchover feature allows the PLL to switch between two reference input clocks. Designers can use this feature for clock redundancy or for a dual clock domain application such as in a system where the system can switch the redundant clock on if the primary clock stops running for some reason. The design can perform clock switchover automatically, when the clock is no longer toggling, or based on a user control signal.

### *Description*

Stratix and Stratix GX device PLLs support a fully configurable clock switch-over capability. Figure 1–14 shows the block diagram of the switch-over circuit built into the enhanced PLL. The major component of this circuitry is the clock inputs sense block that automatically switches from primary to secondary clock for PLL reference when the primary clock signal is not present. The design can send out the `clk0_bad` and `clk1_bad` clock sense block outputs and the `clk_loss` signal to LEs to implement a custom switch-over circuit.

*Figure 1–14. Clock Switch-Over Circuit Block Diagram*



There are at least three possible ways use of the clock switch-over feature.

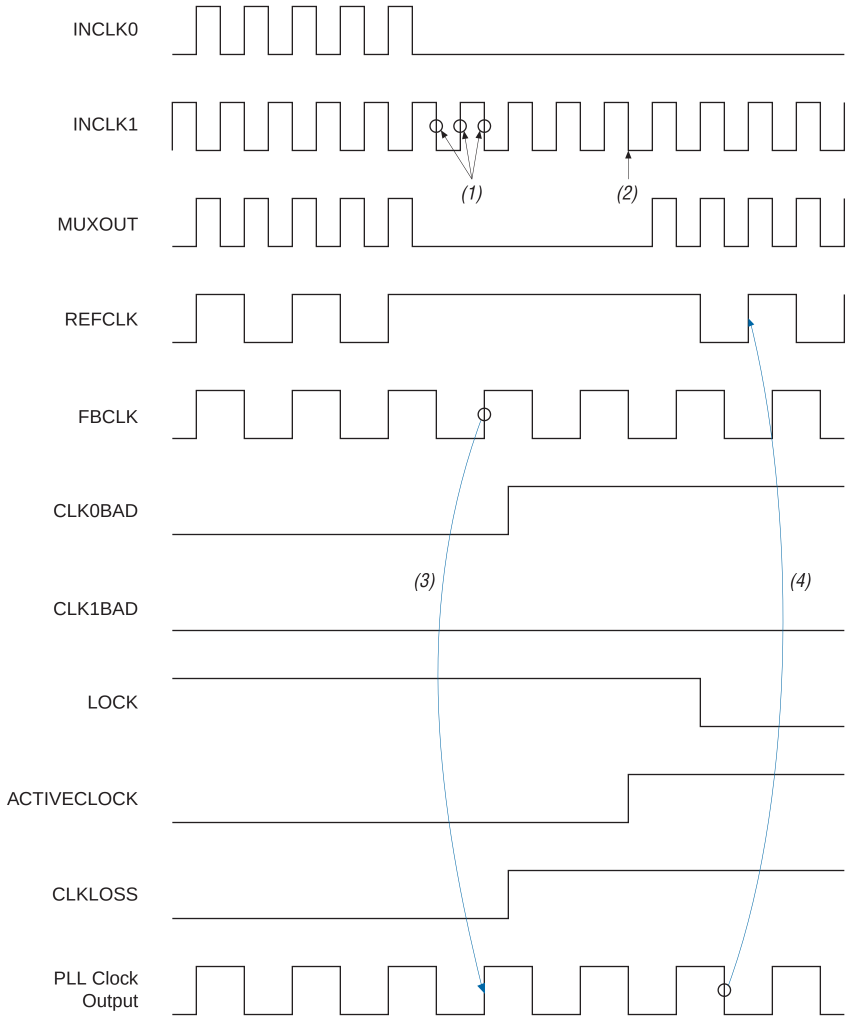
- Designers can use the switch-over circuitry for switching from a primary to secondary input of the same frequency. For example, in applications that require a redundant clock with the same frequency as the primary clock, the switchover state machine generates a signal that controls the multiplexer select input on the bottom of Figure 1–14. In this case, the secondary clock becomes the reference clock for the PLL. This automatic switch only words for the primary to secondary direction.

- Designers can use the `extswitch` input for user- or system-controlled switch conditions. This is possible for same-frequency switchover or to switch between inputs of different frequencies. For example, if `extclk0` is 66 MHz and `extclk1` is 100 MHz, the designer must control the switchover because the automatic clock-sense circuitry cannot monitor primary and secondary clock frequencies with a frequency difference of more than ±20%. This feature is useful when clock sources can originate from multiple cards on the backplane, requiring a system-controlled switchover between frequencies of operation. Also, designers should choose the secondary clock frequency such that the VCO operates within the recommended range of 300 to 800 MHz. Designers can set the *m* and *n* counters accordingly to keep the VCO operating frequency in the recommended range.
- If the PLL loses lock for some reason, designers can set the gated lock to control switchover. The gated lock signal goes low to force the switch-over state machine to switch to the secondary clock. If an external PLL is driving the Stratix or Stratix GX device PLL, excessive jitter on the clock input could cause the PLL to lose lock. Since the switch-over circuit still senses clock edges, it might not sense a switch condition. In this case, the designer can control switchover using the gated version of the locked signal based on the loss of the primary clock.

### Automatic Switchover

Figure 1–15 shows an example of a waveform illustrating the switchover feature when using automatic clkloss detection. Here, the `INCLK0` signal gets stuck low. After the `INCLK1` signal gets stuck at low for approximately two clock cycles, the clock sense circuitry drives the `clk0_bad` signal high. Also, since the reference clock signal is not toggling, the `clk_loss` signal goes low indicating a switch condition. Then, the switchover state machine controls the multiplexer through the `CLKSW` signal to switch to the secondary clock.

*Figure 1–15. Automatic Switchover Upon clkloss Detection*

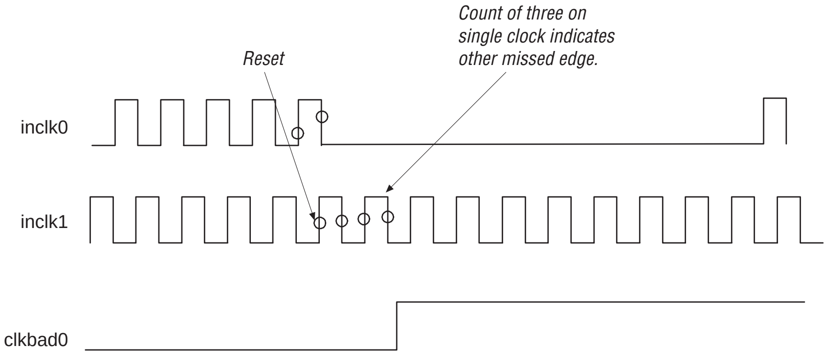


*Notes to Figure 1–15:*

(1) The number of clock edges before allowing switchover is determined by the counter setting.
(2) Switchover is enabled on the falling edge of `INCLK1`.
(3) The rising edge of `FBCLK` causes the VCO frequency to decrease.
(4) The rising edge of `REFCLK` starts the PLL lock process again, and the VCO frequency will increase.

The switchover state machine has two counters that count the edges of the primary and the secondary clocks. `counter0` counts the number of `inclk0` edges and `counter1` counts the number of `inclk1` edges. The counters get reset to zero when the count values reach 1,1; 1,2; 2,1; or 2,2 for `nclock0` and `nclock1`, respectively. For example, if `counter0` counts two edges, its count is set to two and if `counter1` counts two edges before the `counter0` sees another edge, they are both reset to 0. If for some reason, one of the counters counts to 3, it means the other clock missed an edge. `clkbad0` or `clkbad1` goes high, and the switch-over circuitry signals a switch condition. See Figure 1–16

***Figure 1–16. Clock-Edge Detection for Switchover***



## *Manual Switchover*

Figure 1–17 shows an example of a waveform illustrating the switch-over feature when controlled by `extswitch`. In this case, both clock sources are functional and `INCLK0` is selected as the primary clock. `EXTSWITCH` goes high, which starts the switch-over sequence. On the falling edge of `INCLK0`, the reference clock to the *n* counter, `MUXOUT`, is gated off to prevent any clock glitching. On the falling edge of `INCLK1`, the reference clock multiplexer switches from `INCLK0` to `INCLK1` as the PLL reference. This is also the point the `CLKSW` signal changes to indicate which clock is selected as primary and which is secondary. The `CLKLOSS` signal mirrors the `EXTSWITCH` signal in this mode. Since both clocks are still functional during the manual switch, neither `CLK_BAD` signal goes high. Since the switch-over circuit is edge-sensitive, the falling edge of the `EXTSWITCH` signal does not cause the circuit to switch back from `INCLK1` to `INCLK0`. When the `EXTSWITCH` signal goes high again, the process repeats. `EXTSWITCH` and automatic switch will only work if the clock being switched to is available.

*Figure 1–17. Clock Switch-Over Using the EXTSWITCH Control*

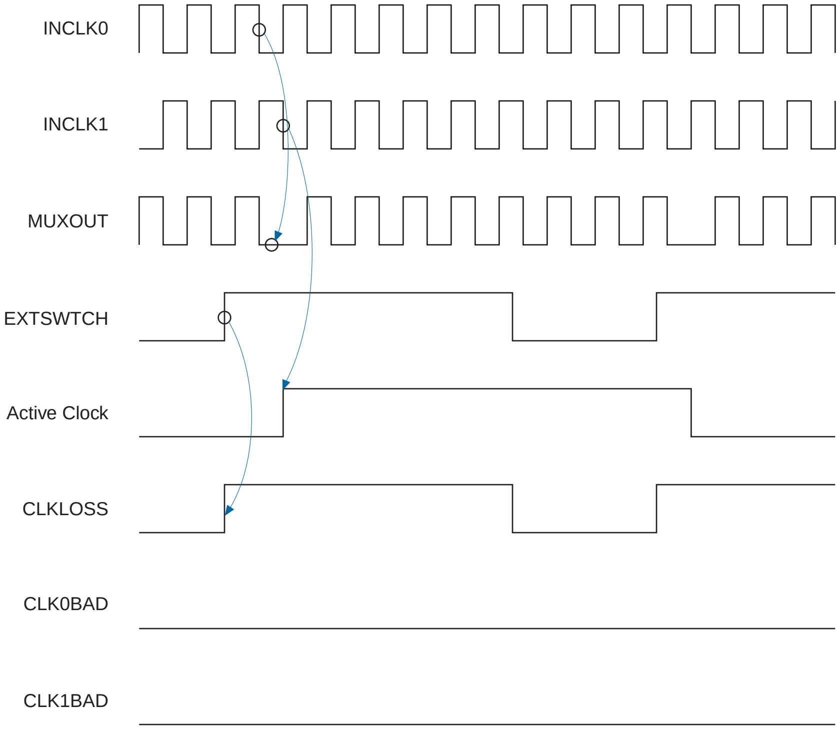
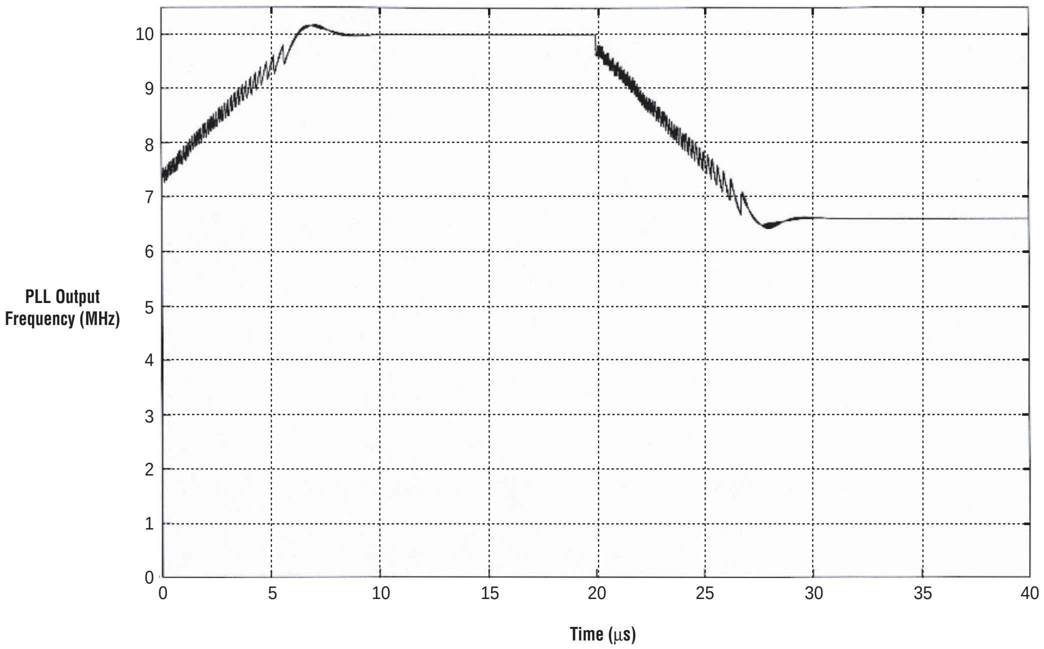


Figure 1–18 shows a simulation of using switchover for two different reference frequencies. In this example simulation, the reference clock is either 100 or 66 MHz. The PLL begins with $f_{IN}$ = 100 MHz and is allowed to lock. At 20 µs, the clock is switched to the secondary clock, which is at 66 MHz.

**Figure 1–18. Switchover Simulation** Note (1)



*Note to Figure 1–18:*

(1) This simulation was performed under the following conditions: the *n* counter is set to 2, the *m* counter is set to 16, and the output counter is set to 8. Therefore, the VCO operates at 800 MHz for the 100-MHz input and at 528 MHz for the 66-MHz reference input.

### Lock-Signal-Based Switchover

The lock circuitry can initiate the automatic switchover. This is useful for cases where the input clock is still clocking, but its characteristics have changed so that the PLL is not locked to it. The switchover lock input is based on both the gated and ungated lock signals. If the ungated lock is low, the switch-over lock will not enable until the gated lock has reached its terminal count. The design will activate the switch-over enable if the gated lock is high, but the ungated lock goes low. The switch-over timing for this mode is similar to the waveform shown in Figure 1–17 for `EXTSWITCH` control, except the lock switch-over enable replaces `EXTSWITCH`. Figure 1–19 shows the switch-over enable circuit when controlled by lock and gated lock.

*Figure 1–19. Switch-Over State Machine*

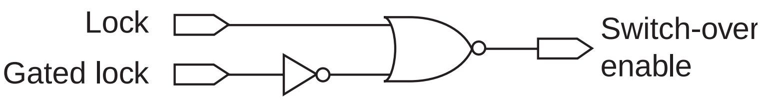


Table 1–9 summarizes the signals used for clock switchover.

*Table 1–9. Clock Switchover Ports*

| Port | Description | Source | Destination |
|---|---|---|---|
| `inclk0` | Reference `clk0` to the PLL | I/O pin | Clock switch-over circuit |
| `inclk1` | Reference `clk1` to the PLL | I/O pin | Clock switch-over circuit |
| `clkbad0` | Signal indicating that `refclk0` is no longer toggling | Clock switch-over circuit | Logic array |
| `clkbad1` | Signal indicating that `refclk1` is no longer toggling | Clock switch-over circuit | Logic array |
| `extswitch` | Switchover signal used to initiate clock switchover asynchronously | Logic array or I/O pin | Clock switch-over circuit |
| `clkloss` | Signal indicating that the switch-over circuit detected a switch condition | Clock switch-over circuit | Logic array |
| `locked` | Signal indicating that the PLL has lost lock | PLL | Clock switch-over circuit |
| `activeclock` | Signal to indicate which clock (`0` = `inclk0` or `1` = `inclk1`) is driving the PLL | PLL | Logic array |

### *Software Support*

All the switchover ports shown in Table 1–9 are supported in the MegaWizard Plug-In Manager. The MegaWizard Plug-In Manager supports two methods for clock switchover:

- Automatic switchover, upon loss of the reference clock
- An internal user-controlled signal to trigger switchover

If the primary and secondary clock frequencies are different, the Quartus II software will select the proper parameters to keep the VCO within the recommended frequency range.

For more information on PLL software support in the Quartus II software, see the *altpll Megafunction User Guide*.

### *Guidelines*

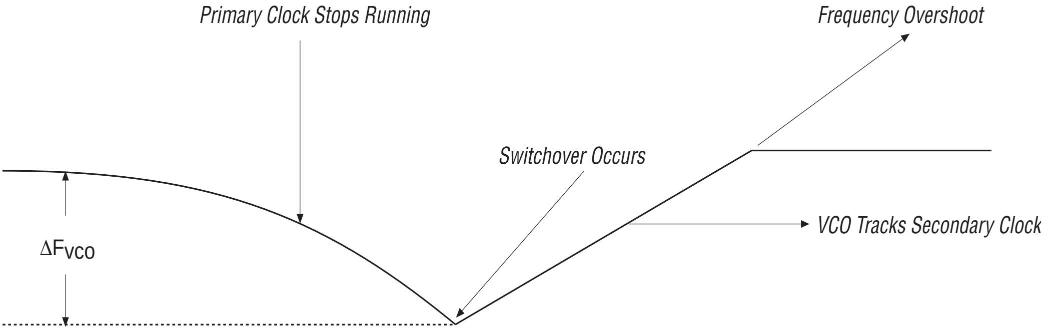
Use the following guidelines to design with clock switchover in PLLs.

- The `EXTSWTCH` signal has a minimum pulse width that is based on the two reference clock periods. The `EXTSWTCH` pulse width must be greater than or equal to the period of the current reference clock ($t_{from\_clk}$) multiplied by two plus the rounded up version of the ratio of the two reference clock periods. As an example, assume nominally $t_{to\_clk}$ is equal to $t_{from\_clk}$. Then the `EXTSWTCH` pulse width should be at least three times the period of the clock pulse.

  $t_{EXTSWTCHmin} \geq t_{from\_clk} \times [2 + int_{round\_up} (t_{to\_clk}/t_{from\_clk})]$

- Applications that require a clock switch-over feature and a small frequency drift should use a low-bandwidth PLL. The low-bandwidth PLL reacts slower than a high-bandwidth PLL to changes to its reference input clock. When the switchover happens, a low-bandwidth PLL propagates this stopping of the clock to the output slower than a high-bandwidth PLL. A low-bandwidth PLL filters out jitter on the reference clock. However, the trade-off is that the low-bandwidth PLL also increases lock time.
- Stratix device PLLs can use both the automatic clock switch-over and the `extswitch` input simultaneously. Therefore, the switch-over circuitry can automatically switch from the primary to the secondary clock, and once the primary clock stabilizes again, the `clkswitch` signal can switch back to the primary clock. During switchover, the PLL VCO continues to run and will slow down, generating frequency drift on the PLL outputs. The `extswitch` signal controls switchover with its rising edge only.
- The clock switchover event is glitch-free. After the switch occurs, there is still a finite resynchronization period to lock onto a new clock as the VCO ramps up. The exact amount of time it takes for the PLL to relock is dependent on the PLL configuration. Designers can use the programmable bandwidth feature of the PLL to adjust the relock time.
- Figure 1–20 shows how the VCO frequency gradually decreases when the primary clock is lost and then increases as the VCO locks on to the secondary clock. After the VCO locks on to the secondary clock, there may be some overshoot (an over-frequency condition) in the VCO frequency.

*Figure 1–20. VCO Switchover Operating Frequency*



- Disable the system during switchover if it is not tolerant to frequency variations during the PLL resynchronization period. There are two ways to disable the system. First, the system may require some time to stop before switchover occurs. The switch-over circuitry includes an optional five-bit counter to delay when the reference clock is switched. The designer can control the time-out setting on this counter (up to 32 cycles of latency) before the clock source switches. The designer can use these cycles for disaster recovery. The clock output frequency will vary slightly during those 32 cycles since the VCO can still drift without an input clock. Programmable bandwidth can control the PLL response to limit drift during this 32-cycle period.
- A second option available is the ability to use the PFD enable signal (`pfdena`) along with user-defined control logic. In this case, the designer can use `clk0_bad` and `clk1_bad` status signals to turn off the PFD so the VCO maintains its last frequency. Designers can also use their own state machine to switch over to the secondary clock. Upon re-enabling the PFD, output clock enable signals (`clkena`) can disable clock outputs during the switchover and resynchronization period. Once the lock indication is stable, the system can re-enable the output clock(s).

For more information on a design issue affecting the `clk0_bad` and `clk1_bad` signals, see the *Stratix FPGA Errata Sheet*.

## Spread-Spectrum Clocking

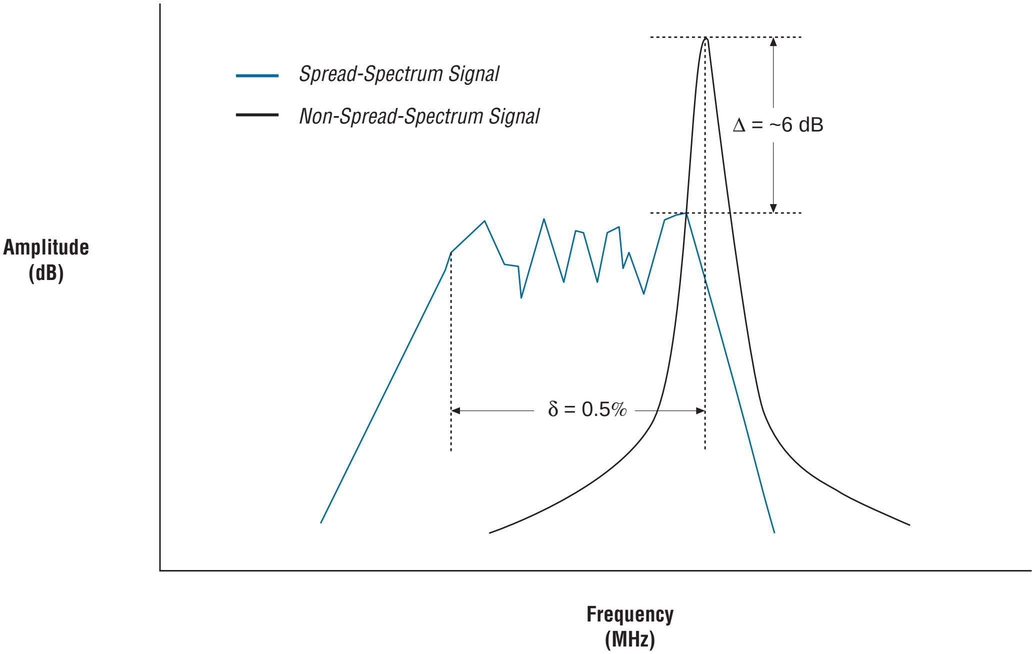
Digital clocks are generally square waves with short rise times and a 50% duty cycle. These high-speed digital clocks concentrate a significant amount of energy in a narrow bandwidth at the target frequency and at the higher frequency harmonics. This results in high energy peaks and increased electromagnetic interference (EMI). The radiated noise from the energy peaks travels in free air and, if not minimized, can lead to corrupted data and intermittent system errors, which can jeopardize system reliability.

### *Background*

Traditional methods for limiting EMI include shielding, filtering, and multi-layer printed circuit boards (PCBs). However, these methods significantly increase the overall system cost and sometimes are not enough to meet EMI compliance. Spread-spectrum technology gives designers a simple and effective technique for reducing EMI emissions without additional cost and the trouble of re-designing a board.

Spread-spectrum technology modulates the target frequency over a small range. For example, if a 100-MHz signal has a 0.5% down-spread modulation, then the frequency is swept from 99.5 to 100 MHz. Figure 1–21 gives a graphical representation of the energy present in a spread-spectrum signal vs. a non-spread-spectrum signal. It is apparent that instead of concentrating the energy at the target frequency, the energy is re-distributed across a wider band of frequencies, which reduces peak energy. Not only is there a reduction in the fundamental peak EMI components, but there is also a reduction in EMI of the higher order harmonics. Since some regulations focus on peak EMI emissions, and not average EMI emissions, spread-spectrum technology is a valuable method of EMI reduction.

*Figure 1–21. Spread-Spectrum Signal Energy vs. Non-Spread-Spectrum Signal Energy*



Spread-spectrum technology would benefit a design with high EMI emissions and/or strict EMI requirements. Device-generated EMI is dependent on frequency, output voltage swing amplitude, and slew rate. For example, a design using LVDS already has low EMI emissions because of the low-voltage swing. The differential LVDS signal also allows for EMI rejection within the signal. Therefore, this situation may not require spread-spectrum technology.

### Description

Stratix and Stratix GX device enhanced PLLs feature spread-spectrum technology to reduce the EMI emitted from the device. The enhanced PLL provides up to a 0.5% down spread (–0.5%) using a triangular, also known as linear, modulation profile. The modulation frequency is programmable and ranges from approximately 30 to 150 kHz. The spread percentage is based on the clock input to the PLL and the *m* and *n* settings. Spread-spectrum technology reduces the peak energy by 4 to 6 dB at the target frequency. However, this number is dependent on bandwidth and the *m* and *n* counter values and can vary from design to design.

Spread percentage, also known as modulation width, is defined as the percentage that the design modulates the target frequency. A negative (–) percentage indicates a down spread, a positive (+) percentage indicates an up spread, and a (±) indicates a center spread. Modulation frequency is the frequency of the spreading signal or how fast the signal sweeps from the minimum to the maximum frequency. Down-spread modulation shifts the target frequency down by half the spread percentage, centering the modulated waveforms on a new target frequency.

The *m* and *n* counter values are toggled at the same time between two fixed values. The loop filter then slowly changes the VCO frequency to provide the spreading effect, which results in a triangular modulation. An additional spread-spectrum counter (shown in Figure 1–22) sets the modulation frequency. Figure 1–22 shows how spread-spectrum technology is implemented in the Stratix device enhanced PLL.

***Figure 1–22. Spread-Spectrum Circuit Block Diagram***

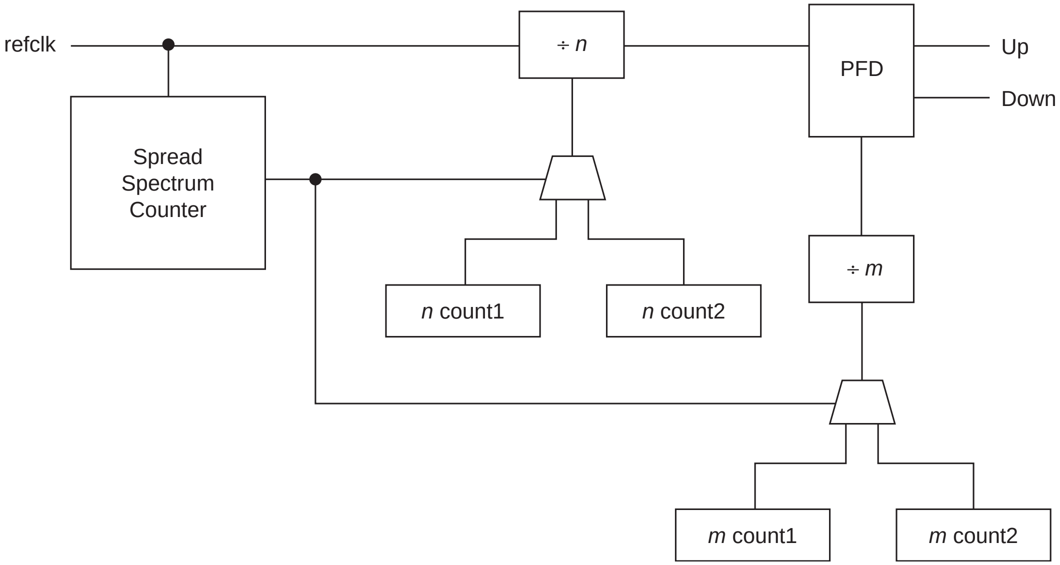


Figure 1–23 shows a VCO frequency waveform when toggling between different counter values. Since the enhanced PLL switches between two different *m* and *n* values, the result is a straight line between two frequencies, which gives a linear modulation. The magnitude of modulation is determined by the ratio of two $m/n$ sets. The percent spread is determined by:

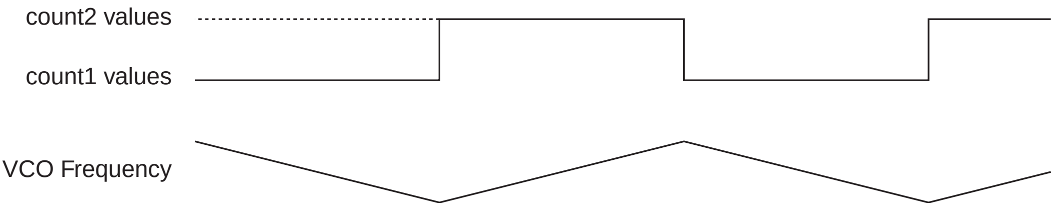
$$\text{percent spread} = (f_{VCOmax} - f_{VCOmin}) / f_{VCOmax} = 1 - [(m_2 \times n_1) / (m_1 \times n_2)]$$

The maximum and minimum VCO frequency is defined as:

$$f_{VCOmax} = (m_1 / n_1) \times f_{ref}$$

$$f_{VCOmin} = (m_2 / n_2) \times f_{ref}$$

**Figure 1–23. VCO Frequency Modulation Waveforms**



### Software Support

The designer can enter the desired down-spread percentage and modulation frequency in the MegaWizard Plug-In Manager through the Quartus II software. Alternatively, the MegaWizard Plug-In Manager can set the `downspread` parameter in the `altpll` megafunction to the desired down-spread percentage. Timing analysis ensures the design operates at the maximum spread frequency and meets all timing requirements.

For more information on PLL software support in the Quartus II software, see the *altpll Megafunction User Guide*.

### Guidelines

If the design cascades PLLs, the source, or upstream, PLL should have a low bandwidth setting, while the destination, or downstream, PLL should have a high bandwidth setting. The upstream PLL must have a low bandwidth setting because a PLL will not generate jitter higher than its bandwidth. The downstream PLL must have a high bandwidth setting to track the jitter. The design must use the spread-spectrum feature in a low-bandwidth PLL, and, therefore, the Quartus II software automatically sets the spread-spectrum PLL's bandwidth to low.

☞ Designs cannot use spread-spectrum PLLs with the programmable bandwidth feature.

Stratix and Stratix GX devices can accept a spread-spectrum input with typical modulation frequencies. However, the device cannot automatically detect that the input is a spread-spectrum signal. Instead, the input signal will look like deterministic jitter at the input of the downstream PLL.

Spread spectrum should only have a minor effect on cycle-to-cycle jitter, but period jitter will increase. Cycle-to-cycle jitter is the deviation of a clock's cycle time from its previous cycle position. Period jitter measures the variation of a clock's output transition from its ideal position over consecutive edges.

With down-spread modulation, the peak of the modulated waveform is the actual target frequency. Therefore, the system will never exceed the maximum clock speed. To maintain reliable communication, the entire system/subsystem should use the Stratix or Stratix GX device as the clock source. Communication could fail if the Stratix or Stratix GX logic array is clocked by the spread-spectrum clock, but the data it receives from another device is not.

Since spread spectrum affects the *m* counter values, all spread-spectrum PLL outputs are affected. Therefore, if only one spread-spectrum signal is needed, the clock signal should use a separate PLL without other outputs from that PLL.

No special considerations are needed when using spread spectrum with the clock switchover feature. This is because the clock switchover feature does not affect the *m* and *n* counter values, which are the counter values that are switching when using spread spectrum.

## PLL Reconfiguration

See *Application Note 282: Implementing PLL Reconfiguration in Stratix & Stratix GX Devices* for information on PLL reconfiguration.

## Enhanced PLL Pins

Table 1–10 shows the physical pins and their purpose for the Enhanced PLLs. For `inclk` port connections to pins see "Clocking" on page 1–48.

*Table 1–10. Enhanced PLL Pins (Part 1 of 3)*

| Pin | Description |
|---|---|
| `CLK4p/n` | Single-ended or differential pins that can drive the `inclk` port for PLL 6. |
| `CLK5p/n` | Single-ended or differential pins that can drive the `inclk` port for PLL 6. |

*Table 1–10. Enhanced PLL Pins (Part 2 of 3)*

| Pin | Description |
|---|---|
| `CLK6p/n` | Single-ended or differential pins that can drive the `inclk` port for PLL 12. |
| `CLK7p/n` | Single-ended or differential pins that can drive the `inclk` port for PLL 12. |
| `CLK12p/n` | Single-ended or differential pins that can drive the `inclk` port for PLL 11. |
| `CLK13p/n` | Single-ended or differential pins that can drive the `inclk` port for PLL 11. |
| `CLK14p/n` | Single-ended or differential pins that can drive the `inclk` port for PLL 5. |
| `CLK15p/n` | Single-ended or differential pins that can drive the `inclk` port for PLL 5. |
| `PLL5_FBp/n` | Single-ended or differential pins that can drive the `fbin` port for PLL 5. |
| `PLL6_FBp/n` | Single-ended or differential pins that can drive the `fbin` port for PLL 6. |
| `PLLENABLE` | Dedicated input pin that drives the `pllena` port of all or a set of PLLs. If you do not use this pin, connect it to ground. |
| `PLL5_OUT[3..0]p/n` | Single-ended or differential pins driven by `extclk[3..0]` ports from PLL 5. |
| `PLL6_OUT[3..0]p/n` | Single-ended or differential pins driven by `extclk[3..0]` ports from PLL 6. |
| `PLL11_OUT, CLK13n` | Single-ended output pin driven by `clk0` port from PLL 11. |
| `PLL12_OUT, CLK6n` | Single-ended output pin driven by `clk0` port from PLL 12. |
| `VCCA_PLL5` | Analog power for PLL 5. The designer must connect this pin to 1.5 V, even if the PLL is not used. |
| `VCCG_PLL5` | Guard ring power for PLL 5. The designer must connect this pin to 1.5 V, even if the PLL is not used. |
| `GNDA_PLL5` | Analog ground for PLL 5. The designer can connect this pin to the `GND` plane on the board. |
| `GNDG_PLL5` | Guard ring ground for PLL 5. The designer can connect this pin to the `GND` plane on the board. |
| `VCCA_PLL6` | Analog power for PLL 6. The designer must connect this pin to 1.5 V, even if the PLL is not used. |
| `VCCG_PLL6` | Guard ring power for PLL 6. The designer must connect this pin to 1.5 V, even if the PLL is not used. |
| `GNDA_PLL6` | Analog ground for PLL 6. The designer can connect this pin to the `GND` plane on the board. |
| `GNDG_PLL6` | Guard ring ground for PLL 6. The designer can connect this pin to the `GND` plane on the board. |
| `VCCA_PLL11` | Analog power for PLL 11. The designer must connect this pin to 1.5 V, even if the PLL is not used. |
| `VCCG_PLL11` | Guard ring power for PLL 11. The designer must connect this pin to 1.5 V, even if the PLL is not used. |
| `GNDA_PLL11` | Analog ground for PLL 11. The designer can connect this pin to the `GND` plane on the board. |
| `GNDG_PLL11` | Guard ring ground for PLL 11. The designer can connect this pin to the `GND` plane on the board. |

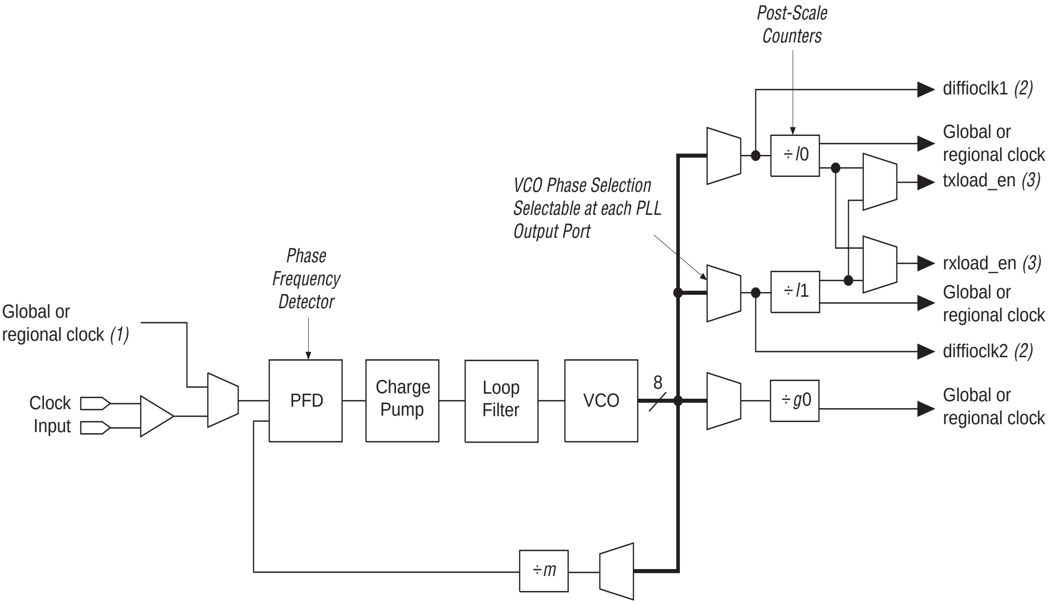
*Table 1–10. Enhanced PLL Pins (Part 3 of 3)*

| Pin | Description |
|---|---|
| `VCCA_PLL12` | Analog power for PLL 12. The designer must connect this pin to 1.5 V, even if the PLL is not used. |
| `VCCG_PLL12` | Guard ring power for PLL 12. The designer must connect this pin to 1.5 V, even if the PLL is not used. |
| `GNDA_PLL12` | Analog ground for PLL 12. The designer can connect this pin to the `GND` plane on the board. |
| `GNDG_PLL12` | Guard ring ground for PLL 12. The designer can connect this pin to the `GND` plane on the board. |
| `VCC_PLL5_OUTA` | External clock output $V_{CCIO}$ power for `PLL5_OUT0p`, `PLL5_OUT0n`, `PLL5_OUT1p`, and `PLL5_OUT1n` outputs from PLL 5. |
| `VCC_PLL5_OUTB` | External clock output $V_{CCIO}$ power for `PLL5_OUT2p`, `PLL5_OUT2n`, `PLL5_OUT3p`, and `PLL5_OUT3n` outputs from PLL 5. |
| `VCC_PLL6_OUTA` | External clock output $V_{CCIO}$ power for `PLL5_OUT0p`, `PLL5_OUT0n`, `PLL5_OUT1p`, and `PLL5_OUT1n` outputs from PLL 6. |
| `VCC_PLL6_OUTB` | External clock output $V_{CCIO}$ power for `PLL5_OUT2p`, `PLL5_OUT2n`, `PLL5_OUT3p`, and `PLL5_OUT3n` outputs from PLL 6. |

## Fast PLLs

Stratix devices contain up to eight fast PLLs and Stratix GX devices contain up to four fast PLLs. Both device PLLs have high-speed differential I/O interface ability along with general-purpose features. Figure 1–24 shows a diagram of the fast PLL. This section discusses the general purpose abilities of the Fast PLL. For information on the high-speed differential I/O interface capabilities, see Chapter 5, Using High-Speed Differential I/O Interfaces in Stratix Devices.

*Figure 1–24. Stratix & Stratix GX Fast PLL Block Diagram*



*Notes to Figure 1–24:*

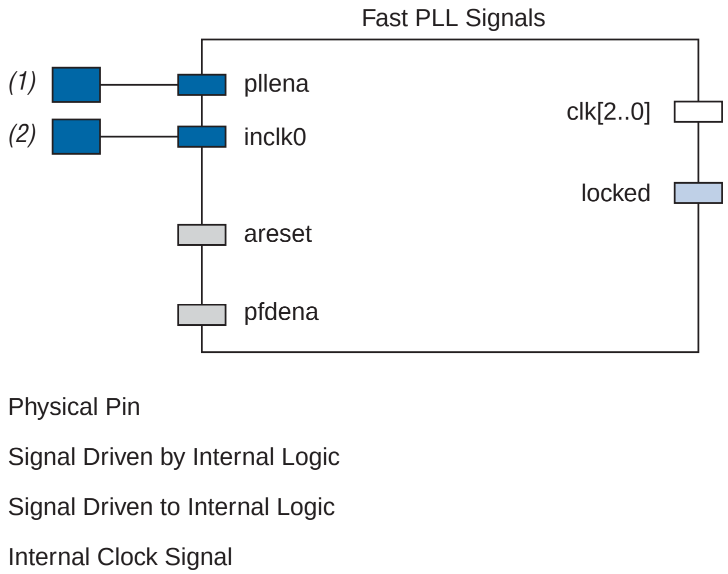
(1) The global or regional clock input can be driven by an output from another PLL or a pin-driven global or regional clock. It cannot be driven by internally-generated global signals.

(2) In high-speed differential I/O support mode, this high-speed PLL clock feeds the SERDES. Stratix and Stratix GX devices only support one rate of data transfer per fast PLL in high-speed differential I/O support mode.

(3) This signal is a high-speed differential I/O support SERDES control signal.

Figure 1–25 shows all possible ports related to fast PLLs.

*Figure 1–25. Fast PLL Ports & Physical Destinations*



*Notes to Figure 1–25:*

(1) This input pin is shared by all enhanced and fast PLLs.

(2) This input pin is either single-ended or differential.

Table 1–11 and Table 1–12 show the description of all fast PLL ports.

*Table 1–11. Fast PLL Input Signals*

| Name | Description | Source | Destination |
|---|---|---|---|
| `inclk1` | Reference clock input to PLL | Pin | PFD |
| `pllena` | Enable pin for enabling or disabling all or a set of PLLs – active high | Pin | PLL control signal |
| `areset` | Signal used to reset the PLL which will re-synchronize all the counter outputs—active high | Logic array | PLL control signal |
| `pfdena` | Enables the up/down outputs from the phase-frequency detector—active high | Logic array | PFD |

*Table 1–12. Fast PLL Output Signals*

| Name | Description | Source | Destination |
|---|---|---|---|
| `clk[2..0]` | PLL outputs driving regional or global clock | PLL counter | Internal clock |
| `locked` | Lock output from lock detect circuit—active high | PLL lock detect | Logic array |

## Clock Multiplication & Division

Stratix and Stratix GX device fast PLLs provide clock synthesis for PLL output ports using $m$/(post scaler) scaling factors. The input clock is multiplied by the $m$ feedback factor. Each output port has a unique post scale counter to divide down the high-frequency VCO. There is one multiply counter, $m$, per fast PLL with a range of 1 to 32. There are three post-scale counters ($g0$, $l0$, and $l1$) for the regional and global clock output ports. All post-scale counters range from 1 to 32. If the design uses a high-speed serial interface, the designer can set the output counter to 1 to allow the high-speed VCO frequency to drive the SERDES.

## External Clock Outputs

Each fast PLL supports differential or single-ended outputs for source-synchronous transmitters or for general-purpose external clocks. There are no dedicated external clock output pins. The fast PLL global or regional outputs can drive any I/O pin as an external clock output pin. The I/O standards supported by any particular bank determines what standards are possible for an external clock output driven by the fast PLL in that bank. Refer to *Application Note 201: Using Selectable I/O Standards in Stratix & Stratix GX Devices* for output standard support.

Table 1–13 shows the I/O standards supported by fast PLL input pins.

*Table 1–13. Fast PLL Port I/O Standards (Part 1 of 2)*

| I/O Standard | Input | |
|---|---|---|
| | INCLK | PLLENABLE |
| LVTTL | ✓ | ✓ |
| LVCMOS | ✓ | ✓ |
| 2.5 V | ✓ | |
| 1.8 V | ✓ | |
| 1.5 V | ✓ | |
| 3.3-V PCI | | |

*Table 1–13. Fast PLL Port I/O Standards (Part 2 of 2)*

| I/O Standard | Input | |
|---|---|---|
| | INCLK | PLLENABLE |
| 3.3-V PCI-X | | |
| LVPECL | ✓ | |
| PCML | ✓ | |
| LVDS | ✓ | |
| HyperTransport technology | ✓ | |
| Differential HSTL | | |
| Differential SSTL | | |
| 3.3-V GTL | | |
| 3.3-V GTL+ | ✓ | |
| 1.5-V HSTL class I | ✓ | |
| 1.5-V HSTL class II | | |
| SSTL-18 class I | ✓ | |
| SSTL-18 class II | | |
| SSTL-2 class I | ✓ | |
| SSTL-2 class II | ✓ | |
| SSTL-3 class I | ✓ | |
| SSTL-3 class II | ✓ | |
| AGP (1× and 2×) | | |
| CTT | ✓ | |

## Phase Shifting

Stratix and Stratix GX device fast PLLs have advanced clock shift ability to provide programmable phase shift. These parameters are set in the Quartus II software.

The Quartus II software automatically sets the phase taps and counter settings according to the phase shift entry. Designers enter a desired phase shift and the Quartus II software automatically sets the closest setting achievable. This type of phase shift is not reconfigurable during system operation. Designers can enter a phase shift (in degrees or time units) for each PLL clock output port or for all outputs together in one shift. Designers can perform phase shifting in time units with a resolution range of 125 to 416.66 ps to create a function of frequency input and the multiplication and division factors (i.e., it is a function of the VCO period), with the finest step being equal to an eighth (×0.125) of the VCO period. Each clock output counter can choose a different phase of the

VCO period from up to eight taps for individual fine-step selection. Also, each clock output counter can use a unique initial count setting to achieve individual coarse shift selection in steps of one VCO period. The combination of coarse shift and grain shift allows phase shifting for the entire input clock period.

The equation to determine the precision of phase in degrees is: 45° ÷ post-scale counter value. Therefore, the maximum step size is 45°, and smaller steps are possible depending on the multiplication and division ratio necessary on the output counter port.

This type of phase shift provides the highest precision since it is the least sensitive to process, supply, and temperature variation.

## Programmable Duty Cycle

The programmable duty cycle allows the fast PLL to generate clock outputs with a variable duty cycle. This feature is supported on each fast PLL post-scale counter. *g*0, *l*0, and *l*1 all support programmable duty. The designer uses a low- and high-time count setting for the post-scale counters to set the duty cycle. The Quartus II software uses the frequency input and multiply/divide rate desired to select the post-scale counter, which determines the possible choices for each duty cycle. The precision of the duty cycle is determined by the post-scale counter value chosen on an output. The precision is defined by 50% divided by the post-scale counter value. The closest value to 100% is not achievable for a given counter value. For example, if the *g*0 counter is 10, then steps of 5% are possible for duty cycle choices between 5 to 90%.

If the device uses external feedback, the designer must set the duty cycle for the counter driving off the device to 50%.

## Control Signals

The lock output indicates a stable clock output signal in phase with the reference clock. Unlike enhanced PLLs, fast PLLs do not have a lock filter counter.

The `pllenable` pin is a dedicated pin that enables/disables both PLLs. When the `pllenable` pin is low, the clock output ports are driven by `GND` and all the PLLs go out of lock. When the `pllenable` pin goes high again, the PLLs relock and resynchronize to the input clocks. The designer can choose which PLLs are controlled by the `pllenable` by connecting the `pllenable` input port of the `altpll` megafunction to the common `pllenable` input pin.

The `areset` signals are reset/resynchronization inputs for each fast PLL. The Stratix and Stratix GX device can drive these input signals from an input pin or from LEs. When driven high, the PLL counters reset, clearing the PLL output and placing the PLL out of lock. The VCO will set back to its nominal setting (~700 MHz). When driven low again, the PLL will resynchronize to its input clock as it relocks. If the target VCO frequency is below this nominal frequency, then the output frequency will start at a higher value then desired as it locks. The `areset` signal for fast PLLs will be supported in a future version of the Quartus II software.

The `pfdena` signals control the PFD output with a programmable gate. If the designer disables the PFD, the VCO will operate at its last set value of control voltage and frequency with some long-term drift to a lower frequency. The system will continue running when the PLL goes out of lock or the input clock disables. By maintaining the last locked frequency, the system has time to store its current settings before shutting down. The `pfdena` signal for fast PLLs will be supported in a future version of the Quartus II software.

## Pins

Table 1–14 shows the physical pins and their purpose for the Fast PLLs. For inclk port connections to pins see "Clocking" on page 1–48.

*Table 1–14. Fast PLL Pins (Part 1 of 3)*

| Pin | Description |
|---|---|
| `CLK0p/n` | Single-ended or differential pins that can drive the inclk port for PLL 1 or 7. |
| `CLK1p/n` | Single-ended or differential pins that can drive the inclk port for PLL 1. |
| `CLK2p/n` | Single-ended or differential pins that can drive the inclk port for PLL 2 or 8. |
| `CLK3p/n` | Single-ended or differential pins that can drive the inclk port for PLL 2. |
| `CLK8p/n` | Single-ended or differential pins that can drive the inclk port for PLL 3 or 9. *(1)* |
| `CLK9p/n` | Single-ended or differential pins that can drive the inclk port for PLL 3. *(1)* |
| `CLK10p/n` | Single-ended or differential pins that can drive the inclk port for PLL 4 or 10. *(1)* |
| `CLK11p/n` | Single-ended or differential pins that can drive the inclk port for PLL 4. *(1)* |
| `FPLL7CLKp/n` | Single-ended or differential pins that can drive the inclk port for PLL 7. |
| `FPLL8CLKp/n` | Single-ended or differential pins that can drive the inclk port for PLL 8. |
| `FPLL9CLKp/n` | Single-ended or differential pins that can drive the inclk port for PLL 9. *(1)* |
| `FPLL10CLKp/n` | Single-ended or differential pins that can drive the inclk port for PLL 10. *(1)* |
| `PLLENABLE` | Dedicated input pin that drives the pllena port of all or a set of PLLs. If you do not use this pin, connect it to ground. |

*Table 1–14. Fast PLL Pins (Part 2 of 3)*

| Pin | Description |
|---|---|
| `VCCA_PLL1` | Analog power for PLL 1. The designer must connect this pin to 1.5 V, even if the PLL is not used. |
| `VCCG_PLL1` | Guard ring power for PLL 1. The designer must connect this pin to 1.5 V, even if the PLL is not used. |
| `GNDA_PLL1` | Analog ground for PLL 1. The designer can connect this pin to the GND plane on the board. |
| `GNDG_PLL1` | Guard ring ground for PLL 1. The designer can connect this pin to the GND plane on the board. |
| `VCCA_PLL2` | Analog power for PLL 2. The designer must connect this pin to 1.5 V, even if the PLL is not used. |
| `VCCG_PLL2` | Guard ring power for PLL 2. The designer must connect this pin to1.5 V, even if the PLL is not used. |
| `GNDA_PLL2` | Analog ground for PLL 2. The designer can connect this pin to the GND plane on the board. |
| `GNDG_PLL2` | Guard ring ground for PLL 2. The designer can connect this pin to the GND plane on the board. |
| `VCCA_PLL3` | Analog power for PLL 3. The designer must connect this pin to 1.5 V, even if the PLL is not used. *(1)* |
| `VCCG_PLL3` | Guard ring power for PLL 3. The designer must connect this pin to 1.5 V, even if the PLL is not used. *(1)* |
| `GNDA_PLL3` | Analog ground for PLL 3. The designer can connect this pin to the GND plane on the board. *(1)* |
| `GNDG_PLL3` | Guard ring ground for PLL 3. The designer can connect this pin to the GND plane on the board. *(1)* |
| `VCCA_PLL4` | Analog power for PLL 4. The designer must connect this pin to 1.5 V, even if the PLL is not used. *(1)* |
| `VCCG_PLL4` | Guard ring power for PLL 4. The designer must connect this pin to 1.5 V, even if the PLL is not used. *(1)* |
| `GNDA_PLL4` | Analog ground for PLL 4. The designer can connect this pin to the GND plane on the board. *(1)* |
| `GNDG_PLL4` | Guard ring ground for PLL 4. The designer can connect this pin to the GND plane on the board. *(1)* |
| `VCCA_PLL7` | Analog power for PLL 7. The designer must connect this pin to 1.5 V, even if the PLL is not used. |
| `VCCG_PLL7` | Guard ring power for PLL 7. The designer must connect this pin to 1.5 V, even if the PLL is not used. |
| `GNDA_PLL7` | Analog ground for PLL 7. The designer can connect this pin to the GND plane on the board. |
| `GNDG_PLL7` | Guard ring ground for PLL 7. The designer can connect this pin to the GND plane on the board. |

*Table 1–14. Fast PLL Pins (Part 3 of 3)*

| Pin | Description |
|---|---|
| `VCCA_PLL8` | Analog power for PLL 8. The designer must connect this pin to 1.5 V, even if the PLL is not used. |
| `VCCG_PLL8` | Guard ring power for PLL 8. The designer must connect this pin to 1.5 V, even if the PLL is not used. |
| `GNDA_PLL8` | Analog ground for PLL 8. The designer can connect this pin to the GND plane on the board. |
| `GNDG_PLL8` | Guard ring ground for PLL 8. The designer can connect this pin to the GND plane on the board. |
| `VCCA_PLL9` | Analog power for PLL 9. The designer must connect this pin to 1.5 V, even if the PLL is not used. *(1)* |
| `VCCG_PLL9` | Guard ring power for PLL 9. The designer must connect this pin to 1.5 V, even if the PLL is not used. *(1)* |
| `GNDA_PLL9` | Analog ground for PLL 9. The designer can connect this pin to the GND plane on the board. *(1)* |
| `GNDG_PLL9` | Guard ring ground for PLL 9. The designer can connect this pin to the GND plane on the board. *(1)* |
| `VCCA_PLL10` | Analog power for PLL 10. The designer must connect this pin to 1.5 V, even if the PLL is not used. *(1)* |
| `VCCG_PLL10` | Guard ring power for PLL 10. The designer must connect this pin to 1.5 V, even if the PLL is not used. *(1)* |
| `GNDA_PLL10` | Analog ground for PLL 10. The designer can connect this pin to the GND plane on the board. *(1)* |
| `GNDG_PLL10` | Guard ring ground for PLL 10. The designer can connect this pin to the GND plane on the board. *(1)* |

*Note to Table 1–14:*

(1) PLLs 3, 4, 9, and 10 are not available on Stratix GX devices for general-purpose configuration. These PLLs are part of the HSSI block. See *Application Note 236: Using Source-Synchronous Signaling with DPA in Stratix GX Devices* for more information.

## Clocking

Stratix and Stratix GX devices provide a hierarchical clock structure and multiple PLLs with advanced features. The large number of clocking resources in combination with the clock synthesis precision provided by enhanced and fast PLLs provides a complete clock management solution.

### Global & Hierarchical Clocking

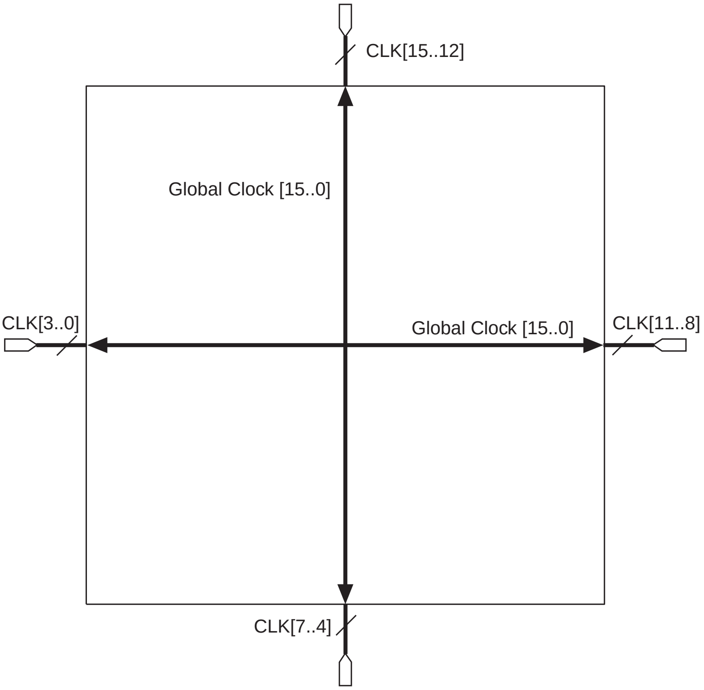
Stratix and Stratix GX devices provide 16 dedicated global clock networks, 16 regional clock networks (four per device quadrant), and 8 dedicated fast regional clock networks. These clocks are organized into a hierarchical clock structure that allows for up to 22 clocks per device region with low skew and delay. This hierarchical clocking scheme provides up to 48 unique clock domains within Stratix and Stratix GX devices.

There are 16 dedicated clock pins (`CLK[15..0]`) on Stratix devices and 12 dedicated clock pins (`CLK[11..0]`) on Stratix GX devices to drive either the global or regional clock networks. Four clock pins drive each side of the Stratix device, as shown in Figures 1–26 and 1–27. On Stratix GX devices, four clock pins drive the top, left, and bottom sides of the device. The clocks on the right side of the device are not available for general-purpose PLLs. Enhanced and fast PLL outputs can also drive the global and regional clock networks.

### *Global Clock Network*

These clocks drive throughout the entire device, feeding all device quadrants. All resources within the device—IOEs, LEs, DSP blocks, and all memory blocks—can use the global clock networks as clock sources. These resources can also be used for control signals, such as clock enables and synchronous or asynchronous clears fed from the external pin. Internal logic can also drive the global clock networks for internally generated global clocks and asynchronous clears, clock enables, or other control signals with large fanout. Figure 1–26 shows the 16 dedicated `CLK` pins driving global clock networks.

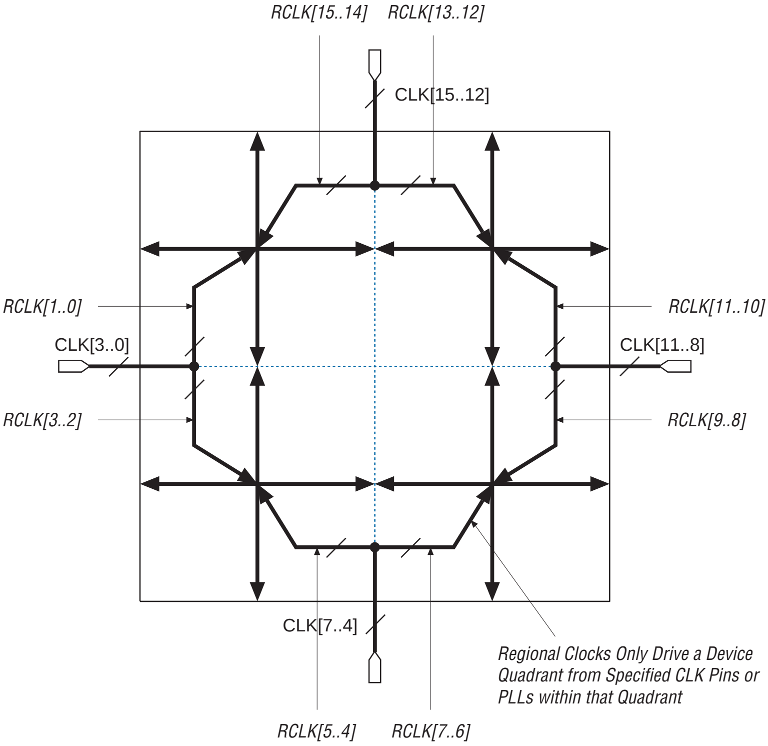
*Figure 1–26. Global Clocking*



### *Regional Clock Network*

There are four regional clock networks `RCLK[3..0]` within each quadrant of the Stratix or Stratix GX device that are driven by the same dedicated `CLK[15..0]` input pins or from PLL outputs. The regional clock networks only pertain to the quadrant they drive into. The regional clock networks provide the lowest clock delay and skew for logic contained within a single quadrant. The `CLK` clock pins symmetrically drive the `RCLK` networks within a particular quadrant, as shown in Figure 1–27.

*Figure 1–27. Regional Clocks*



## Clock Input Connections

Two `CLK` pins drive each enhanced PLL. Designers can use either one or both pins for clock switch-over inputs into the PLL. Either pin can be the primary clock source for clock switch-over, which is controlled in the Quartus II software. Enhanced PLLs 5 and 6 also have feedback input pins as shown in Table 1–15.

Input clocks for fast PLLs 1, 2, 3, and 4 come from `CLK` pins. Stratix GX devices use PLLs 3 and 4 in the HSSI block only. A multiplexer chooses one of two possible `CLK` pins to drive each PLL. This multiplexer is not a clock switch-over multiplexer and is only used for clock input connectivity.

Either a `FPLLCLK` input pin or a `CLK` pin can drive the fast PLLs in the corners (7, 8, 9, and 10) when used for general purpose. `CLK` pins cannot drive these fast PLLs in high-speed differential I/O mode. PLLs 9 and 10 areused for the HSSI block in Stratix GX devices and are not available.

Table 1–15 and 1–16 show which PLLs are available for each Stratix or Stratix GX device and which input clock pin drives which PLLs.

*Table 1–15. Stratix Clock Input Sources For Enhanced & Fast PLLs (Part 1 of 2)*

| Clock Input Pins | All Stratix Devices | | | | | | EP1S30, EP1S40, EP1S60 & EP1S80 Devices Only | | | | EP1S40, EP1S60 & EP1S80 Devices Only | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | PLL 1 (1) | PLL 2 (1) | PLL 3 (1) | PLL 4 (1) | PLL 5 (2) | PLL 6 (2) | PLL 7 (1) | PLL 8 (1) | PLL 9 (1) | PLL 10 (1) | PLL 11 (2) | PLL 12 (2) |
| `Clk0p/n` | ✓ | | | | | | ✓ (3) | | | | | |
| `Clk1p/n` | ✓ | | | | | | | | | | | |
| `Clk2p/n` | | ✓ | | | | | | ✓ (3) | | | | |
| `Clk3p/n` | | ✓ | | | | | | | | | | |
| `Clk4p/n` | | | | | | ✓ | | | | | | |
| `Clk5p/n` | | | | | | ✓ | | | | | | |
| `Clk6p/n` | | | | | | | | | | | | ✓ |
| `Clk7p/n` | | | | | | | | | | | | ✓ |
| `Clk8p/n` | | | ✓ | | | | | | ✓ (3) | | | |
| `Clk9p/n` | | | ✓ | | | | | | | | | |
| `Clk10p/n` | | | | ✓ | | | | | | ✓ (3) | | |
| `Clk11p/n` | | | | ✓ | | | | | | | | |
| `Clk12p/n` | | | | | | | | | | | ✓ | |
| `Clk13p/n` | | | | | | | | | | | ✓ | |
| `Clk14p/n` | | | | | ✓ | | | | | | | |
| `Clk15p/n` | | | | | ✓ | | | | | | | |
| `Fpll7clk` | | | | | | | ✓ | | | | | |
| `Fpll8clk` | | | | | | | | ✓ | | | | |
| `Fpll9clk` | | | | | | | | | ✓ | | | |
| `Fpll10clk` | | | | | | | | | | ✓ | | |

***Table 1–15. Stratix Clock Input Sources For Enhanced & Fast PLLs (Part 2 of 2)***

| Clock Input Pins | All Stratix Devices | | | | | | EP1S30, EP1S40, EP1S60 & EP1S80 Devices Only | | | | EP1S40, EP1S60 & EP1S80 Devices Only | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | PLL 1 *(1)* | PLL 2 *(1)* | PLL 3 *(1)* | PLL 4 *(1)* | PLL 5 *(2)* | PLL 6 *(2)* | PLL 7 *(1)* | PLL 8 *(1)* | PLL 9 *(1)* | PLL 10 *(1)* | PLL 11 *(2)* | PLL 12 *(2)* |
| Clock Feedback Input Pins | | | | | | | | | | | | |
| `Pll5_fbp/n` | | | | | ✓ | | | | | | | |
| `Pll6_fbp/n` | | | | | | ✓ | | | | | | |

***Notes to Table 1–15:***

(1) This is a fast PLL. The global or regional clocks in a fast PLL's quadrant can drive the fast PLL input. A pin or other PLL must drive the global or regional source. The source cannot be driven by internally generated logic before driving the fast PLL.

(2) This is an enhanced PLL.

(3) This clock is available, but its performance is not guaranteed. Contact Altera Applications for more information.

***Table 1–16. Stratix GX Clock Input Sources for Enhanced & Fast PLLs (Part 1 of 2)***

| Clock Input Pins | All Stratix GX Devices | | | | EP1SGX40 Devices Only | | | |
|---|---|---|---|---|---|---|---|---|
| | PLL 1 *(1)* | PLL 2 *(1)* | PLL 5 *(2)* | PLL 6 *(2)* | PLL 7 *(1)* | PLL 8 *(1)* | PLL 11 *(2)* | PLL 12 *(2)* |
| `CLK0p/n` | ✓ | | | | ✓ | | | |
| `CLK1p/n` | ✓ | | | | | | | |
| `CLK2p/n` | | ✓ | | | | ✓ | | |
| `CLK3p/n` | | ✓ | | | | | | |
| `CLK4p/n` | | | | ✓ | | | | |
| `CLK5p/n` | | | | ✓ | | | | |
| `CLK6p/n` | | | | *(3)* | | | | ✓ |
| `CLK7p/n` | | | | *(3)* | | | | ✓ |
| `CLK12p/n` | | | *(3)* | | | | ✓ | |
| `CLK13p/n` | | | *(3)* | | | | ✓ | |
| `CLK14p/n` | | | ✓ | | | | | |
| `CLK15p/n` | | | ✓ | | | | | |
| `FPLL0CLK` | | | | | ✓ | | | |
| `FPLL1CLK` | | | | | | ✓ | | |

**Table 1–16. Stratix GX Clock Input Sources for Enhanced & Fast PLLs (Part 2 of 2)**

| Clock Input Pins | All Stratix GX Devices | | | | EP1SGX40 Devices Only | | | |
|---|---|---|---|---|---|---|---|---|
| | PLL 1 (1) | PLL 2 (1) | PLL 5 (2) | PLL 6 (2) | PLL 7 (1) | PLL 8 (1) | PLL 11 (2) | PLL 12 (2) |
| Clock feedback input pins | | | | | | | | |
| `PLL5_FBp/n` | | | ✓ | | | | | |
| `PLL6_FBp/n` | | | | ✓ | | | | |

*Notes to Table 1–16:*

(1) This is a fast PLL. The global or regional clocks in a fast PLL's quadrant can drive the fast PLL input. A pin or other PLL must drive the global or regional source. The source cannot be driven by internally generated logic before driving the fast PLL.

(2) This is an enhanced PLL.

(3) This clock is available, but its performance is not guaranteed. Contact Altera Applications for more information.

## Clock Output Connections

Enhanced PLLs have outputs for two regional clock outputs and four global outputs. There is line sharing between clock pins, global and regional clock networks and all PLL outputs. Check Tables 1–17 and 1–19 and Figures 1–28 and 1–29 to make sure that the clocking scheme is valid. The Quartus II software automatically maps to regional and global clocks to avoid any restrictions. Enhanced PLLs 5 and 6 drive out to single-ended pins as shown in Table 1–17. PLLs 11 and 12 drive out to single-ended pins.

Designers can connect each fast PLL 1, 2, 3, or 4 outputs (*g*0, *l*0, and *l*1) to either a global or a regional clock. (PLLs 3 and 4 are not available on Stratix GX devices.) There is line sharing between clock pins, `FPLLCLK` pins, global and regional clock networks and all PLL outputs. Check Figures 1–28 and 1–29 to make sure that the clocking is valid. The Quartus II software will automatically map to regional and global clocks to avoid any restrictions.

Table 1–17 and 1–18 show the global and regional clocks that each PLL drives outputs to for Stratix and Stratix GX devices, respectively. Tables 1–19 and 1–20 show the global and regional clock network each of the CLK and FPLLCLK pins drive when bypassing the PLL.

**Table 1–17. Stratix Global & Regional Clock Output Line Sharing for Enhanced & Fast PLLs (Part 1 of 2)**

| Clock Network | All Devices | | | | | | EP1S30, EP1S40, EP1S60 & EP1S80 Devices Only | | | | EP1S40, EP1S60 & EP1S80 Devices Only | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | PLL 1 *(1)* | PLL 2 *(1)* | PLL 3 *(1)* | PLL 4 *(1)* | PLL 5 *(2)* | PLL 6 *(2)* | PLL 7 *(1)* | PLL 8 *(1)* | PLL 9 *(1)* | PLL 10 *(1)* | PLL 11 *(2)* | PLL 12 *(2)* |
| GCLK0 | ✓ | ✓ | | | | | ✓ | ✓ | | | | |
| GCLK1 | ✓ | ✓ | | | | | ✓ | ✓ | | | | |
| GCLK2 | ✓ | ✓ | | | | | ✓ | ✓ | | | | |
| GCLK3 | ✓ | ✓ | | | | | ✓ | ✓ | | | | |
| GCLK4 | | | | | | ✓ | | | | | | ✓ |
| GCLK5 | | | | | | ✓ | | | | | | ✓ |
| GCLK6 | | | | | | ✓ | | | | | | ✓ |
| GCLK7 | | | | | | ✓ | | | | | | ✓ |
| GCLK8 | | | ✓ | ✓ | | | | | ✓ | ✓ | | |
| GCLK9 | | | ✓ | ✓ | | | | | ✓ | ✓ | | |
| GCLK10 | | | ✓ | ✓ | | | | | ✓ | ✓ | | |
| GCLK11 | | | ✓ | ✓ | | | | | ✓ | ✓ | | |
| GCLK12 | | | | | ✓ | | | | | | ✓ | |
| GCLK13 | | | | | ✓ | | | | | | ✓ | |
| GCLK14 | | | | | ✓ | | | | | | ✓ | |
| GCLK15 | | | | | ✓ | | | | | | ✓ | |
| RCLK0 | ✓ | ✓ | | | | | ✓ | | | | | |
| RCLK1 | ✓ | ✓ | | | | | ✓ | | | | | |
| RCLK2 | ✓ | ✓ | | | | | | ✓ | | | | |
| RCLK3 | ✓ | ✓ | | | | | | ✓ | | | | |
| RCLK4 | | | | | | ✓ | | | | | | ✓ |
| RCLK5 | | | | | | ✓ | | | | | | ✓ |

*Table 1–17. Stratix Global & Regional Clock Output Line Sharing for Enhanced & Fast PLLs (Part 2 of 2)*

| Clock Network | All Devices | | | | | | EP1S30, EP1S40, EP1S60 & EP1S80 Devices Only | | | | EP1S40, EP1S60 & EP1S80 Devices Only | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | PLL 1 *(1)* | PLL 2 *(1)* | PLL 3 *(1)* | PLL 4 *(1)* | PLL 5 *(2)* | PLL 6 *(2)* | PLL 7 *(1)* | PLL 8 *(1)* | PLL 9 *(1)* | PLL 10 *(1)* | PLL 11 *(2)* | PLL 12 *(2)* |
| `RCLK6` | | | | | | ✓ | | | | | | ✓ |
| `RCLK7` | | | | | | ✓ | | | | | | ✓ |
| `RCLK8` | | | ✓ | ✓ | | | | | ✓ | | | |
| `RCLK9` | | | ✓ | ✓ | | | | | ✓ | | | |
| `RCLK10` | | | ✓ | ✓ | | | | | | ✓ | | |
| `RCLK11` | | | ✓ | ✓ | | | | | | ✓ | | |
| `RCLK12` | | | | | ✓ | | | | | | ✓ | |
| `RCLK13` | | | | | ✓ | | | | | | ✓ | |
| `RCLK14` | | | | | ✓ | | | | | | ✓ | |
| `RCLK15` | | | | | ✓ | | | | | | ✓ | |
| External Clock Output | | | | | | | | | | | | |
| `PLL5_OUT[3..0]p/n` | | | | | ✓ | | | | | | | |
| `PLL6_OUT[3..0]p/n` | | | | | | ✓ | | | | | | |
| `PLL11_OUT` *(3)* | | | | | | | | | | | ✓ | |
| `PLL12_OUT` *(4)* | | | | | | | | | | | | ✓ |

***Table 1–18. Stratix GX Global & Regional Clock Output Line Sharing for Enhanced & Fast PLLs (Part 1 of 2)***

| Clock Network | All Devices | | | | | EP1SGX40 Devices Only | | | |
|---|---|---|---|---|---|---|---|---|---|
| | PLL 1 *(1)* | PLL 2 *(1)* | HSSI | PLL 5 *(2)* | PLL 6 *(2)* | PLL 7 *(1)* | PLL 8 *(1)* | PLL 11 *(2)* | PLL 12 *(2)* |
| GCLK0 | ✓ | ✓ | | | | ✓ | ✓ | | |
| GCLK1 | ✓ | ✓ | | | | ✓ | ✓ | | |
| GCLK2 | ✓ | ✓ | | | | ✓ | ✓ | | |
| GCLK3 | ✓ | ✓ | | | | ✓ | ✓ | | |
| GCLK4 | | | | | ✓ | | | | ✓ |
| GCLK5 | | | | | ✓ | | | | ✓ |
| GCLK6 | | | | | ✓ | | | | ✓ |
| GCLK7 | | | | | ✓ | | | | ✓ |
| GCLK8 | | | ✓ | | | | | | |
| GCLK9 | | | ✓ | | | | | | |
| GCLK10 | | | ✓ | | | | | | |
| GCLK11 | | | ✓ | | | | | | |
| GCLK12 | | | | ✓ | | | | ✓ | |
| GCLK13 | | | | ✓ | | | | ✓ | |
| GCLK14 | | | | ✓ | | | | ✓ | |
| GCLK15 | | | | ✓ | | | | ✓ | |
| RCLK0 | ✓ | ✓ | | | | ✓ | | | |
| RCLK1 | ✓ | ✓ | | | | ✓ | | | |
| RCLK2 | ✓ | ✓ | | | | | ✓ | | |
| RCLK3 | ✓ | ✓ | | | | | ✓ | | |
| RCLK4 | | | | | ✓ | | | | ✓ |
| RCLK5 | | | | | ✓ | | | | ✓ |
| RCLK6 | | | | | ✓ | | | | ✓ |
| RCLK7 | | | | | ✓ | | | | ✓ |
| RCLK8 | | | ✓ | | | | | | |
| RCLK9 | | | ✓ | | | | | | |
| RCLK10 | | | ✓ | | | | | | |

**Table 1–18. Stratix GX Global & Regional Clock Output Line Sharing for Enhanced & Fast PLLs (Part 2 of 2)**

| Clock Network | All Devices | | | | | EP1SGX40 Devices Only | | | |
|---|---|---|---|---|---|---|---|---|---|
| | PLL 1 *(1)* | PLL 2 *(1)* | HSSI | PLL 5 *(2)* | PLL 6 *(2)* | PLL 7 *(1)* | PLL 8 *(1)* | PLL 11 *(2)* | PLL 12 *(2)* |
| `RCLK11` | | | ✓ | | | | | | |
| `RCLK12` | | | | ✓ | | | | ✓ | |
| `RCLK13` | | | | ✓ | | | | ✓ | |
| `RCLK14` | | | | ✓ | | | | ✓ | |
| `RCLK15` | | | | ✓ | | | | ✓ | |
| External Clock Output | | | | | | | | | |
| `PLL5_OUT[3..0]p/n` | | | | ✓ | | | | | |
| `PLL6_OUT[3..0]p/n` | | | | | ✓ | | | | |
| `PLL11_OUT` *(3)* | | | | | | | | | |
| `PLL12_OUT` *(4)* | | | | | | | | | |

*Notes to Table 1–18:*

(1) This is a fast PLL.

(2) This is an enhanced PLL.

(3) This pin is a tri-purpose pin; it can be an I/O pin, `CLK13n`, or used for PLL 11 output.

(4) This pin is a tri-purpose pin; it can be an I/O pin, `CLK7n`, or used for PLL 12 output.

**Table 1–19. Stratix CLK & FPLLCLK Input Pin Connections to Global & Regional Clock Networks** *Note (1)*

| Clock Network | CLK Pins | | | | | | | | | | | | | | | | FPLLCLK *(2)* | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 7 | 8 | 9 | 10 |
| `GCLK0` | ✓ | | | | | | | | | | | | | | | | ✓ | ✓ | | |
| `GCLK1` | | ✓ | | | | | | | | | | | | | | | ✓ | ✓ | | |
| `GCLK2` | | | ✓ | | | | | | | | | | | | | | ✓ | ✓ | | |
| `GCLK3` | | | | ✓ | | | | | | | | | | | | | ✓ | ✓ | | |
| `GCLK4` | | | | | ✓ | | | | | | | | | | | | | | | |
| `GCLK5` | | | | | | ✓ | | | | | | | | | | | | | | |
| `GCLK6` | | | | | | | ✓ | | | | | | | | | | | | | |
| `GCLK7` | | | | | | | | ✓ | | | | | | | | | | | | |

***Table 1–19. Stratix CLK & FPLLCLK Input Pin Connections to Global & Regional Clock Networks*** *Note (1)*

| Clock Network | CLK Pins | | | | | | | | | | | | | | | | FPLLCLK (2) | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 7 | 8 | 9 | 10 |
| `GCLK8` | | | | | | | | | ✓ | | | | | | | | | | ✓ | ✓ |
| `GCLK9` | | | | | | | | | | ✓ | | | | | | | | | ✓ | ✓ |
| `GCLK10` | | | | | | | | | | | ✓ | | | | | | | | ✓ | ✓ |
| `GCLK11` | | | | | | | | | | | | ✓ | | | | | | | ✓ | ✓ |
| `GCLK12` | | | | | | | | | | | | | ✓ | | | | | | | |
| `GCLK13` | | | | | | | | | | | | | | ✓ | | | | | | |
| `GCLK14` | | | | | | | | | | | | | | | ✓ | | | | | |
| `GCLK15` | | | | | | | | | | | | | | | | ✓ | | | | |
| `RCLK0` | ✓ | | | | | | | | | | | | | | | | ✓ | | | |
| `RCLK1` | | ✓ | | | | | | | | | | | | | | | ✓ | | | |
| `RCLK2` | | | ✓ | | | | | | | | | | | | | | | ✓ | | |
| `RCLK3` | | | | ✓ | | | | | | | | | | | | | | ✓ | | |
| `RCLK4` | | | | | ✓ | | | | | | | | | | | | | | | |
| `RCLK5` | | | | | | ✓ | | | | | | | | | | | | | | |
| `RCLK6` | | | | | | | ✓ | | | | | | | | | | | | | |
| `RCLK7` | | | | | | | | ✓ | | | | | | | | | | | | |
| `RCLK8` | | | | | | | | | ✓ | | | | | | | | | | ✓ | |
| `RCLK9` | | | | | | | | | | ✓ | | | | | | | | | ✓ | |
| `RCLK10` | | | | | | | | | | | ✓ | | | | | | | | | ✓ |
| `RCLK11` | | | | | | | | | | | | ✓ | | | | | | | | ✓ |
| `RCLK12` | | | | | | | | | | | | | ✓ | | | | | | | |
| `RCLK13` | | | | | | | | | | | | | | ✓ | | | | | | |
| `RCLK14` | | | | | | | | | | | | | | | ✓ | | | | | |
| `RCLK15` | | | | | | | | | | | | | | | | ✓ | | | | |

*Notes to Table 1–19:*

(1) The `CLK` and `FPLLCLK` pins cannot drive.

(2) The `FPLLCLK` pin is only available in EP1S80, EP1S60, EP1S40, and EP1S30 devices.

*Table 1–20. Stratix GX CLK & FPLLCLK Input Pin Connections to Global & Regional Clock Networks* Note (1)

| Clock Network | CLK Pins | | | | | | | | | | | | FPLLCLK (2) | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 12 | 13 | 14 | 15 | 7 | 8 |
| `GCLK0` | ✓ | | | | | | | | | | | | ✓ | ✓ |
| `GCLK1` | | ✓ | | | | | | | | | | | ✓ | ✓ |
| `GCLK2` | | | ✓ | | | | | | | | | | ✓ | ✓ |
| `GCLK3` | | | | ✓ | | | | | | | | | ✓ | ✓ |
| `GCLK4` | | | | | ✓ | | | | | | | | | |
| `GCLK5` | | | | | | ✓ | | | | | | | | |
| `GCLK6` | | | | | | | ✓ | | | | | | | |
| `GCLK7` | | | | | | | | ✓ | | | | | | |
| `GCLK8` | | | | | | | | | | | | | | |
| `GCLK9` | | | | | | | | | | | | | | |
| `GCLK10` | | | | | | | | | | | | | | |
| `GCLK11` | | | | | | | | | | | | | | |
| `GCLK12` | | | | | | | | | ✓ | | | | | |
| `GCLK13` | | | | | | | | | | ✓ | | | | |
| `GCLK14` | | | | | | | | | | | ✓ | | | |
| `GCLK15` | | | | | | | | | | | | ✓ | | |
| `RCLK0` | ✓ | | | | | | | | | | | | ✓ | |
| `RCLK1` | | ✓ | | | | | | | | | | | ✓ | |
| `RCLK2` | | | ✓ | | | | | | | | | | | ✓ |
| `RCLK3` | | | | ✓ | | | | | | | | | | ✓ |
| `RCLK4` | | | | | ✓ | | | | | | | | | |
| `RCLK5` | | | | | | ✓ | | | | | | | | |
| `RCLK6` | | | | | | | ✓ | | | | | | | |
| `RCLK7` | | | | | | | | ✓ | | | | | | |
| `RCLK8` | | | | | | | | | | | | | | |
| `RCLK9` | | | | | | | | | | | | | | |
| `RCLK10` | | | | | | | | | | | | | | |
| `RCLK11` | | | | | | | | | | | | | | |

***Table 1–20. Stratix GX CLK & FPLLCLK Input Pin Connections to Global & Regional Clock Networks*** *Note (1)*

| Clock Network | CLK Pins |  |  |  |  |  |  |  |  |  |  |  | FPLLCLK *(2)* |  |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
|  | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 12 | 13 | 14 | 15 | 7 | 8 |
| `RCLK12` |  |  |  |  |  |  |  |  | ✓ |  |  |  |  |  |
| `RCLK13` |  |  |  |  |  |  |  |  |  | ✓ |  |  |  |  |
| `RCLK14` |  |  |  |  |  |  |  |  |  |  | ✓ |  |  |  |
| `RCLK15` |  |  |  |  |  |  |  |  |  |  |  | ✓ |  |  |

***Notes to Table 1–20:***

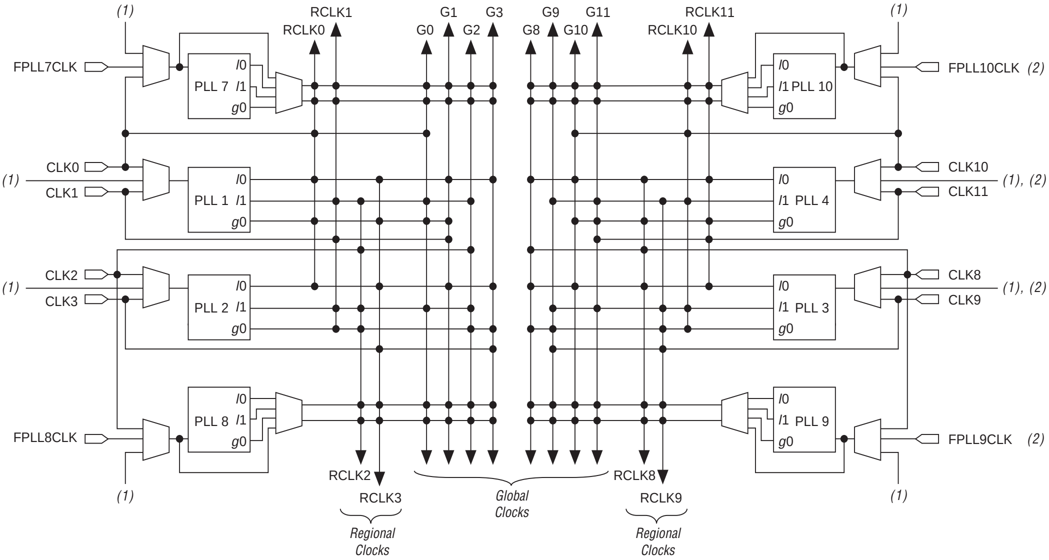
(1) The `CLK` and `FPLLCLK` pins cannot drive.

(2) The `FPLLCLK` pin is only available in EP1SGX40 devices.

The fast PLLs also drive high-speed SERDES clocks for differential I/O interfacing. For information on these `FPLLCLK` pins, see the Chapter 5, Using High-Speed Differential I/O Interfaces in Stratix Devices.

Figure 1–28 shows the global and regional clock input and output connections from the enhanced. Figure 1–28 shows graphically the same information as Tables 1–17 and 1–19 but with the added detail of where each specific PLL output port drives to.

*Figure 1–28. Global & Regional Clock Connections from Side Clock Pins & Fast PLL Outputs*



*Notes to Figures 1–28:*

(1) The global or regional clocks in a fast PLL's quadrant can drive the fast PLL input. A pin or other PLL must drive the global or regional source. The source cannot be driven by internally generated logic before driving the fast PLL.

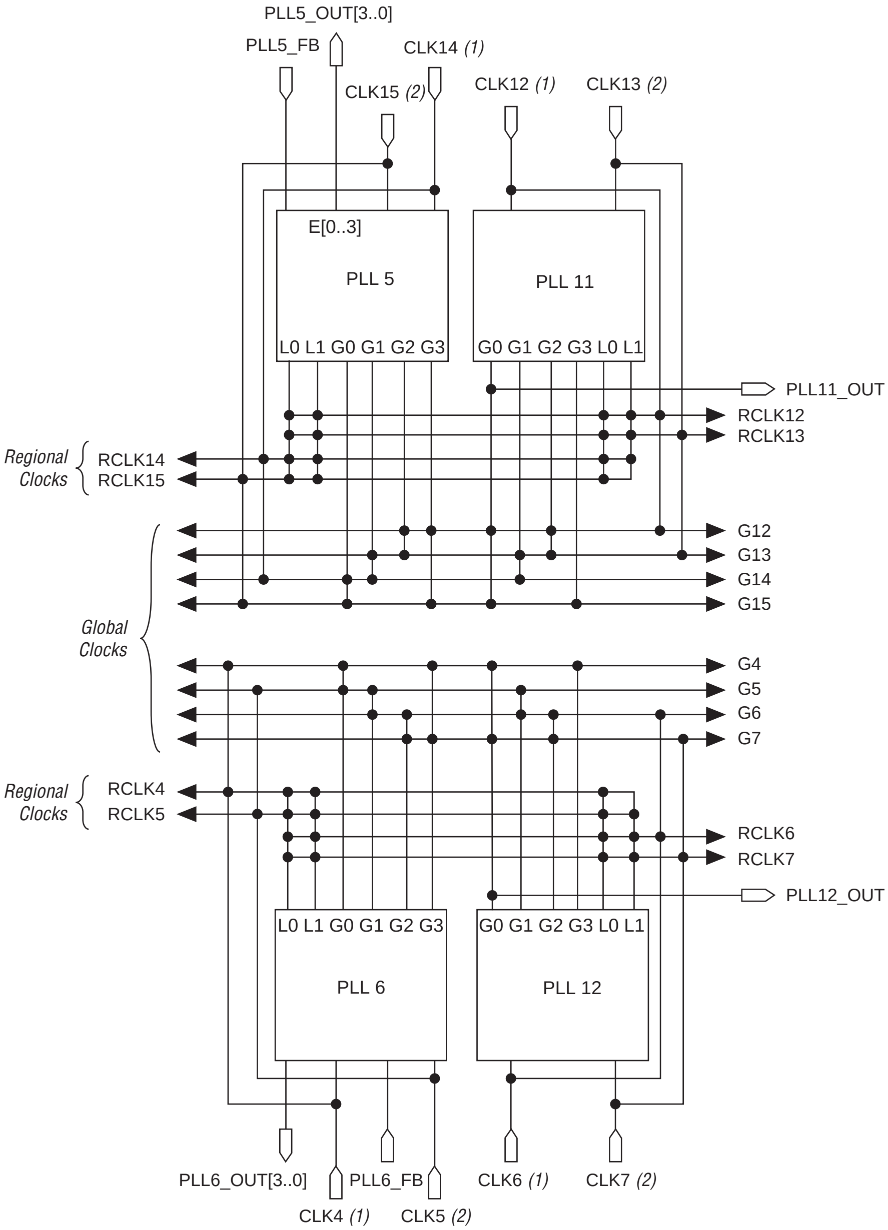
(2) PLLs 3, 4, 9, and 10 are used for the HSSI block in Stratix GX devices and are not available for this use.

When using a fast PLL to compensate for clock delays to drive logic on the chip, the clock delay from the input pin to the clock input port of the PLL will be compensated only if the clock is fed by the dedicated input pin closest to the PLL. If the fast PLL gets its input clock from a global or regional clock or from another dedicated clock pin, which does not directly feed the fast PLL, the clock signal is first routed onto a global clock network. The signal then drives into the PLL. In this case, the clock delay is not fully compensated and the delay compensation is equal to the clock delay from the dedicated clock pin closest to the PLL to the clock input port of the PLL.

For example, If you use `CLK0` to feed PLL 7, then the input clock path delay will not be fully compensated, but the input clock path delay will be fully compensated if `FPLL7CLK` feeds PLL 7.

Figure 1–29 shows the global and regional clock input and output connections from the fast PLLs. Figure 1–29 shows graphically the same information as Tables 1–17 and 1–19 but with the added detail of where each specific PLL output port drives to.

*Figure 1–29. Global & Regional Clock Connections from Top Clock Pins & Enhanced PLL Outputs*



*Notes to Figures 1–29:*

(1) `CLK4`, `CLK6`, `CLK12`, and `CLK14` feed the corresponding PLL’s `inclk0` port.

(2) `CLK5`, `CLK7`, `CLK13`, and `CLK15` feed the corresponding PLL’s `inclk1` port.

# Board Layout

The enhanced and fast PLL circuits in Stratix and Stratix GX devices contain analog components embedded in a digital device. These analog components have separate power and ground pins to minimize noise generated by the digital components. Both Stratix and Stratix GX enhanced and fast PLLs use separate `VCC` and ground pins to isolate circuitry and improve noise resistance.

## VCCA & GNDA

Each enhanced and fast PLL uses separate `VCC` and ground pin pairs for their analog circuitry. The analog circuit power and ground pin for each PLL is called `PLL`<*PLL number*>`_VCCA` and `PLL`<*PLL number*>`_GNDA`. Connect the `VCCA` power pin to a 1.5-V power supply, even if you do not use the PLL. Isolate the power connected to `VCCA` from the power to the rest of the Stratix and Stratix GX device or any other digital device on the board. You can use one of three different methods of isolating the `VCCA` pin: separate $V_{CCA}$ power planes, a partitioned $V_{CCA}$ island within the $V_{CCINT}$ plane, and thick $V_{CCA}$ traces.

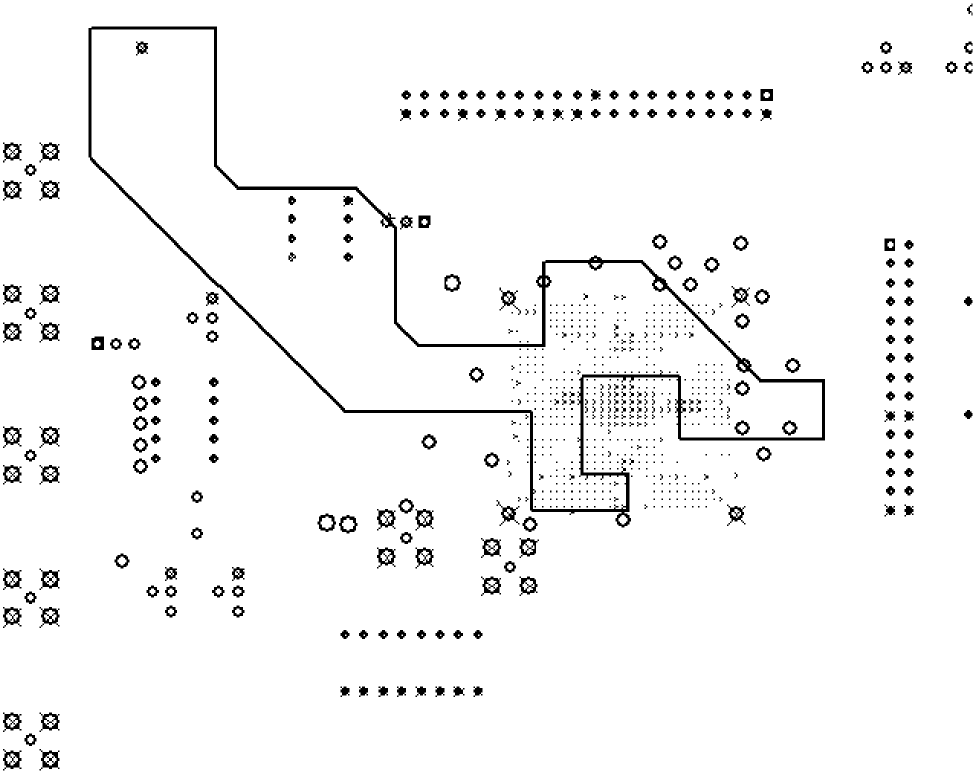
### Separate $V_{CCA}$ Power Plane

A mixed signal system is already partitioned into analog and digital sections, each with its own power planes on the board. To isolate the `VCCA` pin using a separate $V_{CCA}$ power plane, connect the `VCCA` pin to the analog 1.5-V power plane.

### Partitioned $V_{CCA}$ Island within $V_{CCINT}$ Plane

Fully digital systems do not have a separate analog power plane on the board. Since it is expensive to add new planes to the board, you can create islands for `VCCA_PLL`. Figure 9 shows an example board layout with an analog power island. The dielectric boundary that creates the island should be 25 mils thick. Figure 1–30 shows a partitioned plane within $V_{CCINT}$ for $V_{CCA}$.

*Figure 1–30. $V_{CCINT}$ Plane Partitioned for $V_{CCA}$ Island*

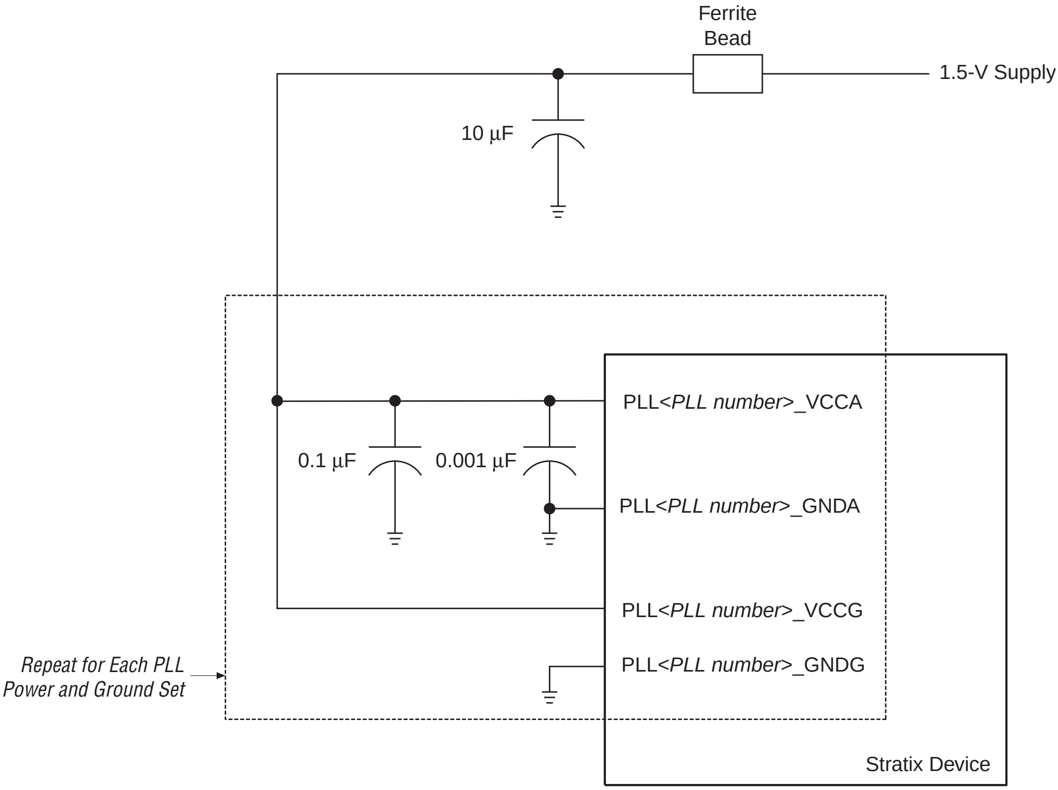


### Thick $V_{CCA}$ Trace

Due to board constraints, you may not be able to partition a $V_{CCA}$ island. Instead, run a thick trace from the power supply to each $V_{CCA}$ pin. The traces should be at least 20 mils thick.

In each of these three cases, you should filter each VCCA pin with a decoupling circuit shown in Figure 1–31. Place a ferrite bead that exhibits high impedance at frequencies of 50 MHz or higher and a 10-µF tantalum parallel capacitor where the power enters the board. Decouple each $V_{CCA}$ pin with a 0.1-µF and 0.001-µF parallel combination of ceramic capacitors located as close as possible to the Stratix or Stratix GX device. You can connect the `GNDA` pins directly to the same ground plane as the device's digital ground.

***Figure 1–31. PLL Power Schematic for Stratix or Stratix GX PLLs***



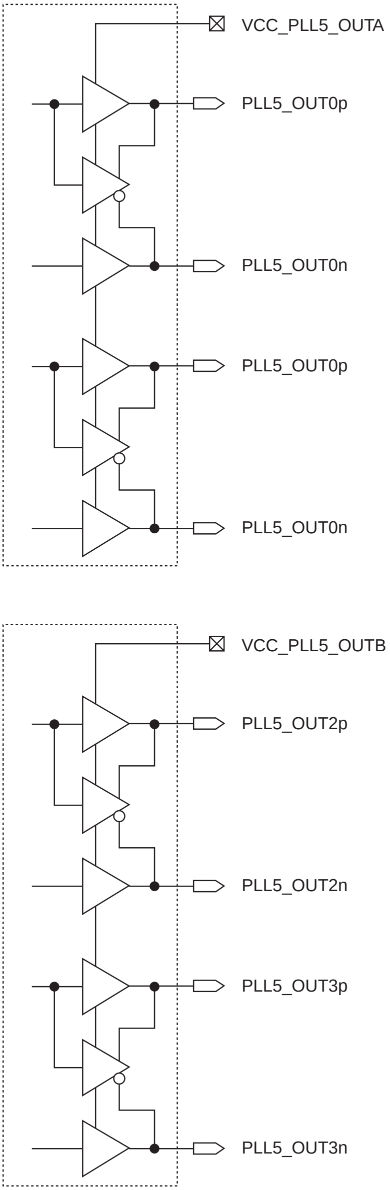
## VCCG & GNDG

The guard ring power and ground pins are called `PLL`<*PLL number*>`_VCCG` and `PLL`<*PLL number*>`_GNDG`. The guard ring isolates the PLL circuit from the rest of the device. Connect these guard ring $V_{CCG}$ pins to the quietest digital supply on the board. In most systems, this is the digital 1.5-V supply supplied to the device's $V_{CCINT}$ pins. Connect the $V_{CCG}$ pins to a power supply even if you do not use the PLL. When connecting the $V_{CCG}$ pins to $V_{CCINT}$, you do not need any filtering or isolation. You can connect the `GNDG` pins directly to the same ground plane as the device’s digital ground. See Figure 1–31.

## External Clock Output Power

Enhanced PLLs 5 and 6 also have isolated power pins for their dedicated external clock outputs (`VCC_PLL5_OUTA` and `VCC_PLL5_OUTB`, or `VCC_PLL6_OUTA` and `VCC_PLL6_OUTB`, respectively). PLLs 5 and 6 both have two banks of outputs. Each bank is powered by a unique output power, `OUTA` or `OUTB`, as illustrated in Figure 1–32. These outputs can by powered by 3.3, 2.5, 1.8, or 1.5 V depending on the I/O standard for the clock output in the A or B groups.

*Figure 1–32. External Clock Output Pin Association to Output Power* *Note (1)*

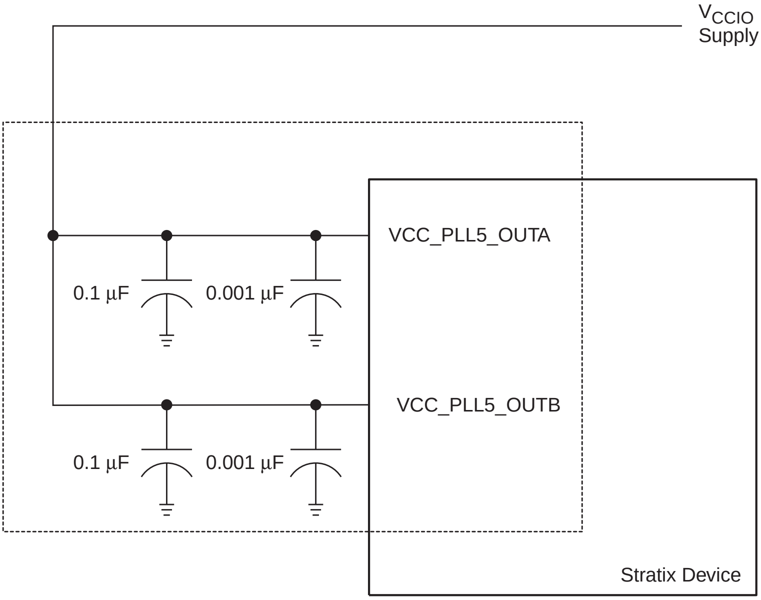


*Note to Figure 1–32:*

(1) These pins apply to PLL 5. The figure for PLL 6 is similar, except that the pin names begin with the prefix `PLL6` instead of `PLL5`.

Filter each isolated power pin with a decoupling circuit shown in Figure 1–33. Decouple the isolated power pins with a 0.1-µF and a 0.001-µF parallel combination of ceramic capacitors located as close as possible to the Stratix device.

*Figure 1–33. Stratix PLL External Clock Output Power Ball Connections* *Note (1)*



*Note to Figure 1–33:*

(1) Figure 1–33 also applies to `VCC_PLL6_OUTA/B`.

## Guidelines

Use the following guidelines for optimal jitter performance on the external clock outputs from enhanced PLLs 5 and 6. If all outputs are running at the same frequency, these guidelines are not necessary to improve performance.

- When driving two or more clock outputs from PLL 5 or 6, separate the outputs into the two groups shown in Figure 1–31. For example, if you are driving 100- and 200-MHz clock outputs off-chip from PLL 5, place one output on `PLL5_OUT0p` (powered by `VCC_PLL5_OUTA`) and the other output on `PLL5_OUT2p` (powered by `VCC_PLL5_OUTB`). Since the output buffers are powered by different pins, they are less susceptible to bimodal jitter. Bimodal jitter is a deterministic jitter not caused by the PLL but rather by coincident edges of clock outputs that are multiples of each other.
- Use phase shift to ensure edges are not coincident on all the clock outputs.
- Use phase shift (as opposed to time delay shift) to skew clock edges with respect to each other for best jitter performance.
- If you cannot drive multiple clocks of different frequencies and phase shifts or isolate banks, you should control the drive capability on the lower frequency clock. Reducing how much current the output buffer has to supply can reduce the noise. Minimize capacitive load on the slower frequency output and configure the output buffer to drive slow slew rate and lower current strength. The higher frequency output should have an improved performance, but this may degrade the performance of your lower frequency clock output.

## Specifications

Table 1–21 and 1–22 describe the Stratix and Stratix GX device enhanced PLL specifications.

*Table 1–21. Enhanced PLL Specifications for -5 & -6 Speed Grades*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{IN}$ | Input clock frequency | 3 *(1)* | | 462 | MHz |
| $f_{INDUTY}$ | Input clock duty cycle | 40 | | 60 | % |
| $f_{EINDUTY}$ | External feedback clock input duty cycle | 40 | | 60 | % |
| $t_{INJITTER}$ | Input clock cycle-to-cycle jitter | | | ±200 | ps |
| $t_{EINJITTER}$ | External feedback clock cycle-to-cycle jitter | | | ±200 | ps |
| $t_{FCOMP}$ | External feedback clock compensation time *(2)* | | | 6 | ns |
| $f_{OUT}$ | PLL output frequency | 0.6 | | 462 | MHz |
| $t_{OUTDUTY}$ | Duty cycle for external clock output (when set to 50%) | 45 | | 55 | % |

*Table 1–21. Enhanced PLL Specifications for -5 & -6 Speed Grades*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{JITTER}$ | Cycle-to-cycle jitter for external or internal global or regional clock output *(3)* | | | ±100 ps or ±15 mUI, whichever is higher | ps or mUI |
| $t_{CONFIG5,6}$ | Time required to reconfigure the scan chains for PLLs 5 and 6 | | | $289/f_{SCANCLK}$ | |
| $t_{CONFIG11,12}$ | Time required to reconfigure the scan chains for PLLs 11 and 12 | | | $193/f_{SCANCLK}$ | |
| $t_{SCANCLK}$ | `scanclk` frequency *(4)* | | | 22 | MHz |
| $t_{DLOCK}$ | Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) *(5)* | *(6)* | | 100 | µs |
| $t_{LOCK}$ | Time required to lock from end of device configuration | 10 | | 1,000 | µs |
| $f_{VCO}$ | PLL internal VCO operating range | 300 | | 800 | MHz |
| $t_{LSKEW}$ | Clock skew between two external clock outputs driven by the same counter | | ±50 | | ps |
| $t_{SKEW}$ | Clock skew between two external clock outputs driven by the different counters with the same settings | | ±75 | | ps |
| $f_{SS}$ | Spread spectrum modulation frequency | 30 | | 150 | kHz |
| % spread | Percentage spread for spread spectrum frequency *(7)* | 0 | 0.5 | | % |

*Table 1–22. Enhanced PLL Specifications for -7 Speed Grade*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{IN}$ | Input clock frequency | 3 *(1)* | | 462 | MHz |
| $f_{INDUTY}$ | Input clock duty cycle | 40 | | 60 | % |
| $f_{EINDUTY}$ | External feedback clock input duty cycle | 40 | | 60 | % |
| $t_{INJITTER}$ | Input clock cycle-to-cycle jitter | | | ±200 | ps |
| $t_{EINJITTER}$ | External feedback clock cycle-to-cycle jitter | | | ±200 | ps |
| $t_{FCOMP}$ | External feedback clock compensation time *(2)* | | | 6 | ns |
| $f_{OUT}$ | PLL output frequency | 0.6 | | 462 | MHz |
| $t_{OUTDUTY}$ | Duty cycle for external clock output (when set to 50%) | 45 | | 55 | % |

| *Table 1–22. Enhanced PLL Specifications for -7 Speed Grade* | | | | | |
|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min** | **Typ** | **Max** | **Unit** |
| $t_{JITTER}$ | Cycle-to-cycle jitter for external or internal global or regional clock output *(3)* | | | ±100 ps or ±15 mUI, whichever is higher | ps or mUI |
| $t_{CONFIG5,6}$ | Time required to reconfigure the scan chains for PLLs 5 and 6 | | | $289/f_{SCANCLK}$ | |
| $t_{CONFIG11,12}$ | Time required to reconfigure the scan chains for PLLs 11 and 12 | | | $193/f_{SCANCLK}$ | |
| $t_{SCANCLK}$ | `scanclk` frequency *(4)* | | | 22 | MHz |
| $t_{DLOCK}$ | Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) *(5)* | *(6)* | | 100 | μs |
| $t_{LOCK}$ | Time required to lock from end of device configuration | 10 | | 1,000 | μs |
| $f_{VCO}$ | PLL internal VCO operating range | 300 | | 600 | MHz |
| $t_{LSKEW}$ | Clock skew between two external clock outputs driven by the same counter | | ±50 | | ps |
| $t_{SKEW}$ | Clock skew between two external clock outputs driven by the different counters with the same settings | | ±75 | | ps |
| $f_{SS}$ | Spread spectrum modulation frequency | 30 | | 150 | kHz |
| % spread | Percentage spread for spread spectrum frequency *(7)* | 0 | 0.5 | | % |

***Notes to Table 1–21 and 1–22:***

(1) The minimum input clock frequency to the PFD ($f_{IN}/N$) must be at least 3 Mhz for Stratix and Stratix GX device enhanced PLLs.

(2) $t_{FCOMP}$ can also equal 50% of the input clock period multiplied by the pre-scale divider *n* (whichever is less).

(3) Actual jitter performance may vary based on the system configuration.

(4) This parameter is timing analyzed by the Quartus II software because the `scanclk` and `scandata` ports can be driven by the logic array.

(5) Total required time to reconfigure and lock is equal to $t_{DLOCK} + t_{CONFIG}$. If only post-scale counters and delays are changed, then $t_{DLOCK}$ is equal to 0.

(6) Lock time is a function of PLL configuration and may be significantly faster depending on bandwidth settings or feedback counter change increment.

(7) Exact, user-controllable value depends on the PLL settings.

Table 1–23 and 1–24 describe the Stratix and Stratix GX device fast PLL specifications.

**Table 1–23. Fast PLL Specifications for -5 & -6 Speed Grades** *Note (1)*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $f_{IN}$ | `CLKIN` frequency (for *m* = 1) *(2), (3)* | 300 | 717 | MHz |
| | `CLKIN` frequency (for *m* = 2 to 19) | 300/*m* | 1,000/*m* | MHz |
| | `CLKIN` frequency (for *m* = 20 to 32) | 15 | 1,000/*m* | MHz |
| $f_{OUT}$ | Output frequency for internal global or regional clock *(4)* | 9.375 | 420 | MHz |
| $f_{OUT\_EXT}$ | Output frequency for external clock *(3)* | 9.375 | 717 | MHz |
| $f_{VCO}$ | VCO operating frequency | 300 | 1,000 | MHz |
| $t_{INDUTY}$ | `CLKIN` duty cycle | 40 | 60 | % |
| $t_{INJITTER}$ | Cycle-to-cycle jitter for `CLKIN` pin | | ±200 | ps |
| $t_{DUTY}$ | Duty cycle for `DFFIO` 1× `CLKOUT` pin *(5)* | 45 | 55 | % |
| $t_{JITTER}$ | Cycle-to-cycle jitter for DIFFIO clock out *(5)* | | ±80 | ps |
| | Cycle-to-cycle jitter for internal global or regional clock | | ±100 ps or ±15 mUI, whichever is higher | ps or mUI |
| $t_{LOCK}$ | Time required for PLL to acquire lock | 10 | 100 | µs |
| m | Multiplication factors for *m* counter *(6)* | 1 | 32 | Integer |
| *l*0, *l*1, *g*0 | Multiplication factors for *l*0, *l*1, and *g*0 counter *(6), (7)* | 1 | 32 | Integer |

**Table 1–24. Fast PLL Specifications for -7 Speed Grade** *Note (1)*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $f_{IN}$ | `CLKIN` frequency (for *m* = 1) *(2), (3)* | 300 | 460 | MHz |
| | `CLKIN` frequency (for *m* = 2 to 19) | 300/*m* | 700/*m* | MHz |
| | `CLKIN` frequency (for *m* = 20 to 32) | 15 | 700/*m* | MHz |
| $f_{OUT}$ | Output frequency for internal global or regional clock *(4)* | 9.375 | 420 | MHz |
| $f_{OUT\_EXT}$ | Output frequency for external clock *(3)* | 9.375 | 460 | MHz |
| $f_{VCO}$ | VCO operating frequency | 300 | 700 | MHz |
| $t_{INDUTY}$ | `CLKIN` duty cycle | 40 | 60 | % |
| $t_{INJITTER}$ | Cycle-to-cycle jitter for `CLKIN` pin | | ±200 | ps |

*Table 1–24. Fast PLL Specifications for -7 Speed Grade* *Note (1)*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{DUTY}$ | Duty cycle for `DFFIO` 1× `CLKOUT` pin *(5)* | 45 | 55 | % |
| $t_{JITTER}$ | Cycle-to-cycle jitter for DIFFIO clock out *(5)* | | ±80 | ps |
| | Cycle-to-cycle jitter for internal global or regional clock | | ±100 ps or ±15 mUI, whichever is higher | ps or mUI |
| $t_{LOCK}$ | Time required for PLL to acquire lock | 10 | 100 | µs |
| m | Multiplication factors for *m* counter *(6)* | 1 | 32 | Integer |
| *l*0, *l*1, *g*0 | Multiplication factors for *l*0, *l*1, and *g*0 counter *(6)*, *(7)* | 1 | 32 | Integer |

***Notes to Table 1–23 and Table 1–24:***

(1) PLLs 3, 4, 9, and 10 on Stratix GX devices are only used for the HSSI block. These PLLs are not available for general-purpose programming.

(2) PLLs 7, 8, 9, and 10 support up to 717-MHz input clock frequency on `FPLL[7..10]clk` pins using differential standards. PLLs 1, 2, 3, and 4 support up to 717-MHz input clock frequency on the `CLK0`, `CLK2`, `CLK9`, and `CLK11` pins using differential standards. All other clock inputs support 462 MHz using differential standards.

(3) PLLs 7, 8, 9, and 10 in the EP1S80 device support up to 462-MHz input and output.

(4) When using the SERDES, high-speed differential I/O mode supports a maximum output frequency of 210 MHz to the global or regional clocks (i.e., the maximum data rate 840 Mbps divided by the smallest SERDES J factor of 4).

(5) This parameter is for high-speed differential I/O mode only.

(6) These counters have a maximum of 32 if programmed for 50/50 duty cycle. Otherwise, they have a maximum of 16.

(7) High-speed differential I/O mode supports $W = 1$ to 16 and $J = 4, 7, 8$, or 10.

## Conclusion

Stratix and Stratix GX device enhanced PLLs provide designers with complete control of their clocks and system timing. These PLLs are capable of offering flexible system level clock management that was previously only available in discrete PLL devices. The embedded PLLs meet and exceed the features offered by these high-end discrete devices, reducing the need for other timing devices in the system.

# Section II. Memory

This section provides information on the TriMatrix Embedded Memory blocks internal to Stratix devices and the supported external memory interfaces.

It contains the following chapters:

- Chapter 2. QDR SRAM Controller Reference Design for Stratix & Stratix GX Devices
- Chapter 3. Using TriMatrix Embedded Memory Blocks in Stratix & Stratix GX Devices

## Revision History

The table below shows the revision history for Chapters 2 and 3.

| Chapter(s) | Date / Version | Changes Made |
|---|---|---|
| 2 | April 2003<br>v1.0 | Added document to the Stratix Device Handbook. |
| 3 | April 2003<br>v1.0 | Added document to the Stratix Device Handbook. |

# 2. QDR SRAM Controller Reference Design for Stratix & Stratix GX Devices

S52002-1.0

Chapter 2, QDR SRAM Controller Reference Design for Stratix & Stratix GX Devices replaces *AN 211: QDR SRAM Controller Reference Design for Stratix & Stratix GX Devices*.

## Introduction

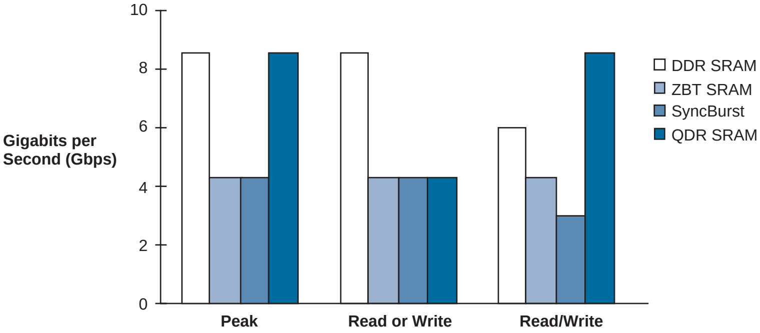
The explosive growth of the Internet has increased the demand for high-speed data communications systems that require fast processors and high-speed interfaces to peripheral components. While the processors in these systems have improved in performance, SRAM performance has not kept pace. New SRAM architectures are evolving to support the high-throughput requirements of current systems. One such architecture is quad data rate (QDR) SRAM, which provides more than four times the bandwidth of other SRAM architectures.

Most existing SRAM solutions are designed for PCs and have interfaces that move data efficiently for long bursts of reads or writes. In contrast, most communications applications require data transfer between the SRAM and the memory controller that alternates between read and write cycles. Devices with bidirectional interfaces, such as standard synchronous pipelined SRAM devices, do not perform well in these applications.

The QDR Consortium, comprised of Cypress Semiconductor, Hitachi, Integrated Device Technology, Inc., Micron Technology, NEC, and Samsung, designed the QDR SRAM architecture for high-performance communications systems such as routers and asynchronous transfer mode (ATM) switches. QDR SRAM devices, which can transfer four words per clock cycle, fulfill the requirements facing next-generation communications system designers. QDR SRAM devices provide concurrent reads and writes, zero latency, and increased data throughput, allowing simultaneous access to the same address location. Their innovative architecture allows them to outperform other SRAM devices by up to four times in networking applications, where reads and writes are balanced, as shown in Figure 2–1.

This application note provides an overview of QDR SRAM and outlines the advantages of using Stratix™ and Stratix GX devices to interface to QDR SRAM devices. Additionally, this document describes the functionality of the QDR SRAM controller reference design for Stratix devices, and explains how to synthesize, place-and-route, and simulate the reference design. The reference design allows communication system designers to implement a QDR SRAM interface in Stratix and Stratix GX devices at clock speeds of up to 167 MHz.

***Figure 2–1. SRAM Memory Architecture Performance Comparison*** *Note (1)*



*Note to Figure 2–1:*

(1) Figure 2–1 compares the performance of QDR SRAM devices versus other SRAM architectures such as double data rate (DDR), zero-bus turnaround (ZBT), and SyncBurst SRAM. This comparison assumes a 125-MHz clock speed for each memory architecture.

For more information on QDR SRAM devices, go to www.qdrsram.com.

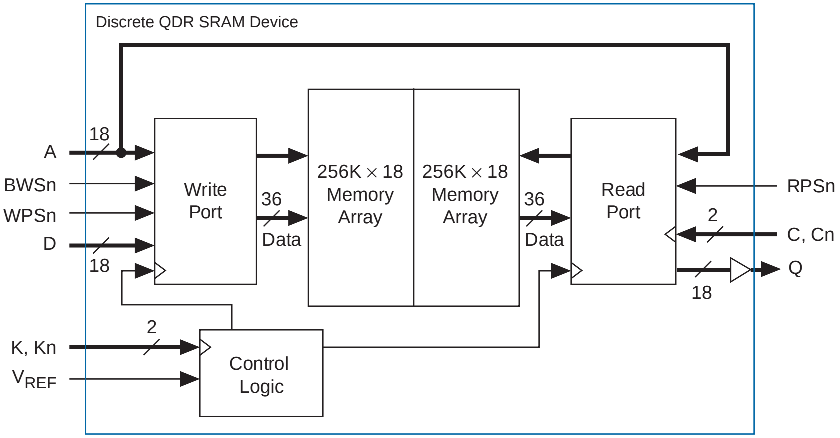
# QDR SRAM Functional Description

The following features distinguish QDR SRAM devices from other SRAM devices:

- Separate write data (`D`) and read data (`Q`) ports that support simultaneous reads and writes and allow back-to-back transactions without the contention issues that can occur when using a single bidirectional data bus
- A shared address bus that alternately carries the read and write addresses
- A memory core made up of multiple SRAM arrays, permitting double data rate (DDR) access and a transfer rate of up to four words on every clock cycle

Figure 2–2 shows a block diagram of the QDR SRAM burst-of-2 architecture.

*Figure 2–2. QDR SRAM Burst-of-2 Architecture*



## QDR SRAM Interface Signals

This section provides a description of the clock, control, address, and data signals on a QDR SRAM device, which is necessary to understand the functionality of the device.

### *Clock Signals*

QDR SRAM devices have two pairs of clocks: `K` and `Kn`, and `C` and `Cn`. The positive input clock, `K`, is the logical complement of the negative input clock, `Kn`. Similarly, the positive output clock, `C`, and the negative output clock, `Cn`, are complements. The QDR SRAM device uses the `K` and `Kn` clocks for write accesses and the `C` and `Cn` clocks for read accesses. QDR SRAM devices also have a single-clock mode, where the `K` and `Kn` clocks are used for both reads and writes. In this mode, the `C` and `Cn` clocks are tied to the supply voltage $V_{DD}$.

### *Control Signals*

QDR SRAM devices use two control signals, write port select (`WPSn`) and read port select (`RPSn`), to control write and read operations, respectively. A third control signal, byte write select (`BWSn`), writes only one byte of data at a time, if necessary.

### *Address Signals*

QDR SRAM devices use one address bus (`A`) for both read and write addresses.

### *Data Signals*

QDR SRAM devices use two unidirectional data buses, one for writes (`D`) and one for reads (`Q`).

## QDR SRAM Functionality

QDR SRAM devices have a two-word or four-word burst capability. The burst metric signifies the number of data words that are read or written on a single access; however, both types of QDR SRAM devices provide the same overall bandwidth at a given clock speed.

### *Burst-of-2 QDR SRAM*

Burst-of-2 QDR SRAM devices support two-word data transfers on all write and read transactions, requiring a relatively simple controller implementation. The sections below outline the basic burst-of-2 functionality for write-only, read-only, and combined read/write operations.

#### Write Cycle

On the rising edge of the `K` clock, the QDR SRAM device latches the control signals `WPSn` and `BWSn` and the lower data word on `D`. On the rising edge of the `Kn` clock, the QDR SRAM device latches the write address on `A` and the upper data word on `D`, thus completing a write cycle.

#### Read Cycle

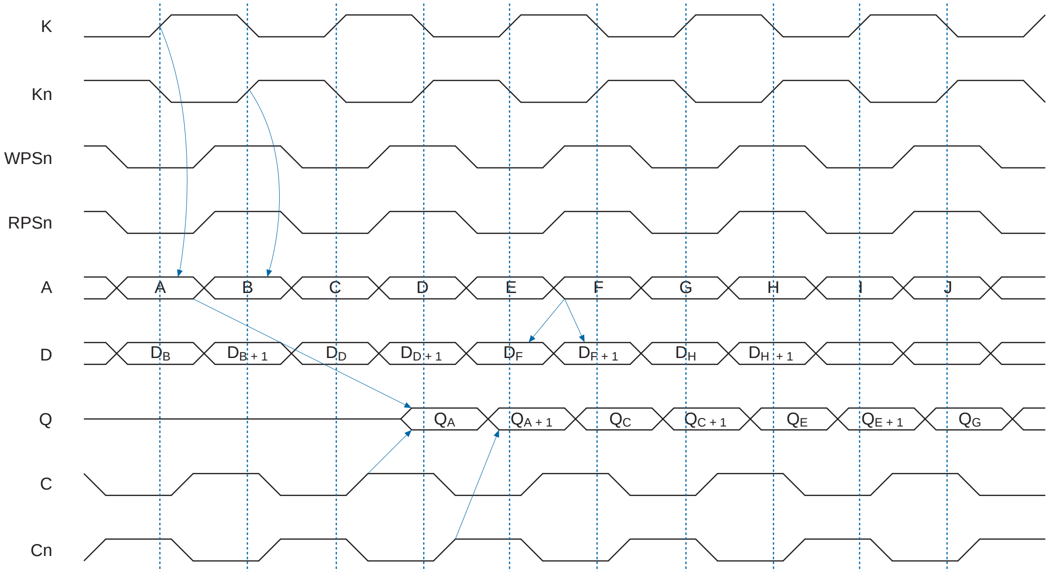
On the rising edge of the `K` clock, the QDR SRAM device latches the control signal `RPSn` and the read address `A`. After a one-clock-cycle latency, the rising edge of `C` clocks out the lower data word at address `A` onto the `Q` bus. The next rising edge of `Cn` clocks out the upper data word, thus completing a read cycle. Single-clock mode uses `K` and `Kn` clocks for both reads and writes. See "QDR SRAM Device Clock Modes" on page 2–18 for more information.

#### Read/Write Cycle

Independent read and write data paths, along with the cycle-shared address bus, allow read and write operations to occur in the same clock cycle. Performing concurrent reads and writes does not change the functionality of either transaction. If a read request occurs simultaneously with a write request at the same address, the data on `D` is forwarded to `Q`; therefore, latency is not required to access valid data.

Figure 2–3 shows the burst-of-2 timing diagram for reads and writes.

*Figure 2–3. Burst-of-2 Timing Diagram*



### Burst-of-4 QDR SRAM Devices

Burst-of-4 QDR SRAM devices support four-word data transfers on all writes and reads, which reduces address bus activity; however, the control circuitry needed to interface to burst-of-4 QDR SRAM devices is more complicated than control circuitry for burst-of-2 QDR SRAM devices. The following sections outline the basic burst-of-4 functionality for writes, reads, and read/write operations.

#### Write Cycle

On the rising edge of the `K` clock, the QDR SRAM device latches the control signals `WPSn` and `BWSn` and the write address `A`. On the following `K` clock rise, the QDR SRAM device latches the first data word on `D`. On the next `Kn` clock rise, the second data word is latched. The third and fourth words are latched in on the subsequent `K` and `Kn` clock rises, respectively, thus completing a write cycle.

#### Read Cycle

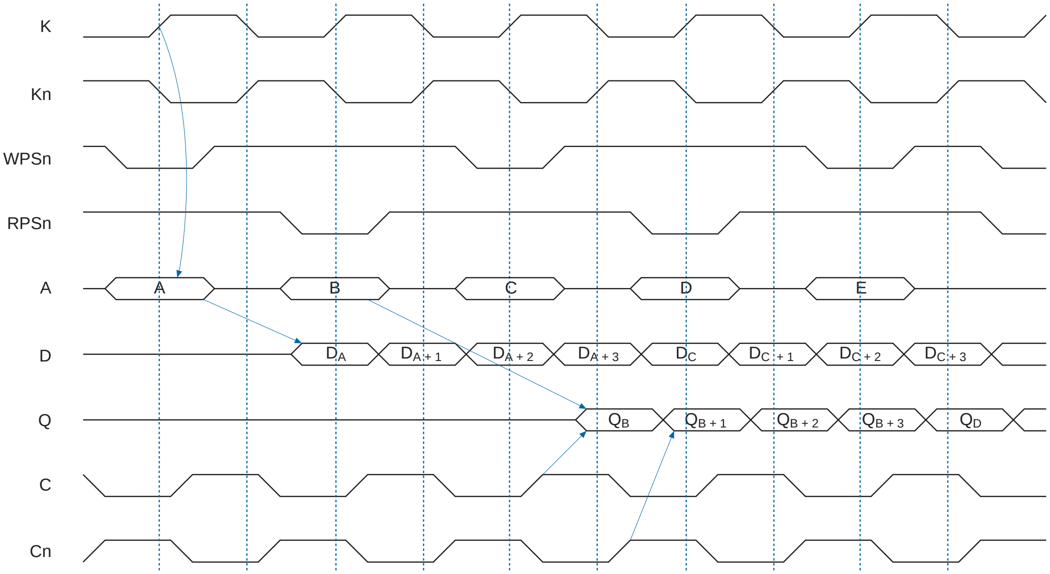
On the rising edge of the `K` clock, the QDR SRAM device latches the control signal `RPSn` and the read address `A`. After a one-clock-cycle latency, the rising edge of `C` clocks out the first data word at address `A` onto the `Q` bus. The next rising edge of `Cn` clocks out the second data word. The subsequent `C` and `Cn` clock rises clock out the third and fourth words, respectively, thus completing a read cycle. Single-clock mode uses the `K` and `Kn` clocks for both reads and writes. See "QDR SRAM Device Clock Modes" on page 2–18 for more information.

### Read/Write Cycle

The independent read and write data paths and the cycle-shared address bus allow read and write operations to occur on subsequent clock cycles. Performing concurrent read and writes does not change the functionality of either transaction. If a read request occurs simultaneously with a write request at the same address, the data on `D` is forwarded to `Q`; therefore, latency is not required to access valid data.

Figure 2–4 shows the burst-of-4 timing diagram for reads and writes.

*Figure 2–4. Burst-of-4 Timing Diagram*



## QDRII SRAM

The QDR Consortium has announced the QDRII architecture specification, designed for operation at clock speeds of up to 333 MHz. QDRII SRAM devices incorporate second-generation improvements in power consumption, packaging, and timing characteristics. These additional features increase the ease of system design and enable QDRII to become the memory architecture of choice for 10-gigabit and 40-gigabit networking systems.

For more information on QDRII, visit **www.qdrsram.com**.

QDRII SRAM device timing requirements are not as strict as QDR SRAM device timing requirements for a given clock speed. Therefore, because Stratix and Stratix GX devices support 167-MHz QDR SRAM devices, they can easily meet the timing requirements for interfacing with 167-MHz QDRII SRAM devices. Stratix and Stratix GX devices can also interface with QDRII SRAM devices at higher clock speeds.

## Controller Implementation: Stratix Advantages

When using QDR SRAM devices in a system, a memory controller generates all of the signals needed for the QDR SRAM device and serves as the interface between the QDR SRAM device and the rest of the system. Altera® Stratix and Stratix GX devices have been designed to interface at high speeds with memories such as QDR SRAM. These advantages allow Stratix and Stratix GX devices to interface with QDR SRAM devices at clock speeds of up to 166.67 MHz (at a total bandwidth of 12 gigabits per second (Gbps)), making them an ideal solution for memory-intensive applications. Stratix and Stratix GX devices offer the following features to interface with QDR SRAM devices:

- DDR I/O registers provide built-in functionality that simplifies the task of interfacing to QDR SRAM devices.
- Stratix and Stratix GX I/O buffers, which are compliant with the HSTL I/O standard, enable fast data transfers to QDR SRAM devices.
- On-chip termination resistors using the Terminator™ technology eliminate the need for complicated board termination schemes.
- High-density Stratix and Stratix GX devices provide up to 79,040 logic elements (LEs) that can be utilized for custom logic connecting to the memory controller.

### *HSTL I/O Standard*

QDR SRAM device pins use the HSTL I/O standard, which is fully supported in Stratix and Stratix GX devices at 333 megabits per second (Mbps) switching rates and beyond.

For more details, see Chapter 4, Using Selectable I/O Standards in Stratix & Stratix GX Devices.

The HSTL I/O standard is used for applications designed to operate in the 0.0- to 1.5-V HSTL logic switching range. This standard defines single ended input and output specifications for all HSTL compliant digital integrated circuits. The single-ended input standard specifies an input voltage range of $-0.3\text{ V} \leq V_I \leq V_{CCIO} + 0.3\text{ V}$. The 1.5-V HSTL I/O standard in Stratix and Stratix GX devices is compatible with the 1.8-V HSTL I/O standard in APEX™ 20KE and APEX 20KC devices because the input and output voltage thresholds are compatible. Using the 1.5-V $V_{CCIO}$, HSTL requires a 0.75-V input reference voltage ($V_{REF}$) and a 0.75-V termination voltage ($V_{TT}$). Stratix and Stratix GX devices support both input and output levels with $V_{REF}$ and $V_{TT}$.

### *Terminator Technology*

Stratix and Stratix GX devices feature on-chip termination resistors that can implement the termination scheme required by the HSTL I/O standard.

See Chapter 4, Using Selectable I/O Standards in Stratix & Stratix GX Devices for more information on Terminator™ technology.

### *DDR I/O Registers*

The main advantage of QDR SRAM devices is their ability to be written to and read from simultaneously on both the rising and falling clock edges. This ability quadruples the throughput of the QDR SRAM device. To take advantage of this high throughput, the Altera QDR SRAM controller uses the advanced I/O elements (IOEs) in Stratix and Stratix GX devices. These structures allow the Stratix or Stratix GX device to receive and transmit data on both the positive and negative clock edges and to meet the strict timing requirements of QDR SRAM devices.

Refer to Section I, Stratix Device Family Data Sheet of the *Stratix Device Handbook, Volume 1*; the *Stratix GX Programmable Logic Device Family Data Sheet*; and Chapter 8, Double Data Rate I/O Signaling in Stratix & Stratix GX Devices for detailed descriptions of the DDR I/O feature.

## Reference Design Description

The Altera QDR SRAM controller reference design implements a QDR SRAM controller targeting an EP1S25F780C6 device. You can use this design as:

- A memory interface module that you can incorporate into a larger system-on-a-programmable-chip (SOPC) design
- An example that you can reference when targeting a different device in the Stratix or Stratix GX families

The reference design implements several optional pipeline registers in the core of the Stratix device. These registers allow the designer to place the controller's user interface signals on device pins for more straightforward simulation, while still maintaining 166.67-MHz operation for the standalone controller. In a typical system, however, custom logic is implemented in the logic array of the Stratix or Stratix GX device, and hence, the user interface signals feed the controller from within the device. In this case, Altera recommends that you remove the optional pipeline stages to reduce latency through the controller (see "Compile in the Quartus II Software" on page 2–25).

The reference design provides an interface to the Cypress CY7C1302V25-167 device, a 9-Mbyte, pipelined, burst-of-2 QDR SRAM device. You can implement controllers for larger QDR SRAM devices, burst-of-4 QDR SRAM devices, QDR SRAM devices from other vendors, QDRII SRAM devices, or a memory bank consisting of multiple QDR SRAM devices, with little or no changes to the reference design. You should fully verify any modifications to the reference design using your design tool flow.

## Controller Structure & Operation

Figure 2–5 shows a block diagram of the controller reference design.

*Figure 2–5. QDR SRAM Controller Reference Design Block Diagram*

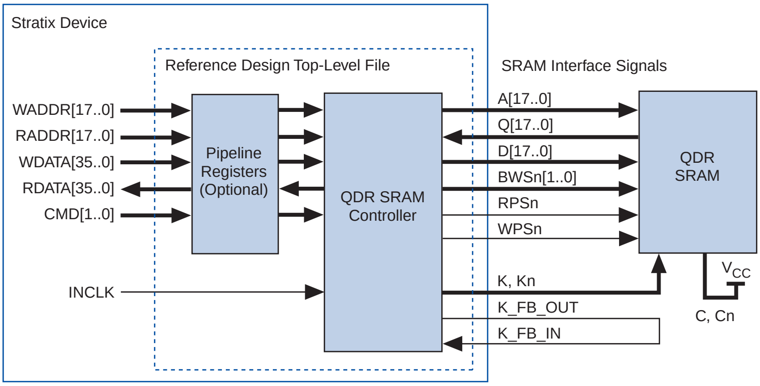


Table 2–1 describes the function of each controller pin on the QDR SRAM device interface.

*Table 2–1. QDR SRAM Device Interface Signals (Part 1 of 2)*

| Type | Direction | Name | Description |
|---|---|---|---|
| Clock | Output | `K, Kn` | `K` and `Kn` are output by the Stratix or Stratix GX device and are clock inputs to the QDR SRAM device. All transactions are initiated synchronously on the rising edge of `K` or `Kn`. These clocks are generated from the rising and falling edges of `WRITE_CLK_90`. |
| | | `K_FB_OUT` | `K_FB_OUT` is fed back to the controller as `K_FB_IN` to imitate the data flight times to and from the QDR SRAM device. (See Figure 2–9 on page 2–17 for more details on the clocking scheme). |
| | Input | `K_FB_IN` | The controller uses the `K_FB_IN` clock to generate `READ_CLK` for clocking in data from the QDR SRAM device. |
| Control | Output | `RPSn` | This active-low read port select signal is clocked out on the rising edge of `WRITE_CLK` and sampled by the QDR SRAM device on the rising edge of `K`. |
| | | `WPSn` | This active-low write port select signal is clocked out on the rising edge of `WRITE_CLK` and sampled by the QDR SRAM device on the rising edge of `K`. |
| | | `BWSn[1..0]` | This active-low byte write select signal is clocked out on the rising edge of `WRITE_CLK` and sampled by the QDR SRAM device on the rising edge of `K`. You can use this signal to individually select which bytes are written or read. For the reference design, both bytes are active on writes. You can add logic for individual byte writes if desired. |
| Address | Output | `A[17..0]` | The QDR SRAM device uses the same address signals for the read and write ports. The address inputs to the QDR SRAM device are clocked out of the controller using `WRITE_CLK` and sampled on the rising edge of `K` for reads and on the rising edge of `Kn` for writes. |
| Data | Input | `Q[17..0]` | Read data output from QDR SRAM. The QDR SRAM device can transfer two words during each clock cycle because the device outputs data on the rising edges of both `K` and `Kn`. On the subsequent falling edge of `READ_CLK`, the controller captures the QDR SRAM device's output data on the rising edge of `K`. The controller captures data output on the rising edge of `Kn` on the subsequent rising edge of `READ_CLK`. |
| | Output | `D[17..0]` | Write data input to the QDR SRAM device. The controller clocks data out on the rising and falling edges of `WRITE_CLK` and the QDR SRAM captures it on the next rising edges of `K` and `Kn`. Therefore, two words can be transferred to the QDR SRAM device during each clock cycle. |

*Table 2–1. QDR SRAM Device Interface Signals (Part 2 of 2)*

| Type | Direction | Name | Description |
|---|---|---|---|
| Reserved | Output | `reserved1_VCC` | Reserved pin driving high. |
| | | `reserved2_GND` | Reserved pin driving low. |
| | | `reserved3_GND` | Reserved pin driving low. |
| | | `reserved4_VCC` | Reserved pin driving high. |
| | | `reserved5_VCC` | Reserved pin driving high. |
| | | `reserved6_GND` | Reserved pin driving low. |

Table 2–2 shows the user interface signals for the controller. In a system implementation of the controller, these controller ports would typically be connected to custom logic within the Stratix or Stratix GX device.

*Table 2–2. User Interface Signals*

| Type | Direction | Name | Description |
|---|---|---|---|
| Clock | Input | `INCLK` | User input clock, which is used to generate `WRITE_CLK` and `WRITE_CLK_90`. This clock is 166.67 MHz in the reference design. |
| Control | Input | `CMD[1..0]` | User command input, which is sampled on the rising edge of `WRITE_CLK`. |
| Address | Input | `RADDR[17..0]`<br>`WADDR[17..0]` | User read and write address inputs, which are sampled on the rising edge of `WRITE_CLK`. |
| Data | Input | `WDATA[35..0]` | Data input for write operations, which is sampled on the rising edge of `WRITE_CLK`. |
| | Output | `RDATA[35..0]` | Data output from read operations; it is output from the controller on the rising edge of `READ_CLK`. |

Table 2–3 shows the commands accepted by the controller.

*Table 2–3. Controller Commands*

| Command | Code (CMD[1..0]) |
|---|---|
| Idle | `00` |
| Read | `01` |
| Write | `10` |
| Read/Write | `11` |

The Altera QDR SRAM controller is a synchronous interface. Because the read and write data paths for the controller are independent, the controller can perform reads and writes together or separately.

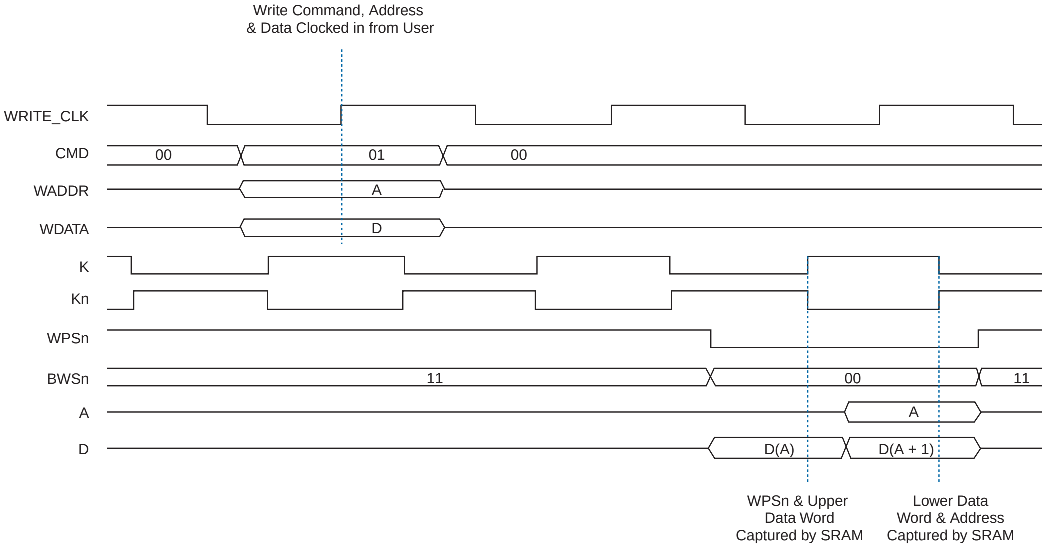
To use the controller, you must first provide an input clock (`INCLK`), which is fed into a fast phase-locked loop (PLL). Once the PLL has locked onto the input clock signal, it generates two clocks for the controller: `WRITE_CLK` and `WRITE_CLK_90`, a 90-degree-phase-shifted version of `WRITE_CLK`. A second fast PLL generates `READ_CLK`. For more information, see "Clock Generation" on page 2–16.

At the rising edge of `WRITE_CLK`, the controller should receive an idle, read, write, or read/write two-bit command, as shown in Table 2–3 on page 2–11. The controller should receive the appropriate read address (`RADDR`) simultaneously with a read or read/write command. Similarly, the controller should receive the write address (`WADDR`) and write data (`WDATA`) simultaneously with a write or read/write command.

At the QDR SRAM side of the controller, the DDR I/O registers output data, address, and control signals as well as the `K` and `Kn` clocks, which are generated using `WRITE_CLK_90`. `WRITE_CLK_90` is also used to output another clock, `K_FB_OUT`, which is fed back to the controller as `K_FB_IN`. `K_FB_IN` is sent to a PLL, which generates `READ_CLK`.

For write operations, the upper data word (`D`) is output and the write port select (`WPSn`) and byte write select (`BWSn`) signals are asserted on the rising edge of `WRITE_CLK`. The QDR SRAM device captures these signals on the rising edge of `K`. On the falling edge of `WRITE_CLK`, the address (`A`) and the lower data word are sent to the QDR SRAM device. These signals are captured on the rising edge of `Kn`. Figure 2–6 shows the functionality of the controller for write operations.

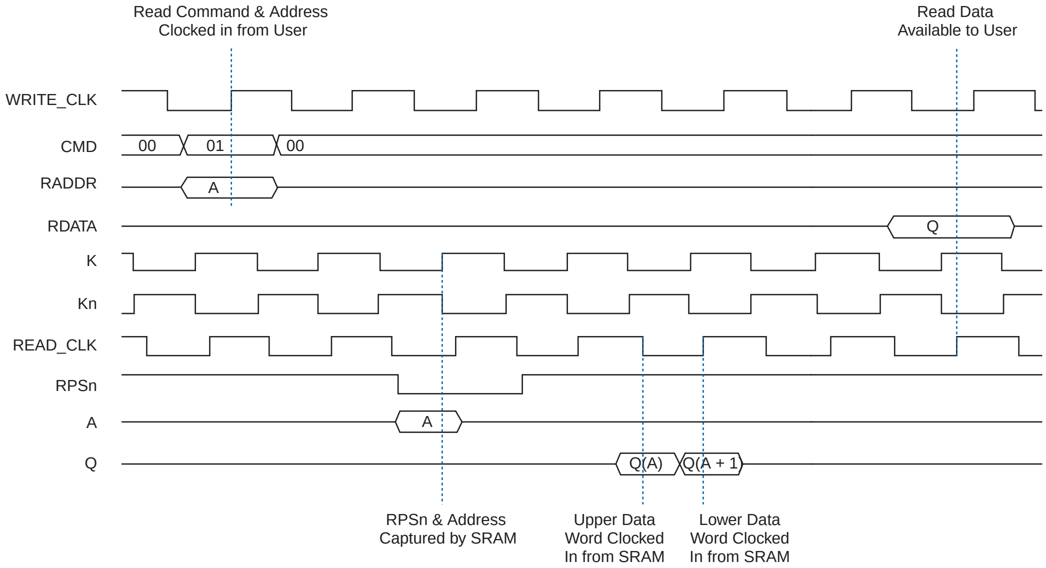
**Figure 2–6. Write Cycle Waveform (Burst-of-2)**



For read operations, the address (`A`) and read port select (`RPSn`) signals are output on the rising edge of `WRITE_CLK`. After the QDR SRAM device captures this information on the rising edge of `K`, the upper and lower data words at that address are driven to `Q` on the next rising edges of `K` and `Kn`, respectively. The controller captures the words on the `READ_CLK` clock's falling and rising edges, respectively. The data is then sent back to the read data (`RDATA`) ports where it is output on the rising edge of `READ_CLK`. Figure 2–7 shows the functionality of the controller for read operations.

This reference design assumes that the QDR SRAM device is operating in single-clock mode. Therefore, the `K` and `Kn` clocks are used for reads as well as writes. See "Clock Generation" on page 2–16 for more details.

*Figure 2–7. Read Cycle Waveform (Burst-of-2)*



## Constraints

The reference design requires constraints to meet the strict timing requirements of QDR SRAM devices. The reference design shows examples of the appropriate pin placement and I/O standard assignments. You can view the assignments required for the reference design by viewing the current assignments floorplan in the Altera Quartus® II software.

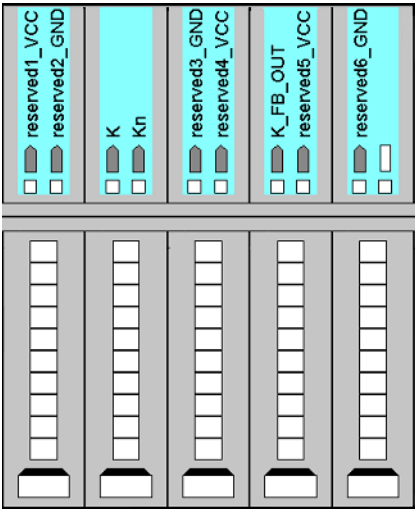
This section provides the required assignments in interface successfully between a QDR SRAM device and a EP1S25F780C6 Stratix device. Other Stratix or Stratix GX devices may require additional location assignments to ensure high-speed operation of the controller.

### *Pin Placement*

To ensure proper pin placement and I/O buffer configuration for the controller, you must use a Quartus II Constraint File (**.csf**) with the following assignments:

- Place the following outputs from the controller on Stratix or Stratix GX device column pins: `A[17..0]`, `D[17..0]`, `RPSn`, `WPSn`, `BWSn[1..0]`, `K`, `Kn`, and `K_FB_OUT`. This placement ensures faster clock-to-out times (**$t_{CO}$**) than could be achieved if the controller outputs were placed on row pins.
- `K`, `Kn`, and `K_FB_OUT` must be assigned to consecutive column pins. Separate these pins by alternating reserved pins tied to $V_{CC}$ and ground to preserve signal integrity, as shown in Figure 2–8.
- You can place the `Q[17..0]` inputs to the controller on either column or row pins.
- Add the assignment **Decrease Input Delay to Input Register = On** to the `Q[17..0]` inputs to minimize the setup time (**$t_{SU}$**) on those pins.

*Figure 2–8. Reserved Pin Placement around K, Kn & K_FB_OUT Clock Pins*



### HSTL I/O Standard Assignments

The QDR SRAM device interface requires the use of the HSTL I/O standard. Stratix and Stratix GX devices are designed to drive out and receive HSTL I/O signals at switching rates greater than 333 Mbps (166.67 MHz, double data rate).

Refer to Chapter 4, Using Selectable I/O Standards in Stratix & Stratix GX Devices for more details on HSTL.

To implement the HSTL I/O interface, perform the following steps:

1. Use the **Assignment Organizer** in the Quartus II software to assign the HSTL Class I I/O standard to all pins that interface with the QDR SRAM device (`A[17..0]`, `D[17..0]`, `Q[17..0]`, `RPSn`, `WPSn`, `BWSn[1..0]`, `K`, `Kn`, `K_FB_IN`, and `K_FB_OUT`).

2. The Quartus II software automatically places reference voltage (`VREF`) pins appropriately, as required by the HSTL Class I I/O standard.

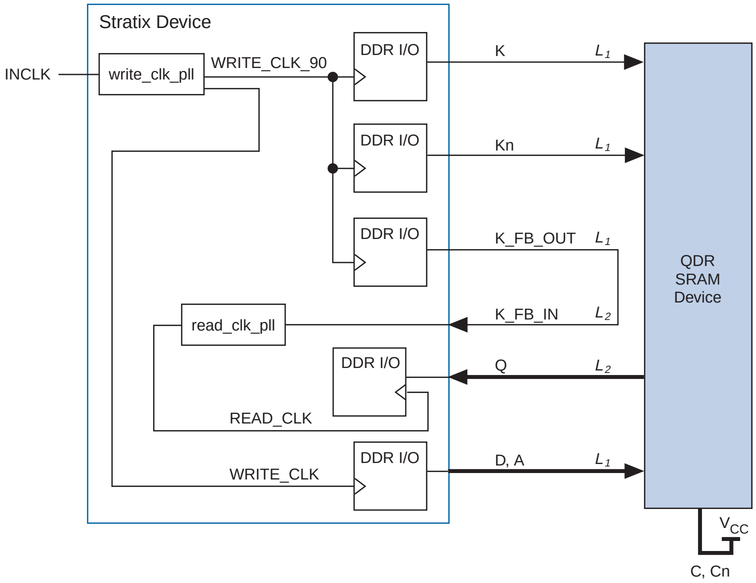
## Clock Generation

The controller clocking scheme maintains consistent and robust high-frequency operation of the QDR SRAM device. The Altera QDR SRAM controller reference design requires two fast PLLs and two global clock resources in the Stratix or Stratix GX device to perform clock generation. The design uses the following clocks:

- `INCLK`—Input clock from the user
- `WRITE_CLK` and `WRITE_CLK_90`—True and 90-degree-phase-shifted controller clocks
- `K` and `Kn`—QDR SRAM clocks
- `K_FB_IN` and `K_FB_OUT`—Controller feedback clock
- `READ_CLK`—Read data capture clock

Figure 2–9 shows how these clocks are generated and used for the QDR SRAM device interface.

*Figure 2–9. Clock Generation* *Note (1)*



*Note to Figure 2–9:*

(1) All L1 traces should be of equal length. All L2 traces should be of equal length. L1 traces do not need to be the same length as L2 traces.

### Internal Clocks

You must supply an input clock (`INCLK`), nominally 166.67 MHz, to the design. This clock feeds an on-chip fast PLL that generates the true (non-phase-shifted) clock for data and address (`WRITE_CLK`) and the 90-degree-shifted clock (`WRITE_CLK_90`) for the `K` and `Kn` outputs.

☞ If necessary, you can supply a lower-frequency input clock and multiply the clock to 166.67 MHz using use the ClockBoost® feature in the PLL.

The controller uses `WRITE_CLK_90` and the DDR I/O registers with the inputs tied to $V_{CC}$ and ground to generate a differential clock signal for the QDR SRAM device. The result is a clock signal (`K`) and a 180° phase-shifted clock signal (`Kn`), each with the same frequency as `WRITE_CLK`.

`READ_CLK`, whose purpose is to clock in the read data from the QDR SRAM device, is generated from a feedback clock using a second PLL, as described in the following sections.

### *QDR SRAM Device Clocks*

The Stratix or Stratix GX device outputs the `K` and `Kn` clocks and the data, address, and control lines to the QDR SRAM device. This action negates the effect of signal skew on the write and read request operations because the propagation delays for `K` and `Kn` from the Stratix or Stratix GX device to the QDR SRAM device are equal to the delays on the data signals. For the controller to operate properly, the trace lengths (and therefore the propagation times) of the data in (`D`), address (`A`), and control signals should be made equal to the trace lengths of the `K` and `Kn` clocks.

Because data is transported both to and from the QDR SRAM device, you should use a similar strategy to eliminate signal skew on read operations. One method is to feed the `K` clock back into the controller and then input this feedback clock to a PLL to generate the `READ_CLK`, which is used capture the read data. In this case, the length of the feedback trace between the QDR SRAM device and the controller should be equal to the read data (`Q`) trace length.

The disadvantage of this method is that the extra tap on the `K` trace (without an additional tap on `Kn`) can cause skew between the `K` and `Kn` clock signals. Because of this issue, the reference design outputs an additional clock, `K_FB_OUT`, to emulate the effect of feedback from `K`. For this method to work properly, the feedback trace length must match the sum of the `D` and `Q` trace lengths. `K_FB_OUT` is returned to the controller as `K_FB_IN`, and used to drive the `READ_CLK` clock.

### *QDR SRAM Device Clock Modes*

QDR SRAM devices can use two pairs of clocks: `K` and `Kn` for writes, and `C` and `Cn` for reads, all provided by the controller. This arrangement is especially useful when a bank of multiple QDR SRAM devices is driven by a single controller. In this case, the `K` and `Kn` traces can be tapped off at various points to drive `C` and `Cn`, respectively, to compensate for differences in flight times between each QDR SRAM device and the controller.

However, the number of loads that must be driven by `K` and `Kn` can have an effect on the switching times of these outputs. Furthermore, when a controller drives a single QDR SRAM device, `C` and `Cn` are unnecessary because propagation delays from the controller to the QDR SRAM device and back are already equal. For these reasons, this reference design assumes that the QDR SRAM device is operating in single-clock mode. In single-clock mode, the `C` and `Cn` inputs are connected to $V_{CC}$, and the `K` and `Kn` inputs are used for both reads and writes.

### *Component Placement*

Finally, Altera recommends that you place the Stratix or Stratix GX device adjacent to the QDR SRAM device on the circuit board. This positioning keeps trace lengths to a minimum and further minimizes any skew caused by board delay.

## Timing

Because data is transferred between the controller and the QDR SRAM device at high speeds, you should take special care to avoid setup or hold violations for the QDR SRAM, Stratix, or Stratix GX device. This section discusses the timing issues that may arise when designing a high-speed QDR SRAM device interface.

### *Write Cycle*

When designing for correct write-cycle timing, meeting the setup and hold requirements of the QDR SRAM device is the primary concern. Setup and hold specifications for the CY7C1302V25-167 device are 0.7 ns each.

The controller drives both the QDR clock and data signals; therefore, the clock-to-output delay from the Stratix or Stratix GX device is the same for both sets of pins. Preliminary timing characteristics show that the clock-to-output delay from the Stratix or Stratix GX column pins under worst-case temperature and voltage conditions can range from 3.2 to 3.5 ns, depending on the pin placement. The board delays for the clock and data are assumed to be roughly equal, because the signal trace lengths should be matched (see "Clock Generation" on page 2–16).

At a clock speed of 166.67 Mhz, the bit period—the length of time between each data bit—is 3 ns. Because `K` and `Kn` are generated from `WRITE_CLK_90`, while data and address are generated from `WRITE_CLK`, there is a timing cushion of one-half of the bit period each way to meet setup and hold times at the QDR SRAM device.

The following calculations apply for 166.67-MHz controller-to-QDR-SRAM data transfers. The calculations allow for up to 0.1 ns of board-induced skew.

$$[\mathbf{t}_{CO}\text{ (Stratix Clock)} - \mathbf{t}_{CO}\text{ (Stratix Data and Address)}] + \text{Board Skew (Clock – Data)} + \mathbf{t}_{SU}\text{ (QDR SRAM)} < \text{(Bit Period)}/2$$

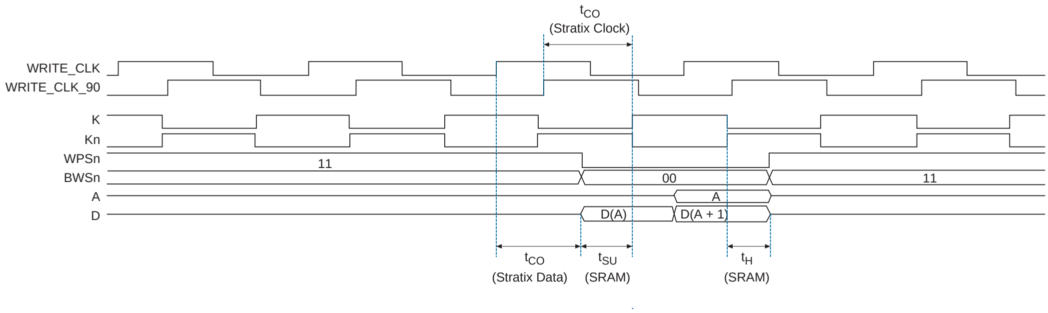
$$[3.5\text{ ns} - 3.2\text{ ns}] + 0.1\text{ ns} + 0.7\text{ ns} = 1.1\text{ ns} < 1.5\text{ ns}$$

[$\mathbf{t_{CO}}$ (Stratix Data and Address) – $\mathbf{t_{CO}}$ (Stratix Clock)] + Board Skew (Clock – Data) + $\mathbf{t_H}$ (QDR SRAM) < (Bit Period)/2

[3.5 ns – 3.2 ns] + 0.1 ns + 0.7 ns = 1.1 ns < 1.5 ns

Figure 2–10 shows the write cycle timing waveform for the QDR SRAM interface pins at 166.67 MHz.

*Figure 2–10. Write Cycle Timing Waveform*



In addition to setup and hold times, an additional concern is the clock-to-clock skew between `K` and `Kn` ($\mathbf{t_{KHKH}}$). The 167-MHz QDR SRAM specification allows for up to 0.6-ns difference between the rising edges of `K` and `Kn`. Because Stratix and Stratix GX clock-to-out times can vary with pin position, place `K` and `Kn` on adjacent pins and check their $\mathbf{t_{CO}}$ times carefully in the Quartus II **Timing Analyzer**. Preliminary timing shows that the controller meets the $\mathbf{t_{KHKH}}$ specification when the `K` and `Kn` pins are adjacent.

### Read Cycle

The read request and address signals are sent to the QDR SRAM device along with the `K` and `Kn` clocks in a similar manner to the write data. Therefore, the write timing parameters apply to these signals as well.

Additionally, when the QDR SRAM device sends read data to the controller, the design must meet the Stratix or Stratix GX device setup and hold times. Preliminary timing characteristics show that the worst-case setup time for the `Q` pins in the reference design is 0.0 ns and worst-case hold time is 0.3 ns.

The clock-to-output specification for the QDR SRAM device determines the arrival time of the `Q` signal. For the CY7C1302V25-167 device, the maximum $\mathbf{t_{CO}}$ value is 2.5 ns and the minimum $\mathbf{t_{CO}}$ value (i.e., the data output hold time $t_{DOH}$) is 1.2 ns.

You can ignore board delay because flight times for the `K_FB` signal and the `Q` bus are roughly equal. Regardless, the timing calculation allows for up to 0.1 ns of board-induced skew between the clock and data lines. Maximum allowed clock skew for `K` and `Kn` is determined by the QDR SRAM device $\mathbf{t_{KHKH}}$ specification as ±0.3 ns. This clock skew allowance is included in the read calculations as well.

The QDR SRAM device sends data out on the rising edge of `K`, and the controller captures it on the falling edge of `READ_CLK`. For a clock speed of 166.67 MHz, there is a window of 3 ns between the rising and falling edges. Subtracting the QDR SRAM device clock-to-output delay of 2.5 ns leaves 0.5 ns of margin for the Stratix setup times and board and clock skew. This margin is sufficient to meet the Stratix device's setup time.

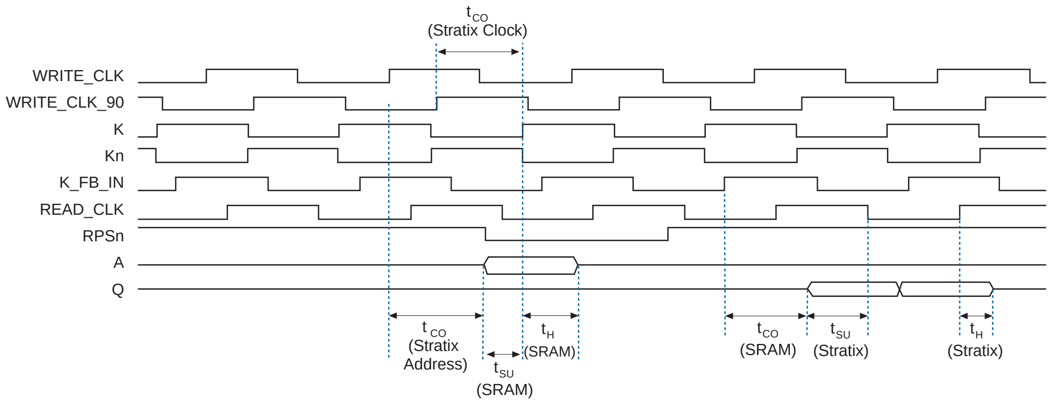
The QDR SRAM device data output hold time is 1.2 ns. This margin is large enough to allow for the Stratix or Stratix GX device hold time.

For the reference design, the following calculations apply for data transfers from the QDR SRAM device to the controller:

> $\mathbf{t_{CO}}$ (QDR SRAM) + Board Skew (`K_FB` – Data) + Clock Skew (`K` – `Kn`) + $\mathbf{t_{SU}}$ (Stratix) < Bit Period
>
> 2.5 ns + 0.1 ns + 0.3 ns + 0.0 ns = 2.9 ns < 3 ns
>
> $\mathbf{t_{DOH}}$ (QDR SRAM) – Board Skew (`K_FB` –Data) – Clock Skew (`K` – `Kn`) – $\mathbf{t_{H}}$ (Stratix) > 0 ns
>
> 1.2 ns – 0.1 ns – 0.3 ns – 0.3 ns = 0.5 ns > 0 ns

Figure 2–11 shows the read cycle timing waveform for the QDR SRAM device interface pins at 166.67 MHz.

***Figure 2–11. Read Cycle Timing Waveform***



### *Read/Write Cycle*

The QDR SRAM controller has independent read and write paths. Therefore, timing does not change for a standalone read or write versus a combined read/write operation.

## Getting Started

This section describes how to install the QDR SRAM controller reference design and walks you through the design flow.

This description is for the Verilog HDL version of the reference design; the description for the VHDL version is similar. However, the filenames have different extensions.

### Hardware & Software Requirements

To use the QDR SRAM controller reference design, you must have the following software installed on your system:

- The Quartus II software version 2.1 or later
- The ModelSim-Altera software version 5.6a or later

This walkthrough uses the Quartus II software version 2.1 and the ModelSim-Altera software version 5.6a on a PC running Windows NT version 4.0.

## Design Installation

Altera provides the QDR SRAM controller reference design as two executable files, one for VHDL and one for Verilog HDL. To install the files, perform the following steps:

☞ You can download both the Verilog HDL and VHDL version of the reference design from the Altera web site at www.altera.com.

1. Save the executable file, **qdr_rd_stratix_vlog-<*version number*>.exe** (Verilog HDL) or **qdr_rd_stratix_vhdl-<*version number*>.exe** (VHDL), onto your hard disk. You can delete this file after you finish installing.

2. Double-click the **qdr_rd_stratix_vlog-<*version number*>.exe** (Verilog HDL) or **qdr_rd_stratix_vhdl-<*version number*>.exe** (VHDL) file in the Windows Explorer to launch the installer.

3. Follow the on-line instructions to complete the installation. The default installation directory is

   **c:\Altera\qdr_rd_stratix_vlog-<*version number*>**.

Figure 2–12 shows the directory structure created by the reference design installer. It also describes selected files (Verilog HDL design files only; the VHDL files have similar functionality).

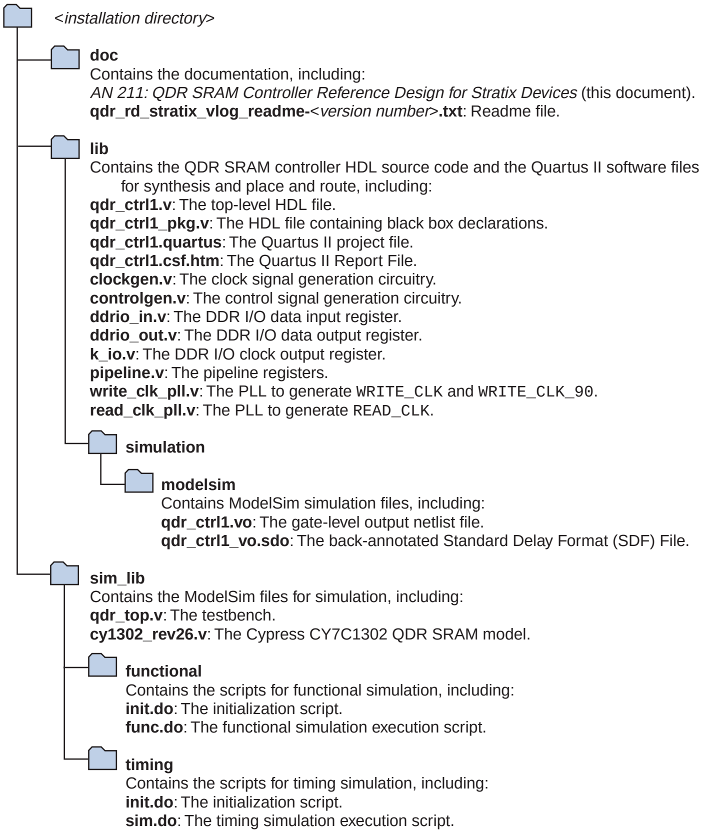


*Figure 2–12. QDR SRAM Controller Directory Structure*

- *<installation directory>*
  - **doc**
    Contains the documentation, including:
    *AN 211: QDR SRAM Controller Reference Design for Stratix Devices* (this document).
    **qdr_rd_stratix_vlog_readme-**<*version number*>**.txt**: Readme file.
  - **lib**
    Contains the QDR SRAM controller HDL source code and the Quartus II software files for synthesis and place and route, including:
    **qdr_ctrl1.v**: The top-level HDL file.
    **qdr_ctrl1_pkg.v**: The HDL file containing black box declarations.
    **qdr_ctrl1.quartus**: The Quartus II project file.
    **qdr_ctrl1.csf.htm**: The Quartus II Report File.
    **clockgen.v**: The clock signal generation circuitry.
    **controlgen.v**: The control signal generation circuitry.
    **ddrio_in.v**: The DDR I/O data input register.
    **ddrio_out.v**: The DDR I/O data output register.
    **k_io.v**: The DDR I/O clock output register.
    **pipeline.v**: The pipeline registers.
    **write_clk_pll.v**: The PLL to generate `WRITE_CLK` and `WRITE_CLK_90`.
    **read_clk_pll.v**: The PLL to generate `READ_CLK`.
    - **simulation**
      - **modelsim**
        Contains ModelSim simulation files, including:
        **qdr_ctrl1.vo**: The gate-level output netlist file.
        **qdr_ctrl1_vo.sdo**: The back-annotated Standard Delay Format (SDF) File.
  - **sim_lib**
    Contains the ModelSim files for simulation, including:
    **qdr_top.v**: The testbench.
    **cy1302_rev26.v**: The Cypress CY7C1302 QDR SRAM model.
    - **functional**
      Contains the scripts for functional simulation, including:
      **init.do**: The initialization script.
      **func.do**: The functional simulation execution script.
    - **timing**
      Contains the scripts for timing simulation, including:
      **init.do**: The initialization script.
      **sim.do**: The timing simulation execution script.

## Design Walkthrough

Altera provides the source files of the reference design, which you can use to synthesize, place-and-route, and simulate the design. This section walks you through the design flow for the reference design. The steps include:

- Compile in the Quartus II software
- Simulate in the ModelSim-Altera software

The reference design includes the results for each step; therefore, you do not need to perform each step unless you have altered the design files. For example, you can run a timing simulation without first compiling the design because the Quartus II software place-and-route results are shipped with the reference design.

### Compile in the Quartus II Software

The <*installation directory*>**\lib** directory contains the Quartus II software version 2.1 project files, including source files for synthesis and place-and-route within the Quartus II software and necessary constraint files for the design to meet the required clock frequencies and I/O timing in the EP1S25F780C6 device.

The following source files are included in the <*installation directory*>**\lib** directory:

- **qdr_ctrl1.v**—Top-level of the QDR SRAM controller.
- **qdr_ctrl1_pkg.v**—Declarations for the black box modules.
- **write_clk_pll.v** and **read_clk_pll.v**—PLL instantiation files created by the Quartus II MegaWizard® Plug-In Manager. These files instantiate the parameterized `altclocklock` function, which generates a PLL in the Stratix device. In the reference design, **write_clk_pll.v** generates `WRITE_CLK` and `WRITE_CLK_90`, and **read_clk_pll.v** generates `READ_CLK`.
- **k_io.v**, **ddrio_out.v**, and **ddrio_in.v**—DDR I/O instantiation files created by the Quartus II MegaWizard Plug-In Manager. **k_io.v** generates the clocks, **ddrio_out.v** generates the output data, and **ddrio_in.v** generates the input data.
- **clockgen.v** and **controlgen.v**—Contain the clock signals (`K`, `Kn`, `K_FB_IN`) and control signals (`BWSn`, `RPSn`, and `WPSn`) generation circuitry, respectively.
- **pipeline.v**—Adds three pipeline stages to both the read and write paths.

The QDR SRAM controller instantiates these pipeline registers so that the design meets the $\mathbf{f_{MAX}}$ performance requirements. The source code (**qdr_ctrl1.v** for Verilog HDL or **qdr_ctrl1_pkg.vhd** for VHDL) includes the parameter `INCLUDE_PIPELINE_REGS`, which controls whether the extra pipeline stages are added to the write and read paths. You can set this parameter to `FALSE` to eliminate the pipeline stages.

To compile the Altera-provided project files, follow the steps below:

1. Run the Quartus II software.

2. Choose **Open Project** (File menu).

3. Browse to the <*installation directory*>**\lib** directory.

4. Select the project file **qdr_ctrl1.quartus** and click **Open**.

5. Choose **Compile Mode** (Processing menu).

6. Choose **Start Compilation** (Processing menu).

### *Simulate in the ModelSim-Altera Software*

The **sim_lib** directory contains an HDL testbench file (**qdr_top.v**) that instantiates the QDR SRAM controller and the QDR SRAM model (**cy1302_rev26.v**). The testbench implements four pipelined writes, four pipelined reads, a standalone write operation, a read/write operation, and a standalone read operation, to demonstrate the functionality of the controller. The testbench adds delay to the board traces to model the propagation delay between the Stratix or Stratix GX device and the QDR SRAM device. You can model different board delay scenarios by changing these values.

Altera provides the following scripts to perform functional and timing simulation in the ModelSim-Altera software.

- **init.do**—This script creates the work library and pre-compiles the correct simulation libraries for functional or timing simulation.
- **func.do**—This script, located in the **functional** subdirectory, compiles the controller source files, the model, and the testbench, and displays the appropriate waveforms.
- **sim.do**—This script, located in the **timing** subdirectory, compiles the gate-level HDL output netlist file generated by the Quartus II software (**\lib\simulation\modelsim\qdr_ ctrl1.vo**), the model, and the testbench, and performs a timing simulation with a back-annotated Standard Delay Format File (**.sdf**) (**\lib\simulation\modelsim\qdr_ ctrl1_v.sdo**).

Before using the **init.do** script, you should update it so that the paths in the script point to the location in which you installed the Quartus II software.

To perform functional simulation, perform the following steps:

1. Run the ModelSim-Altera software.

2. Change your working directory to the <*installation directory*>**\sim_lib\functional** directory.

3. Type the following commands in the **Command Window**:

```
do init.do ↵
do func.do ↵
```

To perform timing simulation, perform the following steps:

1. Copy the files in the <*installation directory*>**\lib\simulation\modelsim** directory to the <*installation directory*>**\sim_lib\timing** directory.
2. Run the ModelSim-Altera software.
3. Change your working directory to the <*installation directory*>**\sim_lib\timing** directory.
4. Type the following commands in the **Command Window**:

```
do init.do ↵
do sim.do ↵
```

☞ For Verilog HDL simulation, the ModelSim-Altera software may show setup violations at the start of simulation as the initial values settle through the controller. However, there should not be any setup violations during actual operation of the controller.

### *Instantiation within an SOPC Design*

You can instantiate the QDR SRAM controller design files in an HDL file and integrate it with an SOPC design. This section describes the steps you should follow to integrate the controller into an SOPC design. Generally, you should use the information found in "Design Walkthrough" on page 2–24 as a reference when integrating the controller with your system.

#### Synthesis

If you are using a third-party synthesis tool for your SOPC design, Altera recommends that you black box the QDR SRAM controller through that synthesis tool, as synthesis of the QDR SRAM controller source files outside of the Quartus II software has not been tested.

#### Place & Route

Before compiling your SOPC design in the Quartus II software, you must add the **lib** directory to your Quartus II project as a user library. Search for "User Libraries" in Quartus II Help for more information.

To ensure that your design meets the QDR timing requirements, you should generate an appropriate constraint file for your SOPC design. See "Constraints" on page 2–14. Refer to the Quartus II project provided in the **lib** directory for example project assignments.

### Simulation

The simulation testbench and scripts shipped with the reference design are intended to demonstrate the correct operation of the stand-alone QDR SRAM device interface. Altera recommends that you generate your own simulation environment that is better-suited to your SOPC design and EDA tools.

## Resource Usage

For Stratix or Stratix GX devices, the QDR SRAM controller reference design requires the device resources shown in Table 2–4.

*Table 2–4. Resource Usage*

| Logic Cells | PLLs | Global Clocks | I/O Pins |
|---|---|---|---|
| 220 | 2 | 2 | 68 *(1)* |

***Note to Table 2–4:***

(1) 68 I/O pins, plus additional `VREF` pins, are needed to interface to the QDR SRAM device. An additional 111 pins are necessary if you want to interface with the controller from outside the Stratix or Stratix GX device, as implemented in the reference design.

## Support

For information or support for the QDR SRAM controller reference design, go to mysupport.altera.com or contact Altera Applications.

## Conclusion

QDR SRAM devices were designed for high-bandwidth communications applications and outperform other memory devices by up to four times in networking applications. The advanced features of Altera's Stratix oand Stratix GX devices help communications system designers take advantage of QDR SRAM technology and achieve the greatest possible performance when interfacing with QDR SRAM devices. Designers can use the QDR SRAM controller reference design to quickly implement a QDR SRAM controller in a Stratix or Stratix GX device to provide the highest possible memory performance for their systems.

## Reference

*CY7C1302V25 9-Mb Pipelined SRAM with QDR Architecture Advance Information*, Cypress Semiconductor Corporation

# 3. Using TriMatrix Embedded Memory Blocks in Stratix & Stratix GX Devices

S52003-1.0

Chapter 3, Using TriMatrix Embedded Memory Blocks in Stratix & Stratix GX Devices replaces *AN 203: Using TriMatrix Emebedded Memory Blocks in Stratix & Stratix GX Devices*.

## Introduction

Stratix™ and Stratix GX devices feature the TriMatrix™ memory structure, composed of three sizes of embedded RAM blocks. TriMatrix memory includes 512-bit M512 blocks, 4-Kbit M4K blocks, and 512-Kbit M-RAM blocks, each of which is configurable to support a wide range of features. Offering up to 10 Mbits of RAM and up to 12 terabits per second of device memory bandwidth, the TriMatrix memory structure makes the Stratix and Stratix GX families ideal for memory-intensive applications.

## TriMatrix Memory

TriMatrix memory structures can implement a wide variety of complex memory functions. For example, use the small M512 blocks for first-in first-out (FIFO) functions and clock domain buffering where memory bandwidth is critical. The M4K blocks are an ideal size for applications requiring medium-sized memory, such as asynchronous transfer mode (ATM) cell processing. M-RAM blocks enhance programmable logic device (PLD) memory capabilities for large buffering applications, such as internet protocol (IP) packet buffering and system cache.

TriMatrix memory blocks support various memory configurations, including single-port, simple dual-port, true dual-port (also known as bidirectional dual-port), shift-register, ROM, and FIFO mode. The TriMatrix memory architecture also includes advanced features and capabilities, such as byte enable support, parity-bit support, and mixed-port width support. This application note describes the various TriMatrix memory modes and features.

Table 3–1 summarizes the features supported by the three sizes of TriMatrix memory.

For more information on selecting which memory block to use, refer to *Application Note 207: TriMatrix Memory Selection Using the Quartus II Software.*

***Table 3–1. Summary of TriMatrix Memory Features***

| Feature | M512 Block | M4K Block | M-RAM Block |
|---|---|---|---|
| Performance | 312 MHz | 312 MHz | 300 MHz |
| Total RAM bits (including parity bits) | 576 | 4,608 | 589,824 |
| Configurations | 512 × 1<br>256 × 2<br>128 × 4<br>64 × 8<br>64 × 9<br>32 × 16<br>32 × 18 | 4K × 1<br>2K × 2<br>1K × 4<br>512 × 8<br>512 × 9<br>256 × 16<br>256 × 18<br>128 × 32<br>128 × 36 | 64K × 8<br>64K × 9<br>32K × 16<br>32K × 18<br>16K × 32<br>16K × 36<br>8K × 64<br>8K × 72<br>4K × 128<br>4K × 144 |
| Parity bits | ✓ | ✓ | ✓ |
| Byte enable |  | ✓ | ✓ |
| Single-port memory | ✓ | ✓ | ✓ |
| Simple dual-port memory | ✓ | ✓ | ✓ |
| True dual-port memory |  | ✓ | ✓ |
| Embedded shift register | ✓ | ✓ |  |
| ROM | ✓ | ✓ |  |
| FIFO buffer | ✓ | ✓ | ✓ |
| Simple dual-port mixed width support | ✓ | ✓ | ✓ |
| True dual-port mixed width support |  | ✓ | ✓ |
| Memory initialization (**.mif**) | ✓ | ✓ |  |
| Mixed-clock mode | ✓ | ✓ | ✓ |
| Power-up condition | Outputs cleared | Outputs cleared | Outputs unknown |
| Register clears | Input and output registers *(1)* | Input and output registers *(2)* | Output registers |
| Same-port read-during-write | New data available at positive clock edge | New data available at positive clock edge | New data available at positive clock edge |
| Mixed-port read-during-write | Outputs set to unknown or old data | Outputs set to unknown or old data | Unknown output |

***Notes to Table 3–1:***

(1) The `rden` register on the M512 memory block does not have a clear port.

(2) On the M4K block, asserting the clear port of the `rden` and byte enable registers drives the output of these registers high.

The extremely high memory bandwidth of the Stratix and Stratix GX device families is a result of increased memory capacity and speed. Table 3–2 shows the memory capacity for TriMatrix memory blocks in each Stratix device. Table 3–3 shows the memory capacity for TriMatrix memory blocks in each Stratix GX device.

*Table 3–2. TriMatrix Memory Distribution in Stratix Devices*

| Device | M512 Columns/Blocks | M4K Columns/Blocks | M-RAM Blocks | Total RAM Bits |
|---|---|---|---|---|
| EP1S10 | 4 / 94 | 2 / 60 | 1 | 920,448 |
| EP1S20 | 6 / 194 | 2 / 82 | 2 | 1,669,248 |
| EP1S25 | 6 / 224 | 3 / 138 | 2 | 1,944,576 |
| EP1S30 | 7 / 295 | 3 / 171 | 4 | 3,317,184 |
| EP1S40 | 8 / 384 | 3 / 183 | 4 | 3,423,744 |
| EP1S60 | 10 / 574 | 4 / 292 | 6 | 5,215,104 |
| EP1S80 | 11 / 767 | 4 / 364 | 9 | 7,427,520 |

*Table 3–3. TriMatrix Memory Distribution in Stratix GX Devices*

| Device | M512 Columns/Blocks | M4K Columns/Blocks | M-RAM Blocks | Total RAM Bits |
|---|---|---|---|---|
| EP1SGX10 | 4 / 94 | 2 / 60 | 1 | 920,448 |
| EP1SGX25 | 6 / 224 | 3 / 138 | 2 | 1,944,576 |
| EP1SGX40 | 8 / 384 | 3 / 183 | 4 | 3,423,744 |

## Parity Bit Support

The memory blocks support a parity bit for each byte. Parity bits are in addition to the amount of memory in each RAM block. For example, the M512 block has 576 bits, 64 of which are optionally used for parity bit storage. The parity bit, along with logic implemented in logic elements (LEs), can implement parity checking for error detection to ensure data integrity. Parity-size data words can also store user-specified control bits.

## Byte Enable Support

In the M4K and M-RAM blocks, byte enables can mask the input data so that only specific bytes of data are written. The unwritten bytes retain the previous written value. The write enable signals (`wren`), in conjunction with the byte enable signals (`byteena`), controls the RAM block's write operations. The default value for the `byteena` signals is high (enabled), in which case writing is controlled only by the `wren` signals.

Asserting the clear port of the byte enable registers drives the byte enable signals to their default high level.

### *M4K Blocks*

M4K blocks support byte writes when the write port has a data width of 16, 18, 32, or 36 bits. Table 3–4 summarizes the byte selection.

***Table 3–4. Byte Enable for M4K Blocks*** *Notes (1), (2)*

| byteena | datain ×18 | datain ×36 |
|---|---|---|
| [0] = 1 | [8..0] | [8..0] |
| [1] = 1 | [17..9] | [17..9] |
| [2] = 1 | – | [26..18] |
| [3] = 1 | – | [35..27] |

***Note to Table 3–4:***

(1) Any combination of byte enables is possible.

(2) Byte enables can be used in the same manner with 8-bit words, i.e., in ×16 and ×32 modes.

### M-RAM Blocks

M-RAM blocks support byte enables for the ×16, ×18, ×32, ×36, ×64, and ×72 modes. In the ×128 or ×144 simple dual-port mode, the two sets of `byteena` signals (`byteena_a` and `byteena_b`) combine to form the necessary 16 byte enables. Tables 3–5 and 3–6 summarize the byte selection.

*Table 3–5. Byte Enable for M-RAM Blocks* Notes (1), (2)

| byteena | datain ×18 | datain ×36 | datain ×72 |
|---|---|---|---|
| [0] = 1 | [8..0] | [8..0] | [8..0] |
| [1] = 1 | [17..9] | [17..9] | [17..9] |
| [2] = 1 | – | [26..18] | [26..18] |
| [3] = 1 | – | [35..27] | [35..27] |
| [4] = 1 | – | – | [44..36] |
| [5] = 1 | – | – | [53..45] |
| [6] = 1 | – | – | [62..54] |
| [7] = 1 | – | – | [71..63] |

***Notes to Table 3–5:***

(1) Any combination of byte enables is possible.

(2) Byte enables can be used in the same manner with 8-bit words, i.e., in ×16, ×32, and ×64 modes.

*Table 3–6. M-RAM Combined Byte Selection for ×144 Mode* Notes (1), (2) *(Part 1 of 2)*

| byteena_a | datain ×144 |
|---|---|
| [0] = 1 | [8..0] |
| [1] = 1 | [17..9] |
| [2] = 1 | [26..18] |
| [3] = 1 | [35..27] |
| [4] = 1 | [44..36] |
| [5] = 1 | [53..45] |
| [6] = 1 | [62..54] |
| [7] = 1 | [71..63] |
| [8] = 1 | [80..72] |
| [9] = 1 | [89..81] |
| [10] = 1 | [98..90] |
| [11] = 1 | [107..99] |

**Table 3–6. M-RAM Combined Byte Selection for ×144 Mode Notes (1), (2) (Part 2 of 2)**

| byteena_a | datain ×144 |
|---|---|
| [12] = 1 | [116..108] |
| [13] = 1 | [125..117] |
| [14] = 1 | [134..126] |
| [15] = 1 | [143..135] |

*Notes to Table 3–6:*

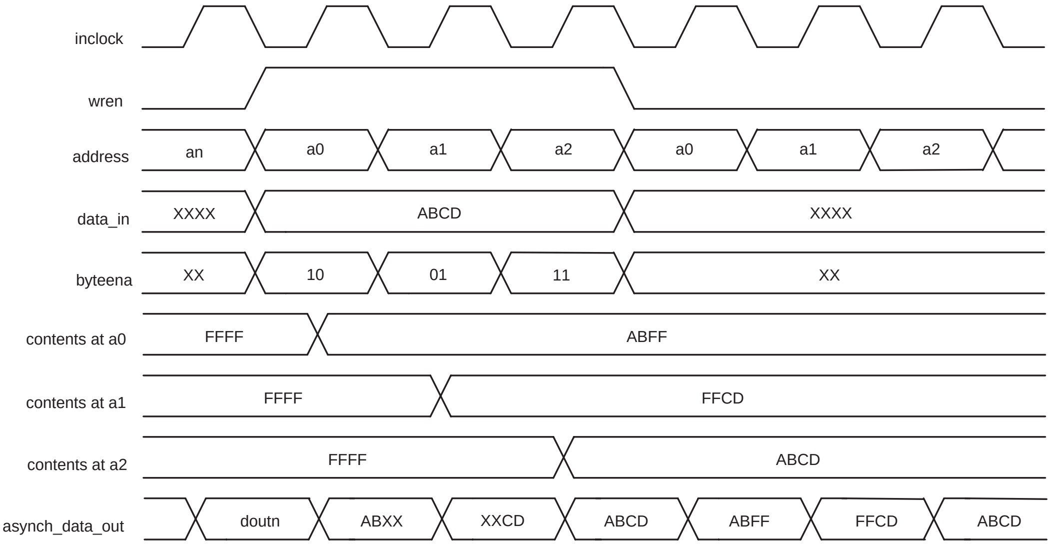
(1) Any combination of byte enables is possible.

(2) Byte enables can be used in the same manner with 8-bit words, i.e., in ×16, ×32, ×64, and ×128 modes.

## Byte Enable Functional Waveform

Figure 3–1 shows how both the `wren` and the `byteena` signals control the write operations of the RAM.

**Figure 3–1. Byte Enable Functional Waveform Note (1)**



*Note to Figure 3–1:*

(1) For more information on simulation output when a read-during-write occurs at the same address location, refer to "Read-during-Write Operation at the Same Address" on page 3–24.

## Using TriMatrix Memory

The TriMatrix memory blocks include input registers that synchronize writes and output registers to pipeline designs and improve system performance. All TriMatrix memory blocks are fully synchronous, meaning that all inputs are registered, but outputs are either registered or combinatorial. TriMatrix memory can emulate asynchronous memory.

For more information, refer to *Application Note 210: Converting Memory from Asynchronous to Synchronous for Stratix & Stratix GX Designs*.

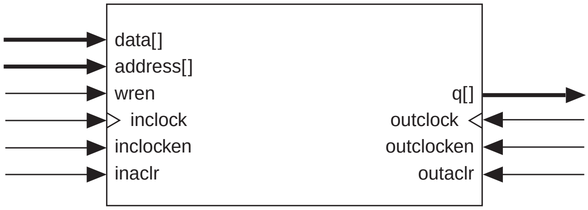
Depending on the TriMatrix memory block type, the memory can have various modes, including:

- Single-port
- Simple dual-port
- True dual-port (bidirectional dual-port)
- Shift-register
- ROM
- FIFO

### Implementing Single-Port Mode

Single-port mode supports non-simultaneous reads and writes. Figure 3–2 shows the single-port memory configuration for TriMatrix memory. All memory block types support the single-port mode.

***Figure 3–2. Single-Port Memory*** *Note (1)*



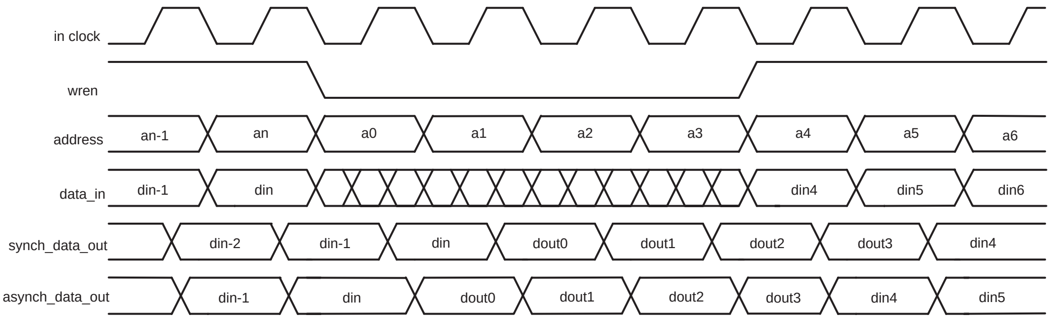
***Note to Figure 3–2:***
(1) Two single-port memory blocks can be implemented in a single M4K block.

M4K memory blocks can also be divided in half and used for two independent single-port RAM blocks. The Altera® Quartus® II software automatically uses this single-port memory packing when running low on memory resources. To force two single-port memories into one M4K block, first ensure that each of the two independent RAM blocks is equal to or less than half the size of the M4K block. Second, assign both single-port RAMs to the same M4K block.

In the single-port RAM configuration, the outputs can only be in read-during-write mode, which means that during the write operation, data written to the RAM flows through to the RAM outputs. When the output registers are bypassed, the new data is available on the rising edge of the same clock cycle it was written on. For more information about read-during-write mode, refer to "Read-during-Write Operation at the Same Address" on page 3–24.

Figure 3–3 shows timing waveforms for read and write operations in single-port mode.

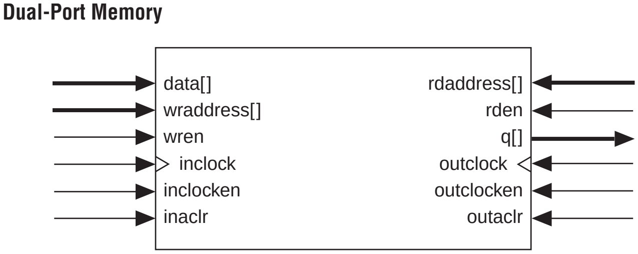
***Figure 3–3. Single-Port Timing Waveforms***



## Implementing Simple Dual-Port Mode

Simple dual-port memory supports a simultaneous read and write. Figure 3–4 shows the simple dual-port memory configuration for TriMatrix memory. All memory block types support this configuration.

***Figure 3–4. Simple Dual-Port Memory*** *Note (1)*



*Note to Figure 3–4:*

(1) Simple dual-port RAM supports read/write clock mode in addition to the input/output clock mode shown.

TriMatrix memory supports mixed-width configurations, allowing different read and write port widths. Tables 3–7 to 3–9 show the mixed width configurations for the M512, M4K, and M-RAM blocks, respectively.

*Table 3–7. M512 Block Mixed-Width Configurations (Simple Dual-Port Mode)*

| Read Port | Write Port | | | | | | |
|---|---|---|---|---|---|---|---|
| | 512 × 1 | 256 × 2 | 128 × 4 | 64 × 8 | 32 × 16 | 64 × 9 | 32 × 18 |
| 512 × 1 | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| 256 × 2 | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| 128 × 4 | ✓ | ✓ | ✓ | | ✓ | | |
| 64 × 8 | ✓ | ✓ | | ✓ | | | |
| 32 × 16 | ✓ | ✓ | ✓ | | ✓ | | |
| 64 × 9 | | | | | | ✓ | |
| 32 × 18 | | | | | | | ✓ |

*Table 3–8. M4K Block Mixed-Width Configurations (Simple Dual-Port Mode)*

| Read Port | Write Port | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | 4K × 1 | 2K × 2 | 1K × 4 | 512 × 8 | 256 × 16 | 128 × 32 | 512 × 9 | 256 × 18 | 128 × 36 |
| 4K × 1 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| 2K × 2 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| 1K × 4 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| 512 × 8 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| 256 × 16 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| 128 × 32 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| 512 × 9 | | | | | | | ✓ | ✓ | ✓ |
| 256 × 18 | | | | | | | ✓ | ✓ | ✓ |
| 128 × 36 | | | | | | | ✓ | ✓ | ✓ |

*Table 3–9. M-RAM Block Mixed-Width Configurations (Simple Dual-Port Mode)*

| Read Port | Write Port | | | | |
|---|---|---|---|---|---|
| | 64K × 9 | 32K × 18 | 16K × 36 | 8K × 72 | 4K × 144 |
| 64K × 9 | ✓ | ✓ | ✓ | ✓ | |
| 32K × 18 | ✓ | ✓ | ✓ | ✓ | |
| 16K × 36 | ✓ | ✓ | ✓ | ✓ | |
| 8K × 72 | ✓ | ✓ | ✓ | ✓ | |
| 4K × 144 | | | | | ✓ |

M512 blocks support serializer and deserializer (SERDES) applications. By using the mixed-width support in combination with double data rate (DDR) I/O standards, the block can function as a SERDES to support low-speed serial I/O standards using global or regional clocks.

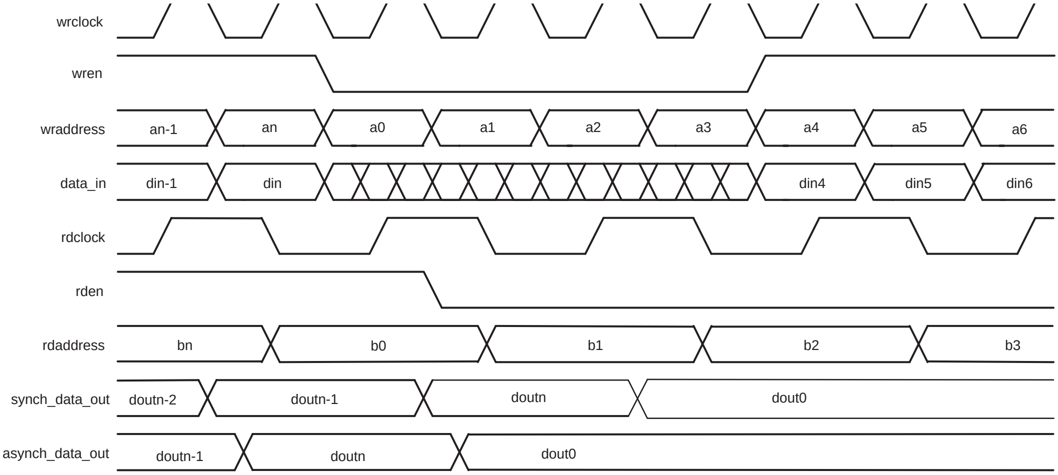
For more information on Stratix device I/O structure refer to Section I, Stratix Device Family Data Sheet of the *Stratix Device Handbook, Volume 1*. For more information on Stratix GX device I/O structure refer to the *Stratix GX FPGA Family Data Sheet*.

In simple dual-port mode, the M512 and M4K blocks have one write enable and one read enable signal. The M512 does not support a clear port on the `rden` register. On the M4K block, asserting the clear port of the `rden` register drives `rden` high, which allows the read operation to occur. When the read enable is deactivated, the current data is retained at the output ports. If the read enable is activated during a write operation with the same address location selected, the simple dual-port RAM output is either unknown or can be set to output the old data stored at the memory address. For more information, refer to "Read-during-Write Operation at the Same Address" on page 3–24.

M-RAM blocks have one write enable signal in simple dual-port mode. To perform a write operation, the write enable is held high. The M-RAM block is always enabled for read operation. If the read address and the write address select the same address location during a write operation, the M-RAM block output is unknown.

Figure 3–5 shows timing waveforms for read and write operations in simple dual-port mode.

*Figure 3–5. Simple Dual-Port Timing Waveforms* Note (1)



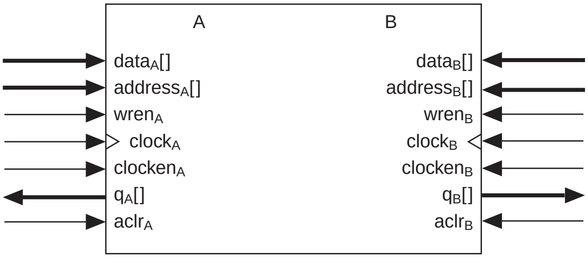
*Note to Figure 3–5:*

(1) The `rden` signal is not available in the M-RAM block. A M-RAM block in simple dual-port mode is always reading out the data stored at the current read address location.

## Implementing True Dual-Port Mode

M4K and M-RAM blocks offer a true dual-port mode to support any combination of two-port operations: two reads, two writes, or one read and one write at two different clock frequencies. Figure 3–6 shows the true dual-port memory configuration for TriMatrix memory.

*Figure 3–6. True Dual-Port Memory* Note (1)



*Note to Figure 3–6:*

(1) True dual-port memory supports input/output clock mode in addition to the independent clock mode shown.

The widest bit configuration of the M4K and M-RAM blocks in true dual-port mode is 256 × 16-bit (× 18-bit with parity) and 8K × 64-bit (× 72-bit with parity), respectively. The 128 × 32-bit (× 36-bit with parity) configuration of the M4K block and the 4K × 128-bit (× 144-bit with parity) configuration of the M-RAM block are unavailable because the number of output drivers is equivalent to the maximum bit width of the respective memory block. Because true dual-port RAM has outputs on two ports, the maximum width of the true dual-port RAM equals half of the total number of output drivers. Tables 3–10 and 3–11 list the possible M4K RAM block and M-RAM block configurations, respectively.

*Table 3–10. M4K Block Mixed-Port Width Configurations (True Dual-Port)*

| Port A | Port B | | | | | | |
|---|---|---|---|---|---|---|---|
| | 4K × 1 | 2K × 2 | 1K × 4 | 512 × 8 | 256 × 16 | 512 × 9 | 256 × 18 |
| 4K × 1 | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| 2K × 2 | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| 1K × 4 | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| 512 × 8 | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| 256 × 16 | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| 512 × 9 | | | | | | ✓ | ✓ |
| 256 × 18 | | | | | | ✓ | ✓ |

*Table 3–11. M-RAM Block Mixed-Port Width Configurations (True Dual-Port)*

| Port A | Port B | | | |
|---|---|---|---|---|
| | 64K × 9 | 32K × 18 | 16K × 36 | 8K × 72 |
| **64K × 9** | ✓ | ✓ | ✓ | ✓ |
| **32K × 18** | ✓ | ✓ | ✓ | ✓ |
| **16K × 36** | ✓ | ✓ | ✓ | ✓ |
| **8K × 72** | ✓ | ✓ | ✓ | ✓ |

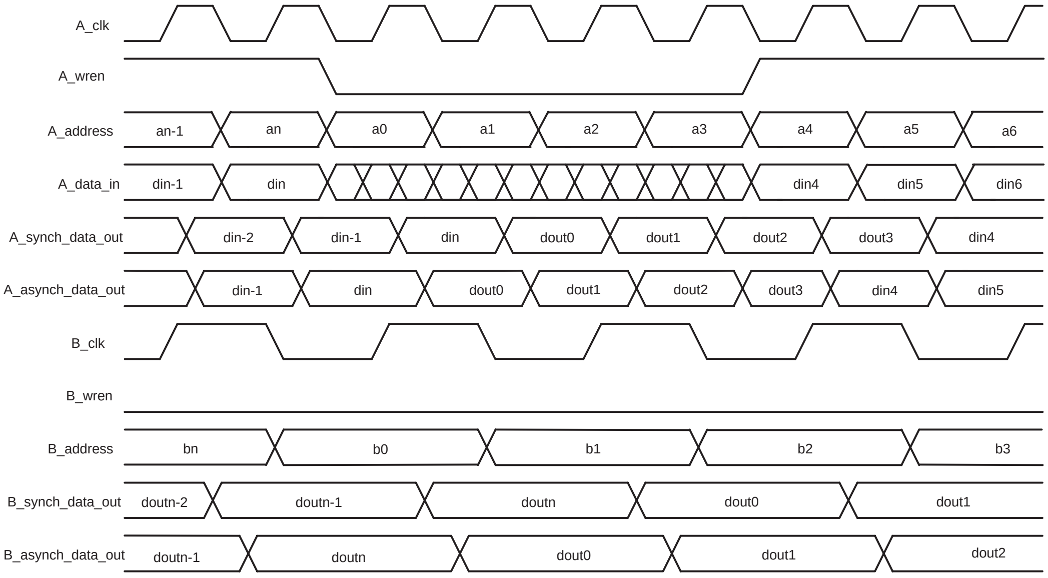
In true dual-port configuration, the RAM outputs can only be configured for read-during-write mode. This means that during write operation, data being written to the A or B port of the RAM flows through to the A or B outputs, respectively. When the output registers are bypassed, the new data is available on the rising edge of the same clock cycle it was written on. For waveforms and information on mixed-port read-during-write mode, refer to "Read-during-Write Operation at the Same Address" on page 3–24.

Potential write contentions must be resolved external to the RAM because writing to the same address location at both ports results in unknown data storage at that location. For a valid write operation to the same address of the M-RAM block, the rising edge of the write clock for port A must occur following the maximum write cycle time interval after the rising edge of the write clock for port B. Since data is written into the M512 and M4K blocks at the falling edge of the write clock, the rising edge of the write clock for port A should occur following half of the maximum write cycle time interval after the falling edge of the write clock for port B. If this timing is not met, the data stored in that particular address will be invalid.

Refer to Section I, Stratix Device Family Data Sheet of the *Stratix Device Handbook, Volume 1* or the *Stratix GX FPGA Family Data Sheet* for the maximum synchronous write cycle time.

Figure 3–7 shows true dual-port timing waveforms for write operation at port A and read operation at port B.

***Figure 3–7. True Dual-Port Timing Waveforms***



## Implementing Shift-Register Mode

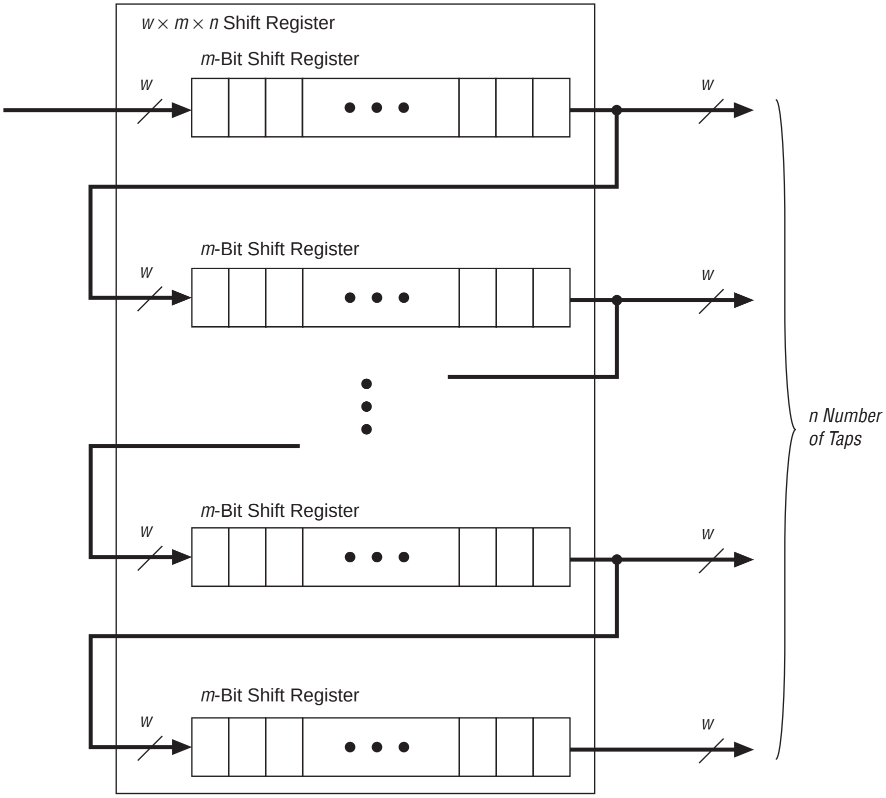
Embedded memory block configurations can implement shift registers for digital signal processing (DSP) applications, such as finite impulse response (FIR) filters, pseudo-random number generators, multi-channel filtering, and auto-correlation and cross-correlation functions. These and other DSP applications require local data storage, traditionally implemented with standard flip-flops that can quickly consume many logic cells for large shift registers. A more efficient alternative is to use embedded memory as a shift register block, which saves logic cell and routing resources and provides a more efficient implementation.

The size of a $(w \times m \times n)$ shift register is determined by the input data width ($w$), the length of the taps ($m$), and the number of taps ($n$). The size of a $(w \times m \times n)$ shift register must be less than or equal to the maximum number of memory bits in the respective block: 576 bits for the M512 block and 4,608 bits for the M4K block. In addition, the size of $w \times n$ must be less than or equal to the maximum width of the respective block: 18 bits for the M512 block and 36 bits for the M4K block. If a larger shift register is required, the memory blocks can be cascaded together.

☞ M-RAM blocks do not support the shift-register mode.

Data is written into each address location at the falling edge of the clock and read from the address at the rising edge of the clock. The shift-register mode logic automatically controls the positive and negative edge clocking to shift the data in one clock cycle. Figure 3–8 shows the TriMatrix memory block in the shift-register mode.

*Figure 3–8. Shift-Register Memory Configuration*



## Implementing ROM Mode

The M512 and the M4K blocks support ROM mode. Use a memory initialization file (**.mif**) to initialize the ROM contents of M512 and M4K blocks. The M-RAM block does not support ROM mode.

All Stratix memory configurations must have synchronous inputs; therefore, the address lines of the ROM are registered. The outputs can be registered or combinatorial. The ROM read operation is identical to the read operation in the single-port RAM configuration.

## Implementing FIFO Buffers

While the small M512 memory blocks are ideal for designs with many shallow FIFO buffers, all three memory sizes support FIFO mode.

All memory configurations have synchronous inputs; however, the FIFO buffer outputs are always combinatorial. Simultaneous read and write from an empty FIFO is not supported.

## Clock Modes

Depending on the TriMatrix memory mode, independent, input/output, read/write, and/or single-port clock modes are available. Table 3–12 shows the clock modes supported by the TriMatrix memory modes.

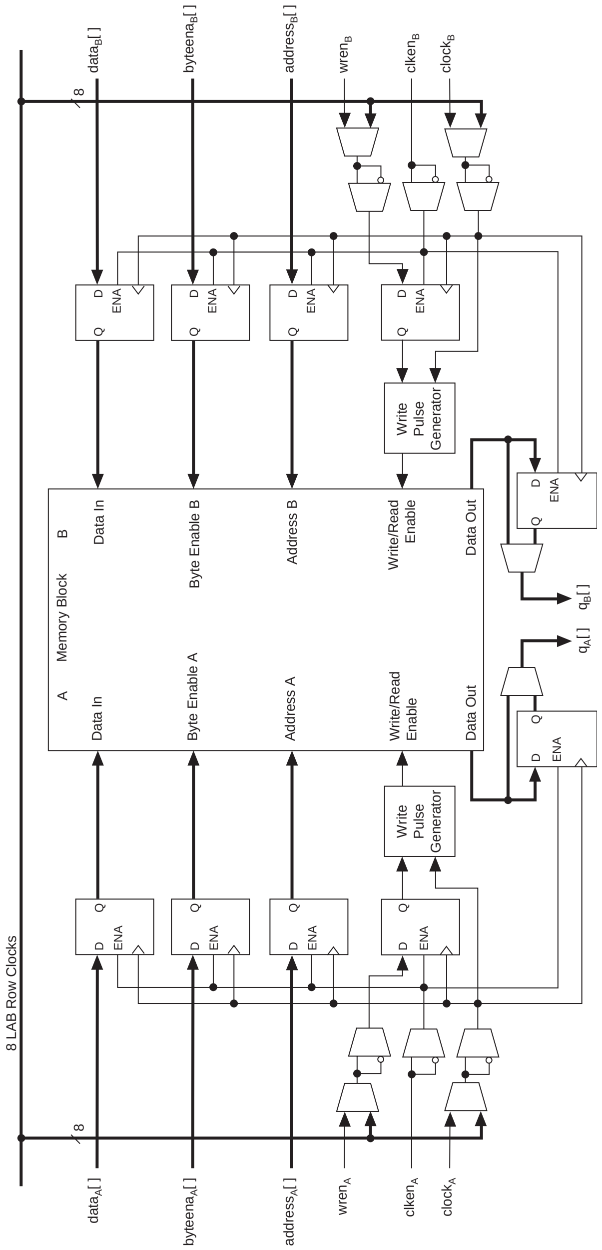
*Table 3–12. TriMatrix Memory Clock Modes*

| Clocking Mode | True-Dual Port Mode | Simple Dual-Port Mode | Single-Port Mode |
|---|---|---|---|
| Independent | ✓ | | |
| Input/output | ✓ | ✓ | |
| Read/write | | ✓ | |
| Single-port | | | ✓ |

### Independent Clock Mode

The TriMatrix memory blocks can implement independent clock mode for true dual-port memory. In this mode, a separate clock is available for each port (A and B). Clock A controls all registers on the port A side, while clock B controls all registers on the port B side. Each port also supports independent clock enables and asynchronous clear signals for port A and B registers. Figure 3–9 shows a TriMatrix memory block in independent clock mode.

*Figure 3–9. Independent Clock Mode*



### Input/Output Clock Mode

The TriMatrix memory blocks can implement input/output clock mode for true and simple dual-port memory. On each of the two ports, A and B, one clock controls all registers for inputs into the memory block: data input, `wren`, and address. The other clock controls the block's data output registers. Each memory block port also supports independent clock enables and asynchronous clear signals for input and output registers. Figures 3–10 and 3–11 show the memory block in input/output clock mode for true and simple dual-port modes, respectively.

*Figure 3–10. Input/Output Clock Mode in True Dual-Port Mode*

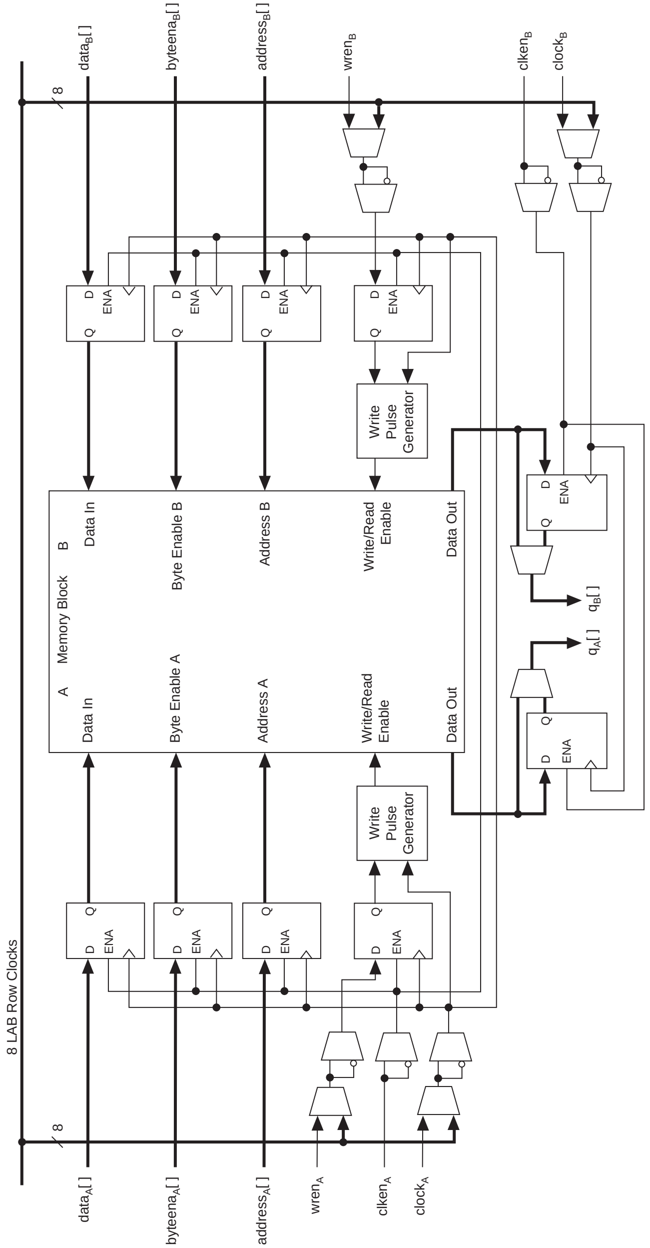
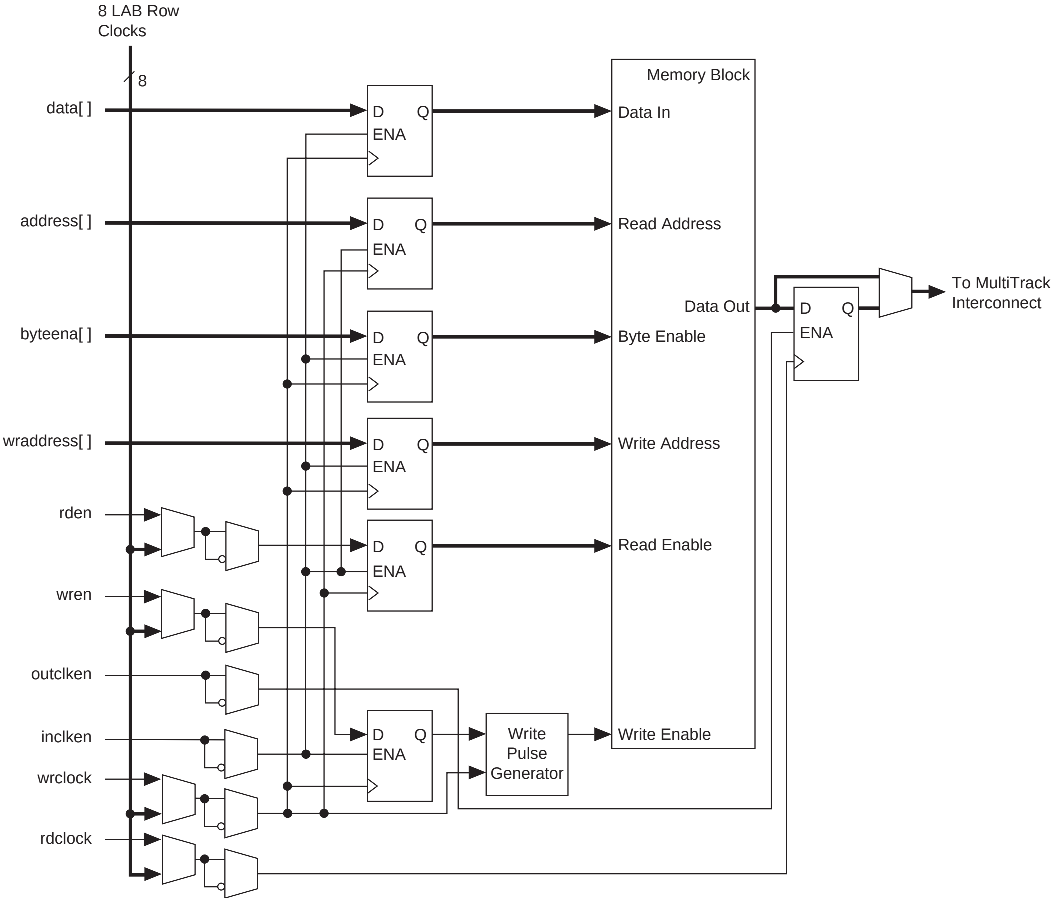


*Figure 3–11. Input/Output Clock Mode in Simple Dual-Port Mode* Notes (1), (2)



*Notes to Figure 3–11:*

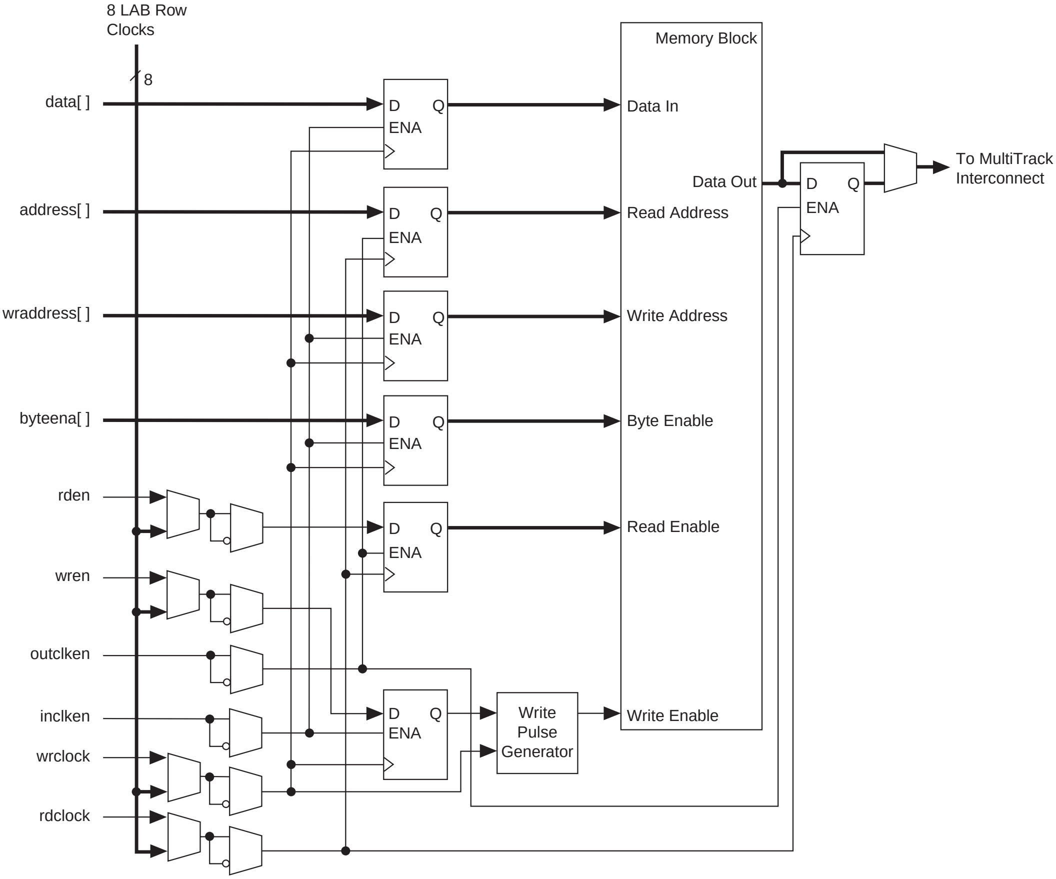
(1) The `rden` signal is not available in the M-RAM block. A M-RAM block in simple dual-port mode is always reading out the data stored at the current read address location.

(2) For more information on the MultiTrack™ interconnect, refer to Section I, Stratix Device Family Data Sheet of the *Stratix Device Handbook, Volume 1* or the *Stratix GX FPGA Family Data Sheet*.

## Read/Write Clock Mode

The TriMatrix memory blocks can implement read/write clock mode for simple dual-port memory. This mode can use up to two clocks. The write clock controls the block's data inputs, `wraddress`, and `wren`. The read clock controls the data output, `rdaddress`, and `rden`. The memory blocks support independent clock enables for each clock and asynchronous clear signals for the read- and write-side registers. Figure 3–12 shows a memory block in read/write clock mode.

***Figure 3–12. Read/Write Clock Mode in Simple Dual-Port Mode*** *Note (1)*



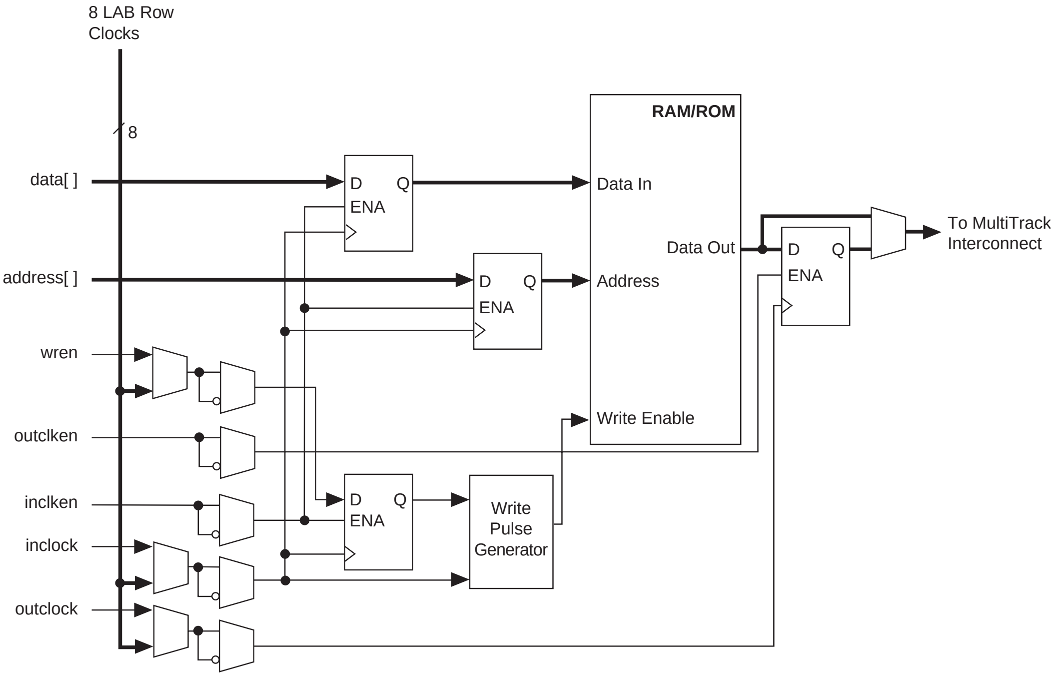
***Note to Figure 3–12:***

(1) For more information on the MultiTrack interconnect, see the Section I, Stratix Device Family Data Sheet of the *Stratix Device Handbook, Volume 1* or the *Stratix GX FPGA Family Data Sheet*.

## Single-Port Mode

The TriMatrix memory blocks can implement single-port clock mode for single-port memory mode. Single-port mode is used when simultaneous reads and writes are not required. See Figure 3–13. A single block in a memory block can support up to two single-port mode RAM blocks in M4K blocks.

***Figure 3–13. Single-Port Mode*** *Note (1)*



***Note to Figure 3–13:***

(1) For more information on the MultiTrack interconnect, refer to Section I, Stratix Device Family Data Sheet of the *Stratix Device Handbook, Volume 1* or the *Stratix GX FPGA Family Data Sheet*.

## Designing With TriMatrix Memory

When instantiating TriMatrix memory the designer must understand the various features that set it apart from other memory architectures. The following sections describe some of the important attributes and functionality of TriMatrix memory.

For information on the difference between APEX®-style memory and TriMatrix memory, refer to Chapter 12, Transitioning APEX Designs to Stratix Devices.

## Selecting TriMatrix Memory Blocks

The Quartus II software automatically partitions user-defined memory into embedded memory blocks using the most efficient size combinations. The memory can also be manually assigned to a specific block size or a mixture of block sizes. Table 3–1 on page 3–2 is a guide for selecting a TriMatrix memory block size based on supported features.

For more information on selecting which memory block to use, refer to *Application Note 207: TriMatrix Memory Selection Using the Quartus II Software*.

## Synchronous & Pseudo-Asynchronous Modes

TriMatrix memory architecture implements synchronous (pipelined) RAM by registering both the input and output signals to the RAM block. All TriMatrix memory inputs are registered providing synchronous write cycles. In synchronous operation, RAM generates its own self-timed strobe write enable (`wren`) signal derived from the global or regional clock. In contrast, a circuit using asynchronous RAM must generate the RAM `wren` signal while ensuring its data and address signals meet setup and hold time specifications relative to the `wren` signal. The output registers can be bypassed.

In an asynchronous memory neither the input nor the output is registered. While Stratix and Stratix GX devices do not support asynchronous memory, they do support a pseudo-asynchronous read where the output data is available during the clock cycle when the read address is driven into it. Pseudo-asynchronous reading is possible in the simple and true dual-port modes of the M512 and M4K blocks by clocking the read enable and read address registers on the negative clock edge and bypassing the output registers.

For more information, refer to *AN 210: Converting Memory from Asynchronous to Synchronous for Stratix & Stratix GX Devices*.

## Power-up Conditions & Memory Initialization

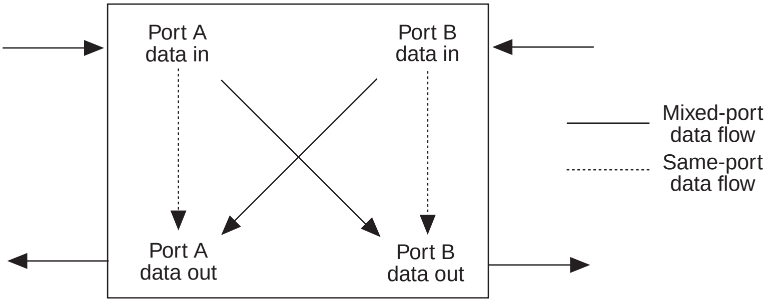
Upon power-up, TriMatrix memory is in an idle state. The M512 and M4K block outputs always power-up to zero, regardless of whether the output registers are used or bypassed. Even if a memory initialization file is used to pre-load the contents of the RAM block, the outputs will still power-up cleared. For example, if address `0` is pre-initialized to `FF`, the M512 and M4K blocks power-up with the output at `00`.

M-RAM blocks do not support memory initialization files; therefore, they cannot be pre-loaded with data upon power-up. M-RAM blocks combinatorial outputs and memory controls always power-up to an unknown state. If M-RAM block outputs are registered, the registers power-up cleared. The undefined output appears one clock cycle later. The output remains undefined until a read operation is performed on an address that has been written to.

## Read-during-Write Operation at the Same Address

The following two sections describe the functionality of the various RAM configurations when reading from an address during a write operation at that same address. There are two types of read-during-write operations: same-port and mixed-port. Figure 3–14 illustrates the difference in data flow between same-port and mixed-port read-during-write.

*Figure 3–14. Read-during-Write Data Flow*

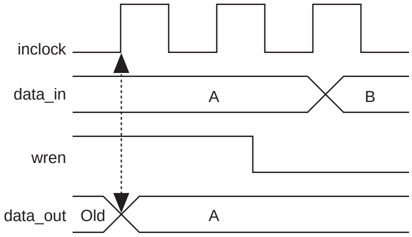


### Same-Port Read-during-Write Mode

For read-during-write operation of a single-port RAM or the same port of a true dual-port RAM, the new data is available on the rising edge of the same clock cycle it was written on. This behavior is valid on all memory-block sizes. See Figure 3–15 for a sample functional waveform.

When using byte enables in true dual-port RAM mode, the outputs for the masked bytes on the same port are unknown. (See Figure 3–1 on page 3–6.) The non-masked bytes are read out as shown in Figure 3–15.

*Figure 3–15. Same-Port Read-during-Write Functionality* Note (1)



*Note to Figure 3–15:*
(1) Outputs are not registered.

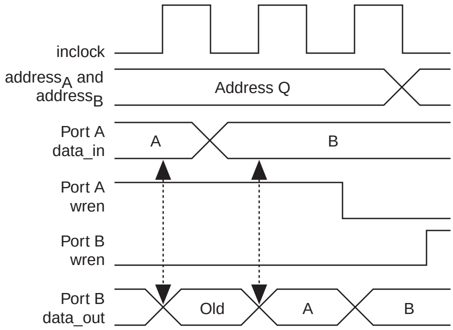
## Mixed-Port Read-during-Write Mode

This mode is used when a RAM in simple or true dual-port mode has one port reading and the other port writing to the same address location with the same clock.

The `READ_DURING_WRITE_MODE_MIXED_PORTS` parameter for M512 and M4K memory blocks determines whether to output the old data at the address or a "don't care" value. Setting this parameter to `OLD_DATA` outputs the old data at that address. Setting this parameter to `DONT_CARE` outputs a "don't care" or unknown value. See Figures 3–16 and 3–17 for sample functional waveforms showing this operation. These figures assume that the outputs are not registered.

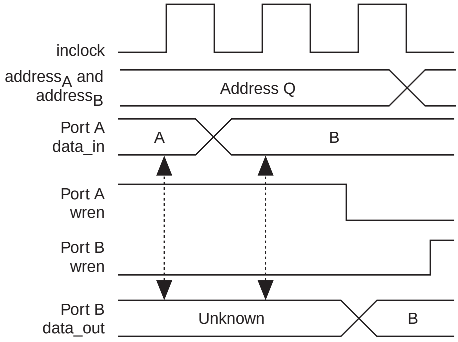
The `DONT_CARE` setting allows memory implementation in any TriMatrix memory block. The `OLD_DATA` setting restricts memory implementation to only M512 or M4K memory blocks. Selecting `DONT_CARE` gives the compiler more flexibility when placing memory functions into TriMatrix memory.

*Figure 3–16. Mixed-Port Read-during-Write: OLD_DATA*



For mixed-port read-during-write operation of the same address location of a M-RAM block, the RAM outputs are unknown, as shown in Figure 3–17.

*Figure 3–17. Mixed-Port Read-during-Write: DONT_CARE*



When two different clocks are used in a dual-port RAM, the read-during-write behavior depends on the relationship of the clocks. For the M512 and M4K blocks, the writing of the new contents starts at the falling edge of the write clock. Therefore, if the read clock's rising edge occurs at any point up to the falling edge of the write clock, the old data is read out. If the read clock's rising edge occurs between the falling edge of the write clock and half the maximum write cycle time interval, the output is unknown data.

For the maximum synchronous write cycle time refer to Section I, Stratix Device Family Data Sheet of the *Stratix Device Handbook, Volume 1* or the *Stratix GX FPGA Family Data Sheet*.

For the M-RAM block, if the read clock's rising edge occurs more than the maximum write cycle time interval after the rising edge of the write clock and the maximum write cycle time interval, the output is new data. If the read clock rising edge occurs between the rising edge of the write clock and the maximum write cycle time interval, the output is unknown data.

For the maximum synchronous write cycle time refer to Section I, Stratix Device Family Data Sheet of the *Stratix Device Handbook, Volume 1* or the *Stratix GX FPGA Family Data Sheet*.

## Conclusion

TriMatrix memory, an enhanced RAM architecture with extremely high memory bandwidth in Stratix and Stratix GX devices, gives advanced control of memory applications with features such as byte enables, parity bit storage, and shift-register mode, as well as mixed-port width support and true dual-port mode.

# Section III. I/O Standards

This section provides information on Stratix single-ended, voltage-referenced, and differential I/O standards.

It contains the following chapters:

- Chapter 4. Using Selectable I/O Standards in Stratix & Stratix GX Devices
- Chapter 5. Using High-Speed Differential I/O Interfaces in Stratix Devices

## Revision History

The table below shows the revision history for Chapters 4 and 5.

| Chapter(s) | Date / Version | Changes Made |
|---|---|---|
| 4 | April 2003<br>v1.0 | Added document to the Stratix Device Handbook. |
| 5 | May 2003<br>v1.1 | Updated high-speed I/O specifications. |
| | April 2003<br>v1.0 | New chapter in Stratix Device Handbook. |

# 4. Using Selectable I/O Standards in Stratix & Stratix GX Devices

S52004-1.0

Chapter 4, Using Selectable I/O Standards in Stratix & Stratix GX Devices replaces *AN 201: Using Selectable I/O Standardsin Stratix & Stratix GX Devices*.

## Introduction

The proliferation of I/O standards and the need for higher I/O performance have made it critical that devices have flexible I/O capabilities. Stratix™ and Stratix™ GX programmable logic devices (PLDs) feature programmable I/O pins that support a wide range of industry I/O standards, permitting increased design flexibility. These I/O capabilities enable fast time-to-market and high-performance solutions to meet the demands of complex system designs. Additionally, Stratix and Stratix GX devices simplify system board design and make it easy to connect to microprocessors, peripherals, memories, gate arrays, programmable logic circuits, and standard logic functions.

This application note provides guidelines for using one or more industry I/O standards in Stratix and Stratix GX devices, including:

- Stratix and Stratix GX I/O standards
- High speed interfaces
- Stratix and Stratix GX I/O banks
- Programmable current drive strength
- Hot socketing
- I/O termination
- I/O driver impedance matching using Terminator™ technology
- I/O pad placement guidelines
- Quartus® II software support

## Stratix & Stratix GX I/O Standards

Stratix and Stratix GX devices support a wide range of industry I/O standards as shown in Section I, Stratix Device Family Data Sheet in *Stratix Device Handbook, Volume 1* and *Stratix GX FPGA Family Data Sheet*. Several applications that use these I/O standards are listed in Table 4–1.

**Table 4–1. I/O Standard Applications & Data Rates (Part 1 of 2)**

| I/O Standard | Application | Data Rate |
|---|---|---|
| 3.3-V LVTTL/LVCMOS | General purpose | - |
| 2.5-V LVTTL/LVCMOS | General purpose | - |

*Table 4–1. I/O Standard Applications & Data Rates (Part 2 of 2)*

| I/O Standard | Application | Data Rate |
|---|---|---|
| 1.8-V LVTTL/LVCMOS | General purpose | - |
| 1.5-V LVCMOS | General purpose | - |
| PCI/PCIX/Compact PCI | PC/embedded systems | 66 to 133 MHz |
| AGP 1× and 2× | Graphics processors | 66 to 133 MHz |
| SSTL-3 class I and II | SDRAM | 166 MHz |
| SSTL-2 class I and II | DDR I SDRAM | 160 to 400 Mbps |
| SSTL-18 class I and II | DDR II SDRAM | 160 to 400 Mbps |
| HSTL class I and II | QDR SRAM/SRAM/CSIX | 150 to 250 MHz |
| Differential HSTL | Clock interfaces | 150 to 250 MHz |
| GTL | Backplane driver | 100 MHz |
| GTL+ | Pentium processor interface | 133 MHz to 200 MHz |
| LVDS | Communications | 840 Mbps |
| HyperTransport technology | Motherboard interfaces | 800 Mbps |
| LVPECL | PHY interface | 840 Mbps |
| PCML | Communications | 840 Mbps |
| Differential SSTL-2 | DDR I SDRAM | 160 to 400 Mbps |
| CTT | JEDEC standard | - |

## 3.3-V Low Voltage Transistor-Transistor Logic (LVTTL) - EIA/JEDEC Standard JESD8-B

The 3.3-V LVTTL I/O standard is a general-purpose, single-ended standard used for 3.3-V applications. The LVTTL standard defines the DC interface parameters for digital circuits operating from a 3.0-V or 3.3-V power supply and driving or being driven by LVTTL-compatible devices.

The LVTTL input standard specifies a wider input voltage range of $-0.3\text{ V} \leq V_I \leq 3.9\text{ V}$. Altera allows an input voltage range of $-0.5\text{ V} \leq V_I \leq 4.1\text{ V}$. The LVTTL standard does not require input reference voltages or board terminations.

Stratix and Stratix GX devices support both input and output levels for 3.3-V LVTTL operation.

## 3.3-V Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS) - EIA/JEDEC Standard JESD8-B

The 3.3-V LVCMOS I/O standard is a general-purpose, single-ended standard used for 3.3-V applications. The LVCMOS standard defines the DC interface parameters for digital circuits operating from a 3.0-V or 3.3-V power supply and driving or being driven by LVCMOS-compatible devices.

The LVCMOS standard specifies the same input voltage requirements as LVTTL ($-0.3 \text{ V} \leq V_I \leq 3.9 \text{ V}$). The output buffer drives to the rail to meet the minimum high-level output voltage requirements. The 3.3-V I/O standard does not require input reference voltages or board terminations.

Stratix and Stratix GX devices support both input and output levels for 3.3-V LVCMOS operation.

## 2.5-V LVTTL Normal & Wide Voltage Ranges - EIA/JEDEC Standard EIA/JESD8-5

The 2.5-V I/O standard is used for 2.5-V LVTTL applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 2.5-V devices. The input and output voltage ranges are:

- The 2.5-V normal and wide range input standards specify an input voltage range of $-0.3 \text{ V} \leq V_I \leq 3.0 \text{ V}$.
- The normal range minimum high-level output voltage requirement ($V_{OH}$) is 2.1 V.
- The wide range minimum high-level output voltage requirement ($V_{OH}$) is $V_{CCIO} - 0.2$ V.

Stratix and Stratix GX devices support both input and output levels for 2.5-V LVTTL operation.

## 2.5-V LVCMOS Normal & Wide Voltage Ranges - EIA/JEDEC Standard EIA/JESD8-5

The 2.5-V I/O standard is used for 2.5-V LVCMOS applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 2.5-V parts. The input and output voltage ranges are:

- The 2.5-V normal and wide range input standards specify an input voltage range of $-0.3\text{ V} \leq V_I \leq 3.0\text{ V}$.
- The normal range minimum $V_{OH}$ requirement is 2.1 V.
- The wide range minimum $V_{OH}$ requirement is $V_{CCIO} - 0.2\text{ V}$.

Stratix and Stratix GX devices support both input and output levels for 2.5-V LVCMOS operation.

## 1.8-V LVTTL Normal & Wide Voltage Ranges - EIA/JEDEC Standard EIA/JESD8-7

The 1.8-V I/O standard is used for 1.8-V LVTTL applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 1.8-V parts. The input and output voltage ranges are:

- The 1.8-V normal and wide range input standards specify an input voltage range of $-0.3\text{ V} \leq V_I \leq 2.25\text{ V}$.
- The normal range minimum $V_{OH}$ requirement is $V_{CCIO} - 0.45\text{ V}$.
- The wide range minimum $V_{OH}$ requirement is $V_{CCIO} - 0.2\text{ V}$.

Stratix and Stratix GX devices support both input and output levels for 1.8-V LVTTL operation.

## 1.8-V LVCMOS Normal & Wide Voltage Ranges - EIA/JEDEC Standard EIA/JESD8-7

The 1.8-V I/O standard is used for 1.8-V LVCMOS applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 1.8-V devices. The input and output voltage ranges are:

- The 1.8-V normal and wide range input standards specify an input voltage range of $-0.3\text{ V} \leq V_I \leq 2.25\text{ V}$.
- The normal range minimum $V_{OH}$ requirement is $V_{CCIO} - 0.45\text{ V}$.
- The wide range minimum $V_{OH}$ requirement is $V_{CCIO} - 0.2\text{ V}$.

Stratix and Stratix GX devices support both input and output levels for 1.8-V LVCMOS operation.

## 1.5-V LVCMOS Normal & Wide Voltage Ranges - EIA/JEDEC Standard JESD8-11

The 1.5-V I/O standard is used for 1.5-V applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 1.5-V devices. The input and output voltage ranges are:

- The 1.5-V normal and wide range input standards specify an input voltage range of $-0.3\text{ V} \leq V_I \leq 1.9\text{ V}$.
- The normal range minimum $V_{OH}$ requirement is 1.05 V.
- The wide range minimum $V_{OH}$ requirement is $V_{CCIO} - 0.2\text{ V}$.

Stratix and Stratix GX devices support both input and output levels for 1.5-V LVCMOS operation.

## 1.5-V High Speed Transceiver Logic (HSTL) Class I & II - EIA/JEDEC Standard EIA/JESD8-6

The HSTL I/O standard is used for applications designed to operate in the 0.0- to 1.5-V HSTL logic switching range. This standard defines single ended input and output specifications for all HSTL-compliant digital integrated circuits. The single ended input standard specifies an input voltage range of $-0.3\text{ V} \leq V_I \leq V_{CCIO} + 0.3\text{ V}$. Stratix and Stratix GX devices support both input and output levels specified by the 1.5-V HSTL I/O standard. Additionally, the 1.5-V HSTL I/O standard in Stratix and Stratix GX devices is compatible with the 1.8-V HSTL I/O standard in APEX™ 20KE and APEX 20KC devices because the input and output voltage thresholds are compatible. See Figures 4–1 and 4–2. Stratix and Stratix GX devices support both input and output levels with $V_{REF}$ and $V_{TT}$.

*Figure 4–1. HSTL Class I Termination*

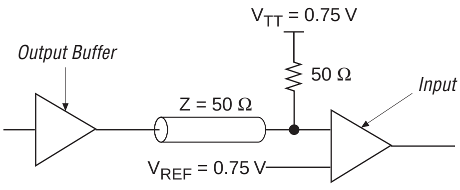
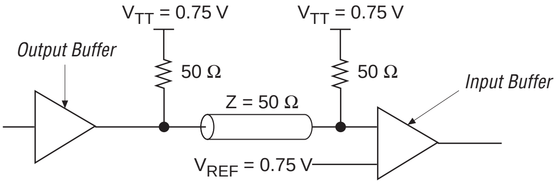


*Figure 4–2. HSTL Class II Termination*



## 1.5-V Differential HSTL - EIA/JEDEC Standard EIA/JESD8-6

The differential HSTL I/O standard is used for applications designed to operate in the 0.0- to 1.5-V HSTL logic switching range such as quad data rate (QDR) memory clock interfaces. The differential HSTL specification is the same as the single ended HSTL specification. The standard specifies an input voltage range of $-0.3\text{ V} \leq V_I \leq V_{CCIO} + 0.3\text{ V}$. Differential HSTL does not require an input reference voltage, however, it does require a 50-Ω termination resistor to $V_{TT}$ at the input buffer (see Figures 4–3 and 4–4). Stratix and Stratix GX devices support both input and output clock levels for 1.5-V differential HSTL.

*Figure 4–3. 1.5-V HSTL Class I Differential Termination*

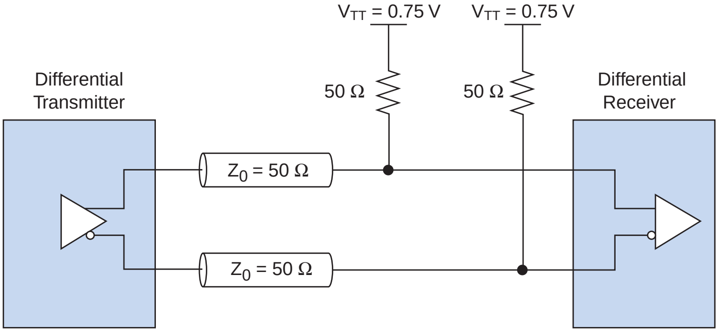
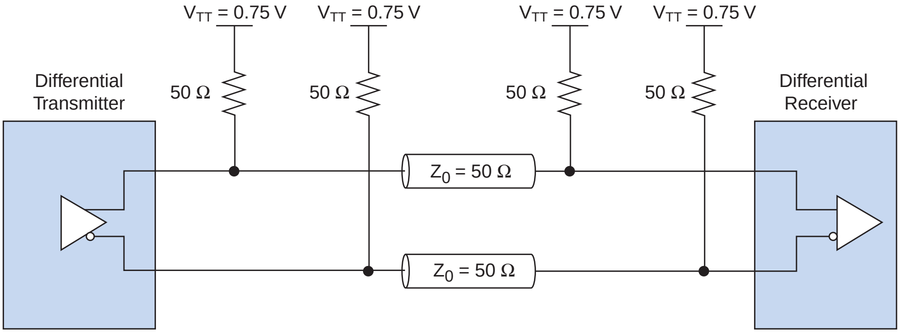


*Figure 4–4. 1.5-V HSTL Class II Differential Termination*



## 3.3-V PCI – PCI Local Bus - PCI Special Interest Group (SIG) PCI Local Bus Specification Revision 2.2

The PCI local bus specification is used for applications that interface to the PCI local bus, which provides a processor-independent data path between highly integrated peripheral controller components, peripheral add-in boards, and processor/memory systems. The conventional PCI specification revision 2.2 defines the PCI hardware environment including the protocol, electrical, mechanical, and configuration specifications for the PCI devices and expansion boards. This standard requires 3.3-V $V_{CCIO}$. Stratix and Stratix GX devices are fully compliant with the 3.3-V *PCI Local Bus Specification Revision 2.2* and meet 64-bit/66-MHz operating frequency and timing requirements. The 3.3-V PCI standard does not require input reference voltages or board terminations. Stratix and Stratix GX devices support both input and output levels.

## 3.3-V PCI-X Local Bus - PCI-SIG PCI-X Local Bus Specification Revision 1.0a

The PCI-X 1.0 standard is used for applications that interface to the PCI local bus. The standard enables the design of systems and devices that operate at clock speeds up to 133 MHz, or 1 gigabit per second (Gbps) for a 64-bit bus. The PCI-X 1.0 protocol enhancements enable devices to operate much more efficiently, providing more usable bandwidth at any clock frequency. By using the PCI-X 1.0 standard, devices can be designed to meet PCI-X 1.0 requirements and operate as conventional 33- and 66-MHz PCI devices when installed in those systems. This standard requires 3.3-V $V_{CCIO.}$ Stratix and Stratix GX devices are fully compliant with the 3.3-V *PCI-X Specification Revision 1.0a* and meet the 133-MHz operating frequency and timing requirements. The 3.3-V PCI standard does not require input reference voltages or board terminations. Stratix and Stratix GX devices support both input and output levels.

## 3.3-V Compact PCI Bus - PCI SIG PCI Local Bus Specification Revision 2.2

The Compact PCI local bus specification is used for applications that interface to the PCI local bus. It follows the *PCI Local Bus Specification Revision 2.2* plus additional requirements and a hotswap specification. This standard has similar electrical requirements as LVTTL and requires 3.3-V $V_{CCIO.}$ Stratix and Stratix GX devices are compliant with the Compact PCI electrical requirements. The 3.3-V PCI standard does not require input reference voltages or board terminations. Stratix and Stratix GX devices support both input and output levels.

## 3.3-V 1× AGP - Intel Corporation Accelerated Graphics Port Interface Specification 2.0

The AGP interface is a platform bus specification that enables high-performance graphics by providing a dedicated high-speed port for the movement of large blocks of 3-dimensional texture data between a PC's graphics controller and system memory. The 1× AGP I/O standard is a single-ended standard used for 3.3-V graphics applications. The 1× AGP input standard specifies an input voltage range of $-0.5\text{ V} \leq V_I \leq V_{CCIO} + 0.5\text{ V}$. The 1× AGP standard does not require input reference voltages or board terminations. Stratix and Stratix GX devices support both input and output levels.

## 3.3-V 2× AGP - Intel Corporation Accelerated Graphics Port Interface Specification 2.0

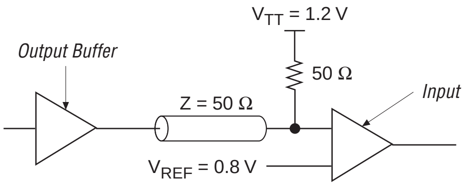
The 2× AGP I/O standard is a voltage-referenced, single-ended standard used for 3.3-V graphics applications. The 2× AGP input standard specifies an input voltage range of $-0.5\text{V} \leq V_I \leq V_{CCIO} + 0.5\text{V}$. The 2× AGP standard does not require board terminations. Stratix and Stratix GX devices support both input and output levels.

## GTL - EIA/JEDEC Standard EIA/JESD8-3

The GTL I/O standard is a low-level, high-speed back plane standard used for a wide range of applications from ASICs and processors to interface logic devices. The GTL standard defines the DC interface parameters for digital circuits operating from power supplies of 2.5, 3.3, and 5.0 V. The GTL standard is an open-drain standard, and Stratix and Stratix GX devices support a 2.5- or 3.3-V $V_{CCIO}$ to meet this standard.

GTL requires a 0.8-V $V_{REF}$ and open-drain outputs with a 1.2-V $V_{TT}$ to which the reference voltage tracks (see Figure 4–5). Stratix and Stratix GX devices support both input and output levels.

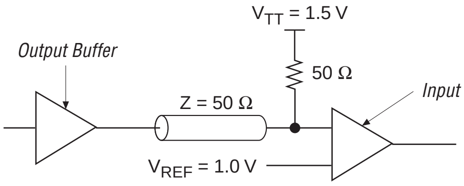
*Figure 4–5. GTL Termination*



## GTL+

The GTL+ I/O standard is used for high-speed back plane drivers and Pentium processor interfaces. The GTL+ standard defines the DC interface parameters for digital circuits operating from power supplies of 2.5, 3.3, and 5.0 V. The GTL+ standard is an open-drain standard, and Stratix and Stratix GX devices support a 2.5- or 3.3-V $V_{CCIO}$ to meet this standard. GTL+ requires a 1.0-V $V_{REF}$ and open-drain outputs with a 1.5-V $V_{TT}$ to which the reference voltage tracks (see Figure 4–6). Stratix and Stratix GX devices support both input and output levels.

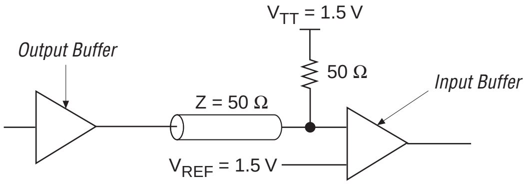
*Figure 4–6. GTL+ Termination*



## CTT - EIA/JEDEC Standard JESD8-4

The CTT I/O standard is used for backplanes and memory bus interfaces. The CTT standard defines the DC interface parameters for digital circuits operating from 2.5- and 3.3-V power supplies. The CTT standard does not require special circuitry to interface with LVTTL or LVCMOS devices when the CTT driver is not terminated. The CTT standard requires a 1.5-V $V_{REF}$ and a 1.5-V $V_{TT}$ (see Figure 4–7). Stratix and Stratix GX devices support both input and output levels.

*Figure 4–7. CTT Termination*



## SSTL-3 Class I & II - EIA/JEDEC Standard JESD8-8

The SSTL-3 I/O standard is a 3.3-V memory bus standard used for applications such as high-speed SDRAM interfaces. This standard defines the input and output specifications for devices that operate in the SSTL-3 logic switching range of 0.0 to 3.3 V. The SSTL-3 standard specifies an input voltage range of $-0.3\text{ V} \leq V_I \leq V_{CCIO} + 0.3\text{ V}$. SSTL-3 requires a 1.5-V $V_{REF}$ and a 1.5-V $V_{TT}$ to which the series and termination resistors are connected (see Figures 4–8 and 4–9). In typical applications, both the termination voltage and reference voltage track the output supply voltage. Stratix and Stratix GX devices support both input and output levels.

*Figure 4–8. SSTL-3 Class I Termination*

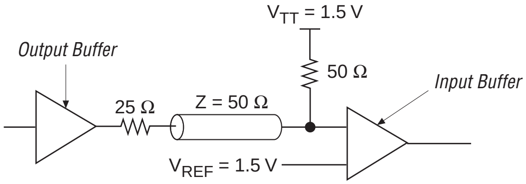
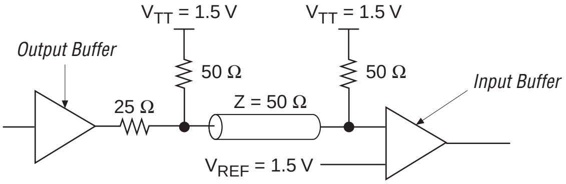


*Figure 4–9. SSTL-3 Class II Termination*



## SSTL-2 Class I & II - EIA/JEDEC Standard JESD8-9A

The SSTL-2 I/O standard is a 2.5-V memory bus standard used for applications such as high-speed DDR SDRAM interfaces. This standard defines the input and output specifications for devices that operate in the SSTL-2 logic switching range of 0.0 to 2.5 V. This standard improves operation in conditions where a bus must be isolated from large stubs. The SSTL-2 standard specifies an input voltage range of $-0.3\text{ V} \leq V_I \leq V_{CCIO} + 0.3\text{ V}$. SSTL-2 requires a 1.25-V $V_{REF}$ and a 1.25-V $V_{TT}$ to which the series and termination resistors are connected (see Figures 4–10 and 4–11). Stratix and Stratix GX devices support both input and output levels.

*Figure 4–10. SSTL-2 Class I Termination*

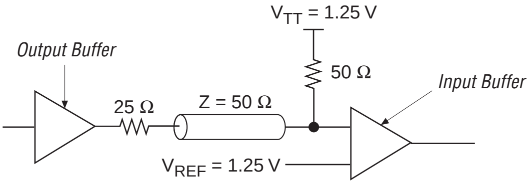
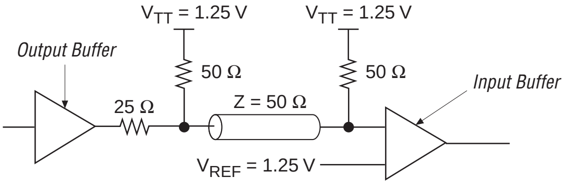


*Figure 4–11. SSTL-2 Class II Termination*



## SSTL-18 Class I & II - EIA/JEDEC Preliminary Standard JC42.3

The SSTL-18 I/O standard is a 1.8-V memory bus standard used for applications such as high-speed DDR II SDRAM interfaces. This standard is similar to SSTL-2 and defines input and output specifications for devices that are designed to operate in the SSTL-18 logic switching range 0.0 to 1.8 V. SSTL-18 requires a 0.9-V $V_{REF}$ and a 0.9-V $V_{TT}$ to which the series and termination resistors are connected. See Figures 4–12 and 4–13 for details on SSTL-18 class I and II termination. Stratix and Stratix GX devices support both input and output levels.

*Figure 4–12. SSTL-18 Class I Termination*

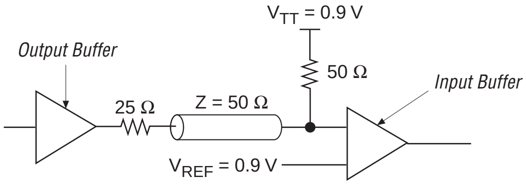
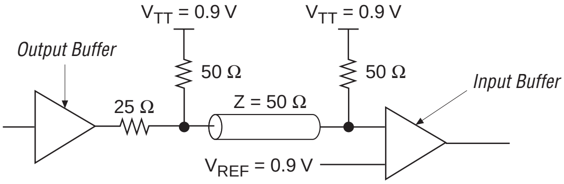


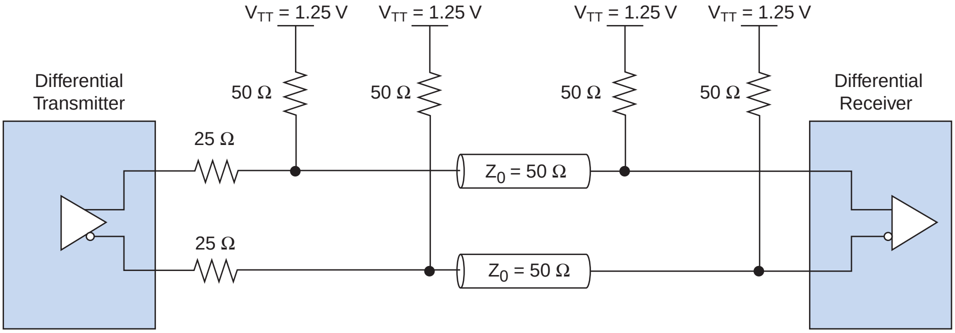
*Figure 4–13. SSTL-18 Class II Termination*



## Differential SSTL-2 - EIA/JEDEC Standard JESD8-9A

The differential SSTL-2 I/O standard is a 2.5-V standard used for applications such as high-speed DDR SDRAM clock interfaces. This standard supports differential signals in systems using the SSTL-2 standard and supplements the SSTL-2 standard for differential clocks. The differential SSTL-2 standard specifies an input voltage range of $-0.3 \text{ V} \leq V_I \leq V_{CCIO} + 0.3 \text{ V}$. The differential SSTL-2 standard does not require an input reference voltage differential. See Figure 4–14 for details on differential SSTL-2 termination. Stratix and Stratix GX devices support output clock levels for differential SSTL-2 class II operation.

*Figure 4–14. SSTL-2 Class II Differential Termination*



## LVDS - ANSI/TIA/EIA Standard ANSI/TIA/EIA-644

The LVDS I/O standard is a differential high-speed, low-voltage swing, low-power, general-purpose I/O interface standard requiring a 3.3-V $V_{CCIO}$. This standard is used in applications requiring high-bandwidth data transfer, backplane drivers, and clock distribution. The ANSI/TIA/EIA-644 standard specifies LVDS transmitters and receivers capable of operating at recommended maximum data signaling rates of 655 Mbps. However, devices can operate at slower speeds if needed, and there is a theoretical maximum of 1.923 Gbps. Stratix and Stratix GX devices meet the ANSI/TIA/EIA-644 standard.

Due to the low voltage swing of the LVDS I/O standard, the electromagnetic interference (EMI) effects are much smaller than CMOS, TTL, and PECL. This low EMI makes LVDS ideal for applications with low EMI requirements or noise immunity requirements. The LVDS standard does not require an input reference voltage, however, it does require a 100-Ω termination resistor between the two signals at the input buffer. Stratix and Stratix GX devices include an optional 100-Ω differential LVDS termination resistor within the device using Terminator technology. Stratix and Stratix GX devices support both input and output levels.

For more information on the LVDS I/O standard in Stratix devices, see Chapter 5, Using High-Speed Differential I/O Interfaces in Stratix Devices.

## LVPECL

The LVPECL I/O standard is a differential interface standard requiring a 3.3-V $V_{CCIO.}$ The standard is used in applications involving video graphics, telecommunications, data communications, and clock distribution. The high-speed, low-voltage swing LVPECL I/O standard uses a positive power supply and is similar to LVDS, however, LVPECL has a larger differential output voltage swing than LVDS. The LVPECL standard does not require an input reference voltage, but it does require a 100-Ω termination resistor between the two signals at the input buffer. See Figures 4–15 and 4–16 for two alternate termination schemes for LVPECL. Stratix and Stratix GX devices support both input and output levels.

*Figure 4–15. LVPECL DC Coupled Termination*

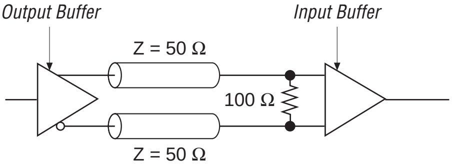
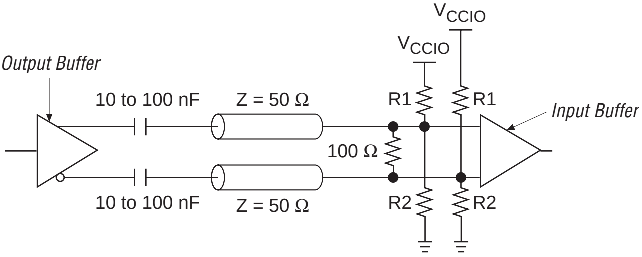


*Figure 4–16. LVPECL AC Coupled Termination*

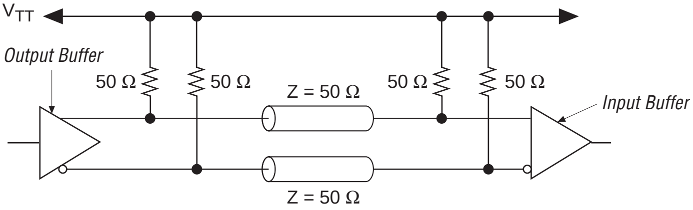


## Pseudo Current Mode Logic (PCML)

The PCML I/O standard is a differential high-speed, low-power I/O interface standard used in applications such as networking and telecommunications. The standard requires a 3.3-V $V_{CCIO}$. The PCML I/O standard consumes less power than the LVPECL I/O standard. The PCML standard is similar to LVPECL, but PCML has a reduced voltage swing, which allows for a faster switching time and lower power consumption. The PCML standard uses open drain outputs and requires a differential output signal. See Figure 4–17 for details on PCML termination. Stratix and Stratix GX devices support both input and output levels.

Additionally, Stratix GX devices support 1.5-V PCML as described in the *Stratix GX FPGA Family Data Sheet*.

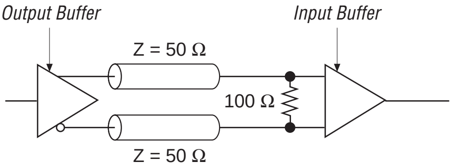
*Figure 4–17. PCML Termination*



## HyperTransport Technology - HyperTransport Consortium

The HyperTransport technology I/O standard is a differential high-speed, high-performance I/O interface standard requiring a 2.5-V VCCIO. This standard is used in applications such as high-performance networking, telecommunications, embedded systems, consumer electronics, and Internet connectivity devices. The HyperTransport technology I/O standard is a point-to-point standard in which each HyperTransport technology bus consists of two point-to-point unidirectional links. Each link is 2 to 32 bits. The HyperTransport technology standard does not require an input reference voltage. However, it does require a 100-Ω termination resistor between the two signals at the input buffer. See Figure 4–18 for details on HyperTransport technology termination. Stratix and Stratix GX devices support both input and output levels.

*Figure 4–18. HyperTransport Technology Termination*



See Section I, Stratix Device Family Data Sheet in *Stratix Device Handbook, Volume 1*; the *Stratix GX FPGA Family Data Sheet*; and Chapter 5, Using High-Speed Differential I/O Interfaces in Stratix Devices for more information on differential I/O standards.

## High Speed Interfaces

In addition to current industry physical I/O standards, Stratix and Stratix GX devices also support a variety of emerging high-speed interfaces. This section provides an overview of these interfaces.

### POS-PHY 4 System Packet Interface Level 4 (SPI-4) – OC-192 Phase 2- Optical Internetworking Forum (OIF) Standard OIF-SPI4-02.0

The POS-PHY Level 4: SPI-4 interface standard is an industry-wide standard used for OC-192 and 10-Gbps multi-service system interfaces. SONET and SDH are synchronous transmission systems over which data packets are transferred. POS-PHY Level 4 is a standard interface for switches and routers, and defines the operation between a physical layer (PHY) device and link layer devices (ATM, Internet protocol, and Gigabit Ethernet) for bandwidths of OC-192 ATM, POS, and 10-Gigabit Ethernet applications. Some key POS-PHY Level 4 system features include:

- Large selection of POS-PHY Level 4-based PHYs
- Independent of data protocol
- Wide industry support
- LVDS I/O standard to improve signal integrity
- Inband addressing/control
- Out of band flow control
- Scalable architecture
- Over 622-Mbps operation
- Dynamic interface timing mode

POS-PHY Level 4 operates at a wide range of frequencies.

### POS-PHY 4: SERDES-Framer Interface Level 4 (SFI-4) – OC-192 - Optical Internetworking Forum (OIF) Standard OIF-SFI4-01.0

The POS-PHY Level 4: SFI-4 interface standard is an industry-wide standard used for OC-192 and 10-Gbps multi-service system interfaces. The POS-PHY Level 4 interface standard defines the SFI-4 standard. POS-PHY Level 4: SFI-4 is a standardized 16-bit × 622-Mbps line-side interface for 10-Gbps applications. Internet LAN and WAN architectures use telecommunication SONET protocols for data transferring data over the PHY layer. SFI-4 interfaces between OC-192 SERDES and SONET framers.

## 10 Gigabit Ethernet Sixteen Bit Interface (XSBI) - IEEE Draft Standard P802.3ae/D2.0

10 Gigabit Ethernet XSBI is an interface standard for LANs, metropolitan area networks (MANs), storage area networks (SANs), and WANs. 10 Gigabit Ethernet XSBI provides many features for efficient, effective high-speed networking, including easy migration to higher performance levels without disruption, lower cost of ownership including acquisition and support versus other alternatives, familiar management tools and common skills, ability to support new applications and data protocols, flexibility in network design, and multiple vendor sourcing and interoperability.

Under the ISO Open Systems Interconnection (OSI) model, Ethernet is a Layer 2 protocol. 10 Gigabit Ethernet XSBI uses the IEEE 802.3 Ethernet media access control (MAC) protocol, Ethernet frame format, and the minimum/maximum frame size. An Ethernet PHY corresponding to OSI layer 1 connects the media to the MAC layer that corresponds to OSI layer 2. The PHY is divided into a physical media dependent (PMD) element, such as optical transceivers, and a physical coding sub-layer (PCS), which has coding and a serializer/multiplexor. This standard defines two PHY types, including the LAN PHY and the WAN PHY, which are distinguished by the PCS. The 10 Gigabit Ethernet XSBI standard is a full-duplex technology standard that can increase the speed and distance of Ethernet.

## RapidIO Interconnect Specification - RapidIO Committee RapidIO Interconnect Specification Revision 1.1

The RapidIO interface is a communications standard used to connect devices on a circuit board and circuit boards on a backplane. RapidIO is a packet-switched interconnect standard designed for embedded systems such as those used in networking and communications. The RapidIO interface standard is a high-performance interconnect interface used for transferring data and control information between microprocessors, DSPs, system memory, communications and network processors, and peripheral devices in a system.

RapidIO replaces existing peripheral bus and processor technologies such as PCI. Some features of RapidIO include multiprocessing support, an open standard, flexible topologies, higher bandwidth, low latency, error management support in hardware, small silicon footprint, widely available process and I/O technologies, and transparency to existing applications and operating system software. The RapidIO standard provides 10-Gbps device bandwidth using 8-bit-wide input and output data ports. RapidIO uses LVDS technology, has the capability to be scaled to multi-GHz frequencies, and features a 10-bit interface.

### HyperTransport Technology - HyperTransport Consortium

The HyperTransport technology I/O standard is a differential high speed, high performance I/O interface standard developed for communications and networking chip-to-chip communications. HyperTransport technology is used in applications such as high-performance networking, telecommunications, embedded systems, consumer electronics, and Internet connectivity devices. The HyperTransport technology I/O standard is a point-to-point (one source connected to exactly one destination) standard that provides a high-performance interconnect between integrated circuits in a system, such as on a motherboard.

Using the maximum rate of HyperTransport technology at 1.6 Gbps and 32 bits in each direction, the effective bandwidth of HyperTransport supports 12.8 Gbps. HyperTransport technology uses an enhanced differential signaling technology to improve performance. HyperTransport technology supports data widths of 2, 4, 8, 16, or 32 bits in each direction. HyperTransport technology in Stratix and Stratix GX devices operates at multiple clock speeds up to 800 MHz.

### UTOPIA Level 4 – ATM Forum Technical Committee Standard AF-PHY-0144.001

The UTOPIA Level 4 frame-based interface standard allows device manufacturers and network developers to develop components that can operate at data rates up to 10 Gbps. This standard increases interface speeds using LVDS I/O and advanced silicon technologies for fast data transfers.

UTOPIA Level 4 provides new control techniques and a 32-, 16-, or 8-bit LVDS bus, a symmetric transmit/receive bus structure for easier application design and testability, nominal data rates of 10 Gbps, in-band control of cell delimiters and flow control to minimize pin count, source-synchronous clocking, and supports variable length packet systems. UTOPIA Level 4 handles sustained data rates for OC-192 and supports ATM cells. UTOPIA Level 4 also supports interconnections across motherboards, daughtercards, and backplane interfaces.

## Stratix & Stratix GX I/O Banks

Stratix devices have eight I/O banks in addition to the four enhanced PLL external clock output banks, as shown in Table 4–2 and Figure 4–19. I/O banks 3, 4, 7, and 8 support all single-ended I/O standards. I/O banks 1, 2, 5, and 6 support differential HSTL (on input clocks), LVDS, LVPECL, PCML, and HyperTransport technology, as well as all single-ended I/O standards except HSTL class II, GTL, SSTL-18 class II, PCI/PCI-X 1.0, and 1×/2× AGP. The four enhanced PLL external clock output banks (I/O banks 9, 10, 11, and 12) support clock outputs all single-ended I/O standards in addition to differential SSTL-2 and HSTL (both on the output clock only). Since Stratix devices support both non-voltage-referenced and voltage-referenced I/O standards, there are different guidelines when working with either separately or when working with both.

*Table 4–2. I/O Standards Supported in Stratix I/O Banks (Part 1 of 2)*

| I/O Standard | I/O Bank | | | | | | | | Enhanced PLL External Clock Output Banks | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
| 3.3-V LVTTL/LVCMOS | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| 2.5-V LVTTL/LVCMOS | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| 1.8-V LVTTL/LVCMOS | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| 1.5-V LVCMOS | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| PCI/PCIX//Compact PCI | | | ✓ | ✓ | | | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| AGP 1× | | | ✓ | ✓ | | | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| AGP 2× | | | ✓ | ✓ | | | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| SSTL-3 class I | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| SSTL-3 class II | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| SSTL-2 class I | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| SSTL-2 class II | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| SSTL-18 class I | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| SSTL-18 class II | | | ✓ | ✓ | | | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Differential SSTL-2 (output clocks) | | | | | | | | | ✓ | ✓ | ✓ | ✓ |
| HSTL class I | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| HSTL class II | | | ✓ | ✓ | | | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Differential HSTL (input clocks) | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | | |
| Differential HSTL (output clocks) | | | | | | | | | ✓ | ✓ | ✓ | ✓ |
| GTL | | | ✓ | ✓ | | | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| GTL+ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| CTT | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

*Table 4–2. I/O Standards Supported in Stratix I/O Banks (Part 2 of 2)*

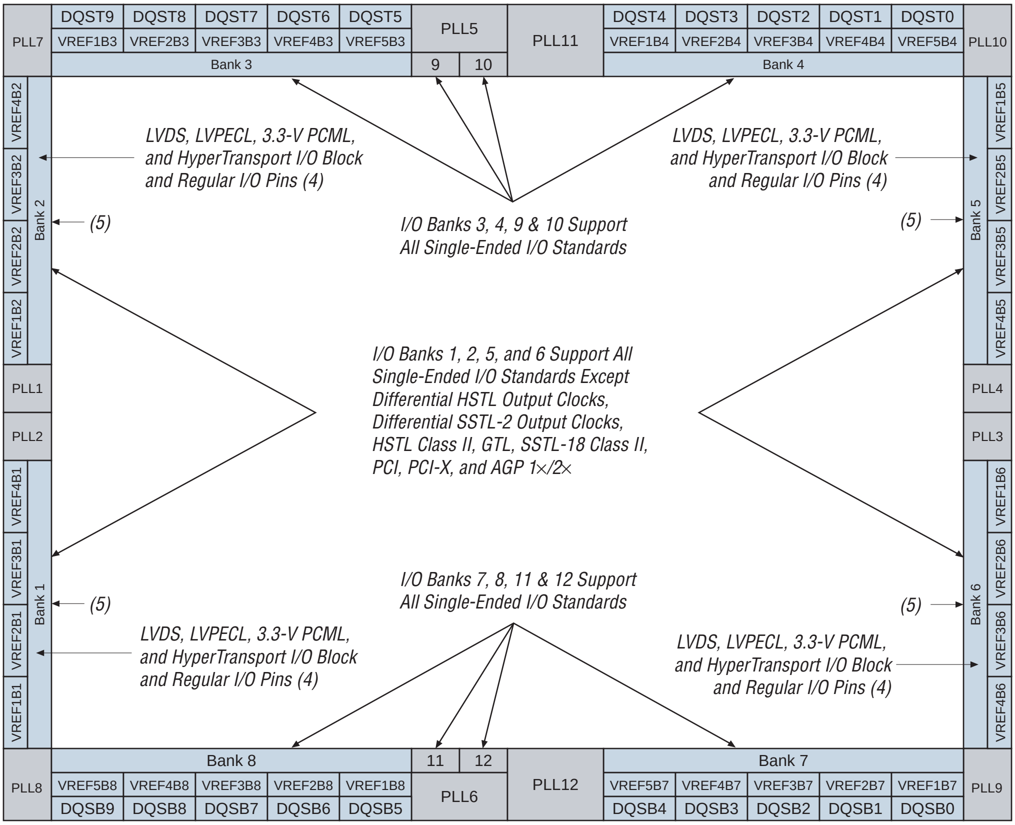
| I/O Standard | I/O Bank | | | | | | | | Enhanced PLL External Clock Output Banks | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
| LVDS | ✓ | ✓ | *(1)* | *(1)* | ✓ | ✓ | *(1)* | *(1)* | *(2)* | *(2)* | *(2)* | *(2)* |
| HyperTransport technology | ✓ | ✓ | *(1)* | *(1)* | ✓ | ✓ | *(1)* | *(1)* | *(2)* | *(2)* | *(2)* | *(2)* |
| LVPECL | ✓ | ✓ | *(1)* | *(1)* | ✓ | ✓ | *(1)* | *(1)* | *(2)* | *(2)* | *(2)* | *(2)* |
| PCML | ✓ | ✓ | *(1)* | *(1)* | ✓ | ✓ | *(1)* | *(1)* | *(2)* | *(2)* | *(2)* | *(2)* |

***Notes to Table 4–2:***

(1) This I/O standard is only supported on input clocks in this I/O bank.

(2) This I/O standard is only supported on output clocks in this I/O bank.

**Figure 4–19. Stratix I/O Banks** *Notes (1), (2), (3)*



*Notes to Figure 4–19:*

(1) Figure 4–19 is a top view of the silicon die. This will correspond to a top-down view for non-flip-chip packages, but will be a reverse view for flip-chip packages.

(2) Figure 4–19 is a graphic representation only. Refer to the pin list and the Quartus II software for exact locations.

(3) Banks 9 through 12 are enhanced PLL external clock output banks.

(4) If the high-speed differential I/O pins are not used for high-speed differential signaling, they can support all of the I/O standards except HSTL class I and II, GTL, SSTL-18 Class II, PCI, PCI-X, and AGP 1×/2×.

(5) You can only place single-ended input pads four or more pads away from a differential pad. You can only place single-ended output/bidirectional pads five or more pads away from a differential pad. Use the Show Pads view in the Quartus II Floorplan Editor to locate these pads. The Quartus II software will give an error message for illegal output or bidirectional pin placement next to a high-speed differential I/O pin.

Tables 4–3 and 4–4 list the I/O standards that Stratix GX enhanced and fast PLL pins support. Figure 4–20 shows the I/O standards that each Stratix GX I/O bank supports.

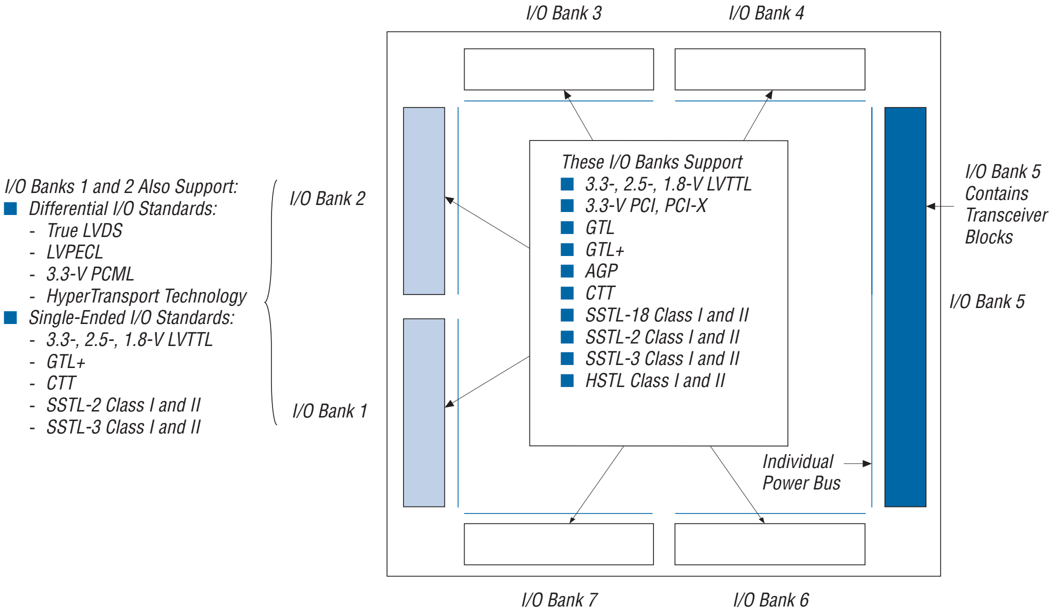
*Table 4–3. I/O Standards Supported in Stratix GX Enhanced PLL Pins*

| I/O Standard | Input | | | Output |
|---|---|---|---|---|
| | INCLK | FBIN | PLLENABLE | EXTCLK |
| LVTTL | ✓ | ✓ | ✓ | ✓ |
| LVCMOS | ✓ | ✓ | ✓ | ✓ |
| 2.5 V | ✓ | ✓ | | ✓ |
| 1.8 V | ✓ | ✓ | | ✓ |
| 1.5 V | ✓ | ✓ | | ✓ |
| 3.3-V PCI | ✓ | ✓ | | ✓ |
| 3.3-V PCI-X | ✓ | ✓ | | ✓ |
| LVPECL | ✓ | ✓ | | ✓ |
| 3.3-V PCML | ✓ | ✓ | | ✓ |
| LVDS | ✓ | ✓ | | ✓ |
| HyperTransport technology | ✓ | ✓ | | ✓ |
| Differential HSTL | ✓ | | | ✓ |
| Differential SSTL | | | | ✓ |
| 3.3-V GTL | ✓ | ✓ | | ✓ |
| 3.3-V GTL+ | ✓ | ✓ | | ✓ |
| 1.5-V HSTL class I | ✓ | ✓ | | ✓ |
| 1.5-V HSTL class II | ✓ | ✓ | | ✓ |
| SSTL-18 class I | ✓ | ✓ | | ✓ |
| SSTL-18 class II | ✓ | ✓ | | ✓ |
| SSTL-2 class I | ✓ | ✓ | | ✓ |
| SSTL-2 class II | ✓ | ✓ | | ✓ |
| SSTL-3 class I | ✓ | ✓ | | ✓ |
| SSTL-3 class II | ✓ | ✓ | | ✓ |
| AGP (1× and 2×) | ✓ | ✓ | | ✓ |
| CTT | ✓ | ✓ | | ✓ |

*Table 4–4. I/O Standards Supported in Stratix GX Fast PLL Pins*

| I/O Standard | Input | |
|---|---|---|
| | INCLK | PLLENABLE |
| LVTTL | ✓ | ✓ |
| LVCMOS | ✓ | ✓ |
| 2.5 V | ✓ | |
| 1.8 V | ✓ | |
| 1.5 V | ✓ | |
| 3.3-V PCI | | |
| 3.3-V PCI-X | | |
| LVPECL | ✓ | |
| 3.3-V PCML | ✓ | |
| LVDS | ✓ | |
| HyperTransport technology | ✓ | |
| Differential HSTL | | |
| Differential SSTL | | |
| 3.3-V GTL | ✓ | |
| 3.3-V GTL+ | ✓ | |
| 1.5V HSTL class I | ✓ | |
| 1.5V HSTL class II | ✓ | |
| SSTL-18 class I | ✓ | |
| SSTL-18 class II | ✓ | |
| SSTL-2 class I | ✓ | |
| SSTL-2 class II | ✓ | |
| SSTL-3 class I | ✓ | |
| SSTL-3 class II | ✓ | |
| AGP (1× and 2×) | ✓ | |
| CTT | ✓ | |

*Figure 4–20. Stratix GX I/O Banks*



There is some flexibility with the number of I/O standards each Stratix I/O bank can simultaneously support. The following sections provide guidelines for mixing non-voltage-referenced and voltage-referenced I/O standards in Stratix devices.

## Non-Voltage-Referenced Standards

Each Stratix I/O bank has its own `VCCIO` pins and supports only one $V_{CCIO}$, either 1.5, 1.8, 2.5 or 3.3 V. A Stratix I/O bank can simultaneously support any number of input signals with different I/O standard assignments, as shown in Table 4–5.

For output signals, a single I/O bank can only support non-voltage-referenced output signals driving at the same voltage as $V_{CCIO}$. A Stratix I/O bank can only have one $V_{CCIO}$ value, so it can only drive out that one value for non-voltage referenced signals. For example, an I/O bank with a 2.5-V $V_{CCIO}$ setting can support 2.5-V LVTTL inputs and outputs, Hypertransport technology inputs and outputs, and 3.3-V LVCMOS inputs (not output or bidirectional pins).

***Table 4–5. Acceptable Input Levels for LVTTL/LVCMOS***

| Bank $V_{CCIO}$ | Acceptable Input Levels | | | |
|---|---|---|---|---|
| | **3.3 V** | **2.5 V** | **1.8 V** | **1.5 V** |
| 3.3 V | ✓ | ✓ *(1)* | | |
| 2.5 V | ✓ | ✓ | | |
| 1.8 V | ✓ *(2)* | ✓ *(2)* | ✓ | ✓ *(1)* |
| 1.5 V | ✓ *(2)* | ✓ *(2)* | ✓ | ✓ |

*Notes to Table 4–5:*

(1) Because the input signal will not drive to the rail, the input buffer does not completely shut off, and the I/O current will be slightly higher than the default value. Contact Altera Applications for details.

(2) These input values overdrive the input buffer, so the pin leakage current will be slightly higher than the default value. Contact Altera Applications for details.

## Voltage-Referenced Standards

To accommodate voltage-referenced I/O standards, each Stratix I/O bank supports multiple `VREF` pins feeding a common `VREF` bus. The number of available `VREF` pins increases as device density increases. If these pins are not used as `VREF` pins, they can not be used as generic I/O pins.

An I/O bank featuring single-ended or differential standards can support voltage-referenced standards as long as all voltage-referenced standards use the same $V_{REF}$ setting. For example, although one I/O bank can implement both SSTL-3 and SSTL-2 I/O standards, I/O pins using these standards must be in different banks since they require different $V_{REF}$ values

For voltage-referenced inputs, the receiver compares the input voltage to the voltage reference and does not take into account the $V_{CCIO}$ setting. Therefore, the $V_{CCIO}$ setting is irrelevant for voltage referenced inputs.

Voltage-referenced bidirectional and output signals must be the same as the I/O bank's $V_{CCIO}$ voltage. For example, although you can place an SSTL-2 input pin in any I/O bank with a 1.25-V $V_{REF}$ level, you can only place SSTL-2 output pins in an I/O bank with a 2.5-V $V_{CCIO}$.

### Mixing Voltage Referenced & Non-Voltage Referenced Standards

Non-voltage referenced and voltage referenced pins can safely be mixed in a bank by applying each of the rule-sets individually. For example, on I/O bank can support SSTL-3 inputs and 1.8-V LVCMOS inputs and outputs with a 1.8-V $V_{CCIO}$ and a 1.5-V $V_{REF}$. Similarly, an I/O bank can support 1.5-V LVCMOS, 3.3-V LVTTL (inputs, but not outputs), and HSTL I/O standards with a 1.5-V $V_{CCIO}$ and 0.75-V $V_{REF}$.

For the voltage-referenced examples, refer to the "I/O Pad Placement Guidelines" section. For details on how the Quartus II software supports I/O standards, see the "Quartus II Software Support"section.

## Programmable Current Drive Strength

The Stratix and Stratix GX device I/O pins support various output current drive settings as shown in Table 4–6. These programmable drive strength settings help decrease the effects of simultaneously switching outputs (SSO) in conjunction with reducing system noise. The supported settings ensure that the device driver meets the $I_{OH}$ and $I_{OL}$ specifications for the corresponding I/O standard.

*Table 4–6. Programmable Drive Strength*

| I/O Standard | $I_{OH}$ / $I_{OL}$ Current Strength Setting (mA) |
|---|---|
| 3.3-V LVTTL | 24 *(1)*, 16, 12, 8, 4 |
| 3.3-V LVCMOS | 24 *(2)*, 12 *(1)*, 8, 4, 2 |
| 2.5-V LVTTL/LVCMOS | 16 *(1)*, 12, 8, 2 |
| 1.8-V LVTTL/LVCMOS | 12 *(1)*, 8, 2 |
| 1.5-V LVCMOS | 8 *(1)*, 4, 2 |

***Notes to Table 4–6:***

(1) This is the Quartus II software default current setting.

(2) I/O banks 1, 2, 5, and 6 do not support this setting.

These drive-strength settings are programmable on a per-pin basis (for output and bidirectional pins only) using the Quartus II software. To modify the current strength of a particular pin, see "Programmable Drive Strength Settings" on page 4–46.

## Hot Socketing

In a hot socketing situation, a device's output buffers are turned off during system power-up or power-down. Stratix and Stratix GX devices support any power-up or power-down sequence ($V_{CCIO}$ and $V_{CCINT}$) to simplify designs. For mixed-voltage environments, you can drive signals into the device before or during power-up or power-down without damaging the device. Stratix and Stratix GX devices will not drive out until the device is configured and has attained proper operating conditions.

You can power up or power down the $V_{CCIO}$ and $V_{CCINT}$ pins in any sequence. The power supply ramp rates can range from 100 ns to 100 ms. During hot socketing, the I/O pin capacitance is less than 15 pF and the clock pin capacitance is less than 20 pF. The hot socketing DC specification is $| I_{IOPIN} | < 300\ \mu$ A. The hot socketing AC specification is $| I_{IOPIN} | < 8$ mA for 10 ns or less.

## I/O Termination

Although single-ended, non-voltage-referenced I/O standards do not require termination, Stratix and Stratix GX devices provide series termination through the programmable Terminator™ technology. This termination can assist with impedance matching to reduce reflections and improve signal integrity.

The following I/O standards do not require termination:

- LVTTL
- LVCMOS
- 2.5 V
- 1.8 V
- 1.5 V
- 3.3-V PCI/Compact PCI
- 3.3-V PCI-X 1.0
- 3.3-V AGP 1×

### Voltage-Referenced I/O Standards

Voltage-referenced I/O standards require both an input reference voltage, $V_{REF,}$ and a termination voltage, $V_{TT}$. The reference voltage of the receiving device tracks the termination voltage of the transmitting device. The designer can implement the series resistors shown in "Stratix & Stratix GX I/O Standards" on page 4–1 using the on-chip Stratix and Stratix GX device Terminator technology.

For more information on termination for voltage-referenced I/O standards, see "Stratix & Stratix GX I/O Standards" on page 4–1; the Section I, Stratix Device Family Data Sheet in *Stratix Device Handbook, Volume 1*; or the *Stratix GX FPGA Family Data Sheet*.

### Differential I/O Standards

Differential I/O standards typically require a termination resistor between the two signals at the receiver. The termination resistor must match the differential load impedance of the bus. Stratix and Stratix GX devices provide an optional differential termination on-chip resistor when using LVDS.

Refer to Chapter 5, Using High-Speed Differential I/O Interfaces in Stratix Devices for more information on differential I/O standards and their interfaces.

## I/O Driver Impedance Matching Using Terminator Technology

Stratix and Stratix GX devices provide I/O impedance matching and termination capabilities with the Terminator technology. The Terminator technology enables the use of on-chip parallel, differential, and series termination that aids in impedance matching by maintaining signal integrity and reducing reflections. The device constantly calibrates the internal resistor values after configuration and during operation. This calibration allows the termination resistors to compensate for voltage variation, temperature, and process. The feature helps simplify PCB design by reducing termination resistors.

You can use this feature for a given I/O bank by selecting one of the Terminator technology I/O standards in the Quartus II software. You can only use this feature for one I/O standard per bank at a time. The $V_{CCIO}$ must be compatible for all I/O pins in a given bank.

The Terminator technology can provide parallel termination for input drivers and series or parallel termination for output drivers. For input LVDS buffers, the feature can provide differential termination. You can also use the Terminator technology with bidirectional pins, allowing either series termination or parallel termination for I/O standards. You can only implement one type of termination, series or parallel, at a time.

### How Terminator Technology Works

Two external precision resistors ($R_{UP}$ and $R_{DN}$) per $V_{CCIO}$ bank are used as reference resistors. $R_{UP}$ is a pull-up resistor connected to $V_{CCIO}$; $R_{DN}$ is a pull-down resistor connected to GND. Altera recommends using resistors with a tolerance of 1%. Terminator technology monitors the value of the two reference resistors and uses the value to adjust internal termination circuitry to the same impedance. In addition, Terminator technology circuitry compensates for voltage, temperature, and process variation. This circuitry continuously calibrates the internal termination resistors during normal device operation.

Terminator technology supports one type of I/O standard per I/O bank. You can enable or disable on-chip termination within an I/O bank on a pin-by-pin basis. To use different on-chip termination I/O standards on a device, select separate I/O banks. For example, if you want to use on-chip termination for GTL+ (3.3-V $V_{CCIO}$) and SSTL-3 class II (3.3-V $V_{CCIO}$), use two separate I/O banks.

Different I/O standards need different $V_{CCIO}$ and $V_{REF}$ voltages. You can simultaneously use some I/O standards with the same $V_{CCIO}$ in an I/O bank.

## Series Termination Resistor ($R_S$)

Terminator technology provides an on-chip series termination resistor ($R_S$) for single-ended voltage-referenced I/O standard such as SSTL-2 and SSTL-3. The series termination value for these I/O standards is 25 Ω. The impedance matching value for LVTTL and LVCMOS is either 25 or 50 Ω. All I/O pins in Stratix and Stratix GX devices support this termination method. Table 4–7 shows the I/O standards supported for series termination and impedance matching.

*Table 4–7. Supported I/O Standards for Series Termination & Impedance Matching*

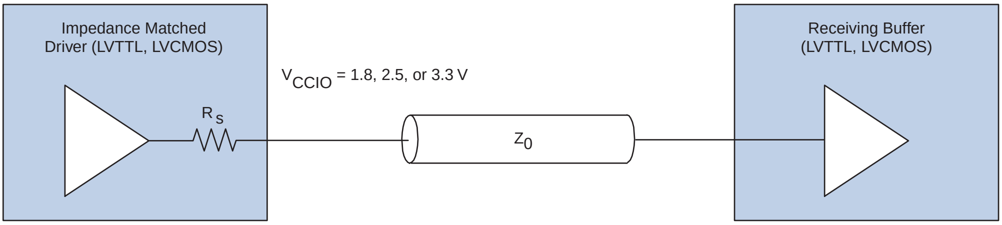
| Feature | Supported I/O Standards | $V_{CCIO}$ (V) |
|---|---|---|
| Series Termination | SSTL-3 class I | 3.3 |
| | SSTL-3 class II | 3.3 |
| | SSTL-2 class I | 2.5 |
| | SSTL-2 class II | 2.5 |
| Impedance Matching | LVTTL/LVCMOS | 3.3 |
| | LVTTL/LVCMOS | 2.5 |
| | LVTTL/LVCMOS | 1.8 |

The impedance of the output driver is matched with the transmission line impedance. Stratix output buffers can match output impedance to either 25 or 50 Ω. This impedance matching results in properly terminated signals, improving signal integrity. This feature is supported by all Stratix I/O pins.

☞ When using impedance matching for an output buffer, variable drive current strength and slow-slew rate features are not available.

Figure 4–21 shows the on-chip impedance matching resistor for an output driver.

*Figure 4–21. Driver Impedance Matching*



## Parallel Termination ($R_T$)

Terminator technology supports on-chip parallel termination for several voltage-referenced I/O standards. To maintain signal integrity and save board space, use Terminator technology resistors instead of external pull-up termination resistors. Parallel termination is supported for SSTL-2, SSTL-3, HSTL (class I and II), GTL, GTL+, and CTT I/O standards. Additionally, bidirectional pins support parallel termination. All the I/O pins in the top and bottom I/O banks support parallel termination. Figure 4–22 shows the parallel termination connections for a Stratix and Stratix GX device.

*Figure 4–22. Terminator Technology Parallel Termination*

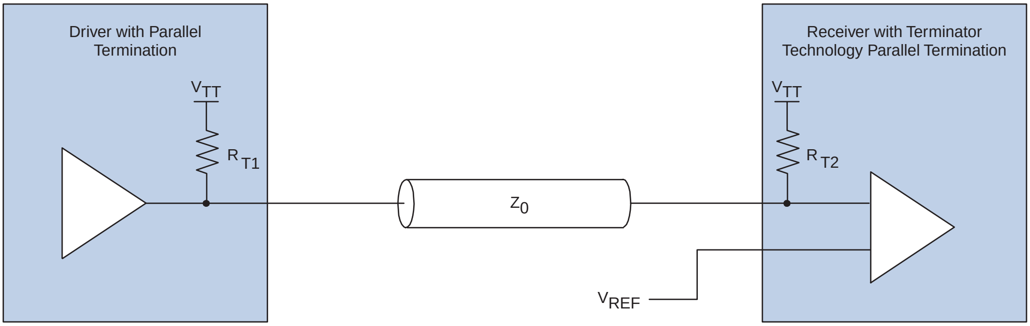


Table 4–8 shows the supported I/O standards for parallel termination in Stratix and Stratix GX devices.

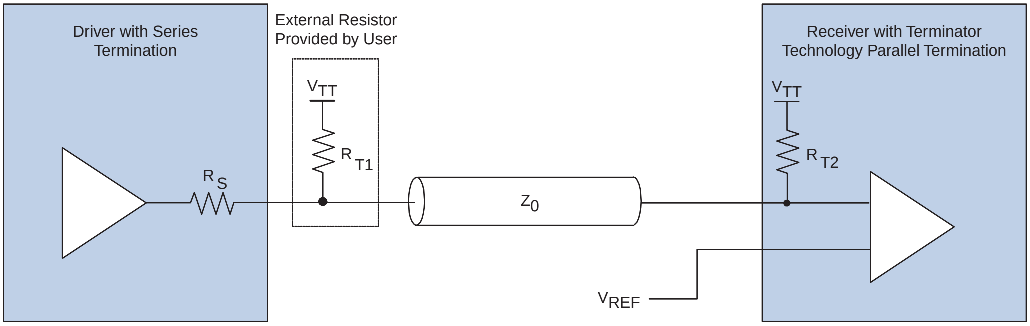
*Table 4–8. Supported I/O Standards for Parallel Termination*

| Supported I/O Standards | Parallel Termination ($R_{T1}$) | Parallel Termination ($R_{T2}$) | $V_{CCIO}$ (V) |
|---|---|---|---|
| SSTL-3 class I | N/A | 50 Ω | 3.3 |
| SSTL-3 class II *(1)* | 50 Ω | 50 Ω | 3.3 |
| SSTL-2 class I | N/A | 50 Ω | 2.5 |
| SSTL-2 class II *(1)* | 50 Ω | 50 Ω | 2.5 |
| HSTL class I | N/A | 50 Ω | 1.5 |
| HSTL class II | 50 Ω | 50 Ω | 1.5 |
| GTL | 50 Ω | 50 Ω | 3.3 |
| GTL+ | 50 Ω | 50 Ω | 3.3 |
| CTT | N/A | 50 Ω | 3.3 |

*Note to Table 4–8:*

(1) In addition to parallel termination, SSTL-3 and SSTL-2 class II I/O standards require a series termination next to the output buffer. If you are using these I/O standards for the output pins, Altera recommends using the on-chip series termination and an external pull-up resistor to $V_{TT}$ for parallel termination. Figure 4–23 shows the connection scheme for these particular I/O standards.

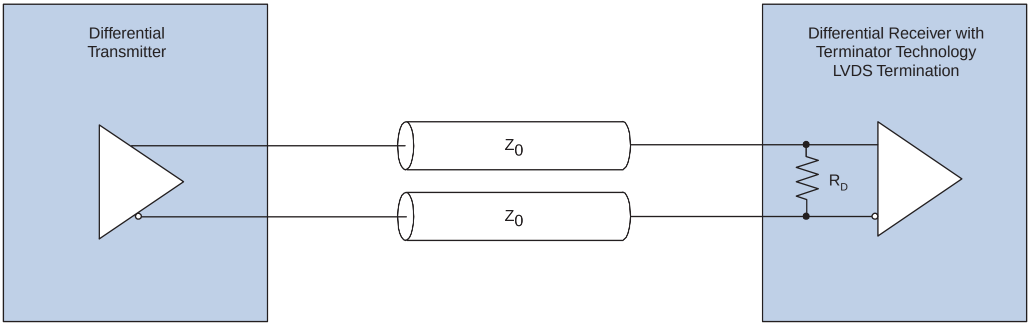
*Figure 4–23. Terminator Technology Series-Parallel Termination*



## Differential Termination ($R_D$)

Terminator technology supports on-chip differential termination for source-synchronous LVDS signaling. The differential termination resistors are adjacent to the differential input buffers on the device. This placement eliminates stub effects, improving the signal integrity of the serial link. Using on-chip differential termination resistors also saves board space. Figure 4–24 shows the differential termination connections for Stratix and Stratix GX devices.

*Figure 4–24. Terminator Technology Differential Termination*



Differential termination for Stratix devices is supported for the left and right I/O banks. Differential termination for Stratix GX devices is supported for the left, source-synchronous I/O bank. Some of the clock input pins are in the top and bottom I/O banks, which do not support differential termination. External reference resistors are not required for I/O banks that support differential termination. The value of on-chip differential termination resistors is 100 Ω.

## Transceiver Termination

Stratix GX devices feature built-in on-chip termination within the transceiver at both the transmit and receive buffers. This termination improves signal integrity and provides support for the 1.5-V PCML I/O standard.

See *Application Note 237: Using High-Speed Transceiver Blocks in Stratix GX Devices* for more information on transceiver termination.

## Reference Resistors

Connect the two reference resistors ($R_{UP}$ and $R_{DN}$) to the two dual-purpose reference pins per I/O bank. $R_{UP}$ is a pull-up resistor and is connected to the $V_{CCIO}$ of that I/O bank. $R_{DN}$ is a pull-down resistor and is connected to GND of that I/O bank. Figure 4–25 below shows the reference resistor connections.

*Figure 4–25. Terminator Reference Resistor Connections*

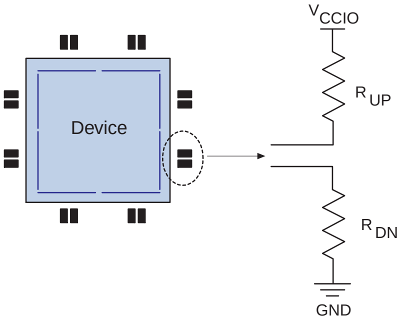


Table 4–9 shows the external reference resistors, $R_{UP}/R_{DN}$, required to achieve the target on-chip impedance, $R_L$.

*Table 4–9. External Reference Resistance Values* *Notes (1), (2)*

| Termination Type | $R_L$ (Ω) | $R_{UP}$ & $R_{DN}$ |
|---|---|---|
| Impedance matching or series termination *(3)* | 25 | 10 × $R_L$ |
| | 50 | 10 × $R_L$ |
| Parallel termination | 50 | 20 × $R_L$ |
| Differential termination | 100 | Not needed |

***Notes to Table 4–9:***

(1) $R_L$ is the target on-chip impedance.

(2) The on-chip termination resistors are within a 10% tolerance and the $R_{UP}$ and $R_{DN}$ values should be within a 1% tolerance.

(3) Use the **Series Termination** setting in the Quartus II software to implement impedance matching.

## Design Tips

The following list of design tips is a summary of key information required when using Terminator technology:

- Parallel termination is supported only on the top and bottom I/O banks.
- Series termination and impedance matching is supported on all the I/O banks.
- Differential termination is supported only on the left and right I/O banks in Stratix devices and on the left I/O bank in Stratix GX devices.
- Transceiver termination is supported in the Stratix GX transceiver.
- Terminator technology supports one type of on-chip termination I/O standard for a given I/O bank.
- Some features, such as LVTTL variable drive strength and slow slew rate control, cannot be used when impedance matching is enabled.
- Each I/O bank has two dual-purpose reference pins to which two external reference resistors need to be connected when using Terminator technology.
- Each I/O pin can either support series or parallel termination. In the case of SSTL-2 class II and SSTL-3 class II output pins, Altera recommends using on-chip series termination and parallel external pull-up resistors.
- There are no current draw limitations for 1.8-V $V_{CCIO}$ levels (thermally-enhanced BGA cavity up packages).
- Total current draw of 10 consecutive I/O pins, including two dual-purpose pins for external reference resistors within these 10 I/O pins, should not exceed 200 mA for thermally-enhanced cavity down packages or 150 mA for non-thermally enhanced cavity up and non-thermally enhanced FineLine BGA packages.

## I/O Pad Placement Guidelines

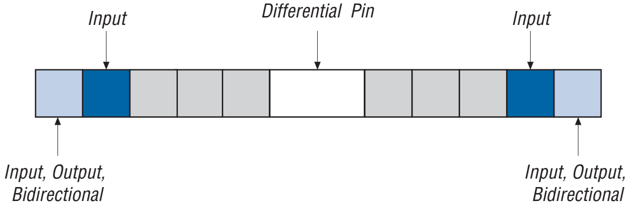
This section provides pad placement guidelines for the programmable I/O standards supported by Stratix and Stratix GX devices and includes essential information for designing systems using the devices' selectable I/O capabilities.

### Differential pad Placement Guidelines

In order to avoid cross coupling and maintain an acceptable noise level on the $V_{CCIO}$ supply, there are restrictions on the placement of single-ended I/O pads in relation to differential pads. Use the following guidelines for placing single-ended pads with respect to differential pads in Stratix devices. For Stratix GX guidelines, contact Altera Applications

- Single-ended input pads may only be placed four or more pads away from a differential pad (see Figure 4–26).
- Single-ended outputs and bidirectional pads may only be placed five or more pads away from a differential pad (see Figure 4–26).

*Figure 4–26. Using Two Different I/O Standards*



## VREF pad Placement Guidelines

Restrictions on the placement of single-ended voltage-referenced I/O pads with respect to `VREF` pads help maintain an acceptable noise level on the $V_{CCIO}$ supply and to prevent output switching noise from shifting the `VREF` rail. The following guidelines are for placing single-ended pads in Stratix devices. For Stratix GX guidelines, contact Altera Applications.

### *Input Pins*

Each `VREF` pad supports a maximum of 40 input pads with up to 20 on each side of the `VREF` pad.

### *Output Pins*

When a voltage referenced input or bidirectional pad does not exist in a bank, there is no limit to the number of output pads that can be implemented in that bank. When a voltage referenced input exists, each `VREF` pad supports 20 outputs for thermally enhanced FineLine BGA® and thermally enhanced BGA cavity up packages or 15 outputs for Non-thermally enhanced cavity up and non-thermally enhanced FineLine BGA packages.

### *Bidirectional Pins*

Bidirectional pads must satisfy input and output guidelines simultaneously. If the bidirectional pads are all controlled by the same OE and there are no other outputs or voltage referenced inputs in the bank, then there is no case where there is a voltage referenced input active at the same time as an output. Therefore, the output limitation does not apply. However, since the bidirectional pads are linked to the same OE, the bidirectional pads will all act as inputs at the same time. Therefore, the input limitation of 40 input pads (20 on each side of the `VREF` pad) will apply.

If any of the bidirectional pads are controlled by different output enables (OE) and there are no other outputs or voltage referenced inputs in the bank, then there may be a case where one group of bidirectional pads is acting as inputs while another group is acting as outputs. In such cases, apply the formulas shown in Table 4–10.

*Table 4–10. Input-Only Bidirectional Pin Limitation Formulas*

| Package Type | Formula |
|---|---|
| Thermally enhanced FineLine BGA and thermally enhanced BGA cavity up | *<Total number of bidirectional pads> – <Total number of pads from the smallest group of pads controlled by an OE>* ≤ 20 (per `VREF` pad) |
| Non-thermally enhanced cavity up and non-thermally enhanced FineLine BGA | *<Total number of bidirectional pads> – <Total number of pads from the smallest group of pads controlled by an OE>* ≤ 15 (per `VREF` pad). |

Consider a thermally enhanced FineLine BGA package with eight bidirectional pads controlled by OE1, eight bidirectional pads controlled by OE2, and six bidirectional pads controlled by OE3. While this totals 22 bidirectional pads, it is safely allowable because there would be a maximum of 16 outputs per `VREF` pad possible assuming the worst case where OE1 and OE2 are active and OE3 is inactive. This is particularly relevant in DDR SDRAM applications.

When at least one additional voltage referenced input and no other outputs exist in the same `VREF` bank, then the bidirectional pad limitation must simultaneously adhere to the input and output limitations. See the following equation.

*<Total number of bidirectional pads>* + *<Total number of input pads>* ≤ 40 (20 on each side of the `VREF` pad)

The previous equation accounts for the input limitations, but you must apply the appropriate equation from Table 4–11 to determine the output limitations.

*Table 4–11. Bidirectional pad Limitation Formulas (Where VREF Inputs Exist)*

| Package Type | Formula |
|---|---|
| Thermally enhanced FineLine BGA and thermally enhanced BGA cavity up | *<Total number of bidirectional pads>* ≤ 20 (per `VREF` pad) |
| Non-thermally enhanced cavity up and non-thermally enhanced FineLine BGA | *<Total number of bidirectional pads>* ≤ 15 (per `VREF` pad) |

When at least one additional output exists but no voltage referenced inputs exist, apply the appropriate formula from Table 4–12.

**Table 4–12. Bidirectional Pad Limitation Formulas (Where VREF Outputs Exist)**

| Package Type | Formula |
|---|---|
| Thermally enhanced FineLine BGA and thermally enhanced BGA cavity up | *<Total number of bidirectional pads>* + *<Total number of additional output pads>* – *<Total number of pads from the smallest group of pads controlled by an OE>* $\leq$ 20 (per `VREF` pad) |
| Non-thermally enhanced cavity up and non-thermally enhanced FineLine BGA | *<Total number of bidirectional pads>* + *<Total number of additional output pads>* – *<Total number of pads from the smallest group of pads controlled by an OE>* $\leq$ 15 (per `VREF` pad) |

When additional voltage referenced inputs and other outputs exist in the same `VREF` bank, then the bidirectional pad limitation must again simultaneously adhere to the input and output limitations. See the following equation.

*<Total number of bidirectional pads>* + *<Total number of input pads>* $\leq$ 40 (20 on each side of the `VREF` pad)

The previous equation accounts for the input limitations, but you must apply the appropriate equation from Table 4–11 to determine the output limitations.

**Table 4–13. Bidirectional Pad Limitation Formulas (Multiple VREF Inputs & Outputs)**

| Package Type | Formula |
|---|---|
| Thermally enhanced FineLine BGA and thermally enhanced BGA cavity up | *<Total number of bidirectional pads>* + *<Total number of additional output pads>* $\leq$ 20 (per `VREF` pad) |
| non-thermally enhanced cavity up and non-thermally enhanced FineLine BGA | *<Total number of bidirectional pads>* + *<Total number of additional output pads>* $\leq$ 15 (per `VREF` pad) |

In addition to the pad placement guidelines, use the following guidelines when working with $V_{REF}$ standards:

- Each bank can only have a single $V_{CCIO}$ voltage level and a single $V_{REF}$ voltage level at a given time. Pins of different I/O standards can share the bank if they have compatible $V_{CCIO}$ values (see Table 4–14 for more details).
- In all cases listed above, the Quartus II software generates an error message for illegally placed pads.

## DC Guidelines

Variables affecting the DC current draw include package type and desired termination methods. This section provides information on each of these variables and also shows how to calculate the DC current for pin placement.

☞ The Quartus II software automatically takes these variables into account during compilation.

For any 10 consecutive output pads in an I/O bank, Altera recommends a maximum current of 200 mA for thermally enhanced FineLine BGA and thermally enhanced BGA cavity up packages and 150 mA for non-thermally enhanced cavity up and non-thermally enhanced FineLine BGA packages. The following equation shows the current density limitation equation for thermally enhanced FineLine BGA and thermally enhanced BGA cavity up packages:

$$\sum_{pin}^{pin + 9} I_{pin} < 200 \text{ mA}$$

The following equation shows the current density limitation equation for non-thermally enhanced cavity up and non-thermally enhanced FineLine BGA packages:

$$\sum_{pin}^{pin + 9} I_{pin} < 150 \text{ mA}$$

Table 4–14 shows the DC current specification per pin for each I/O standard. I/O standards not shown in the table will not exceed these current limitations.

***Table 4–14. I/O Standard DC Specification (Part 1 of 2)***

| Pin I/O Standard | $I_{PIN}$ (mA) | | |
|---|---|---|---|
| | 3.3-V $V_{CCIO}$ | 2.5-V $V_{CCIO}$ | 1.5-V $V_{CCIO}$ |
| GTL | 40 | 40 | - |
| GTL+ | 34 | 34 | - |
| SSTL-3 class I | 8 | - | - |
| SSTL-3 class II | 16 | - | - |

*Table 4–14. I/O Standard DC Specification (Part 2 of 2)*

| Pin I/O Standard | $I_{PIN}$ (mA) | | |
|---|---|---|---|
| | 3.3-V $V_{CCIO}$ | 2.5-V $V_{CCIO}$ | 1.5-V $V_{CCIO}$ |
| CTT | 8 | - | - |
| SSTL-2 class I | - | 8.1 | - |
| SSTL-2 class II | - | 16.4 | - |
| HSTL class I | - | - | 8 |
| HSTL class II | - | - | 8 |

For more information on Altera device packaging, see Chapter 8, Package Information for Stratix Devices in *Stratix Device Handbook, Volume 1*.

## DC Guidelines for Terminator Technology

Enabling Terminator technology on-chip termination resistors will increase the total current draw of the device. This increase in current draw occurs because the termination circuitry, which is normally external to the device, is now a part of the device.

Table 4–15 lists the DC current draw when using on-chip series termination for single-ended I/O standards.

*Table 4–15. DC Current Draw for On-Chip Series Termination*

| Bank I/O Standard Selected by Terminator Technology | DC Current Draw per Pin for Series Termination ($I_{pin}$ in mA) *(1)* | $V_{CCIO}$ (V) |
|---|---|---|
| LVTTL | 0 | 1.8, 2.5, 3.3 |
| LVCMOS | 0 | 1.8, 2.5, 3.3 |
| SSTL-2 class I | 10 | 2.5 |
| SSTL-2 class II | 23 | 2.5 |
| SSTL-3 class I | 11 | 3.3 |
| SSTL-3 class II | 24 | 3.3 |

***Note to Table 4–15:***

(1) $I_{pin}$ is the DC current drawn per pin.

Table 4–16 lists the DC current draw when using Terminator technology on-chip parallel termination resistors for single-ended inputs or outputs.

*Table 4–16. DC Current Draw for On-Chip Series-Parallel Termination (Input & Output Pins) Note (1)*

| Bank I/O Standard Selected by Terminator Technology | DC Current Draw per Pin for Series & Parallel Termination ($I_{pin}$ in mA) (2) | | | $V_{CCIO}$ (V) |
|---|---|---|---|---|
| | Output Mode | | Input Mode | |
| | $R_S$ | $R_{T1}$ (3) | $R_{T2}$ (3) | |
| GTL | N/A | 40 | 15 | 3.3 |
| GTL+ | N/A | 34 | 14 | 3.3 |
| SSTL-2 class I | 10 | N/A | 12 | 2.5 |
| SSTL-2 class II | 23 | N/A | 12 | 2.5 |
| SSTL-3 class I | 11 | N/A | 15 | 3.3 |
| SSTL-3 class II | 24 | N/A | 17 | 3.3 |
| CTT | N/A | N/A (4) | 18 | 3.3 |
| HSTL class I | N/A | N/A (4) | 9 | 1.5 |
| HSTL class II | N/A | 20 | 10 | 1.5 |

*Notes to Table 4–16:*

(1) There are no current limitations for 1.8-V I/O standards (thermally-enhanced ball-grid array (BGA) cavity-up packages).

(2) $I_{pin}$ is the DC current drawn per pin.

(3) $R_{T1}$ and $R_{T2}$ are the parallel termination resistors for the voltage-referenced I/O standards. $R_{T1}$is the parallel termination resistor next to the output buffer and $R_{T2}$ is the parallel termination resistor next to the input buffer. See Figure 4–22.

(4) The CTT output buffer and HSTL Class I output buffer do not draw any current due to the on-chip termination resistor for single-ended I/O pads, but they will still source 8 mA as specified in the corresponding JEDEC specifications.

When using bidirectional pads, the total DC current draw by Terminator technology on-chip termination resistors is different than the values listed in Table 4–16. Table 4–17 lists the DC current draw values for bidirectional pads.

*Table 4–17. DC Current Draw for On-Chip Series-Parallel Termination (Bidirectional Pins) Note (1)*

| Bank I/O Standard Selected by Terminator Technology | DC Current Draw per Pin for Series & Parallel Termination ($I_{pin}$ in mA) (2) | | | $V_{CCIO}$ (V) |
|---|---|---|---|---|
| | $R_S$ | $R_{T1}$ (3) | $R_{T2}$ (3) | |
| GTL | N/A | 40 | 40 | 3.3 |
| GTL+ | N/A | 34 | 34 | 3.3 |
| SSTL-3 class I | 11 | N/A | 25 | 3.3 |
| SSTL-3 class II | 24 | N/A | 37 | 3.3 |
| SSTL-2 class I | 10 | N/A | 19 | 2.5 |
| SSTL-2 class II | 23 | N/A | 25 | 2.5 |
| CTT | N/A | N/A (4) | 27 | 3.3 |
| HSTL class I | N/A | N/A (4) | 16 | 1.5 |
| HSTL class II | N/A | 20 | 20 | 1.5 |

*Notes to Table 4–17:*

(1) There are no current limitations for 1.5- and 1.8-V $V_{CCIO}$ I/O standards.

(2) $I_{pin}$ is the DC current drawn per pin.

(3) $R_{T1}$ and $R_{T2}$ are the parallel termination resistors for the voltage referenced I/O standards. $R_{T1}$ is the parallel termination resistor next to output buffer and $R_{T2}$ is the parallel termination resistor next to input buffer.

(4) The CTT output buffer and HSTL class I output buffer do not draw any current due to the on-chip termination resistor for single-ended I/O pads, but they will still draw 8 mA as specified in the corresponding JEDEC specifications.

When you enable Terminator technology for an I/O bank, the dual-purpose pads connected to your external reference resistors for that bank are activated. When enabled, these reference resistors also draw a finite amount of current. The current consumption of these resistors for different I/O standards is shown in the Table 4–18.

*Table 4–18. $R_{UP}$ & $R_{DN}$ Current Consumption* *Note (1)*

| Bank I/O Standard Selected by Terminator Technology | $R_{UP}$ & $R_{DN}$ Current Consumption per I/O Bank ($I_{ref}$ in mA) *(2)* | | $V_{CCIO}$ (V) |
|---|---|---|---|
| | Series Termination | Parallel Termination | |
| LVTTL/LVCMOS *(3)* | 16 | N/A | 3.3 |
| LVTTL/LVCMOS *(3)* | 10 | N/A | 2.5 |
| SSTL-2 class I | 9 | 13 | 2.5 |
| SSTL-2 class II | 12 | 14 | 2.5 |
| SSTL-3 class I | 15 | 22 | 3.3 |
| SSTL-3 class II | 19 | 26 | 3.3 |
| HSTL class I | N/A | 5 | 1.5 |
| HSTL class II | N/A | 5 | 1.5 |
| GTL | N/A | 17 | 3.3 |
| GTL+ | N/A | 17 | 3.3 |
| CTT | N/A | 24 | 3.3 |

***Notes to Table 4–18:***

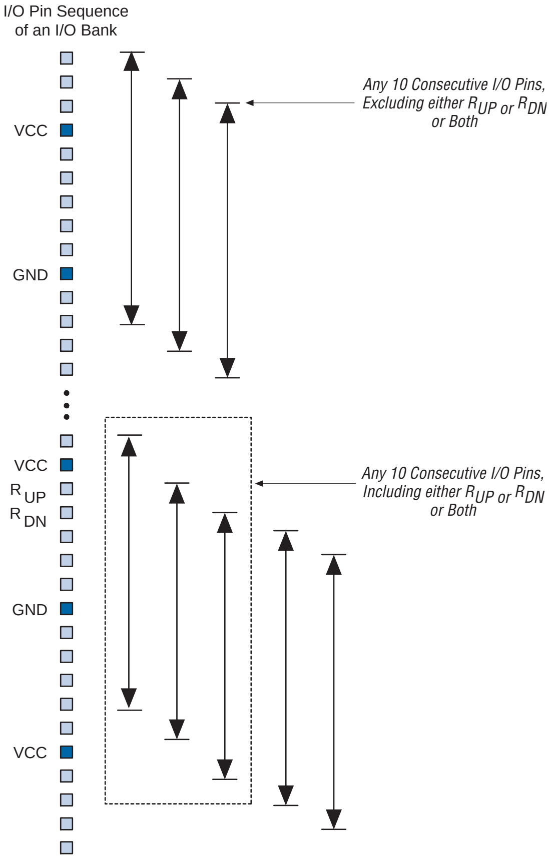
(1) There are no current restrictions for the HSTL class I and class II I/O standards (thermally-enhanced BGA cavity-up packages).

(2) $I_{ref}$ is the current drawn by the Terminator technology control circuitry, including the external reference resistors $R_{UP}$ and $R_{DN}$, per I/O bank.

(3) These values are the same whether you are using 250- or 500-Ω reference resistors.

Dual-purpose pads for connecting external reference resistors are also included while counting 10 consecutive I/O pads. When using Terminator technology, Figure 4–27 shows a Stratix or Stratix GX device's current draw limitation guidelines.

*Figure 4–27. Current Draw Limitation Guidelines Using Terminator Technology*



If the 10 consecutive I/O pads exclude either $R_{UP}$ or $R_{DN}$ or both pads, the current draw limitations cannot exceed 200 mA in thermally enhanced FineLine BGA and thermally enhanced BGA cavity up packages or 150 mA in non-thermally enhanced cavity up and non-thermally enhanced FineLine BGA packages.

For example, consider a case where a group of 10 consecutive pads are configured as follows for a thermally enhanced FineLine BGA and thermally enhanced BGA cavity up package:

- Number of SSTL-3 Class I output pads with Terminator technology = 3
- Number of GTL+ output pads without Terminator technology = 4
- The rest of the surrounding I/O pads in the consecutive group of 10 are unused

In this case, the total current draw for these 10 consecutive I/O pads would be (see Tables 4–16 and 4–17 for values):

(# of SSTL-3 Class I pads with Terminator technology × 11 mA) +
(# of GTL+ output pads × 34 mA) = (3 × 11 mA) + (4 × 34 mA) = 169 mA

In the above example, the total current draw for all 10 consecutive I/O pads is less than 200 mA.

If the 10 consecutive I/O pads also include either $R_{UP}$ or $R_{DN}$ or both pads, the current draw limitation for Stratix and Stratix GX devices should be less than (200 mA - $I_{ref}$), where $I_{ref}$ is the current drawn by either $R_{UP}$ or $R_{DN}$ or both.

For example, consider another case where a group of 10 consecutive pads are configured as follows for a thermally enhanced FineLine BGA and thermally enhanced BGA cavity up package:

- Number of SSTL-3 Class II output pads with Terminator technology = 8
- Number of external reference resistor pads ($R_{UP}$ and $R_{DN}$) = 1
- The rest of the surrounding I/O pads in the consecutive group of 10 are unused

In this case, the sum total of current draw for these 10 consecutive I/O pads would be (see Tables 4–15 and 4–18 for values):

(# of SSTL-3 Class II output pads with Terminator technology × 25 mA) +
(total current due to the Terminator technology, including external
reference resistor pads $R_{UP}$ and $R_{DN}$) = (8 × 24 mA) + (26 mA) = 218 mA

In the above example, the total current draw for all 10 consecutive I/O pads is more than 200 mA. Therefore, this case is not allowed and the Quartus II software generates an error message during design compilation.

## Quartus II Software Support

You specify which programmable I/O standards to use for Stratix and Stratix GX devices with the Quartus II software. This section describes Quartus II implementation, placement, and assignment guidelines, including

- Compiler Settings
- Device & Pin Options
- Assign Pins
- Programmable Drive Strength Settings
- I/O Banks in the Floorplan View
- Auto Placement & Verification

## Compiler Settings

You make Compiler settings in the **Compiler Settings** dialog box (Processing menu). Click the **Chips & Devices** tab to specify the device family, specific device, package, pin count, and speed grade to use for your design.

## Device & Pin Options

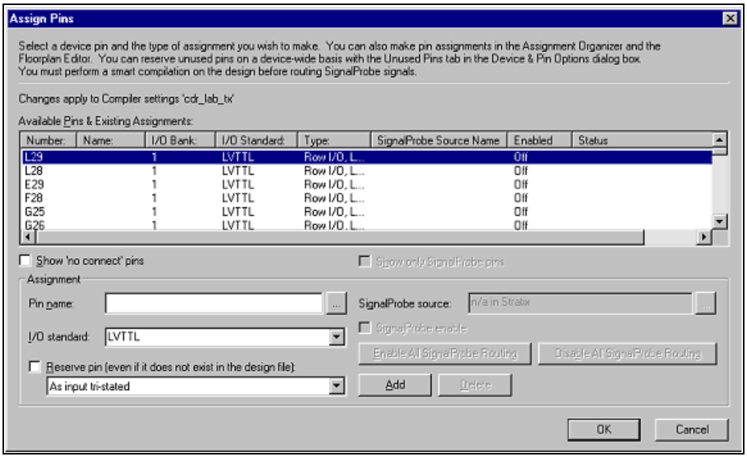
Click **Device & Pin Options** in the **Compiler Settings** dialog box to access the I/O pin settings. For example, in the **Voltage** tab you can select a default I/O standard for all pins for the targeted device. I/O pins that do not have a specific I/O standard assignment default this standard. Click **OK** when you are done setting I/O pin options to return to the **Compiler Settings** dialog box.

## Assign Pins

Click **Assign Pins** in the **Compiler Settings** dialog box to view the device's pin settings and pin assignments (see Figure 4–28). You can view the pin settings under **Available Pins & Existing Assignments**. The listing does not include $V_{REF}$ pins because they are dedicated pins. The information for each pin includes:

- Number
- Name
- I/O Bank
- I/O Standard
- Type (e.g., row or column I/O and differential or control)
- SignalProbe Source Name
- Enabled (i.e., whether SignalProbe routing is enabled or disabled
- Status

*Figure 4–28. Assign Pins*



Select a device pin and the type of assignment you wish to make. You can also make pin assignments in the Assignment Organizer and the Floorplan Editor. You can reserve unused pins on a device-wide basis with the Unused Pins tab in the Device & Pin Options dialog box. You must perform a smart compilation on the design before routing SignalProbe signals.

Changes apply to Compiler settings 'cdr_lab_tx'

Available Pins & Existing Assignments:

| Number: | Name: | I/O Bank: | I/O Standard: | Type: | SignalProbe Source Name | Enabled | Status |
|---|---|---|---|---|---|---|---|
| L29 | | 1 | LVTTL | Row I/O, L... | | Off | |
| L28 | | 1 | LVTTL | Row I/O, L... | | Off | |
| E29 | | 1 | LVTTL | Row I/O, L... | | Off | |
| F28 | | 1 | LVTTL | Row I/O, L... | | Off | |
| G25 | | 1 | LVTTL | Row I/O, L... | | Off | |
| G26 | | 1 | LVTTL | Row I/O, L... | | Off | |

☐ Show 'no connect' pins

☐ Show only SignalProbe pins

Assignment

Pin name:

I/O standard: LVTTL

☐ Reserve pin (even if it does not exist in the design file):

As input tri-stated

SignalProbe source: n/a in Stratix

☐ SignalProbe enable

When you assign an I/O standard that requires a reference voltage to an I/O pin, the Quartus II software automatically assigns $V_{REF}$ pins. Refer to Quartus II Help for instructions on how to use an I/O standard for a pin.

## Programmable Drive Strength Settings

To make programmable drive strength settings, perform the following steps:

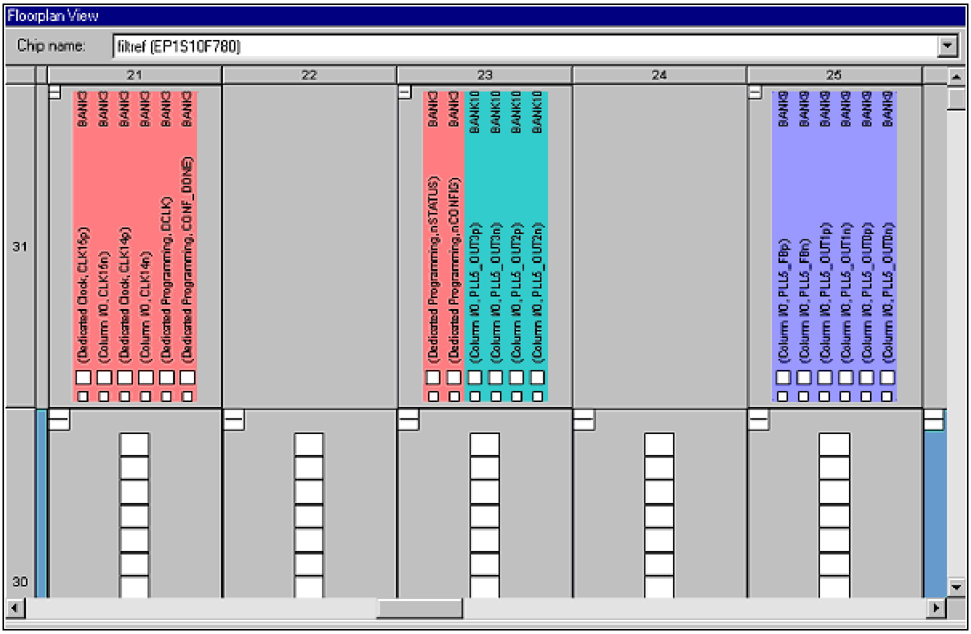
1. Choose **Assignment Organizer** (Tools menu).
2. Choose the **Edit specific entity & node settings for:** setting, then select the output or bidirectional pin to specify the current strength for.
3. Select **Options for Individual Nodes Only** in the **Assignment Categories** dialog box.
4. Select **Click here to add a new assignment**.
5. In the **Assignment** dialog box, set the **Name** field to **Current Strength** and set the **Setting** field to the desired, allowable value.
6. Click **Add**.
7. Click **Apply**, then **OK**.

## I/O Banks in the Floorplan View

You can view the arrangement of the device I/O banks in the **Floorplan View** (View menu) as shown in Figure 4–29. You can assign multiple I/O standards to the I/O pins in any given I/O bank as long as the $V_{CCIO}$ of the standards is the same. Pins that belong to the same I/O bank must use the same $V_{CCIO}$ signal.

Each device I/O pin belongs to a specific, numbered I/O bank. The Quartus II software color codes the I/O bank to which each I/O pin and $V_{CCIO}$ pin belong. Turn on the **Show I/O Banks** option to display the I/O bank color and the bank numbers for each pin.

*Figure 4–29. Floorplan View Window*



Chip name: filtref (EP1S10F780)

## Auto Placement & Verification of Selectable I/O Standards

The Quartus II software automatically verifies the placement for all I/O and $V_{REF}$ pins and performs the following actions.

- Automatically places I/O pins of different $V_{REF}$ standards without pin assignments in separate I/O banks and enables the $V_{REF}$ pins of these I/O banks.

- Verifies that voltage-referenced I/O pins requiring different $V_{REF}$ levels are not placed in the same bank.
- Reports an error message if the current limit is exceeded for a Stratix or Stratix GX power bank, as determined by the equation documented in "DC Guidelines" on page 4–38.
- Reserves the unused high-speed differential I/O channels and regular user I/O pins in the high-speed differential I/O banks when any of the high-speed differential I/O channels are being used.
- Automatically assigns $V_{REF}$ pins and I/O pins such that the current requirements are met and I/O standards are placed properly.

## Conclusion

Stratix and Stratix GX devices provide the I/O capabilities to allow system designers to work with current and emerging I/O standards and requirements. Today's complex designs demand increased flexibility to work with the wide variety of available I/O standards and to simplify board design. With Stratix and Stratix GX device features, such as hot socketing and Terminator technology, you can reduce board design interface costs and increase your development flexibility.

## More Information

For more information, refer to the following sources:

- Section I, Stratix Device Family Data Sheet in *Stratix Device Handbook, Volume 1*
- *Stratix GX FPGA Family Data Sheet*
- Chapter 5, Using High-Speed Differential I/O Interfaces in Stratix Devices
- *Application Note 224: High Speed Board Layout Guidelines*

## References

For more information, see the folloiwng references:

- Stub Series Terminated Logic for 2.5-V (SSTL-2), JESD8-9A, Electronic Industries Association, December 2000.
- High Speed Transceiver Logic (HSTL) – A 1.5-V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits, EIA/JESD8-6, Electronic Industries Association, August 1995.
- 1.5-V +/- 0.1 V (Normal Range) and 0.9 V – 1.6 V (Wide Range) Power Supply Voltage and Interface Standard for Non-terminated Digital Integrated Circuits, JESD8-11, Electronic Industries Association, October 2000.
- 1.8-V +/- 0.15 V (Normal Range) and 1.2 V – 1.95 V (Wide Range) Power Supply Voltage and Interface Standard for Non-terminated Digital Integrated Circuits, JESD8-7, Electronic Industries Association, February 1997.

- Center-Tap-Terminated (CTT) Low-Level, High-Speed Interface Standard for Digital Integrated Circuits, JESD8-9A, Electronic Industries Association, November 1993.
- 2.5-V +/- 0.2V (Normal Range) and 1.8-V to 2.7V (Wide Range) Power Supply Voltage and Interface Standard for Non-terminated Digital Integrated Circuits, JESD8-5, Electronic Industries Association, October 1995.
- Interface Standard for Nominal 3V/ 3.3-V Supply Digital Integrated Circuits, JESD8-B, Electronic Industries Association, September 1999.
- Gunning Transceiver Logic (GTL) Low-Level, High-Speed Interface Standard for Digital Integrated Circuits, JESD8-3, Electronic Industries Association, November 1993.
- Accelerated Graphics Port Interface Specification 2.0, Intel Corporation.
- Stub Series Terminated Logic for 1.8-V (SSTL-18), Preliminary JC42.3, Electronic Industries Association.
- PCI Local Bus Specification, Revision 2.2, PCI Special Interest Group, December 1998.
- PCI-X Local Bus Specification, Revision 1.0a, PCI Special Interest Group.
- UTOPIA Level 4, AF-PHY-0144.001, ATM Technical Committee.
- POS-PHY Level 4: SPI-4, OIF-SPI4-02.0, Optical Internetworking Forum.
- POS-PHY Level 4: SFI-4, OIF-SFI4-01.0, Optical Internetworking Forum.
- Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits, ANSI/TIA/EIA-644, American National Standards Institute/Telecommunications Industry/Electronic Industries Association, October 1995.

# 5. Using High-Speed Differential I/O Interfaces in Stratix Devices

S52005-1.1

Chapter 5, Using High-Speed Differential I/O Interfaces in Stratix Devices replaces *AN 202: Using High-Speed Differential I/O Interfaces in Stratix Devices*.

## Introduction

To achieve high data transfer rates, Stratix™ devices support True-LVDS™ differential I/O interfaces which have dedicated serializer/deserializer (SERDES) circuitry for each differential I/O pair. Stratix SERDES circuitry transmits and receives up to 840 megabits per second (Mbps) per channel. The differential I/O interfaces in Stratix devices support many high-speed I/O standards, such as LVDS, LVPECL, PCML, and HyperTransport™ technology. Stratix device high-speed modules are designed to provide solutions for many leading protocols such as SPI-4 Phase 2, SFI-4, 10G Ethernet XSBI, RapidIO, HyperTransport technology, and UTOPIA-4.

The SERDES transmitter is designed to serialize 4-, 7-, 8-, or 10-bit wide words and transmit them across either a cable or printed circuit board (PCB). The SERDES receiver takes the serialized data and reconstructs the bits into a 4-, 7-, 8-, or 10-bit-wide parallel word. The SERDES contains the necessary high-frequency circuitry, multiplexer, demultiplexer, clock, and data manipulation circuitry. You can use double data rate I/O (DDRIO) circuitry to transmit or receive differential data in by-one (×1) or by-two (×2) modes.

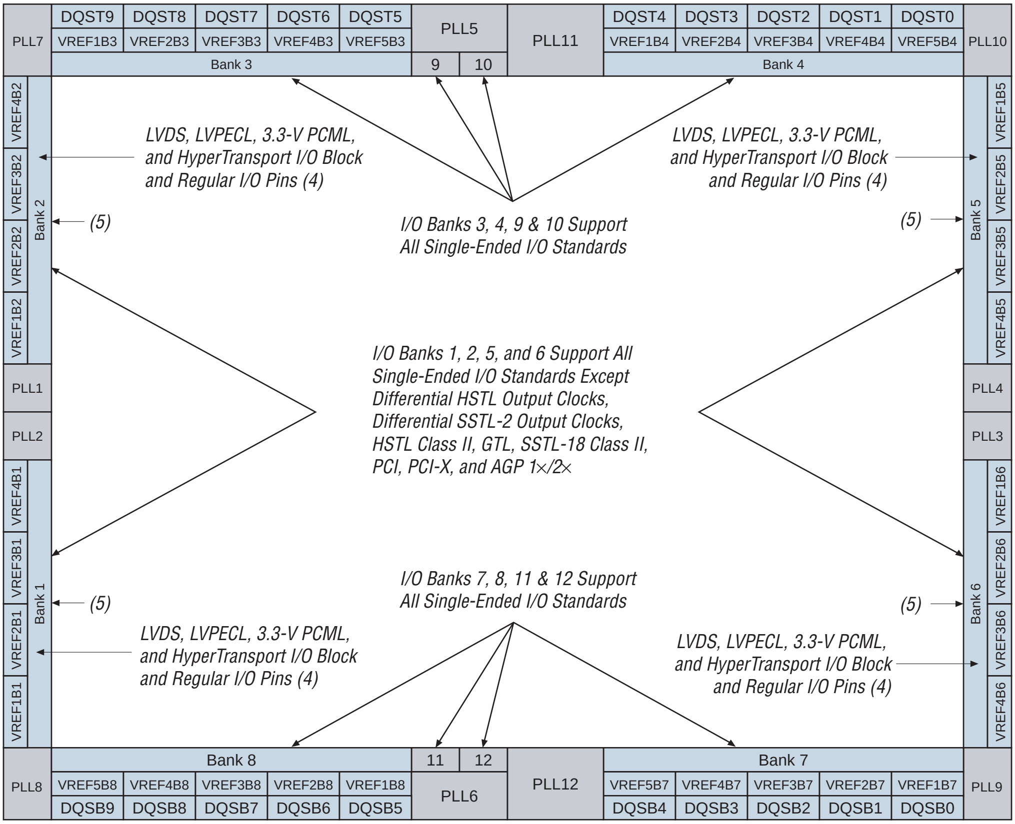
☞ Contact Altera Applications for more information on other *B* values that the Stratix devices support and using ×7-mode in the Quartus® II software. Stratix devices currently only support *B* = 1 and B = 7 in ×7 mode.

This application note describes the high-speed differential I/O capabilities of Stratix programmable logic devices (PLDs) and provides guidelines for their optimal use. You should use this document in conjunction with Section I, Stratix Device Family Data Sheet of the *Stratix Device Handbook, Volume 1*. Consideration of the critical issues of controlled impedance of traces and connectors, differential routing, termination techniques, and DC balance will help get the best performance from the device. Therefore, an elementary knowledge of high-speed clock-forwarding techniques is also helpful.

## Stratix I/O Banks

Stratix devices contain eight I/O banks, as shown in Figure 5–1. The two I/O banks on each side contain circuitry to support high-speed LVDS, LVPECL, PCML, HSTL class I and II, SSTL-2 class I and II, and HyperTransport inputs and outputs.

*Figure 5–1. Stratix I/O Banks* *Notes (1), (2), (3)*



*Notes to Figure 5–1:*

(1) Figure 5–1 is a top view of the Stratix silicon die, which corresponds to a top-down view of non-flip-chip packages and a bottom-up view of flip-chip packages.

(2) Figure 5–1 is a graphic representation only. Refer to the pin list and the Quartus II software for exact locations.

(3) Banks 9 through 12 are enhanced PLL external clock output banks.

(4) If the high-speed differential I/O pins are not used for high-speed differential signaling, they can support all of the I/O standards except HSTL class I and II, GTL, SSTL-18 Class II, PCI, PCI-X, and AGP 1×/2×.

(5) You can only place single-ended input pads four or more pads away from a differential pad. You can only place single-ended output/bidirectional pads five or more pads away from a differential pad. Use the **Show Pads** view in the Quartus II Floorplan Editor to locate these pads. The Quartus II software will give an error message for illegal output or bidirectional pin placement next to a high-speed differential I/O pin.

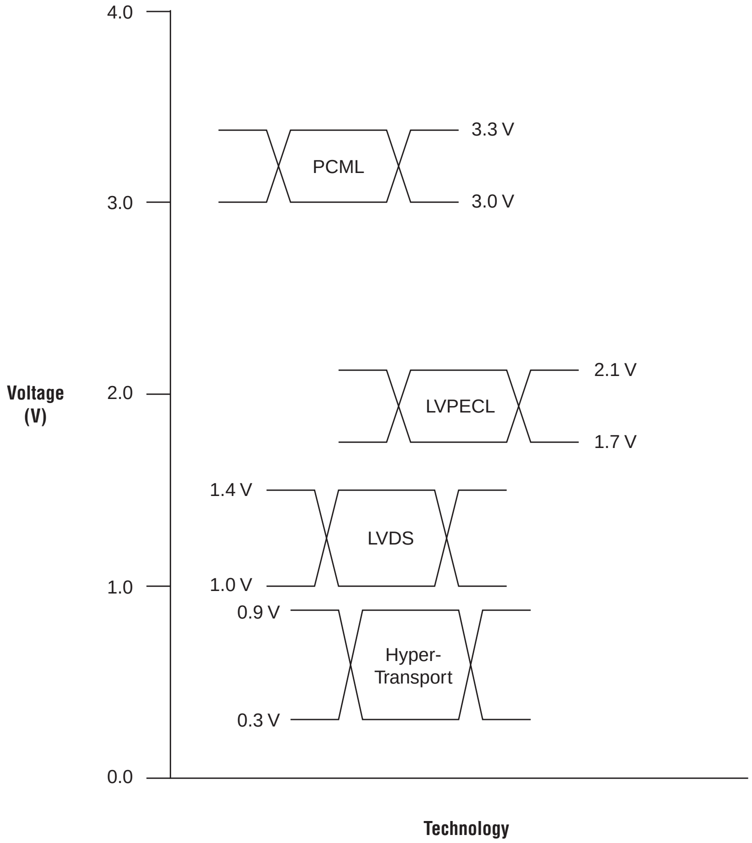
## Stratix Differential I/O Standards

Stratix devices provide a multi-protocol interface that allows communication between a variety of I/O standards, including LVDS, HyperTransport technology, LVPECL, PCML, HSTL class I and II, and SSTL-2 class I and II. This feature makes the Stratix device family ideal for applications that require multiple I/O standards, such as a protocol translator.

For more information on termination for Stratix I/O standards, see "Differential I/O Termination" on page 5–44.

Figure 5–2 compares the voltage levels between differential I/O standards supported in all the Stratix devices.

*Figure 5–2. Differential I/O Standards Supported by Stratix Devices*



### *LVDS*

The LVDS I/O standard is a differential high-speed, low-voltage swing, low-power, general-purpose I/O interface standard requiring a 3.3-V $V_{CCIO}$. This standard is used in applications requiring high-bandwidth data transfer, backplane drivers, and clock distribution. The ANSI/TIA/EIA-644 standard specifies LVDS transmitters and receivers capable of operating at recommended maximum data signaling rates of 655 Mbps. However, devices can operate at slower speeds if needed, and there is a theoretical maximum of 1.923 Gbps. Stratix devices meet the ANSI/TIA/EIA-644 standard.

Due to the low voltage swing of the LVDS I/O standard, the electromagnetic interference (EMI) effects are much smaller than CMOS, transistor-to-transistor logic (TTL), and PECL. This low EMI makes LVDS ideal for applications with low EMI requirements or noise immunity requirements. The LVDS standard specifies a differential output voltage range of $0.25\text{ V} \leq V_{OD} \leq 0.45\text{ V}$. The LVDS standard does not require an input reference voltage, however, it does require a 100-Ω termination resistor between the two signals at the input buffer. Stratix devices include an optional 100-Ω termination resistor within the device using Terminator technology. See Section I, Stratix Device Family Data Sheet of the *Stratix Device Handbook, Volume 1* for the LVDS parameters.

### *HyperTransport Technology*

The HyperTransport technology I/O standard is a differential high-speed, high-performance I/O interface standard requiring a 2.5-V VCCIO. This standard is used in applications such as high-performance networking, telecommunications, embedded systems, consumer electronics, and Internet connectivity devices. The HyperTransport technology I/O standard is a point-to-point standard in which each HyperTransport technology bus consists of two point-to-point unidirectional links. Each link is 2 to 32 bits. See Section I, Stratix Device Family Data Sheet of the *Stratix Device Handbook, Volume 1* for the HyperTransport parameters.

### *LVPECL*

The LVPECL I/O standard is a differential interface standard requiring a 3.3-V $V_{CCIO.}$ The standard is used in applications involving video graphics, telecommunications, data communications, and clock distribution. The high-speed, low-voltage swing LVPECL I/O standard uses a positive power supply and is similar to LVDS, however, LVPECL has a larger differential output voltage swing than LVDS. See Section I, Stratix Device Family Data Sheet of the *Stratix Device Handbook, Volume 1* for the LVPECL signaling characteristics.

### *PCML*

The PCML I/O standard is a differential high-speed, low-power I/O interface standard used in applications such as networking and telecommunications. The standard requires a 3.3-V $V_{CCIO}$. The PCML I/O standard achieves better performance and consumes less power than the LVPECL I/O standard. The PCML standard is similar to LVPECL, but PCML has a reduced voltage swing, which allows for a faster switching time and lower power consumption. See Section I, Stratix Device Family Data Sheet of the *Stratix Device Handbook, Volume 1* for the PCML signaling characteristics.

### *Differential HSTL (Class I & II)*

The differential HSTL I/O standard is used for applications designed to operate in the 0.0- to 1.5-V HSTL logic switching range such as quad data rate (QDR) memory clock interfaces. The differential HSTL specification is the same as the single ended HSTL specification. The standard specifies an input voltage range of $-0.3\text{ V} \leq V_I \leq V_{CCIO} + 0.3\text{ V}$. The differential HSTL I/O standard is only available on the input and output clocks. See Section I, Stratix Device Family Data Sheet of the *Stratix Device Handbook, Volume 1* for the HSTL signaling characteristics

### *Differential SSTL-2 (Class I & II)*

The differential SSTL-2 I/O standard is a 2.5-V memory bus standard used for applications such as high-speed double data rate (DDR) SDRAM interfaces. This standard defines the input and output specifications for devices that operate in the SSTL-2 logic switching range of 0.0 to 2.5 V. This standard improves operation in conditions where a bus must be isolated from large stubs. The SSTL-2 standard specifies an input voltage range of $-0.3\text{ V} \leq V_I \leq V_{CCIO} + 0.3\text{ V}$. Stratix devices support both input and output levels. The differential SSTL-2 I/O standard is only available on output clocks. See Section I, Stratix Device Family Data Sheet of the *Stratix Device Handbook, Volume 1* for the SSTL-2 signaling characteristics.

## Stratix Differential I/O Pin Location

The differential I/O pins are located on the I/O banks on the right and left side of the Stratix device. Table 5–1 shows the location of the Stratix device high-speed differential I/O buffers. When the I/O pins in the I/O banks that support differential I/O standards are not used for high-speed signaling, you can configure them as any of the other supported I/O standards. DDRIO capabilities are detailed in "SERDES Bypass DDR Differential Signaling" on page 5–40.

*Table 5–1. I/O Pin Locations on Each Side of Stratix Devices*

| Device Side *(1)* | Differential Input | Differential Output | DDRIO |
|---|---|---|---|
| Left | ✓ | ✓ | ✓ |
| Right | ✓ | ✓ | ✓ |
| Top | | | ✓ |
| Bottom | | | ✓ |

***Note to Table 5–1:***

(1) Device sides are relative to pin `1A` in the upper left corner of the device.

## Principles of SERDES Operation

Stratix devices support source-synchronous differential signaling up to 840 Mbps. Serial data is transmitted and received along with a low-frequency clock. The PLL can multiply the incoming low-frequency clock by a factor of 1 to 10. The SERDES factor *J* can be 4, 7, 8, or 10 and does not have to equal the clock multiplication value. ×1 and ×2 operation is also possible by bypassing the SERDES; it is explained in "SERDES Bypass DDR Differential Interface Review" on page 5–40.

On the receiver side, the high-frequency clock generated by the PLL shifts the serial data through a shift register (also called deserializer). The parallel data is clocked out to the logic array synchronized with the low-frequency clock. On the transmitter side, the parallel data from the logic array is first clocked into a parallel-in, serial-out shift register synchronized with the low-frequency clock and then transmitted out by the output buffers.

There are four dedicated fast PLLs in EP1S10 to EP1S25 devices, and eight in EP1S30 to EP1S80 devices. These PLLs are used for the SERDES operations as well as general-purpose use.

The differential channels and the high-speed PLL layout in Stratix devices are described in the "Differential I/O Interface & Fast PLLs" section on page 5–16.

## Stratix Differential I/O Receiver Operation

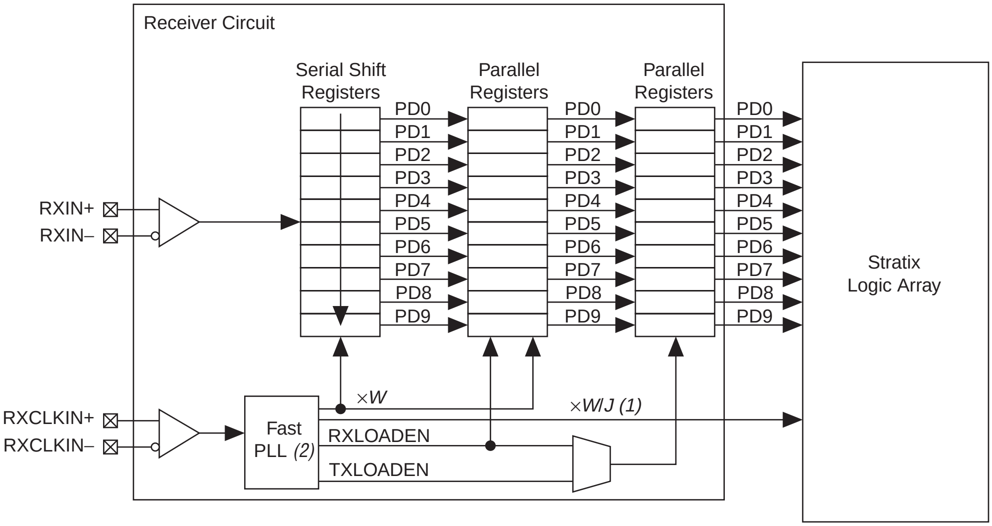
You can configure any of the Stratix differential input channels as a receiver channel (see Figure 5–3). The differential receiver deserializes the incoming high-speed data. The input shift register continuously clocks the incoming data on the negative transition of the high-frequency clock generated by the PLL clock (×*W*).

The data in the serial shift register is shifted into a parallel register by the `RXLOADEN` signal generated by the fast PLL counter circuitry on the third falling edge of the high-frequency clock. However, you can select which falling edge of the high frequency clock loads the data into the parallel register, using the data-realignment circuit. For more information on the data-realignment circuit, see "Data Realignment Principles of Operation" on page 5–25.

In normal mode, the enable signal `RXLOADEN` loads the parallel data into the next parallel register on the second rising edge of the low-frequency clock. You can also load data to the parallel register through the `TXLOADEN` signal when using the data-realignment circuit.

Figure 5–3 shows the block diagram of a single SERDES receiver channel. Figure 5–4 shows the timing relationship between the data and clocks in Stratix devices in ×10 mode. *W* is the low-frequency multiplier and *J* is data parallelization division factor.

Figure 5–3. Stratix High-Speed Interface Deserialized in ×10 Mode

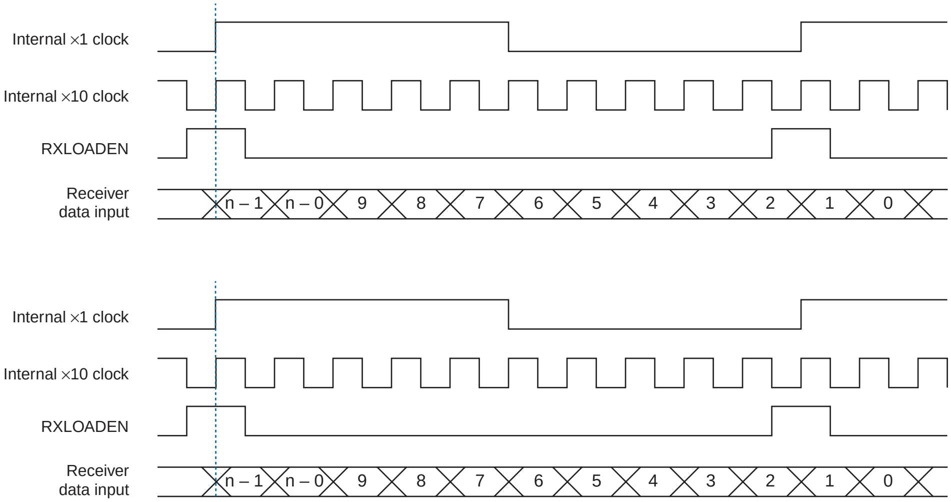


*Notes to Figure 5–3:*

(1) $W = 1, 2, 4, 7, 8$, or 10.
$J = 4, 7, 8$, or 10.
$W$ does not have to equal $J$. When $J = 1$ or 2, the deserializer is bypassed. When $J = 2$, the device uses DDRIO registers.

(2) This figure does not show additional circuitry for clock or data manipulation.

Figure 5–4. Receiver Timing Diagram



## Stratix Differential I/O Transmitter Operation

You can configure any of the Stratix differential output channels as a transmitter channel. The differential transmitter is used to serialize outbound parallel data.

The logic array sends parallel data to the SERDES transmitter circuit when the `TXLOADEN` signal is asserted. This signal is generated by the high-speed counter circuitry of the logic array low-frequency clock's rising edge. The data is then transferred from the parallel register into the serial shift register by the `TXLOADEN` signal on the third rising edge of the high-frequency clock.

Figure 5–5 shows the block diagram of a single SERDES transmitter channel and Figure 5–6 shows the timing relationship between the data and clocks in Stratix devices in ×10 mode. *W* is the low-frequency multiplier and *J* is the data parallelization division factor.

*Figure 5–5. Stratix High-Speed Interface Serialized in ×10 Mode*

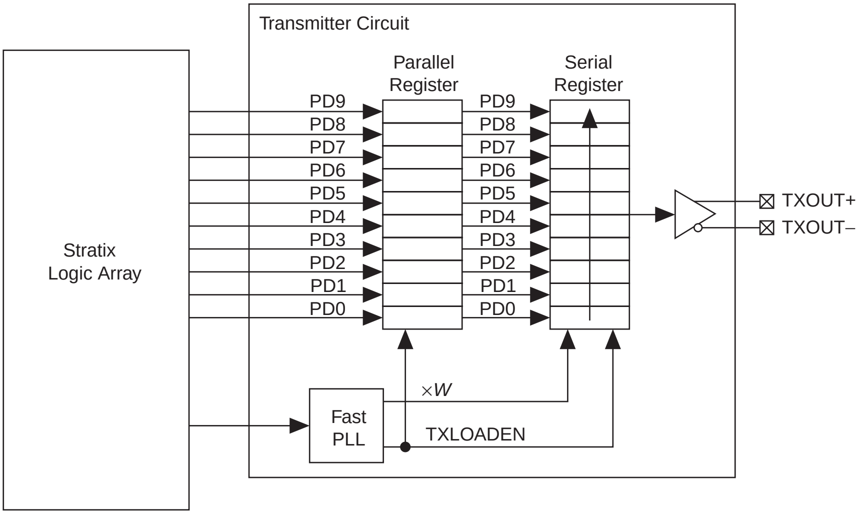
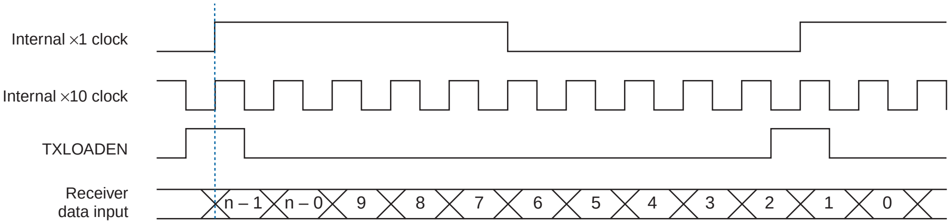


*Figure 5–6. Transmitter Timing Diagram*



## Transmitter Clock Output

Different applications and protocols call for various clocking schemes. Some applications require you to center-align the rising or falling clock edge with the data. Other applications require a divide version of the transmitted clock, or the clock and data to be at the same high-speed frequency. The Stratix device transmitter clock output is versatile and easily programmed for all such applications.

Stratix devices transmit data using the source-synchronous scheme, where the clock is transmitted along with the serialized data to the receiving device. Unlike APEX™ 20KE and APEX II devices, Stratix devices do not have a fixed transmitter clock output pin. The Altera® Quartus II software generates the transmitter clock output by using a fast clock to drive a transmitter `dataout` channel. Therefore, you can place the transmitter clock pair close to the data channels, reducing clock-to-data skew and increasing system margins. This approach is more flexible, as any channel can drive a clock, not just specially designated clock pins.

## Divided-Down Transmitter Clock Output

You can divide down the high-frequency clock by 2, 4, 8, or 10, depending on the system requirements. The various options allow Stratix devices to accommodate many different types of protocols. The divided-down clock is generated by an additional transmitting data channel.

Table 5–2 shows the divided-down version of the high-frequency clock and the selected serialization factor *J* (described in pervious sections). The Quartus II software automatically generates the data input to the additional transmitter data channel.

*Table 5–2. Differential Transmitter Output Clock Division*

| J | Data Input | Output Clock Divided By *(1)* |
|---|---|---|
| 4 | `1010` | 2 |
| 4 | `0011` | 4 |
| 8 | `10101010` | 2 |
| 8 | `00110011` | 4 |
| 8 | `11000011` | 8 |
| 10 | `1010101010` | 2 |
| 10 | `1110000011` | 10 |

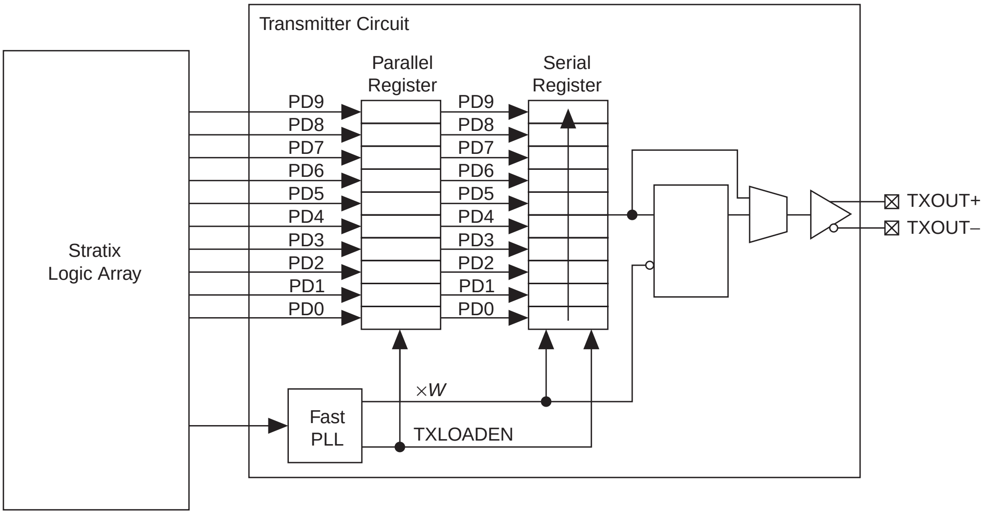
***Note to Table 5–2:***

(1) This value is usually referred to as *B*.

## Center-Aligned Transmitter Clock Output

A negative-edge-triggered D flipflop (DFF) register is located between the serial register of each data channel and its output buffer, as show in Figure 5–7. The negative-edge-triggered DFF register is used when center-aligned data is required. For center alignment, the DFF only shifts the output from the channel used as the transmitter clock out. The transmitter data channels bypass the negative-edge DFF. When you use the DFF register, the data is transmitted at the negative edge of the multiplied clock. This delays the transmitted clock output relative to the data channels by half the multiplied clock cycle. This is used for HyperTransport technology, but can also be used for any interface requiring center alignment.

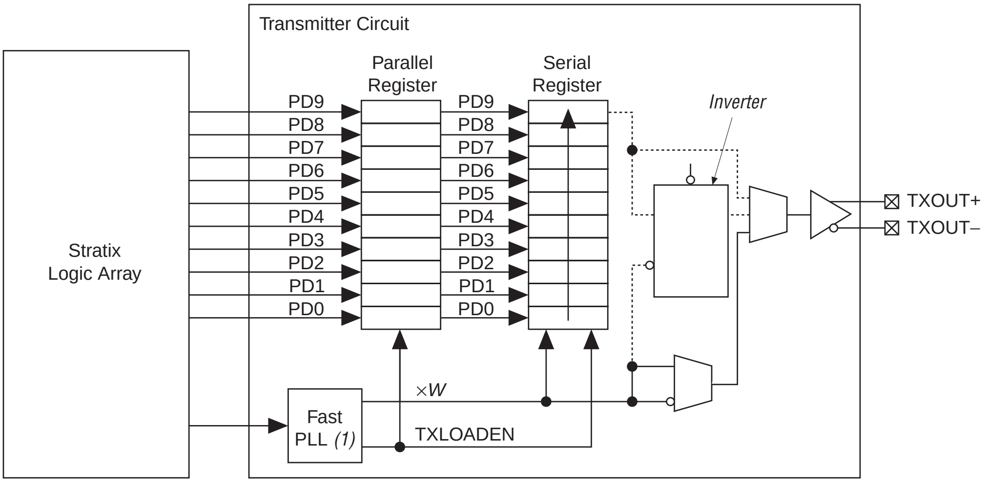
*Figure 5–7. Stratix Programmable Transmitter Clock*



## SDR Transmitter Clock Output

You can route the high-frequency clock internally generated by the PLL out as a transmitter clock output on any of the differential channels. The high-frequency clock output allows Stratix devices to support applications that require a 1-to-1 relationship between the clock and data. The path of the high-speed clock is shown in Figure 5–8. A programmable inverter allows you to drive the signal out on either the negative edge of the clock or 180° out of phase with the streaming data.

*Figure 5–8. High-Speed 1-to-1 Transmitter Clock Output*



*Note to Figure 5–8:*

(1) This figure does not show additional circuitry for clock or data manipulation.

## Using SERDES to Implement DDR

Some designs require a 2-to-1 data-to-clock ratio. These systems are usually based on Rapid I/O, SPI-4 Phase 2 (POS_PHY Level 4), or HyperTransport interfaces, and support various data rates. Stratix devices meet this requirement for such applications by providing a variable clock division factor. The SERDES clock division factor is set to 2 for double data rate (DDR).

An additional differential channel (as described in "Transmitter Clock Output" on page 5–10) is automatically configured to produce the transmitter clock output signal with half the frequency of the data.

For example, when a system is required to transmit 6.4 Gbps with a 2-to-1 clock-to-data ratio, program the SERDES with eight high-speed channels running at 800 Mbps each. When you set the output clock division factor (2 for this example), the Quartus II software automatically assigns a ninth channel as the transmitter clock output. You can edge- or center-align the transmitter clock by selecting the default PLL phase or selecting the negative-edge transmitter clock output. On the receiver side, the clock signal is connected to the receiver PLL's clock.

The multiplication factor *W* is also calculated automatically. The data rate divides by the input clock frequency to calculate the *W* factor. The deserialization factor (*J*) may be 4, 7, 8, or 10.

Figure 5–9 shows a DDR clock-to-data timing relationship with the clock center-aligned with respect to data. Figure 5–10 shows the connection between the receiver and transmitter circuits.

*Figure 5–9. DDR Clock-to-Data Relationship*

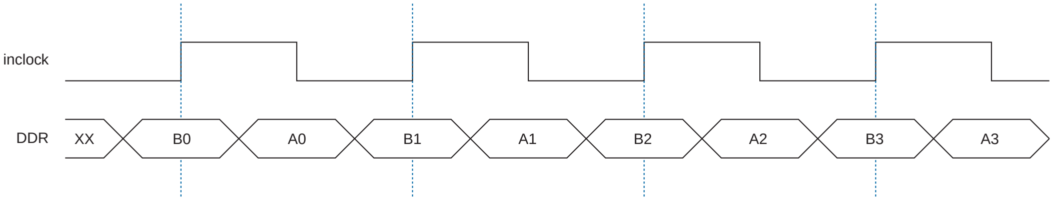
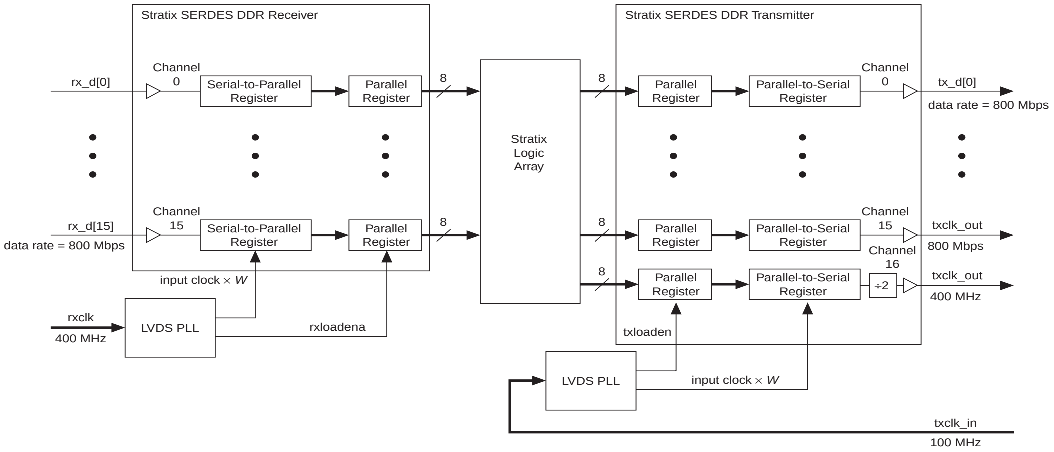


*Figure 5–10. DDR Receiver & Transmitter Circuit Connection*



## Using SERDES to Implement SDR

Stratix devices support systems based on single data rate (SDR) operations applications by allowing you to directly transmit out the multiplied clock (as described in "SDR Transmitter Clock Output" on page 5–12). These systems are usually based on Utopia-4, SFI-4, or XSBI interfaces, and support various data rates.

An additional differential channel is automatically configured to produce the transmitter clock output signal and is transmitted along with the data.

For example, when a system is required to transmit 10 Gbps with a 1-to-1 clock-to-data ratio, program the SERDES with sixteen high-speed channels running at 624 Mbps each. The Quartus II software

]

automatically assigns a seventeenth channel as the transmitter clock output. You can edge- or center-align the transmitter clock output by selecting the default PLL phase or selecting the 90° phase of the PLL output. On the receiver side, the clock signal is connected to the receiver PLL's clock input, and you can assign identical clock-to-data alignment.

The multiplication factor *W* is calculated automatically. The data rate is dividing by the input clock frequency to calculate the *W* factor. The deserialization factor *J* may be 4, 7, 8, or 10.

Figure 5–11 shows an SDR clock-to-data timing relationship, with clock center aligned with respect to data. Figure 5–12 shows the connection between the receiver and transmitter circuits.

***Figure 5–11. SDR Clock-to-Data Relationship***

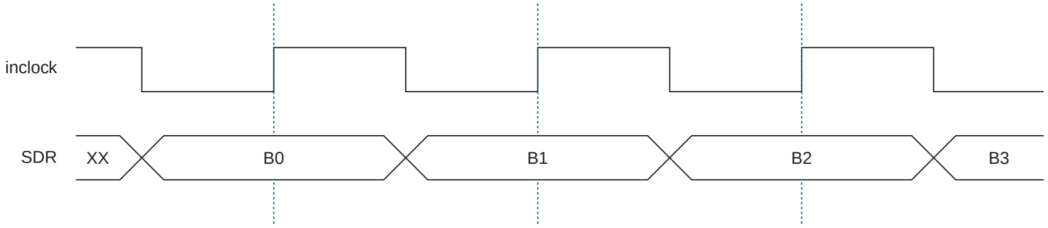
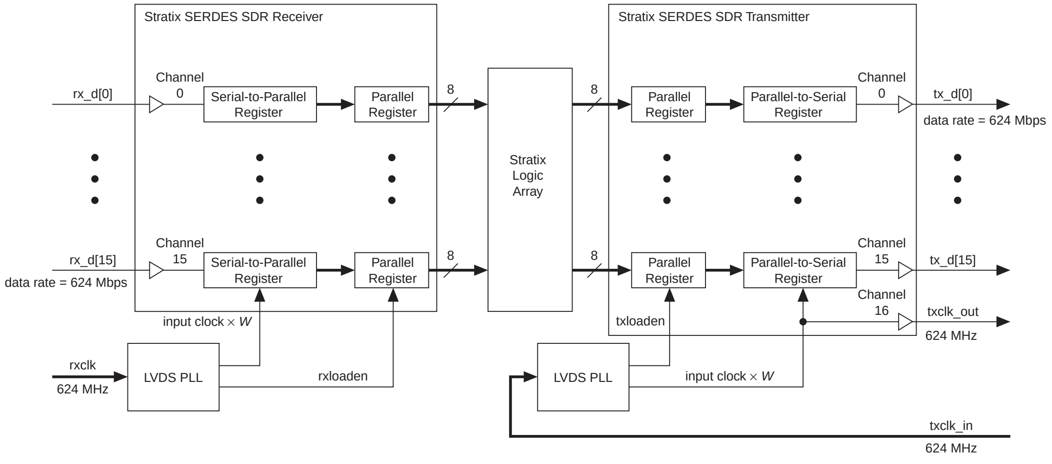


***Figure 5–12. SDR Receiver & Transmitter Circuit Connection***



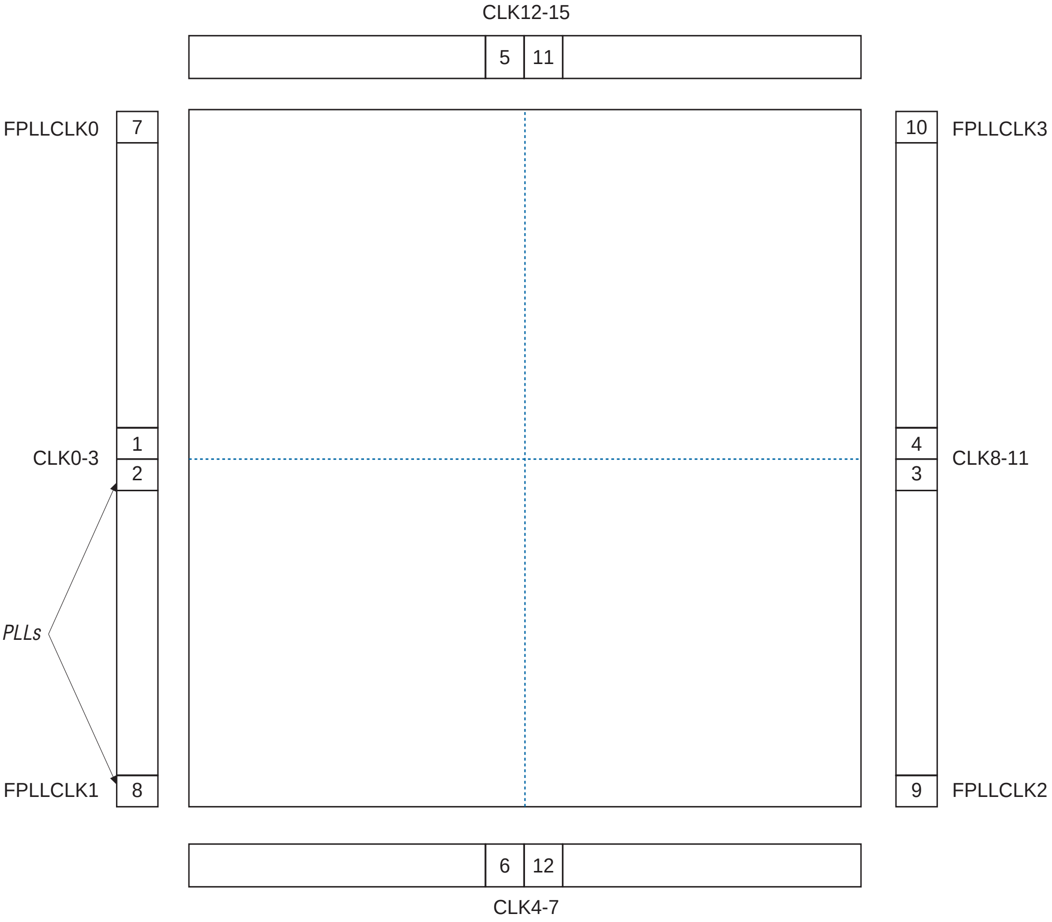
## Differential I/O Interface & Fast PLLs

Stratix devices provide 16 dedicated global clocks, 8 dedicated fast regional I/O pins, and up to 16 regional clocks (four per device quadrant) that are fed from the dedicated global clock pins or PLL outputs. The 16 dedicated global clocks are driven either by global clock input pins that support all I/O standards or from enhanced and fast PLL outputs.

Stratix devices use the fast PLLs to implement clock multiplication and division to support the SERDES circuitry. The input clock is either multiplied by the *W* feedback factor and/or divided by the *J* factor. The resulting clocks are distributed to SERDES, local, or global clock lines.

Fast PLLs are placed in the center of the left and right sides for EP1S10 to EP1S25 devices. For EP1S30 to EP1S80 devices, fast PLLs are placed in the center of the left and right sides, as well as the device corners (see Figure 5–13). These fast PLLs drive a dedicated clock network to the SERDES in the rows above and below or top and bottom of the device as shown in Figure 5–13.

*Figure 5–13. Stratix Fast PLL Positions & Clock Naming Convention* *Note (1)*



*Notes to Figure 5–13:*

(1) Dedicated clock input pins on the right and left sides do not support PCI or PCI-X.

(2) PLLs 7, 8, 9, and 10 are not available on the EP1S30 device in the 780-pin FineLine BGA® package.

## Clock Input & Fast PLL Output Relationship

Table 5–3 summarizes the PLL interface to the input clocks and the enable signal (`ENA`). Table 5–4 summarizes the clock networks each fast PLL can connect to across all Stratix family devices.

**Table 5–3. Fast PLL Clock Inputs (Including Feedback Clocks) & Enables** *Note (1)*

| Input Pin | All Stratix Devices | | | | EP1S30 to EP1S80 Devices Only | | | |
|---|---|---|---|---|---|---|---|---|
| | PLL 1 | PLL 2 | PLL 3 | PLL 4 | PLL 7 | PLL 8 | PLL 9 | PLL 10 |
| `CLK0` *(2)* | ✓ | | | | ✓ *(3)* | | | |
| `CLK1` | ✓ | | | | | | | |
| `CLK2` *(2)* | | ✓ | | | | ✓ *(3)* | | |
| `CLK3` | | ✓ | | | | | | |
| `CLK4` | | | | | | | | |
| `CLK5` | | | | | | | | |
| `CLK6` | | | | | | | | |
| `CLK7` | | | | | | | | |
| `CLK8` | | | ✓ | | | | ✓ *(3)* | |
| `CLK9` *(2)* | | | ✓ | | | | | |
| `CLK10` | | | | ✓ | | | | ✓ *(3)* |
| `CLK11` *(2)* | | | | ✓ | | | | |
| `CLK12` | | | | | | | | |
| `CLK13` | | | | | | | | |
| `CLK14` | | | | | | | | |
| `CLK15` | | | | | | | | |
| `ENA` | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| `FPLL7CLK` | | | | | ✓ | | | |
| `FPLL8CLK` | | | | | | ✓ | | |
| `FPLL9CLK` | | | | | | | ✓ | |
| `FPLL10CLK` | | | | | | | | ✓ |

*Notes to Table 5–3:*

(1) PLLs 5, 6, 11, and 12 are not fast PLLs.

(2) Clock pins `CLK0`, `CLK2`, `CLK9`, `CLK11`, and pins `FPLL[7..10]CLK` do not support Terminator technology.

(3) Either a `FPLLCLK` pin or a `CLK` pin can drive the corner fast PLLs (PLL7, PLL8, PLL9, and PLL10) when used for general purpose. `CLK` pins cannot drive these fast PLLs in high-speed differential I/O mode.

*Table 5–4. Fast PLL Relationship with Stratix Clock Networks (Part 1 of 2)* *Note (1)*

| Output Signal | All Stratix Devices | | | | EP1S30 to EP1S80 Devices Only | | | |
|---|---|---|---|---|---|---|---|---|
| | PLL 1 | PLL 2 | PLL 3 | PLL 4 | PLL 7 | PLL 8 | PLL 9 | PLL 10 |
| GCLK0 | ✓ | | | | | | | |
| GCLK1 | ✓ | | | | | | | |
| GCLK2 | | ✓ | | | | | | |
| GCLK3 | | ✓ | | | | | | |
| GCLK4 | | | ✓ | | | | | |
| GCLK9 | | | ✓ | | | | | |
| GCLK10 | | | | ✓ | | | | |
| GCLK11 | | | | ✓ | | | | |
| RCLK1 | ✓ | ✓ | | | ✓ | | | |
| RCLK2 | ✓ | ✓ | | | ✓ | | | |
| RCLK3 | ✓ | ✓ | | | | ✓ | | |
| RCLK4 | ✓ | ✓ | | | | ✓ | | |
| RCLK9 | | | ✓ | ✓ | | | ✓ | |
| RCLK10 | | | ✓ | ✓ | | | ✓ | |
| RCLK11 | | | ✓ | ✓ | | | | ✓ |
| RCLK12 | | | ✓ | ✓ | | | | ✓ |
| DIFFIOCLK1 | ✓ | | | | | | | |
| DIFFIOCLK2 | ✓ | | | | | | | |
| DIFFIOCLK3 | | ✓ | | | | | | |
| DIFFIOCLK4 | | ✓ | | | | | | |
| DIFFIOCLK5 | | | ✓ | | | | | |
| DIFFIOCLK6 | | | ✓ | | | | | |
| DIFFIOCLK7 | | | | ✓ | | | | |
| DIFFIOCLK8 | | | | ✓ | | | | |
| DIFFIOCLK9 | | | | | ✓ | | | |
| DIFFIOCLK10 | | | | | ✓ | | | |
| DIFFIOCLK11 | | | | | | ✓ | | |
| DIFFIOCLK12 | | | | | | ✓ | | |
| DIFFIOCLK13 | | | | | | | ✓ | |

*Table 5–4. Fast PLL Relationship with Stratix Clock Networks (Part 2 of 2) Note (1)*

| Output Signal | All Stratix Devices | | | | EP1S30 to EP1S80 Devices Only | | | |
|---|---|---|---|---|---|---|---|---|
| | PLL 1 | PLL 2 | PLL 3 | PLL 4 | PLL 7 | PLL 8 | PLL 9 | PLL 10 |
| `DIFFIOCLK14` | | | | | | | ✓ | |
| `DIFFIOCLK15` | | | | | | | | ✓ |
| `DIFFIOCLK16` | | | | | | | | ✓ |

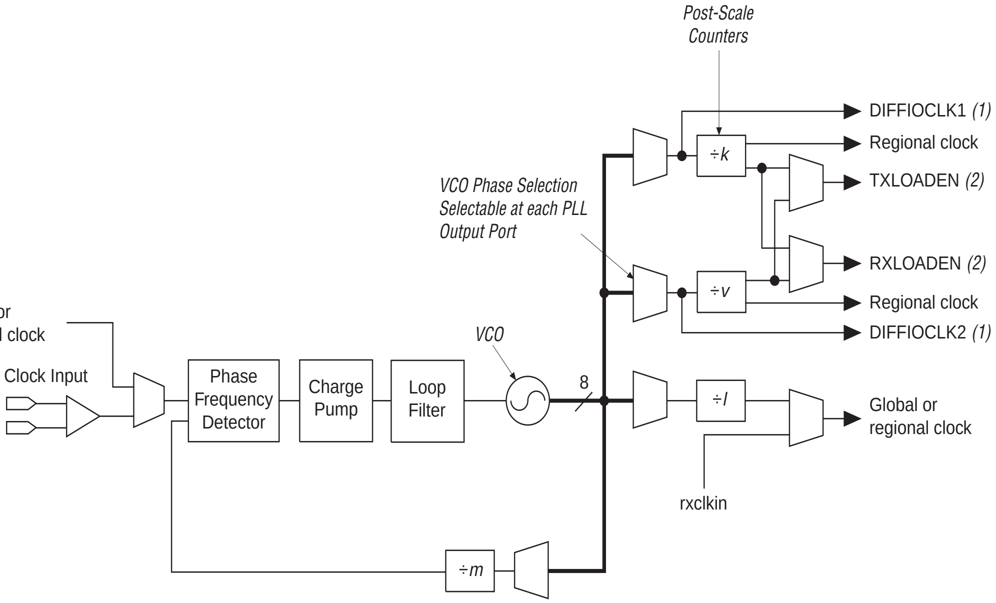
***Note to Table 5–4:***

(1) PLLs 5, 6, 11, and 12 are not fast PLLs.

## Fast PLL Specifications

You can drive the fast PLLs by an external pin or any one of the sectional clocks [21:0]. You can connect the clock input directly to local or global clock lines, as shown in Figure 5–14. You cannot use the sectional-clock inputs to the fast PLL's input multiplexer for the receiver PLL. You can only use the sectional clock inputs in the transmitter only mode or as a general purpose PLL.

*Figure 5–14. Fast PLL Block Diagram*



*Notes to Figure 5–14:*
(1) In high-speed differential I/O mode, the high-speed PLL clock feeds the SERDES. Stratix devices only support one rate of data transfer per fast PLL in high-speed differential I/O mode.
(2) Control signal for high-speed differential I/O SERDES.

You can multiply the input clock by a factor of 1 to 16. The multiplied clock is used for high-speed serialization or deserialization operations. Fast PLL specifications are shown in Section I, Stratix Device Family Data Sheet of the *Stratix Device Handbook, Volume 1*. The voltage controlled oscillators (VCOs) are designed to operate within the frequency range of 300 to 840 MHz, to provide data rates of up to 840 Mbps.

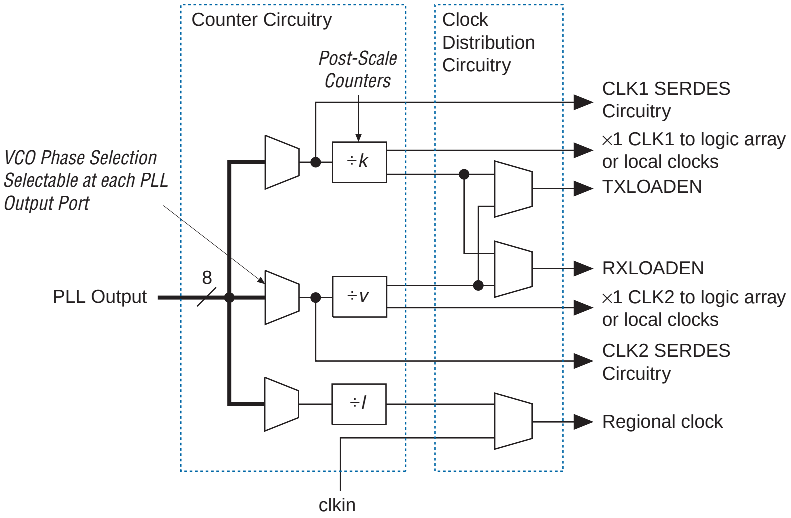
## High-Speed Phase Adjust

There are eight phases of the multiplied clock at the PLL output, each delayed by 45° from the previous clock and synchronized with the original clock. The three multiplexers (shown in Figure 5–14) select one of the delayed, multiplied clocks. The PLL output drives the three counters *k*, *v*, and *l*. You can program the three individual post scale counters (*k*, *v*, and *l*) independently for division ratio or phase. The selected PLL output is used for the serialization or deserialization process in SERDES.

## Counter Circuitry

The multiplied clocks bypass the counter taps *k* and *v* to directly feed the SERDES serial registers. These two taps also feed to the quadrant local clock network and the dedicated `RXLOADENA` or `TXLOADENA` pins, as shown in Figure 5–15. Both *k* and *v* are utilized simultaneously during the data-realignment procedure. When the design does not use the data realignment, both `TXLOADEN` and `RXLOADEN` pins use a single counter.

**Figure 5–15. Fast PLL Connection to Logic Array**



The Stratix device fast PLL has another `GCLK` connection for general-purpose applications. The third tap *l* feeds the quadrant local clock as well as the global clock network. You can use the *l* counter's multiplexer for applications requiring the device to connect the incoming clock directly to the local or global clocks. You can program the multiplexer to connect the `RXCLKIN` signal directly to the local or global clock lines. Figure 5–15 shows the connection between the incoming clock, the *l* tap, and the local or global clock lines.

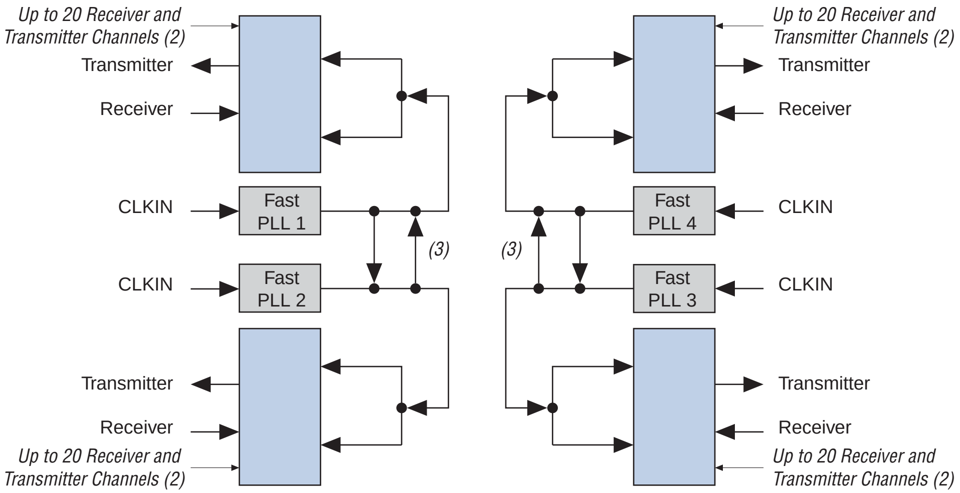
The differential clock selection is made per differential bank. Since the length of the clock tree limits the performance, each fast PLL should drive only one differential bank.

## Fast PLL SERDES Channel Support

The Quartus II MegaWizard Plug-In Manager only allows you to implement up to 20 receiver or 20 transmitter channels for each fast PLL. These channels operate at up to 840 Mbps. For more information on implementing more than 20 channels, see "Fast PLLs" on page 5–51. The receiver and transmitter channels are interleaved such that each I/O bank on the left and right side of the device has one receiver channel and one transmitter channel per row. Figure 5–16 shows the fast PLL and channel layout in EP1S10, EP1S20, and EP1S25 devices. Figure 5–17 shows the fast PLL and channel layout in EP1S30 to EP1S80 devices.

For more the number of channels in each device, see the Tables 5–10 through 5–14.

**Figure 5–16. Fast PLL & Channel Layout in EP1S10, EP1S20 & EP1S25 Devices** *Note (1)*



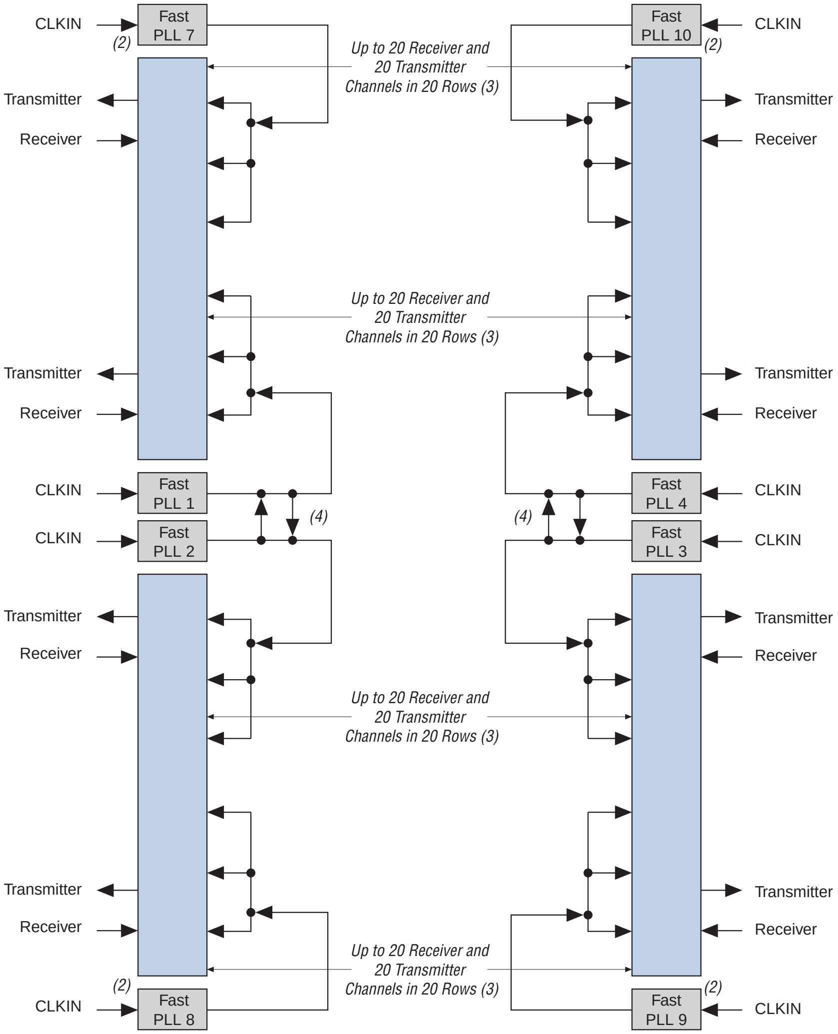
*Notes to Figure 5–16:*

(1) Wire-bond packages only support up to 462 Mbps until characterization shows otherwise.

(2) See Tables 5–10 through 5–14 for the exact number of channels each package and device density supports.

(3) There is a multiplexer here to select the PLL clock source. If a PLL uses this multiplexer to clock channels outside of its bank quadrant (e.g., if PLL 2 clocks PLL 1's channel region), those clocked channels support up to 462 Mbps.

***Figure 5–17. Fast PLL & Channel Layout in EP1S30 to EP1S80 Devices*** *Note (1)*



*Notes to Figure 5–17:*

(1) Wire-bond packages only support up to 462-Mbps until characterization shows otherwise.

(2) For EP1S80 devices, the fast PLLs located at the corners of the device support up to 462 Mbps except for the EP1S80 device in the 1,508-pin FineLine BGA package. The corner fast PLLs of this device support up to 840 Mbps.

(3) See Tables 5–10 through 5–14 for the exact number of channels each package and device density supports.

(4) There is a multiplexer here to select the PLL clock source. If a PLL uses this multiplexer to clock channels outside of its bank quadrant (e.g., if PLL 2 clocks PLL 1's channel region), those clocked channels support up to 462 Mbps.

### Advanced Clear & Enable Control

There are several control signals for clearing and enabling PLLs and their outputs. You can use these signals to control PLL resynchronization and to gate PLL output clocks for low-power applications.

The `PLLENABLE` pin is a dedicated pin that enables and disables Stratix device enhanced and fast PLLs. When the `PLLENABLE` pin is low, the clock output ports are driven by `GND` and all the PLLs go out of lock. When the `PLLENABLE` pin goes high again, the PLLs relock and resynchronize to the input clocks.

The reset signals are reset/resynchronization inputs for each enhanced PLL. Stratix devices can drive these input signals from an input pin or from LEs. When driven high, the PLL counters reset, clearing the PLL output and placing the PLL out of lock. When driven low again, the PLL resynchronizes to its input as it relocks.

## Receiver Data Realignment

Most systems using serial differential I/O data transmission require a certain data-realignment circuit. Stratix devices contain embedded data-realignment circuitry. While normal I/O operation guarantees that data is captured, it does not guarantee the parallelization boundary, as this point is randomly determined based on the power-up of both communicating devices. The data-realignment circuitry corrects for bit misalignments by shifting, or delaying, data bits.

### Data Realignment Principles of Operation

Stratix devices use a realignment and clock distribution circuitry (described in "Counter Circuitry" on page 5–22) for data realignment.

Set the internal `rx_data_align` node end high to assert the data-realignment circuitry. When this node is switched from a low to a high state, the realignment circuitry is activated and the data is delayed by one bit. To ensure the rising edge of the `rx_data_align` node end is latched into the PLL, the `rx_data_align` node end should stay high for at least two low-frequency clock cycles.

An external circuit or an internal custom-made state machine using LEs can generate the signal to pull the `rx_data_align` node end to a high state.

When the data realignment circuitry is activated, it generates an internal pulse Sync S1 or Sync S2 that disables one of the two counters used for the SERDES operation (described in "Counter Circuitry" on page 5–22). One counter is disabled for one high-frequency clock cycle, delaying the

`RXLOADEN` signal and dropping the first incoming bit of the serial input data stream located in the first serial register of the SERDES circuitry (shown in Figure 5–3 on page 5–8).

Figure 5–18 shows the function-timing diagram of a Stratix SERDES in normal ×8 mode, and Figure 5–19 shows the function-timing diagrams of a Stratix SERDES when data realignment is used.

*Figure 5–18. SERDES Function Timing Diagram in Normal Operation*

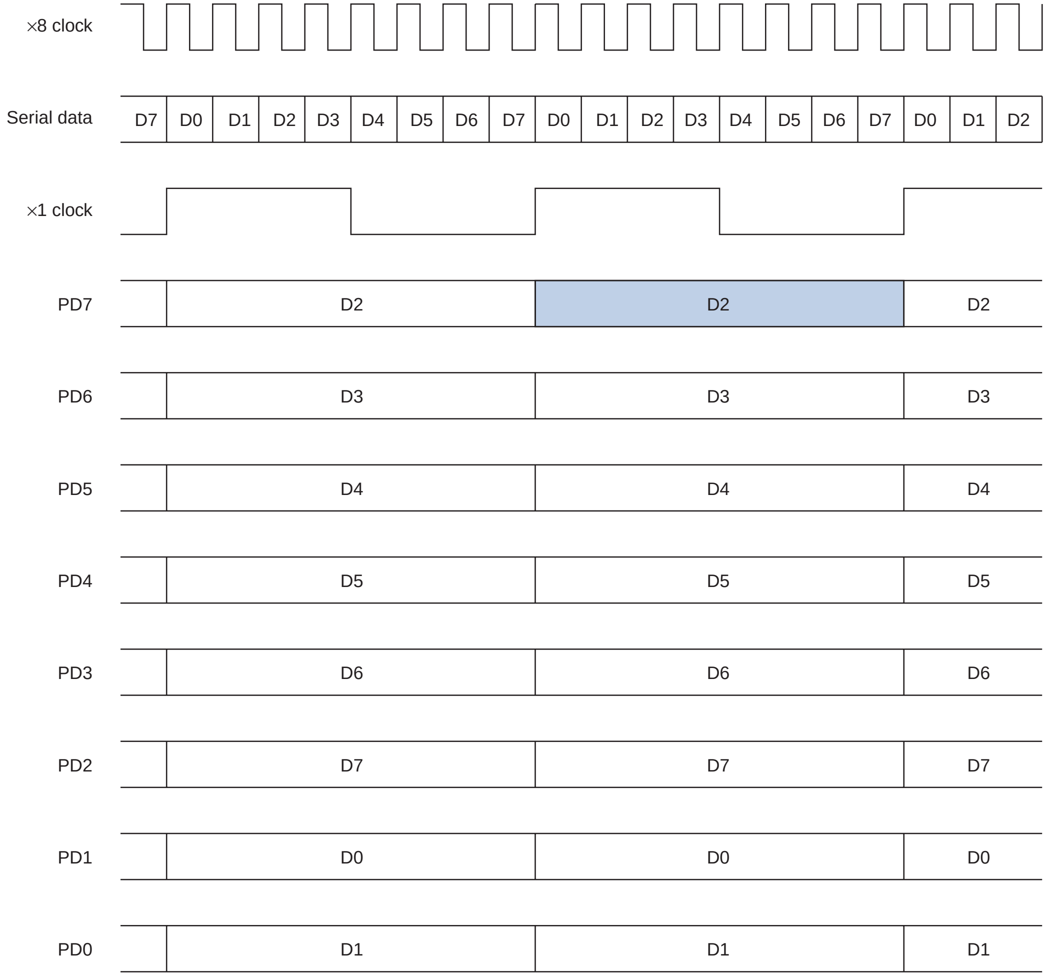
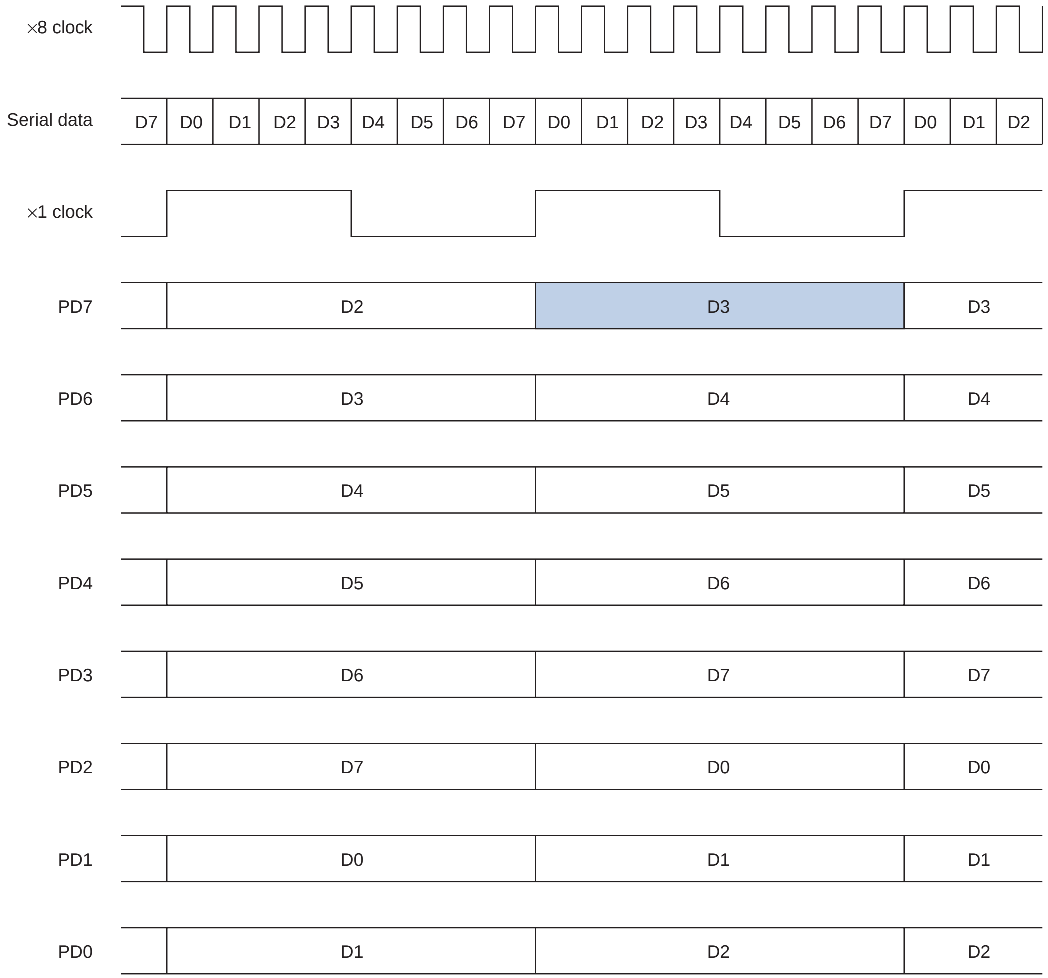


*Figure 5–19. SERDES Function Timing Diagram with Data-Realignment Operation*



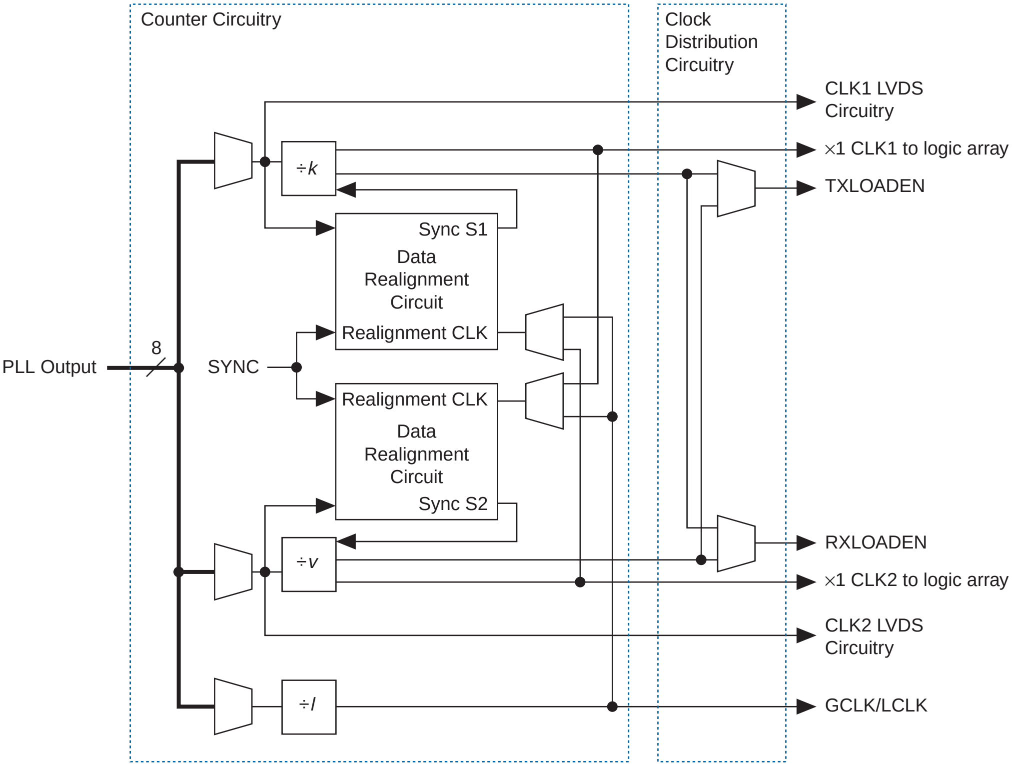
## Generating TXLOADEN Signal

The `TXLOADEN` signal controls the transfer of data between the SERDES circuitry and the logic array when data realignment is used. To prevent the interruption of the `TXLOADEN` signal during data realignment, both *k* and *v* counter are used.

In normal operation the `TXLOADEN` signal is generated by the *k* counter. However, during the data-realignment operation this signal is generated by either counter. When the *k* counter is used for realignment, the

`TXLOADEN` signal is generated by the *v* counter, and when the *v* counter is used for realignment, the `TXLOADEN` signal is generated by the *k* counter, as shown in Figure 5–20.

***Figure 5–20. Realignment Circuit TXLOADEN Signal Control*** *Note (1)*



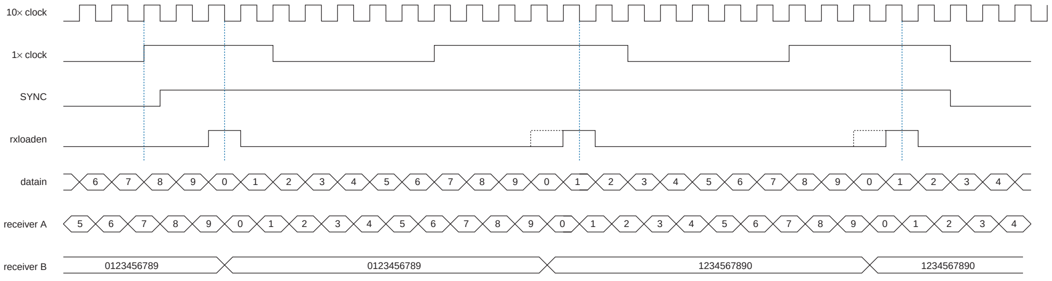
***Note to Figure 5–20:***

(1) This figure does not show additional realignment circuitry.

## Realignment Implementation

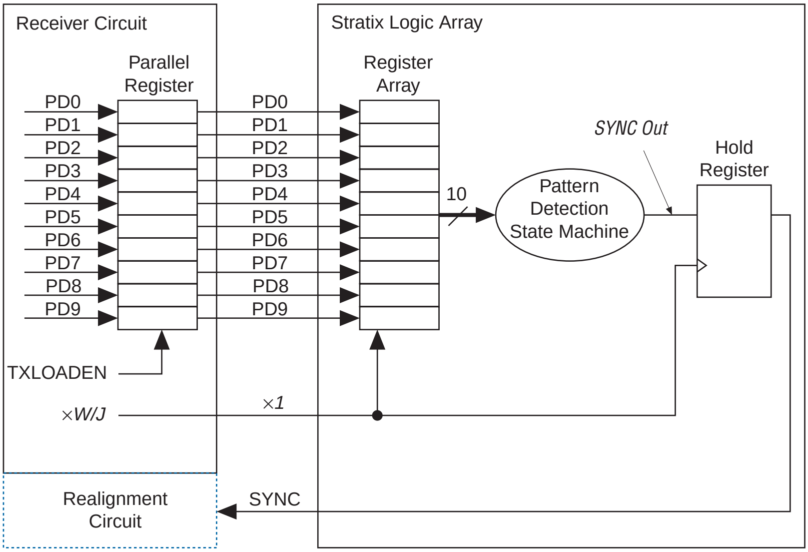
The realignment signal (`SYNC`) is used for data realignment and reframing. An external pin (`RX_DATA_ALIGN`) or an internal signal controls the `rx_data_align` node end. When the `rx_data_align` node end is asserted high for at least two low-frequency clock cycles, the `RXLOADEN` signal is delayed by one high-frequency clock period and the parallel bits shift by one bit. Figure 5–21 shows the timing relationship between the high-frequency clock, the `RXLOADEN` signal, and the parallel data.

### Figure 5–21. Realignment by rx_data_align Node End



A state machine can generate the realignment signal to control the alignment procedure. Figure 5–22 shows the connection between the realignment signal and the `rx_data_align` node end.

### Figure 5–22. SYNC Signal Path to Realignment Circuit



To guarantee that the `rx_data_align` signal generated by a user state machine is latched correctly by the counters, the user circuit must meet certain requirements.

- The design must include an input synchronizing register to ensure that data is synchronized to the ×1 clock.

- After the pattern detection state machine, use another synchronizing register to capture the generated `SYNC` signal and synchronize it to the ×1 clock.
- Since the skew in the path from the output of this synchronizing register to the PLL is undefined, the state machine must generate a pulse that is high for two ×1 clock periods.
- Since the `SYNC` generator circuitry only generates a single fast clock period pulse for each `SYNC` pulse, you cannot generate additional `SYNC` pulses until the comparator signal is reset low.
- To guarantee the pattern detection state machine does not incorrectly generate multiple `SYNC` pulses to shift a single bit, the state machine must hold the `SYNC` signal low for at least three ×1 clock periods between pulses.

## Source-Synchronous Timing Budget

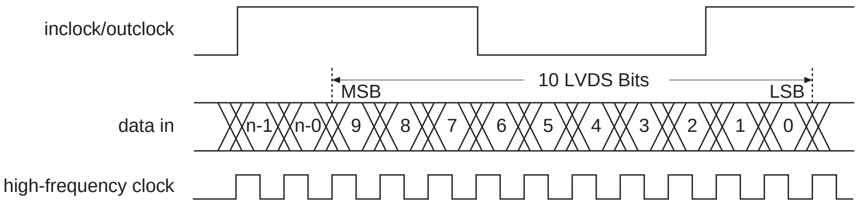
This section discusses the timing budget, waveforms, and specifications for source-synchronous signaling in Stratix devices. LVDS, LVPECL, PCML, and HyperTransport I/O standards enable high-speed data transmission. This high data-transmission rate results in better overall system performance. To take advantage of fast system performance, you must understand how to analyze timing for these high-speed signals. Timing analysis for the differential block is different from traditional synchronous timing analysis techniques.

Rather than focusing on clock-to-output and setup times, source-synchronous timing analysis is based on the skew between the data and the clock signals. High-speed differential data transmission requires you to use timing parameters provided by IC vendors and to consider board skew, cable skew, and clock jitter. This section defines the source-synchronous differential data orientation timing parameters, and timing budget definitions for Stratix devices, and explains how to use these timing parameters to determine a design's maximum performance.

### Differential Data Orientation

There is a set relationship between an external clock and the incoming data. For operation at 840 Mbps and $W = 10$, the external clock is multiplied by 10 and phase-aligned by the PLL to coincide with the sampling window of each data bit. The third falling edge of high-frequency clock is used to strobe the incoming high-speed data. Therefore, the first two bits belong to the previous cycle. Figure 5–23 shows the data bit orientation of the ×10 mode as defined in the Quartus II software.

*Figure 5–23. Bit Orientation in the Quartus II Software*



## Differential I/O Bit Position

Data synchronization is necessary for successful data transmission at high frequencies. Figure 5–24 shows the data bit orientation for a receiver channel operating in ×8 mode. Similar positioning exists for the most significant bits (MSBs) and least significant bits (LSBs) after deserialization, as listed in Table 5–5.

*Figure 5–24. Bit Order for One Channel of Differential Data*

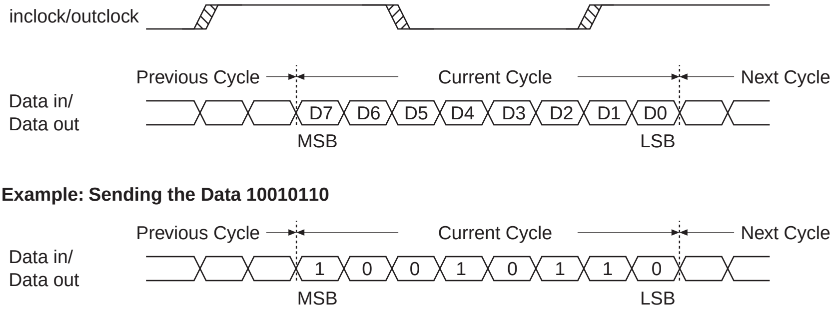


Table 5–5 shows the conventions for differential bit naming for 18 differential channels. However, the MSB and LSB are increased with the number of channels used in a system.

*Table 5–5. LVDS Bit Naming*

| Receiver Data Channel Number | Internal 8-Bit Parallel Data | |
|---|---|---|
| | MSB Position | LSB Position |
| 1 | 7 | 0 |
| 2 | 15 | 8 |
| 3 | 23 | 16 |
| 4 | 31 | 24 |
| 5 | 39 | 32 |
| 6 | 47 | 40 |
| 7 | 55 | 48 |
| 8 | 63 | 56 |
| 9 | 71 | 64 |
| 10 | 79 | 72 |
| 11 | 87 | 80 |
| 12 | 95 | 88 |
| 13 | 103 | 96 |
| 14 | 111 | 104 |
| 15 | 119 | 112 |
| 16 | 127 | 120 |
| 17 | 135 | 128 |
| 18 | 143 | 136 |

## Timing Definition

The specifications used to define high-speed timing are described in Tables 5–6 and 5–7. .

*Table 5–6. High-Speed Timing Specifications & Terminology (Part 1 of 2)*

| High-Speed Timing Specification | Terminology |
|---|---|
| $t_C$ | High-speed receiver/transmitter input and output clock period. |
| $f_{HSCLK}$ | High-speed receiver/transmitter input and output clock frequency. |
| $t_{RISE}$ | Low-to-high transmission time. |

*Table 5–6. High-Speed Timing Specifications & Terminology (Part 2 of 2)*

| High-Speed Timing Specification | Terminology |
|---|---|
| $t_{FALL}$ | High-to-low transmission time. |
| Timing unit interval (TUI) | The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency × Multiplication Factor) = $t_C/w$). |
| $f_{HSDR}$ | Maximum LVDS data transfer rate ($f_{HSDR}$ = 1/TUI). |
| Channel-to-channel skew (TCCS) | The timing difference between the fastest and slowest output edges, including $t_{CO}$ variation and clock skew. The clock is included in the TCCS measurement. |
| Sampling window (SW) | The period of time during which the data must be valid in order for you to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window.<br>SW = $t_{SW}$ (max) – $t_{SW}$ (min). |
| Input jitter (peak-to-peak) | Peak-to-peak input jitter on high-speed PLLs. |
| Output jitter (peak-to-peak) | Peak-to-peak output jitter on high-speed PLLs. |
| $t_{DUTY}$ | Duty cycle on high-speed transmitter output clock. |
| $t_{LOCK}$ | Lock time for high-speed transmitter and receiver PLLs. |

*Table 5–7. High-Speed I/O Specifications for Flip-Chip Packages Notes (1), (2) (Part 1 of 3)*

| Symbol | Conditions | -5 Speed Grade | | | -6 Speed Grade | | | -7 Speed Grade | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{HSCLK}$ (Clock frequency) (LVDS, LVPECL, HyperTransport technology) | $W$ = 10 | 30 | | 84 | 30 | | 84 | 30 | | 62.4 | MHz |
| | $W$ = 8 | 37.5 | | 105 | 37.5 | | 105 | 37.5 | | 78 | MHz |
| | $W$ = 7 | 42.9 | | 120 | 42.9 | | 120 | 42.9 | | 89.14 | MHz |
| | $W$ = 4 | 75 | | 210 | 75 | | 210 | 75 | | 156 | MHz |
| | $W$ = 2 | 150 | | 420 | 150 | | 420 | 150 | | 231 | MHz |
| | $W$ = 1 (LVDS and LVPECL only) | 300 | | 717 | 300 | | 717 | 300 | | 462 | MHz |
| $f_{HSPR}$ Device operation (LVDS, LVPECL, HyperTransport technology) | $J$ = 10 | 300 | | 840 | 300 | | 840 | 300 | | 624 | Mbps |
| | $J$ = 8 | 300 | | 840 | 300 | | 840 | 300 | | 624 | Mbps |
| | $J$ = 7 | 300 | | 840 | 300 | | 840 | 300 | | 624 | Mbps |
| | $J$ = 4 | 300 | | 840 | 300 | | 840 | 300 | | 624 | Mbps |
| | $J$ = 2 | 100 | | 462 | 100 | | 462 | 100 | | 462 | Mbps |
| | $J$ = 1 (LVDS and LVPECL only) | 100 | | 462 | 100 | | 462 | 100 | | 462 | Mbps |

*Table 5–7. High-Speed I/O Specifications for Flip-Chip Packages Notes (1), (2) (Part 2 of 3)*

| Symbol | Conditions | -5 Speed Grade | | | -6 Speed Grade | | | -7 Speed Grade | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{HSCLK}$ (Clock frequency) (PCML) | $W$ = 10 | 30 | | 40 | 30 | | 40 | 30 | | 31.1 | MHz |
| | $W$ = 8 | 37.5 | | 50 | 37.5 | | 50 | 37.5 | | 38.87 | MHz |
| | $W$ = 7 | 42.9 | | 57.14 | 42.9 | | 57.14 | 42.9 | | 44.43 | MHz |
| | $W$ = 4 | 75 | | 100 | 75 | | 100 | 75 | | 77.75 | MHz |
| | $W$ = 2 | 50 | | 200 | 50 | | 200 | 50 | | 150 | MHz |
| | $W$ = 1 | 100 | | 250 | 100 | | 250 | 100 | | 200 | MHz |
| $f_{HSDR}$ Device operation (PCML) | $J$ = 10 | 300 | | 400 | 300 | | 400 | 300 | | 311 | Mbps |
| | $J$ = 8 | 300 | | 400 | 300 | | 400 | 300 | | 311 | Mbps |
| | $J$ = 7 | 300 | | 400 | 300 | | 400 | 300 | | 311 | Mbps |
| | $J$ = 4 | 300 | | 400 | 300 | | 400 | 300 | | 311 | Mbps |
| | $J$ = 2 | 100 | | 400 | 100 | | 400 | 100 | | 300 | Mbps |
| | $J$ = 1 | 100 | | 250 | 100 | | 250 | 100 | | 200 | Mbps |
| TCCS | All | | | ±100 | | | ±100 | | | ±150 | ps |
| SW | PCML ($J$ = 4, 7, 8, 10) | | | 750 | | | 750 | | | 800 | ps |
| | PCML ($J$ = 2) | | | 900 | | | 900 | | | 1,200 | ps |
| | PCML ($J$ = 1) | | | 1,500 | | | 1,500 | | | 1,700 | ps |
| | LVDS and LVPECL ($J$ = 1) | | | 500 | | | 500 | | | 550 | ps |
| | LVDS, LVPECL, HT ($J$ = 2 through 10) | | | 440 | | | 440 | | | 500 | ps |
| Input jitter tolerance (peak-to-peak) | All | | | 250 | | | 250 | | | 250 | ps |
| Output jitter (peak-to-peak) | All | | | 160 | | | 160 | | | 200 | ps |
| Output $t_{RISE}$ | LVDS | 80 | 110 | 120 | 80 | 110 | 120 | 80 | 110 | 120 | ps |
| | HyperTransport technology | 110 | 170 | 200 | 110 | 170 | 200 | 120 | 170 | 200 | ps |
| | LVPECL | 90 | 130 | 150 | 90 | 130 | 150 | 100 | 135 | 150 | ps |
| | PCML | 80 | 110 | 135 | 80 | 110 | 135 | 80 | 110 | 135 | ps |

**Table 5–7. High-Speed I/O Specifications for Flip-Chip Packages Notes (1), (2) (Part 3 of 3)**

| Symbol | Conditions | -5 Speed Grade | | | -6 Speed Grade | | | -7 Speed Grade | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Output $t_{FALL}$ | LVDS | 80 | 110 | 120 | 80 | 110 | 120 | 80 | 110 | 120 | ps |
| | HyperTransport technology | 110 | 170 | 200 | 110 | 170 | 200 | 110 | 170 | 200 | ps |
| | LVPECL | 90 | 130 | 160 | 90 | 130 | 160 | 100 | 135 | 160 | ps |
| | PCML | 105 | 140 | 175 | 105 | 140 | 175 | 110 | 145 | 175 | ps |
| $t_{DUTY}$ | LVDS ($J$ = 2 through 10) | 47.5 | 50 | 52.5 | 47.5 | 50 | 52.5 | 47.5 | 50 | 52.5 | % |
| | LVDS ($J$ =1) and LVPECL, PCML, HT | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | % |
| $t_{LOCK}$ | All | | | 100 | | | 100 | | | 100 | µs |

*Notes for Table 5–7:*

(1) When J=4, 7, 8, and 10, the SERDES block is used.

(2) When J=2 or J=1, the SERDES is bypassed.

**Table 5–8. High-Speed I/O Specifications for Wire-Bond Packages (Part 1 of 3)**

| Symbol | Conditions | -6 Speed Grade | | | -7 Speed Grade | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| $f_{HSCLK}$ (clock frequency) (LVDS,LVPECL, HyperTransport technology) | W = 10 | 30 | | 62.4 | 30 | | 46 | MHz |
| | W = 8 | 37.5 | | 78 | 37.5 | | 57.5 | MHz |
| | W = 7 | 42.9 | | 89.14 | 42.9 | | 65.71 | MHz |
| | W = 4 | 75 | | 156 | 75 | | 115 | MHz |
| | W = 2 | 50 | | 231 | 50 | | 230 | MHz |
| | W = 1 (LVDS and LVPECL only) | 100 | | 311 | 100 | | 311 | MHz |
| Device operation, $f_{HSDR}$ (LVDS,LVPECL, HyperTransport technology) | J = 10 | 300 | | 624 | 300 | | 460 | Mbps |
| | J = 8 | 300 | | 624 | 300 | | 460 | Mbps |
| | J = 7 | 300 | | 624 | 300 | | 460 | Mbps |
| | J = 4 | 300 | | 624 | 300 | | 460 | Mbps |
| | J = 2 | 100 | | 462 | 100 | | 460 | Mbps |
| | J = 1 (LVDS and LVPECL only) | 100 | | 311 | 100 | | 270 | Mbps |

**Table 5–8. High-Speed I/O Specifications for Wire-Bond Packages (Part 2 of 3)**

| Symbol | Conditions | -6 Speed Grade | | | -7 Speed Grade | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| $f_{HSCLK}$ (clock frequency) (PCML) | W = 10 | 30 | | 31.1 | | | | MHz |
| | W = 8 | 37.5 | | 38.87 | | | | MHz |
| | W = 7 | 42.9 | | 44.43 | | | | MHz |
| | W = 4 | 75 | | 77.75 | | | | MHz |
| | W = 2 | 50 | | 150 | 50 | | 150 | MHz |
| | W = 1 | 100 | | 200 | 100 | | 200 | MHz |
| Device operation, $f_{HSDR}$ (PCML) | J = 10 | 300 | | 311 | | | | Mbps |
| | J = 8 | 300 | | 311 | | | | Mbps |
| | J = 7 | 300 | | 311 | | | | Mbps |
| | J = 4 | 300 | | 311 | | | | Mbps |
| | J = 2 | 100 | | 300 | 100 | | 155 | Mbps |
| | J = 1 | 100 | | 200 | 100 | | 155 | Mbps |
| TCCS | All | | | ± 200 | | | ± 200 | ps |
| SW | PCML (J = 4, 7, 8, 10) only | | | 800 | | | 800 | ps |
| | PCML (J = 2) only | | | 1,200 | | | 1,200 | ps |
| | PCML (J = 1) only | | | 1,700 | | | 1,700 | ps |
| | LVDS and LVPECL (J = 1) only | | | 550 | | | 550 | ps |
| | LVDS, LVPECL, HT (J = 2..10) only | | | 500 | | | 500 | ps |
| Input jitter tolerance (peak-to-peak) | All | | | 250 | | | 250 | ps |
| Output jitter (peak-to-peak) | All | | | 200 | | | 200 | ps |
| Output $t_{RISE}$ | LVDS | 80 | 110 | 120 | 80 | 110 | 120 | ps |
| | HyperTransport | 120 | 170 | 200 | 120 | 170 | 200 | ps |
| | LVPECL | 100 | 135 | 150 | 100 | 135 | 150 | ps |
| | PCML | 80 | 110 | 135 | 80 | 110 | 135 | ps |
| Output $t_{FALL}$ | LVDS | 80 | 110 | 120 | 80 | 110 | 120 | ps |
| | HyperTransport | 110 | 170 | 200 | 110 | 170 | 200 | ps |
| | LVPECL | 100 | 135 | 160 | 100 | 135 | 160 | ps |
| | PCML | 110 | 145 | 175 | 110 | 145 | 175 | ps |

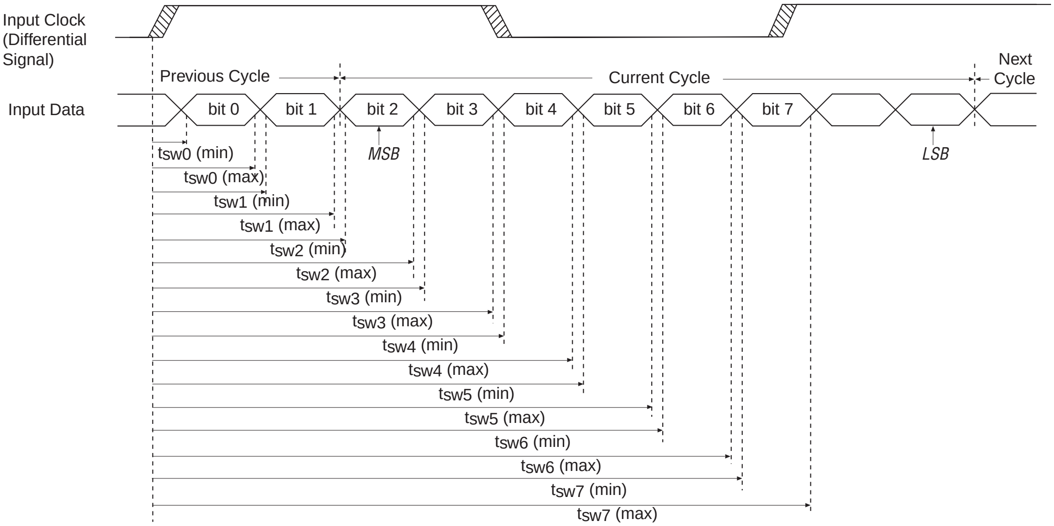
*Table 5–8. High-Speed I/O Specifications for Wire-Bond Packages (Part 3 of 3)*

| Symbol | Conditions | -6 Speed Grade | | | -7 Speed Grade | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| $t_{DUTY}$ | LVDS (J =2..10) only | 47.5 | 50 | 52.5 | 47.5 | 50 | 52.5 | % |
| | LVDS (J =1) and LVPECL, PCML, HT | 45 | 50 | 55 | 45 | 50 | 55 | % |
| $t_{LOCK}$ | All | | | 100 | | | 100 | us |

## Input Timing Waveform

Figure 5–25 illustrates the essential operations and the timing relationship between the clock cycle and the incoming serial data. For a functional description of the SERDES, see "Principles of SERDES Operation" on page 5–6.

*Figure 5–25. Input Timing Waveform* Note (1)



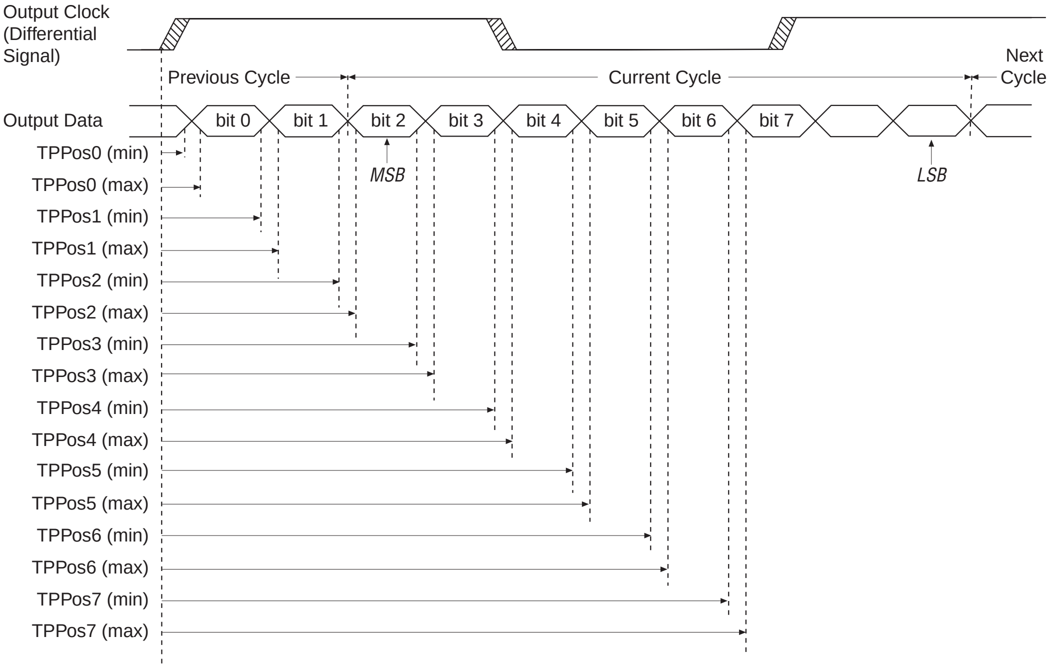
*Note to Figure 5–25:*

(1) The timing specifications are referenced at a 100-mV differential voltage.

## Output Timing

The output timing waveform in Figure 5–26 illustrates the relationship between the output clock and the serial output data stream.

*Figure 5–26. Output Timing Waveform* *Note (1)*



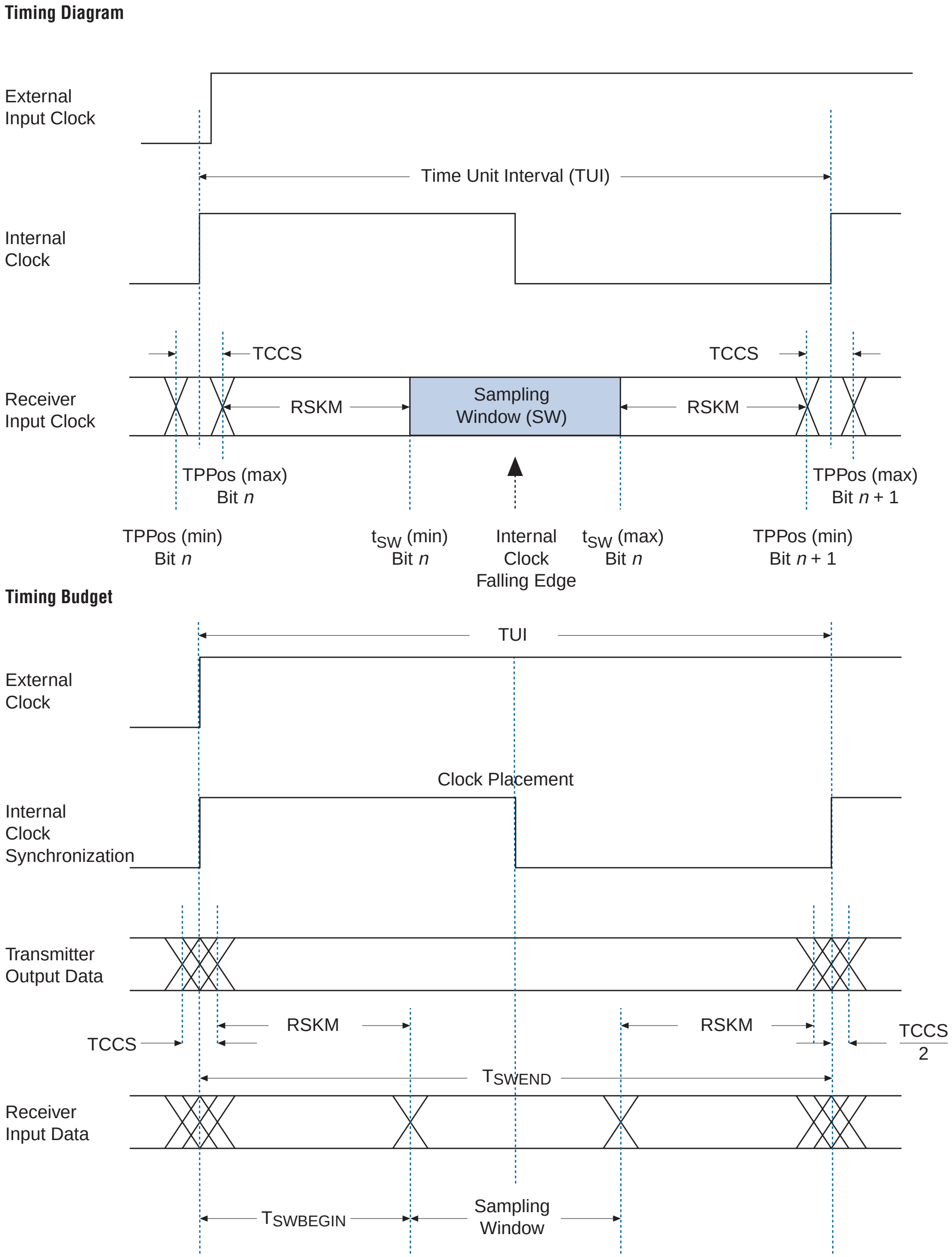
*Note to Figure 5–26:*

(1) The timing specifications are referenced at a 250-mV differential voltage.

## Receiver Skew Margin

Change in system environment, such as temperature, media (cable, connector, or PCB) loading effect, a receiver's inherent setup and hold, and internal skew, reduces the sampling window for the receiver. The timing margin between receiver's clock input and the data input sampling window is known as RSKM. Figure 5–27 illustrates the relationship between the parameter and the receiver's sampling window.

*Figure 5–27. Differential High-Speed Timing Diagram & Timing Budget*



### Switching Characteristics

Timing specifications for Stratix devices are listed in Tables 5–7 and 5–8. You can also find Stratix device timing information in Section I, Stratix Device Family Data Sheet of the *Stratix Device Handbook, Volume 1*.

### Timing Analysis

Differential timing analysis is based on skew between data and the clock signals. For static timing analysis, the timing characteristics of the differential I/O standards are guaranteed by design and depend on the frequency at which they are operated. Use the values in Section I, Stratix Device Family Data Sheet of the *Stratix Device Handbook, Volume 1* to calculate system timing margins for various I/O protocols. For detailed descriptions and implementations of these protocols, refer to the Altera web site at www.altera.com.

## SERDES Bypass DDR Differential Signaling

Each Stratix device high-speed differential I/O channel can transmit or receive data in by-two (×2) mode at up to 462 Mbps using PLLs. These pins do not require dedicated SERDES circuitry and they implement serialization and deserialization with minimal logic.

### SERDES Bypass DDR Differential Interface Review

Stratix devices use dedicated DDR circuitry to implement ×2 differential signaling. Although SDR circuitry samples data only at the positive edge of the clock, DDR captures data on both the rising and falling edges for twice the transfer rate of SDR. Stratix device shift registers, internal global PLLs, and I/O cells can perform serial-to-parallel conversions on incoming data and parallel-to-serial conversion on outgoing data.

### Clock Domains

The SERDES bypass differential signaling can use any of the many clock domains available in Stratix devices. These clock domains fall into four categories: global, regional, fast regional, and internally generated.

General-purpose PLLs generate the global clock domains. The fast PLLs can generate additional global clocks domains. Each PLL features two taps that directly drive two unique global clock networks. A dedicated clock pin drives each general-purpose PLL. These clock lines are utilized when designing for speeds up to 462 Mbps. Tables 5–3 and 5–4 on page 5–19, respectively, show the available clocks in Stratix devices.

## SERDES Bypass DDR Differential Signaling Receiver Operation

The SERDES bypass differential signaling receiver uses the Stratix device DDR input circuitry to receive high-speed serial data. The DDR input circuitry consists of a pair of shift registers used to capture the high-speed serial data, and a latch.

One register captures the data on the positive edge of the clock (generated by PLL) and the other register captures the data on the negative edge of the clock. Because the data captured on the negative edge is delayed by one-half of the clock cycle, it is latched before it interfaces with the system logic.

Figure 5–28 shows the DDR timing relationship between the incoming serial data and the clock. In this example, the `inclock` signal is running at half the speed of the incoming data. However, other combinations are also possible. Figure 5–29 shows the DDR input and the other modules used in a Flexible-LVDS receiver design to interface with the system logic.

*Figure 5–28. ×2 Timing Relation between Incoming Serial Data & Clock*

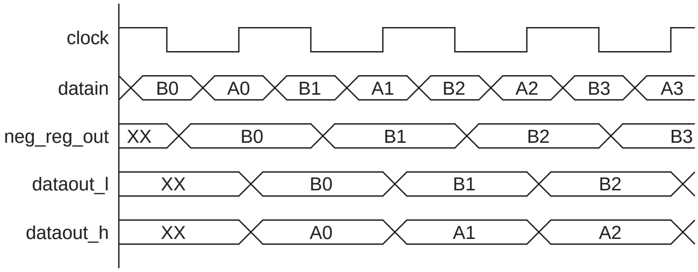
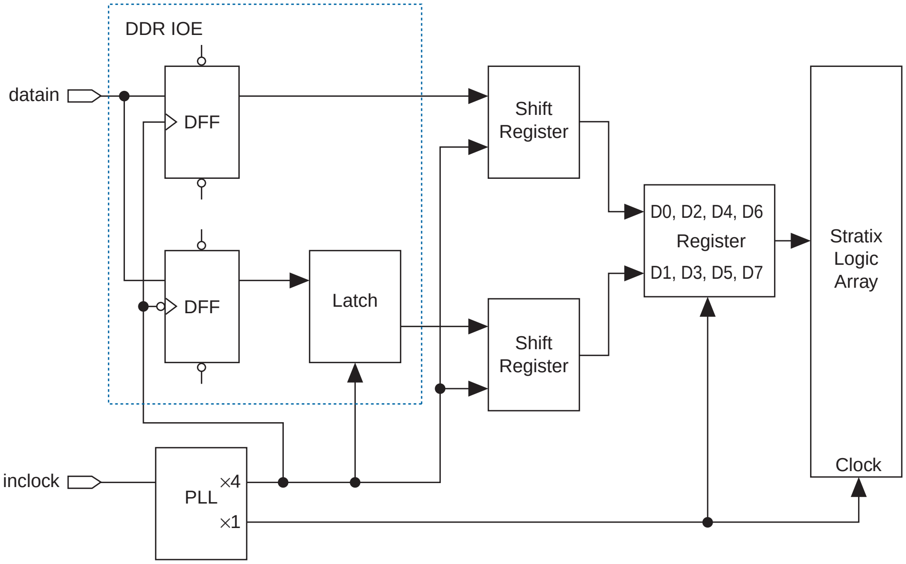


*Figure 5–29. ×2 Data Rate Receiver Channel with Deserialization Factor of 8*



## SERDES Bypass DDR Differential Signaling Transmitter Operation

The ×2 differential signaling transmitter uses the Stratix device DDR output circuitry to transmit high-speed serial data. The DDR output circuitry consists of a pair of shift registers and a multiplexer. The shift registers capture the parallel data on the clock's rising edge (generated by the PLL), and a multiplexer transmits the data in sync with the clock. Figure 5–30 shows the DDR timing relation between the parallel data and the clock. In this example, the `inclock` signal is running at half the speed of the data. However, other combinations are possible. Figure 5–31 shows the DDR output and the other modules used in a ×2 transmitter design to interface with the system logic.

*Figure 5–30. ×2 Timing Relation between Parallel Data & Clock*

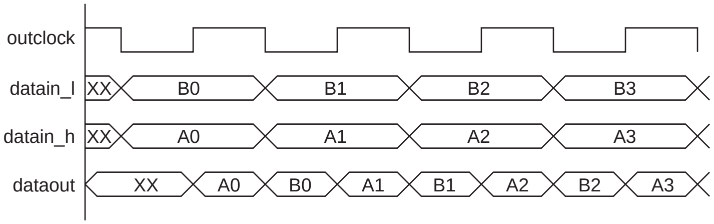
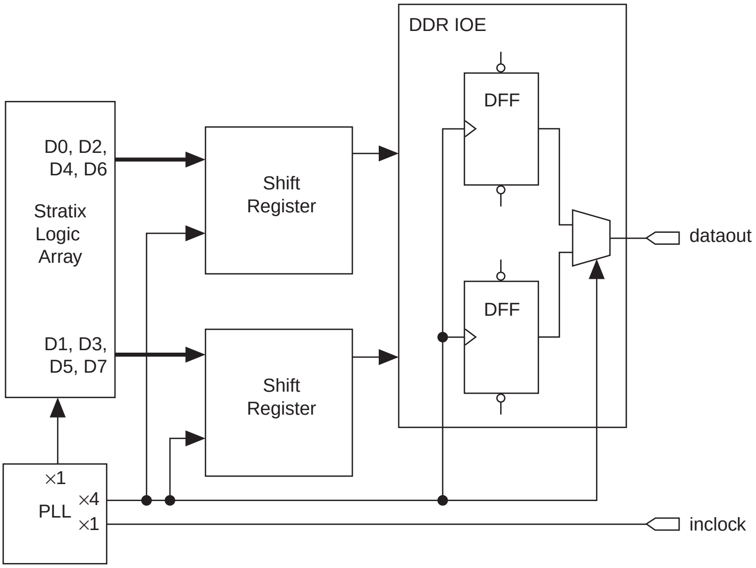


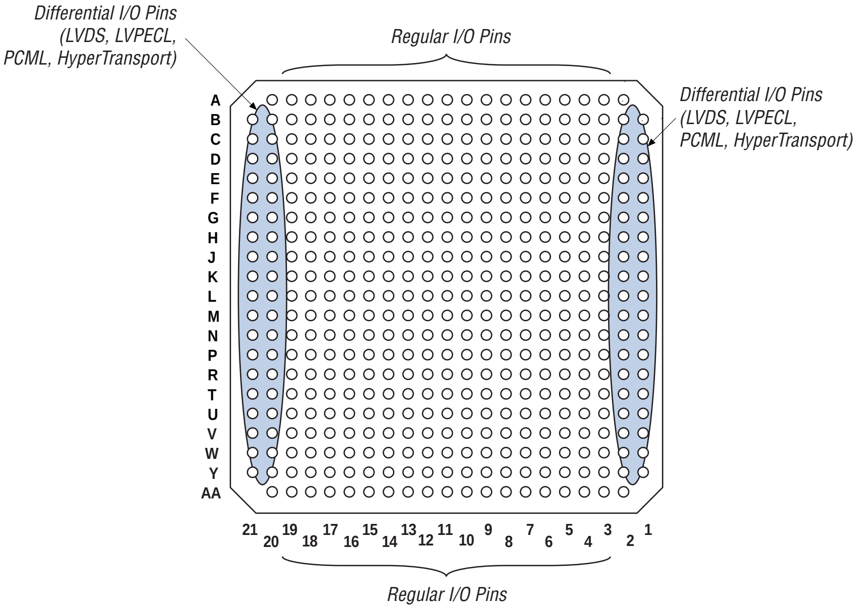
*Figure 5–31. ×2 Data Rate Transmitter Channel with Serialization Factor of 8*



## High-Speed Interface Pin Locations

Stratix high-speed interface pins are located at the edge of the package to limit the possible mismatch between a pair of high-speed signals. Stratix devices have eight programmable I/O banks. Figure 5–32 shows the I/O pins and their location relative to the package.

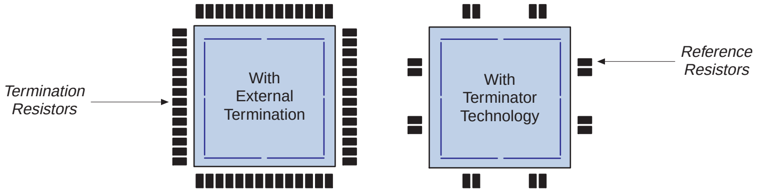
*Figure 5–32. Differential I/O Pin Locations*



## Differential I/O Termination

Stratix devices implement Terminator™ technology which provides on-chip termination and impedance matching to reduce reflections and maintain signal integrity. On-chip termination also minimizes the number of external resistors required. This simplifies board design and places the resistors closer to the package, eliminating small stubs that can still lead to reflections. Additionally, the on-chip termination constantly calibrates the internal resistor values after configuration and during normal operation via two external reference resistors. The constant calibration allows the termination resistors to compensate for process, temperature, and voltage variation, providing a robust termination scheme. Figure 5–33 shows two footprints of a device, one with external termination and one with on-chip termination. Differential on-chip termination does not require external reference resistors. You can use the $R_{UP}$ and $R_{DN}$ pins as an additional differential channel.

*Figure 5–33. Device Footprint with & without On-Chip Termination*



Terminator technology supports one type of I/O standard per I/O bank. You can enable or disable on-chip termination within an I/O bank on a pin-by-pin basis. To use different on-chip termination I/O standards on a device, select separate I/O banks. For example, if you want to use on-chip termination for LVDS (3.3-V $V_{CCIO}$) and HSTL Class II (1.5-V $V_{CCIO}$), use two separate I/O banks.

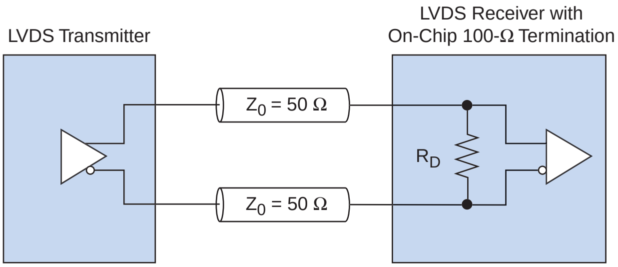
Different I/O standards need different $V_{CCIO}$ and $V_{REF}$ voltages. You can simultaneously use certain I/O standards with the same $V_{CCIO}$ in an I/O bank. For more information, refer to Chapter 4, Using Selectable I/O Standards in Stratix & Stratix GX Devices.

## $R_D$ Differential Termination

Stratix Terminator technology supports differential termination with a 100-Ω resistor for the LVDS I/O standard. External termination is required on the output and the input pin for LVPECL, PCML, or HyperTransport signals. Figure 5–34 shows the device with differential termination for the LVDS I/O standard.

For more information on Stratix Terminator technology, see Chapter 4, Using Selectable I/O Standards in Stratix & Stratix GX Devices.

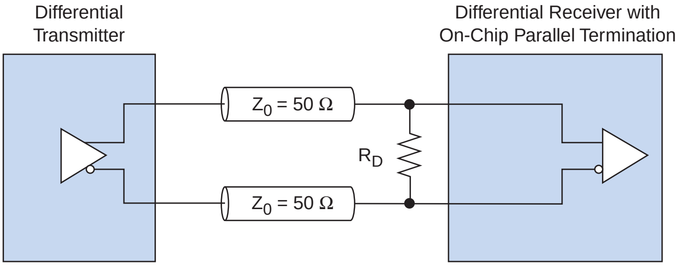
*Figure 5–34. On-Chip LVDS Differential Termination*



## HyperTransport & LVPECL Differential Termination

HyperTransport and LVPECL I/O standards are terminated by an external 100-Ω resistor on the input pin. Figure 5–35 shows the device with differential termination for the HyperTransport or LVPECL I/O standard.

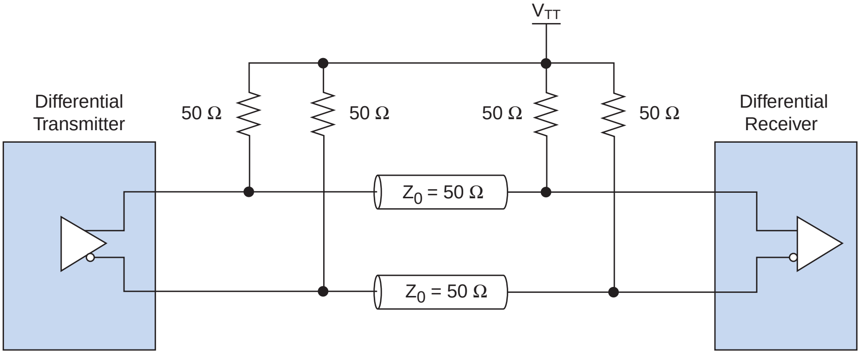
*Figure 5–35. HyperTransport & LVPECL Differential Termination*



## PCML Differential Termination

The PCML I/O technology is an alternative to the LVDS I/O technology, and use an external voltage source ($V_{TT}$), a pair of 100-Ω resistors on the input side and a pair of 50-Ω resistors on the output side. Figure 5–36 shows the device with differential termination for PCML I/O standard.

*Figure 5–36. PCML Differential Termination*



## HSTL Differential Termination

The HSTL class I and II I/O standards require a 0.75-V $V_{REF}$ and a 0.75-V $V_{TT}$. Figures 5–37 and 5–38 show the device with differential termination for HSTL class I and II I/O standard.

*Figure 5–37. HSTL Class I Differential Termination*

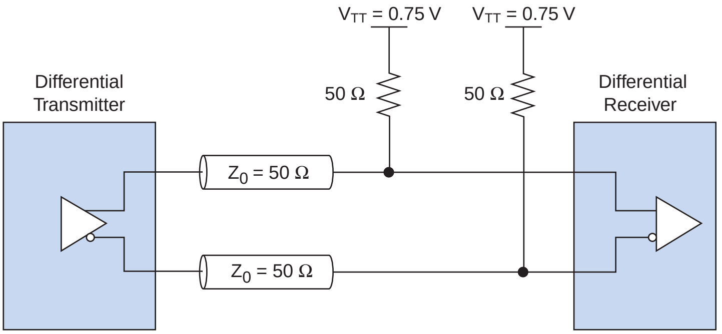
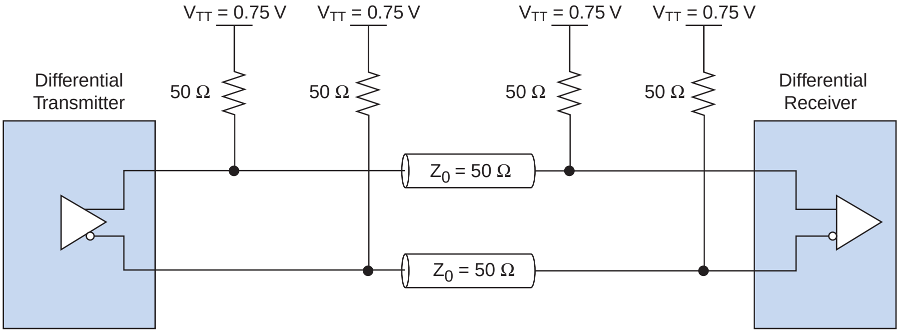


*Figure 5–38. HSTL Class II Differential Termination*



## SSTL-2 Differential Termination

The SSTL-2 class I and II I/O standards require a 1.25-V $V_{REF}$ and a 1.25-V $V_{TT}$. Figures 5–38 and 5–39 show the device with differential termination for SSTL-2 class I and II I/O standard.

Figure 5–39. SSTL-2 Class I Differential Termination

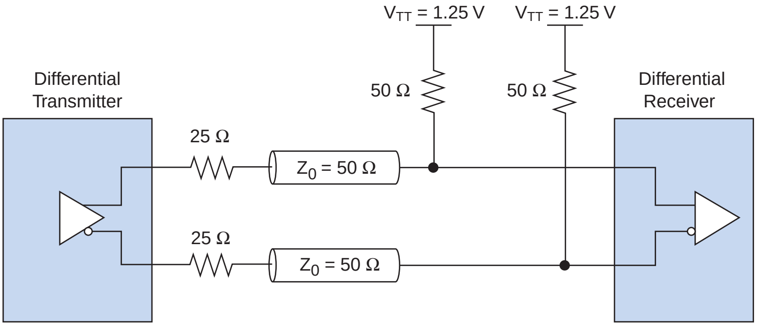
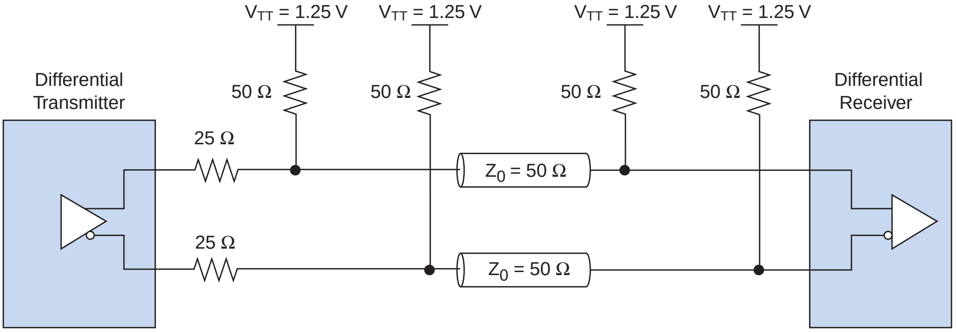


Figure 5–40. SSTL-2 Class II Differential Termination



## Board Design Consideration

This section is a brief explanation of how to get the optimal performance from the Stratix high-speed I/O block and ensure first-time success in implementing a functional design with optimal signal quality. For more information on detailed board layout recommendation and I/O pin terminations see *Application Note 224: High-Speed Board Layout Guidelines*.

You must consider the critical issues of controlled impedance of traces and connectors, differential routing, and termination techniques to get the best performance from the IC. Use this application note together with Section I, Stratix Device Family Data Sheet of the *Stratix Device Handbook, Volume 1*.

The Stratix high-speed module generates signals that travel over the media at frequencies as high as 840 Mbps. Board designers should use the following general guidelines:

- Baseboard designs on controlled differential impedance. Calculate and compare all parameters such as trace width, trace thickness, and the distance between two differential traces.
- Place external reference resistors as close to receiver input pins as possible.
- Use surface mount components.
- Avoid 90° or 45° corners.
- Use high-performance connectors such as HS-3 connectors for backplane designs. High-performance connectors are provided by Teradyne Corp (www.teradyne.com) or Tyco International Ltd. (www.tyco.com).
- Design backplane and card traces so that trace impedance matches the connector's and/or the termination's impedance.
- Keep equal number of vias for both signal traces.
- Create equal trace lengths to avoid skew between signals. Unequal trace lengths also result in misplaced crossing points and system margins as the TCCS value increases.
- Limit vias because they cause discontinuities.
- Use the common bypass capacitor values such as 0.001 µF, 0.01 µF, and 0.1 µF to decouple the fast PLL power and ground planes.
- Keep switching TTL signals away from differential signals to avoid possible noise coupling.
- Do not route TTL clock signals to areas under or above the differential signals.

## Software Support

This section provides information on using the Quartus II software to create Stratix designs with LVDS transmitters or receivers. You can use the `altlvds` megafunction in the Quartus II software to implement the SERDES circuitry. You must bypass the SERDES circuitry in ×1 and ×2 mode designs and use the `altddio` megafunction to implement the deserialization instead. You can use either the logic array or the M512 RAM blocks closest to the differential pins for deserialization in SERDES bypass mode.

### Differential Pins in Stratix

Stratix device differential pins are located in I/O banks 1, 2, 5, and 6 (see Figure 5–1 on page 5–2). Each bank has differential transmitter and differential receiver pin pairs. You can use each differential transmitter pin pair as either a differential data pin pair or a differential clock pin pair because Stratix devices do not have dedicated LVDS `tx_outclock` pin pairs. The differential receiver pin pairs can only function as differential data pin pairs. You can use these differential pins as regular user I/O pins when not used as differential pins. When using differential signaling in an I/O bank, you cannot place non-differential input pads within four

I/O pads and non-differential output or bidirectional pads within five I/O pads of either side of the differential pins to avoid a decrease in performance on the LVDS signals.

You only need to make assignments to the positive pin of the pin-pair. The Quartus II software automatically reserves and makes the same assignment to the negative pin. If you do not assign any differential I/O standard to the differential pins, the Quartus II software will set them as LVDS differential pins during fitting if the design uses the SERDES circuitry. Additionally, if you bypass the SERDES circuitry, you can still use the differential pins by assigning a differential I/O standard to the pins in the Quartus II software. However, when you bypass the SERDES circuitry in the ×1 and ×2 mode, you must assign the correct differential I/O standard to the associated pins in the Assignment Organizer. For more information on how to use the Assignment Organizer, see the Quartus II On-Line Help.

Stratix devices can drive the `PLL_LOCK` signal to both output pins and internal logic. As a result, you do not need a dedicated `LOCK` pin for your PLLs. In addition, there is only one `PLL_ENABLE` pin that enables all the PLLs on the device, including the fast PLLs. You must use either the LVTTL or LVCMOS I/O standard with this pin.

Table 5–9 displays the LVDS pins in Stratix devices.

***Table 5–9. LVDS Pin Names***

| Pin Names | Functions |
|---|---|
| `DIFFIO_TX#p` | Transmitter positive data or output clock pin |
| `DIFFIO_TX#n` | Transmitter negative data or output clock pin |
| `DIFFIO_RX#p` | Receiver positive data pin |
| `DIFFIO_RX#n` | Receiver negative data pin |
| `FPLLCLK#p` | Positive input clock pin to the corner fast PLLs *(1)*, *(2)* |
| `FPLLCLK#n` | Negative input clock pin to the corner fast PLLs *(1)*, *(2)* |
| `CLK#p` | Positive input clock pin *(2)* |
| `CLK#n` | Negative input clock pin *(2)* |

***Notes to Table 5–9:***

(1) The `FPLLCLK` pin-pair is only available in EP1S30, EP1S40, EP1S60, EP1S80 devices.

(2) Either a `FPLLCLK` pin or a `CLK` pin can drive the corner fast PLLs (PLL7, PLL8, PLL9, and PLL10) when used for general purpose. `CLK` pins cannot drive these fast PLLs in high-speed differential I/O mode.

## Fast PLLs

Each fast PLL features a multiplexed input path from a global or regional clock net. A clock pin or an output from another PLL in the device can drive the input path. EP1S10, EP1S20, and EP1S25 devices have a total of four fast PLLs located in the center of both sides of the device (see Figure 5–16 on page 5–23). EP1S30 and larger devices have two additional fast PLLs per side at the top and bottom corners of the device. As shown in Figure 5–17 on page 5–24, the corner fast PLL shares an I/O bank with the closest center fast PLL (e.g., PLLs 1 and 7 share an I/O bank). The maximum input clock frequency for enhanced PLLs is 462 MHz and 717 MHz for fast PLLs.

For more information on Stratix PLLs, see Chapter 1, Using General-Purpose PLLs in Stratix & Stratix GX Devices.

One fast PLL can drive the 20 transmitter channels and 20 receiver channels closest to it with data rates of up to 840 Mbps. Wire-bond packages have a preliminary rating of 462 Mbps. This value will be updated after device characterization. The corner fast PLLs in EP1S80 devices only support data rates of up to 462 Mbps (except the EP1S80 device in the 1,508-pin FineLine BGA package; the corner fast PLLs in this device support up to 840 Mbps). See Tables 5–10 through 5–14 for the number of high-speed differential channels in a particular Stratix device density and package.

Since the fast PLL drives the 20 closest differential channels, there are coverage overlaps in the EP1S30 and larger devices that have two fast PLLs per I/O bank. In these devices, either the center fast PLL or the corner fast PLL can drive the differential channels in the middle of the I/O bank.

Fast PLLs can drive more than 20 transmitter and 20 receiver channels when the data rate is less than 462 Mbps (see Tables 5–10 through 5–14 for the number of channels each PLL can drive). In addition, the center fast PLLs can drive either one I/O bank or both I/O banks on the same side (left or right) of the device, while the corner fast PLLs can only drive the differential channels in its I/O bank. Neither fast PLL can drive the differential channels in the opposite side of the device.

The center fast PLLs can only drive two I/O banks when the data rate is less than 462 Mbps. For example, EP1S20 device fast PLL 1 can drive all 33 differential channels on its side (17 channels from I/O bank 2 and 16 channels from I/O bank 1) running at 400 Mbps in 4× mode. When a center fast PLL drives the opposite bank on the same side of the device, the other center fast PLL cannot drive any differential channels on the device.

See Tables 5–10 through 5–14 for the maximum number of channels that one fast PLL can drive when the data rate is less than 462 Mbps. The number of channels is also listed in the Quartus II software. The Quartus II software will give an error if you try to compile a design exceeding the maximum number of channels.

Table 5–10 shows the number of channels and fast PLLs in EP1S10, EP1S20, and EP1S25 devices. Tables 5–11 through 5–14 show this information for EP1S30, EP1S40, EP1S60, and EP1S80 devices.

***Table 5–10. EP1S10, EP1S20 & EP1S25 Device Differential Channels (Part 1 of 2)*** *Note (1)*

| Device | Package | Transmitter/ Receiver | Total Channels | Maximum Speed (Mbps) | Center Fast PLLs | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | PLL 1 | PLL 2 | PLL 3 | PLL 4 |
| EP1S10 | 484-pin FineLine BGA | Transmitter *(2)* | 20 | 840 | 5 | 5 | 5 | 5 |
| | | | | 462 *(3)* | 10 | 10 | 10 | 10 |
| | | Receiver | 20 | 840 | 5 | 5 | 5 | 5 |
| | | | | 462 *(3)* | 10 | 10 | 10 | 10 |
| | 672-pin FineLine BGA | Transmitter *(2)* | 36 | 462 *(4)* | 9 | 9 | 9 | 9 |
| | | | | 462 *(3)* | 18 | 18 | 18 | 18 |
| | | Receiver | 36 | 462 *(4)* | 9 | 9 | 9 | 9 |
| | | | | 462 *(3)* | 18 | 18 | 18 | 18 |
| | 780-pin FineLine BGA | Transmitter *(2)* | 44 | 840 | 11 | 11 | 11 | 11 |
| | | | | 462 *(3)* | 22 | 22 | 22 | 22 |
| | | Receiver | 44 | 840 | 11 | 11 | 11 | 11 |
| | | | | 462 *(3)* | 22 | 22 | 22 | 22 |
| EP1S20 | 484-pin FineLine BGA | Transmitter *(2)* | 24 | 840 | 6 | 6 | 6 | 6 |
| | | | | 462 *(3)* | 12 | 12 | 12 | 12 |
| | | Receiver | 20 | 840 | 5 | 5 | 5 | 5 |
| | | | | 462 *(3)* | 10 | 10 | 10 | 10 |
| | 672-pin FineLine BGA | Transmitter *(2)* | 48 | 462 *(4)* | 12 | 12 | 12 | 12 |
| | | | | 462 *(3)* | 24 | 24 | 24 | 24 |
| | | Receiver | 50 | 462 *(4)* | 13 | 12 | 12 | 13 |
| | | | | 462 *(3)* | 25 | 25 | 25 | 25 |
| | 780-pin FineLine BGA | Transmitter *(2)* | 66 | 840 | 17 | 16 | 16 | 17 |
| | | | | 462 *(3)* | 33 | 33 | 33 | 33 |
| | | Receiver | 66 | 840 | 17 | 16 | 16 | 17 |
| | | | | 462 *(3)* | 33 | 33 | 33 | 33 |

**Table 5–10. EP1S10, EP1S20 & EP1S25 Device Differential Channels (Part 2 of 2) Note (1)**

| Device | Package | Transmitter/ Receiver | Total Channels | Maximum Speed (Mbps) | Center Fast PLLs | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | PLL 1 | PLL 2 | PLL 3 | PLL 4 |
| EP1S25 | 672-pin FineLine BGA | Transmitter (2) | 56 | 462 (4) | 14 | 14 | 14 | 14 |
| | | | | 462 (3) | 28 | 28 | 28 | 28 |
| | | Receiver | 58 | 462 (4) | 14 | 15 | 15 | 14 |
| | | | | 462 (3) | 29 | 29 | 29 | 29 |
| | 780-pin FineLine BGA | Transmitter (2) | 70 | 840 | 18 | 17 | 17 | 18 |
| | | | | 462 (3) | 35 | 35 | 35 | 35 |
| | | Receiver | 66 | 840 | 17 | 16 | 16 | 17 |
| | | | | 462 (3) | 33 | 33 | 33 | 33 |
| | 1,020-pin FineLine BGA | Transmitter (2) | 78 | 840 | 19 | 20 | 20 | 19 |
| | | | | 462 (3) | 39 | 39 | 39 | 39 |
| | | Receiver | 78 | 840 | 19 | 20 | 20 | 19 |
| | | | | 462 (3) | 39 | 39 | 39 | 39 |

*Notes to Table 5–10:*

(1) Table 5–10 shows two different number of channels depending on the channel speed. For example, in the 484-pin FineLine BGA EP1S10 device, PLL 1 can drive a maximum of five channels at 840 Mbps or a maximum of 10 channels at 462 Mbps. The Quartus II software may also merge receiver and transmitter PLLs when a receiver is driving a transmitter. In this case, one fast PLL can drive both the maximum numbers of receiver and transmitter channels.

(2) The number of channels listed includes the transmitter clock output (`tx_outclock`) channel. You can use an extra data channel if you need a DDR clock.

(3) These channels span across two banks per side of the device. When a center fast PLL drives the opposite bank on the same side of the device, the other center fast PLL cannot drive any differential channels on the device. For example, if PLL 1 in a 484-pin FineLine BGA EP1S10 device drives 10 channels at 462 Mbps, PLL 2 cannot drive any differential channels. Similar restrictions apply to PLLs 3 and 4.

(4) 672-pin packages only support up to 462 Mbps. These values show the channels available for each PLL without crossing another bank.

***Table 5–11. EP1S30 Differential Channels*** *Note (1)*

| Package | Transmitter/ Receiver | Total Channels | Maximum Speed (Mbps) | Center Fast PLLs | | | | Corner Fast PLLs *(2)*, *(7)* | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | PLL1 | PLL2 | PLL3 | PLL4 | PLL7 | PLL8 | PLL9 | PLL10 |
| 780-pin FineLine BGA | Transmitter *(3)* | 70 | 840 | 18 | 17 | 17 | 18 | *(5)* | *(5)* | *(5)* | *(5)* |
| | | | 462 *(4)* | 35 | 35 | 35 | 35 | *(5)* | *(5)* | *(5)* | *(5)* |
| | Receiver | 66 | 840 | 17 | 16 | 16 | 17 | *(5)* | *(5)* | *(5)* | *(5)* |
| | | | 462 *(4)* | 33 | 33 | 33 | 33 | *(5)* | *(5)* | *(5)* | *(5)* |
| 956-pin FineLine BGA | Transmitter *(3)* | 80 (2) *(6)* | 840 | 19 | 20 | 20 | 19 | 20 | 20 | 20 | 20 |
| | | | 462 *(4)* | 39 | 39 | 39 | 39 | 20 | 20 | 20 | 20 |
| | Receiver | 80 (2) *(6)* | 840 | 20 | 20 | 20 | 20 | 19 | 20 | 20 | 19 |
| | | | 462 *(4)* | 40 | 40 | 40 | 40 | 19 | 20 | 20 | 19 |
| 1,020-pin FineLine BGA | Transmitter *(3)* | 80 (2) *(6)* | 840 | 20 | 20 | 20 | 20 | 20 | 20 | 20 | 20 |
| | | | 462 *(4)* | 40 | 40 | 40 | 40 | 20 | 20 | 20 | 20 |
| | Receiver | 80 (2) *(6)* | 840 | 20 | 20 | 20 | 20 | 20 | 20 | 20 | 20 |
| | | | 462 *(4)* | 40 | 40 | 40 | 40 | 20 | 20 | 20 | 20 |

***Table 5–12. EP1S40 Differential Channels*** *Note (1)* ***(Part 1 of 2)***

| Package | Transmitter/ Receiver | Total Channels | Maximum Speed (Mbps) | Center Fast PLLs | | | | Corner Fast PLLs *(2)*, *(7)* | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | PLL1 | PLL2 | PLL3 | PLL4 | PLL7 | PLL8 | PLL9 | PLL10 |
| 780-pin FineLine BGA | Transmitter *(3)* | 68 | 840 | 18 | 16 | 16 | 18 | *(5)* | *(5)* | *(5)* | *(5)* |
| | | | 462 *(4)* | 34 | 34 | 34 | 34 | *(5)* | *(5)* | *(5)* | *(5)* |
| | Receiver | 66 | 840 | 17 | 16 | 16 | 17 | *(5)* | *(5)* | *(5)* | *(5)* |
| | | | 462 *(4)* | 33 | 33 | 33 | 33 | *(5)* | *(5)* | *(5)* | *(5)* |
| 956-pin FineLine BGA | Transmitter *(3)* | 80 | 840 | 18 | 17 | 17 | 18 | 20 | 20 | 20 | 20 |
| | | | 462 *(4)* | 35 | 35 | 35 | 35 | 20 | 20 | 20 | 20 |
| | Receiver | 80 | 840 | 20 | 20 | 20 | 20 | 18 | 17 | 17 | 18 |
| | | | 462 *(4)* | 40 | 40 | 40 | 40 | 18 | 17 | 17 | 18 |
| 1,020-pin FineLine BGA | Transmitter *(3)* | 80 (10) *(6)* | 840 | 20 | 20 | 20 | 20 | 20 | 20 | 20 | 20 |
| | | | 462 *(4)* | 40 | 40 | 40 | 40 | 20 | 20 | 20 | 20 |
| | Receiver | 80 (10) *(6)* | 840 | 20 | 20 | 20 | 20 | 20 | 20 | 20 | 20 |
| | | | 462 *(4)* | 40 | 40 | 40 | 40 | 20 | 20 | 20 | 20 |

*Table 5–12. EP1S40 Differential Channels* *Note (1)* ***(Part 2 of 2)***

| Package | Transmitter/ Receiver | Total Channels | Maximum Speed (Mbps) | Center Fast PLLs | | | | Corner Fast PLLs *(2)*, *(7)* | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | PLL1 | PLL2 | PLL3 | PLL4 | PLL7 | PLL8 | PLL9 | PLL10 |
| 1,508-pin FineLine BGA | Transmitter *(3)* | 80<br>(10) *(6)* | 840 | 20 | 20 | 20 | 20 | 20 | 20 | 20 | 20 |
| | | | 462 *(4)* | 40 | 40 | 40 | 40 | 20 | 20 | 20 | 20 |
| | Receiver | 80<br>(10) *(6)* | 840 | 20 | 20 | 20 | 20 | 20 | 20 | 20 | 20 |
| | | | 462 *(4)* | 40 | 40 | 40 | 40 | 20 | 20 | 20 | 20 |

*Table 5–13. EP1S60 Differential Channels* *Note (1)*

| Package | Transmitter/ Receiver | Total Channels | Maximum Speed (Mbps) | Center Fast PLLs | | | | Corner Fast PLLs *(2)*, *(7)* | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | PLL1 | PLL2 | PLL3 | PLL4 | PLL7 | PLL8 | PLL9 | PLL10 |
| 956-pin FineLine BGA | Transmitter *(3)* | 80 | 840 | 12 | 10 | 10 | 12 | 20 | 20 | 20 | 20 |
| | | | 462 *(4)* | 40 | 40 | 40 | 40 | 20 | 20 | 20 | 20 |
| | Receiver | 80 | 840 | 20 | 20 | 20 | 20 | 12 | 10 | 10 | 12 |
| | | | 462 *(4)* | 22 | 22 | 22 | 22 | 12 | 10 | 10 | 12 |
| 1,020-pin FineLine BGA | Transmitter *(3)* | 80<br>(12) *(6)* | 840 | 14 | 14 | 14 | 14 | 20 | 20 | 20 | 20 |
| | | | 462 *(4)* | 28 | 28 | 28 | 28 | 20 | 20 | 20 | 20 |
| | Receiver | 80<br>(10) *(6)* | 840 | 20 | 20 | 20 | 20 | 14 | 13 | 13 | 14 |
| | | | 462 *(4)* | 40 | 40 | 40 | 40 | 14 | 13 | 13 | 14 |
| 1,508-pin FineLine BGA | Transmitter *(3)* | 80<br>(36) *(6)* | 840 | 20 | 20 | 20 | 20 | 20 | 20 | 20 | 20 |
| | | | 462 *(4)* | 40 | 40 | 40 | 40 | 20 | 20 | 20 | 20 |
| | Receiver | 80<br>(36) *(6)* | 840 | 20 | 20 | 20 | 20 | 20 | 20 | 20 | 20 |
| | | | 462 *(4)* | 40 | 40 | 40 | 40 | 20 | 20 | 20 | 20 |

***Table 5–14. EP1S80 Differential Channels*** *Note (1)*

| Package | Transmitter/ Receiver | Total Channels | Maximum Speed (Mbps) | Center Fast PLLs | | | | Corner Fast PLLs *(2)* | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | PLL1 | PLL2 | PLL3 | PLL4 | PLL7 | PLL8 | PLL9 | PLL10 |
| 1020-pin FineLine BGA | Transmitter *(3)* | 92 (12) *(6)*, | 840 | 12 | 14 | 14 | 12 | 20 | 20 | 20 | 20 |
| | | | 462 *(4)* | 26 | 26 | 26 | 26 | 20 | 20 | 20 | 20 |
| | Receiver | 90 (10) *(6)*, | 840 | 20 | 20 | 20 | 20 | 10 | 10 | 10 | 10 |
| | | | 462 *(4)* | 40 | 40 | 40 | 40 | 12 | 13 | 13 | 12 |
| 956-pin FineLine BGA | Transmitter *(3)* | 80 (40) *(6)* | 840 | 10 | 10 | 10 | 10 | 20*(7)* | 20*(7)* | 20*(7)* | 20*(7)* |
| | | | 462 *(4)* | 20 | 20 | 20 | 20 | 20 | 20 | 20 | 20 |
| | Receiver | 80 | 840 | 20 | 20 | 20 | 20 | 10 | 10 | 10 | 10 |
| | | | 462 *(4)* | 40 | 40 | 40 | 40 | 10 | 10 | 10 | 10 |
| 1,508-pin FineLine BGA | Transmitter *(3)* | 80 (72) *(6)* | 840 | 20 | 20 | 20 | 20 | 20 | 20 | 20 | 20 |
| | | | 462 *(4)* | 40 | 40 | 40 | 40 | 28 | 28 | 28 | 28 |
| | Receiver | 80 (56) *(6)* | 840 | 20 | 20 | 20 | 20 | 20 | 20 | 20 | 20 |
| | | | 462 *(4)* | 40 | 40 | 40 | 40 | 24 | 24 | 24 | 24 |

*Notes to Tables 5–11 through 5–14*

(1) This table shows two different number of channels depending on the channel speed. For example, in the 780-pin FineLine BGA EP1S30 device, PLL 1 can drive a maximum of 18 channels at 840 Mbps or a maximum of 35 channels at 462 Mbps. The Quartus II software may also merge transmitter and receiver PLLs when a receiver is driving a transmitter. In this case, one fast PLL can drive both the maximum numbers of receiver and transmitter channels.

(2) Some of the channels accessible by the center fast PLL and the channels accessible by the corner fast PLL overlap. Therefore, the total number of channels is not the addition of the number of channels accessible by PLLs 1, 2, 3, and 4 with the number of channels accessible by PLLs 7, 8, 9, and 10. For more information on which channels overlap, contact Altera Applications.

(3) The numbers of channels listed include the transmitter clock output (`tx_outclock`) channel. You can use an extra data channel if you need a DDR clock.

(4) When a center fast PLL drives the opposite bank on the same side of the device, the other center fast PLL cannot drive any differential channels on the device. For example, if PLL 1 in a 484-pin FineLine BGA EP1S10 device drives 10 channels at 462 Mbps, PLL 2 cannot drive any differential channels. Similar restrictions apply to PLLs 3 and 4.

(5) PLLs 7, 8, 9, and 10 are not available in this device.

(6) The number in parentheses is the number of slow-speed channels, guaranteed to operate at up to 462 Mbps. These channels are independent of the high-speed differential channels. For the location of these channels, contact Altera Applications.

(7) The corner fast PLLs in this device support a preliminary data rate of 462 Mbps. Contact Altera Applications for more information.

The Quartus II software may also merge transmitter and receiver PLLs when a receiver block is driving a transmitter block if the **Use Common PLLs for Rx and Tx** option is set for both modules. The Quartus II software will not merge the PLLs in multiple transmitter-only or multiple receiver-only modules fed by the same clock

### LVDS Receiver Block

You only need to enter the input clock frequency, deserialization factor, and the input data rate to implement an LVDS receiver block. The Quartus II software will then automatically set the clock boost (*W*) factor for the receiver. In addition, you can also indicate the clock and data alignment for the receiver or add the `pll_enable`, `rx_data_align`, and `rx_locked` output ports. Table 5–15 explains the function of the available ports in the LVDS receiver block.

*Table 5–15. LVDS Receiver Ports*

| Port Name | Direction | Function | Input Port Source/Output Port Destination |
|---|---|---|---|
| `rx_in[number_of_channels - 1..0]` | Input | Input data channel | Pin |
| `rx_inclock` | Input | Reference input clock | Pin or output from a PLL |
| `rx_pll_enable` | Input | Enables fast PLL | Pin *(1)*, *(2)*, *(3)* |
| `rx_data_align` | Input | Control for the data realignment circuitry | Pin or logic array *(1)*, *(3)*, *(4)* |
| `rx_locked` | Output | Fast PLL locked pin | Pin or logic array *(1)*, *(3)* |
| `rx_out[Deserialization_factor * number_of_channels -1..0]` | Output | De-serialized data | Logic array |
| `rx_outclock` | Output | Internal reference clock | Logic array |

*Notes to Table 5–15:*

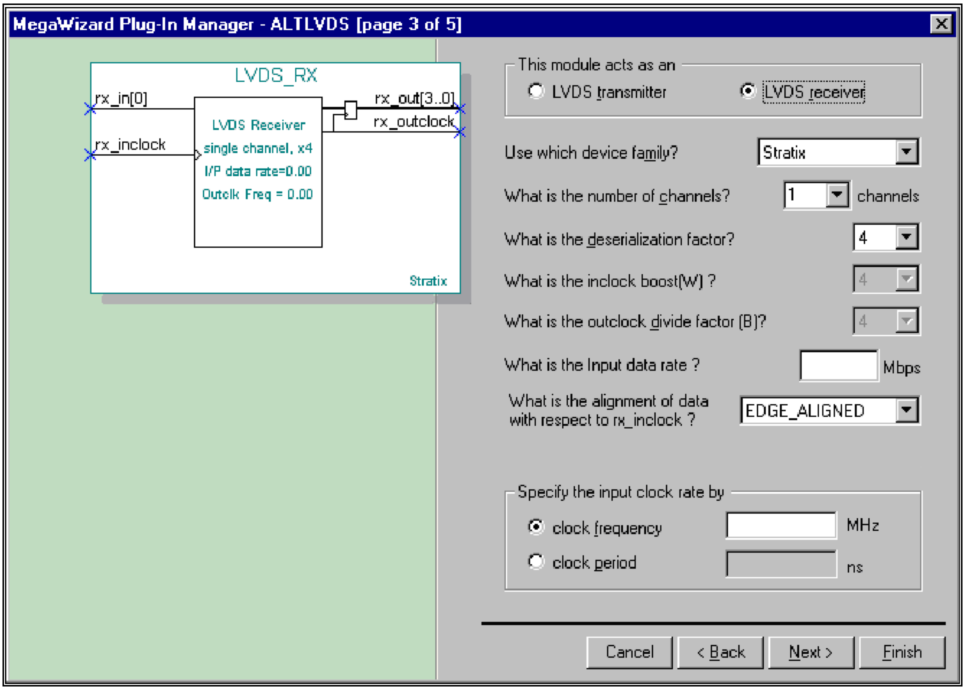
(1) This is an optional port.
(2) Only one `rx_pll_enable` pin is necessary to enable all the PLLs in the device.
(3) This is a non-differential pin.
(4) See "Realignment Implementation" on page 5–28 for more information. For guaranteed performance and data alignment, you must synchronize `rx_data_align` with `rx_outclock`.

Use the `altlvds` MegaWizard Plug-In Manager to create an LVDS receiver block. The following sections explain the parameters available in the Plug-In Manager when creating an LVDS receiver block.

#### *Page 3 of the altlvds_rx MegaWizard Plug-In Manager*

On page 3 of the `altlvds` MegaWizard Plug-In Manager, you can choose to create either an LVDS transmitter or receiver. Depending on what you select, the MegaWizard Plug-In Manager will provide you with different options. Figure 5–41 shows page 3 of the `altlvds` MegaWizard Plug-In Manager with options for creating an LVDS receiver.

*Figure 5–41. Page 3 of the altlvds_rx MegaWizard Plug-In Manager*



MegaWizard Plug-In Manager - ALTLVDS [page 3 of 5]

This module acts as an

○ LVDS transmitter ● LVDS receiver

Use which device family? Stratix

What is the number of channels? 1 channels

What is the deserialization factor? 4

What is the inclock boost(W) ? 4

What is the outclock divide factor (B)? 4

What is the Input data rate ? Mbps

What is the alignment of data with respect to rx_inclock ? EDGE_ALIGNED

Specify the input clock rate by

● clock frequency MHz

○ clock period ns

### Number of Channels

The **What is the number of channels?** parameter specifies the number of receiver channels required and the width of `rx_out` port. To set a fast PLL to drive over 20 channels, type the required number in the Quartus II window instead of choosing a number from the drop-down menu, which only has selections of up to 20 channels.

### Deserialization Factor

Use the **What is the deserialization factor?** parameter to specify the number of bits per channel. The Stratix LVDS receiver supports 4, 7, 8, and 10 for deserialization factor (*J*) values. Based on the factor specified, the Quartus II software determines the multiplication and/or division factor for the LVDS PLL to deserialize the data.

See Table 5–5 for the differential bit naming convention. The parallel data for the n$^{th}$ channel spans from the MSB (`rx_out` bit $[(J \times n) - 1]$) to the LSB (`rx_out` bit $[J \times (n - 1)]$), where *J* is the deserialization factor. The total width of the receiver `rx_out` port is equal to the number of channels multiplied by your deserialization factor.

### Input Data Rate

The **What is the inclock boost(W)?** parameter sets the data rate coming into the receiver and is usually the deserialization factor (*J*) multiplied by the `inclock` frequency. This parameter's value must be larger than the input clock frequency and has a maximum input data rate of 840 Mbps for Stratix devices. You do not have to provide a value for the inclock boost (*W*) when designing with Stratix devices because the Quartus II software can calculate it automatically from this parameter and the clock frequency or clock period.

The `rx_outclock` frequency is ($W/J$) × input frequency. The parallel data coming out of the receiver has the same frequency as the `rx_outclock` port. The clock-to-data alignment of the parallel data output from the receiver depends on the **What is the alignment of data with respect to rx_inclock?** parameter.

### Data Alignment with Clock

The **What is the alignment of data with respect to rx_inclock?** parameter adjusts the clock-to-data skew. For most applications, the data is source synchronous to the clock. However, there are applications where you must center-align the data with respect to the clock. You can use the **What is the alignment of data with respect to rx_inclock?** parameter to align the input data with respect to the `rx_inclock` port. The MegaWizard Plug-In automatically calculates the phase for the fast PLL outputs from the **What is the alignment of data with respect to rx_inclock?** parameter. This parameter's default value is `EDGE_ALIGNED`, and other values available from the pull-down menu are `EDGE_ALIGNED`, `CENTER_ALIGNED`, `45_DEGREES`, `135_DEGREES`, `180_DEGREES`, `225_DEGREES`, `270_DEGREES`, and `315_DEGREES`. `CENTER_ALIGNED` is the same as 90 degrees aligned and is useful for applications like HyperTransport technology.

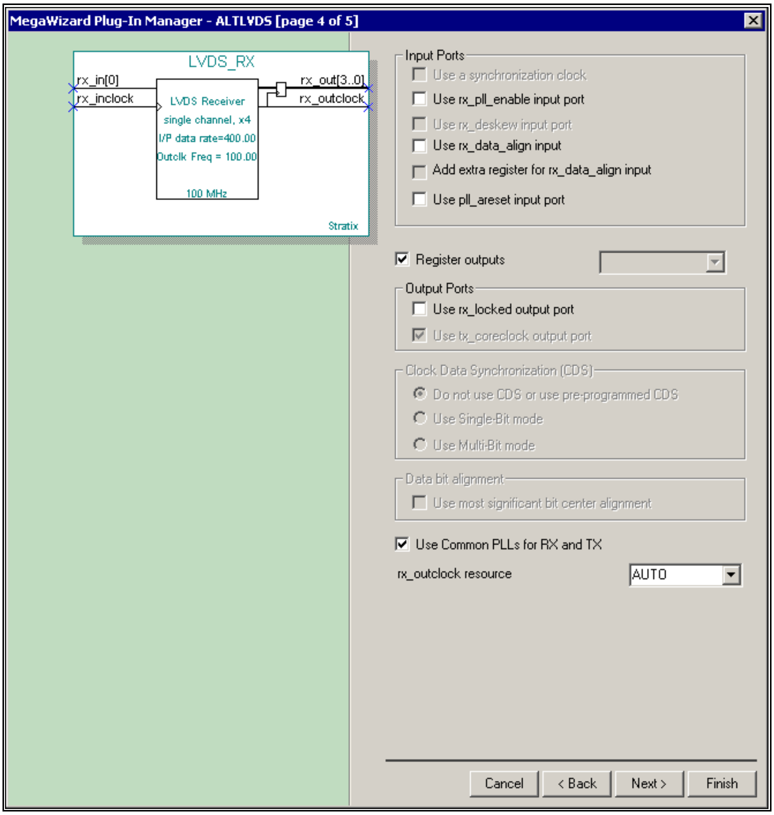
### Clock Frequency or Clock Period

The fields in the **Specify the input clock rate by** box specify the input frequency or the period of the input clock going into the fast PLL. When using the same input clock to feed a transmitter and receiver simultaneously, the Quartus II software can use one fast PLL for both the transmitter and receiver.

## *Page 4 of the altlvds_rx MegaWizard Plug-In Manager*

This section describes the parameters found on page 4 of the `altlvds_rx` MegaWizard Plug-In Manager (see Figure 5–42).

*Figure 5–42. Page 4 of the altlvds_rx MegaWizard Plug-In Manager*



MegaWizard Plug-In Manager - ALTLVDS [page 4 of 5]

Input Ports

- ☐ Use a synchronization clock
- ☐ Use rx_pll_enable input port
- ☐ Use rx_deskew input port
- ☐ Use rx_data_align input
- ☐ Add extra register for rx_data_align input
- ☐ Use pll_areset input port

☑ Register outputs

Output Ports

- ☐ Use rx_locked output port
- ☑ Use tx_coreclock output port

Clock Data Synchronization (CDS)

- ● Do not use CDS or use pre-programmed CDS
- ○ Use Single-Bit mode
- ○ Use Multi-Bit mode

Data bit alignment

- ☐ Use most significant bit center alignment

☑ Use Common PLLs for RX and TX

rx_outclock resource: AUTO

## Data Realignment

Check the **Use the "rx_data_align" input port** box within the **Input Ports** box to add the `rx_data_align` output port and enable the data realignment circuitry in Stratix SERDES. See "Receiver Data Realignment" on page 5–25 for more information. If necessary, you can create a state machine to send a pulse to the `rx_data_align` port to realign the data coming in the LVDS receiver. You need to assert the port for at least two clock cycles to enable the data realignment circuitry. Go to the Altera web site at www.altera.com for a sample design written in Verilog HDL.

For guaranteed performance when using data realignment, check the **Add Extra registers for rx_data_align input** box when using the `rx_data_align` port. The Quartus II software places one synchronization register in the LE closest to the `rx_data_align` port.

### Register Outputs

Check the **Register outputs** box to register the receiver's output data. The register acts as the module's register boundary. If the module fed by the receiver does not have a register boundary for the data, turn this option on. The number of registers used is proportional to the deserialization factor (*J*). The Quartus II software places the synchronization registers in the LEs closest to the SERDES circuitry.

### Use Common PLL for Both Transmitter & Receiver

Check the **Use Common PLLs for Rx and Tx** box to place both the LVDS transmitter and the LVDS receiver in the same Stratix device I/O bank. The Quartus II software allows the transmitter and receiver to share the same fast PLL when they use the same input clock. Although you must separate the transmitter and receiver modules in your design, the Quartus II software merges the fast PLLs when appropriate and give you the following message:

Receiver fast PLL <*lvds_rx PLL name*> and transmitter fast PLL <*lvds_tx PLL name*> are merged together

The Quartus II software provides the following message when it cannot merge the fast PLLs for the LVDS transmitter and receiver pair in the design:

Can't merge transmitter-only fast PLL <*lvds_tx PLL name*> and receiver-only fast PLL <*lvds_rx PLL name*>

### rx_outclock Resource

You can use either the global or regional clock for the `rx_outclock` signal. If you select **Auto** in the Quartus II software, the tool will use any available lines.

## LVDS Transmitter Module

The Quartus II software calculates the inclock boost (*W*) factor for the LVDS transmitter based on input data rate, input clock frequency, and the deserialization factor. In addition to setting the data and clock alignment, you can also set the outclock divide factor (*B*) for the transmitter output clock and add the `pll_enable`, `tx_locked`, and `tx_coreclock` ports. Table 5–16 explains the function of the available ports in the LVDS transmitter block.

**Table 5–16. LVDS Transmitter Ports**

| Port Name | Direction | Function | Input port Source/Output port Destination |
|---|---|---|---|
| `tx_in[Deserialization_factor * number_of_channels - 1..0]` | Input | Input data | Logic array |
| `tx_inclock` | Input | Reference input clock | Pin or output clock from a PLL |
| `tx_pll_enable` | Input | Fast PLL enable | Pin *(1)*, *(2)*, *(3)* |
| `tx_out[number_of_channels - 1..0]` | Output | Serialized LVDS data signal | Pin |
| `tx_outclock` | Output | External reference clock | Pin |
| `tx_coreclock` | Output | Internal reference clock | Pin, logic array, or input clock to a fast PLL *(1)* |
| `tx_locked` | Output | Fast PLL locked pin | Pin or logic array *(1)*, *(2)*, *(3)* |

*Notes to Table 5–16:*

(1) This is an optional port.

(2) Only one `tx_pll_enable` pin is necessary to enable all the PLLs in the device.

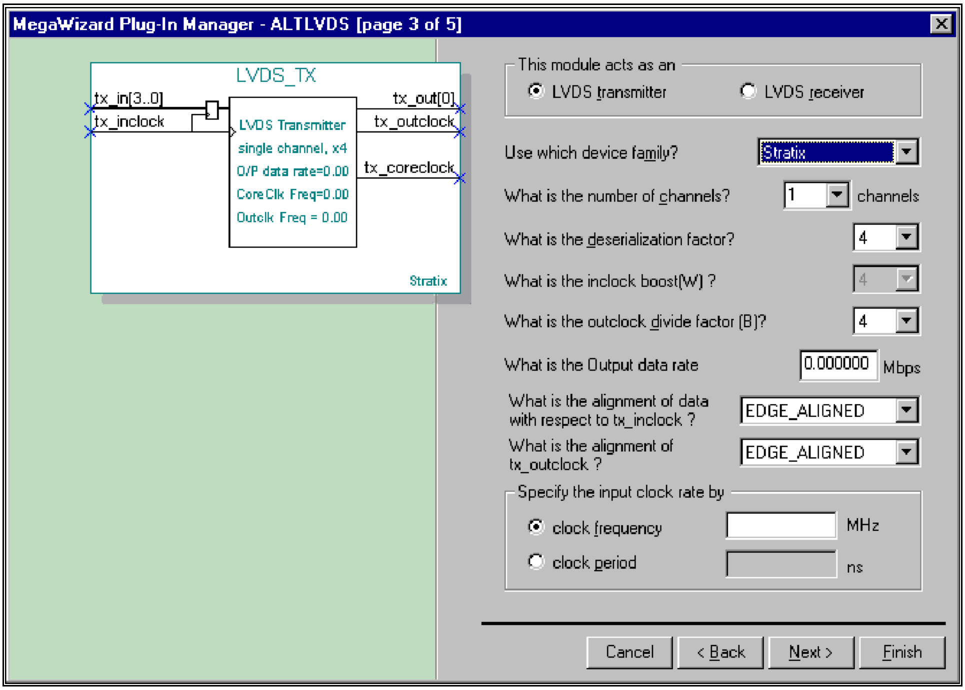
(3) This is a non-differential pin.

You can also use the `altlvds` MegaWizard Plug-In Manager to create an LVDS transmitter block. The following sections explain the parameters available in the Plug-In Manager when creating an LVDS transmitter block.

### *Page 3 of the altlvds_tx MegaWizard Plug-In Manager*

This section describes the parameters found on page 3 of the `altlvds_tx` MegaWizard Plug-In Manager (see Figure 5–43).

*Figure 5–43. Page 3 of the Transmitter altlvds MegaWizard Plug-In Manager*



MegaWizard Plug-In Manager - ALTLVDS [page 3 of 5]

This module acts as an

● LVDS transmitter ○ LVDS receiver

Use which device family? Stratix

What is the number of channels? 1 channels

What is the deserialization factor? 4

What is the inclock boost(W) ? 4

What is the outclock divide factor (B)? 4

What is the Output data rate 0.000000 Mbps

What is the alignment of data with respect to tx_inclock ? EDGE_ALIGNED

What is the alignment of tx_outclock ? EDGE_ALIGNED

Specify the input clock rate by

● clock frequency MHz

○ clock period ns

### Number of Channels

The **What is the number of channels?** parameter specifies the number of transmitter channels required and the width of the `tx_in` port. You can have more than 20 channels in a transmitter or receiver module by typing in the required number instead of choosing a number from the drop down menu, which only has selections of up to 20 channels.

### Deserialization Factor

The **What is the deserialization factor?** parameter specifies the number of bits per channel. The transmitter block supports deserialization factors of 4, 7, 8, and 10. Based on the factor specified, the Quartus II software will determine the multiplication and/or division factor for the LVDS PLL in order to serialize the data.

Table 5–5 on page 5–32 lists the differential bit naming convention. The parallel data for the n$^{th}$ channel spans from the MSB (`rx_out` bit $[(J \times n) - 1]$) to the LSB (`rx_out` bit $[J \times (n - 1)]$), where $J$ is the deserialization factor. The total width of the `tx_in` port of the transmitter is equal to the number of channels multiplied by the deserialization factor.

### Outclock Divide Factor

The **What is the Output data rate?** parameter specifies the ratio of the `tx_outclock` frequency compared to the data rate. The default value for this parameter is the value of the deserialization factor parameter. The `tx_outclock` frequency is equal to $[W/(B \times J)]$ x input clock frequency. There is also an optional `tx_coreclock` port which has the same frequency as the $(W/J) \times$ input frequency.

The outclock divide factor is useful for applications that do not require the data rate to be the same as the clock frequency. For example, HyperTransport technology uses a half-clock data rate scheme where the clock frequency is half the data rate. Table 5–17 shows the supported outclock divide factor for a given deserialization factor.

*Table 5–17. Deserialization Factor (J) vs. Outclock Divide Factor (B)*

| Deserialization Factor (*J*) | Outclock Divide Factor (*B*) |
|---|---|
| 4 | 1, 2, 4 |
| 7 | 1, 7*(1)* |
| 8 | 1, 2, 4, 8 |
| 10 | 1, 2, 10 |

*Note to Table 5–17:*

(1) The clock does not have a 50% duty cycle when b=7 in x7 mode.

### Output Data Rate

The **What is the Output data rate** parameter specifies the data rate out of the fast PLL and determines the input clock boost/multiplication factor needed for the transmitter. This parameter must be larger than the input clock frequency and has a maximum rate of 840 Mbps for Stratix devices. The input clock boost factor ($W$) is the output data rate divided by the input clock frequency. The Stratix SERDES circuitry supports input clock boost factors of 4, 7, 8, or 10. The maximum output data rate is 840 Mbps, while the clock has a maximum output of 462 MHz.

### Data Alignment with Clock

Use the **What is the alignment of data with respect to tx_inclock?** parameter and the **What is the alignment of tx_outclock?** to align the input and output data, respectively, with the clock. For most applications, the data is edge-aligned with the clock. However, there are applications where the data must be center-aligned with respect to the clock. With

Stratix devices, you can align the input data with respect to the `tx_inclock` port and align the output data with respect to the `tx_outclock` port. The MegaWizard Plug-In Manager uses the alignment of input and output data to automatically calculate the phase for the fast PLL outputs. Both of these parameters default to `EDGE_ALIGNED`, and other values are `CENTER_ALIGNED`, `45_DEGREES`, `135_DEGREES`, `180_DEGREES`, `225_DEGREES`, `270_DEGREES`, and `315_DEGREES`. `CENTER_ALIGNED` is the same as 90 degrees aligned and is required for the HyperTransport technology I/O standard.

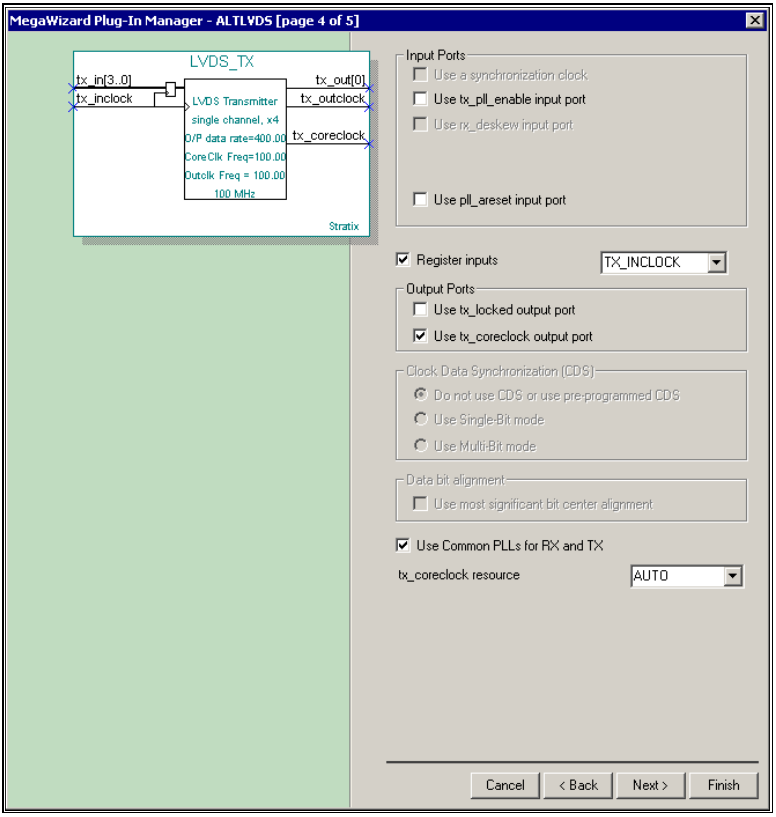
#### Clock Frequency & Clock Period

The fields in the **Specify the input clock rate by** box specify either the frequency or the period of the input clock going into the fast PLL. However, you cannot specify both. If your design uses the same input clock to feed a transmitter and a receiver module simultaneously, the Quartus II software can merge the fast PLLs for both the transmitter and receiver when the **Use common PLLs for Tx & Rx** option is turned on.

### *Page 4 of the altlvds_tx MegaWizard Plug-In Manager*

This section describes the parameters found on page 4 of the `altlvds_tx` MegaWizard Plug-In Manager (see Figure 5–44).

*Figure 5–44. Page 4 of the Transmitter altlvds MegaWizard Plug-In Manager*



MegaWizard Plug-In Manager - ALTLVDS [page 4 of 5]

Input Ports

☐ Use a synchronization clock

☐ Use tx_pll_enable input port

☐ Use rx_deskew input port

☐ Use pll_areset input port

☑ Register inputs TX_INCLOCK

Output Ports

☐ Use tx_locked output port

☑ Use tx_coreclock output port

Clock Data Synchronization (CDS)

● Do not use CDS or use pre-programmed CDS

○ Use Single-Bit mode

○ Use Multi-Bit mode

Data bit alignment

☐ Use most significant bit center alignment

☑ Use Common PLLs for RX and TX

tx_coreclock resource AUTO

### Registered Inputs

Check the **Register inputs** box if the input data to the transmitter is not registered just before it feeds the transmitter module. You can choose either `tx_clkin` or `tx_coreclk` to clock the transmitter data (`tx_in[]`) signal. This serves as the register boundary. The number of registers used is proportional to the deserialization factor (*J*). The Quartus II software places the synchronization registers with the LEs in the same row and closest to the SERDES circuitry.

### Use Common PLL for Transmitter & Receiver

Check the **Use Common PLLs for Rx and Tx** box to place both the LVDS transmitter and receiver in the same I/O bank in Stratix devices. The Quartus II software also allows the transmitter and receiver to share the PLL when the same input clock is used for both. Although you must separate the transmitter and receiver in your design, the Quartus II software will merge the fast PLLs when appropriate and give you the following message:

Receiver fast PLL <lvds_rx pll name> and transmitter fast PLL <lvds_tx pll name> are merged together

The Quartus II software will give the following message when it cannot merge the fast PLLs for the LVDS transmitter and receiver pair in the design:

```
Can't merge transmitter-only fast PLL <lvds_tx pll
name> and receiver-only fast PLL <lvds_rx pll name>
```

**tx_outclock Resource**

You can use either the global or regional clock for the `tx_outclock` signal. If you select **Auto** in the Quartus II software, the tool will use any available lines.

## SERDES Bypass Mode

You can bypass the SERDES block if your data rate is less than 462 MHz, and you must bypass the SERDES block for the ×1 and ×2 LVDS modules.

Since you cannot route the fast PLL output to an output pin, you must create additional DDR I/O circuitry for the transmitter clock output. To create an ×*J* transmitter output clock, instantiate an `alt_ddio` megafunction clocked by the ×*J* clock with `datain_h` connected to $V_{CC}$ and `datain_l` connected to `GND`.

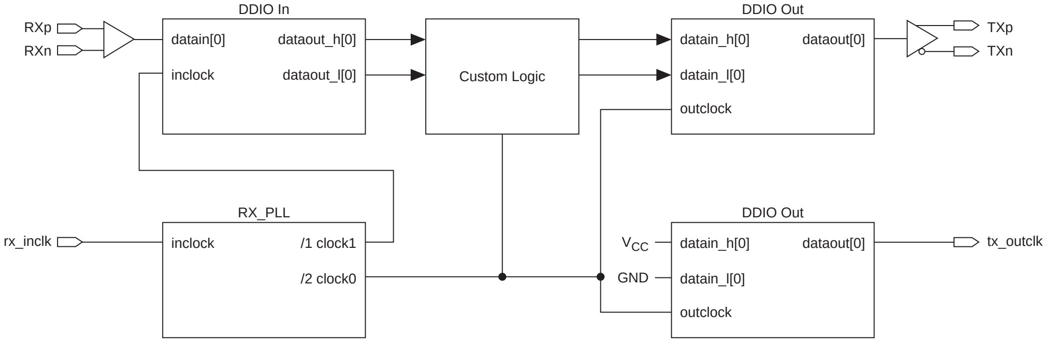
### ×1 Mode

For ×1 mode, you only need to specify the I/O standard of the pins to tell the Quartus II software that you are using differential signaling. However, Altera recommends using the DDRIO circuitry when the input or output data rate is higher than 231 Mbps. The maximum output clock frequency for ×1 mode is 462 MHz.

### ×2 Mode

You must use the DDRIO circuitry for ×2 mode. The Quartus II software provides the `altddio_in` and `altddio_out` megafunctions to use for ×2 receiver and ×2 transmitter, respectively. The maximum data rate in ×2 mode is 462 Mbps. Figure 5–45 shows the schematic for using DDR circuitry in ×2 mode.

*Figure 5–45. LVDS x2 Mode Schematic Using DDR I/O Circuitry*



The transmitter output clock requires extra DDR output circuitry that has the input high and input low connected to $V_{CC}$ and `GND` respectively. The output clock frequency is the same as the input frequency of the DDR output circuitry.

### *Other Modes*

For other modes, you can still to use the DDR circuitry for better frequency performance. You can use either the LEs or the M512 RAM block for the deserialization.

#### M512 RAM Block as Serializer/Deserializer Interface

In addition to using the DDR circuitry and the M512 RAM block, you need two extra counters per memory block to provide the address for the memory: a fast counter powering up at 0 and a slow counter powering up at 2. The M512 RAM block is configured as a simple dual-port memory block, where the read enable and the write enable signals are always tied high. Figures 5–46 and 5–47 show the block diagram for the SERDES bypass receiver and SERDES bypass transmitter, respectively.

*Figure 5–46. SERDES Bypass LVDS Receiver Using M512 RAM Block as the Deserializer*

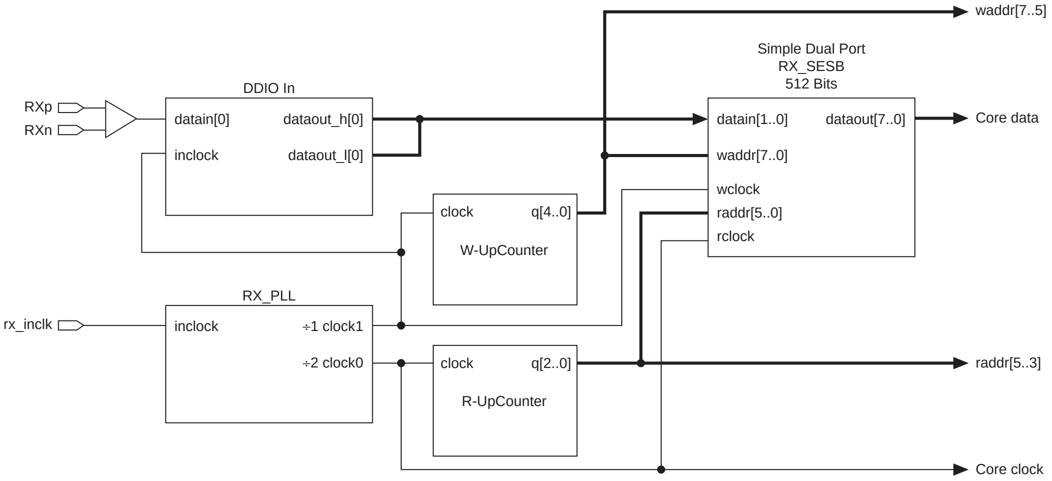
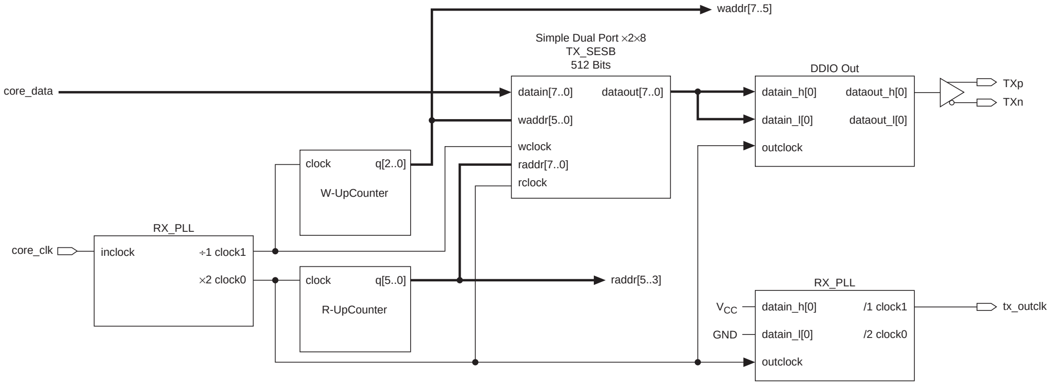


*Figure 5–47. SERDES Bypass LVDS Transmitter Using M512 RAM Block as Deserializer*



For the transmitter, the read counter is the fast counter and the write counter is the slow counter. For the receiver, the write counter is the fast counter and the read counter is the slow counter. Tables 5–18 and 5–19 provide the address counter configurations for the transmitter and the receiver, respectively.

*Table 5–18. Address Counters for SERDES Bypass LVDS Receiver*

| M512 Mode | Deserialization Factor | Write Up-Counter (Fast Counter) | | Read Up-Counter (Slow Counter) | | Invalid Initial Cycles | |
|---|---|---|---|---|---|---|---|
| | | Width | Starts at | Width | Starts at | Write | Read |
| X2X4 | 4 | 4 | 0 | 3 | 2 | 12 | 6 |
| X2X8 | 8 | 5 | 0 | 3 | 2 | 24 | 6 |
| X4X16 | 8 | 5 | 0 | 3 | 2 | 24 | 6 |
| X2X16 | 16 | 6 | 0 | 3 | 2 | 48 | 6 |

*Table 5–19. Address Counters for SERDES Bypass LVDS Transmitter*

| M512 Mode | Deserialization Factor | Write Up-Counter (Fast Counter) | | Read Up-Counter (Slow Counter) | | Invalid Initial Cycles | |
|---|---|---|---|---|---|---|---|
| | | Width | Starts at | Width | Starts at | Write | Read |
| X2X4 | 4 | 4 | 0 | 3 | 2 | 2 | 4 |
| X2X8 | 8 | 5 | 0 | 3 | 2 | 2 | 8 |
| X4X16 | 8 | 5 | 0 | 3 | 2 | 2 | 8 |
| X2X16 | 16 | 6 | 0 | 3 | 2 | 2 | 16 |

In different M512 memory configurations, the counter width is smaller than the address width, so you must ground some of the most significant address bits. Table 5–20 summarizes the address width, the counter width, and the number of bits to be grounded.

*Table 5–20. Address & Counter Width*

| M512 Mode | Write Counter Width | Read Counter Width | Write Address Width | Read Address Width | Number of Grounded Bits | |
|---|---|---|---|---|---|---|
| | | | | | Write Address | Read Address |
| X2X4 | 4 | 3 | 8 | 7 | 4 | 4 |
| X2X8 | 5 | 3 | 8 | 6 | 3 | 3 |
| X4X16 | 6 | 3 | 7 | 5 | 1 | 2 |
| X2X16 | 5 | 3 | 8 | 5 | 3 | 2 |

### Logic Array as Serializer/Deserializer Interface

The design can use the `lpm_shift_reg` megafunction instead of a simple dual port memory block to serialize/deserialize data. The receiver requires an extra flip-flop clocked by the slow clock to latch on to the deserialized data. The transmitter requires a counter to generate the enable signal for the shift register to indicate the times to load and serialize the data. Figures 5–48 and 5–49 show the schematic of the ×8 LVDS receiver and ×8 LVDS transmitter, respectively, with the logic array performing the deserialization.

This scheme can also be used for APEX II and Mercury device flexible LVDS solutions.

*Figure 5–48. SERDES Bypass LVDS Receiver with Logic Array as Deserializer*

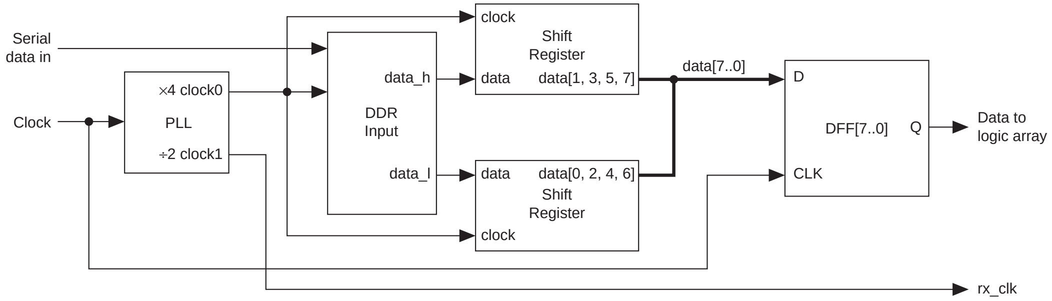
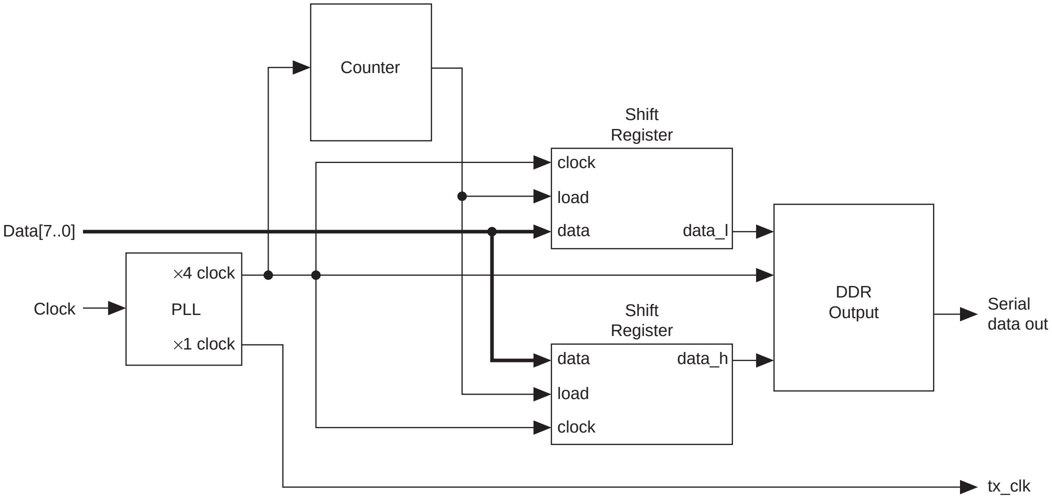


*Figure 5–49. SERDES Bypass LVDS Transmitter with Logic Array as Deserializer*



## Summary

The Stratix device family of flexible, high-performance, high-density PLDs delivers the performance and bandwidth necessary for complex system-on-a-programmable-chip (SOPC) solutions. Stratix devices support multiple I/O protocols to interface with other devices within the system. Stratix devices can easily implement processing-intensive data-path functions that are received and transmitted at high speeds. The Stratix family of devices combines a high-performance enhanced PLD architecture with dedicated I/O circuitry in order to provide I/O standard performances of up to 840 Mbps.

# Section IV. Digital Signal Processing (DSP)

This section provides information for design and optimization of digital signal processing (DSP) functions and arithmetic operations in the on-chip DSP blocks.

It contains the following chapters:

- Chapter 6. Using the DSP Blocks in Stratix & Stratix GX Devices
- Chapter 7. Implementing High-Performance DSP Functions in Stratix & Stratix GX Devices

## Revision History

The table below shows the revision history for Chapters 6 and 7.

| Chapter(s) | Date / Version | Changes Made |
|---|---|---|
| 6 | April 2003<br>v1.0 | Added document to the Stratix Device Handbook. |
| 7 | April 2003<br>v1.0 | Added document to the Stratix Device Handbook. |

# 6. Using the DSP Blocks in Stratix & Stratix GX Devices

S52006-1.0

Chapter 6, Using the DSP Blocks in Stratix & Stratix GX Devices replaces *AN 214: Using the DSP Blocks in Stratix & Stratix GX Devices*.

## Introduction

Traditionally, designers had to make a trade-off between the flexibility of off-the-shelf digital signal processors and the performance of custom-built devices. Altera® Stratix™ and Stratix GX devices eliminate the need for this trade-off by providing exceptional performance combined with the flexibility of programmable logic devices (PLDs). Stratix and Stratix GX devices have dedicated digital signal processing (DSP) blocks, which have high-speed parallel processing capabilities, that are optimized for DSP applications. DSP blocks are ideal for implementing DSP applications that need high data throughput.

The most commonly used DSP functions are finite impulse response (FIR) filters, complex FIR filters, infinite impulse response (IIR) filters, fast Fourier transform (FFT) functions, discrete cosine transform (DCT) functions, and correlators. These functions are the building blocks for more complex systems such as wideband code division multiple access (W-CDMA) basestations, voice over Internet protocol (VoIP), and high-definition television (HDTV).

Although these functions are complex, they all use similar building blocks such as multiply-adders and multiply-accumulators. Stratix and Stratix GX DSP blocks combine five arithmetic operations—multiplication, addition, subtraction, accumulation, and summation—to meet the requirements of complex functions and to provide improved performance.

This application note describes the Stratix and Stratix GX DSP blocks, and explains how you can use them to implement high-performance DSP functions. It addresses the following topics:

- Architecture
- Operational Modes
- Software Support
- Quartus II DSP Megafunctions

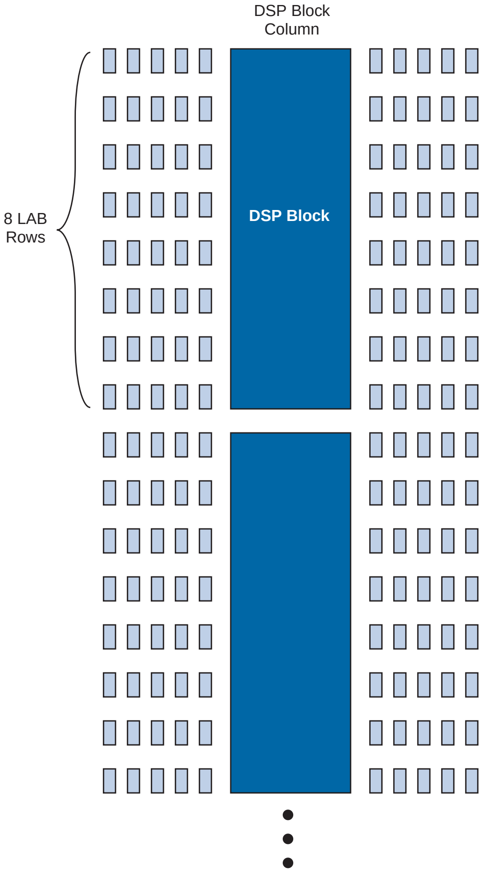
Refer to Section I, Stratix Device Family Data Sheet of the *Stratix Device Handbook, Volume 1* and the *Stratix GX FPGA Family Data Sheet* for more information on Stratix and Stratix GX devices, respectively.

# DSP Block Overview

Each Stratix and Stratix GX device has two columns of DSP blocks that efficiently implement multiplication, multiply accumulate (MAC), and filtering functions. Figure 6–1 shows one of the columns with surrounding LAB rows. You can configure each DSP block to support:

- Eight 9 × 9 bit multipliers
- Four 18 × 18 bit multipliers
- One 36 × 36 bit multiplier

*Figure 6–1. DSP Blocks Arranged in Columns*



The multipliers can then feed an adder or an accumulator block, depending on the DSP block operational mode. Additionally, you can use the DSP block input registers as shift registers to implement applications such as FIR filters efficiently. The number of DSP blocks per column increases with device density. Tables 6–1 and 6–2 describe the number of DSP blocks in each Stratix and Stratix GX device, respectively, and the multipliers that you can implement.

***Table 6–1. Number of DSP Blocks in Stratix Devices*** *Note (1)*

| Device | DSP Blocks | 9 × 9 Multipliers | 18 × 18 Multipliers | 36 × 36 Multipliers |
|---|---|---|---|---|
| EP1S10 | 6 | 48 | 24 | 6 |
| EP1S20 | 10 | 80 | 40 | 10 |
| EP1S25 | 10 | 80 | 40 | 10 |
| EP1S30 | 12 | 96 | 48 | 12 |
| EP1S40 | 14 | 112 | 56 | 14 |
| EP1S60 | 18 | 144 | 72 | 18 |
| EP1S80 | 22 | 176 | 88 | 22 |

***Table 6–2. Number of DSP Blocks in Stratix GX Devices*** *Note (1)*

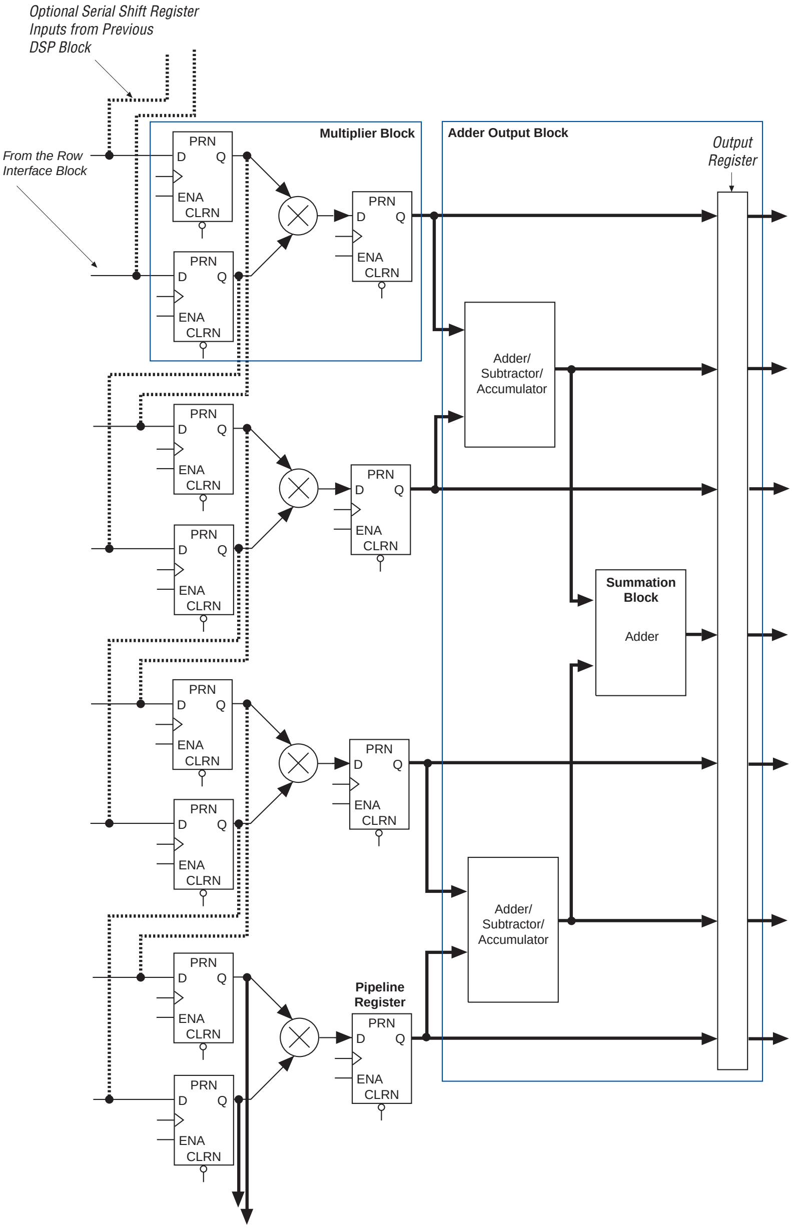
| Device | DSP Blocks | 9 × 9 Multipliers | 18 × 18 Multipliers | 36 × 36 Multipliers |
|---|---|---|---|---|
| EP1SGX10C | 6 | 48 | 24 | 6 |
| EP1SGX10D | 6 | 48 | 24 | 6 |
| EP1SGX25C | 10 | 80 | 40 | 10 |
| EP1SGX25D | 10 | 80 | 40 | 10 |
| EP1SGX25F | 10 | 80 | 40 | 10 |
| EP1SGX40D | 14 | 112 | 56 | 14 |
| EP1SGX40G | 14 | 112 | 56 | 14 |

***Note to Tables 6–1 and 6–2:***

(1) Each device has either the number of 9 · 9-, 18 · 18-, or 36 · 36-bit multipliers shown. The total number of multipliers for each device is not the sum of all the multipliers.

Figure 6–2 shows the DSP block operating as an 18 × 18 multiplier.

*Figure 6–2. DSP Block in 18 × 18 Mode*



# Architecture

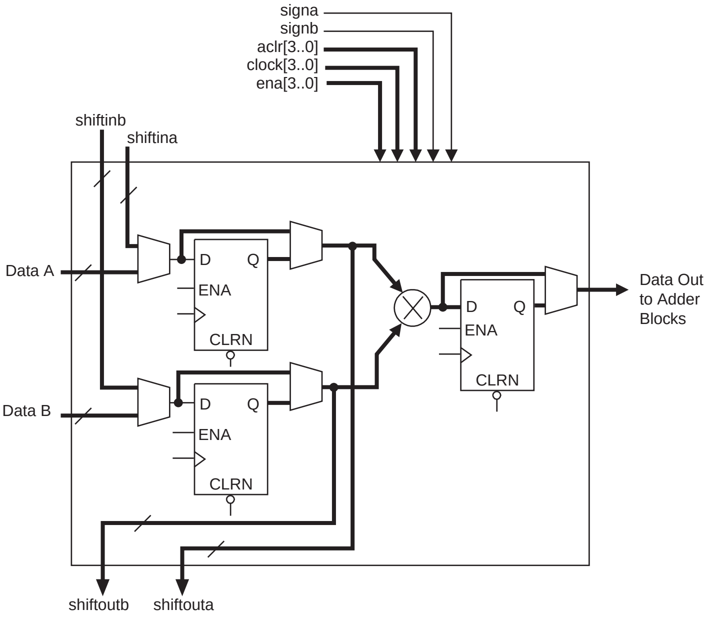
The DSP block consists of the following elements:

- A multiplier block
- An adder/subtractor/accumulator block
- A summation block
- An output interface
- Output registers
- Routing and control signals

## Multiplier Block

Each multiplier block has input registers, a multiplier stage, and a pipeline register. See Figure 6–3.

**Figure 6–3. Multiplier Block Architecture**



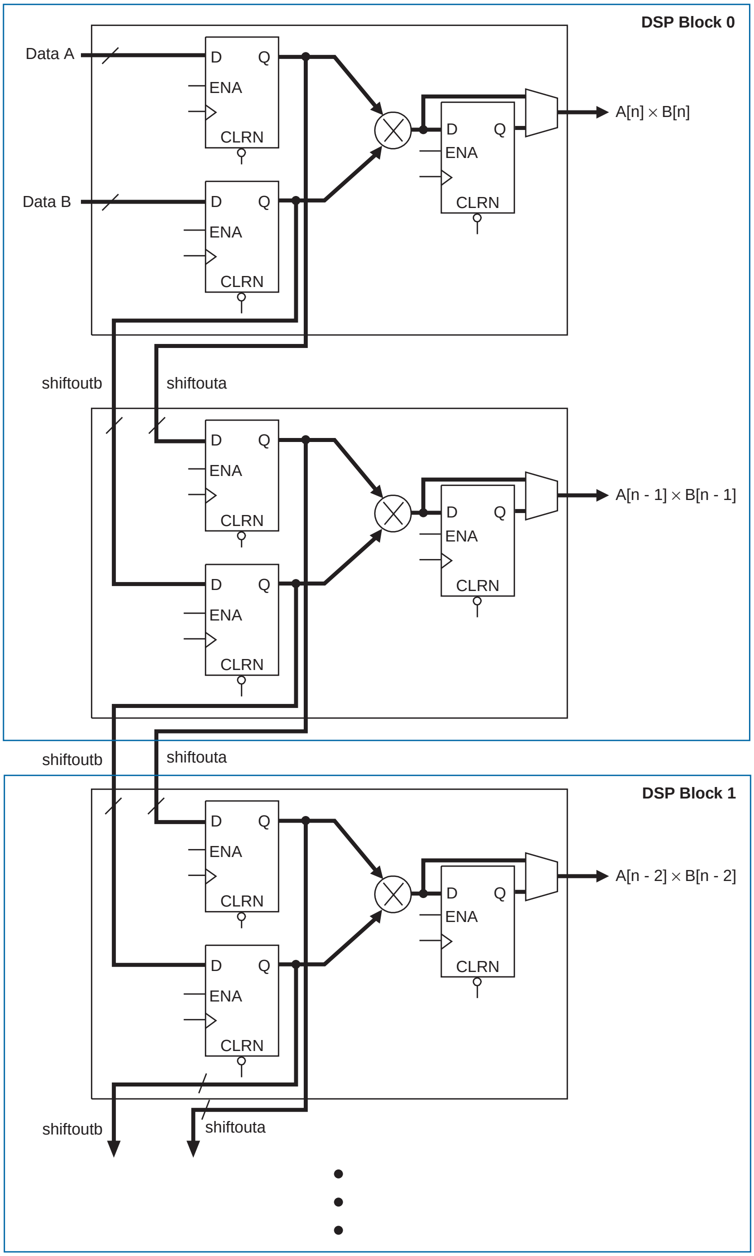
### *Input Registers*

Each operand feeds an input register or the multiplier directly. The DSP block has the following signals (one of each controls every input and output register):

- `clock[3..0]`
- `ena[3..0]`
- `aclr[3..0]`

The input registers feed the multiplier and drive two dedicated shift output lines, `shiftouta` and `shiftoutb`. The shift outputs from one multiplier block directly feed the adjacent multiplier block in the same DSP block (or the next DSP block), as shown in Figure 6–4 on page 6–7, to form a shift register chain. This chain can terminate in any block, i.e., you can create any length of shift register chain up to 224 registers. A shift register is useful in DSP applications such as FIR filters. When implementing 9 × 9 and 18 × 18 multipliers, you do not need external logic to create the shift register chain because the input shift registers are internal to the DSP block. This implementation greatly reduces the required LE count and routing resources, and produces repeatable timing.

*Figure 6–4. Shift Register Chain*



### *Multiplier Stage*

The multiplier stage supports 9 × 9, 18 × 18, or 36 × 36 multiplication. (The multiplier stage also support smaller multipliers. Refer to "Operational Modes" on page 6–18 for details.) Based on the data width, a single DSP block can perform many multiplications in parallel.

The multiplier operands can be signed or unsigned numbers. Two signals, `signa` and `signb`, indicate the representation of the two operands. For example, a logic 1 on the `signa` signal indicates that data A is a signed number; a logic 0 indicates an unsigned number. The result of the multiplication is signed if any one of the operands is a signed number, as shown in Table 6–3.

***Table 6–3. Multiplier Signed Representation***

| Data A | Data B | Result |
|---|---|---|
| Unsigned | Unsigned | Unsigned |
| Unsigned | Signed | Signed |
| Signed | Unsigned | Signed |
| Signed | Signed | Signed |

The `signa` and `signb` signals affect the entire DSP block. Therefore, all of the data A inputs feeding the same DSP block must have the same sign representation. Similarly, all of the data B inputs feeding the same DSP block must have the same sign representation. The multiplier offers full precision regardless of the sign representation.

☞ By default, the Altera Quartus® II software sets the multiplier to perform unsigned multiplication when the `signa` and `signb` signals are not used.

### *Pipeline Registers*

The output from the multiplier can feed a pipeline register or be bypassed. You can use pipeline registers for any multiplier size; pipelining is useful for increasing the DSP block performance, particularly when using subsequent adder stanges.

☞ In the DSP block, pipelining improves the performance of 36 × 36 multipliers. For 18 × 18 multipliers and smaller, pipelining adds latency but does not improve performance.

## Adder/Output Block

The adder/output block has the following elements (See Figure 6–5 on page 6–10):

- An adder/subtractor/accumulator block
- A summation block
- An output select multiplexer
- Output registers

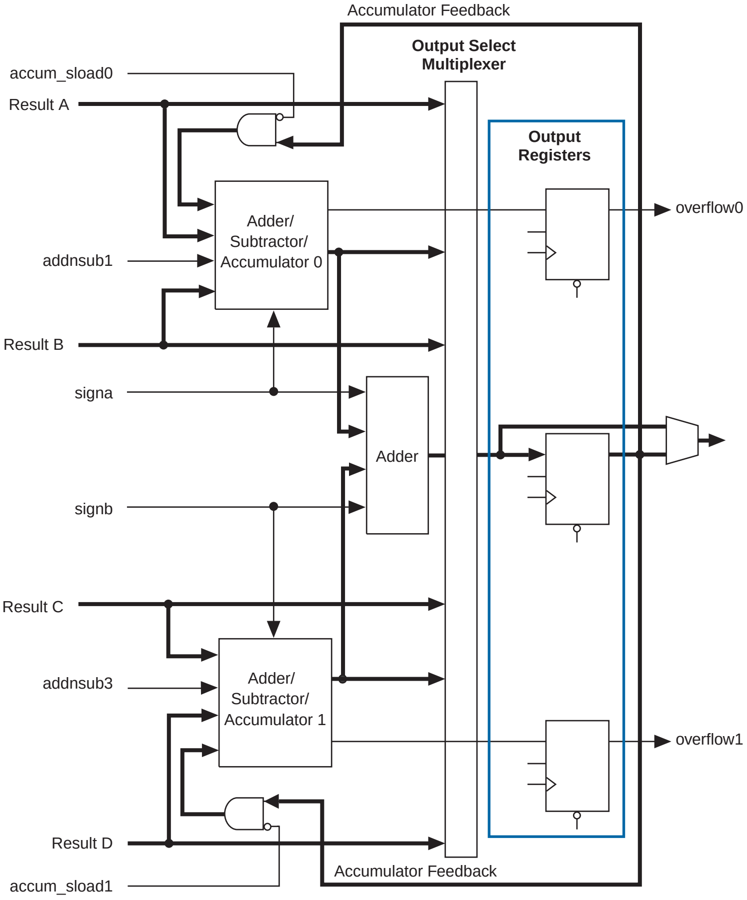
You can configure the adder/output block as:

- A pure output interface
- An accumulator
- A simple one-level adder
- A two-level adder with dynamic addition/subtraction control on the first-level adder
- The final stage of a 36-bit multiplier

The output select multiplexer sets the output of the DSP block. You can register the adder/output block's output using the output registers.

☞ You cannot use the adder/output block independently from the multiplier.

*Figure 6–5. Adder/Output Block*



### *Adder/Subtractor/Accumulator Block*

The adder/subtractor/accumulator is the first level of the adder/output block. You can configure the block as an accumulator or as an adder/subtractor.

**Accumulator**

When the adder/subtractor/accumulator is configured as an accumulator, the output of the adder/output block feeds back to the accumulator as shown in Figure 6–5 on page 6–10. You can use the `accum_sload[1..0]` signals to clear the accumulator asynchronously. This action is not the same as resetting the output registers. You can clear the accumulation and begin a new one without losing any clock cycles.

The `overflow` signal goes high on the positive edge of the clock when the accumulator overflows or underflows. In the next clock cycle, however, the `overflow` signal resets to zero even though an overflow (or underflow) occurred in the previous clock cycle. Use a latch to preserve the overflow condition indefinitely (until the latch is cleared).

#### Adder/Subtractor

The `addnsub[1..0]` signals select addition or subtraction: high for addition and low for subtraction. You can control the `addnsub[1..0]` signals using external logic; therefore, the first-level block can switch from an adder to a subtractor dynamically, simply by changing the `addnsub[1..0]` signals. If the first stage is configured as a subtractor, the output is A - B and C - D.

The adder/subtractor also uses two signals, `signa` and `signb`, like the multiplier block. These signals indicate the sign representation of both operands together. You can register the signals with a latency of 1 or 2 clock cycles.

### *Summation Block*

The output from the adder/subtractor feeds to an optional summation block, which is an adder block that sums the outputs of the adder/subtractor. The summation block is important in applications such as FIR filters.

### *Output Select Multiplexer*

The outputs from the various elements of the adder/output block are routed through an output select multiplexer. Based on the DSP block operational mode, the outputs of the multiplier block, adder/subtractor/accumulator, or summation block feed straight to the output, bypassing the remaining blocks in the DSP block.

☞ The output select multiplier configuration is configured automatically by software.

### *Output Registers*

You can use the output registers to register the DSP block output. Like the input registers, the output registers are controlled by the four `clock[3..0]`, `aclr[3..0]`, and `ena[3..0]` signals. You can use the output registers in any DSP block operational mode.

☞ The output registers form part of the accumulator in the multiply-accumulate mode.

## Routing Structure & Control Signals

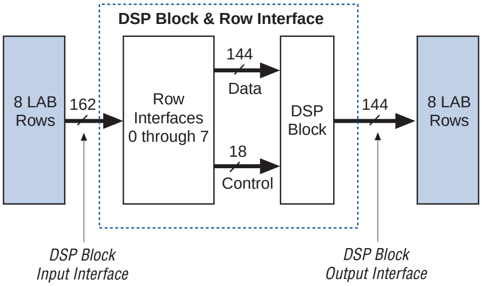
This section describes the interface between the DSP blocks and the row interface blocks. It also describes how the DSP block generates control signals and how the signals route from the row interface to the DSP block.

### *DSP Block Interface*

The DSP blocks are organized in columns, which provides efficient horizontal communication between the blocks and the column-based memory blocks. The DSP block communicates with other parts of the device through an input and output interface. Each DSP block, including the input and output interface, is 8 logic array blocks (LABs) long.

The DSP block and row interface blocks consist of eight blocks that connect to eight adjacent LAB rows on the left and right. Each of the eight blocks has two regions: right and left, one per row. The DSP block receives 144 data input signals and 18 control signals for a total of 162 input signals. This block drives out 144 data output signals; 2 of the data signals can be used as overflow signals (`overflow`). Figure 6–6 provides an overview of the DSP block and its interface to adjacent LABs.

*Figure 6–6. DSP Block Interface to Adjacent LABs*



**Input Interface**
The DSP block input interface has 162 input signals from adjacent LABs; 18 data signals per row and 18 control signals per block.

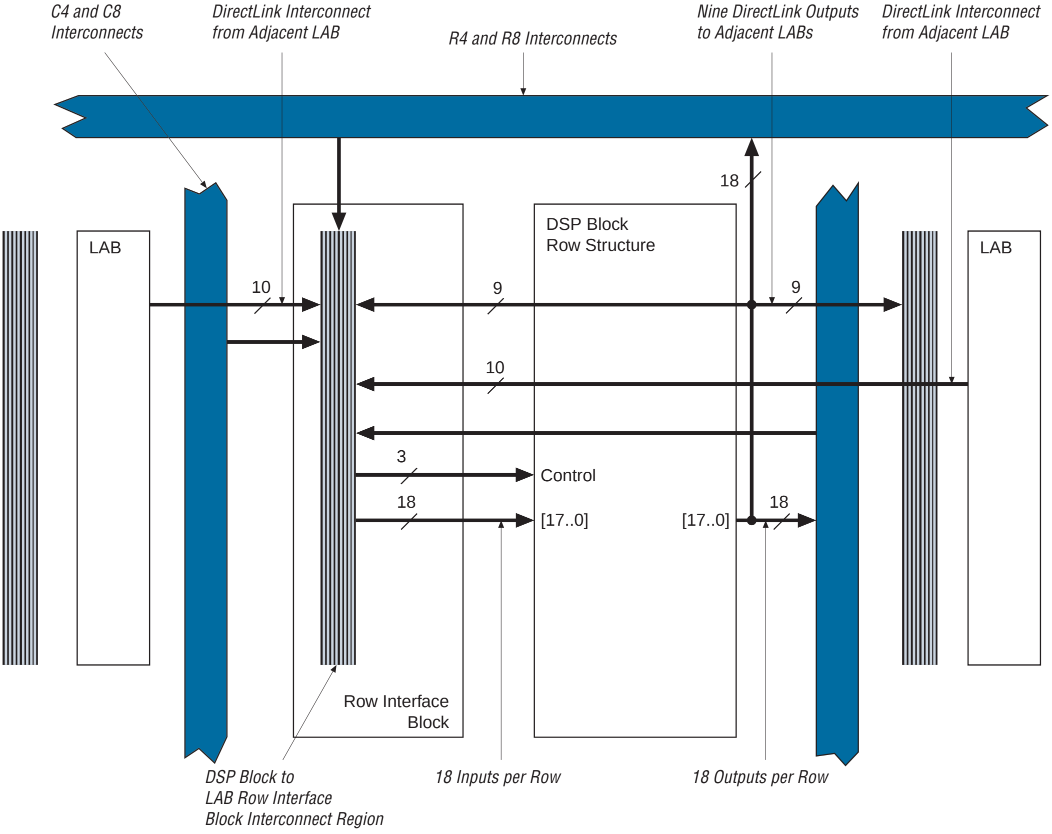
**Output Interface**
The DSP block output interface drives 144 outputs to adjacent LABs, 18 signals per row from 8 rows.

Because the DSP block outputs communicate horizontally, and because each DSP block row has more outputs than an LAB (18 from the DSP block compared to 10 from an LAB), the DSP block has double the number of row channel drivers compared to an LAB. The DSP block has the same number of row channels, but the row channels are staggered as if there were two LABs within each block. The DSP blocks have the same number of column channels as LABs because DSP blocks communicate primarily through row channels.

**Row Interface Block**

Each row interface block connects to the DSP block row structure with 21 signals. Because each DSP block has eight row interface blocks, this block receives 162 signals from the eight row interfaces. Of the 162 signals, 144 are data inputs and 18 are control signals. Figure 6–7 on page 6–14 shows one row block within the DSP block.

*Figure 6–7. DSP Row Interface Block*



### *Control Signals in the Row Interface Block*

The DSP block has a set of input registers, a pipeline register, and an output register. Each register is grouped in banks that share the same clock and clear resources:

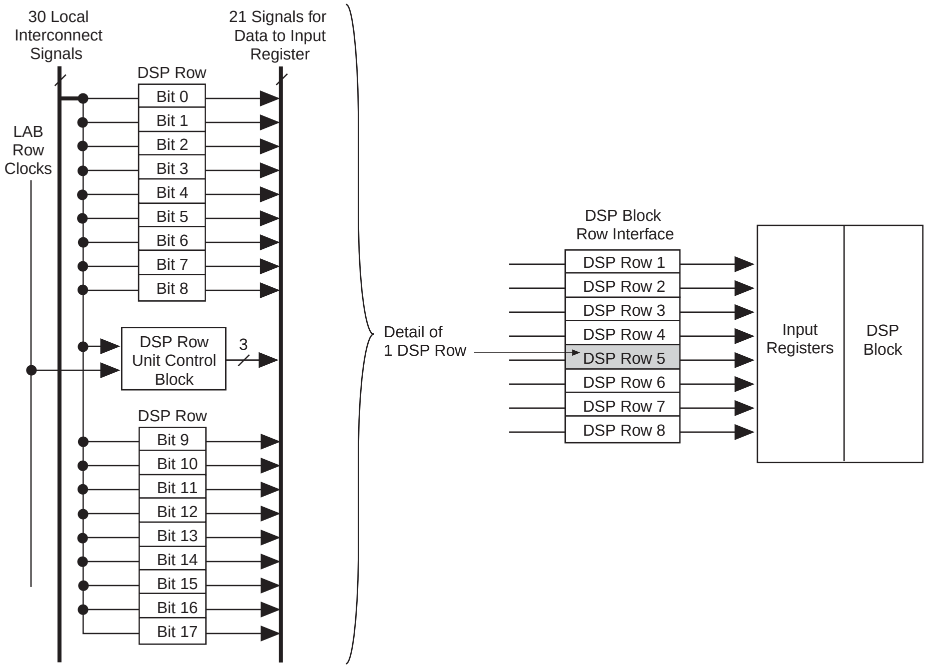
- 1- to 9-bit banks for the input register
- 1- to 18-bit banks for the pipeline register
- 18 bits for the output register

The row interface block generates the control signals and routes them to the DSP block. Each DSP block has 18 control signals:

- Four clock signals (`clock[3..0]`), which are available to each bank of DSP blocks
- Four clear signals (`aclr[3..0]`), which are available to each bank of DSP blocks
- Four clock enable signals (`ena[3..0]`), which the whole DSP block can use
- `signa` and `signb`, which are specific to each DSP block
- `addnsub[1..0]` signals
- `accum_sload[1..0]` signals

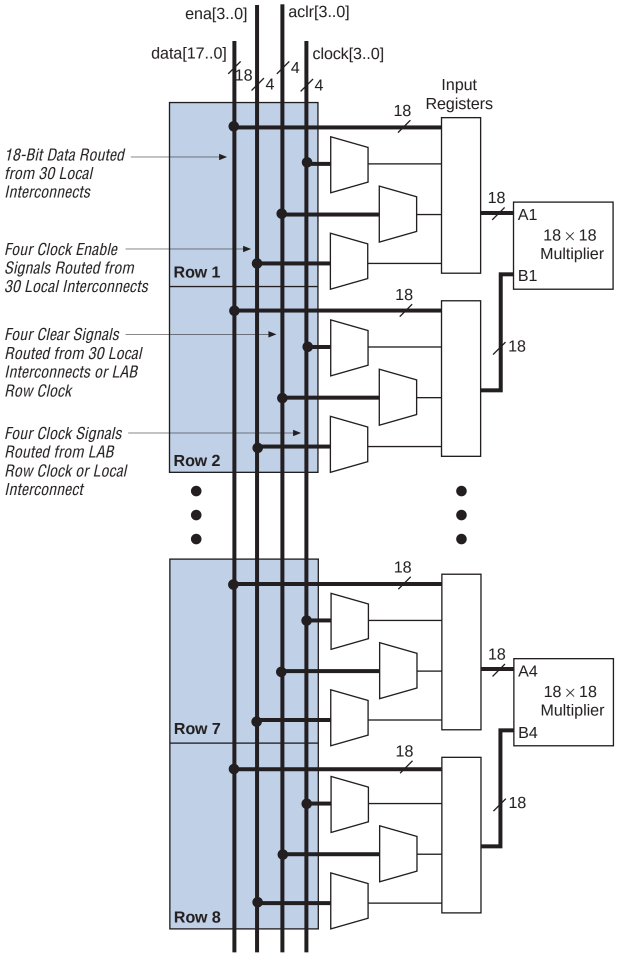
The `signa`, `signb`, and `addnsub[1..0]`, `accum_sload[1..0]` signals have independent clocks and clears and can be registered individually. When each 18 × 18 multiplier in the DSP block splits in half to two 9 × 9 multipliers, each 9 × 9 multiplier has independent control signals. Figure 6–8 shows the DSP block row interface and shows how it generates the data and control signals.

*Figure 6–8. DSP Block Row Interface*



The DSP block interface generates the clock signals from LAB row clocks or the local interconnect. The clear signals are generated from the local interconnects within each DSP block row interface or from LAB row clocks. The four clock enable signals are generated from the 30 local interconnects from the same LAB rows that generate the clock signals. The clock enable is paired with the clock because the enable logic is implemented at the interface. Figure 6–9 shows the signal distribution within the row interface block.

*Figure 6–9. DSP Block Row Interface Signal Distribution*



Each row block provides 18 bits of data to the multiplier (i.e., one of the operands to the multiplier), which are routed through the 30 local interconnects within each DSP row interface block. Any signal in the device can be the source of the 18-bit multiplier data, by connecting to the local row interconnect through any row or column.

Each control signal routes through one of the eight rows of the DSP block. Table 6–4 shows the 18 control signals and the row to which each one routes.

*Table 6–4. Control Signals in DSP Block*

| Signal Name | Row | Description |
|---|---|---|
| `signa` | 1 | DSP block-wide signed and unsigned control signals for all multipliers. The multiplier outputs are unsigned only if both `signa` and `signb` are low. |
| `signb` | 6 | |
| `addnsub1` | 3 | Controls addition or subtraction of the two one-level adders. The `addnsub0` signal controls the top two one-level adders; the `addnsub1` signal controls the bottom two one-level adders. A high indicates addition; a low indicates subtraction. |
| `addnsub3` | 7 | |
| `accum_sload0` | 2 | Resets the feedback input to the accumulator. The signal asynchronously clears the accumulator and allows new accumulation to begin without losing any clock cycles. The `accum_sload0` controls the top two one-level adders, and the `accum_sload1` controls the bottom two one-level adders. A low is for normal accumulation operations and a high is for zeroing the accumulator. |
| `accum_sload1` | 7 | |
| `clock0` | 3 | DSP block-wide clock signals. |
| `clock1` | 4 | |
| `clock2` | 5 | |
| `clock3` | 6 | |
| `aclr0` | 1 | DSP block-wide clear signals. |
| `aclr1` | 4 | |
| `aclr2` | 5 | |
| `aclr3` | 7 | |
| `ena[3..0]` | Same rows as the Clock Signals | DSP block-wide clock enable signals. |

### *Input/Output Data Interface Routing*

The 30 local interconnects generate the 18 inputs to the row interface blocks. The 21 outputs of the row interface block are the inputs to the DSP row block (see Figure 6–7 on page 6–14).

The row interface block has DirectLink™ connections that connect the DSP block input or output signals to the left and right adjacent LABs at each row. (The DirectLink connections provide interconnects between LABs and adjacent blocks.) The DirectLink connection reduces the use of row and column interconnects, providing higher performance and flexibility.

Each row interface block receives 10 DirectLink connections from the right adjacent LABs and 10 from the left adjacent LABs. Additionally, the row interface block receives signals from the DSP block, making a total of 30 local interconnects for each row interface block. All of the row and column resources within the DSP block can access this interconnect region (see Figure 6–7 on page 6–14).

A DSP block has nine outputs that drive the right adjacent LAB and nine that drive the left adjacent LAB through DirectLink interconnects. All 18 outputs drive any row or column.

## Operational Modes

You can use the DSP block in one of four operational modes, depending on your application needs (see Table 6–4). The Quartus II software has built-in megafunctions that you can use to control the mode. After you have made your parameter settings using the megafunction's MegaWizard® Plug-In, the Quartus II software automatically configures the DSP block.

*Table 6–5. DSP Block Operational Modes*

| Mode | 9 × 9 | 18 × 18 | 36 × 36 |
|---|---|---|---|
| Simple multiplier | Eight multipliers with eight product outputs | Four multipliers with four product outputs | One multiplier |
| Multiply accumulator | Two 34-bit multiply-accumulate blocks | Two 52-bit multiply-accumulate blocks | – |
| Two-multiplier adder | Four two-multiplier adders | Two two-multiplier adders | – |
| Four-multiplier adder | Two four-multiplier adders | One four-multiplier adder | – |

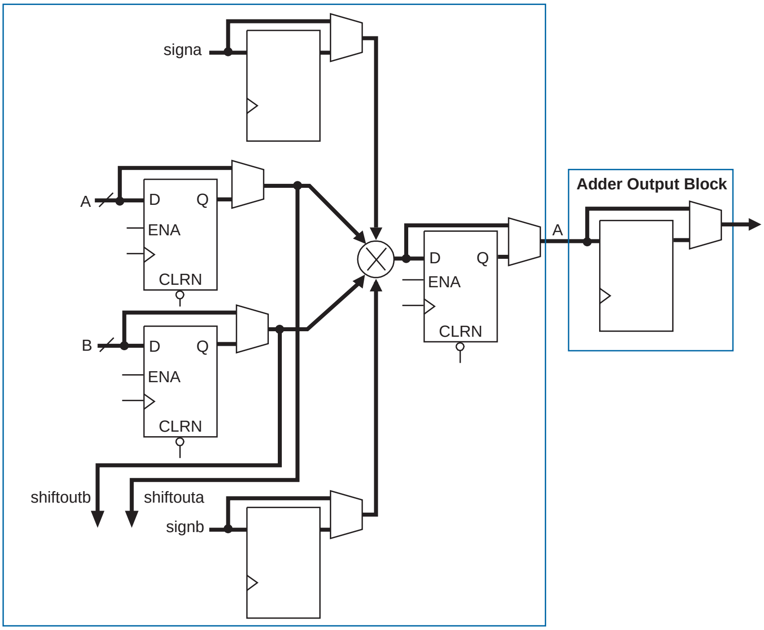
### Simple Multiplier Mode

In simple multiplier mode, the DSP block performs individual multiplication operations for general-purpose multipliers and for applications such as equalizer coefficient updates that require many individual multiplication operations.

### 9- & 18-Bit Multipliers

You can configure each DSP block multiplier for 9 or 18 bits. A single DSP block can support up to 8 individual 9-bit or smaller multipliers, or up to 4 individual multipliers with operand widths between 10- and 18-bits. Figure 6–10 shows the simple multiplier mode.

**Figure 6–10. Simple Multiplier Mode**



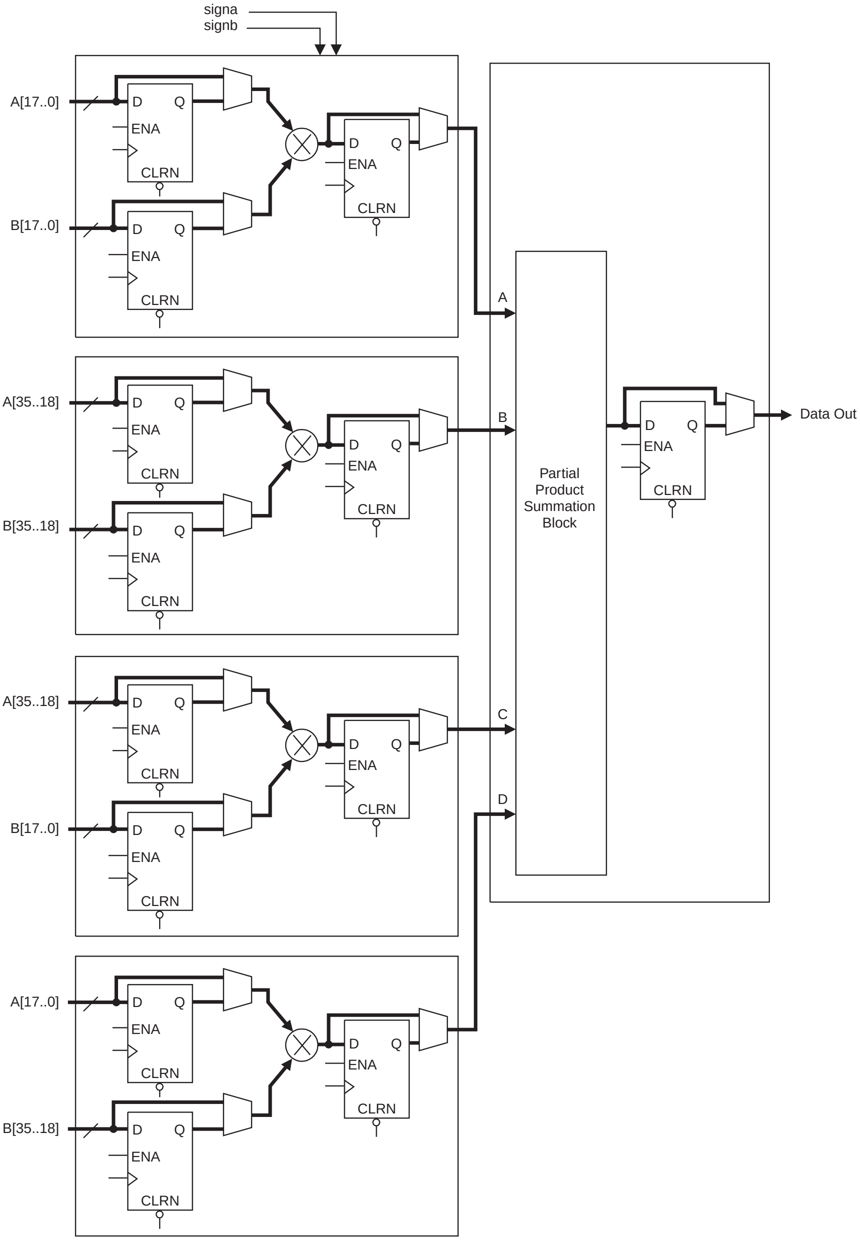
The multiplier operands can accept signed integers, unsigned integers, or a combination. The `signa` and `signb` signals are dynamic and can be registered in the DSP block. Additionally, you can register the multiplier inputs and results independently. Pipelining the result, using the pipeline registers in the block, increases the performance of the DSP block.

### 36-Bit Multiplier

The 36-bit multiplier is a subset of the simple multiplier mode. It uses the entire DSP block to implement one 36 × 36-bit multiplier. The four 18-bit multipliers are fed part of each input, as shown in Figure 6–11 on page 6–21. The adder/output block adds the partial products using the summation block. You can use pipeline registers between the multiplier stage and the summation block. The 36 × 36-bit multiplier supports signed and unsigned operation.

The 36-bit multiplier is useful when your application needs more than 18-bit precision, for example, for mantissa multiplication of precision floating-point arithmetic applications.

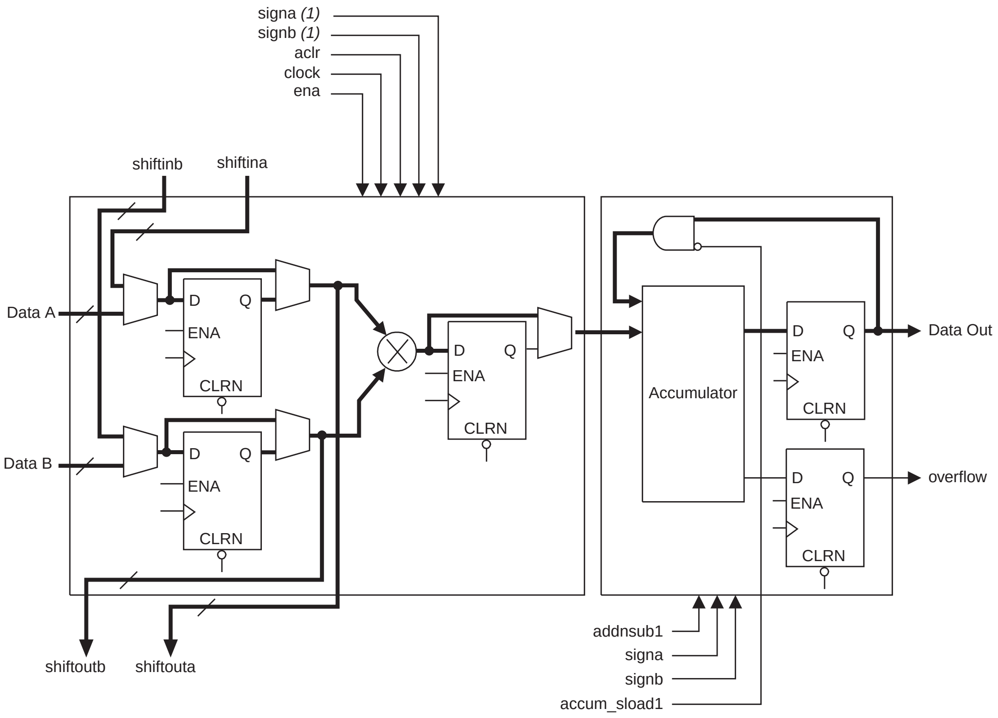
*Figure 6–11. 36-Bit Multiplier*



## Multiply Accumulator Mode

In multiply accumulator mode, the output of the multiplier stage feeds the adder/output block, which is configured as an accumulator or subtractor (see Figure 6–12). You can implement up to two independent 18-bit multiply accumulators in one DSP block. The Quartus II software implements smaller multiplier-accumulators by tying the unused low-order bits of an 18-bit multiplier to ground.

*Figure 6–12. Multiply Accumulator Mode*



*Note to Figure 6–12:*

(1) The `signa` and `signb` signals are the same in the multiplier stage and the adder/output block.

The multiply accumulator output can be up to 52 bits wide for a maximum 36-bit result with 16-bits of accumulation. In this mode, the DSP block uses output registers and the `accum_sload` and `overflow` signals. The `accum_sload[1..0]` signal synchronously loads the multiplier result to the accumulator output. This signal can be unregistered or registered once or twice. The DSP block can then begin a new accumulation without losing any clock cycles. The `overflow` signal indicates an overflow or underflow in the accumulator. This signal is cleared for the next accumulation cycle, and you can use an external latch to preserve the signal. You can use the `addnsub[1..0]` signals to perform accumulation or subtraction dynamically.

If you want to use DSP blocks and your design only has an accumulator, you can use a multiply by one followed by an accumulator to force the software to implement the logic in the DSP block.

## Two-Multiplier Adder

The two-multiplier adder mode uses the adder/output block to add or subtract the outputs of the multiplier block, which is useful for applications such as FFT functions and complex FIR filters. Additionally, in this mode, the DSP block outputs two sums or differences for multipliers up to 18 bits, or 4 sums or differences for 9-bit or smaller multipliers. A single DSP block can implement one 18 × 18-bit complex multiplier or two 9 × 9-bit complex multipliers.

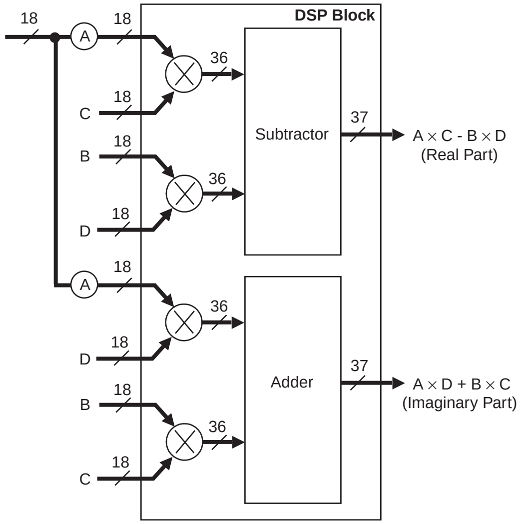
A complex multiplication can be written as:

$$(a + jb) \times (c + jd) = (a \times c - b \times d) + j \times (a \times d + b \times c)$$

In this mode, a single DSP block calculates the real part $(a \times c - b \times d)$ using one adder/subtractor/accumulator and the imaginary part $(a \times d + b \times c)$ using another adder/subtractor/accumulator for data up to 18 bits. Figure 6–13 shows an 18-bit complex multiplication. For data widths up to 9 bits, the DSP block can perform two complex multiplications using four one-level adders. Resources outside of the DSP block route each input to the two multiplier inputs.

You can only use the adder block if it follows multiplication operations.

*Figure 6–13. Complex Multiplier Implemented Using Two-Multiplier Adder Mode*



## Four-Multiplier Adder Mode

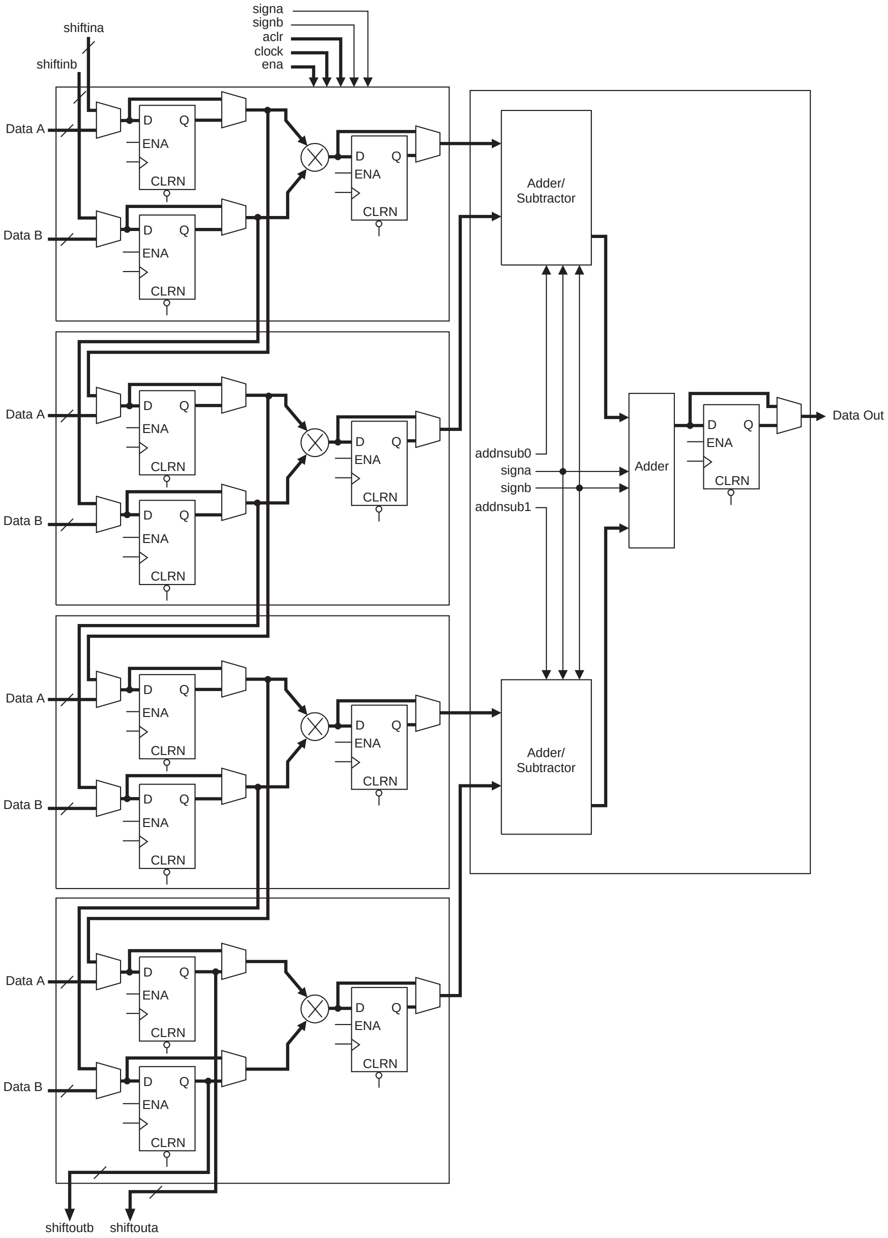
In the four-multiplier adder mode, which you can use for 1-dimensional and 2-dimensional filtering applications, the DSP block adds the results of two adder/subtractor/accumulators in a final stage (the summation block).

☞ You can only use the adder block if it follows multiplication operations.

### *9- & 18-Bit Summation Blocks*

A single DSP block can implement one 18 × 18 or two 9 × 9 summation blocks (see Figure 6–14 on page 6–25). The multiplier product widths must be the same size.

*Figure 6–14. Four-Multiplier Adder Mode*



### *FIR Filters*

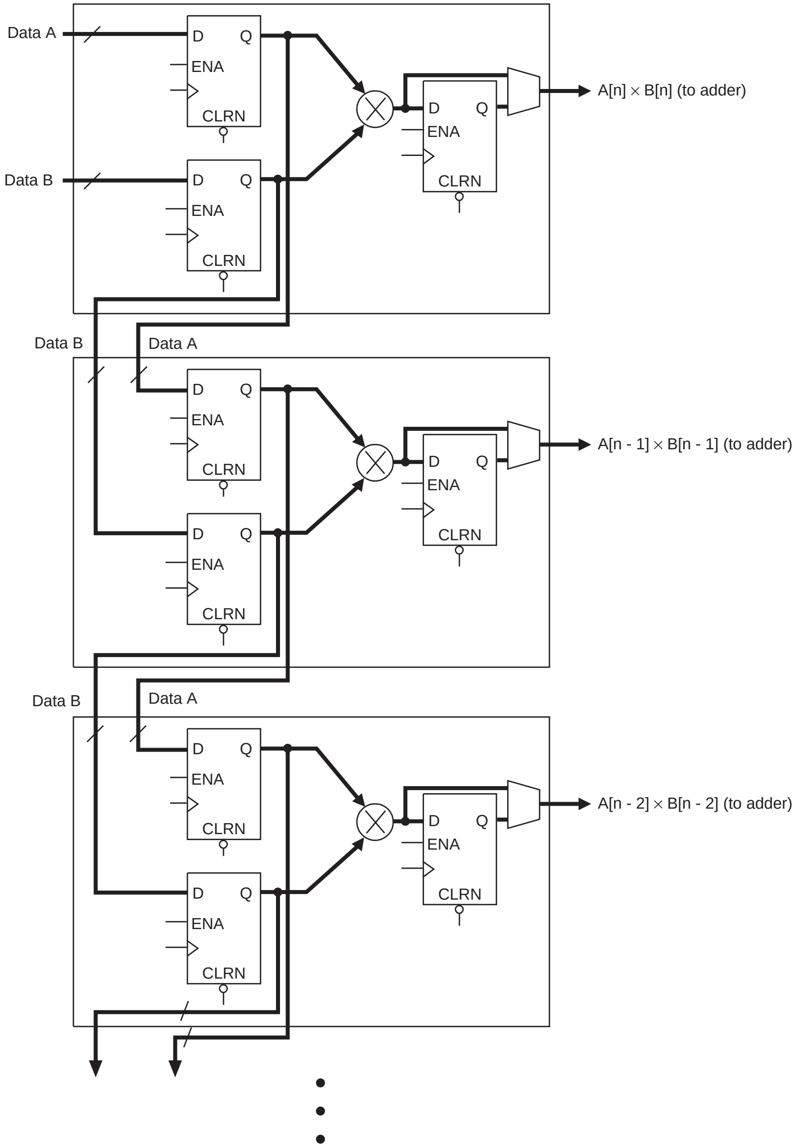
The four-multiplier adder mode can be used for FIR filter and complex FIR filter applications. The DSP block combines a four-multiplier adder with the input registers configured as shift registers. One set of shift inputs contains the filter data, while the other holds the coefficients, which can be loaded serially or in parallel (see Figure 6–15).

The input shift register eliminates the need for shift registers external to the DSP block (e.g., implemented in device logic elements). This architecture simplifies filter design and improves performance because the DSP block implements all of the filter circuitry.

☞ Serial shift inputs in 36-bit simple multiplier mode require external registers.

One DSP block can implement an entire 18-bit FIR filter with up to four taps. For FIR filters larger than four taps, you can cascade DSP blocks with additional adder stages implemented in logic elements.

Figure 6–15. Input Shift Registers Configured for a FIR Filter



## Software Support

Altera provides two distinct methods for implementing various modes of the DSP block in your design: instantiation and inference. Both methods use the following three Quartus II megafunctions:

- lpm_mult
- altmult_add
- altmult_accum

You can instantiate the megafunctions in the Quartus II software to use the DSP block. Alternatively, with inference, you create an HDL design and synthesize with a third-party synthesis tool (LeonardoSpectrum or Synplify) that infers the appropriate megafunction by recognizing multipliers, multiplier adders, and multiply accumulators (MACs). For both methods, the Quartus II software maps the functionality to the DSP blocks in the device during compilation.

### Instantiation Using the MegaWizard Plug-In Manager

You can use the MegaWizard Plug-In Manager (Tools menu) in the Quartus II software to create custom variations of the `lpm_mult`, `altmult_add`, and `altmult_accum` megafunctions. The wizard interface provides an easy way for you to specify parameters or use optional ports. The wizard generates a variety of output files that you can use to include the megafunction variation in your design.

Search for “MegaWizard“ in Quartus II Help for detailed instructions on using the MegaWizard Plug-In Manager.

### Inference Using LeonardoSpectrum or Synplify

The LeonardoSpectrum and Synplify synthesis tools provide inference support for the `lpm_mult`, `altmult_add`, and `altmult_accum` megafunctions. The tools recognize multipliers, multiplier adders, and MACs, infer the appropriate megafunction, and black box the corresponding code when generating synthesized netlists. When you compile the netlists in the Quartus II software, the software maps the megafunction to the Stratix or Stratix GX DSP block.

☞ The FPGA Compiler II software provides some inference support. It can infer `lpm_mult` and implements the functionality in the Stratix or Stratix GX DSP block.

Refer to the following documents for more information on synthesis tool inference support.

- *Application Note 193: Design Guidelines for Using DSP Blocks in the Synplify Software*
- *Application Note 194: Design Guidelines for Using DSP Blocks in the LeonardoSpectrum Software*

## Quartus II DSP Megafunctions

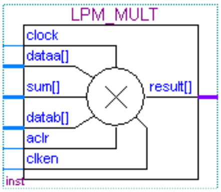
The following sections describe the `lpm_mult`, `altmult_add`, and `altmult_accum` megafunctions that Altera provides with the Quartus II software. Each section includes the megafunction symbol, the input and output ports, a description of the wizard options, example wizard screen shots, and an example inference.

Refer to the Quartus II Help for the megafunction parameters.

### lpm_mult

You can implement this megafunction to use the DSP block in simple multiplier mode. Figure 6–16 shows the `lpm_mult` symbol.

*Figure 6–16. lpm_mult Symbol*



If you want to use features of the DSP block that are not accessible using `lpm_mult`, e.g., multiplier operand sign signals, input registers, or output registers, you can use `altmult_add` as a single multiplier (i.e., specify 1 as the number of multipliers).

With `lpm_mult`, the input registers cannot be used to create shift registers.

### *lpm_mult Input Ports*

Table 6–6 shows the input ports for the `lpm_mult` megafunction.

***Table 6–6. lpm_mult Input Ports***

| Name | Required | Description |
|---|---|---|
| `dataa[]` | Yes | Multiplicand. This port is `LPM_WIDTHA` wide. |
| `datab[]` | Yes | Multiplier. This port is `LPM_WIDTHB` wide. |
| `sum[]` | No | Partial sum. This port is `LPM_WIDTHS` wide. The `sum` input is added to the multiplier output outside of the DSP block. |
| `clock` | No | Clock for pipelined usage. The clock port provides pipelined operation for the `lpm_mult` function. For `LPM_PIPELINE` values other than 0 (default value), the clock port must be connected. |
| `clken` | No | Clock enable for pipelined usage. If omitted, the default is 1 (i.e., always enabled). |
| `aclr` | No | Asynchronous clear for pipelined usage. When `lpm_mult` is implemented in the DSP block, the pipeline initializes to 0; if implemented in LEs, it initializes to an undefined (X) logic level. The `aclr` port can be used at any time to reset the pipeline to all 0s, asynchronously to the clock signal. |

### *lpm_mult Output Ports*

Table 6–7 shows the output ports for the `lpm_mult` megafunction.

***Table 6–7. lpm_mult Output Ports***

| Name | Required | Description |
|---|---|---|
| `result[]` | Yes | `result = dataa[] × datab[] + sum[]`. The product least significant bit (LSB) is aligned with the sum LSB. This port is `LPM_WIDTHP` wide. If `LPM_WIDTHP` < max(`LPM_WIDTHA` + `LPM_WIDTHB`, `LPM_WIDTHS`) or (`LPM_WIDTHA` + `LPM_WIDTHS`), only the `LPM_WIDTHP` most significant bits (MSBs) are present. |

### *lpm_mult Customization*

You can use the MegaWizard Plug-In Manager to customize the `lpm_mult` megafunction to specify a multiplier in a design. Table 6–8 describes customization options available in the wizard.

Search for “lpm_mult“ in the Quartus II Help for a listing of the parameters that you can use when implementing the megafunction in an HDL instead of using the wizard.

***Table 6–8. lpm_mult Customization (Part 1 of 2)***

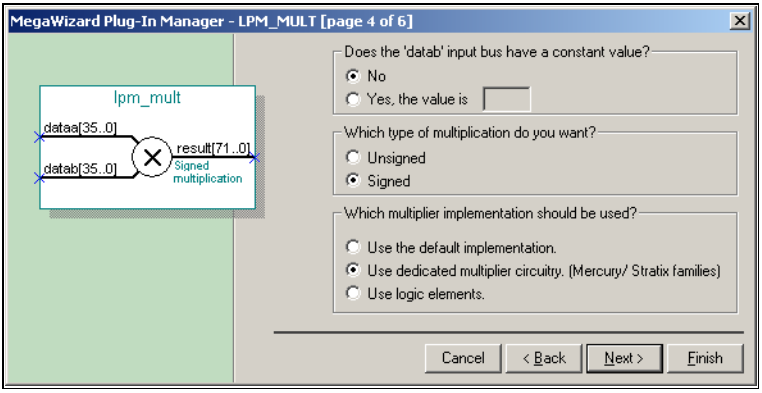
| Function | Description |
|---|---|
| Data Input Bus | Select the widths of the multiplier and the multiplicand. The maximum size for implementation in DSP blocks is 36 × 36. The Quartus II software implements multipliers with operand widths greater than 36 bits in multiple DSP blocks and automatically adds the logic needed to link the DSP blocks. |
| Sum Input Bus | Use the `sum[]` port to add the value of a bus to the multiplier result. The Quartus II software implements the adder using logic cells. Refer to “altmult_add” on page 6–33 to implement two multipliers and an adder in the DSP block. |
| Result Output Bus | Specify the width of the result port or let the wizard calculate it automatically. If you restrict the output width, you lose the least significant result bits. |
| Constant Multiplication | Specify whether one of the multiplier operands is a constant and give its value. This option helps the Quartus II software decide how to implement the megafunction if you choose a default multiplier implementation. For example, the software may place the multiplier in logic elements (LEs) for better resource usage. Additionally, this setting is useful if `lpm_mult` is implemented in LEs. |
| Signed or Unsigned Multiplication | Choose signed or unsigned multiplication. To control the operand signs dynamically, use the `altmult_add` megafunction, which has sign signals for each operand. |
| Multiplier Implementation | Specify whether to implement the megafunction in dedicated multiplier circuitry (e.g., in the DSP block), LEs, or let the Quartus II software choose the implementation (default). If the Quartus II software chooses the implementation, it picks DSP blocks or LEs based on the width of the multiplier, whether an operand is a constant, and other options you specify. For example, implementing a 2 × 2 multiplier in LEs is more efficient than using a DSP block. |
| Pipelining | Specify the multiplier latency. The DSP block includes 1 stage of pipeline registers and registers for both input and output stages. For a latency of 3, all three sets of registers are used. For a latency of 1, input registers are used. For a latency of 2, input and pipeline registers are used. Latency higher than 3 requires LE registers, which are external to the DSP block and add latency without improving performance. You can add optional asynchronous clear and clock enable signals. Pipelining improves the performance of 36 × 36 multipliers. For 18 × 18 multipliers and smaller, pipelining adds latency but does not improve performance.<br>To implement multipliers with a latency of 1 using the output registers, use `altmult_add` instead of `lpm_mult`. See “altmult_add” on page 6–33.<br>A 36 × 36 multiplier uses the multiplier stage as well as the adder/output block of the DSP block. Therefore, you may want to use a latency of 3 with LPM_MULT or instead use `altmult_add` to control use of the input, pipeline, or output registers. See “altmult_add” on page 6–33. |

*Table 6–8. lpm_mult Customization (Part 2 of 2)*

| Function | Description |
|---|---|
| Optimization | Specify the type of optimization if you want to implement the multiplier in LEs; this option does not apply to the DSP block. If, however, you use the default multiplier implementation option, the optimization setting can influence whether the Quartus II software uses DSP blocks or LEs to implement the megafunction. |
| Output Files | The last wizard page shows the files that the MegaWizard Plug-In Manager will create. The MegaWizard Plug-In Manager generates wrapper files for `lpm_mult` in Verilog HDL or VHDL, and a Quartus II Symbol File (**.bsf**). |

Figure 6–17 shows an example `lpm_mult` wizard page.

*Figure 6–17. lpm_mult Example Wizard Page*



MegaWizard Plug-In Manager - LPM_MULT [page 4 of 6]

Does the 'datab' input bus have a constant value?
● No
○ Yes, the value is

Which type of multiplication do you want?
○ Unsigned
● Signed

Which multiplier implementation should be used?
○ Use the default implementation.
● Use dedicated multiplier circuitry. (Mercury/ Stratix families)
○ Use logic elements.

### lpm_mult HDL Inference

The following shows example Verilog HDL code that infers an 18-bit multiplier with registered inputs and outputs and an asynchronous clear.

```
reg [17:0] reg_ina, reg_inb;
wire dataout;
reg [35:0] reg_dataout;
...
assign dataout = reg_dataout;

always @ (posedge clk or posedge aclr)
begin
    if (aclr)
        reg_dataout = 0;
    else if (clkena)
```

```
        begin
            reg_ina <= ina;
            reg_inb <= inb;
            reg_dataout = reg_ina * reg_inb;
        end
end
```

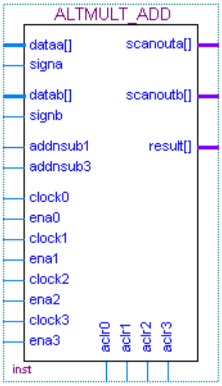
## altmult_add

You can use this megafunction to implement multiplication with addition/subtraction. Implement this megafunction to use the DSP block in two-multiplier adder or four-multiplier adder mode (e.g., FIR filters). Behaviorally, the megafunction consists of two or more multipliers feeding a parallel adder. A maximum of four 18-bit or eight 9-bit multipliers fit in a single DSP block.

☞ You can use `altmult_add` as a single multiplier (i.e., specify 1 as the number of multipliers) if you want to use features of the DSP block that are not accessible using `lpm_mult`, e.g., multiplier operand sign signals.

Figure 6–18 shows the `altmult_add` symbol.

*Figure 6–18. altmult_add Symbol*



### altmult_add Input Ports

Table 6–9 shows the input ports for the `altmult_add` function.

**Table 6–9. altmult_add Input Ports**

| Name | Required | Description |
|---|---|---|
| `dataa[]` | Yes | Data input to the multipliers. This port is `[(WIDTH_A × NUMBER_OF_MULTIPLIERS) - 1..0]` wide. |
| `datab[]` | Yes | Data input to the multipliers. This port is `[(WIDTH_B × NUMBER_OF_MULTIPLIERS) - 1..0]` wide. |
| `clock0/1/2/3` | No | Positive-edge-triggered clock inputs to the multiplier. |
| `ena0/1/2/3` | No | Clock enables. `ena0` is for `clock0`, `ena1` is for `clock1`, etc. |
| `aclr0/1/2/3` | No | Asynchronous clear inputs for the DSP block input, output, and pipeline registers. |
| `signa/signb` | No | Specifies the numeric representation of the `dataa[]` and `datab[]` ports. If the port is high, the multiplier treats the input as a signed two's complement number. If the port is low, the multiplier treats the input as an unsigned number. |
| `addnsub1/3` | No | If the `addnsub1/3` port is high, the adder performs an add function. If the `addnsub1/3` port is low, the adder performs a subtract function. |

### altmult_add Output Ports

Table 6–10 shows the output ports for the `altmult_add` function

**Table 6–10. altmult_add Output Ports**

| Name | Required | Description |
|---|---|---|
| `result[]` | Yes | Adder output. This port is `[WIDTH_RESULT - 1..0]` wide. |
| `shiftouta[]`<br>`shiftoutb[]` | No | Outputs of the first and second input shift registers, which consist of the multiplier input registers. These ports are `[WIDTH_A - 1..0]` and `[WIDTH_B - 1..0]` wide, respectively. |

### altmult_add Customization

You can use the MegaWizard Plug-In Manager to customize the `altmult_add` megafunction for a multiplier with an adder/subtractor. Table 6–11 describes customization options available in the MegaWizard Plug-In Manager.

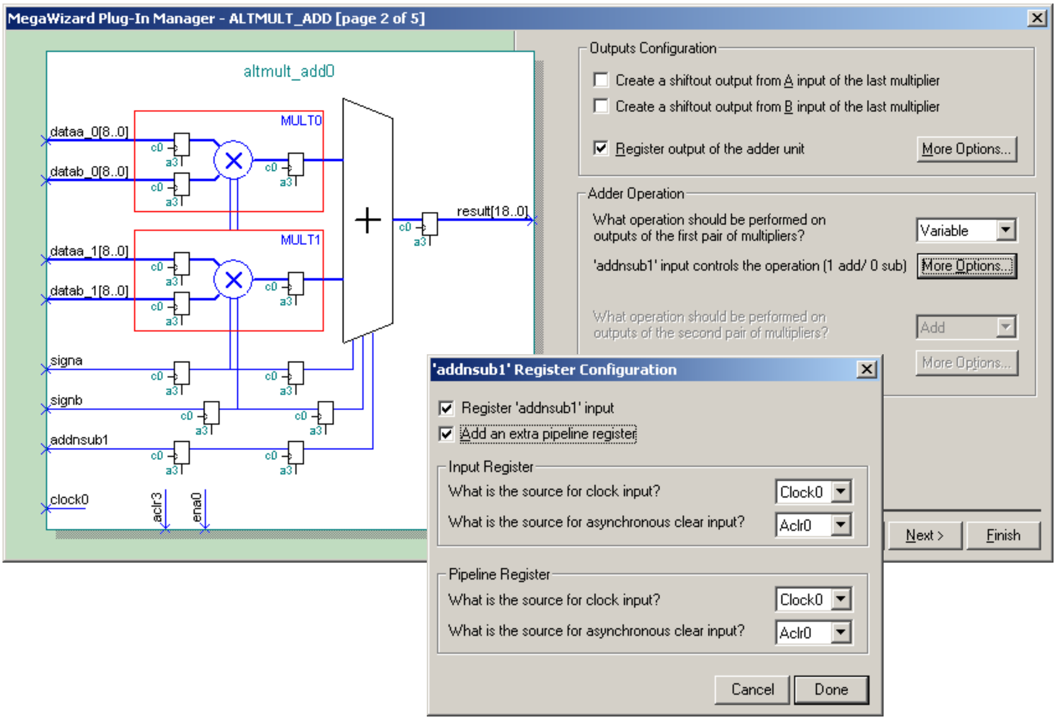
Search for "altmult_add" in Quartus II Help for a listing of the parameters that you can use when implementing the megafunction in an HDL instead of using the wizard.

*Table 6–11. altmult_add Customization*

| Function | Description |
|---|---|
| General Configuration | Specify the number of multipliers and whether the multipliers have the same configuration, e.g, they have the same operands registered, the operands use the same clock and clear signals, and the pipeline registers have the same configuration.<br>The multiplier output widths must be the same. Therefore, all multiplicands (operand A) have the same widths and all multipliers (operand B) have the same widths. However, operands A and B can be different widths. Because each DSP block contains four 18-bit multipliers, you can specify a maximum of 8 multipliers with 9-bit operands or 4 multipliers with up to 18-bit operands. You can also add clock enable and asynchronous clear signals. |
| Input Representation | Specify whether the operands are signed, unsigned, or variable. |
| `signa/b` Register Configuration | If you choose variable operand input representation, you can specify additional options by clicking **More Options**. For example, you can specify whether the input is registered or pipelined, and the clock and asynchronous clear source. |
| Adder Block Outputs | You can indicate whether to use a shift register at the output of each operand of the last multiplier to form a shift register chain spanning multiple DSP blocks. These shift registers are configured using the input registers and are part of the DSP block.<br>You can register the adder block's output, specify control signals, and add additional pipelining. |
| Adder Block Operation | The adder block adds or subtracts the multiplier outputs or can dynamically perform either operation (i.e., variable). Variable operation uses the `addnsub1/3` signal(s), which you can register and pipeline by clicking **More Options**. |
| Multiplier Input Configuration | Specify whether to register one or both multiplier inputs. If you register them, click **More Options** to set control signals. For the second and subsequent multipliers in the DSP block, you can feed the multiplier with a multiplier input or by the output of the previous multiplier's input register, i.e., the shift-in input. You use the shift-in input for FIR filter applications such as a 4-tap 18-bit FIR filter implemented within a single DSP block.<br>Refer to Figure 6–4 on page 6–7 for the structure of the DSP block shift register chain. |
| Multiplier Output Configuration | You can register the multiplier output before it feeds the adder block by using the DSP block's pipeline register. click **More Options** to set control signals. |
| Output Files | The last wizard page shows the files that the MegaWizard Plug-In Manager will create. The MegaWizard Plug-In Manager generates wrapper files for `altmult_add` in Verilog HDL or VHDL, and a Quartus II Symbol File (**.bsf**). |

Figure 6–19 shows an example page of the `altmult_add` wizard.

*Figure 6–19. altmult_add Example Wizard Page*



MegaWizard Plug-In Manager - ALTMULT_ADD [page 2 of 5]

Outputs Configuration

☐ Create a shiftout output from A input of the last multiplier

☐ Create a shiftout output from B input of the last multiplier

☑ Register output of the adder unit — More Options...

Adder Operation

What operation should be performed on outputs of the first pair of multipliers? Variable

'addnsub1' input controls the operation (1 add/ 0 sub) — More Options...

What operation should be performed on outputs of the second pair of multipliers? Add — More Options...

'addnsub1' Register Configuration

☑ Register 'addnsub1' input

☑ Add an extra pipeline register

Input Register

What is the source for clock input? Clock0

What is the source for asynchronous clear input? Aclr0

Pipeline Register

What is the source for clock input? Clock0

What is the source for asynchronous clear input? Aclr0

### *altmult_add HDL Inference*

The LeonardoSpectrum and Synplify synthesis tools infer the following types of multiplier adders:

- Multipliers with a first-level adder or subtractor (maps to the two-multiplier adder DSP block mode). These adders or multiplier-adders can have 2 multipliers as inputs.

- Multipliers with a first-level adder or subtractor and a second-level adder (maps to the four-multiplier adder DSP block mode). These adders can have 3 or 4 multipliers as inputs.

The tools infer an `altmult_add` megafunction in the netlist, which the Quartus II software maps to the DSP block during compilation. Additionally, the tools support a pipelining stage between the multipliers and adder. The tools also infer `altmult_add` megafunctions for FIR filters, which use the input shift register chain with the multiplier and adder block.

☞ If, in your HDL code, you add a multiplier output to another bus that is not a multiplier output, the synthesis tools map the functionality to `lpm_mult`, not `altmult_add`, and implement it in logic cells.

The following shows example Verilog HDL code that infers a FIR filter.

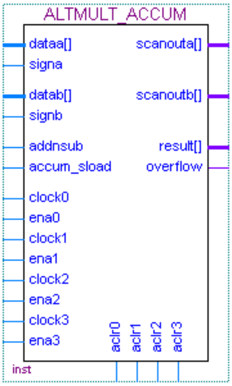
```
module fir_filter (clk, clkena, aclr, data,
coeff_data, result);

// Port Declaration
input clk, clkena, aclr;
input [15:0] data;
input [15:0] coeff_data;
output [33:0] result;

// Register Declaration
reg [15:0] data_reg0;
reg [15:0] coeff_reg0;

reg [15:0] data_reg1;
reg [15:0] coeff_reg1;

reg [15:0] data_reg2;
reg [15:0] coeff_reg2;

reg [15:0] data_reg3;
reg [15:0] coeff_reg3;

// Wire Declaration
wire [31:0] mult0_result;
wire [31:0] mult1_result;
wire [31:0] mult2_result;
wire [31:0] mult3_result;

// Implementation
// Each assignment fits into one of the
// 4 multipliers in a DSP block
assign mult0_result = data_reg0 * coeff_reg0;
assign mult1_result = data_reg1 * coeff_reg1;
assign mult2_result = data_reg2 * coeff_reg2;
assign mult3_result = data_reg3 * coeff_reg3;
```

```
// This adder fits into the two-level adder in a
// DSP block
assign result = mult0_result + mult1_result +
mult2_result + mult3_result;

always @(posedge clk or posedge aclr)
begin
   if (aclr)
      begin
         data_reg0 <= 0;
         coeff_reg0 <= 0;

         data_reg1 <= 0;
         coeff_reg1 <= 0;

         data_reg2 <= 0;
         coeff_reg2 <= 0;

         data_reg3 <= 0;
         coeff_reg3 <= 0;
      end
   else if (clkena)
      begin
         // Shift register chain:
         // Output of one input register feeds the
         // input of the next input register
         data_reg0 <= data;
         coeff_reg0 <= coeff_data;

         data_reg1 <= data_reg0;
         coeff_reg1 <= coeff_reg0;

         data_reg2 <= data_reg1;
         coeff_reg2 <= coeff_reg1;

         data_reg3 <= data_reg2;
         coeff_reg3 <= coeff_reg2;
      end
end
endmodule
```

## altmult_accum

You can use this megafunction to implement MACs. Behaviorally, the megafunction consists of a single multiplier feeding an accumulator. You can specify widths and register options, and if the widths exceed those that a single DSP block supports, the megafunction adds logic as needed. Figure 6–20 shows the symbol for an 18-bit MAC created using the `altmult_accum` megafunction.

***Figure 6–20. altmult_accum Symbol for 18-Bit MAC***



### *altmult_accum Input Ports*

Table 6–12 shows the input ports for the `altmult_accum` function.

***Table 6–12. altmult_accum Input Ports***

| Name | Required | Description |
|---|---|---|
| `dataa[]` | Yes | Data input to the multiplier. This port is `[WIDTH_A - 1..0]` wide. |
| `datab[]` | Yes | Data input to the multiplier. This port is `[WIDTH_B - 1..0]` wide. |
| `clock0/1/2/3` | Yes | Positive-edge-triggered clock inputs to the multiplier and output register. |
| `ena0/1/2/3` | No | Clock enables. `ena0` is for `clock0`, `ena1` is for `clock1`, etc. |
| `aclr0/1/2/3` | No | Asynchronous clear inputs for the DSP block input, output, and pipeline registers. |
| `signa/signb` | No | Specifies the numeric representation of the `dataa[]` and `datab[]` ports. If the port is high, the multiplier treats the input as a signed two's complement number. If the port is low, the multiplier treats the input as an unsigned number. |
| `addnsub` | No | If the `addnsub` port is high, the adder performs an add function. If the `addnsub` port is low, the adder performs a subtract function. |
| `accum_sload` | No | If the accumulator is adding and the `accum_sload` port is high, then the multiplier output is synchronously loaded into the accumulator. If the accumulator is subtracting, then the opposite (negative value) of the multiplier output is loaded into the accumulator. |

### *altmult_accum Output Ports*

Table 6–13 shows the output ports for the `altmult_accum` function.

**Table 6–13. altmult_accum Output Ports**

| Name | Required | Description |
|---|---|---|
| `result[]` | Yes | Multiplier output port. This port is `[WIDTH_RESULT - 1..0]` wide. |
| `shiftouta[]`<br>`shiftoutb[]` | No | Outputs of the first and second shift register chains, which consist of the multiplier input registers. These ports are `[WIDTH_A - 1..0]` and `[WIDTH_B - 1..0]` wide, respectively. |
| `overflow` | No | Overflow or underflow flag for the accumulator. |

### *altmult_accum Customization*

You can use the MegaWizard Plug-In Manager to customize the `altmult_accum` megafunction for a MAC function. Table 6–14 describes customization options available in the wizard.

Search for "altmult_accum" in the Quartus II Help for a listing of the parameters that you can use when implementing the megafunction in an HDL instead of using the wizard.

**Table 6–14. altmult_accum Customization (Part 1 of 2)**

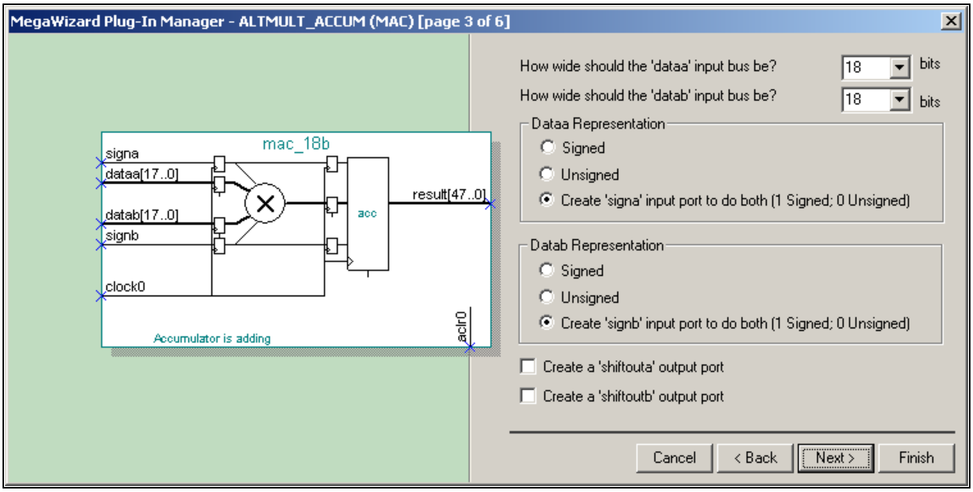
| Function | Description |
|---|---|
| Input Data | Specify the input widths and whether they are signed, unsigned, or both (i.e., variable). |
| Shift Register Output | You can use the input registers as shift registers, e.g., for FIR filter applications by enabling the `shiftouta` and `shiftoutb` ports. Refer to Figure 6–4 on page 6–7 for the structure of the DSP block shift register chain. |
| Output Bus | Choose the accumulator output bit width. Each accumulator output of a single DSP block can be up to 52-bits wide when multiplying operands up to 18 bits (36-bit output) and using a 52-bit accumulator. Therefore, the DSP block can perform up to 65,536 ($2^{16}$) MAC operations for an 18-bit multiplier before an overflow occurs. If you choose a larger multiplier or accumulator width, the Quartus II software implements the accumulator in LEs. |
| Accumulator Direction | Choose to add, subtract, or both (i.e., variable) to add/subtract the multiplier result to/from the output register feedback. |
| Accumulator Loading | Each of the two accumulators in a DSP block has the `accum_sload` input, which can clear the feedback path from the accumulator output back into the input of the add/subtract/accumulate unit. Then, the accumulator synchronously loads the multiplier result output. You can only load the result of the multiplier feeding the accumulator into the accumulator, not a constant value. You can register and pipeline `accum_sload` independently within the DSP block. |

*Table 6–14. altmult_accum Customization (Part 2 of 2)*

| Function | Description |
|---|---|
| Overflow | This output port flags an overflow if the accumulation output is larger than the 52-bit output width. It is an underflow if the accumulator sum is negative. |
| Clocking Method | You can clock the operand input registers and the pipeline registers with any of the 4 DSP block-wide clocks. |
| Latency | You can register the multiplier output before it reaches the accumulator input to add latency and further improve the MAC operation speed. Because the DSP block has only one pipeline stage between the multiplier and the add/subtract/accumulate block, if you specify a latency greater than 1 clock cycle, the Quartus II software implements the accumulator in LEs. In MAC mode, the accumulator block output is always registered. You can use LE registers after the DSP block output if you want extra latency for the accumulator. |
| MAC Control Signals | You can choose which clocks register the megafunction's ports. Additionally, you can use a clock enable with each clock and an asynchronous clear for the registers. If you use an asynchronous clear for the registers, click **More Options** to choose one of 4 DSP block-wide clear signals for each of the registered ports. |
| Output Files | The last wizard page shows the files that the MegaWizard Plug-In Manager will create. The MegaWizard Plug-In Manager generates wrapper files for `altmult_accum` in Verilog HDL or VHDL, and a Quartus II Symbol File (**.bsf**). |

Figure 6–21 shows an example page of the `altmult_accum` wizard.

*Figure 6–21. altmult_accum Example Wizard Page*



MegaWizard Plug-In Manager - ALTMULT_ACCUM (MAC) [page 3 of 6]

How wide should the 'dataa' input bus be? 18 bits

How wide should the 'datab' input bus be? 18 bits

Dataa Representation
○ Signed
○ Unsigned
● Create 'signa' input port to do both (1 Signed; 0 Unsigned)

Datab Representation
○ Signed
○ Unsigned
● Create 'signb' input port to do both (1 Signed; 0 Unsigned)

☐ Create a 'shiftouta' output port
☐ Create a 'shiftoutb' output port

### *altmult_accum HDL Inference*

The LeonardoSpectrum and Synplify synthesis tools infer a MAC when the design adds a multiplier output and the registered output of the adder block and map it to the `altmult_accum` megafunction.

The tools also support clock enables and asynchronous clears on all registers. Different clocks can clock the input registers, the accumulator register, and the pipeline registers.

The following shows example Verilog HDL code that infers a pipelined MAC.

```
module mult_acc_pipeline (dataout, dataax, dataay,
clk);
    output [16:0] dataout;
    input [7:0] dataax, dataay;
    input clk;
    reg  [16:0] dataout;

    wire [15:0] multa = dataax * dataay;
    wire [16:0] adder_out;
    reg  [15:0] multout;
    assign adder_out = multout + dataout;

    always @(posedge clk)
    begin
        multout <= multa;
        dataout <= adder_out;
    end
endmodule
```

## Conclusion

The Stratix and Stratix GX device DSP blocks are optimized to support DSP applications that need high data throughput, such as FIR filters, FFT functions, and encoders. These DSP blocks are flexible and can be configured in one of four operational modes to suit any application need. The DSP block's adder/subtractor/accumulator and the summation blocks minimize the amount of logic resources used and provide efficient routing. This efficiency results in improved performance and data throughput for DSP applications. The Quartus II software, together with the LeonardoSpectrum and Synplify software, provides a complete and easy-to-use flow for implementing functionality in the DSP block.

# 7. Implementing High-Performance DSP Functions in Stratix & Stratix GX Devices

S52007-1.0

Chapter 7, Implementing High-Performance DSP Functions in Stratix & Stratix GX Devices replaces *AN 215: Implementing High-Performance DSP Functions in Stratix & Stratix GX Devices*.

## Introduction

Digital signal processing (DSP) is a rapidly advancing field. With products increasing in complexity, designers face the challenge of selecting a solution with both flexibility and high performance that can meet fast time-to-market requirements. DSP processors offer flexibility, but they lack real-time performance, while application-specific standard products (ASSPs) and application-specific integrated circuits (ASICs) offer performance, but they are inflexible. Only programmable logic devices (PLDs) offer both flexibility and high performance to meet advanced design challenges.

The mathematical theory underlying basic DSP building blocks—such as the finite impulse response (FIR) filter, infinite impulse response (IIR) filter, fast fourier transform (FFT), and direct cosine transform (DCT)—is computationally intensive. Altera® Stratix™ and Stratix GX devices feature dedicated DSP blocks optimized for implementing arithmetic operations, such as multiply, multiply-add, and multiply-accumulate.

In addition to DSP blocks, Stratix and Stratix GX devices have TriMatrix™ embedded memory blocks that feature various sizes that can be used for data buffering, which is important for most DSP applications. These dedicated hardware features make Stratix and Stratix GX devices an ideal DSP solution.

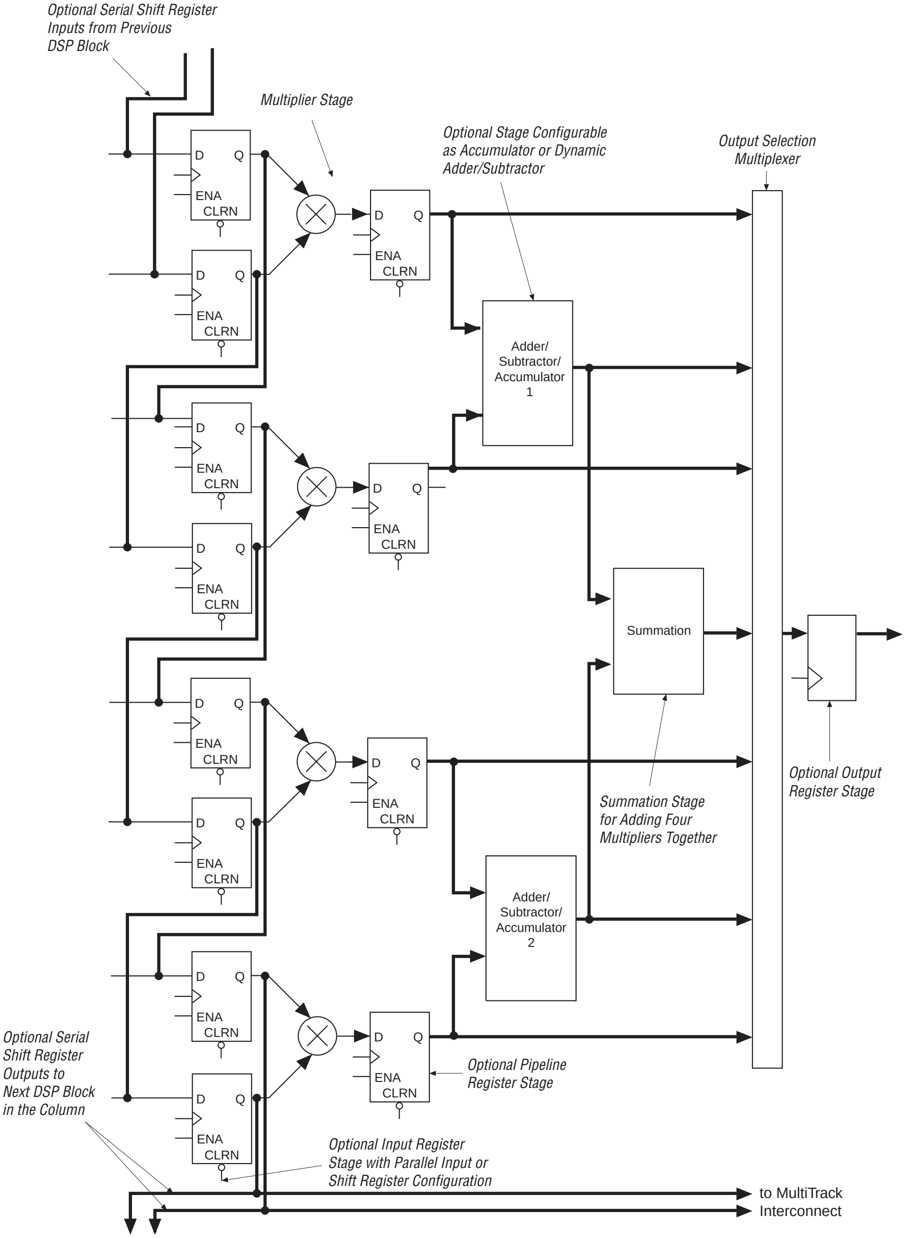
This application note describes the implementation of high performance DSP functions, including filters, transforms, and arithmetic functions, using Stratix and Stratix GX DSP blocks. The following topics are discussed:

- FIR filters
- IIR filters
- Matrix manipulation
- Discrete Cosine Transform
- Arithmetic functions

## Stratix & Stratix GX DSP Block Overview

Stratix and Stratix GX devices feature DSP blocks that can efficiently implement DSP functions, including multiply, multiply-add, and multiply-accumulate. The DSP blocks also have three built-in registers sets: the input registers, the pipeline registers at the multiplier output, and the output registers. Figure 7–1 shows the DSP block operating in the 18 × 18-bit mode.

*Figure 7–1. DSP Block Diagram for 18 x 18-bit Mode*



The DSP blocks are organized into columns enabling efficient horizontal communication with adjacent TriMatrix memory blocks. Tables 7–1 and 7–2 show the DSP block resources in Stratix and Stratix GX devices, respectively.

*Table 7–1. DSP Block Resources in Stratix Devices*

| Device | DSP Blocks | Maximum 9 × 9 Multipliers | Maximum 18 × 18 Multipliers | Maximum 36 × 36 Multipliers |
|---|---|---|---|---|
| EP1S10 | 6 | 48 | 24 | 6 |
| EP1S20 | 10 | 80 | 40 | 10 |
| EP1S25 | 10 | 80 | 40 | 10 |
| EP1S30 | 12 | 96 | 48 | 12 |
| EP1S40 | 14 | 112 | 56 | 14 |
| EP1S60 | 18 | 144 | 72 | 18 |
| EP1S80 | 22 | 176 | 88 | 22 |

*Table 7–2. DSP Block Resources in Stratix GX Devices*

| Device | DSP Blocks | Maximum 9 × 9 Multipliers | Maximum 18 × 18 Multipliers | Maximum 36 × 36 Multipliers |
|---|---|---|---|---|
| EP1SGX10C | 6 | 48 | 24 | 6 |
| EP1SGX10D | 6 | 48 | 24 | 6 |
| EP1SGX25C | 10 | 80 | 40 | 10 |
| EP1SGX25D | 10 | 80 | 40 | 10 |
| EP1SGX25F | 10 | 80 | 40 | 10 |
| EP1SGX40D | 14 | 112 | 56 | 14 |
| EP1SGX40G | 14 | 112 | 56 | 14 |

Each DSP block supports either eight 9 × 9-bit multipliers, four 18-bit multipliers, or one 36 × 36-bit multiplier. These multipliers can feed an adder or an accumulator unit based on the operation mode. Table 7–3 shows the different operation modes for the DSP blocks.

*Table 7–3. Operation Modes for DSP Blocks*

| DSP Block Mode | Number & Size of Multipliers per DSP Block | | |
|---|---|---|---|
| | 9 x 9-bit | 18 x 18-bit | 36 x 36-bit |
| Simple multiplier | Eight multipliers with eight product outputs | Four multipliers with four product outputs | One multiplier with one product output |
| Multiply-accumulate | Two multiply and accumulate (34 bit) | Two multiply and accumulate (52 bit) | |
| Two-multipliers adder | 4 two-multipliers adders | 2 two-multipliers adders | |
| Four-multipliers adder | 2 four-multipliers adder | 1 four-multipliers adder | |

Implementing multipliers, multiply-adders, and multiply-accumulators in the DSP blocks has a performance advantage over logic cell implementation. Using DSP blocks also reduces logic cell and routing resource consumption. To achieve higher performance, register each stage of the DSP block to allow pipelining. For implementing applications, such as FIR filters, efficiently use the input registers of the DSP block as shift registers.

For more information on DSP blocks, refer to Chapter 6, Using the DSP Blocks in Stratix & Stratix GX Devices.

## TriMatrix Memory Overview

Stratix and Stratix GX devices feature the TriMatrix memory structure, composed of three sizes of embedded RAM blocks. These include the 512-bit size M512 block, the 4-Kbit size M4K block, and the 512-Kbit size M-RAM block. Each block is configurable to support a wide range of features.

Tables 7–4 and 7–5 show the number of memory blocks in each Stratix and Stratix GX device, respectively.

*Table 7–4. TriMatrix Memory Resources in Stratix Devices (Part 1 of 2)*

| Device | M512 | M4K | M-RAM |
|---|---|---|---|
| EP1S10 | 94 | 60 | 1 |
| EP1S20 | 194 | 82 | 2 |
| EP1S25 | 224 | 138 | 2 |

*Table 7–4. TriMatrix Memory Resources in Stratix Devices (Part 2 of 2)*

| Device | M512 | M4K | M-RAM |
|---|---|---|---|
| EP1S30 | 295 | 171 | 4 |
| EP1S40 | 384 | 183 | 4 |
| EP1S60 | 574 | 292 | 6 |
| EP1S80 | 767 | 364 | 9 |

*Table 7–5. TriMatrix Memory Resources in Stratix GX Devices*

| Device | M512 | M4K | M-RAM |
|---|---|---|---|
| EP1SGX10C | 94 | 60 | 1 |
| EP1SGX10D | 94 | 60 | 1 |
| EP1SGX25C | 224 | 138 | 2 |
| EP1SGX25D | 224 | 138 | 2 |
| EP1SGX25F | 224 | 138 | 2 |
| EP1SGX40D | 384 | 183 | 4 |
| EP1SGX40G | 384 | 183 | 4 |

Most DSP applications require local data storage for intermediate buffering or for filter storage. The TriMatrix memory blocks enable efficient use of available resources for each application.

The M512 and M4K memory blocks can implement shift registers for applications, such as multi-channel filtering, auto-correlation, and cross-correlation functions. Implementing shift registers in embedded memory blocks reduces logic cell and routing resource consumption.

For more information on TriMatrix memory blocks, refer to Chapter 3, Using TriMatrix Embedded Memory Blocks in Stratix & Stratix GX Devices.

## DSP Function Overview

The following sections describe commonly used DSP functions. Each section illustrates the implementation of a basic DSP building block, including FIR and IIR filters, in Stratix and Stratix GX devices using DSP blocks and TriMatrix memory blocks.

# Finite Impulse Response (FIR) Filters

This section describes the basic theory and implementation of basic FIR filters, time-domain multiplexed (TDM) FIR filters, and interpolation and decimation polyphase FIR filters. An introduction to the complex FIR filter is also presented in this section.

## FIR Filter Background

Digital communications systems use FIR filters for a variety of functions, including waveform shaping, anti-aliasing, band selection, decimation/interpolation, and low pass filtering. The basic structure of a FIR filter consists of a series of multiplications followed by an addition.

The following equation represents an FIR filter operation:

$$y(n) = x(n) \otimes h(n)$$

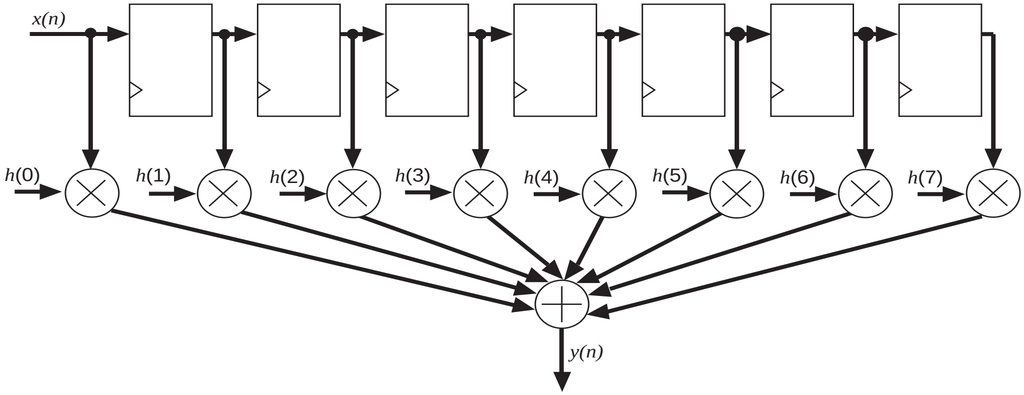
$$y(n) = \sum_{i=0}^{L-1} x(n-i)h(i)$$

where:

$x(n)$ represents the sequence of input samples
$h(n)$ represents the filter coefficients
$L$ is the number of filter taps

A sample FIR filter with $L$=8 is shown in Figure 7–2.

*Figure 7–2. Basic FIR Filter*



This example filter in Figure 7–2 uses the input values at eight different time instants to produce an output. Hence, it is an 8-tap filter. Each register provides a unit sample delay. The delayed inputs are multiplied with their respective filter coefficients and added together to produce the output. The width of the output bus depends on the number of taps and the bit width of the input and coefficients.

## Basic FIR Filter

A basic FIR filter is the simplest FIR filter type. As shown in Figure 7–2, a basic FIR filter has a single input channel and a single output channel.

### *Basic FIR Filter Implementation*

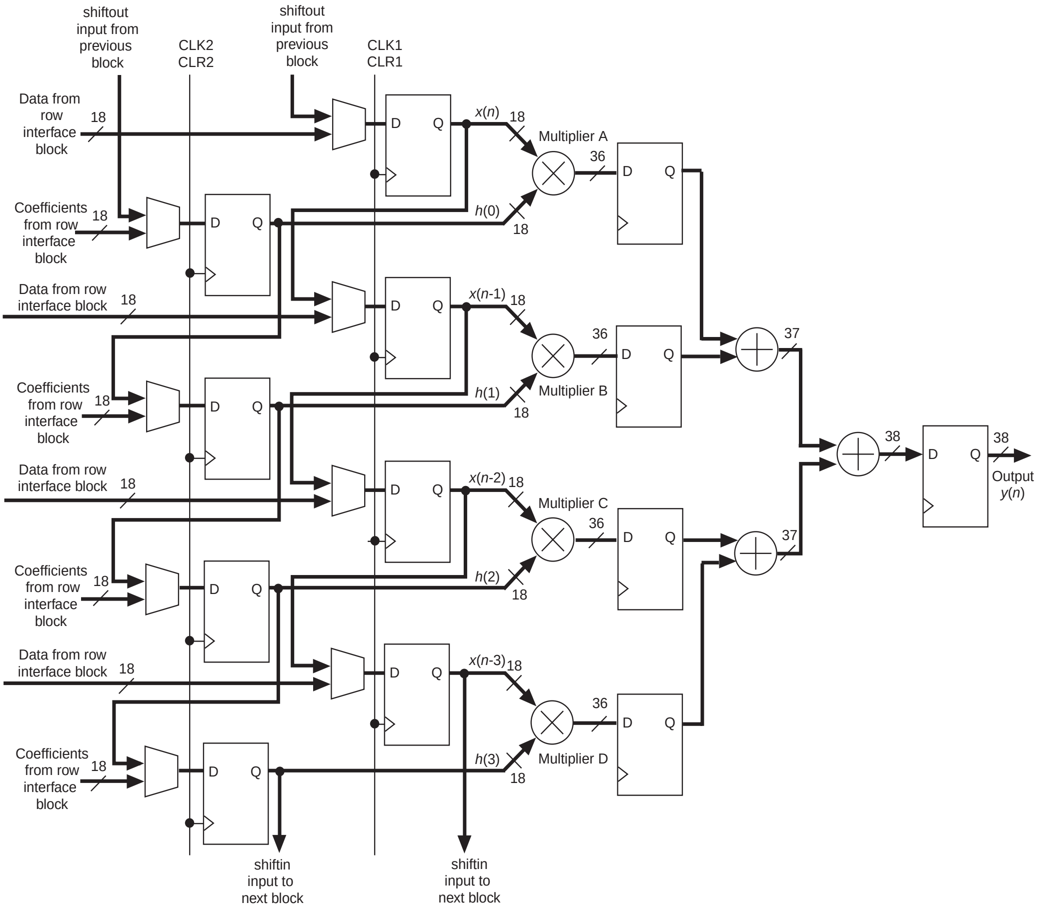
Stratix and Stratix GX devices' dedicated DSP blocks can implement basic FIR filters. Because these DSP blocks have closely integrated multipliers and adders, filters can be implemented with minimal routing resources and delays. For implementing FIR filters, the DSP blocks are configured in the four-multipliers adder mode.

See Chapter 6, Using the DSP Blocks in Stratix & Stratix GX Devices for more information on the different modes of the DSP blocks.

This section describes the implementation of an 18-bit 8-tap FIR filter. Because Stratix and Stratix GX devices support modularity, cascading two 4-tap filters can implement an 8-tap filter. Larger FIR filters can be designed by extending this concept. Users can also increase the number of taps available per DSP block if 18 bits of resolution are not required. For example, by using only 9 bits of resolution for input samples and coefficient values, 8 multipliers are available per DSP block. Therefore, a 9-bit 8-tap filter can be implemented in a single DSP block provided an external adder is implemented in logic cells.

The four-multipliers adder mode, shown in Figure 7–3, provides four 18 × 18-bit multipliers and three adders in a single DSP block. Hence, it can implement a 4-tap filter. The data width of the input and the coefficients is 18 bits, which results in a 38-bit output for a 4-tap filter.

*Figure 7–3. Hardware View of a DSP Block in Four-Multipliers Adder Mode* Notes (1). (2), (3)



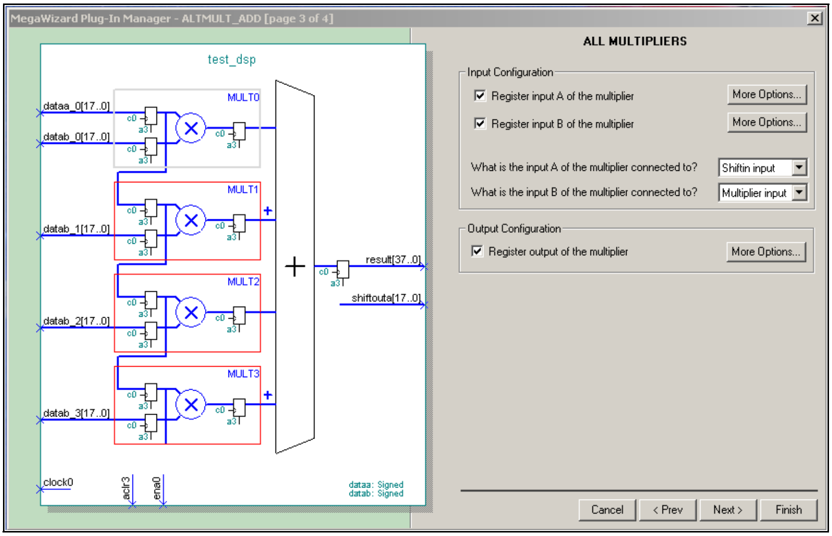
*Notes to Figure 7–3:*

(1) The input registers feed the multiplier blocks. These registers can increase the DSP block performance, but are optional. These registers can also function as shift registers if the dedicated shiftin/shiftout signals are used.

(2) The pipeline registers are fed by the multiplier blocks. These registers can increase the DSP block performance, but are optional.

(3) The output registers register the DSP block output. These registers can increase the DSP block performance, but are optional.

*Figure 7–4. Quartus II Software View of MegaWizard Implementation of a DSP Block in Four-Multipliers Adder Mode*



MegaWizard Plug-In Manager - ALTMULT_ADD [page 3 of 4]

ALL MULTIPLIERS

Input Configuration

☑ Register input A of the multiplier

☑ Register input B of the multiplier

What is the input A of the multiplier connected to? Shiftin input

What is the input B of the multiplier connected to? Multiplier input

Output Configuration

☑ Register output of the multiplier

Each input register of the DSP block provides a shiftout output that connects to the shiftin input of the adjacent input register of the same DSP block. The registers on the boundaries of a DSP block also connect to the registers of adjacent DSP blocks through the use of shiftin/shiftout connections. These connections create register chains spanning multiple DSP blocks, which makes it easy to increase the length of FIR filters. Figure 7–5 shows two DSP blocks connected to create an 8-tap FIR filter. Filters with more taps can be implemented by connecting DSP blocks in a similar manner, provided sufficient DSP blocks are available in the device.

Adding the outputs of the two DSP blocks requires an external adder which can be implemented using logic cells.

The input data can be fed directly or by using the shiftout/shiftin chains, which allow a single input to shift down the register chain inside the DSP block. The input to each of the registers has a multiplexer, hence, the data can be fed either from outside the DSP block or the preceding register. This can be selected from the MegaWizard® in the Quartus® II software, as shown in Figure 7–4. The example in Figure 7–5 uses the shiftout/shiftin flip-flop chains where the multiplexers are configured to use these chains. In this example, the flip-flops inside the DSP blocks serve as the taps of the FIR filter.

When the coefficients are loaded in parallel, they can be fed directly from memory elements or any other muxing scheme. This facilitates the implementation of an adaptive (variable) filter.

Further, if the user wants to implement the shift register chains external to the DSP block, this can be done by using the `altshift_taps` megafunction. In this case, the coefficient and data shifting is done external to the DSP block. The DSP block is only used to implement the multiplications and the additions.

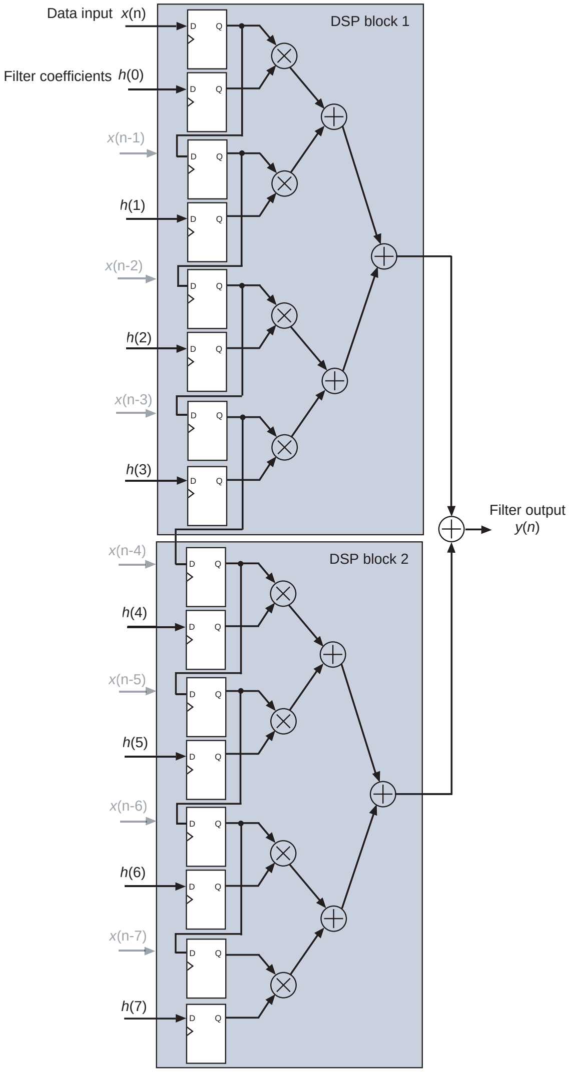
### Parallel vs. Serial Implementation

The fastest implementations are fully parallel, but consume more logic resources than serial implementations. To trade-off performance for logic resources, implement a serial scheme with a specified number of taps. To facilitate this, Altera provides the FIR Compiler core through its MegaCore program. The FIR Compiler is an easy-to-use, fully-integrated graphical user interface (GUI) based FIR filter design software.

For more information on the FIR Compiler MegaCore, visit the Altera web site at www.altera.com and search for “FIR compiler” in the “Intellectual Property” page.

It is important to note that the four-multipliers adder mode allows a DSP block to be configured for parallel or serial input. When it is configured for parallel input, as shown in Figure 7–6, the data input and the coefficients can be loaded directly without the need for shiftin/shiftout chains between adjacent registers in the DSP block. When the DSP block is configured for serial input, as shown in Figure 7–5, the shiftin/shiftout chains create a register cascade both within the DSP block and also between adjacent DSP blocks.

***Figure 7–5. Serial Loading 18-Bit 8-Tap FIR Filter Using Two DSP Blocks*** *Notes (1), (2), (3)*



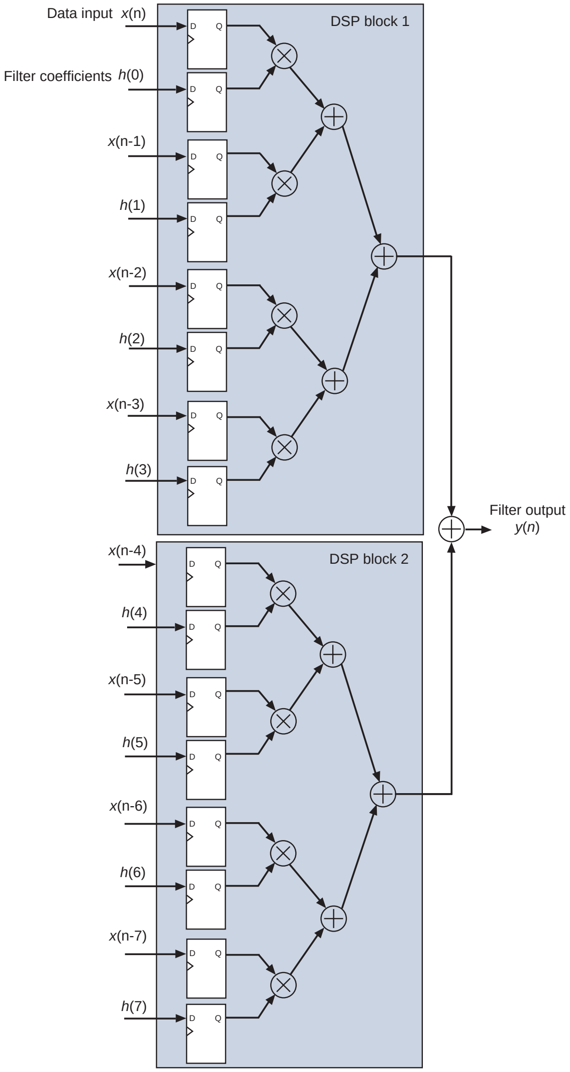
*Notes to Figure 7–5:*

(1) Unused ports grayed out.

(2) The indexing $x(n\text{-}1)$, ..., $x(n\text{-}7)$ refers to the case of parallel loading and should be ignored here. This indexing is retained in this figure for consistency with other figures in this application note.

(3) To increase the DSP block performance, include the pipeline and output registers. Refer to Figure 7–3 for the details.

*Figure 7–6. Parallel Loading 18-Bit 8-Tap FIR Filter Using Two DSP Blocks* *Notes (1), (2)*



*Notes to Figure 7–6:*

(1) The indexing $x(n\text{-}1)$, ..., $x(n\text{-}7)$ refers to the case of parallel loading.

(2) To increase the DSP block performance, include the input, pipeline, and output registers. Refer to Figure 7–3 for the details.

### Basic FIR Filter Implementation Results

Table 7–6 shows the results of the serial implementation of an 18-bit 8 tap FIR filter as shown in Figure 7–5 on page 7–12

Table 7–6. Basic FIR Filter Implementation Results

| Part | EP1S10F780 |
|---|---|
| Utilization | LCELL: 130/10570 (1%)<br>DSP Block 9-bit elements: 16/48 (33%)<br>Memory bits: 288/920448 (<1%) |
| Performance | 247 MHz |

### Basic FIR Filter Design Example

Download the Basic FIR Filter (**base_fir.zip**) design example from the Design Examples section of the Altera web site at www.altera.com**.**

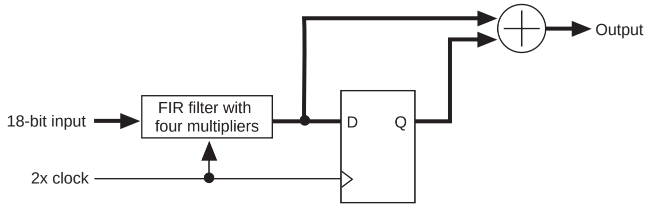
## Time-Domain Multiplexed FIR Filters

A TDM FIR filter is clocked `n`-times faster than the sample rate in order to reuse the same hardware. Consider the 8-tap filter shown in Figure 7–2. The TDM technique can be used with a TDM factor of 2, i.e., `n` = 2, to implement this filter using only four multipliers, provided the filter is clocked two times faster internally.

To understand this concept, consider Figure 7–7 that shows a TDM filter with a TDM factor of 2. A 2×-multiplied clock is required to run the filter. On cycle 0 of the 2× clock, the user loads four coefficients into the four multiplier inputs. The resulting output is stored in a register. On cycle 1 of the 2× clock, the user loads the remaining four coefficients into the multiplier inputs. The output of cycle 1 is added with the output of cycle 0 to create the overall output. See the "TDM Filter Implementation" on page 7–15 section for details on the coefficient loading schedule.

The TDM implementation shown in Figure 7–7 requires only four multipliers to achieve the functionality of an 8-tap filter. Thus, TDM is a good way to save logic resources, provided the multipliers can run at n-times the clock speed. The coefficients can be stored in ROM/RAM, or any other muxing scheme.

Figure 7–7. Block Diagram of 8-Tap FIR Filter with TDM Factor of n=2



### TDM Filter Implementation

TDM FIR filters are implemented in Stratix and Stratix GX devices by configuring the DSP blocks in the multiplier-adder mode. Figure 7–9 shows the implementation of an 8-tap TDM FIR filter (n=2) with 18 bits of data and coefficient inputs. Because the input data needs to be loaded into the DSP block in parallel, a shift register chain is implemented using a combination of logic cells and the altshift_taps function. This shift register is clocked with the same data sample rate (clock 1×). The filter coefficients are stored in ROM and loaded into the DSP block in parallel as well. Because the TDM factor is 2, both the ROM and DSP block are clocked with clock 2×.

Table 7–7. Operation of TDM Filter (Shown in Figure 7–9 on page 7–17)

| Cycle of 2× Clock | Cycle Output | Operation | Overall Output, y(n) |
|---|---|---|---|
| 0 | $y_0 = x(n-1)h(1) + x(n-3)h(3) + x(n-5)h(5) + x(n-7)h(7)$ | Store result | N/A |
| 1 | $y_1 = x(n)h(0) + x(n-2)h(2) + x(n-4)h(4) + x(n-6)h(6)$ | Generate output | $y(n) = y_0 + y_1$ |
| 2 | $y_2 = x(n)h(1) + x(n-2)h(3) + x(n-4)h(5) + x(n-6)h(7)$ | Store result | N/A |
| 3 | $y_3 = x(n+1)h(0) + x(n-1)h(2) + x(n-3)h(4) + x(n-5)h(6)$ | Generate output | $y(n) = y_2 + y_3$ |
| 4 | $y_4 = x(n+1)h(1) + x(n-1)h(3) + x(n-3)h(5) + x(n-5)h(7)$ | Store result | N/A |
| 5 | $y_5 = x(n+2)h(0) + x(n)h(2) + x(n-2)h(4) + x(n-4)h(6)$ | Generate output | $y(n) = y_4 + y_5$ |
| 6 | $y_6 = x(n+2)h(1) + x(n)h(3) + x(n-2)h(5) + x(n-4)h(7)$ | Store result | N/A |
| 7 | $y_7 = x(n+3)h(0) + x(n+1)h(2) + x(n-1)h(4) + x(n-3)h(6)$ | Generate output | $y(n) = y_6 + y_7$ |

Figure 7–8 and Table 7–7 show the coefficient loading schedule. For example, during cycle 0, only the flip-flops corresponding to $h(1)$, $h(3)$, $h(5)$, and $h(7)$ are enabled. This produces the temporary output, $y_0$, which is stored in a flip-flop outside the DSP block. During cycle 1, only the flip-

flops corresponding to *h*(0), *h*(2), *h*(4) and *h*(6) are enabled. This produces the temporary output, $y_1$, which is added to $y_0$ to produce the overall output, $y(n)$. The following shows what the overall output, $y(n)$, equals:

$$y(n) = y_0 + y_1$$

$$\begin{aligned} y(n) = {} & x(0)h(0) + x(n-1)h(1) + x(n-2)h(2) + x(n-3)h(3) \\ & + x(n-4)h(4) + x(n-5)h(5) + x(n-6)h(6) + x(n-7)h(7) \end{aligned}$$

This is identical to the output of the 8-tap filter shown in Figure 7–2. After cycle 1, this process is repeated at every cycle.

***Figure 7–8. Coefficient Loading Schedule in a TDM Filter***

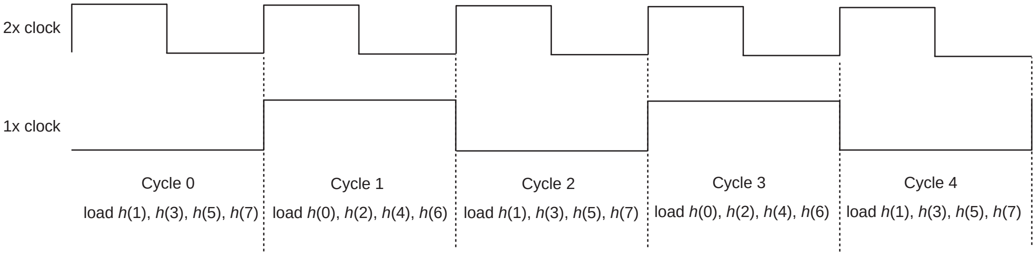
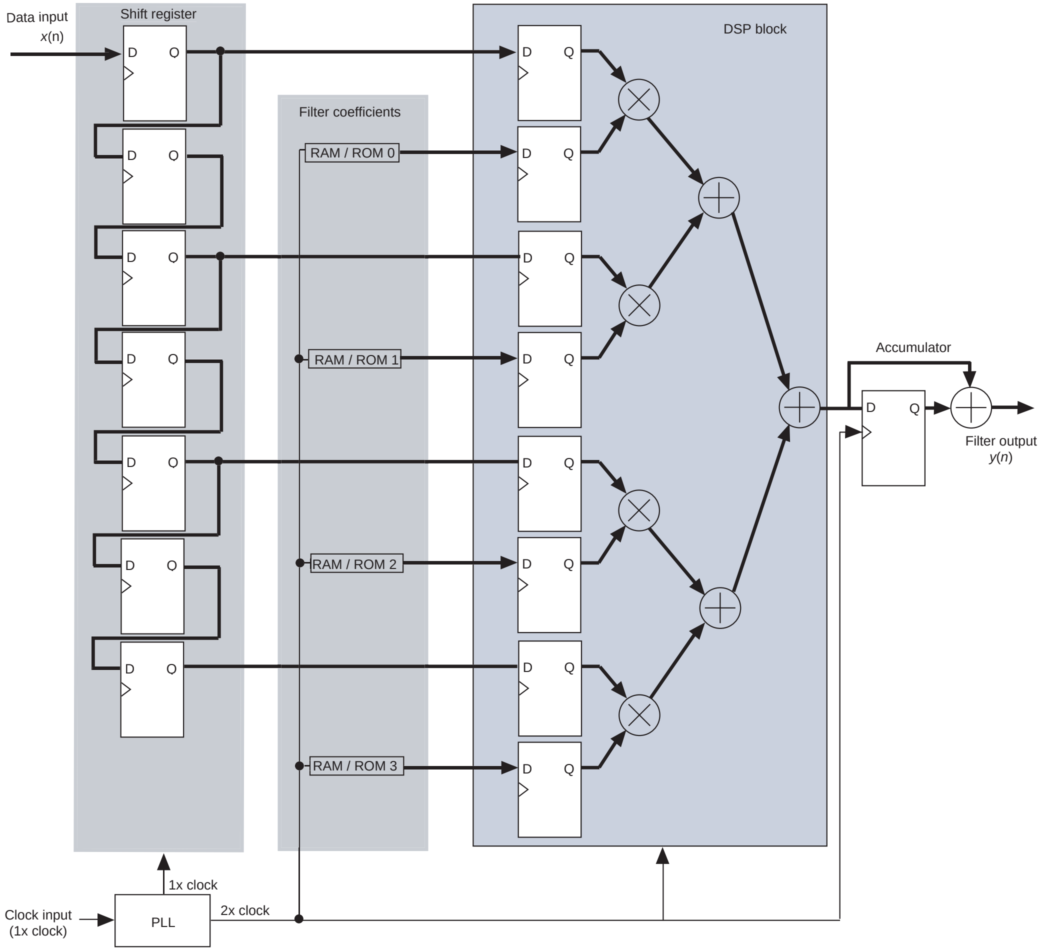


*Figure 7–9. TDM FIR Filter Implementation* Note (1)



*Note to Figure 7–9:*

(1) To increase the DSP block performance, include the pipeline and output registers. Refer to Figure 7–3 on page 7–9 for details.

If the TDM factor is more than 2, then a multiply-accumulator needs to be implemented. This multiply-accumulator can be implemented using the soft logic outside the DSP block if all the multipliers of the DSP block are needed. Alternatively, the multiply-accumulator may be implemented inside the DSP block if all the multipliers of the DSP block are not needed. The accumulator needs to be zeroed at the start of each new sample input. The user also needs a way to store additional sample inputs in memory. For example, consider a sample rate of r and TDM factor of 4. Then, the user needs a way to accept this sample data and send it at a 4r rate to the input of the DSP block. One way to do this is using a first-in-first-out (FIFO) memory with input clocked at rate r and output clocked at rate 4r. The FIFO may be implemented in the TriMatrix memory.

### TDM Filter Implementation Results

Table 7–8 shows the results of the implementation of an 18-bit 8-tap TDM FIR filter as shown in Figure 7–9 on page 7–17.

**Table 7–8. TDM Filter Implementation Results**

| | |
|---|---|
| Part | EP1S10F780 |
| Utilization | Lcell: 196/10570 (1%)<br>DSP Block 9-bit elements: 8/48 (17%)<br>Memory bits: 360/920448 (<1%) |
| Performance | 240 MHz *(1)* |

***Note to Table 7–8:***

(1) This refers to the performance of the DSP blocks. The input and output rate is 120 million samples per second (MSPS), clocked in and out at 120 MHz.

### TDM Filter Design Example

Download the TDM FIR Filter (**tdm_fir.zip**) design example from the Design Examples section of the Altera web site at www.altera.com**.**

## Polyphase FIR Interpolation Filters

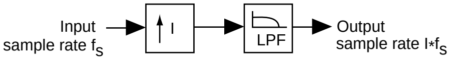
An interpolation filter can be used to increase sample rate. An interpolation filter is efficiently implemented with a polyphase FIR filter. DSP systems frequently use polyphase filters because they simplify overall system design and also reduce the number of computations per cycle required of the hardware. This section first describes interpolation filters and then how to implement them as polyphase filters in Stratix and Stratix GX devices. See the "Polyphase FIR Decimation Filters" on page 7–25 section for a discussion of decimation filters.

### Interpolation Filter Basics

An interpolation filter increases the output sample rate by a factor of `I` through the insertion if `I`-1 zeros between input samples, a process known as zero padding. After the zero padding, the output samples in time domain are separated by $Ts/I = 1/(I \times f_s)$, where $T_s$ and $f_s$ are the sample period and sample frequency of the original signal, respectively. Figure 7–10 shows the concept of signal interpolation.

Inserting zeros between the samples creates reflections of the original spectrum, thus, a low pass filter is needed to filter out the reflections.

*Figure 7–10. Block Diagram Representation of Interpolation*



To see how interpolation filters work, consider the Nyquist Sampling Theorem. This theorem states that the maximum frequency of the input to be sampled must be smaller than $f_s/2$, where $f_s$ is the sampling frequency, to avoid aliasing. This frequency, $f_s/2$, is also known as the Nyquist frequency ($F_n$). Typically, before a signal is sampled using an analog to digital converter (ADC), it needs to be low pass filtered using an analog anti-aliasing filter to prevent aliasing. If the input frequency spectrum extends close to the Nyquist frequency, then the first alias is also close to the Nyquist frequency. Therefore, the low pass filter needs to be very sharp to reject this alias. A very sharp analog filter is hard to design and manufacture and could increase passband ripple, thereby compromising system performance.

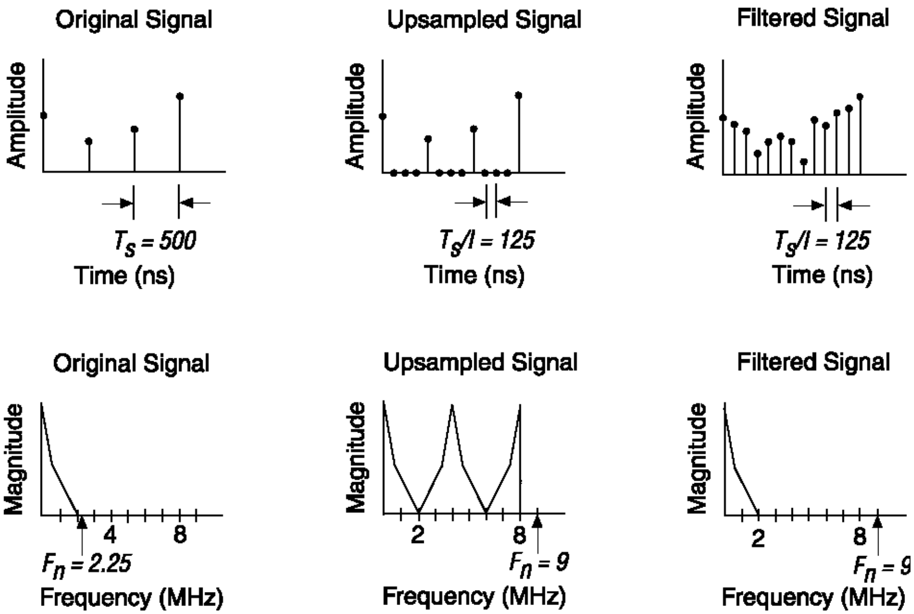
The solution is to increase the sampling rate of the ADC, so that the new Nyquist frequency is higher and the spacing between the desired signal and the alias is also higher. Zero padding as described above increase the sample rate. This process also known as upsampling (oversampling) relaxes the roll off requirements of the anti-aliasing filter. Consequently, a simpler filter achieves alias suppression. A simpler analog filter is easier to implement, does not compromise system performance, and is also easier to manufacture.

Similarly, the digital to analog converter (DAC) typically interpolates the data before the digital to analog conversion. This relaxes the requirement on the analog low pass filter at the output of the DAC.

The interpolation filter does not need to run at the oversampled (upsampled) rate of $f_s \times I$. This is because the extra sample points added are zeros, so they do not contribute to the output.

Figure 7–11 shows the time and frequency domain representation of interpolation for a specific case where the original signal spectrum is limited to 2 MHz and the interpolation factor ($I$) is 4. The Nyquist frequency of the upsampled signal must be greater than 8 MHz, and is chosen to be 9 MHz for this example.

*Figure 7–11. Time & Frequency Domain Representations of Interpolation for I = 4*



As an example, CD players use interpolation, where the nominal sample rate of audio input is 44.1 kilosamples per second. A typical implementation might have an interpolation (oversampling) factor of 4 generating 176.4 kilosamples per second of oversampled data stream.

### Polyphase Interpolation Filters

A direct implementation of an interpolation filter, as shown in Figure 7–10, imposes a high computational burden. For example, if the filter is 16 taps long and a multiplication takes one cycle, then the number of computations required per cycle is 16×`I`. Depending on the interpolation factor (`I`), this number can be quite big and may not be achievable in hardware. A polyphase implementation of the low pass filter can reduce the number of computations required per cycle, often by a large factor, as will be evident later in this section.

The polyphase implementation "splits" the original filter into `I` polyphase filters whose impulse responses are defined by the following equation:

$$h_k(n) = h(k + nI)$$

where:

$k = 0, 1, \ldots, I-1$
$n = 0, 1, \ldots, P-1$
$P = L/I$ = length of polyphase filters
$L$ = length of the filter (selected to be a multiple of $I$)
$I$ = interpolation factor
$h(n)$ = original filter impulse response

This equation implies that the first polyphase filter, $h_0(n)$, has coefficients $h(0)$, $h(I)$, $h(2I)$,..., $h((P-1)I)$. The second polyphase filter, $h_1(n)$, has coefficients $h(1)$, $h(1+I)$, $h(1+2I)$, ..., $h(1+(P-1)I)$. Continuing in this way, the last polyphase filter, $h_{I-1}(n)$, has coefficients $h(I-1)$, $h((I - 1) + N)$, $h((I - 1) + 2I)$, ..., $h((I - 1) + (P-1)I)$.

An example helps in understanding the polyphase implementation of interpolation. Consider the polyphase representation of a 16-tap low pass filter with an interpolation factor of 4. Thus, the output is given below:

$$y(n) = \sum_{i=0}^{15} h(n - iI)x(i)$$

Referring back to Figure 7–11 on page 7–20, the only nonzero samples of the input are $x(0)$, $x(4)$, $x(8,)$ and $x(12)$. The first output, $y(0)$, only depends on $h(0)$, $h(4)$, $h(8)$ and $h(12)$ because $x(i)$ is zero for $i \neq 0, 4, 8, 12$. Table 7–9 shows the coefficients required to generate output samples.

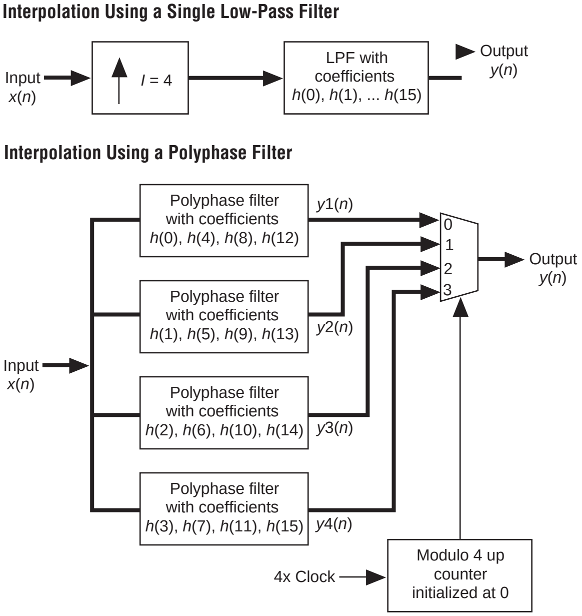
*Table 7–9. Decomposition of a 16-Tap Interpolating Filter into Four Polyphase Filters*

| Output Sample | Coefficients Required | Polyphase Filter Impulse Response |
|---|---|---|
| y(0), y(4)... | h(0), h(4), h(8), h(12) | $h_0(n)$ |
| y(1), y(5)... | h(1), h(5), h(9), h(13) | $h_1(n)$ |
| y(2), y(6)... | h(2), h(6), h(10), h(14) | $h_2(n)$ |
| y(3), y(7)... | h(3), h(7), h(11), h(15) | $h_3(n)$ |

Table 7–9 shows that this filter operation can be represented by four parallel polyphase filters. This is shown in Figure 7–12. The outputs from the filters are multiplexed to generate the overall output. The multiplexer is controlled by a counter, which counts up modulo-`I` starting at `0`.

It is illuminating to compare the computational requirements of the direct implementation versus polyphase implementation of the low pass filter. In the direct implementation, the number of computations per cycle required is 16 × `I` = 16 × 4 = 64. In the polyphase implementation, the number of computations per cycle required is 4 × 4 = 16. This is because there are four polyphase filters, each with four taps.

*Figure 7–12. Polyphase Representation of I=4 Interpolation Filter*



### *Polyphase Interpolation Filter Implementation*

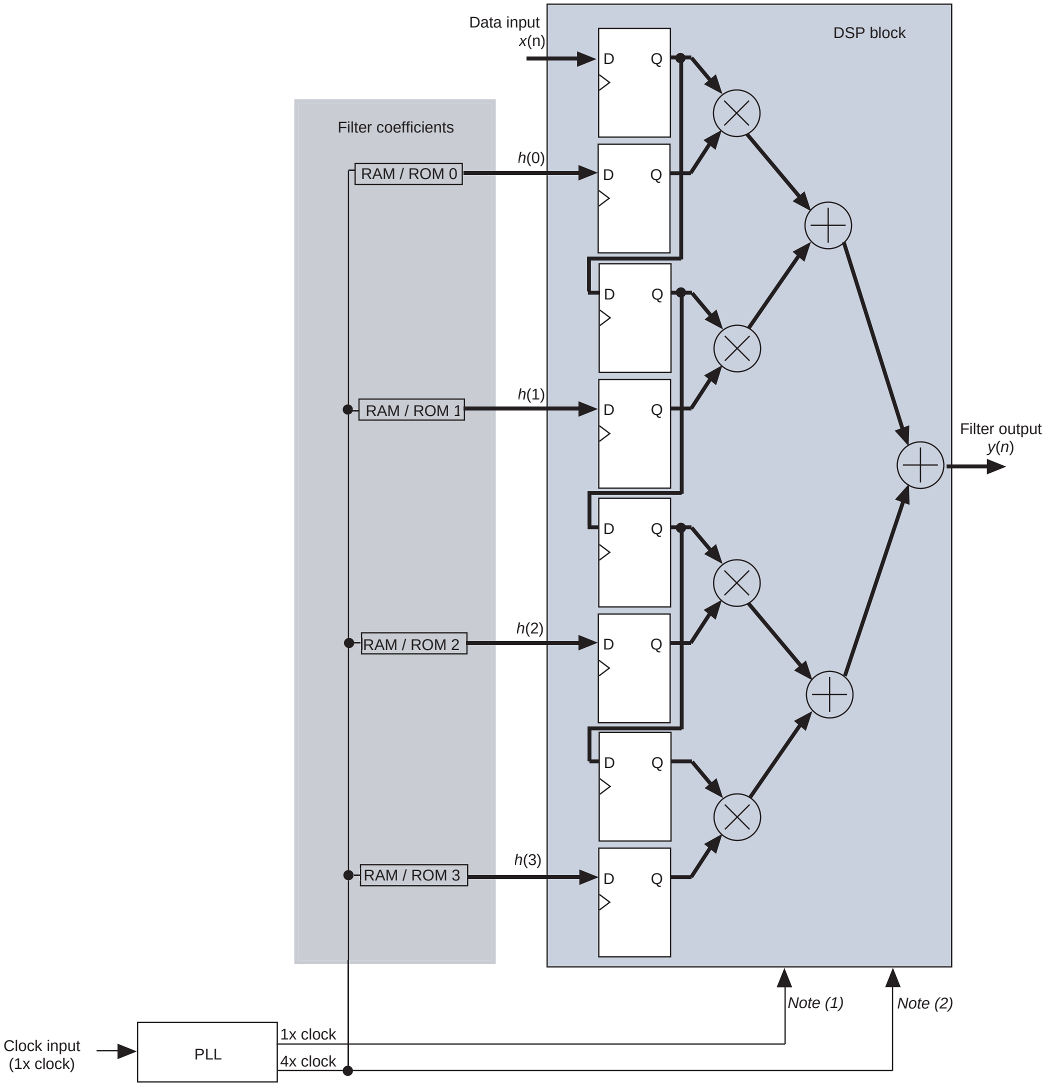
Figure 7–13 shows the Stratix or Stratix GX implementation of the polyphase interpolation filter in Figure 7–12. The four polyphase filters share the same hardware, which is a 4-tap filter. One Stratix or Stratix GX DSP block can implement one 4-tap filter with 18-bit wide data and coefficients. A multiplexer can be used to load new coefficient values on every cycle of the 4× clock. Stratix and Stratix GX phase lock loops (PLLs) can generate the 4× clock. In the first cycle of the 4× clock, the user needs to load coefficients for polyphase filter $h_0$(`n`); in the second cycle of the 4×

clock, the users needs to load coefficients of the polyphase filter $h_1$(`n`) and so on. Table 7–10 summarizes the coefficient loading schedule. The output, $y$(`n`), is clocked using the 4× clock.

*Table 7–10. Polyphase Interpolation (I=4) Filter Coefficient Loading Schedule*

| Cycle of 4× Clock | Coefficients to Load | Corresponding RAM/ROM |
|---|---|---|
| 1, 5,... | h(0), h(4), h(8), h(12) | 0, 1, 2, 3 |
| 2, 6,... | h(1), h(5), h(9), h(13) | 0, 1, 2, 3 |
| 3, 7,... | h(2), h(6), h(10), h(14) | 0, 1, 2, 3 |
| 4, 8,... | h(3), h(7), h(11), h(15) | 0, 1, 2, 3 |

***Figure 7–13. Implementation of the Polyphase Interpolation Filter (I=4)*** *Notes (1), (2), (3)*



***Notes to Figure 7–13:***

(1) The 1× clock feeds the input data shiftin register chain.

(2) The 4×clock feeds the input registers for the filter coefficients and other optional registers in the DSP block. Refer to *Note (3)*.

(3) To increase the DSP block performance, include the pipeline, and output registers. Refer to Figure 7–3 for the details.

### Polyphase Interpolation Filter Implementation Results

Table 7–11 shows the results of the polyphase interpolation filter implementation in a Stratix device shown in Figure 7–13.

*Table 7–11. Polyphase Interpolation Filter Implementation Results*

| Part | EP1S10F780 |
|---|---|
| Utilization | Lcell: 3/10570 (<1%)<br>DSP Block 9-bit elements: 8/48 (17%)<br>Memory bits: 288/920448 (<1%) |
| Performance | 240 MHz *(1)* |

***Note to Table 7–11:***

(1) This refers to the performance of the DSP blocks, as well as the output clock rate. The input rate is 60 MSPS, clocked in at 60MHz.

### Polyphase Interpolation Filter Design Example

Download the Interpolation FIR Filter (**interpolation_fir.zip**) design example from the Design Examples section of the Altera web site at **http://www.altera.com.**

## Polyphase FIR Decimation Filters

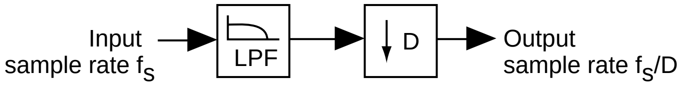
A decimation filter can be used to decrease the sample rate. A decimation filter is efficiently implemented with a polyphase FIR filter. DSP systems frequently use polyphase filters because they simplify overall system design and also reduce the number of computations per cycle required of the hardware. This section first describes decimation filters and then how to implement them as polyphase filters in Stratix devices. See the "Polyphase FIR Interpolation Filters" section for a discussion of interpolation filters.

### Decimation Filter Basics

A decimation filter decreases the output sample rate by a factor of `D` through keeping only every `D`-th input sample. Consequently, the samples at the output of the decimation filter are separated by $D \times T_s = D/f_s$, where $T_s$ and $f_s$ are the sample period and sample frequency of the original signal, respectively. Figure 7–14 shows the concept of signal decimation.

The signal needs to be low pass filtered before downsampling can begin in order to avoid the reflections of the original spectrum from being aliased back into the output signal.

*Figure 7–14. Block Diagram Representation of Decimation*

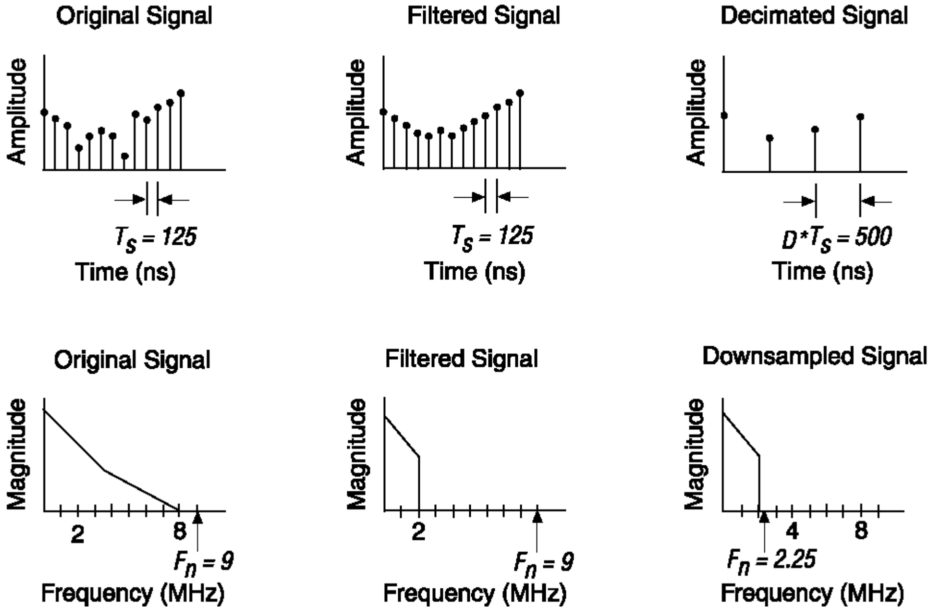


Decimation filters reverse the effect of the interpolation filters. Before the decimation process, a low pass filter is applied to the signal to attenuate noise and aliases present beyond the Nyquist frequency. The filtered signal is then applied to the decimation filter, which processes every D-th input. Therefore the values between samples `D`, `D`-1, `D`-2 etc. are ignored. This allows the filter to run `M` times slower than the input data rate.

In a typical system, after the analog to digital conversion is complete, the data needs to be filtered to remove aliases inherent in the sampled data. Further, at this point there is no need to continue to process this data at the higher sample (oversampled) rate. Therefore, a decimation FIR filter at the output of the ADC lowers the data rate to a value that can be processed digitally.

Figure 7–15 shows a specific example where a signal spread over 8 MHz is decimated by a factor of 4 to 2 MHz. The Nyquist frequency of the downsampled signal must be greater than 2 MHz, and is chosen to be 2.25 MHz in this example.

*Figure 7–15. Time & Frequency Domain Representations of Decimation for D=4*



### *Polyphase Decimation Filters*

Figure 7–14 shows a direct implementation of a decimation filter, which imposes a high computational burden. For example, if the filter is 16 taps long and a multiplication takes one cycle, the number of computations required per cycle is 16×`D`. Depending on the decimation factor (`D`), this number can be quite big and may not be achievable in hardware. A polyphase implementation of the low pass filter can reduce the number of computations required, often by a large ratio, as will be evident later in this section.

The polyphase implementation "splits" the original filter into `D` polyphase filters with impulse responses defined by the following equation.

$$h_k(n) = h(k + nD)$$

where:

$k = 0,1, \ldots, D-1$
$n = 0,1, \ldots, P-1$
$P = L/D$ = length of polyphase filters
$L$ is the length of the filter (selected to be a multiple of $D$)
$D$ is the decimation factor
$h(n)$ is the original filter impulse response

This equation implies that the first polyphase filter, $h_0(n)$, has coefficients $h(0)$, $h(D)$, $h(2D) \ldots h((P-1)D)$. The second polyphase filter, $h_1(n)$, has coefficients $h(1)$, $h(1+D)$, $h(1+2D)$, ..., $h(1+(P-1)D)$. Continuing in this way, the last polyphase filter, $h_{D-1}(n)$ has coefficients $h(D-1)$, $h((D-1)+D)$, $h((D-1)+2D)$, ..., $h((D-1)+(P-1)D)$.

An example helps in the understanding of the polyphase implementation of decimation. Consider the polyphase representation of a 16-tap low pass filter with a decimation factor of 4. The output is given by:

$$y(n) = \sum_{i=0}^{15} h(i)x(nD - i)$$

Referring to Figure 7–15 on page 7–27, it is clear that the output, $y(n)$ is discarded for $n \neq 0, 4, 8, 12$, hence the only values of $y(n)$ that need to be computed are $y(0)$, $y(4)$, $y(8)$, $y(12)$. Table 7–12 shows which coefficients are required to generate the output samples.

*Table 7–12. Decomposition of a 16-Tap Decimation Filter into Four Polyphase Filters*

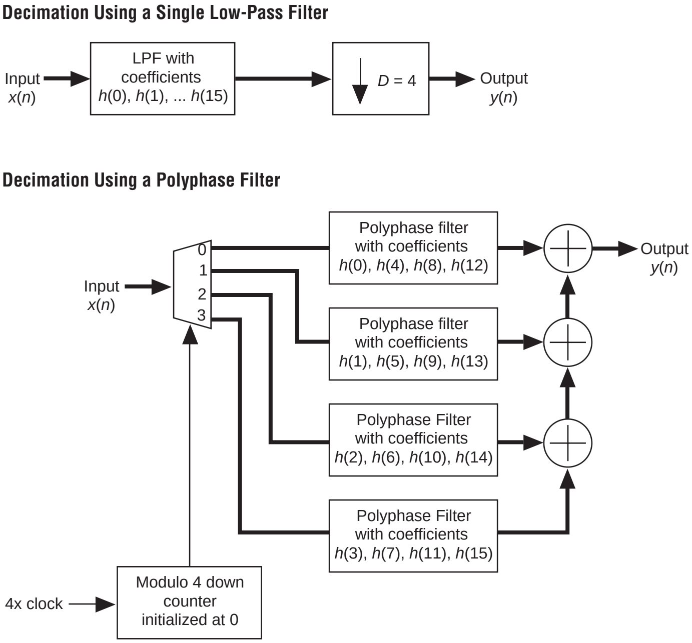
| Output Sample *(1)* | Coefficients Required | Polyphase Filter Impulse Response |
|---|---|---|
| $y(0)_0$, $y(4)_0$, . . . | h(0), h(4), h(8), h(12) | $h_0(n)$ |
| $y(0)_1$, $y(4)_1$, . . . | h(1), h(5), h(9), h(13) | $h_1(n)$ |
| $y(0)_2$, $y(4)_2$, . . . | h(2), h(6), h(10), h(14) | $h_2(n)$ |
| $y(0)_3$, $y(4)_3$, . . . | h(3), h(7), h(11), h(15) | $h_3(n)$ |

***Note to Table 7–12:***
(1) The output sample is the sum of the results from four polyphase filters: $y(n) = y(n)_0 + y(n)_1 + y(n)_2 + y(n)_3$.

Table 7–12 shows that the overall decimation filter operation can be represented by 4 parallel polyphase filters. Figure 7–16 shows the polyphase representation of the decimation filter. A demultiplexer at the input ensures that the input is applied to only one polyphase filter at a time. The demultiplexer is controlled by a counter, which counts down modulo-`D` starting at `0`. The overall output is taken by adding the outputs of all the filters.

The polyphase representation of the decimation filter also reduces the computational requirement. For the example in Figure 7–16, the direct implementation requires 16 × `D` = 16 × 4 = 64 computations per cycle, whereas the polyphase implementation requires only 4 × 4 × 1 = 16 computations per cycle. This saving in computational complexity is quite significant and is often a very convincing reason to use polyphase filters.

*Figure 7–16. Polyphase Filter Representation of a D=4 Decimation Filter*



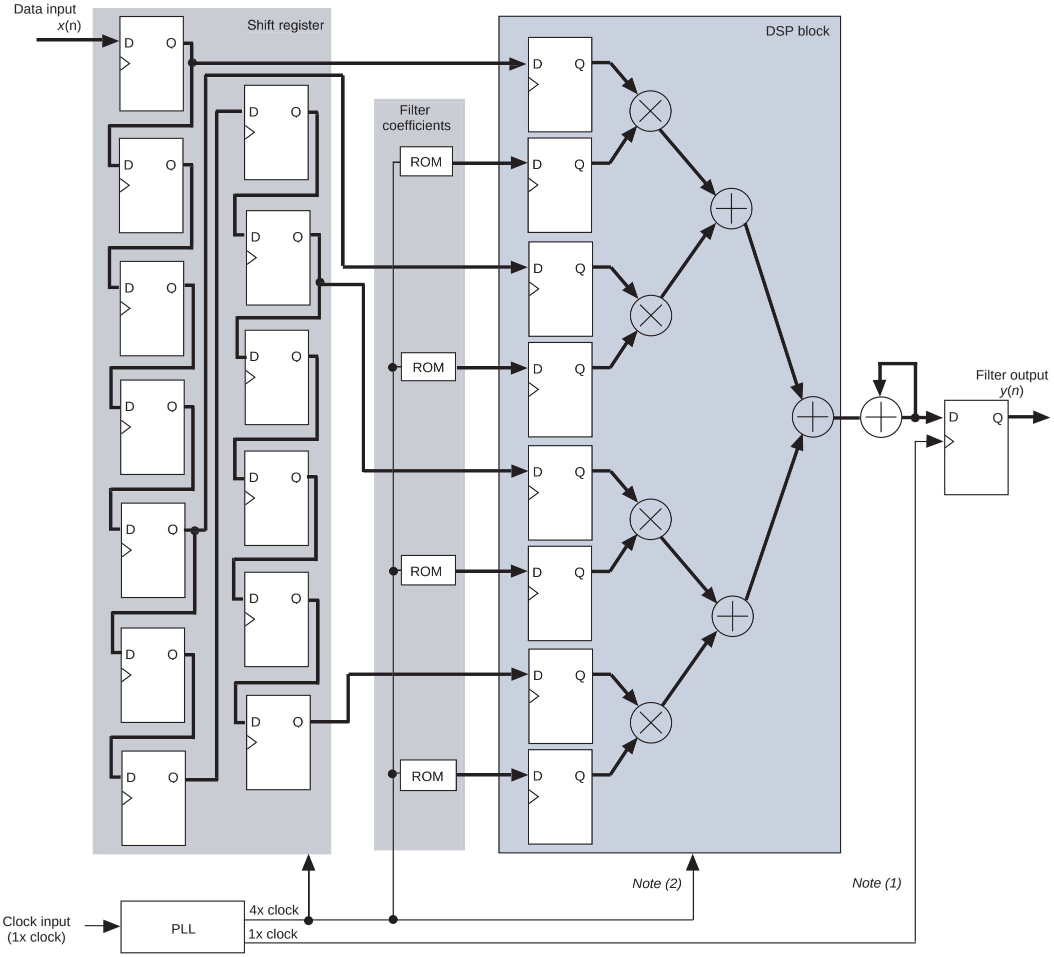
### *Polyphase Decimation Filter Implementation*

Figure 7–17 shows the decimation polyphase filter example of Figure 7–16 as it would fit into Stratix or Stratix GX DSP blocks. The coefficients of the polyphase filters need to be cycled using the schedule shown in Table 7–13. The output $y(n)$, is clocked using the 1× clock.

***Table 7–13. Coefficient Loading Schedule for Polyphase Decimation Filter (D=4)***

| Cycle of 4× Clock | Coefficients to Load | Corresponding RAM/ROM |
|---|---|---|
| 1, 5,... | h(0), h(4), h(8), h(12) | 0, 1, 2, 3 |
| 2, 6,... | h(3), h(7), h(11), h(15) | 0, 1, 2, 3 |
| 3, 7,... | h(2), h(6), h(10), h(14) | 0, 1, 2, 3 |
| 4, 8,... | h(1), h(5), h(9), h(13) | 0, 1, 2, 3 |

*Figure 7–17. Implementation of the Polyphase Decimation Filter (D=4)* Notes (1), (2), (3)



*Notes to Figure 7–17:*

(1) The 1× clock feeds the register after the accumulator block.

(2) The 4× clock feeds the shift register for the data, the input registers for both the data and filter coefficients, the other optional registers in the DSP block (refer to Note (3)), and the accumulator block.

(3) To increase the DSP block performance, include the pipeline, and output registers. Refer to Figure 7–3 for the details.

### Polyphase Decimation Filter Implementation Results

Table 7–14 shows the results of the polyphase decimation filter implementation in a Stratix device shown in Figure 7–17.

**Table 7–14. Polyphase Decimation Filter Implementation Results**

| | |
|---|---|
| Part | EP1S10F780 |
| Utilization | Lcell: 168/10570 (1%)<br>DSP Block 9-bit elements: 8/48 (17%)<br>Memory bits: 300/920448(<1%) |
| Performance | 240 MHz *(1)* |

***Note to Table 7–14:***

(1) This refers to the performance of the DSP blocks, as well as the input clock rate. The output rate is 60 MSPS (clocked out at 60MHz).

### Polyphase Decimation Filter Design Example

Download the Decimation FIR Filter (**decimation_fir.zip**) design example from the Design Examples section of the Altera web site at www.altera.com.

## Complex FIR Filter

A complex FIR filter takes real and imaginary input signals and performs the filtering operation with real and imaginary filter coefficients. The output also consists of real and imaginary signals. Therefore, a complex FIR filter is similar to a regular FIR filter except for the fact that the input, output, and coefficients are all complex numbers.

One example application of complex FIR filters is equalization. Consider a Phase Shift Keying (PSK) system; a single complex channel can represent the I and Q data channels. A FIR filter with complex coefficients could then process both data channels simultaneously. The filter coefficients are chosen in order to reverse the effects of intersymbol interference (ISI) inherent in practical communication channels. This operation is called equalization. Often, the filter is adaptive, i.e. the filter coefficients can be varied as desired, to optimize performance with varying channel characteristics.

A complex variable FIR filter is a cascade of complex multiplications followed by a complex addition. Figure 7–18 shows a block diagram representation of a complex FIR filter. To compute the overall output of the FIR filter, it is first necessary to determine the output of each complex multiplier. This can be expressed as:

$$y_{real} = x_{real} \times h_{real} - x_{imag} \times h_{imag}$$
$$y_{imag} = x_{real} \times h_{imag} + h_{real} \times x_{imag}$$

where:

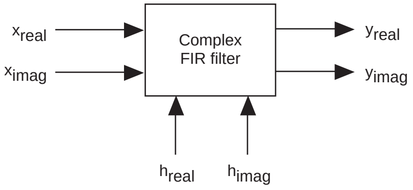
$x_{real}$ is the real input signal
$x_{imag}$ is the imaginary input signal
$h_{real}$ is the real filter coefficients
$h_{imag}$ is the imaginary filter coefficients
$y_{real}$ is the real output signal
$y_{imag}$ is the imaginary output signal

In complex representation, this equals:

$$y_{real} + jy_{imag} = (x_{real} + jx_{imag}) \times (h_{real} + jh_{imag})$$

The overall real channel output is obtained by adding the real channel outputs of all the multipliers. Similarly, the overall imaginary channel output is obtained by adding the imaginary channel outputs of all the multipliers.

**Figure 7–18. Complex FIR Filter Block Diagram**



### Complex FIR Filter Implementation

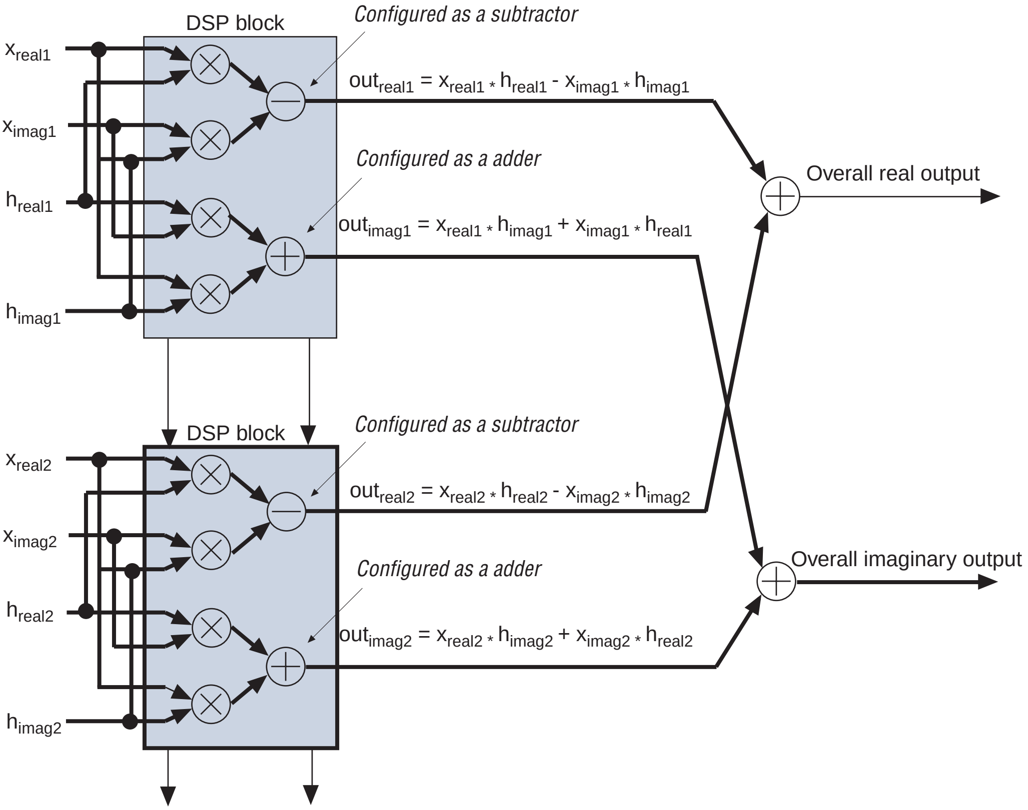
Complex filters can be easily implemented in Stratix devices with the DSP blocks configured in the two-multipliers adder mode. One DSP block can implement a 2-tap complex FIR filter with 9-bit inputs, or a single tap complex FIR filter with 18-bit inputs. DSP blocks can be cascaded to implement complex filters with more taps.

☞ The two-multipliers adder mode has two adders, each adding the outputs of two multipliers. One of the adders is configured as a subtractor.

For more information on the different modes of the DSP blocks see Chapter 6, Using the DSP Blocks in Stratix & Stratix GX Devices.

Figure 7–19 shows an example of a 2-tap complex FIR filter design with 18-bit inputs. The real and the complex outputs of the DSP blocks are added externally to generate the overall real and imaginary output. As in the case of basic, TDM, or polyphase FIR filters, the coefficients may be loaded in series or parallel.

*Figure 7–19. 2-Tap 18-Bit Complex FIR Filter Implementation*



# Infinite Impulse Response (IIR) Filters

Another class of digital filters are IIR filters. These are recursive filters where the current output is dependent on previous outputs. In order to maintain stability in an IIR filter, careful design consideration must be given, especially to the effects of word-length to avoid unbounded conditions. The following section discusses the general theory and applications behind IIR Filters.

## IIR Filter Background

The impulse response of an IIR filter extends for an infinite amount of time because their output is based on feedback from previous outputs. The general expression for IIR filters is:

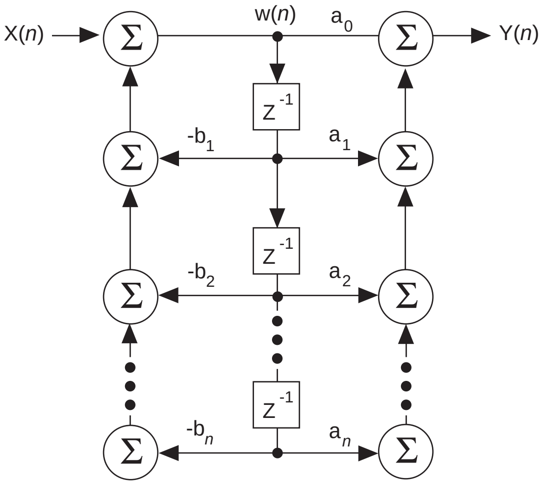
$$y(n) = \sum_{i=0}^{n} a(i)x(n-i) - \sum_{i=1}^{n} b(i)y(n-i)$$

where $a_i$ and $b_i$ represent the coefficients in the feed-forward path and feedback path, respectively, and `n` represents the filter order. These coefficients determine where the poles and zeros of the IIR filter lie. Consequently, they also determine how the filter functions (i.e., cut-off frequencies, band pass, low pass, etc.).

The feedback feature makes IIR filters useful in high data throughput applications that require low hardware usage. However, feedback also introduces complications and caution must be taken to make sure these filters are not exposed to situations in which they may become unstable. The complications include phase distortion and finite word length effects, but these can be overcome by ensuring that the filter always operates within its intended range.

Figure 7–20 shows a direct form II structure of an IIR filter.

*Figure 7–20. Direct Form II Structure of an IIR Filter*



The transfer function for an IIR filter is:

$$H(z) = \frac{\sum_{i=0} a_i z^{-i}}{1 + \sum_{i=1}^{n} b_i z^{-i}}$$

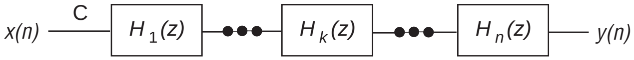
The numerator contains the zeros of the filter and the denominator contains the poles. The IIR filter structure requires a multiplication followed by an accumulation. Constructing the filter directly from the transfer function shown above may result in finite word length limitations and make the filter potentiality unstable. This becomes more critical as the filter order increases, because it only has a finite number of bits to represent the output. To prevent overflow or instability, the transfer function can be split into two or more terms representing several second order filters called biquads. These biquads can be individually scaled and cascaded, splitting the poles into multiples of two. For example, an IIR filter having ten poles should be split into five biquad sections. Doing this minimizes quantization and recursive accumulation errors.

This cascaded structure rearranges the transfer function. This is shown in the equation below, where each product term is a second order IIR filter. If n is odd, the last product term is a first order IIR filter:

$$H(z) = C \times \prod_{k=1}^{(n+1)/2} \frac{a_{0k} + a_{1k}z^{-1} + a_{2k}z^{-2}}{1 + b_{1k}z^{-1} + b_{2k}z^{-2}} = C \times \prod_{k=1}^{(n+1)/2} H_k(z)$$

Figure 7–21 shows the cascaded structure.

*Figure 7–21. Cascaded IIR Filter*



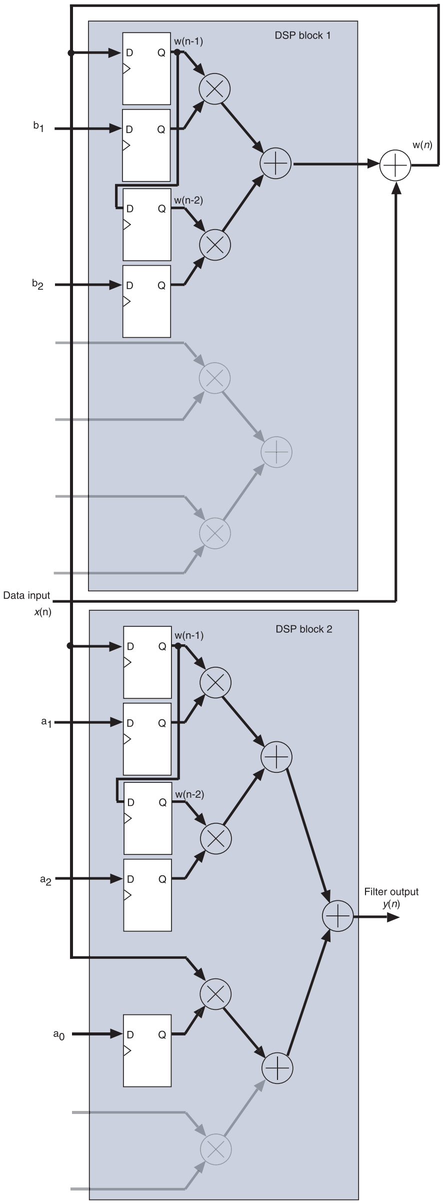
## Basic IIR Filters

In this section, the basic IIR filter is implemented using cascaded second order blocks or biquads in the direct form II structure.

### Basic IIR FIlter Implementation

Multiplier blocks, adders and delay elements can implement a basic IIR filter. The Stratix architecture lends itself to IIR filters because of its embedded DSP blocks, which can easily be configured to perform these operations. The `altmult_add` megafunction can be used to implement the multiplier-adder mode in the DSP blocks. Figure 7–22 shows the implementation of an individual biquad using Stratix and Stratix GX DSP blocks.

*Figure 7–22. IIR Filter Biquad* *Note (1)*

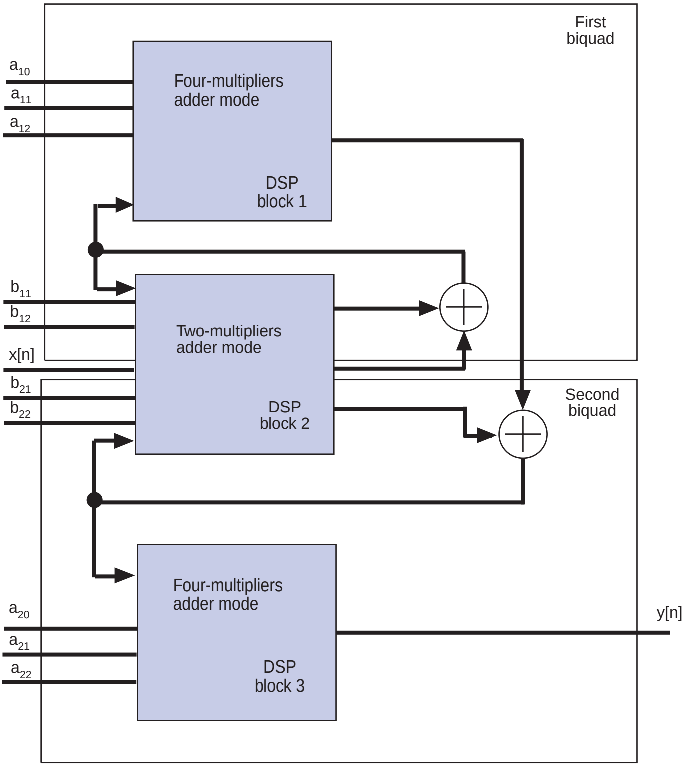


*Notes to Figure 7–22:*

(1) Unused ports are grayed out.

The first DSP block in Figure 7–22 is configured in the two-multipliers adder mode, and the second DSP block is in the four-multipliers adder mode. For an 18-bit input to the IIR filter, each biquad requires five multipliers and five adders (two DSP blocks). One of the adders is implemented using logic elements. Cascading several biquads together can implement more complex, higher order IIR filters. It is possible to insert registers in between the biquad stages to improve the performance. Figure 7–23 shows a 4th order IIR filter realized using two cascaded biquads in three DSP blocks.

*Figure 7–23. Two Cascaded Biquads*



### *Basic IIR Filter Implementation Results*

Table 7–15 shows the results of implementing a 4th order IIR filter in a Stratix device.

**Table 7–15. 4th Order IIR Filter Implementation Results**

| | |
|---|---|
| Part | EP1S10F780C5 |
| Utilization | Lcell: 102/10570(<1%)<br>DSP Block 9-bit elements: 24/48 (50%)<br>Memory bits: 0/920448(0%) |
| Performance | 73 MHz |
| Latency | 4 clock cycles |

### *Basic IIR Filter Design Example*

Download the 4th Order IIR Filter (**iir.zip**) design example from the Design Examples section of the Altera web site at www.altera.com**.**

## Butterworth IIR Filters

Butterworth filters are the most popular version of IIR analog filters. These filters are also known as “maximally flat” because they have no passband ripple. Additionally, they have a monotonic response in both the stopband and the passband. Butterworth filters trade-off roll off steepness for their no ripple characteristic. The distinguishing Butterworth filter feature is its poles are arranged in a uniquely symmetrical manner along a circle in the *s*-plane. The expression for the Butterworth filter’s magnitude-squared function is as follows:

$$|H_c(j\omega)|^2 = \frac{1}{1+\left(\frac{j\omega}{j\omega_c}\right)^{2N}}$$

where:

$\omega_c$ is the cut-off frequency
$N$ is the filter order

The filter’s cutoff characteristics become sharper as $N$ increases. If a substitution is made such that $j\omega = s$, then the following equation is derived:

$$H_c(s)H_c(-s) = \frac{1}{1+\left(\frac{s}{j\omega_c}\right)^{2N}}$$

with poles at:

$$\begin{aligned} s_k &= (-1)^{\frac{1}{2N}}(j\omega_c) \\ &= \omega_c e^{\left(\frac{j\pi}{2N}\right)(2k+N-1)} \end{aligned} \qquad \text{for } k=0,1,\ldots,2N\text{-}1$$

There are 2N poles on the circle with a radius of $\omega_c$ in the *s*-plane. These poles are evenly spaced at $\pi/N$ intervals along the circle. The poles chosen for the implementation of the filter lie in the left half of the *s*-plane, because these generate a stable, causal filter.

Each of the impulse invariance, the bilinear, and matched *z* transforms can transform the Laplace transform of the Butterworth filter into the *z*-transform.

- Impulse invariance transforms take the inverse of the Laplace transform to obtain the impulse response, then perform a *z*-transform on the sampled impulse response. The impulse invariance method can cause some aliasing.
- The bilinear transform maps the entire *j*ω-axis in the *s*-plane to one revolution of the unit circle in the *z*-plane. This is the most popular method because it inherently eliminates aliasing.
- The matched *z*-transform maps the poles and the zeros of the filter directly from the *s*-plane to the *z*-plane. Usually, these transforms are transparent to the user because several tools, such as MATLAB, exist for determining the coefficients of the filter. The *z*-transform generates the coefficients much like in the basic IIR filter discussed earlier.

### *Butterworth Filter Implementation*

For digital designs, consideration must be made to optimize the IIR biquad structure so that it maps optimally into logic. Because speed is often a critical requirement, the goal is to reduce the number of operations per biquad. It is possible to reduce the number of multipliers needed in each biquad to just two.

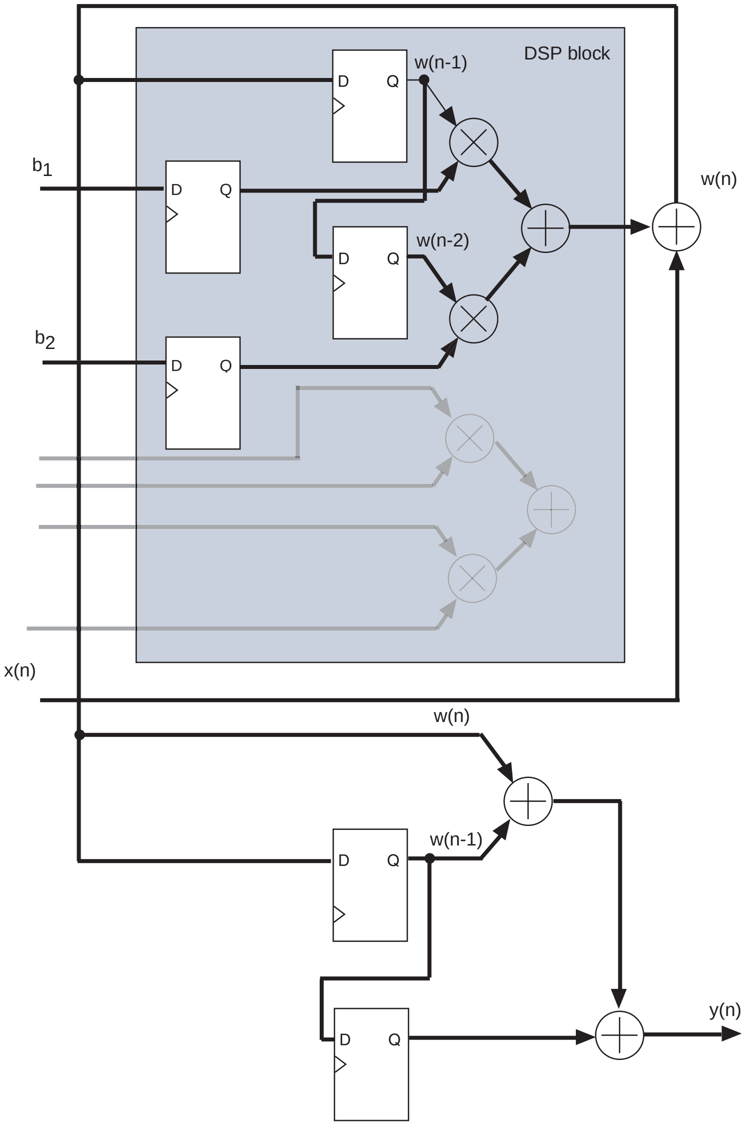
Through the use of integer feedforward multiplies, which can be implemented by combining addition, shifting, and complimenting operations, a Butterworth filter's transfer function biquad can be optimized for logic synthesis. The most efficient transformation is that of an all pole filter. This is because there is a unique relationship between the feedforward integer coefficients of the filter represented as:

$$H(z) = \frac{1 + 2z^{-1} + z^{-2}}{1 + b_1 z^{-1} + b_2 z^{-2}}$$

As can be seen by this equation, the $z^{-1}$ coefficient in the numerator (representing the feedforward path) is twice the other two operands ($z^{-2}$ and 1). This is always the case in the transformation from the frequency to the digital domain. This represents the normalized response, which is faster and smaller to implement in hardware than real multipliers. It introduces a scaling factor as well, but this can be corrected at the end of the cascade chain through a single multiply.

Figure 7–24 shows how a Butterworth filter biquad is implemented in a Stratix or Stratix GX device.

*Figure 7–24. Butterworth Filter Biquad* Notes (1), (2)



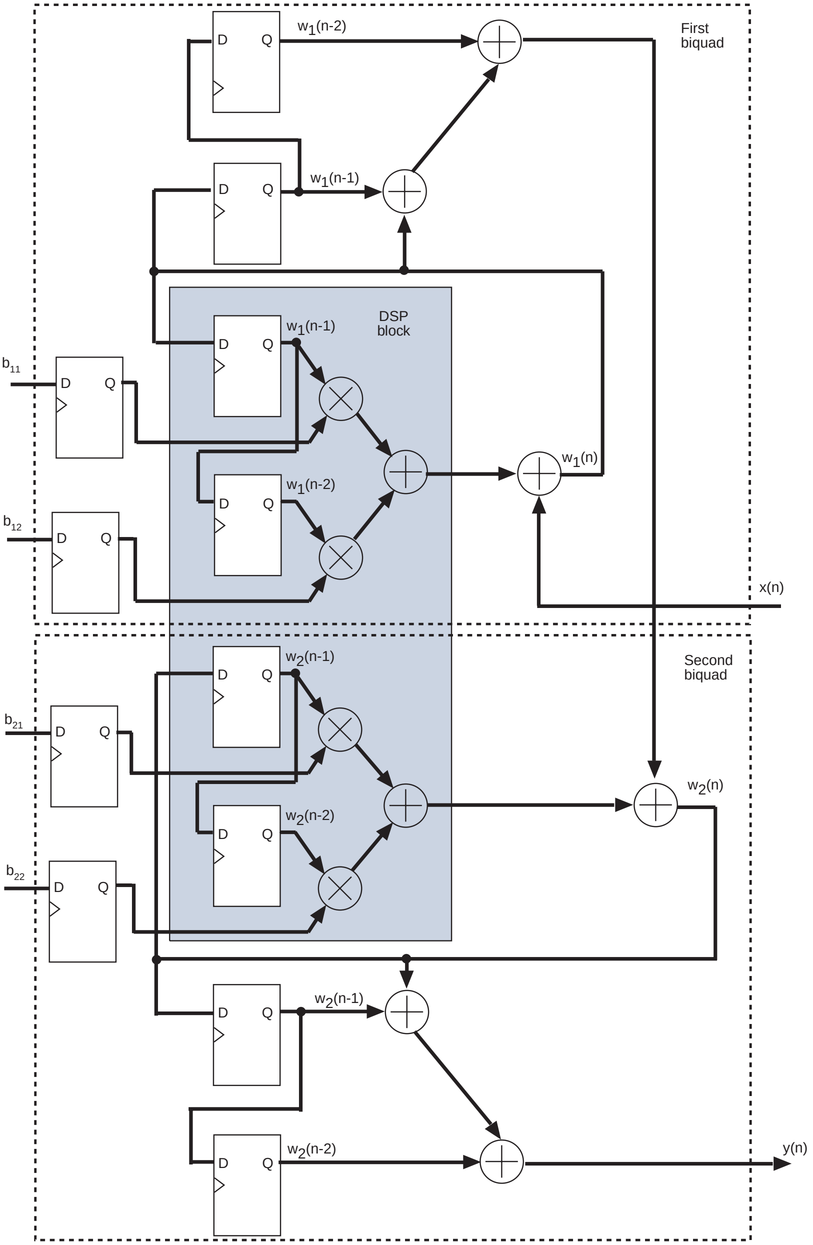
*Notes to Figure 7–24:*

(1) Unused ports are grayed out.

(2) The $z^{-1}$ coefficient is a multiple of the other coefficients ($z$-2 and 1) in the feedforward path. This is implemented using a shift operation.

The DSP block in Figure 7–24 is configured in multiply and add mode. The three external adders are implemented in logic elements and therefore are not part of the DSP block. Therefore, for an 18-bit input, each biquad requires half a DSP block and three logic element adders. The gain factor can be compensated for at the end of the filtering stage and is not shown in this simple example. More complex, higher order Butterworth filters can be realized by cascading several biquads together, as in the IIR example. Figure 7–25 below shows a 4th order Butterworth filter using two cascaded biquads in a single DSP block.

*Figure 7–25. Cascaded Butterworth Biquads* *Note (1)*



*Notes to Figure 7–25:*

(1) The gain factor is compensated for at the end of the filtering stage and is not shown in this figure.

### *Butterworth Filter Implementation Results*

Table 7–16 shows the results of implementing a 4th order Butterworth filter as shown in Figure 7–25.

*Table 7–16. 4th Order Butterworth Filter Implementation Results*

| | |
|---|---|
| Part | EP1S10F780C6 |
| Utilization | Lcell: 251/10570(2%)<br>DSP Block 9-bit elements: 16/48 (33%)<br>Memory bits: 0/920448 (0%) |
| Performance | 80 MHz |
| Latency | 4 clock cycles |

### *Butterworth Filter Design Example*

Download the 4th Order Butterworth Filter (**butterworth.zip**) design example from the Design Examples section of the Altera web site at www.altera.com**.**

## Matrix Manipulation

DSP relies heavily on matrix manipulation. The key idea is to transform the digital signals into a format that can then be manipulated mathematically.

This section describes an example of matrix manipulation used in 2-D convolution filter, and its implementation in a Stratix device.

### Background on Matrix Manipulation

A matrix can represent all digital signals. Apart from the convenience of compact notation, matrix representation also exploits the benefits of linear algebra. As with one-dimensional, discrete sequences, this advantage becomes more apparent when processing multi-dimensional signals.

In image processing, matrix manipulation is important because it requires analysis in the spatial domain. Smoothing, trend reduction, and sharpening are examples of common image processing operations, which are performed by convolution. This can also be viewed as a digital filter operation with the matrix of filter coefficients forming a convolutional kernel, or mask.

## Two-Dimensional Filtering & Video Imaging

FIR filtering for video applications and image processing in general is used in many applications, including noise removal, image sharpening to feature extraction.

For noise removal, the goal is to reduce the effects of undesirable, contaminative signals that have been linearly added to the image. Applying a low pass filter or smoothing function flattens the image by reducing the rapid pixel-to-pixel variation in gray levels and, ultimately, removing noise. It also has a blurring effect usually used as a precursor for removing unwanted details before extracting certain features from the image.

Image sharpening focuses on the fine details of the image and enhances sharp transitions between the pixels. This acts as a high-pass filter that reduces broad features like the uniform background in an image and enhances compact features or details that have been blurred.

Feature extraction is a form of image analysis slightly different from image processing. The goal of image analysis in general is to extract information based on certain characteristics from the image. This is a multiple step process that includes edge detection. The easiest form of edge detection is the derivative filter, using gradient operators.

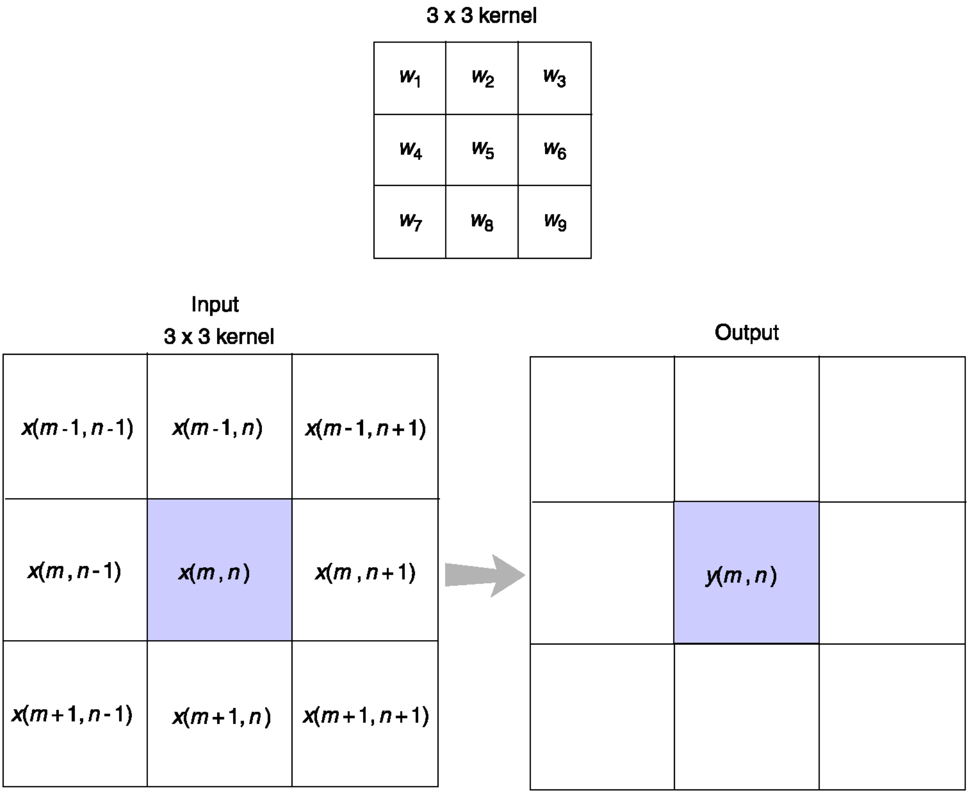
All of the operations above involve transformation of the input image. This can be presented as the convolution of the two-dimensional input image, $x(m,n)$ with the impulse response of the transform, $f(k,l)$, resulting in $y(m,n)$ which is the output image.

$$y(m, n) = f(k, l) \otimes x(m, n)$$

$$y(m, n) = \sum_{k=-N}^{N} \sum_{l=-N}^{N} f(k, l)x(m-k, n-l)$$

The $f(k,l)$ function refers to the matrix of filter coefficients. Because the matrix operation is analogous to a filter operation, the matrix itself is considered the impulse response of the filter. Depending on the type of operation, the choice of the convolutional kernel or mask, $f(k,l)$ is different. Figure 7–26 shows an example of convolving a 3 × 3 mask with a larger image.

*Figure 7–26. Convolution Using a 3 × 3 Kernel*

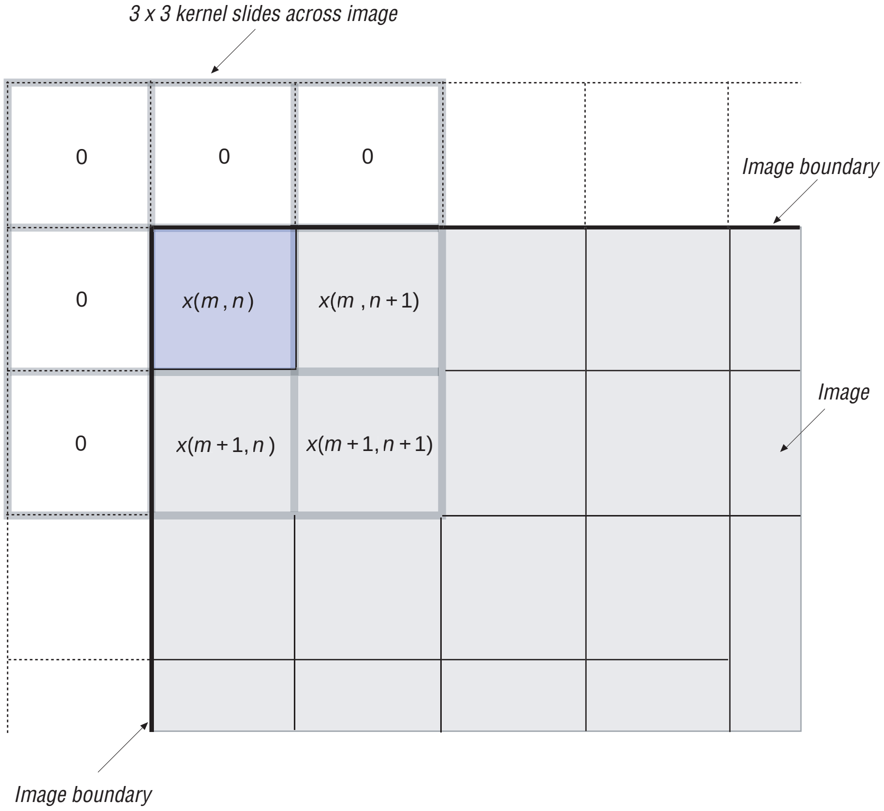


The output pixel value, *y(*`m,n`*)* depends on the surrounding pixel values in the input image, as well as the filter weights:

$$\begin{aligned} y(m, n) = {} & w_1x(m-1, n-1) + w_2x(m-1, n) + w_3x(m-1, n+1) \\ & + w_4x(m, n-1) + w_5x(m, n) + w_6x(m, n+1) \\ & + w_7x(m+1, n-1) + w_8x(m+1, n) + w_9x(m+1, n+1) \end{aligned}$$

To complete the transformation, the kernel slides across the entire image. For pixels on the edge of the image, the convolution operation does not have a complete set of input data. To workaround this problem, the pixels on the edge can be left unchanged. In some cases, it is acceptable to have an output image of reduced size. Alternatively, the matrix effect can be applied to edge pixels as if they are surrounded on the “empty” side by black pixels, that is pixels with value zero. This is similar to padding the edges of the input image matrix with zeros and is referred to as the free boundary condition. This is shown in Figure 7–27.

*Figure 7–27. Using Free Boundary Condition for Edge Pixels*

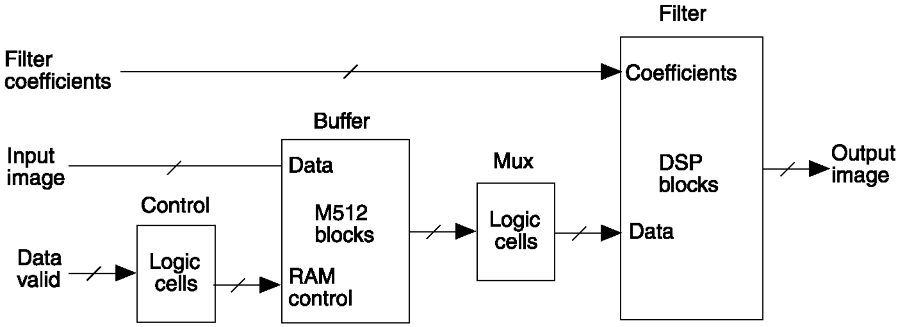


### Convolution Implementation

This design example shows a 3 × 3 2-D FIR filter that takes in an 8 × 8 input image with gray pixel values ranging from 0-255 (8-bit). Data is fed in serially starting from the top left pixel, moving horizontally on a row-by-row basis. Next the data is stored in three separate RAM blocks in the buffering stage. Each M512 memory block represents a line of the image, and this is cycled through. For a 32 × 32 input image, the design needs M4K memory blocks. For larger images (640 × 480), this can be extended to M-RAM blocks or other buffering schemes. The control logic block provides the RAM control signals to interleave the data across all three

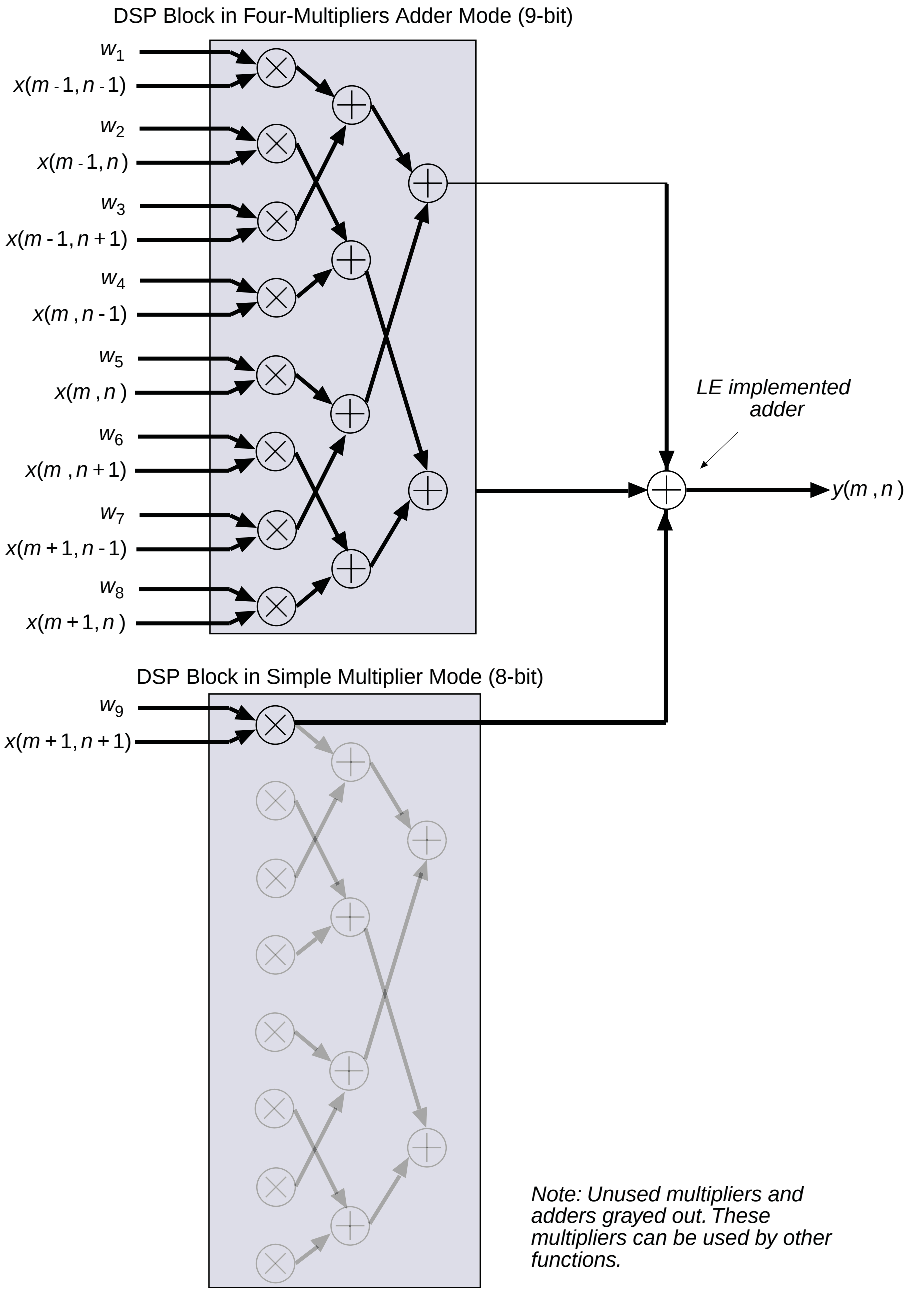
RAM blocks. The 9-bit signed filter coefficients feed directly into the filter block. As the data is shifted out from the RAM blocks, the multiplexer block checks for edge pixels and uses the free boundary condition. Figure 7–28 shows a top-level diagram of the design.

*Figure 7–28. Block Diagram on Implementation of 3 × 3 Convolutional Filter for an 8 × 8 Pixel Input Image*



The 3 × 3 filter block implements the nine multiply-add operations in parallel using two DSP blocks. One DSP block can implement eight of these multipliers. The second DSP block implements the ninth multiplier. The first DSP block is in the four-multipliers adder mode, and the second is in simple multiplier mode. In addition to the two DSP blocks, an external adder is required to sum the output of all nine multipliers. Figure 7–29 shows this implementation.

Figure 7–29. Implementation of 3 × 3 Convolutional Filter Block



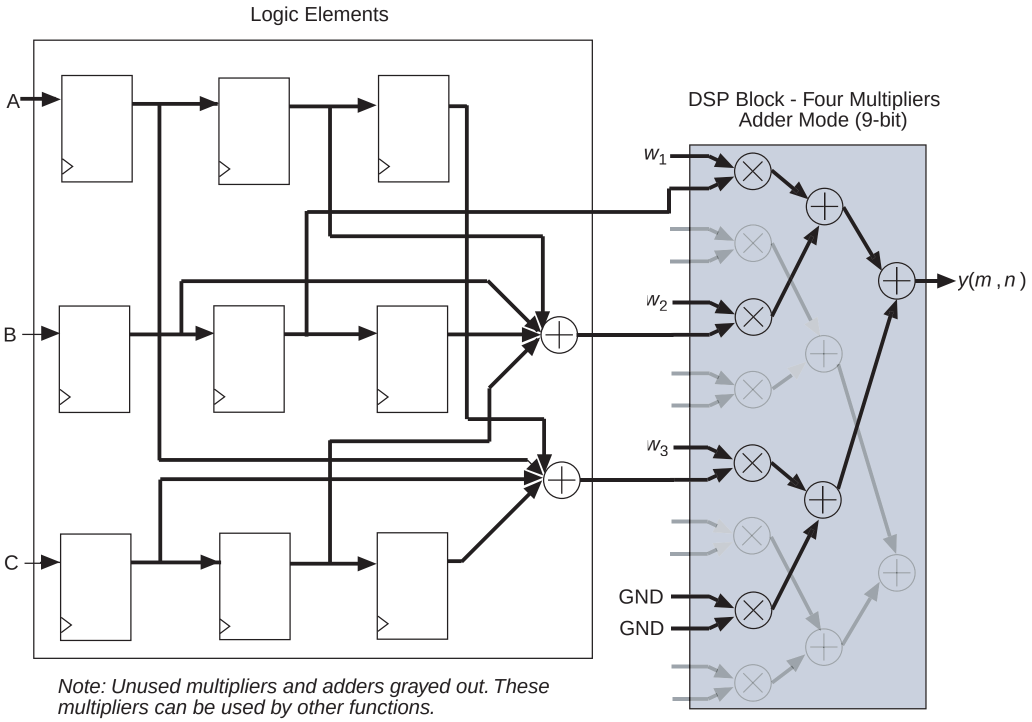
Note: Unused multipliers and adders grayed out. These multipliers can be used by other functions.

In cases where a symmetric 2-D filter is used, pixels sharing the same filter coefficients from three separate line-stores A, B, and C can be added together prior to the multiplication operation. This reduces the number of multipliers used. Referring to Figure 7–30, $w_1$, $w_2$, and $w_3$ are the filter coefficients. Figure 7–31 shows the implementation of this circular symmetric filter.

*Figure 7–30. Symmetric 3 × 3 Kernel*

| | | |
|---|---|---|
| $w_3$ | $w_2$ | $w_3$ |
| $w_2$ | $w_1$ | $w_2$ |
| $w_3$ | $w_2$ | $w_3$ |

*Figure 7–31. Details on Implementation of Symmetric 3 × 3 Convolution Filter Block*



*Note: Unused multipliers and adders grayed out. These multipliers can be used by other functions.*

### *Convolution Implementation Results*

Table 7–17 shows the results of the 3 × 3 2-D FIR filter implementation in Figure 7–28.

*Table 7–17. 3 × 3 2-D Convolution Filter Implementation Results*

| Part | EP1S10F780 |
|---|---|
| Utilization | Lcell: 372/10570 (3%)<br>DSP block 9-bit elements: 9/48 (18%)<br>Memory bits: 768/920448 (<1%) |
| Performance | 226 MHz |
| Latency | 15 clock cycles |

The design requires the input to be an 8 × 8 image, with 8-bit input data and 9-bit filter coefficient width. The output is an image of the same size.

### *Convolution Design Example*

Download the 3 × 3 2-D Convolutional Filter (**two_d_fir.zip**) design example from the Design Examples section of the Altera web site at http://www.altera.com**.**

## Discrete Cosine Transform (DCT)

The discrete cosine transform (DCT) is widely used in video and audio compression, for example in JPEG, MPEG video, and MPEG audio. It is a form of transform coding, which is the preferred method for compression techniques. Images tend to compact their energy in the frequency domain making compression in the frequency domain much more effective. This is an important element in compressing data, where the goal is to have a high data compression rate without significant degradation in the image quality.

### DCT Background

Similar to the discrete fourier transform (DFT), the DCT is a function that maps the input signal or image from the spatial to the frequency domain. It transforms the input into a linear combination of weighted basis functions. These basis functions are the frequency components of the input data.

For 1-D with input data *x*(`n`) of size `N`, the DCT coefficients *Y*(`k`) are:

$$Y(k) = \frac{\alpha(k)}{2}\sum_{n=0}^{N-1} x(n)\cos\left(\frac{(2n+1)\pi k}{2N}\right) \quad \text{for } 0 \leq k \leq N{-}1$$

where:

$$\alpha(k) = \sqrt{\frac{1}{N}} \quad \text{for } k = 0$$

$$\alpha(k) = \sqrt{\frac{2}{N}} \quad \text{for } 1 \leq k \leq N-1$$

For 2-D with input data *x*(`m`,`n`) of size `N` × `N`, the DCT coefficients for the output image, *Y*(`p`,`q`) are:

$$Y(p, q) = \frac{\alpha(p)\alpha(q)}{2}\sum_{m=0}^{N-1}\sum_{n=0}^{N-1} x(m, n)\cos\left(\frac{(2m+1)\pi p}{2N}\right)\cos\left(\frac{(2n+1)\pi q}{2N}\right)$$

where:

$$\alpha(p) = \sqrt{\frac{1}{N}} \quad \text{for } p = 0$$

$$\alpha(q) = \sqrt{\frac{1}{N}} \quad \text{for } q = 0$$

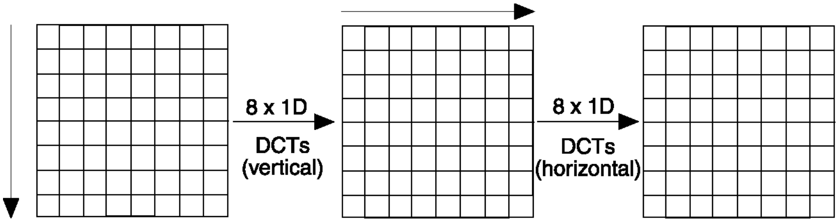
$$\alpha(p) = \sqrt{\frac{2}{N}} \quad \text{for } 1 \leq p \leq N-1$$

$$\alpha(q) = \sqrt{\frac{2}{N}} \quad \text{for } 1 \leq q \leq N{-}1$$

## 2-D DCT Algorithm

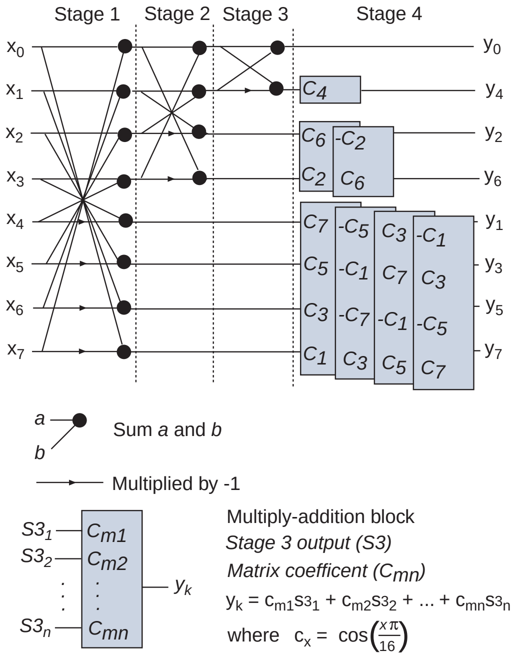
The 2-D DCT can be thought of as an extended 1-D DCT applied twice; once in the *x* direction and again in the *y* direction. Because the 2-D DCT is a separable transform, it is possible to calculate it using efficient 1-D algorithms. Figure 7–32 illustrates the concept of a separable transform.

Figure 7–32. A 2-D DCT is a Separable Transform



This section uses a standard algorithm proposed in [1]. Figure 7–33 shows the flow graph for the algorithm. This is similar to the butterfly computation of the fast fourier transform (FFT). Similar to the FFT algorithms, the DCT algorithm reduces the complexity of the calculation by decomposing the computation into successively smaller DCT components. The even coefficients ($y_0$, $y_2$, $y_4$, $y_6$) are calculated in the upper half and the odd coefficients ($y_1$, $y_3$, $y_5$, $y_7$) in the lower half. As a result of the decomposition, the output is reordered as well.

Figure 7–33. Implementing an N=8 Fast DCT



The following defines in matrix format, the 8-point 1-D DCT of Figure 7–33:

$$\left[Y_{1D}\right] = \left[x\right] \times \left[\mathrm{Add}_1\right] \times \left[\mathrm{Add}_2\right] \times \left[\mathrm{Add}_3\right] \times \left[C\right]$$

where:

[$x$] is the 1 × 8 input matrix

$$\left[\mathrm{Add}_1\right] = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 1 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & -1 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & -1 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & -1 \end{bmatrix}$$

$$\left[\mathrm{Add}_2\right] = \begin{bmatrix} 1 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & -1 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$

$$\left[\mathrm{Add}_3\right] = \begin{bmatrix} 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$

$$[C] = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & C_4 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & C_6 & -C_2 & 0 & 0 & 0 & 0 \\ 0 & 0 & C_2 & C_6 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & C_7 & -C_5 & C_3 & -C_1 \\ 0 & 0 & 0 & 0 & C_5 & -C_1 & C_7 & C_3 \\ 0 & 0 & 0 & 0 & C_3 & -C_7 & -C_1 & -C_5 \\ 0 & 0 & 0 & 0 & C_1 & C_3 & C_5 & C_7 \end{bmatrix}$$

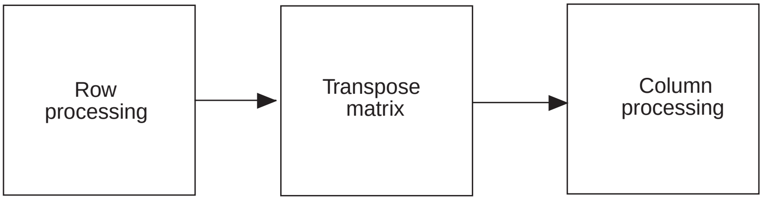
$$C_x = \cos\frac{\pi x}{16}$$

All of the additions in stages 1, 2 and 3 of Figure 7–32 appear in symmetric add and subtract pairs. The entire first stage is simply four such pairs in a very typical cross-over pattern. This pattern is repeated in stages 2 and 3. Multiplication operations are confined to stage 4 in the algorithm. This implementation is shown in more detail in the next section.

### DCT Implementation

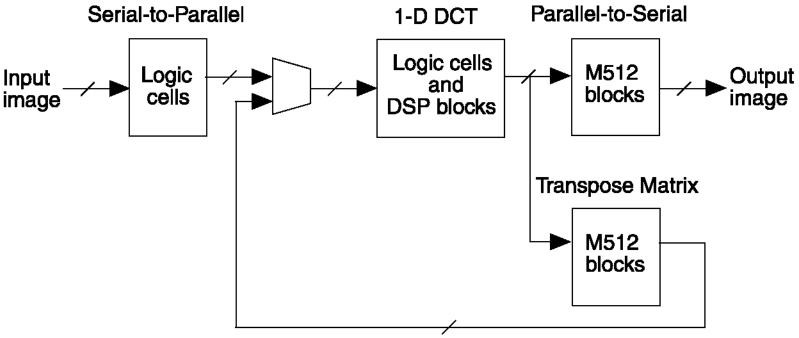
In taking advantage of the separable transform property of the DCT, the implementation can be divided into separate stages; row processing and column processing. However, some data restructuring is necessary before applying the column processing stage to the results from the row processing stage. The data buffering stage must transpose the data first. Figure 7–34 shows the different stages.

**Figure 7–34. Three Separate Stages in Implementing the 2-D DCT**



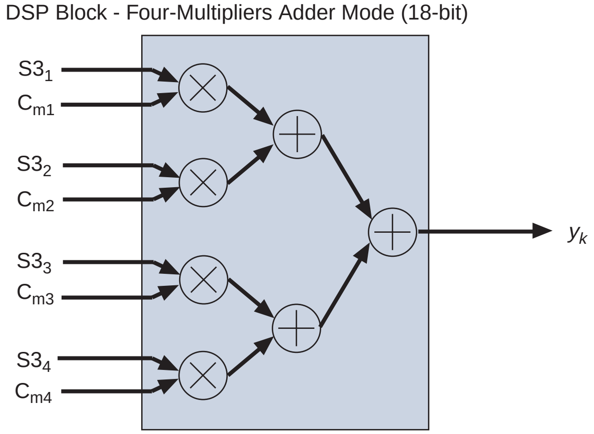
Because the row processing and column processing blocks share the same 1-D 8-point DCT algorithm, the hardware implementation shows this block as being shared. The DCT algorithm requires a serial-to-parallel conversion block at the input because it works on blocks of eight data points in parallel. There is also a parallel-to-serial conversion block at the output because the column processing stage generates the output image column-by-column. In order to have the output in the same order as the input (i.e., row-by-row), this conversion is necessary. Appropriate scaling needs to be applied to the completed transform but this can be combined with the quantization stage which often follows a DCT [1]. Figure 7–35 shows a top-level block diagram of this design.

*Figure 7–35. Block Diagram on Serial Implementation of 2-D DCT*



The implementation of the 1-D DCT block is based on the algorithm shown in Figure 7–33. The simple addition and subtraction operations in stages 1, 2 and 3 are implemented using logic cells. The multiply and multiply-addition operations in stage 4 are implemented using DSP blocks in the Stratix device in the simple multiplier mode, two-multiplier adder mode, and the four-multiplier adder mode. An example of the multiply-addition block is shown in Figure 7–36.

## Figure 7–36. Details on the Implementation of the Multiply-Addition Operation in Stage 4 of the 1-D DCT Algorithm



*Note to Figure 7–36:*

(1) Referring to Figure 7–33.$S3_n$ is an output from stage 3 of the DCT and $C_{mn}$ is a matrix coefficient. $C_x = \cos(x\pi/16)$.

### DCT Implementation Results

Table 7–18 shows the results of implementing a 2-D DCT with 18-bit precision, as shown in Figure 7–35.

**Table 7–18. 2-D DCT Implementation Results**

| | |
|---|---|
| Part | EP1S20F780 |
| Utilization | Lcell: 1717/18460 (9%)<br>DSP Block 9-bit element: 18/80 (22%)<br>Memory bits: 2816/1669248 (<1%) |
| Performance | 165 MHz |
| Latency | 80 clock cycles |

### DCT Design Example

Download the 2-D convolutional filter (**d_dct.zip**) design example from the Design Examples section of the Altera web site at www.altera.com**.**

# Arithmetic Functions

Arithmetic functions, such as trigonometric functions, including sine, cosine, magnitude and phase calculation, are important DSP elements. This section discusses the implementation of a simple vector magnitude function in a Stratix device.

## Background

Complex numbers can be expressed in two parts: real and imaginary.

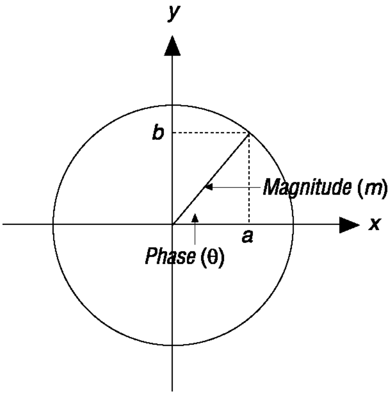
$$z = a + jb$$

Where:

`a` is the real part
`b` is the imaginary part
$j^2 = -1$

In a two-dimensional plane, a vector (`a`,`b`) with reference to the origin (0,0) can also be represented as a complex number. In essence, the x-axis represents the real part, and the y-axis represents the imaginary part (see Figure 7–37).

*Figure 7–37. Magnitude of Vector (a,b)*



Complex numbers can be converted to phase and amplitude or magnitude representation, using a Cartesian-to-polar coordinate conversion. For a vector (`a`,`b`), the phase and magnitude representation is the following:

$$\text{Magnitude } m = \sqrt{a^2 + b^2}$$

$$\text{Phase angle } \theta = \tan^{-1}(b/a)$$

This conversion is useful in different applications, such as position control and position monitoring in robotics. It is also important to have these transformations at very high speeds to accommodate real-time processing.

## Arithmetic Function Implementation

A common approach to implementing these arithmetic functions is using the coordinate rotation digital computer (CORDIC) algorithm. The CORDIC algorithm calculates the trigonometric functions of sine, cosine, magnitude, and phase using an iterative process. It is made up of a series of micro-rotations of the vector by a set of predetermined constants, which are powers of 2.

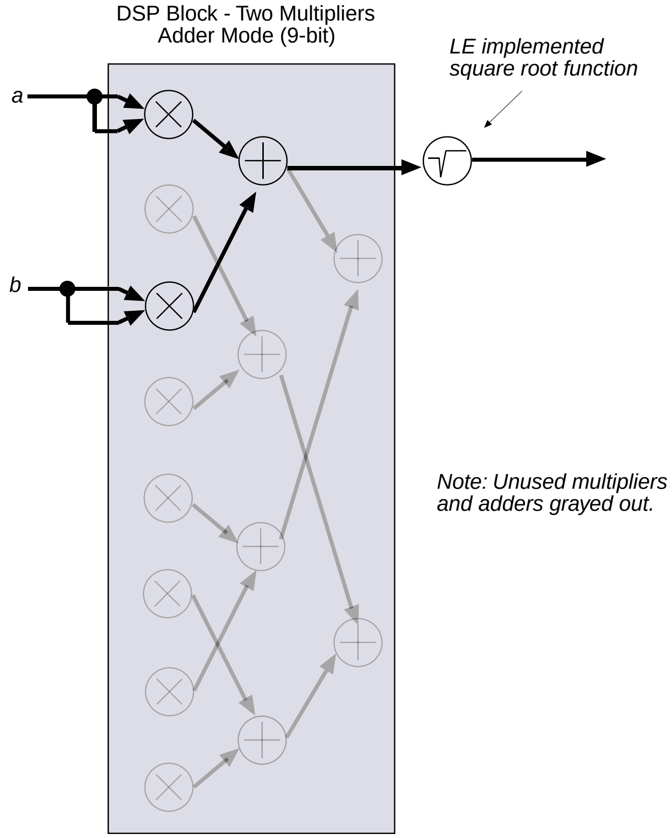
Using binary arithmetic, this algorithm essentially replaces multipliers with shift and add operations. In Stratix devices, it is possible to calculate some of these arithmetic functions directly, without having to implement the CORDIC algorithm.

This section describes a design example that calculates the magnitude of a 9-bit signed vector (`a`,`b`) using a pipelined version of the square root function available at the Altera IP Megastore. To calculate the sum of the squares of the input ($a^2 + b^2$), configure the DSP block in the two-multipliers adder mode. The square root function is implemented using an iterative algorithm similar to the long division operation. The binary numbers are paired off, and subtracted by a trial number. Depending on if the remainder is positive or negative, each bit of the square root is determined and the process is repeated. This square root function does not require memory and is implemented in logic cells only.

In this example, the input bit precision (`IN_PREC`) feeding into the square root macro is set to twenty, and the output precision (`OUT_PREC`) is set to ten. The number of precision bits is parameterizable. Also, there is a third parameter, `PIPELINE`, which controls the architecture of the square root macro. If this parameter is set to `YES`, it includes pipeline stages in the square root macro. If set to `NO`, the square root macro becomes a single-cycled combinatorial function.

Figure 7–38 shows the implementation the magnitude design.

**Figure 7–38. Implementing the Vector Magnitude Function**



### Arithmetic Function Implementation Results

Table 7–19 shows the results of the implementation shown in Figure 7–38 with the `PIPELINE` parameter set to `YES`. Table 7–20 shows the results of the implementation shown in Figure 7–38 with the `PIPELINE` parameter set to `NO`.

*Table 7–19. Vector Magnitude Function Implementation Results (PIPELINE=YES)*

| | |
|---|---|
| Part | EP1S10F780 |
| Utilization | Lcell: 497/10570 (4%)<br>DSP block 9-bit elements: 2/48 (4%)<br>Memory bits: 0/920448 (0%) |
| Performance | 194 MHz |
| Latency | 15 clock cycles |

*Table 7–20. Vector Magnitude Function Implementation Results (PIPELINE=NO)*

| | |
|---|---|
| Part | EP1S10F780 |
| Utilization | Lcell: 244/10570 (2%)<br>DSP block 9-bit elements: 2/48 (4%)<br>Memory bits: 0/920448 (0%) |
| Performance | 30 MHz |
| Latency | 3 clock cycles |

### Arithmetic Function Design Example

Download the Vector Magnitude Function (**magnitude.zip**) design example from the Design Examples section of the Altera web site at www.altera.com.

## Conclusion

The DSP blocks in Stratix and Stratix GX devices are optimized to support DSP functions requiring high data throughput, such as FIR filters, IIR filters and the DCT. The DSP blocks are flexible and configurable in different operation modes based on the application’s needs. The TriMatrix memory provides the data storage capability often needed in DSP applications.

The DSP blocks and TriMatrix memory in Stratix and Stratix GX devices offer performance and flexibility that translates to higher performance DSP functions.

## References

See the following for more information:

- *Optimal DCT for Hardware Implementation*
  M. Langhammer. Proceedings of International Conference on Signal Processing Applications & Technology (ICSPAT) '95, October 1995

- *Digital Signal Processing: Principles, Algorithms, and Applications*
  John G. Proakis, Dimitris G. Manolakis. Prentice Hall

- *Hardware Implementation of Multirate Digital Filters*
  Tony San. Communication Systems Design, April 2000

- *Application Note 73: Implementing FIR Filters in FLEX Devices*

- *Efficient Logic Synthesis Techniques for IIR Filters*
  M.Langhammer. Proceedings of International Conference on Signal Processing Applications & Technology (ICSPAT) '95, October 1995

# Section V. IP & Design Considerations

This section provides documentation on some of the IP functions offered by Altera for Stratix devices. (Also refer to the Intellectual Property section of the Altera web site for a complete offering of IP cores for Stratix devices.) The last chapter details design considerations for designers that are migrating from the APEX architecture.

This section contains the following chapters:

- Chapter 8, Double Data Rate I/O Signaling in Stratix & Stratix GX Devices
- Chapter 9. Using Soft Multipliers with Stratix & Stratix GX Devices
- Chapter 10. Implementing 10-Gigabit Ethernet Using Stratix Devices
- Chapter 11. Implementing SFI-4 in Stratix Devices
- Chapter 12. Transitioning APEX Designs to Stratix Devices

## Revision History

The table below shows the revision history for Chapters 8 through 12.

| Chapter(s) | Date / Version | Changes Made |
|---|---|---|
| 8 | April 2003<br>v1.0 | Added document to the Stratix Device Handbook. |
| 9 | April 2003<br>v1.0 | Added document to the Stratix Device Handbook. |
| 10 | April 2003<br>v1.0 | Added document to the Stratix Device Handbook. |
| 11 | April 2003<br>v1.0 | Added document to the Stratix Device Handbook. |
| 12 | April 2003<br>v1.0 | Added document to the Stratix Device Handbook. |

# 8. Double Data Rate I/O Signaling in Stratix & Stratix GX Devices

S52008-1.0

Chapter 8, Double Data Rate I/O Signaling in Stratix & Stratix GX Devcies replaces *AN 212: Double Data Rate I/O Signaling in Stratix & Stratix GX Devcies*.

## Introduction

Typical I/O architectures transmit a single data word on each positive clock edge and are limited to the associated clock speed using this protocol. To achieve a 400-megabits per second (Mbps) transfer rate, a system requires a 400-MHz clock. Many new applications have introduced a double data rate I/O (DDRIO) architecture as an alternative to single data rate (SDR) architectures. While SDR architectures capture data on one edge of a clock, the DDR architectures captures data on both edges of the clock, doubling the throughput for a given clock and accelerating performance. For example, a 200-MHz clock can capture a 400-Mbps data stream, enhancing system performance and simplifying board design.

Stratix™ and Stratix GX devices feature dedicated DDR I/O circuitry. This circuitry allows you to build applications that use DDR signaling, such as memory interfaces including DDR SDRAM, fast cycle random access memory (FCRAM), reduced latency DRAM I (RLDRAM I), and quad data rate static random access memory (QDR) as well as implement high-speed interface standards. For more information on RLDRAM II, please contact Altera Applications.

This application note first describes the DDR I/O capabilities of Stratix and Stratix GX devices, including I/O element (IOE) details to be used in general applications. It then details the DQS dedicated circuitry that Stratix and Stratix GX FPGAs offer for use in external memory interfaces.

☞ This application note should be used in conjunction with the *External RAM Interfacing* section from the *Stratix FPGA Family Data Sheet* or the *Stratix GX FPGA Family Data Sheet*. If you are designing a memory controller, see *Appendix B* of *DDR SDRAM Controller User Guide*.

## DDR I/O Elements

Each IOE contains six registers and one latch. Two registers and a latch are used for input, two registers are used for output, and two registers are used for output enable control. The functionality of these registers is described below for input, output, and bidirectional pin configuration.

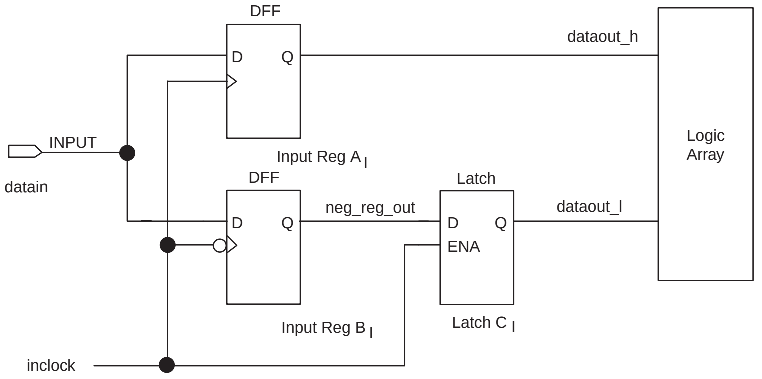
You can use the DDR I/O elements by instantiating the following modules in the MegaWizard® Plug-In Manager:

- `altddio_in` for double data rate input interface
- `altddio_out` for double data rate output interface
- `altddio_bidir` for double data rate bidirectional interface

## Input Configuration

When the IOE is configured as an input pin, input registers $A_I$, $B_I$, and latch $C_I$ implement the input path for DDR I/O. Figure 8–1 shows an IOE configured for DDR inputs for a Stratix or Stratix GX device.

*Figure 8–1. Input DDR I/O Path Configuration*

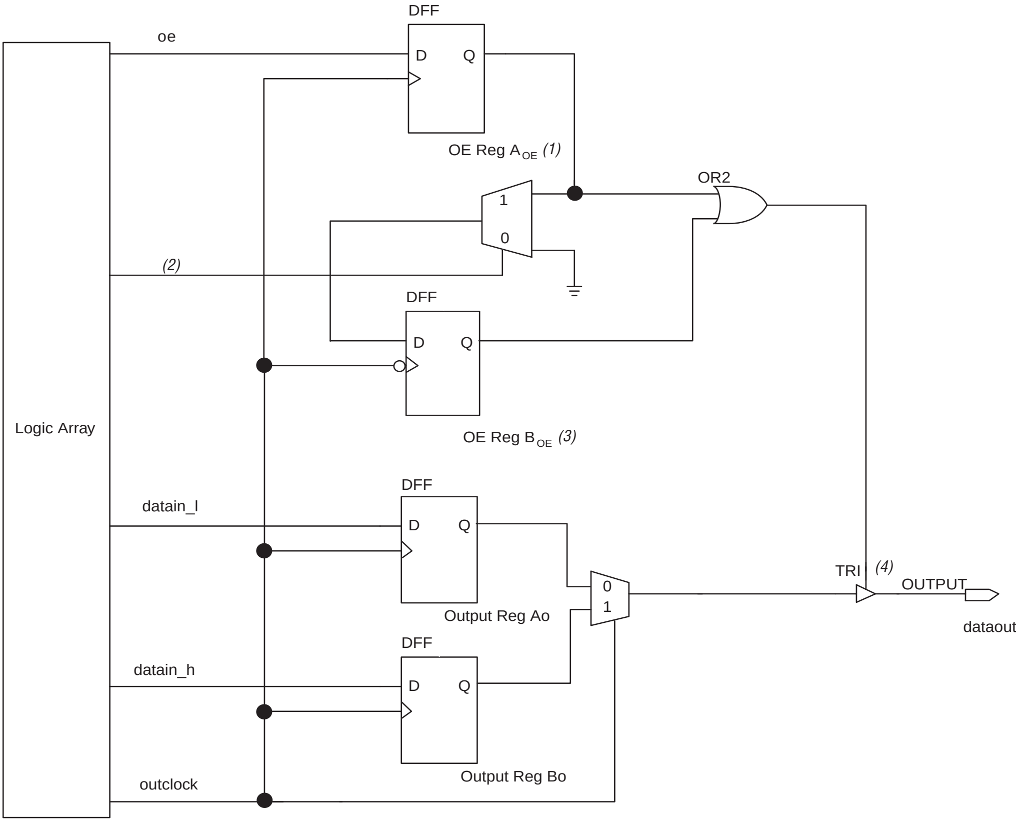


On the falling edge of the clock, the negative-edge triggered register $B_I$ acquires the first data bit. On the corresponding rising edge of the clock, the positive-edge triggered register $A_I$ acquires the second data bit. For a successful data transfer to the logic array, the latch $C_I$ synchronizes the data from register $B_I$ to the positive edge of the clock.

## Output Configuration

The dedicated output registers for Stratix and Stratix GX devices are labeled $A_O$ and $B_O$. These positive-edge triggered registers and a multiplexer are used for implementing the output path for DDR I/O. Figure 8–2 shows the IOE configuration for DDR outputs in Stratix and Stratix GX devices.

*Figure 8–2. Output DDR I/O Path Configuration*



*Notes to Figure 8–2:*

(1) Register $A_{0E}$ generates the enable signal for general-purpose DDR I/O applications.

(2) This select line corresponds to the **Delay Switch-on by a half clock cycle** option in the MegaWizard Plug-In Manager.

(3) Register $B_{0E}$ generates the delayed enable signal for DDR SDRAM applications.

(4) The tristate is by default active high. You can, however, design it to be active low.

On the positive edge of the clock, two consecutive data bits are captured in registers $A_0$ and $B_0$. The outputs of these two registers are fed to the inputs of a 2-to-1 multiplexer, which uses the output register clock as its control signal. A high clock selects the data in register $B_0$, and a low level of the clock selects the data in register $A_0$. This process doubles the data rate.

## Bidirectional Configuration

Input and output registers are independent of each other, enabling the bidirectional DDR I/O path to be implemented entirely in the I/O element. The bidirectional configuration includes an input path, an output path, and two output enable registers. The bidirectional path consists of two data flow paths: input path active and output path active.

When the input path is active, the output enable disables the tri-state buffer, which prevents data from being sent out on the output path. Disabling the tri-state buffer prevents contention at the I/O pin. The input path behaves like the input configuration as shown in Figure 8–1 on page 8–2.

During output transactions, the output enable register $A_{OE}$ controls the flow of data from the output registers. During outgoing transactions, the bidirectional configuration behaves like the output configuration. (See Figure 8–2.)

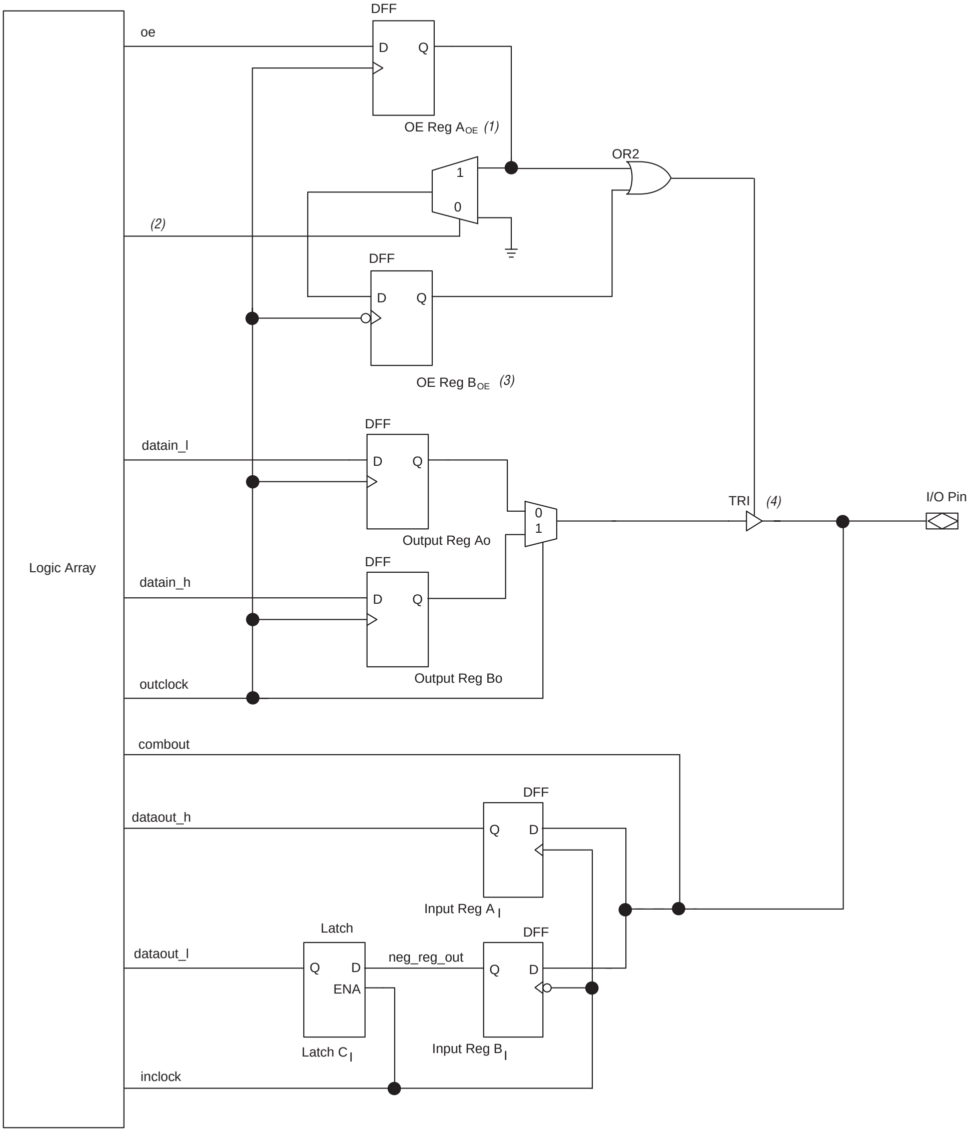
The second output enable register ($B_{OE}$) is used for DDR SDRAM interfaces. This negative-edge register extends the high-impedance state of the pin by a half clock cycle. This option is useful to provide the write preamble for the DQS strobe in the DDR SDRAM interfaces. This feature is enabled by using the **Delay switch on by a half clock cycle** option in the `altddio_bidir` megafunction in the Quartus II software.

You can bypass the input registers and latch to get a combinatorial output `combout` from the pin going into the Stratix device. Furthermore, the input data ports (`dataout_h` and `dataout_l`) can be disabled. These features are especially useful for generating data strobes like DQS. See Figure 8–3

Figure 8–3 shows the bidirectional DDR I/O configuration for Stratix and Stratix GX devices.

To see how the output enable is extended by a half clock cycle, see Figure 8–14 on page 8–26.

*Figure 8–3. Bidirectional DDR I/O Path Configuration*



*Notes to Figure 8–3:*

(1) Register A$_{0E}$ generates the enable signal for general-purpose DDR I/O applications.

(2) This select line corresponds to the **Delay Switch-on by a half clock cycle** option in the MegaWizard Plug-In Manager.

(3) Register B$_{0E}$ generates the delayed enable signal for DDR SDRAM applications.

(4) The tristate is by default active high. You can, however, design it to be active low.

For more information about clock signals and output enable signals for Stratix or Stratix GX devices, see the *Stratix FPGA Family Data Sheet* or the *Stratix GX FPGA Family Data Sheet*.

## DDR I/O Timing

Figure 8–4 shows the functional timing waveform for the input path. The signal names are the port names used in the `altddio_in` megafunction. The signal `datain` is the input from the pin to the DDR circuitry. `neg_reg_out` is the output of register $B_I$. `dataout_h` is the output of latch $C_I$ and `dataout_l` is the output of register $A_I$. `dataout_h` and `dataout_l` feed the core and illustrate the conversion of the data from a DDR implementation to positive-edge triggered data.

*Figure 8–4. DDR I/O Input Timing Waveform*

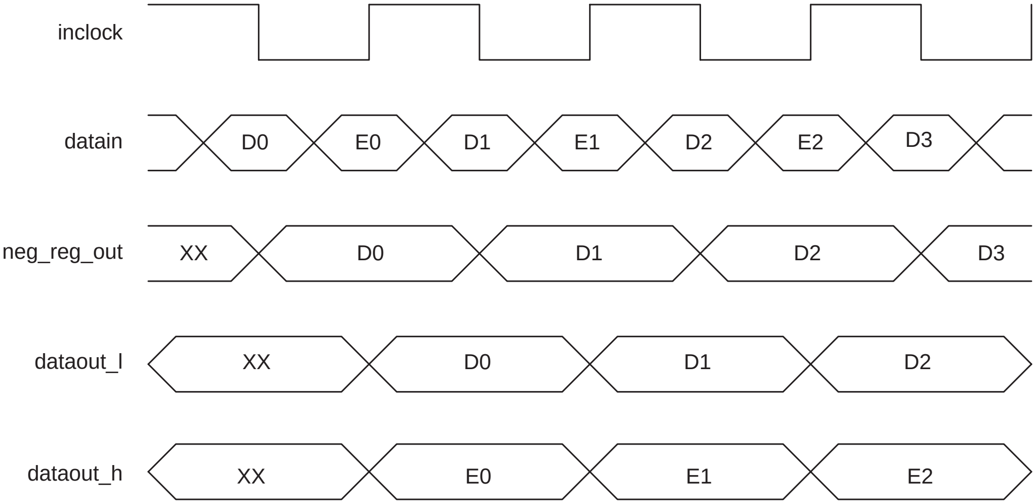
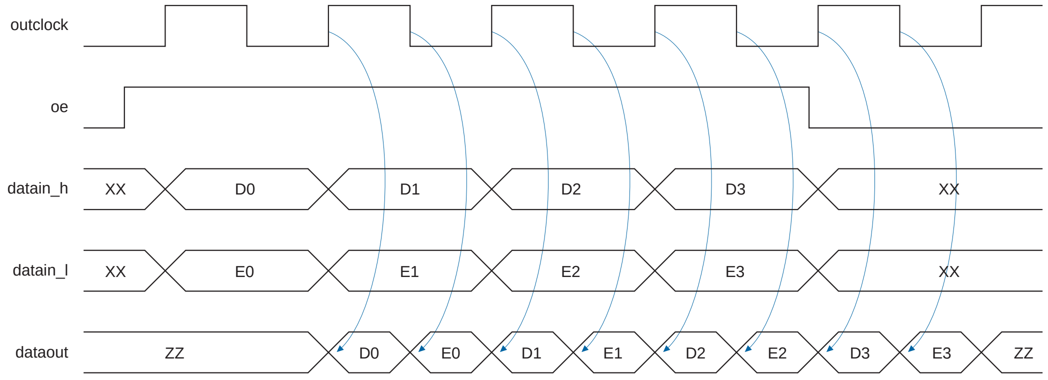


Figure 8–5 shows a functional timing waveform example for the output path with the output enable registered. In this particular example, the **Delay switch-on by half clock cycle** is not turned on, hence the second output enable register ($B_{OE}$) is not used. The output enable `OE` is active high and can be driven from a pin or internal logic. The data signals `datain_l` and `datain_h` are driven from the logic array to output registers `Ao` and `Bo`. The signal `dataout` is the output from the DDR circuitry to the pin.

*Figure 8–5. DDR I/O Output Timing Waveform*



## DDR I/O Applications

This section provides information on the following DDR I/O applications:

- DDR SDRAM, FCRAM, RLDRAM I & II
- QDR SRAM
- High-speed interface applications

### DDR SDRAM, FCRAM & RLDRAM I & II

DDR SDRAM, FCRAM, and RLDRAM I & II can write and read data at twice the clock rate by capturing data on both the positive and negative edge of a clock. DDR SDRAM is a JEDEC standard and the FCRAM standard is developed by Fujitsu and Toshiba. FCRAM uses a proprietary pipeline method and precharge to help reduce random access cycle times. RLDRAM I & II is developed by Micron and Infineon Technologies and has a lower row access time and initial latency. These DDR memory interfaces use a variety of I/O standards such as SSTL-II, 1.8-V HSTL and LVTTL/LVCMOS.

See the *DDR SDRAM Controller User Guide* for more information.

### QDR SRAM

The QDR SRAM standard is defined jointly by Cypress, IDT and Micron. QDR SRAMs have separate DDR read and write ports that can pass data concurrently. The combination of concurrent transactions and DDR signaling allow for data to be passed four times faster than conventional SRAMs. The I/O standards used for QDR SRAMs are 1.5-V HSTL class I and II.

For more information on QDR SRAM, see Chapter 2, QDR SRAM Controller Reference Design for Stratix & Stratix GX Devices.

### High-Speed Interface Applications

High-speed interface applications can use various differential standards such as LVDS, LVPECL, PCML, or Hypertransport as the transfer medium. These standards often use DDR data. Stratix and Stratix GX devices can implement high-speed standards either by using the dedicated differential I/O SERDES blocks or by bypassing SERDES and using the DDR I/O circuitry in SERDES bypass mode. DDR I/O megafunctions, PLLs, and shift registers are all used in SERDES functionality.

For more information about the differential I/O capabilities and SERDES bypass, see Chapter 4, Using Selectable I/O Standards in Stratix & Stratix GX Devices and Chapter 5, Using High-Speed Differential I/O Interfaces in Stratix Devices.

## External Memory Support in Stratix

DDR SDRAM, DDR FCRAM, and RLDRAM I memory devices, referred to as DDR memory for the rest of this Application Note, rely on the use of a data strobe signal, called DQS, to achieve high speed operation. When writing to a DDR SDRAM or DDR FCRAM device, the memory controller from the Stratix device must generate a DQS signal that is center-aligned with DQ, the data signal. RLDRAM I does not use the DQS signal for writing to the memory device. When reading from the memory device, data coming into the Stratix device is edge-aligned with respect with the DQS signal such that the Stratix device needs to shift the DQS before using it to sample the read data. DDR SDRAM and RLDRAM I require a 90 degree phase shift in the read direction while DDR FCRAM uses a 72 degree shift. Stratix devices contain dedicated circuitry to shift the incoming DQS signals by either 72 or 90 degrees. This DQS phase shift circuitry uses a frequency reference to generate control signals for the delay lines on each of the dedicated DQS pins, allowing it to compensate for process, voltage, and temperature (PVT) variations. This frequency reference has to be supplied through one of the dedicated clock input pin as detailed on page 8–11. The dedicated circuitry also gives you comfortable and consistent margins for your data sampling window.

For more information on DDR SDRAM, refer to JEDEC standard publication JESD 79 at **www.jedec.org**. For details on RLDRAM I, go to **www.rldram.com**. The DDR FCRAM devices are developed by Fujitsu and Toshiba.

## DQS & DQ Pins

In every Stratix device, the I/O banks at the top (I/O banks 3 and 4) and bottom (I/O banks 7 and 8) of the device support DDR memory I/O pins. These pins support DQS signals with DQ bus modes of ×8, ×16, or ×32. For ×8 mode, there are up to 20 groups of programmable DQS and DQ pins—10 groups in I/O banks 3 and 4 and 10 groups in I/O banks 7 and 8. The EP1S10 device supports up to 16 groups total. See Table 8–1. Each group consists of one DQS pin and a set of eight DQ pins, see Figure 8–6. Each DQS pin drives the set of eight DQ pins within that group.

The DQ and DQS pins must be configured as bidirectional pins to enable the DQS phase shift circuitry. If you only want to use the DQ and DQS pins as inputs, you need to set the output enable of the `altddio_bidir` module to GND.

For ×16 mode, there are up to eight groups of programmable DQS and DQ pins—four groups in I/O banks 3 and 4, and four groups in I/O banks 7 and 8. The EP1S20 device supports seven ×16 groups. The EP1S10 device does not support ×16 mode. All other devices support the full eight groups. See Table 8–1 for more details on what each device supports. Each group consists of one DQS and 16 DQ pins. In ×16 mode, DQST1, DQST3, DQST6, and DQST8, on the top side of the device, and DQSB1, DQSB3, DQSB6, and DQSB8, on the bottom side of the device, are the dedicated DQS pins for the ×16 mode. DQST2, DQST7, DQSB2, and DQSB7 are the dedicated DQS pins for the ×32 mode. You can use any of the column I/O pins for the DM signals.

In Stratix devices, ×16 mode uses 1 DQS pin to drive 16 DQ pins and ×32 mode uses one DQS pin to drive 32 DQ pins. If your ×16 memory device uses two DQS pins where each DQS pin is associated with 8 DQ pins, you need to configure the Stratix FPGAs to use two sets of ×8 mode. Similarly if your ×32 memory device uses four DQS pins where each DQS pin is associated with eight DQ pins, you need to configure the Stratix FPGAs to use four sets of ×8 mode .

***Table 8–1. DQS & DQ Bus Mode Support*** *Note (1)*

| Device | Package | Number of ×8 Groups | Number of ×16 Groups | Number of ×32 Groups |
|---|---|---|---|---|
| EP1S10 | 672-pin BGA<br>672-pin FineLine BGA | 12 *(2)* | 0 | 0 |
| | 484-pin FineLine BGA<br>780-pin FineLine BGA | 16 *(3)* | 0 | 4 |

**Table 8–1. DQS & DQ Bus Mode Support** *Note (1)*

| Device | Package | Number of ×8 Groups | Number of ×16 Groups | Number of ×32 Groups |
|---|---|---|---|---|
| EP1S20 | 484-pin FineLine BGA | 18 *(4)* | 7 | 4 |
| | 672-pin BGA<br>672-pin FineLine BGA | 16 *(3)* | 7 *(5)* | 4 |
| | 780-pin FineLine BGA | 20 | 7 *(5)* | 4 |
| EP1S25 | 672-pin BGA<br>672-pin FineLine BGA | 16 *(3)* | 8 | 4 |
| | 780-pin FineLine BGA<br>1,020-pin FineLine BGA | 20 | 8 | 4 |
| EP1S30 | 956-pin BGA<br>780-pin FineLine BGA<br>1,020-pin FineLine BGA | 20 | 8 | 4 |
| EP1S40 | 956-pin BGA<br>1,020-pin FineLine BGA<br>1,508-pin FineLine BGA | 20 | 8 | 4 |
| EP1S60 | 956-pin BGA<br>1,020-pin FineLine BGA<br>1,508-pin FineLine BGA | 20 | 8 | 4 |
| EP1S80 | 956-pin BGA<br>1,508-pin FineLine BGA<br>1,923-pin FineLine BGA | 20 | 8 | 4 |

***Notes to Table 8–1:***

(1) See Chapter 4, Using Selectable I/O Standards in Stratix & Stratix GX Devices for $V_{REF}$ guidelines.

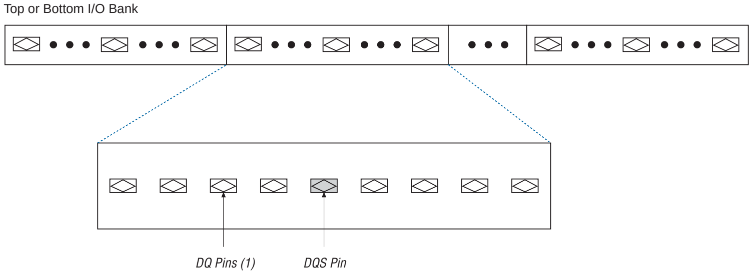
(2) These packages have six groups in I/O banks 3 and 4 and six groups in I/O banks 7 and 8.

(3) These packages have eight groups in I/O banks 3 and 4 and eight groups in I/O banks 7 and 8.

(4) This package has nine groups in I/O banks 3 and 4 and nine groups in I/O banks 7 and 8.

(5) These packages have three groups in I/O banks 3 and 4 and four groups in I/O banks 7 and 8.

*Figure 8–6. Stratix Device DQ & DQS Groups in ×8 Mode*



*Note to Figure 8–6:*

(1) There are at least eight `DQ` pins per group. Some devices may have more.

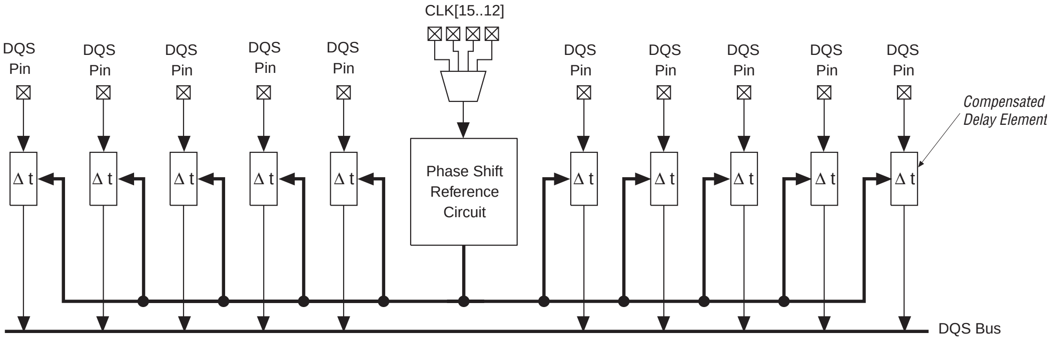
You can also create a design other than ×8, ×16, or ×32 mode. Quartus II will use the next larger mode with the unused DQ pins available as regular use I/O pins. For example, if you create a design for ×9 mode, (9 DQ pins driven by 1 DQS pin) Stratix will implement a ×16 mode with 7 DQ pins unconnected to the DQS bus.

## DQS Phase Shift Circuitry

A single phase shifting circuit is located on the I/O banks on the top (I/O banks 3 and 4) and bottom (I/O banks 7 and 8) of the Stratix device. The phase shifting circuit on the top of the device can control all ten DQS pins located at the top of the device and the phase shifting circuit on the bottom of the device can control all ten DQS pins located on the bottom of the device. All ten DQS pins on either the top or bottom of the device must be shifted by the same degree amount. For example, all ten DQS pins on the top of the device can be shifted by 90 degrees and all ten DQS pins on the bottom of the device can be shifted by 72 degrees. You cannot have both a phase shift of 90 degrees and 72 degrees on the top of the device and likewise for the bottom of the device.

In order to generate the correct phase shift, a clock signal with the same frequency as the DQS signal will need to be provided to the DQS phase shift circuitry. You can choose anyone of the following `CLK[15..12]p` clock pins to feed the phase circuitry on the top of the device (I/O banks 3 and 4) or choose anyone of the `CLK[7..4]p` clock pins to feed the phase circuitry on the bottom of the device (I/O banks 7 and 8). When using both the top and bottom phase shift circuits, two separate clocks will need to be used to generate the appropriate phase shift. The phase shift circuitry needs a maximum of 256 clock cycles to calculate the correct phase shift. When using the DQS circuitry, the data will not be properly captured if it is sent during this 256 clock cycle time. Figure 8–7 shows how the incoming DQS signal is shifted using the phase shift circuitry.

*Figure 8–7. Phase Control of DQS Pins*



*Note to Figure 8–7*

(1) Clock pins `CLK[15..12]p` feed the phase circuitry on the top of the device and clock pins `CLK[7..4]p` feed the phase circuitry on the bottom of the device.

The DQS Phase Shift Circuitry is only used when reading from the DDR SDRAM, DDR FCRAM, and RLDRAM I devices. Due to the Stratix DDR IOE structure, you need to also invert the incoming DQS signal to ensure proper data transfer. As shown in Figure 8–1, register $A_I$ is clocked by the rising edge of inclock, register $B_I$ is clocked by the falling edge of `inclock`, and latch $C_I$ is opened when `inclock` = 1. In a DDR memory read operation, the last data coincides with DQS being low. If you do not invert the DQS pin, you will not get this last data as the latch does not open until the next rising edge of the DQS signal. Figure 8–13 shows a proper read operation with the DQS signal inverted after the 90 degree shift.

If you are using a Stratix PLL to multiply an input clock to create a higher rate clock for the DDR memory interface, you need to feed this multiplied clock to an external clock pin and route in on the board to the reference clock input of the DQS phase shift circuitry. If a full rate clock is available as an input to the Stratix device the same clock can feed both the DQS phase shift circuitry and the PLL via the same clock input pin. You do not need to worry about the phase of the input clock to the DQS phase shift circuitry with respect to other system clocks in the device. The DQS phase shift circuitry only needs the frequency of the clock to create the degree shift amount.

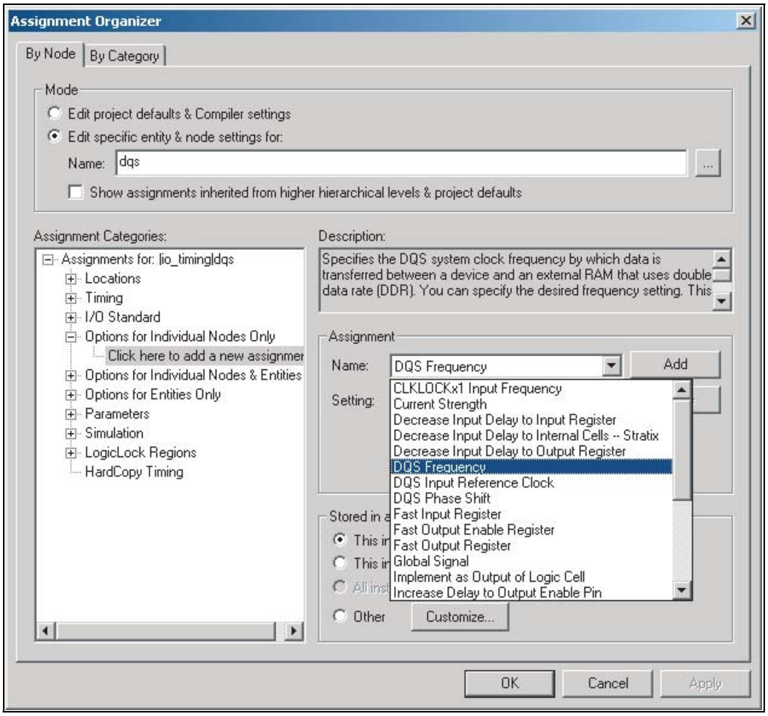
## Quartus II Software Support

To create a memory controller interface using the DQ and DQS pins, you need to use the `altddio_bidir` megafunction. The DQ and DQS pins must be used as bidirectional pins if you want to use the DQS phase shift circuitry. However, you can set the output enable of the `altddio_bidir` to ground if you just want to input edge-aligned data. You also need to use three logic options for the DQS pin(s) that are available from the Assignment Organizer. Quartus II has the capability to automatically place the DQ and DQS pins once the logic options are set for the DQS pin(s). The section details the three logic options, the $V_{REF}$ constraints and the on-chip termination constraints for the DQ and DQS pins.

## Quartus II Memory Interface Logic Options

There are three logic options that you need to set in order to your DQS pin(s) to make use of the dedicated phase shifting circuitry: **DQS Frequency, DQS Input Reference Clock,** and **DQS Phase Shift**. These logic options can be found in the Assignment Organizer under **Options for Individual Nodes Only**. See Figure 8–8 to see where these options are located in the Assignment Organizer.

*Figure 8–8. Logic Options for the DQS Pin(s) in the Assignment Organizer*



Mode: ● Edit specific entity & node settings for:

Name: dqs

Description: Specifies the DQS system clock frequency by which data is transferred between a device and an external RAM that uses double data rate (DDR). You can specify the desired frequency setting. This

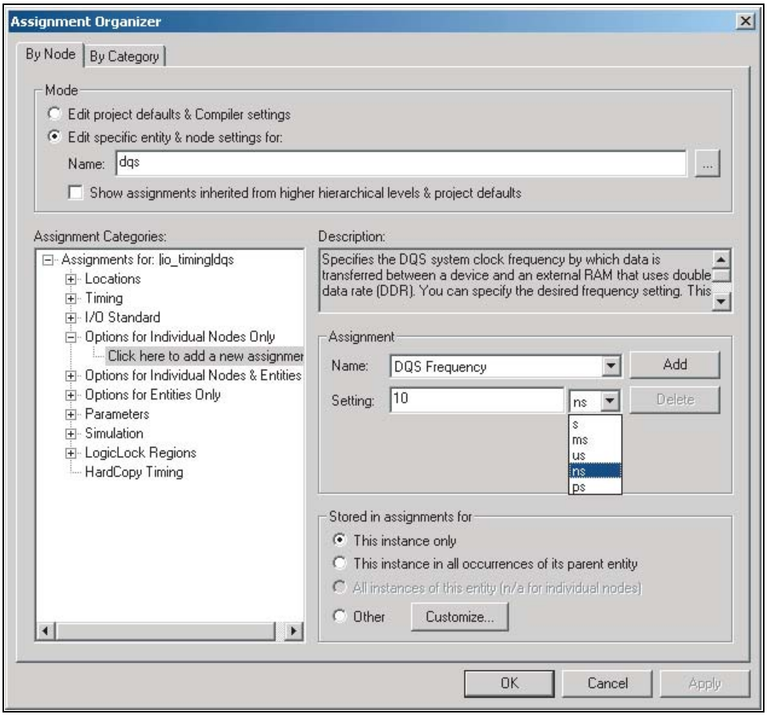
Assignment Name: DQS Frequency

The DQS frequency should be set to the frequency of the incoming DQS signal. See Figure 8–9 on how to set the **DQS frequency** option for your DQS pin.

If this frequency is a result of PLL multiplication, one PLL output has to be routed on the board back to the device, since the input to the DQS phase shift circuitry must come from a clock pin. You can either use an extra PLL output or use one of the clock outputs to the memory (CK or CK#) for this purpose. In the example design on page 8–19, `ref_clk` is used as the **DQS Reference Input Clock**. This is because of the `input_clk` is multiplied by 2 and there are no input clocks in the design running at the DQS frequency. You do not need to connect this `ref_clk` pin to any logic in the design if only used for the DQS shifting purpose. The phase relationship between this DQS Reference Input Clock and other system clocks in the design is unimportant. See Figure 8–10 on how to set the **DQS Reference Input Clock**.

If the PLL input frequency is the same as the output clock to the memory device, you can set the input pin to the PLL as your DQS Reference Input Clock.

*Figure 8–9. DQS Frequency Setting*


Mode:
- ○ Edit project defaults & Compiler settings
- ● Edit specific entity & node settings for:

Name: dqs

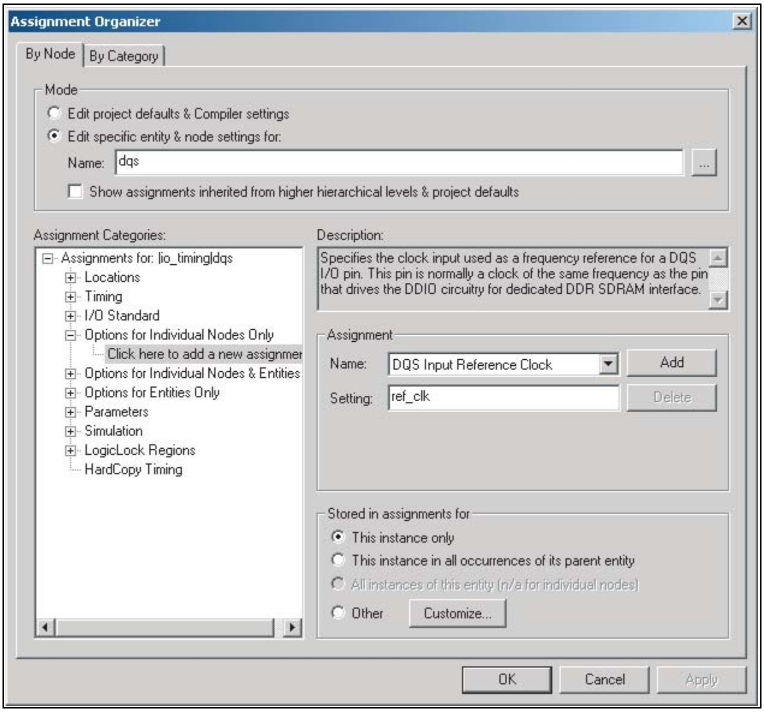
☐ Show assignments inherited from higher hierarchical levels & project defaults

Description:
Specifies the DQS system clock frequency by which data is transferred between a device and an external RAM that uses double data rate (DDR). You can specify the desired frequency setting. This

Assignment:
- Name: DQS Frequency
- Setting: 10 ns

Stored in assignments for:
- ● This instance only
- ○ This instance in all occurrences of its parent entity
- ○ All instances of this entity (n/a for individual nodes)
- ○ Other

*Figure 8–10. DQS Input Reference Clock Setting*



○ Edit project defaults & Compiler settings
● Edit specific entity & node settings for:
Name: dqs
☐ Show assignments inherited from higher hierarchical levels & project defaults

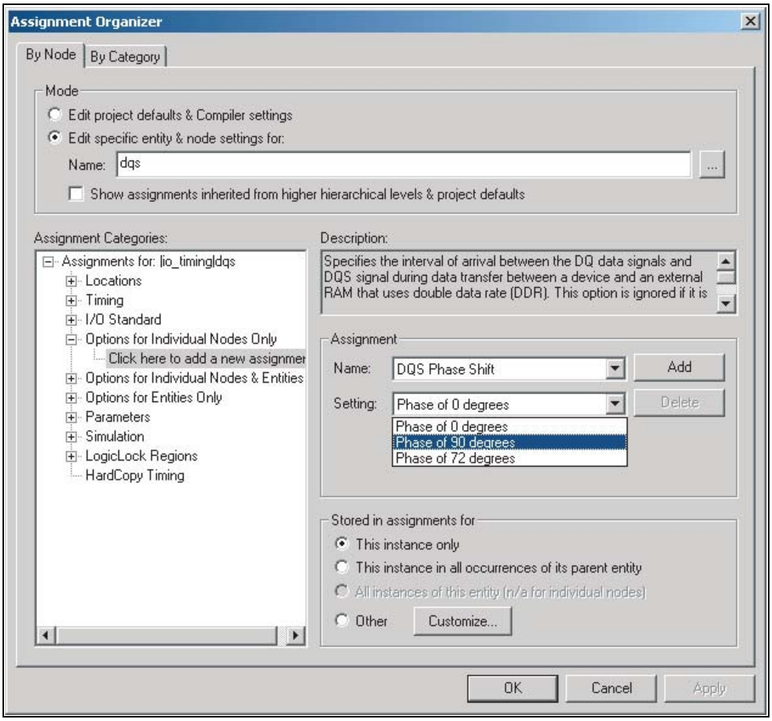
Specifies the clock input used as a frequency reference for a DQS I/O pin. This pin is normally a clock of the same frequency as the pin that drives the DDIO circuitry for dedicated DDR SDRAM interface.

Name: DQS Input Reference Clock
Setting: ref_clk

● This instance only
○ This instance in all occurrences of its parent entity
○ All instances of this entity (n/a for individual nodes)
○ Other

The DQS Phase Shift logic option gives the user the option of selecting 90 degrees for DDR SDRAM and RLDRAM I, or 72 degrees for DDR FCRAM, shown in Figure 8–11. You also have a choice of 0 degree DQS Phase Shift for interfacing with other devices that send data center-aligned with respect to the data strobe.

*Figure 8–11. DQS Phase Shift Settings*



Mode: ● Edit specific entity & node settings for:

Name: dqs

Assignments for: |io_timing|dqs

Description: Specifies the interval of arrival between the DQ data signals and DQS signal during data transfer between a device and an external RAM that uses double data rate (DDR). This option is ignored if it is

Assignment

Name: DQS Phase Shift

Setting: Phase of 0 degrees

Stored in assignments for: ● This instance only

## $V_{REF}$ Constraints

Quartus II only allows a maximum of 20 outputs or bidirectional pins per dedicated $V_{REF}$ pin. There are exceptions for bidirectional pins that share different output enables. For more information, refer to IO pin placement guidelines section in Chapter 4, Using Selectable I/O Standards in Stratix & Stratix GX Devices.

## On-Chip Termination

The Stratix device family offers the Terminator Technology whereby you can use on-chip termination in lieu of external termination. You can also apply on-chip termination on the DQ and DQS pins. However, you must ensure you do not violate the maximum current supported per group of 10 I/O pins as specified in Chapter 4, Using Selectable I/O Standards in Stratix & Stratix GX Devices for details.

## Implementing the DQS & DQ Interfaces

This section describes an example design to enable the DQS phase shift circuitry. You can use the design as a drop-in solution for your I/O interface with your own memory controller. You can also modify the design to suit your needs in interfacing with your chosen memory device.

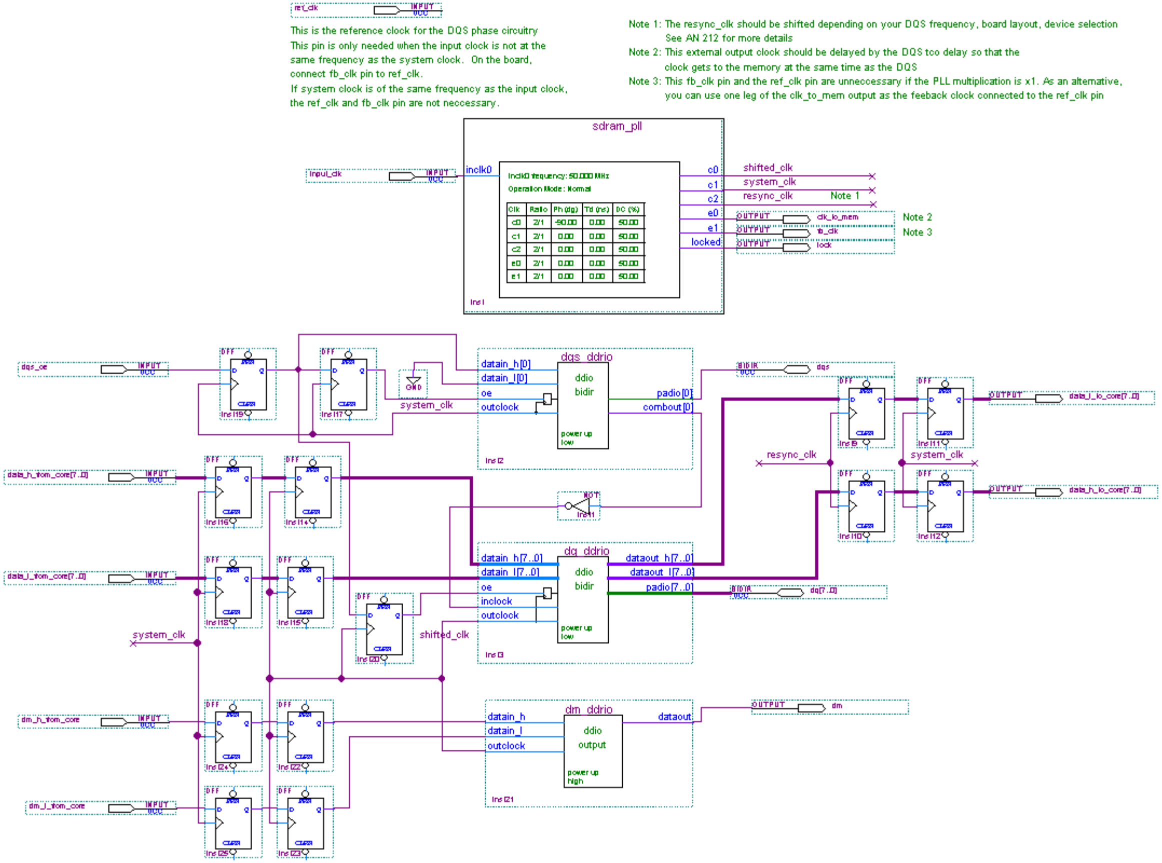
Go to **www.altera.com** to download the design either in VHDL or Verilog HDL.

### Design Example Overview

The design incorporates extra clocks that may not be needed for your application. These extra clocks are marked as optional in Table 8–2 on page 8–20.

Figure 8–12 shows an example design to properly implement the I/O interface of DDR SDRAM and FCRAM memory interfaces. See Table 8–2 for pin descriptions.

*Figure 8–12. DDR SDRAM & FCRAM Memory Interface*



This is the reference clock for the DQS phase circuitry
This pin is only needed when the input clock is not at the same frequency as the system clock. On the board, connect fb_clk pin to ref_clk.
If system clock is of the same frequency as the input clock, the ref_clk and fb_clk pin are not neccessary.

Note 1: The resync_clk should be shifted depending on your DQS frequency, board layout, device selection
See AN 212 for more details

Note 2: This external output clock should be delayed by the DQS tco delay so that the clock gets to the memory at the same time as the DQS

Note 3: This fb_clk pin and the ref_clk pin are unneccessary if the PLL multiplication is x1. As an alternative, you can use one leg of the clk_to_mem output as the feeback clock connected to the ref_clk pin

*Table 8–2. Pin Descriptions for Example Design in Figure 8–12*

| Pin name | Direction | Functional Description |
|---|---|---|
| `input_clk` | Input clock pin | Input clock to the PLL. If the frequency of this clock is the same as the DQS frequency, this pin also feeds the DQS phase shift circuitry. Otherwise, you need the `ref_clk` pin. |
| `ref_clk` | Extra input clock for DQS phase shift | Input clock to the DQS phase shift circuitry. Only needed if the `input_clk` is multiplied to get the specified DQS frequency. This pin is optional. |
| `clk_to_mem` | Output clock | Output clock to feed the `CK` and `CK#` ports of the DDR SDRAM or FCRAM device. This pin is set to be a differential SSTL-2 output. |
| `fb_clk` | Output feedback clock | Only needed if the `input_clk` is multiplied to get the specified DQS frequency. On the board, the `fb_clock` is looped back to the `ref_clk` pin. This pin is optional. |
| `dqs_oe` | Input from logic array | Output enable for the `DQS_DDRIO` module. A unregistered version of this signal is connected to the `datain_h` of the `DQS_DDRIO` module. |
| `data_h_from_core` | Input from logic array | This port contains the data to be output through the DQ pins on the rising edge of the system clock. |
| `data_l_from_core` | Input from logic array | This port contains the data to be output through the DQ pins on the falling edge of the system clock. |
| `dm_h_from_core` | Input from logic array | This port contains the data mask to be output through the DM pins on the rising edge of the system clock. |
| `dm_l_from_core` | Input from logic array | This port contains the data mask to be output through the DM pins on the falling edge of the system clock. |
| `dqs` | Bidirectional | This port connects to the DQS pin in the DDR SDRAM and FCRAM device. |
| `dq` | Bidirectional | This port connects to the DQ pins in the DDR SDRAM and FCRAM device. |
| `dm` | Output | This port connects to the DM pin in the DDR SDRAM and FCRAM device. |
| `lock` | Output | Indicates that the PLL is locked. |
| `data_h_to_core` | Input to logic array | This port contains the data that was captured on the rising edge of the shifted-and-inverted DQS signal. The data is then ready to be resynchronized to the system clock. |
| `data_l_to_core` | Input to logic array | This port contains the data that was captured on the falling edge of the shifted-and-inverted DQS signal. The data is then ready to be resynchronized to the system clock. |

The PLL in this design is used to generate the following signals:

- Output clock to the memory device.
  This clock goes to the pin `clk_to_mem`. You need to add some PLL time delay to match the delay of the output pin to the `dqs` $t_{co}$ delay. The pin is also assigned to use the differential SSTL I/O standard. For example, if the `clk_to_mem` $t_{CO}$ = 1.444 ns and the `dqs` $t_{CO}$ = 2.799 ns, you need to add a time delay of 1.355 ns for the `clk_to_mem` output in the `altpll` MegaWizard Plug-In Manger.
- Feedback clock to the DQS reference input clock.
  This output clock goes to the pin `fb_clk`. This is only needed if you are not using the full-rate clock in the system as your DQS frequency. On the board, you need to route this output pin to the input pin `ref_clk`. You can also use one of the leg of `clk_to_mem` pin for this purpose. The phase of this clock going into the `ref_clk` is unimportant.
- System clock.
  This clock is named `system_clk`. This is the system clock that is used to clock the memory controller. Depending on your board traces, you may need to use the negative edge to clock the memory controller. "Re-synchronization Calculation" on page 8–28
- 90 degree shifted clock to generate the center-aligned data for writing.
  This clock is named `shifted_clk`. This clock is strictly to generate the DQ signals for writing so that you'll get a center-aligned data with respect to the DQS strobe.
- Resynchronization clock for operation above 167 MHz.
  This clock is named `resync_clk` and may be required depending on your system. "Re-synchronization Calculation" on page 8–28.

To create the `dqs_ddrio` instance for the DQS pins, use the `altddio_bidir` MegaWizard Plug-In Manager and select the following options:

- Create an output enable port.
- Register output enable.
- Delay switch-on by a half clock cycle.
- Add unregistered output port (i.e., `combout`).

To create the `dq_ddrio` instance for the DQ pins, select the following options in the `altddio_bidir` MegaWizard Plug-In Manager:

- Create a clock enable port for each clock port.
- Create an output enable port.
- Register output enable.

The `dm_ddrio` module should be created like the `dq_ddrio` module, with the exception of it being bidirectional. The DM pins are only used when writing to the DDR SDRAM and FCRAM memory; the memory devices do not generate the DM signals.

Make the following logic options to the DQS pins in the Quartus II software:

- **DQS Frequency** – the frequency of your DDR SDRAM or FCRAM device
- **DQS Phase Shift** – either 72 or 90 degrees
- **DQS Input reference clock** – the input clock to be used for your DQS Phase Shift circuitry

☞ Make sure to add an inverter between the `combout` port of the `dqs_ddrio` module and the inclock port of the `dq_ddrio` module.

In the example design shown in Figure 8–12, the input to the PLL, `input_clk`, is at 50 MHz. The PLL then multiplies this signal by 2 so that the DQS is running at 100 MHz. You then need to make the three logic options to the DQS pin. See Figure 8–9 on how to set the **DQS Frequency** option. Due to this multiplication, a PLL output has to be routed on the board then back to the device, since the input to the DQS phase shift circuitry must come from a clock input pin. The example above uses the PLL output `fb_clk` as the clock to be looped back into the board to the input clock `ref_clk`. Therefore, you need to set `ref_clk` (which is the PLL output signal `fb_clk` looped back to the device) as the **DQS Input Reference Clock**. Figure 8–10 shows how to set the **DQS Input Reference Clock option**.

Refer to Quartus II Interface Logic Options section on how to make these logic options.

When interfacing with an RLDRAM I device, the DQS signal is only used when reading from the memory device. RLDRAM I also uses a pair of differential DQS signals, however, since Stratix and Stratix GX devices do not support differential DQS signaling, the negative leg of the DQS signal from the RLDRAM I device is ignored. You can make the signal run continuously as DQS is not used for writing.

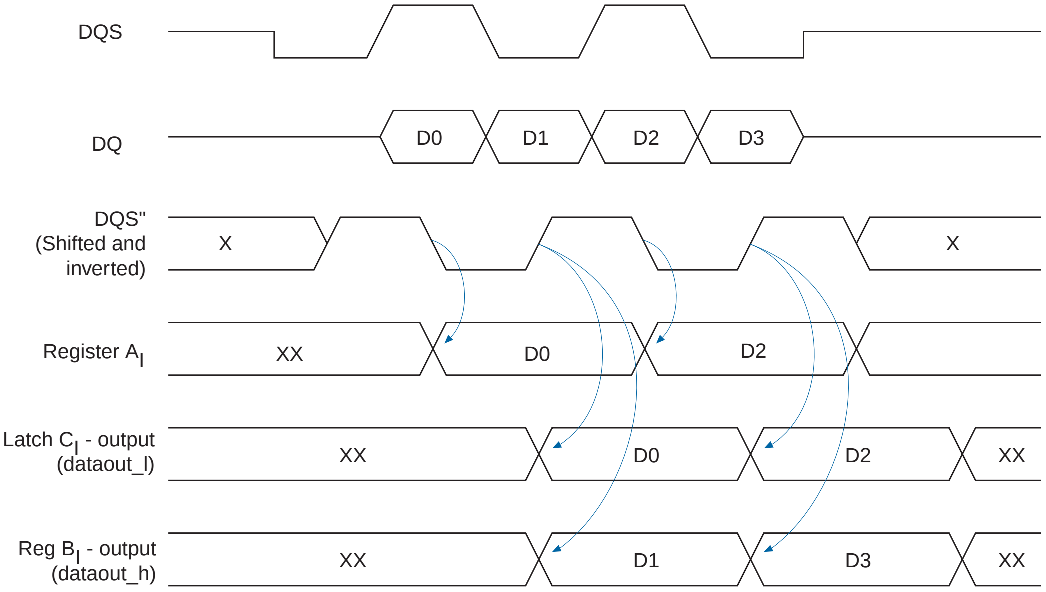
### *Read Operation*

The DQS phase shift circuitry is used when reading from the DDR SDRAM, DDR FCRAM, and RLDRAM I memory device. The DDR SDRAM and FCRAM device sends the data edge aligned with respect to the DQS signal. To properly read the data in, the DQS signal needs to be center aligned. Setting the DQS logic options in the Quartus II software enables the dedicated circuitry to shift the DQS by 72 degrees (for DDR FCRAM interfaces) or by 90 degrees (for DDR SDRAM interfaces) to center align the strobe signal to the data.

During read operations, the DQS signal is phase shifted by 72 or 90 degrees. See Figure 8–12. The phase shifted DQS signal then goes into the `dqs_ddrio` megafuction. The DQS signal bypasses the DDR input registers and is sent out through a combinatorial path on the `combout` port. During a read operation, in order to capture the last word the memory sends, the `combout` signal needs to inverted before going into the `dq_ddrio` megafunction. The phase shifted DQS signal can then clock the data on the DQ pins into input registers. Due to the inversion, however, the outputs from the `dq_ddrio` are also inverted; `dataout_h` corresponds to the DQ signal that was received along with the falling edge of the clock and `dataout_l` corresponds to the DQ signal that was received along with the rising edge of the clock. This is why `data_l_to_core` and `data_h_to_core` are connected to `dataout_h` and `dataout_l`, respectively, in the `dq_ddrio` module.

Figure 8–13 shows a functional waveform for the read operation for the memory interface. The registers and DDR latch names refer to the output signals from the same registers latch in Figure 8–1. DQS and DQ signals come from pins and DQS" is the 90° shifted and inverted version of the DQS signal used to clock the registers and enable the latch.

***Figure 8–13. DDR Memory Interface Read Operation***



The DDR SDRAM device is clocked by CK and CK# which is generated by the Stratix or Stratix GX PLL. This clock is at the same frequency as the DQS frequency and shifted by the amount of the DQS clock-to-out time in the device. The shift is to ensure that when writing to the DDR SDRAM device, the DQS signal is aligned with the CK signal (provided that the CK, CK#, and DQS trace lengths are the same). The DDR SDRAM device generates the DQS signal; this DQS signal is aligned with the edges of the CK and CK# signals within $t_{DQSCK}$ (typically about ±0.75 ns for 133-MHz operation).

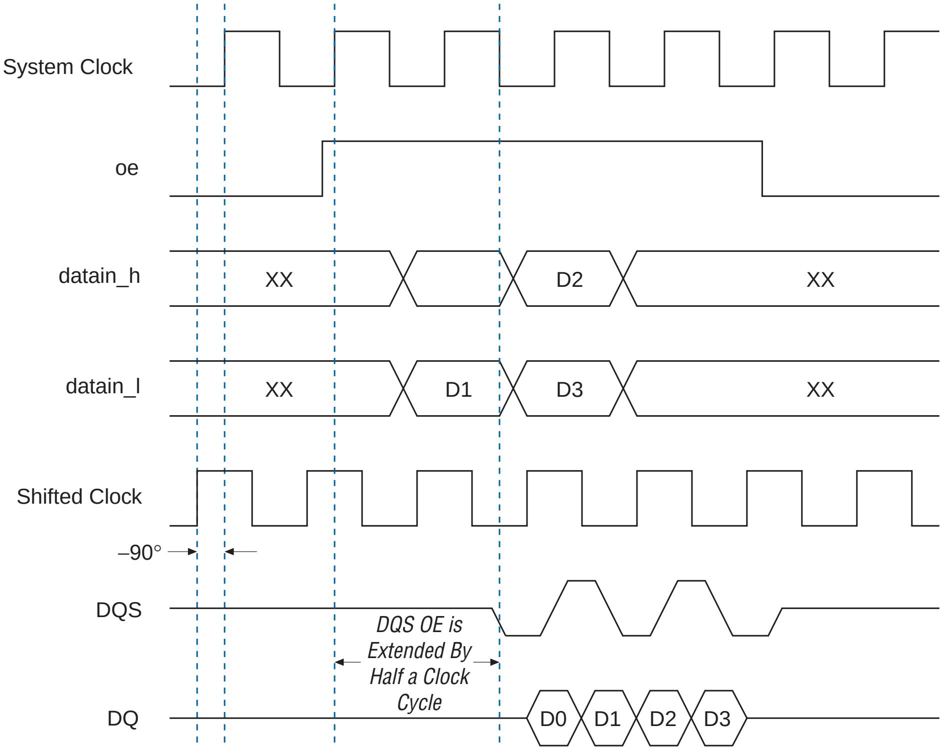
When arriving at the Stratix device, the DQS signal is shifted by the dedicated phase shift circuitry by 90 degree to capture the DQ signals. The DQ signals are then ready to be synchronized with the system clock. Depending on the board delay and the device internal delay, these numbers vary and you need to do a timing analysis to decide whether to use the falling edge or the rising edge of the system clock for the synchronization registers. This method works for up to 167-MHz operation. To interface with a faster memory device, you may need to have an extra PLL output as a resynchronization clock.

For a more detailed example, please refer to the *Appendix B* of the *DDR SDRAM Controller MegaCore® Function User Guide* and "Re-synchronization Calculation" on page 8–28 or contact Altera Applications for a preliminary **Round Trip Delay Calculator**.

### *Write Operation*

During write operations, the Stratix or Stratix GX device needs to send the data to the memory center-aligned to the DQS signal. The PLL shown in Figure 8–12 is used make sure that the data is center-aligned with the DQS signal. The PLL generates a zero degree phase shifted system clock and a -90 degrees phase shifted system clock. The zero degree phase shifted clock feeds the inclock port of the `dqs_ddrio` megafunction. In this example, the `datain_h` is tied to the registered `dqs_oe`, the output enable signal and `datain_l` is tied to `GND`. The zero degree phase shifted clock will generate a DQS signal at the same frequency of the system clock. The -90 degrees phase shifted clock is fed into the `inclock` port of the `dq_ddrio` megafunction for the DQ signal. By using the -90 degrees phase shifted clock, the data will be sent out center-aligned to the DQS signal. A phase shift of -90 degrees is used so that the output enable sends out the first data on the positive edge as opposed to the negative edge. Figure 8–14 shows a functional waveform for the write operation for the memory interfaces.

*Figure 8–14. DDR SDRAM & FCRAM Memory Interface Write Operation* *Note (1)*



*Note for Figure 8–14*

(1) The RLDRAM I device does not use the DQS signal for writing.

You can use 270° phase shift is similar to -90°, but the Quartus II Timing Analyzer uses -90° for reference, so the $t_{CO}$ is reported to be larger than what it actually is when using 270 degrees phase shift.

Check the **Delay switch-on by half a clock cycle** option for the `dqs_ddrio` megafunction to enable the extra output enable register in the I/O element (IOE), noted by $B_{0E}$ in Figure 8–2. This is to provide the appropriate write preamble on the DQS signal.

The PLL can also generate the clock that goes to the DDR SDRAM and FCRAM memories. Stratix supports differential SSTL on output clock pins, which is required by the DDR SDRAM and FCRAM memories. The design in Figure 8–12 shows the `e0` port of the PLL generating the DDR SDRAM clock. You need to assign the differential SSTL I/O standard of the output clock pin.

## Understanding Quartus II Results

Knowing that the DQS phase shift circuitry is implemented properly is vital in designing a controller for the memory device. This section describes how to understand the Quartus II compilation result.

### Quartus II Report

When compiling a design with the DQS phase shift circuitry enabled, you will see the following message:

> **Device takes up to 256 clock cycles to train dedicated DDR I/O circuitry to generate correct DQS phase shift on system power-up.**

You should also see a similar entry like Table 8–3 in the Compilation Report under *Global and Other Fast Signals* (*Resource Section*). For this particular example, the table shows that pin `dqs` is located in location C24 and uses the DQS bus with 8 DQ pins connected to this bus.

*Table 8–3. Sample Report File When Using DQS Phase Shift* *Figure 8–7*

| Name | Location | Fan-out | Global Resource Used |
|---|---|---|---|
| `dqs` | C24 | 8 | DQS-8 I/O bus |

### Timing Analysis Result

System timing analysis is crucial for high-speed memory interfaces. This section describes the Quartus II Timing Analysis result.

**Read Timing Analysis**

The Quartus II software shows the setup and hold time values for the DQ signals with regards to incoming DQS signals that have not been shifted and inverted. Expect negative setup time and positive hold time for the DQ pins due to the shifted DQS signal.

**Write Timing Analysis**

The Quartus II software displays the clock-to-out time values for the DQ, DQS, and DM pins with respect to the input clock to the PLL. To find the skew between these pins, you need to calculate the difference in the $t_{CO}$

time. You also need to make sure that the external output clock to the memory device has the same clock-to-out delay as the DQS pin to meet the $t_{DQSS}$ margin.

## Re-synchronization Calculation

To ensure the DQ signals are captured correctly in the Stratix device, you need to determine when to resynchronize the DQ signals to the logic array. In operation up to 167 MHz, you need to decide whether you will need a positive edge or a negative edge clocking scheme for your controller. For operation faster than 167 MHz, you may need to add an extra shifted PLL output for your resynchronization phase. In either case, you need to perform a timing analysis of the round trip delay of the system.

To perform the timing analysis, you need the following minimum and maximum numbers for your system:

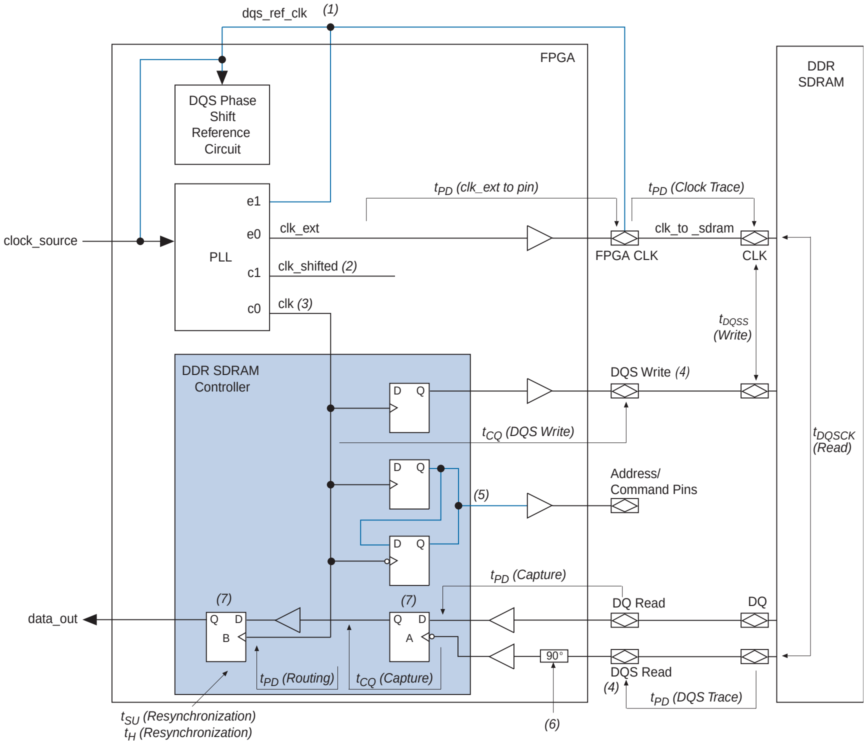
- Clock and DQS board trace length
- $t_{DQSCK}$ number (from the DDR memory data sheet)
- DQS clock-to-out delay
- Delay from the pin to IOE register
- Micro clock-to-out number for the IOE register
- Delay from IOE register to the LE resynchronization register.

The round trip delay takes into account the following paths as shown in Figure 8–15:

*Table 8–4. Round Trip System Delay*

| Delay | Description |
|---|---|
| $t_{PD}$ (clk_ext to pin) | This delay is the same as the clock-to-out delay of the DQS pin. You can calculate how much to shift the external clock by subtracting the routing delay from the PLL to the pin from the DQS clock-to-out delay. |
| $t_{PD}$ (Clock trace) | Your board trace delay for the clock pin. |
| $t_{DQSCK}$ | The skew between DQS and the CK clock per your DDR memory data sheet. |
| $t_{PD}$ (DQS trace) | Your board trace delay for the DQS pin. Normally the same as your Clock trace. |
| $t_{PD}$ (Capture) | Delay from the DQS pin to the DQ IOE register. This delay includes the routing delay and the phase shift error. |
| $t_{CQ}$ (Capture) | Micro clock-to-out time for the IOE register. |
| $t_{PD}$ (Routing) | Delay from the Q port of the IOE to the D port of the resynchronization register in the logic array. |

*Figure 8–15. Round Trip Delay Diagram*



*Notes for Figure 8–15:*

(1) The `dqs_ref_clk` input for Stratix devices can be either fed back from the clock output driving the DDR SDRAM or a separate clock output from the PLL. The phase of this reference clock relative to the other clocks in the system is unimportant.

(2) The `clk_shifted` signal is shown for completeness, but it is not needed in the timing analysis for round-trip delay or address/command timing.

(3) The `clk` clock is the system clock, and you do not need to take into account any skew across the device.

(4) The dqs signal is bidirectional. DQS Write and DQS Read signals are shown as two separate pins for this timing analysis.

(5) This signal path depends on whether you use the positive edge or negative edge for the resynchronization.

(6) The DQS phase-shift reference circuit controls the 90° phase shift dynamically. The control path is not shown and its operation is transparent to the user.

(7) Register A resides in the IOE, part of the DDR I/O circuitry, while Register B is in the LE closest to the pin.

You can find the total minimum and maximum delay of your system by adding all the numbers in the round trip delay. Once you find that delay, you can figure out the safe resynchronization window. See Figure 8–16 for an example; this assumes a hold time of 0 ns. The resynchronization window can also be calculated by the following equation:

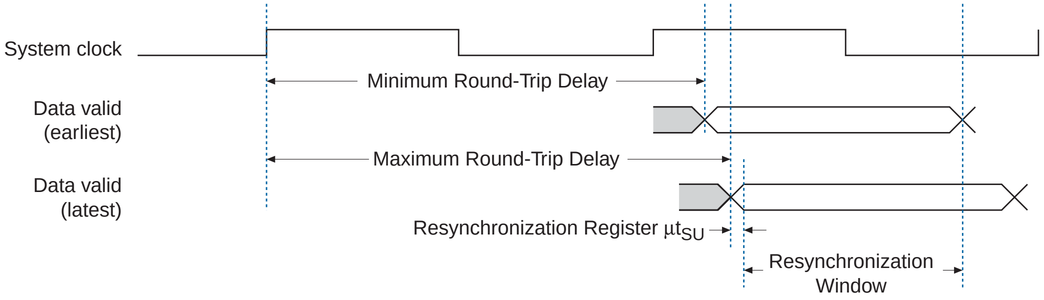
Resynchronization window = minimum Round Trip Delay + half-period – maximum round trip delay - max micro setup time of the resynchronization register.

You need to find out whether the resynchronization window falls on a clock edge. If it does, you can use this clock edge for your resynchronization (whether this is a positive or negative clock edge). Else you need to use another PLL output clock that is shifted so that the edge will be within this small window. Use the following equations to calculate the smallest or largest shift values:

Smallest PLL shift value = max round trip delay + max micro setup time of the resynchronization register − PLL clock skew − last clock edge time

Largest PLL shift value = min. round trip delay + clock period − PLL clock skew − last clock edge time

*Figure 8–16. Determining the Resynchronization Window*



☞ Contact Altera Applications for further information on the resynchronization calculation. You can also refer to the *Appendix B* of the *DDR SDRAM Controller MegaCore Function User Guide* for calculating the round trip delay.

## Conclusion

Modern systems require faster interfaces to memory and other high-speed applications. With faster system and I/O speeds, interfaces have become a bottleneck. DDR I/O architecture helps increase the speed of these interfaces by allowing them to communicate with system logic at a higher data rates. The DDR I/O circuitry in Stratix and Stratix GX devices enables a robust and easy-to-implement solution to enhance system performance.

With Stratix and Stratix GX dedicated circuitry, you can have comfortable and consistent margins when reading data from a DDR SDRAM, DDR FCRAM, and RLDRAM I memories. The Stratix and Stratix GX PLL helps to center-align your data with the DQS signal.

These features are easily accessible in the Quartus II software. You can also use the sample design to start designing your own memory controller design.

## Revision History

The information contained in *Application Note 212: Implementing Double Data Rate I/O Signaling in Stratix & Stratix GX Devices* version 2.0 supersedes information published in previous versions. The following changes were made in *Application Note 212: Implementing Double Data Rate I/O Signaling in Stratix & Stratix GX Devices* version 2.0:

- Added DQS information.
- Removed `altddio_in`, `altddio_out`, and `altddio_bidir` information.
- Various text changes throughout document.

# 9. Using Soft Multipliers with Stratix & Stratix GX Devices

S52009-1.0

Chapter 9, Using Soft Multipliers with Stratix & Stratix GX Devices replaces *AN 246: Using Soft Multipliers with Stratix & Stratix GX Devices*.

## Introduction

Traditionally, designers have been forced to make a tradeoff between the flexibility of digital signal processors and the performance of ASICs and application-specific standard product (ASSPs) digital signal processing (DSP) solutions. The Altera® DSP solution eliminates the need for this tradeoff by providing exceptional performance combined with the flexibility of Stratix™ and Stratix GX FPGAs.

Stratix and Stratix GX devices include embedded high-performance multiplier-accumulators (MACs) in dedicated DSP blocks. The DSP blocks can operate at data rates above 300 million samples per second (MSPS), making Stratix and Stratix GX FPGAs ideal for high-speed DSP applications. In addition to the dedicated DSP blocks, designers can use the TriMatrix™ memory blocks to implement variable depth/width, high-performance multipliers. In this instance, TriMatrix memory blocks are used as a look-up table (LUT), which contains all possible results from multiplication of input data to constant coefficients.

There are four different soft multiplier modes of operation:

- Parallel Multiplications - Multiple memories produce one multiplication result with each clock cycle (e.g., high speed data scaling)
- Semi-Parallel Multiplications - Each memory produces one multiplication with multi-cycle operation (e.g., coefficient update of least mean squares (LMSs), coefficient update of equalizer)
- Sum of Multiplications - One memory or group of memories produce the sum of multiplications (e.g., finite impulse response (FIR), discrete cosine transform (DCT))
- Hybrid Multiplications - Combination and optimization of semi-parallel and sum of multiplications modes of operation. Ideal for a complex number of multiplications (e.g., complex fast Fourier transform (FFT), infinite impulse response (IIR))

This application note covers the sum of multipliers mode of operation.

## Stratix & Stratix GX Memory & DSP Blocks

The TriMatrix memories consist of three types of RAM blocks: M512, M4K, and M-RAM blocks. M512 and M4K RAM blocks are memory blocks with a maximum width of 18 and 36 bits, respectively, and a maximum performance of approximately 300 MHz (ideal for soft multipliers). You can use these memory blocks for DSP applications that are multiplier intensive, such as imaging and mobile wireless technologies where the data word size does not fit within the standard 8-, 16-, or 32-bit widths.

Tables 9–1 and 9–2 show the number of Stratix and Stratix GX TriMatrix M4K memory blocks.

*Table 9–1. Stratix TriMatrix Memory Blocks*

| Feature | EP1S10 | EP1S20 | EP1S25 | EP1S30 | EP1S40 | EP1S60 | EP1S80 |
|---|---|---|---|---|---|---|---|
| M512 RAM (32 × 18 bits) | 94 | 194 | 224 | 295 | 384 | 574 | 767 |
| M4K RAM (128 × 36 bits) | 60 | 82 | 138 | 171 | 183 | 292 | 364 |
| M-RAM (4K × 144 bits) | 1 | 2 | 2 | 4 | 4 | 6 | 9 |
| Total RAM bits | 920,448 | 1,669,248 | 1,944,576 | 3,317,184 | 3,423,744 | 5,215,104 | 7,427,520 |

*Table 9–2. Stratix GX M4K Memory Blocks*

| Feature | EP1SGX10C<br>EP1SGX10D | EP1SGX25C<br>EP1SGX25D<br>EP1SGX25F | EP1SGX40D<br>EP1SGX40G |
|---|---|---|---|
| M512 RAM (32 × 18 bits) | 94 | 224 | 384 |
| M4K RAM (128 × 36 bits) | 60 | 138 | 183 |
| M-RAM (4K × 144 bits) | 1 | 2 | 4 |
| Total RAM bits | 920,448 | 1,944,576 | 3,423,744 |

## Basics of DSP Operation

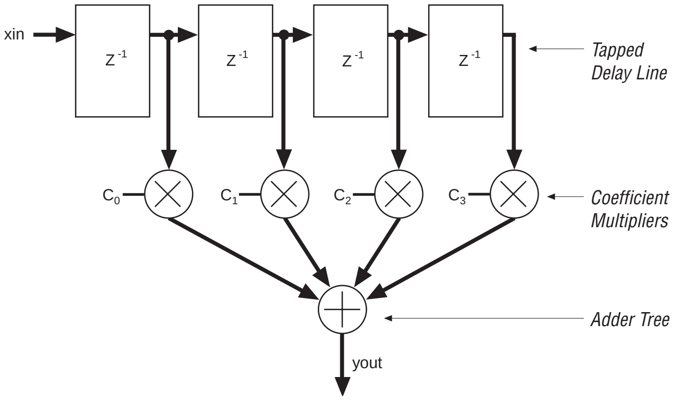
DSP is an arithmetic-intensive technology. To achieve high-speed signal processing, arithmetic operation must be accelerated.

Many digital systems use signal filtering to remove unwanted noise to provide spectral shaping, or to perform signal detection or analysis. Filters are used with communication applications such as band selection, low-pass filtering, and video convolution functions. Two types of filters that provide these functions are FIR and IIR filters. You can use FIR filters in systems that require a linear phase and have an inherently stable structure. You can use IIR filters in systems that can tolerate phase distortion. Typical filter applications include signal pre-conditioning, band selection, and low-pass filtering.

## FIR Filter Architecture

The structure of a FIR filter is a weighted, tapped delay line. The filter design process involves identifying coefficients that match the frequency response specified for the system. The coefficients determine the response of the filter. By changing the coefficient values or by adding more coefficients to the filter, you can change the signal frequencies, which pass through the filter. Figure 9–1 shows the basic FIR filter structure.

*Figure 9–1. Basic FIR Filter Structure*



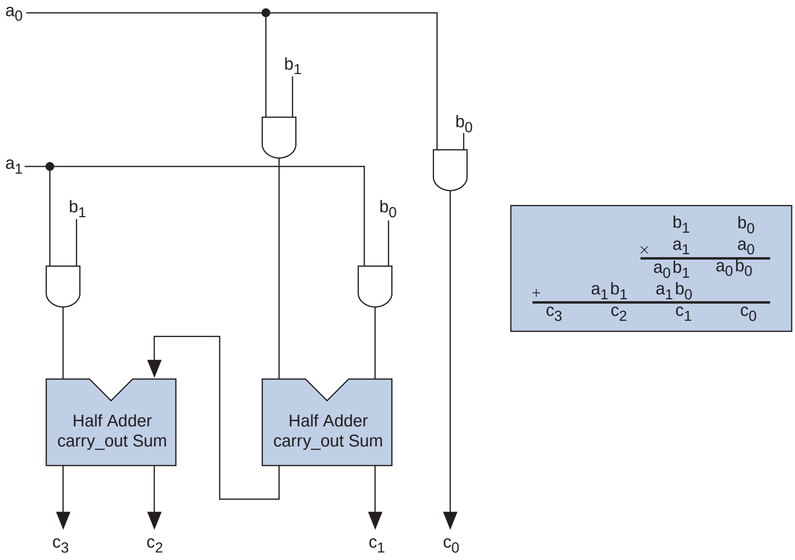
The FIR filter function (or many other DSP functions) is based on a MAC operation. The input data shifts into the shift register. The output of each register, which is called a tap, is the parallel input to the multiplier. Each parallel input is multiplied by a coefficient ($C_n$) as it is presented (see Figure 9–1).

## MAC Function

The base of many DSP algorithms is a MAC function. The MAC function is represented by multiplication of a multiplier to a multiplicand, which implies that each element of the multiplier is multiplied by each bit of the multiplicand. The partial product of each multiplication is accumulated according to the weight of the partial product (weight indicates the location of a bit corresponding to other bits). For example, if a partial product of bits 4 through 7 is added to a partial product of bits 0 through

3, the partial product of 4 through 7 is shifted according to their weight and then accumulated to the partial product of previous stages. Figure 9–2 shows a simple 2 × 2 multiplication of multiplier $a_1a_0$ to multiplicand $b_1b_0$.

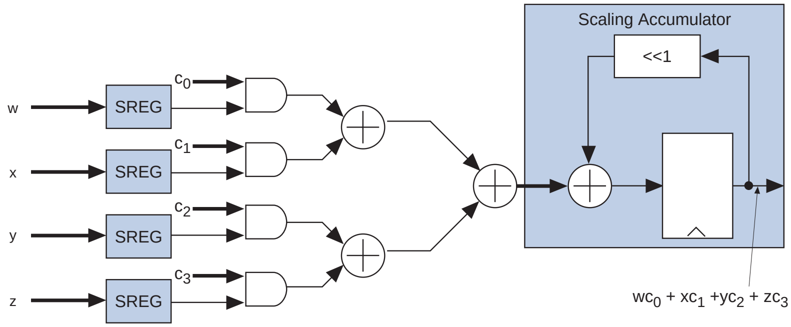
*Figure 9–2. Multiplication of Two 2-Bit Numbers*



## Distributed Arithmetic

Distributed arithmetic is a method of performing multiplication by distributing the operation over many LUTs. Figure 9–3 shows the four-product MAC function that uses sequential shift and add to multiply four pairs, and then sum their partial product to obtain a final result. Each multiplier forms partial products by multiplying the coefficient by one bit of the data at a time using an AND gate.

*Figure 9–3. Distributed Arithmetic with Four Constant Multiplicands*



At the end of the process, these partial products (of a particular bit) are summed up and the final stage performs the final shift-accumulate at the scaling accumulator.

The scaling accumulator shifts the sums of partial products accordingly and then sums the result. The distributed-arithmetic circuit simultaneously performs four multiplications and sums the results when all of products are completed.

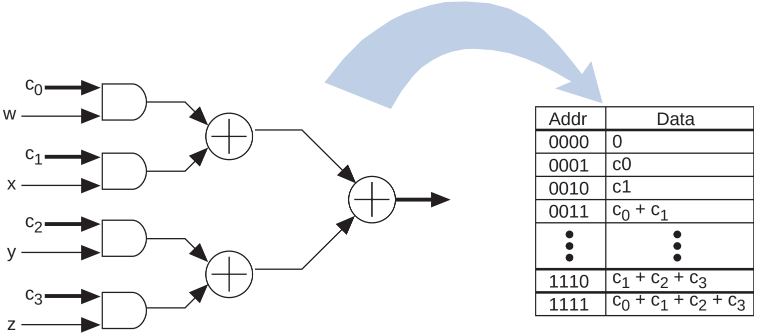
## DSP Applications with Stratix & Stratix GX Devices

You can use Stratix and Stratix GX RAM blocks to implement DSP applications. Specifically, you can use the M512 and M4K RAM blocks, with 32 × 18-bit and 128 × 36-bit capacity, as LUTs to store the multiplication result of multiplier to multiplicand.

### Distributed Arithmetic in LUT

Figure 9–4 shows how to implement distributed arithmetic using LUTs. The combined product and adder tree can be reduced to an LUT. The LUT contains the sums of constant coefficients for all possible input combinations to the LUT. Finally, the sums of the bits from the LUTs are added together, keeping in mind that different coefficient multiplications have different weight. Therefore, some shifting is required before the bit sums are performed.

*Figure 9–4. Four-Bit Multiplication to Constant Coefficient* Note (1)



| Addr | Data |
|---|---|
| 0000 | 0 |
| 0001 | c0 |
| 0010 | c1 |
| 0011 | $c_0 + c_1$ |
| ⋮ | ⋮ |
| 1110 | $c_1 + c_2 + c_3$ |
| 1111 | $c_0 + c_1 + c_2 + c_3$ |

*Note to Figure 9–4:*

(1) $c_0$ to $c_3$ are constant coefficients.

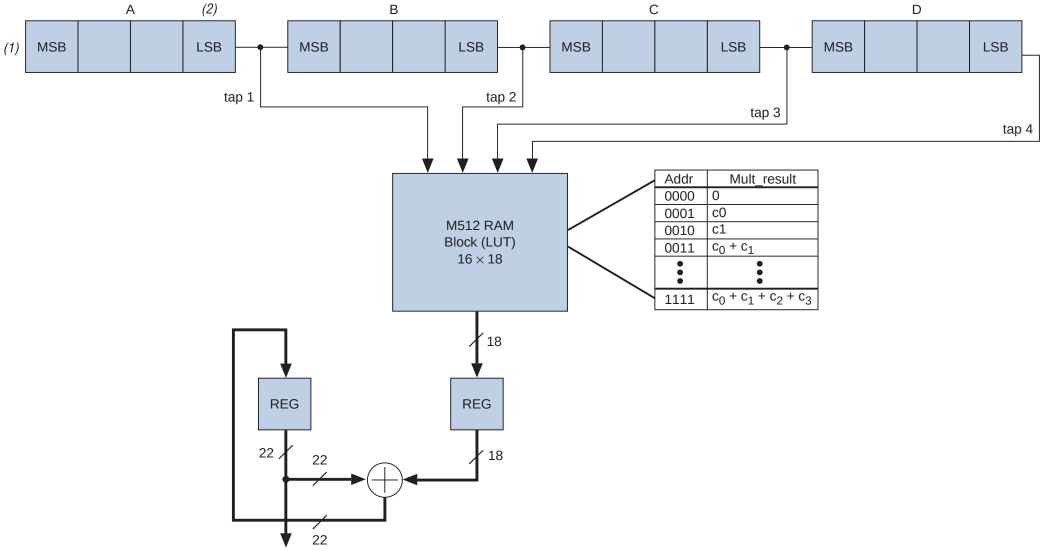
## LUT Implementation in M512 & M4K RAM Blocks

You can use the Stratix and Stratix GX M512 or M4K RAM memory blocks as a LUTs to implement multiplication for DSP applications. All possible combinations of a multiplicand summation are calculated and stored in the M512 or M4K RAM block as an LUT. As a result, each address in the memory blocks represent a unique multiplication result.

Each multiplier's *n*-data bits load into a shift register at the data rate of clock/*n*-data bits. The shift register's data is the input, which point to an address location in the M512 or M4K RAM block. The output of the RAM block indicates the multiplication result for a specific bit, at each clock cycle.

Figure 9–5 shows the RAM LUT implementation of four 4-bit data inputs and up to 16-bit constant coefficients. This implementation takes four clock cycles to complete multiplication operation by adding partial products. At each cycle, the addition of partial products will generate one extra bit as the carry on bit. By the end of fourth cycle, the final addition of partial products will generate a 22-bit output.

*Figure 9–5. Four-Tap FIR Filter Implementation Using M512 RAM Blocks as LUTs*



*Notes to Figure 9–5:*

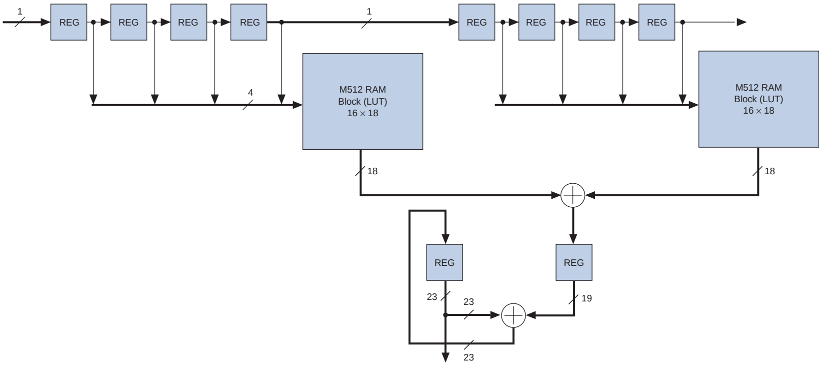
(1) MSB: most significant bit.
(2) LSB: least significant bit.

For example, Figure 9–5 shows four 4-bit data inputs called A, B, C, and D. The input data width determines the length of the shift register (e.g., a 4-bit shift register for 4-bit data). The outputs from the shift registers are called taps (the number of taps is equal to the number of input data). Since the size for Stratix and Stratix GX M512 RAM blocks is 32 × 18 bits, the maximum taps for each M512 RAM block is five ($2^5 = 32$ addresses). Depending on the number of inputs, coefficients, taps, and the required frequency, the number of RAM blocks that are used will vary. The example in Figure 9–5 requires only one M512 RAM block.

On each clock cycle, the LSB of each shift register simultaneously shifts out as inputs to the RAM block. The longer the shift register cycle, the more clock cycles required to shift out all the data to the RAM block. On the first cycle, the LSB of data cells A, B, C, and D are multiplied by all four bits of the coefficients. It will take four clock cycles to multiply the 4-bit inputs to the 16-bit coefficients.

If the FIR filter has more than five taps, you must use multiple M512 blocks or M4K RAM blocks (which are larger memory blocks) to complete multiplication. The reason for this requirement is that M512 RAM blocks have a maximum of 32 words (18 bits) per RAM block which is equal to $2^5$ addresses, while M4K RAM blocks have a maximum of 128 words (36 bits) per RAM block which is equal to $2^7$ addresses. The outputs of RAM blocks is shift-accumulated according to their weight, and provides the final multiplication result. Figure 9–6 shows the multiplication of eight 4-bit data inputs to a 16-bit constant coefficient in two M512 RAM blocks. The output from the RAM block is an 18-bit output. Since it takes four clock cycles to complete the multiplication operation (by adding the partial products), the final output after the forth cycle will be a 23-bit output.

***Figure 9–6. Using Multiple M512 RAM Blocks for an 8-Tap FIR Filter***

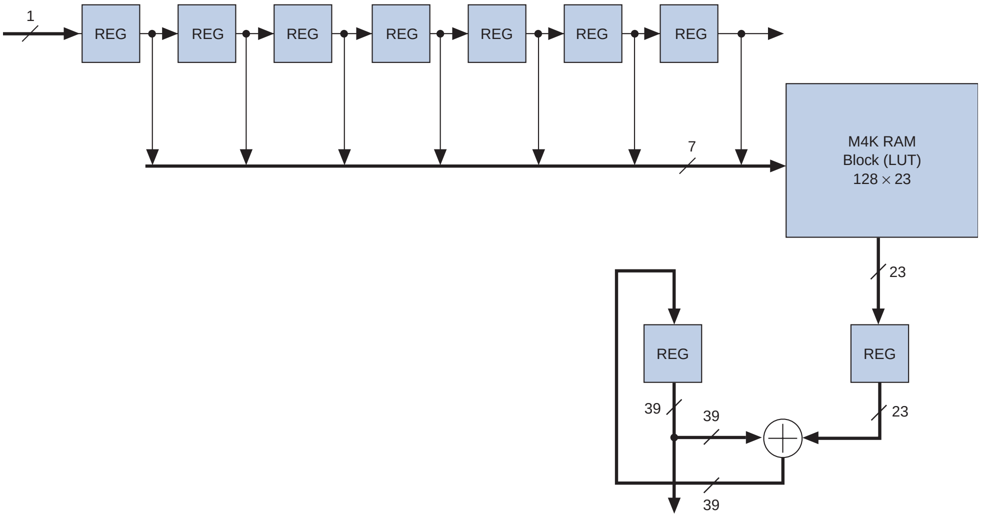


Since the application's performance is determined by the length of the shift register (MSPS = system clock/$N$, where $N$ equals the width of input data bus) for filters that require high performance, Altera recommends that you split the shift register into smaller shift registers. This technique increases the performance, but uses more RAM blocks. See Table 9–1 on page 9–2 for the total number of TriMatrix memory blocks.

Also, if the FIR filter requires a coefficient larger than 16 bits, you can use multiple M512 RAM blocks or use M4K RAM blocks (M4K RAM blocks can perform multiplication up to a 34-bit coefficient). RAM block outputs are shifted and accumulated in a scaling accumulator to add up the partial products together and to obtain a final multiplication result.

Figure 9–7 shows multiplication of seven 16-bit data inputs to a 20-bit constant coefficient in one M4K RAM block. The 128 addressed lines correspond to seven data inputs in a M4K RAM block. Performing seven 16-bit × 20-bit multiplications will generate a 23-bit output from a M4K RAM block. Since it takes 16 clock cycles to complete adding the partial products, and at each partial product addition one bit is added to the total number of output bits, the final output is 39 bits.

*Figure 9–7. Using a M4K RAM Block for a 7-Tap FIR Filter*



Even though this technique is for a multiplication of constant coefficients, to change the coefficients, you can rewrite the RAM blocks since Stratix and Stratix GX memory blocks are dual-port RAM. This operation is useful for adaptive FIR filters.

## DSP Performance (MMAC)

Because digital signal processors are typically assigned MAC-intensive tasks, the DSP performance is related to MAC throughput. The unit for DSP speed is million multiply-accumulate operations per second (MMACS). Tables 9–3 and 9–4 show throughput for DSP applications implemented in Stratix and Stratix GX RAM blocks for 16 × 16 multipliers and the total number of 16 × 16 multipliers within Stratix and Stratix GX M512 and M4K blocks.

*Table 9–3. 16 × 16 Multiplier in Stratix RAM Blocks* *Notes (1), (2)*

| Device | Number of Multipliers *(3)* | | | Performance (MMACS) | | |
|---|---|---|---|---|---|---|
| | M512 Blocks | M4K Blocks | Total Blocks *(4)* | M512 Blocks | M4K Blocks | Total Blocks *(4)* |
| EP1S10 | 23 | 30 | 53 | 6,900 | 9,000 | 15,900 |
| EP1S20 | 48 | 41 | 89 | 14,000 | 12,300 | 26,700 |
| EP1S25 | 56 | 69 | 125 | 16,800 | 20,700 | 37,500 |
| EP1S30 | 74 | 85 | 159 | 22,200 | 25,500 | 47,700 |
| EP1S40 | 96 | 91 | 187 | 22,800 | 27,300 | 56,100 |
| EP1S60 | 144 | 146 | 290 | 43,200 | 43,800 | 87,000 |
| EP1S80 | 192 | 182 | 370 | 57,600 | 54,600 | 112,200 |

*Table 9–4. 16 × 16 Multiplier in Stratix GX RAM Blocks* *Notes (1), (2)*

| Device | Number of Multipliers *(3)* | | | Performance (MMACS) | | |
|---|---|---|---|---|---|---|
| | M512 Blocks | M4K Blocks | Total Blocks *(4)* | M512 Blocks | M4K Blocks | Total Blocks *(4)* |
| EP1S10C | 23 | 30 | 53 | 6,900 | 9,000 | 15,900 |
| EP1S10D | 23 | 30 | 53 | 6,900 | 9,000 | 15,900 |
| EP1S25C | 56 | 69 | 125 | 16,800 | 20,700 | 37,500 |
| EP1S25D | 56 | 69 | 125 | 16,800 | 20,700 | 37,500 |
| EP1S25F | 56 | 69 | 125 | 16,800 | 20,700 | 37,500 |
| EP1S40D | 96 | 91 | 187 | 22,800 | 27,300 | 56,100 |
| EP1S40G | 96 | 91 | 187 | 22,800 | 27,300 | 56,100 |

*Notes to Table 9–3:*

(1) Both coefficient and input data width are 16 bits.

(2) These values are for four inputs. The number of multipliers will increase by approximately 50% with optimization of five inputs for M512 blocks and seven inputs for M4K blocks.

(3) The number of multipliers are normalized (divided by 16) to create throughput of one result per clock cycle.

(4) The total number of M512 and M4K blocks in a device.

To calculate the MAC throughput, use the following equation:

$$\text{MMACS} = \text{Frequency (MHz)} \times \text{number of multipliers in RAM block}$$

For these calculations, assume that the operation frequency in M512 or M4K RAM blocks is approximately 300 MHz. It is also assumed that it will take 16 clock cycles to perform a multiplication operation (due to the width of the input data).

## Software Implementation

The Altera FIR Compiler MegaCore® function generates FIR filters customized for Altera devices. You can use the FIR Compiler wizard interface to implement a variety of filter architectures, including fully parallel, serial, and multi-bit serial-fixed coefficient filters, and MAC-based and multi-cycle variable filters. The wizard also includes a coefficient generator to help you create filter coefficients.

☞ FIR Compiler version 2.6.0 supports FIR filter implementation in Stratix and Stratix GX TriMatrix memory blocks. You can use this version of the FIR Compiler to implement soft multiplier-based FIR filters.

The FIR Compiler function speeds up the design cycle by:

- Finding the coefficients needed to design custom FIR filters.
- Generating bit-accurate and clock-cycle-accurate FIR filter models (also known as bit-true models) in the Verilog HDL and VHDL languages, and for the MATLAB environment (Simulink Model Files and M-Files).
- Automatically generating the code required for the MAX+PLUS® II or Quartus® II software to synthesize high-speed, area-efficient FIR filters of various architectures.
- Creating Quartus II test vectors to test the FIR filter's impulse response.

For more information on the FIR Compiler function, refer to *FIR Compiler MegaCore Function User Guide*. For more information on FIR Filter and programmable logic device (PLD) implementation, refer to *AN 73: Implementing FIR Filters in FLEX Devices*.

## Conclusion

You can use Stratix and Stratix GX DSP blocks to implement DSP applications. An alternative to DSP block implementation is the use of Stratix and Stratix GX TriMatrix blocks (M512 or M4K RAM blocks). This alternative is useful for designs that need more multipliers than are available using DSP blocks. This implementations is particularly useful when these multipliers are multiplied by a constant or a value that infrequently changes, as in an adaptive FIR filter.

# 10. Implementing 10-Gigabit Ethernet Using Stratix Devices

S52010-1.0

Chapter 10, Implementing 10-Gigabit Ethernet Using Stratix Devices replaces *AN 220: Implementing 10-Gigabit Ethernet Using Stratix Devices*.

## Introduction

Ethernet has evolved to meet ever-increasing bandwidth demands and is the most prevalent local-area network (LAN) communications protocol. 10-Gigabit Ethernet extends that protocol to higher bandwidth for future high-speed applications. The accelerated growth of network traffic and the resulting increase in bandwidth requirements is driving service providers and enterprise network architects towards high-speed network solutions. Potential applications for 10-Gigabit Ethernet include private campus or LAN backbones, high-speed access links between service providers and enterprises, and aggregation and transport in metropolitan area networks (MANs).

The I/O features of Stratix™ devices enable support for 10-Gigabit Ethernet, supporting 10-Gigabit 16-bit interface (XSBI) and 10-Gigabit medium independent interface (XGMII). Next-generation Stratix devices will support the 10-Gigabit attachment unit interface (XAUI).

This application note discusses the following topics:

- Fundamentals of 10-Gigabit Ethernet
- Description and implementation of XSBI
- Description and implementation of XGMII
- Description of XAUI
- I/O characteristics of XSBI, XGMII, and XAUI

### Related Links

- 10-Gigabit Ethernet Alliance at http://www.10gea.org
- *Section I, Stratix Device Family Data Sheet* of the *Stratix Device Handbook, Volume 1*
- Chapter 5, Using High-Speed Differential I/O Interfaces in Stratix Devices

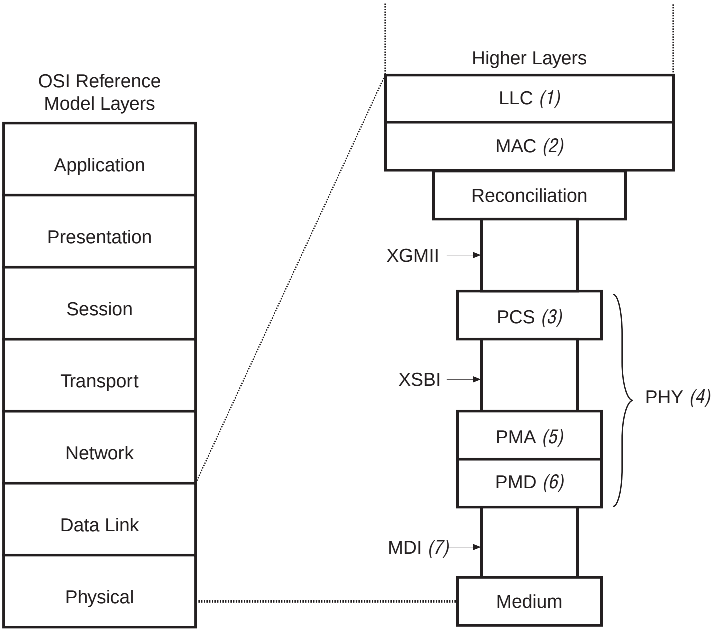
## 10-Gigabit Ethernet

Ethernet speed has increased to keep pace with demand, initially to 10 megabits per second (Mbps), later to 100 Mbps, and recently to 1 gigabit per second (Gbps). Ethernet is the dominant network technology in LANs, and with the advent of 10-Gigabit Ethernet, it is entering the MAN and wide area network (WAN) markets.

The purpose of the 10-Gigabit Ethernet proposed standard is to extend the operating speed to 10 Gbps defined by protocol IEEE 802.3 and include WAN applications. These additions provide a significant increase in bandwidth while maintaining maximum compatibility with current IEEE 802.3 interfaces.

Since its inception in March 1999, the 10-Gigabit Ethernet Task Force has been working on the IEEE 802.3ae Standard. Some of the information in the following sections is derived from Clauses 46, 47, 49, and 51 of the IEEE Draft P802.3ae/D3.1 document. A fully ratified standard is expected in the first half of 2002. Figure 10–1 shows the relationship of 10-Gigabit Ethernet to the Open Systems Interconnection (OSI) protocol stack.

*Figure 10–1. 10-Gigabit Ethernet Protocol in Relation to OSI Protocol Stack*



*Notes to Figure 10–1:*

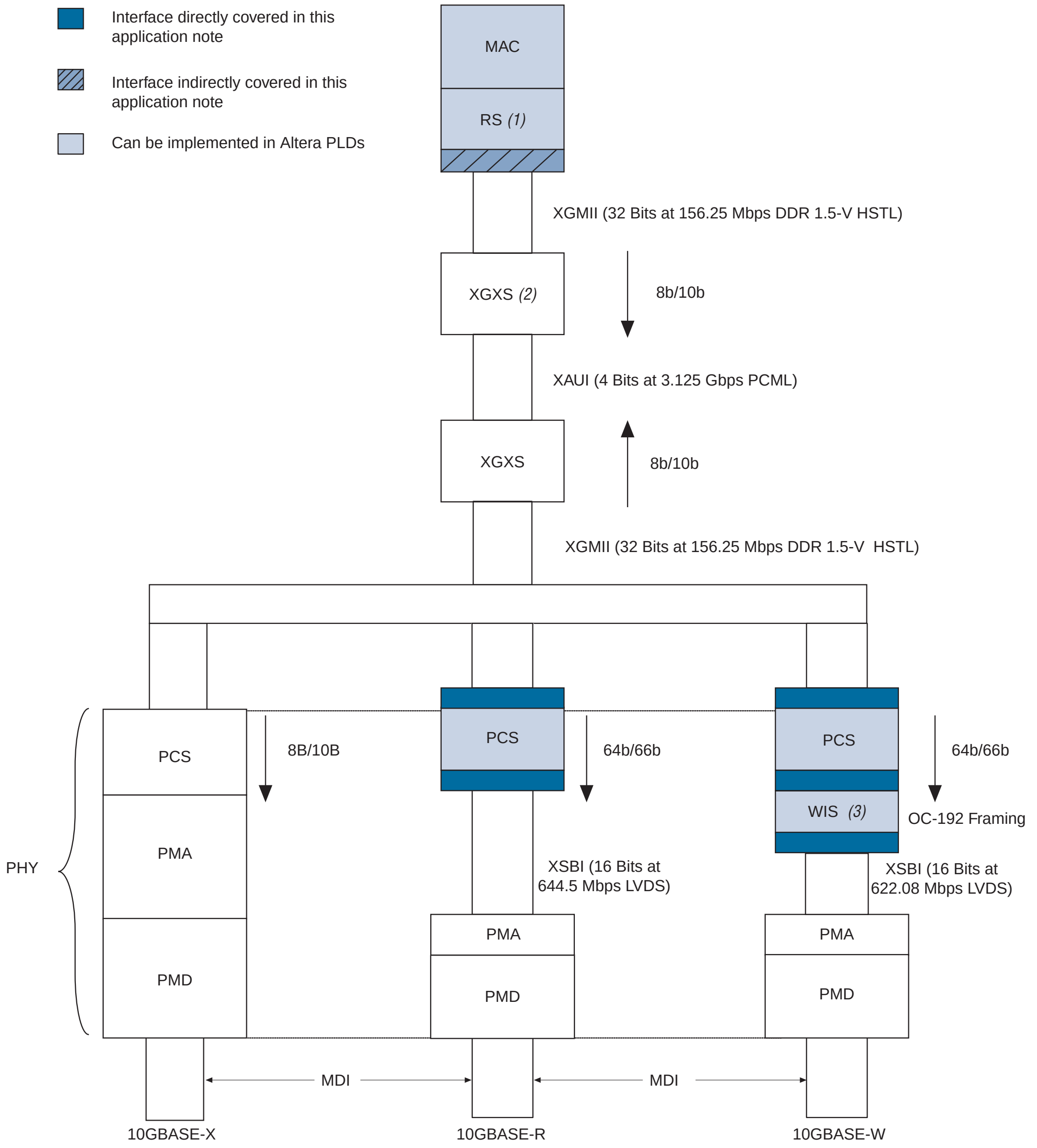
(1) LLC: logical link controller
(2) MAC: media access controller
(3) PCS: physical coding sublayer
(4) PHY: physical layer
(5) PMA: physical medium attachment
(6) PMD: physical medium dependent
(7) MDI: medium dependent interface

The Ethernet PHY (layer 1 of the OSI model) connects the media (optical or copper) to the MAC (layer 2). The Ethernet architecture further divides the PHY (layer 1) into a PMD sublayer, a PMA sublayer, and a PCS. For example, optical transceivers are PMD sublayers. The PMA converts the data between the PMD sublayer and the PCS sublayer. The PCS is made up of coding (e.g., 8b/10b, 64b/66b) and serializer or multiplexing functions. Figure 10–2 shows the components of 10-Gigabit Ethernet and how Altera implements certain blocks and interfaces.

10-Gigabit Ethernet has three different implementations for the PHY: 10GBASE-X, 10GBASE-R, and 10GBASE-W. The 10GBASE-X implementation is a PHY that supports the XAUI interface. The XAUI interface used in conjunction with the XGMII extender sublayer (XGXS) allows more separation in distance between the MAC and PHY. 10GBASE-X PCS uses four lanes of 8b/10b coded data at a rate of

3.125 Gbps. 10GBASE-X is a wide wave division multiplexing (WWDM) LAN PHY. 10GBASE-R and 10GBASE-W are serial LAN PHYs and serial WAN PHYs, respectively. Unlike 10GBASE-X, 10GBASE-R and 10GBASE-W implementations have a XSBI interface and are described in more detail in the following section.

*Figure 10–2. 10-Gigabit Ethernet Block Diagram*



*Notes to Figure 10–2*

(1) The reconciliation sublayer (RS) interfaces the serial MAC data stream and the parallel data of XGMII.

(2) The XGMII extender sublayer (XGXS) extends the distance of XGMII when used with XUAI and provides the data conversion between XGMII and XAUI.

(3) The WAN interface sublayer (WIS) implements the OC-192 framing and scrambling functions.

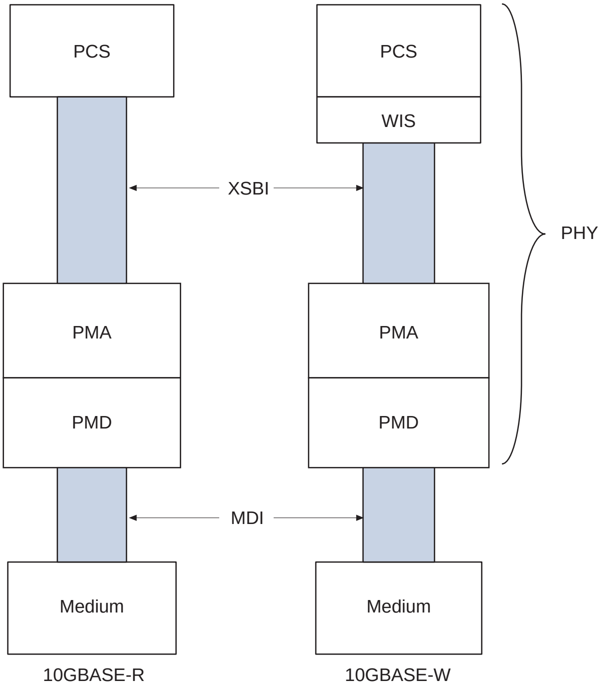
# Interfaces

The following sections discuss XSBI, PCS, XGMII, and XAUI.

## XSBI

One of the blocks of 10-Gigabit Ethernet is the XSBI interface. XSBI is the interface between the PCS and the PMA sublayers of the PHY layer of the OSI model. XSBI supports two types of PHY layers, LAN PHY and WAN PHY. The LAN PHY is part of 10GBASE-R, and supports existing Gigabit Ethernet applications at ten times the bandwidth. The WAN PHY is part of 10GBASE-W, and supports connections to existing and future installations of SONET/SDH circuit-switched access equipment. 10GBASE-R is a physical layer implementation that is comprised of the PCS sublayer, the PMA, and the PMD. 10GBASE-R is based upon 64b/66b data coding. 10GBASE-W is a PHY layer implementation that is comprised of the PCS sublayer, the WAN interface sublayer (WIS), the PMA, and the PMD. 10GBASE-W is based on STS-192c/SDH VC-4-64c encapsulation of 64b/66b encoded data. Figure 10–3 shows the construction of these two PHY layers.

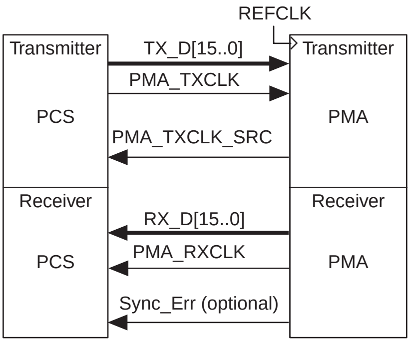
*Figure 10–3. XSBI Interface for the Two PHY Layers*



### *Functional Description*

XSBI uses 16-bit LVDS data to interface between the PCS and the PMA sublayer. Figure 10–4 shows XSBI between these two sublayers.

**Figure 10–4. XSBI Functional Block Diagram**



On the transmitter side, the transmit data (`TX_D[15..0]`) is output by the PCS and input at the PMA using the transmitter clock (`PMA_TXCLK`), which is derived from the PMA source clock (`PMA_TXCLK_SRC`). The PMA source clock is generated from the PMA with its reference clock (`REFCLK`). On the receiver side, the receiver data (`RX_D[15..0]`) is output by the PMA and input at the PCS using the PMA-generated receiver clock (`PMA_RXCLK`). The `SYNC_ERR` optional signal is sent to the PCS by the PMA if the PMA fails to recover the clock from the serial data stream.

The ratios for these two clocks and data are dependent on the type of PHY used. Table 10–1 shows the rates for both PHY types.

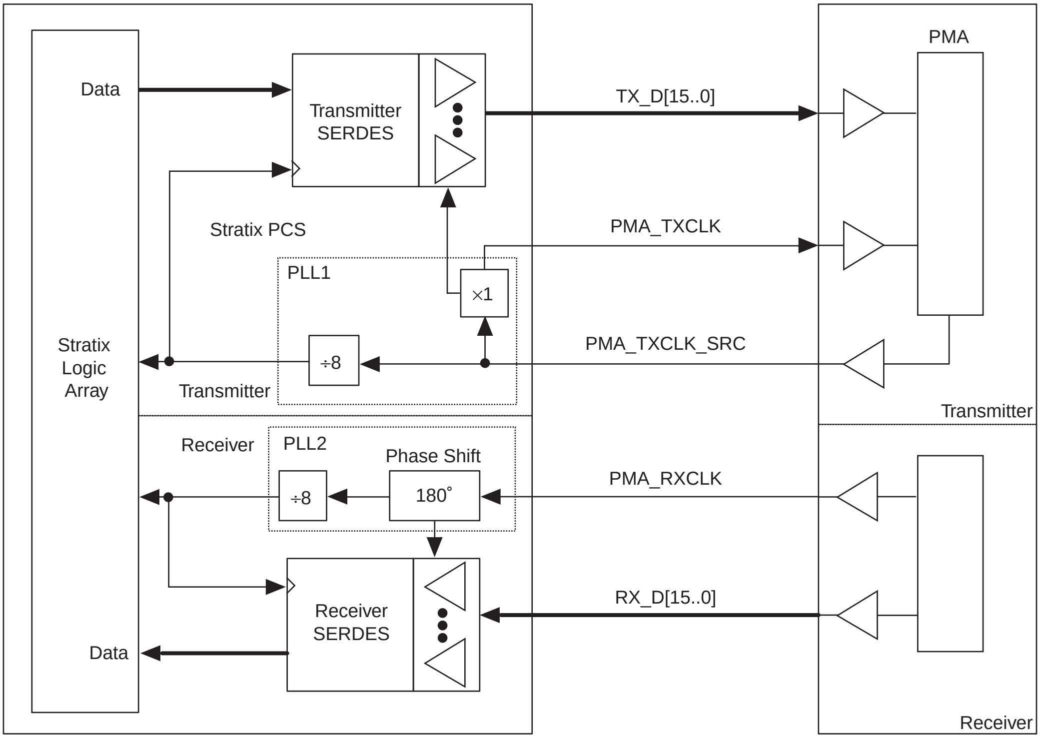
**Table 10–1. XSBI Clock & Data Rates for WAN & LAN PHY**

| Parameter | WAN PHY | LAN PHY | Unit |
|---|---|---|---|
| `TX_D[15..0]` | 622.08 | 644.53125 | Mbps |
| `PMA_TXCLK` | 622.08 | 644.53125 | MHz |
| `PMA_TXCLK_SRC` | 622.08 | 644.53125 | MHz |
| `RX_D[15..0]` | 622.08 | 644.53125 | Mbps |
| `PMA_RXCLK` | 622.08 | 644.53125 | MHz |

### *Implementation*

The 16-bit full duplex LVDS implementation of XSBI in Stratix devices is shown in Figure 10–5.

***Figure 10–5. Stratix Device XSBI Implementation***



The transmit serializer/deserializer (SERDES) clock comes from the transmitter clock source (`PMA_TXCLK_SRC`). The receiver SERDES clock comes from the PMA receiver recovered clock (`PMA_RXCLK`).

Figure 10–6 shows the transmitter output of the XSBI core. Data transmitted from the PCS to the PMA starts at the core of the Stratix device and travels to the Stratix transmitter SERDES block. The transmitter SERDES block converts the parallel data to serial data for 16 individual channels (`TX_D[15..0]`). The PMA source clock (`PMA_TXCLK_SRC`) is used to clock out the signal data. `PMA_TXCLK` is generated from the same phase-locked loop (PLL) as the data, and it travels to the PMA at the same rate as the data. By using one of the data channels in the middle of the bus as the clock (in this case, the eighth channel CH8), the clock-to-data skew improves.

*Figure 10–6. Stratix Device XSBI Transmitter Implementation*

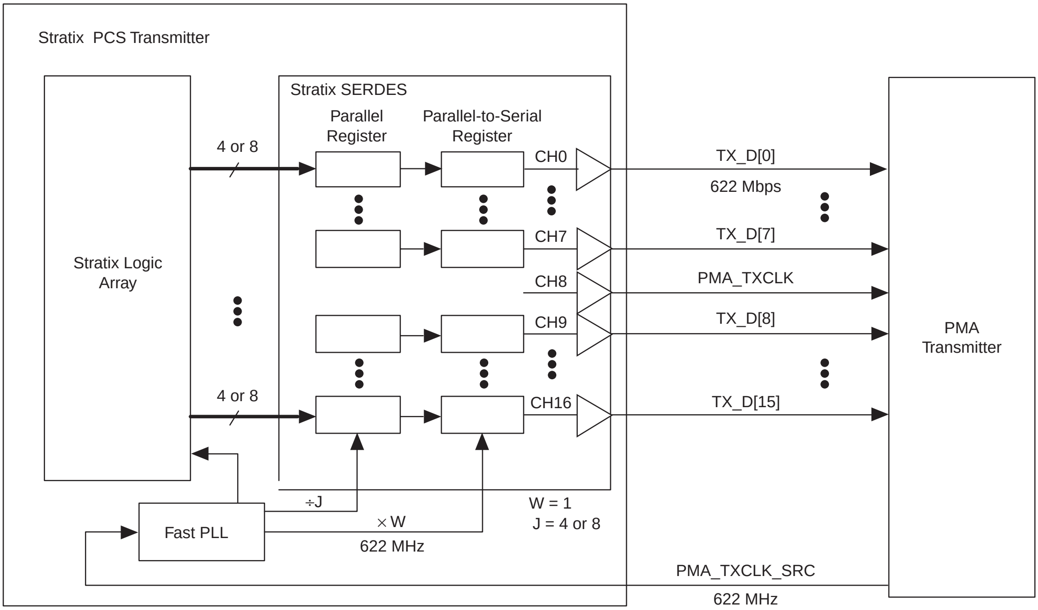
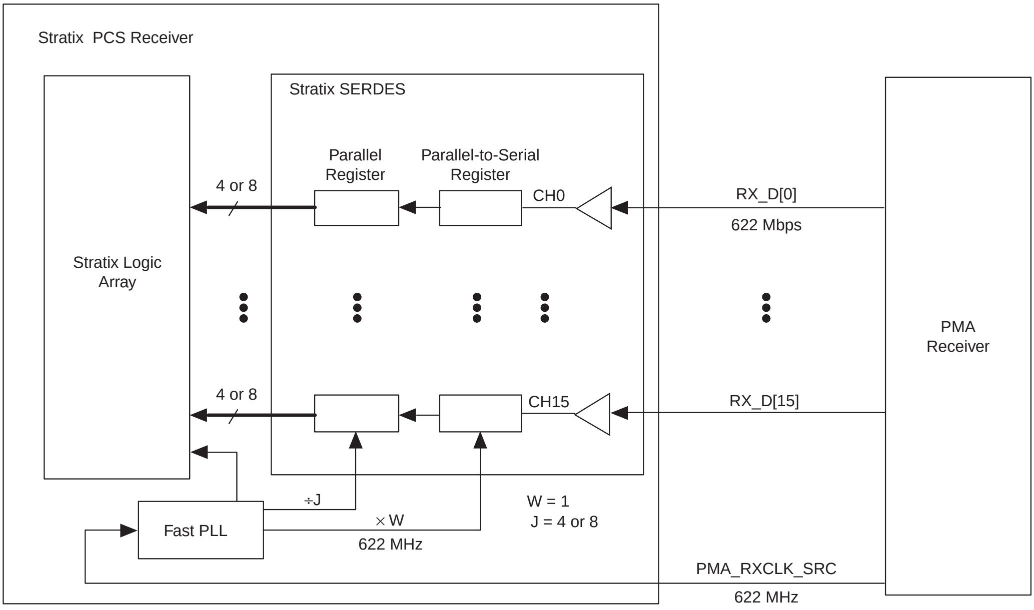


Figure 10–7 shows the receiver input of the XSBI core. From the receiver side, data (`RX_D[15..0]`) comes from the PMA to the Stratix receiver SERDES block along with the PMA receiver clock (`PMA_RXCLK`). The PMA receiver clock is used to convert the serial data to parallel data. The phase shift or inversion on the PMA receiver clock is needed to capture the receiver data.

Stratix devices contain up to eight fast PLLs. These PLLs provide high-speed outputs for high-speed differential I/O support as well as general-purpose clocking with multiplication and phase shifting. The fast PLL incorporates this 180° phase shift. The Stratix device’s data realignment feature enables you to save more logic elements (LEs). This feature provides a byte-alignment capability, which is embedded inside the SERDES. The data realignment circuitry can correct for bit misalignments by slipping data bits.

For more information about fast PLLs, refer to Section I, Stratix Device Family Data Sheet of the *Stratix Device Handbook, Volume 1*.

*Figure 10–7. Stratix XSBI Receiver Implementation*



With this XSBI transmitter and receiver block implementation, each XSBI core requires two fast PLLs. The potential number of XSBI cores per device corresponds to the number of fast PLLs each Stratix device contains. Table 10–2 shows the number of LVDS channels, the number of fast PLLs, and the number of XSBI cores that can be supported for each Stratix device.

*Table 10–2. Stratix Device XSBI Core Support*

| Stratix Device | Number of LVDS Channels (Receive/Transmit) *(1)*, *(2)* | Number of Fast PLLs | Number of XSBI Interfaces (Maximum) |
|---|---|---|---|
| EP1S10 | 44/44 | 4 | 2 |
| EP1S20 | 66/66 | 4 | 2 |
| EP1S25 | 78/78 | 4 | 2 |
| EP1S30 | 82/82 | 8 | 4 |
| EP1S40 | 90/90 | 8 | 4 |
| EP1S60 | 116/116 | 8 | 4 |
| EP1S80 | 80/40 | 8 | 4 |

***Notes to Table 10–2:***

(1) Preliminary data.

(2) The LVDS channels can go up to 840 Mbps.

### AC Timing Specifications

Stratix devices support a PCS interface. Figures 10–8 and 10–9 and Tables 10–3 and 10–4 illustrate timing characteristics of the PCS transmitter and receiver interfaces.

Figure 10–8 shows the AC timing diagram for the Stratix PCS transmitter. You can determine PCS channel-to-channel skew by adding the data invalid window before the rising edge ($T_{cq\_pre}$) to the data invalid window after the rising edge ($T_{cq\_post}$).

### *Figure 10–8. PCS Transmitter Timing Diagram*

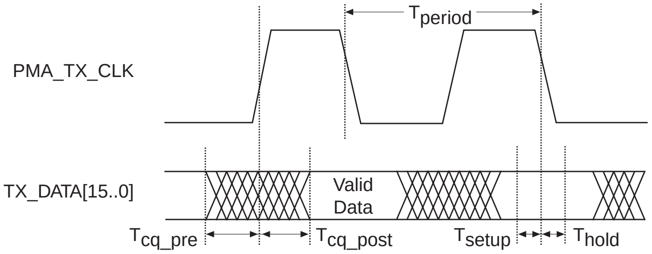


Table 10–3 lists the AC timing specifications for the PCS transmitter.

### *Table 10–3. PCS Transmitter Timing Specifications*

| Parameter | Value | | | Unit |
|---|---|---|---|---|
| | Min | Typ | Max | |
| `PMA_TX_CLK` $T_{period}$ (WAN) | | 1,608 | | ps |
| `PMA_TX_CLK` $T_{period}$ (LAN) | | 1,552 | | ps |
| Data invalid window before the rising edge ($T_{cq\_pre}$) | | | 200 | ps |
| Data invalid window after the rising edge ($T_{cq\_post}$) | | | 200 | ps |
| `PMA_TX_CLK` duty cycle | 40 | | 60 | % |
| PCS transmitter channel-to-channel skew | | | 400 | ps |

Figure 10–9 shows the AC timing diagram for the Stratix PCS receiver interface. You can determine the PCS sampling window by adding $T_{setup}$ to $T_{hold}$. Receiver skew margin (RSKM) refers to the amount of skew tolerated on the printed circuit board (PCB).

### *Figure 10–9. PCS Receiver Timing Diagram*

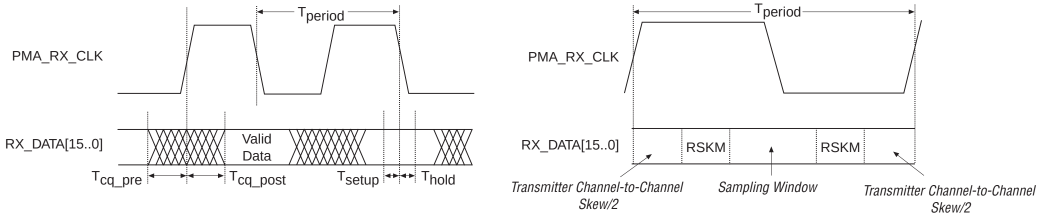


Table 10–4 lists the AC timing specifications for the PCS receiver interface.

*Table 10–4. PCS Receiver Timing Specifications*

| Parameter | Value | | | Unit |
|---|---|---|---|---|
| | Min | Typ | Max | |
| `PMA_RX_CLK` $T_{period}$ (WAN) | | 1,608 | | ps |
| `PMA_RX_CLK` $T_{period}$ (LAN) | | 1,552 | | ps |
| Data invalid window before the rising edge ($T_{cq\_pre}$) | | | 200 | ps |
| Data invalid window after the rising edge ($T_{cq\_post}$) | | | 200 | ps |
| `PMA_RX_CLK` duty cycle | 45 | | 55 | % |
| Data set-up time ($T_{setup}$) | 300 | | | ps |
| Data hold time ($T_{hold}$) | 300 | | | ps |
| PCS sampling window | 600 | | | ps |
| RSKM (WAN) | | | 304 | ps |
| RSKM (LAN) | | | 276 | ps |

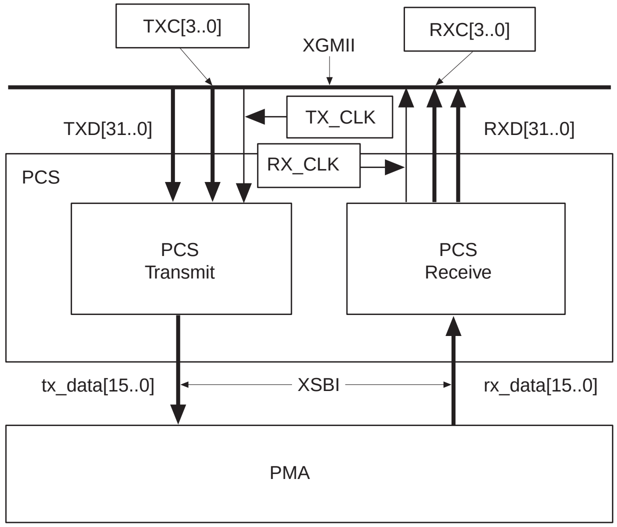
## XGMII

The purpose of XGMII is to provide a simple, inexpensive, and easy to implement interconnection between the MAC sublayer and the PHY. Though XGMII is an optional interface, it is used extensively in the 10-Gigabit Ethernet standard as the basis for the specification. The conversion between the parallel data paths of XGMII and the serial MAC data stream is carried out by the reconciliation sublayer. The reconciliation sublayer maps the signal set provided at the XGMII to the physical layer signaling (PLS) service primitives provided at the MAC. XGMII supports a 10-Gbps MAC data rate.

### *Functional Description*

The XGMII is composed of independent transmit and receive paths. Each direction uses 32 data signals, `TXD[31..0]` and `RXD[31..0]`, 4 control signals, `TXC[3..0]` and `RXC[3..0]`, and a clock `TX_CLK` and `RX_CLK`. Figure 10–10 shows the XGMII functional block diagram.

*Figure 10–10. XGMII Functional Block Diagram*



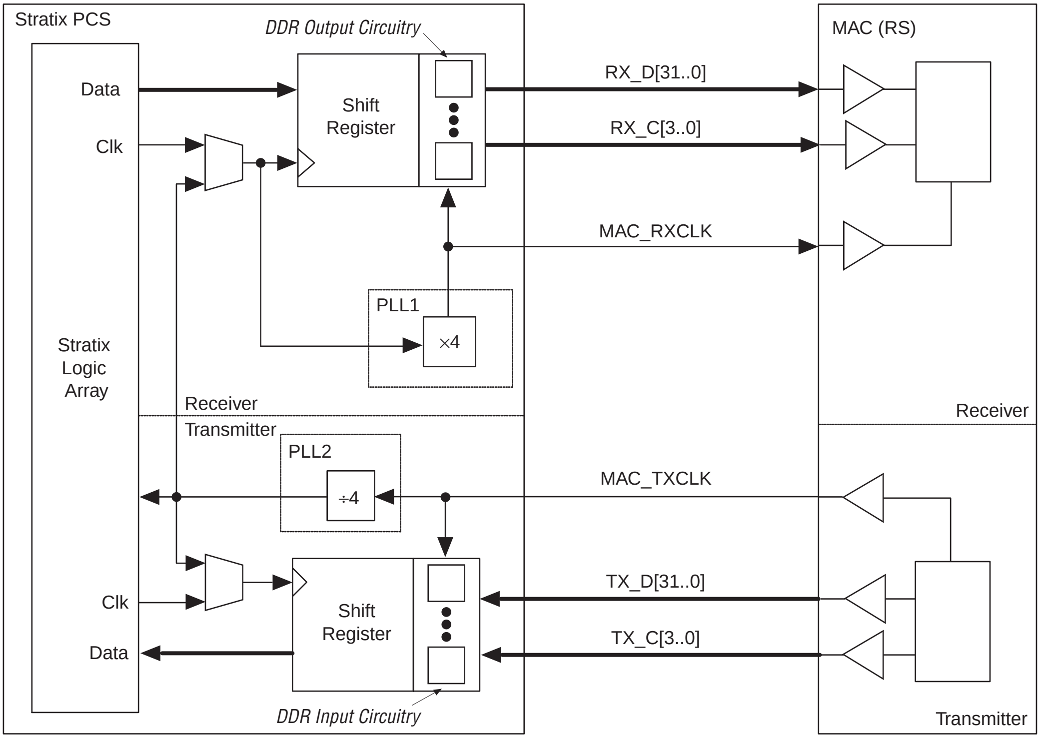
The 32 `TXD` and four `TXC` signals as well as the 32 `RXD` and four `RXC` signals are organized into four data lanes. The four lanes in each direction share a common clock (`TX_CLK` for transmit and `RX_CLK` for receive). The four lanes are used in round-robin sequence to carry an octet stream (8 bits of data per lane). The reconciliation sublayer generates continuous data or control characters on the transmit path and expects continuous data or control characters on the receive path.

### Implementation

XGMII uses the 1.5-V HSTL I/O standard. Stratix devices support the 1.5-V HSTL Class I and Class II I/O standard (EIA/JESD8-6). The standard requires a differential input with an external reference voltage ($V_{REF}$) of 0.75 V, as well as a termination voltage $V_{TT}$ of 0.75 V, to which termination resistors are connected. The HSTL Class I standard requires a 1.5-V $V_{CCIO}$ voltage, which is supported by Stratix devices.

Figure 10–11 shows the 32-bit full-duplex 1.5-V HSTL implementation of XGMII.

*Figure 10–11. Stratix XGMII Implementation*



For this implementation, the shift register clocks can either be generated from a divided down MAC reconciliation sublayer transmitter clock (`MAC_TXCLK`), or the asynchronous core clock, or both if using a FIFO buffer.

Figure 10–12 shows one channel of the output half of XGMII. Data that is transmitted from the PCS to the MAC reconciliation sublayer starts at the core of the Stratix device and travels to the shift register. The shift register takes in the parallel data (even bits sent to the top register and odd bits sent to the bottom register) and serializes the data. After the data is serialized, it travels to the double data rate (DDR) output circuitry, which is clocked with the ×4 clock from the PLL. Out of the DDR output circuitry, the data drives off-chip along with the ×4 clock. This transaction creates the DDR relationship between the clock and the data output. This implementation only shows one channel, but can be duplicated to include all 32 bits of the `RX_D` signal and all 4 bits of the `RX_C` signal.

*Figure 10–12. Stratix XGMII Output Implementation (One Channel)*

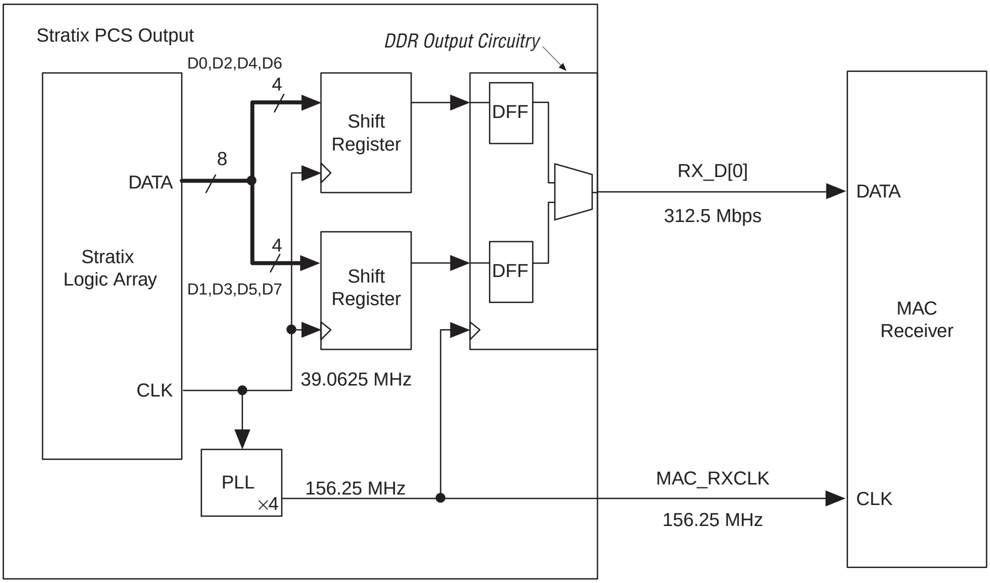
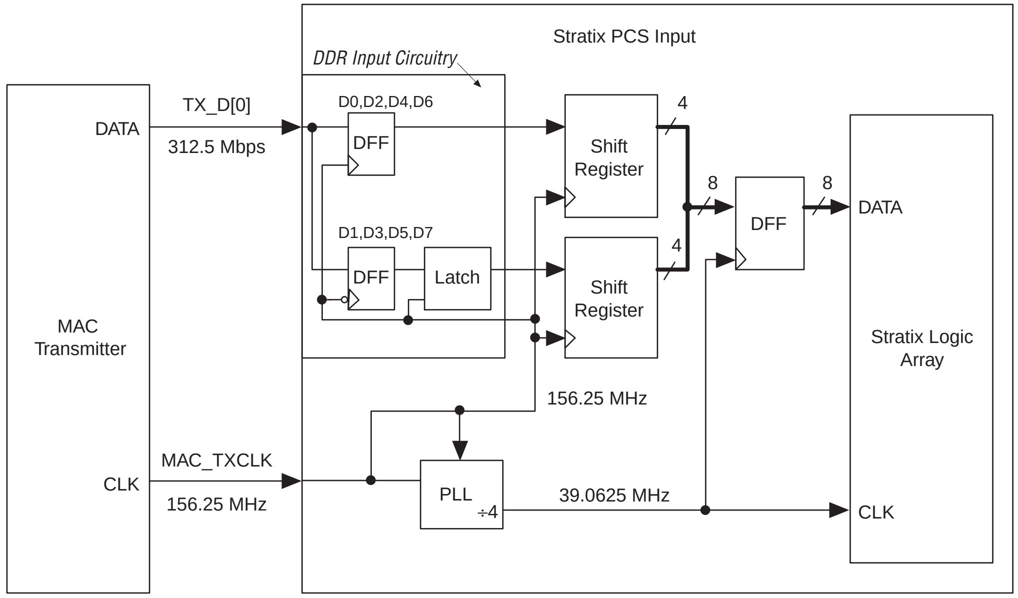


Figure 10–13 shows one channel of the input half of the XGMII interface. From the receiver side, the DDR data is captured from the MAC to the Stratix PCS DDR input circuitry. The serial data is separated into two individual data streams with the even bits routed to the top register and odd bits routed to the bottom register. The DDR input circuitry produces two output data streams that go into the shift registers. From the shift registers, the data is deserialized using the clock from the MAC, combining into an 8-bit word. This parallel data goes to a register that is clocked by the divide-by-4 clock from the PLL. This data and clock go to the Stratix core. This implementation shows only one channel, but can be duplicated to include all 32 bits of the `TX_D` signal and all 4 bits of the `TX_C` signal.

***Figure 10–13. Stratix XGMII Input Implementation (One Channel)***



Stratix devices contain up to four enhanced PLLs. These PLLs provide features such as clock switchover, spread-spectrum clocking, programmable bandwidth, phase and delay control, and PLL reconfiguration. Since the maximum clock rate is 156.25 MHz, you can use a fast or enhanced PLL for both the XGMII output and input blocks.

For more information about fast PLLs, refer to Section I, Stratix Device Family Data Sheet of the *Stratix Device Handbook, Volume 1*.

With this implementation for the XGMII output and input blocks, the number of XGMII cores per device corresponds to the number of PLLs each Stratix device contains. Table 10–5 shows the number of 1.5-V HSTL I/O pins, PLLs, and XGMII cores that are supported in each Stratix device. Each core requires 72 1.5-V HSTL I/O pins for data and control and 2 clock pins for the transmitter and receiver clocks. Each XGMII core also needs two PLLs (one for each direction).

*Table 10–5. Stratix XGMII Core Support*

| Stratix Device | Number of 1.5-V HSTL Class I I/O Pins | Number of Fast & Enhanced PLLs | Number of XGMII Interfaces |
|---|---|---|---|
| EP1S10 | 410 | 6 | 3 |
| EP1S20 | 570 | 6 | 3 |
| EP1S25 | 690 | 6 | 3 |
| EP1S30 | 718 | 10 | 5 |
| EP1S40 | 814 | 12 | 6 |
| EP1S60 | 1,014 | 12 | 6 |
| EP1S80 | 1,195 | 12 | 6 |

### Reduced System Noise

The output buffer of each Stratix device I/O pin has a programmable drive strength control for certain I/O standards. The 1.5-V HSTL Class I standard supports the minimum setting, which is the lowest drive strength that guarantees $I_{OH}$ and $I_{OL}$ of the standard. Using minimum settings provides signal slew rate control to reduce system noise and signal overshoot.

For more information on $I_{OH}$ and $I_{OL}$ values, refer to "Operating Conditions" in Section I, Stratix Device Family Data Sheet of the *Stratix Device Handbook, Volume 1*.

### On-Chip Termination Support

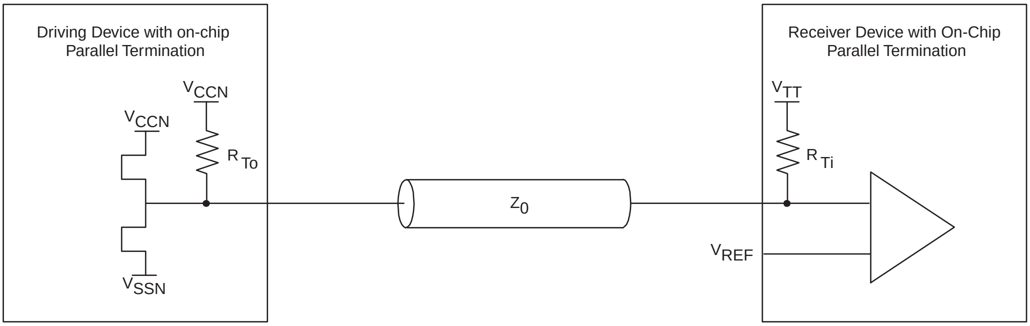
Stratix devices provide a Terminator™ technology capability for on-chip parallel termination support for 1.5-V HSTL (Class I and II). Terminator technology can be used at the drivers and receivers to avoid implementing an external pull-up termination resistor. Table 10–6 describes the values of on-chip termination used by the 1.5-V HSTL I/O standard. Terminator technology supports only one type of on-chip termination I/O standard per given I/O bank.

*Table 10–6. HSTL Class I Termination*

| I/O Standard | On-Chip Termination | $R_{To}$ | $R_{Ti}$ | $V_{CCN}$ |
|---|---|---|---|---|
| HSTL Class I | HSTL_I_OCT | – | 50 Ω | 1.5 V |

Figure 10–14 describes the circuit topology for HSTL.

*Figure 10–14. HSTL Circuit Topology*



### Timing

XGMII signals must meet the timing requirements shown in Figure 10–15. Make all XGMII timing measurements at the driver output with the optional termination (shown in Figure 10–14) and a capacitive load from all sources of 20 pF that are specified relative to the $V_{IL}$_AC(max) and $V_{IH}$_AC(min) thresholds.

*Figure 10–15. XGMII Timing Diagram*

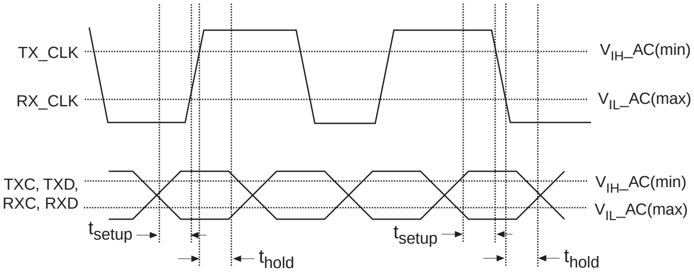


Table 10–7 shows the XGMII timing specifications.

**Table 10–7. XGMII Timing Specifications** *Note (1)*

| Symbol | Driver | Receiver | Unit |
|---|---|---|---|
| $T_{setup}$ | 960 | 480 | ps |
| $T_{hold}$ | 960 | 480 | ps |

*Note to Table 10–7*

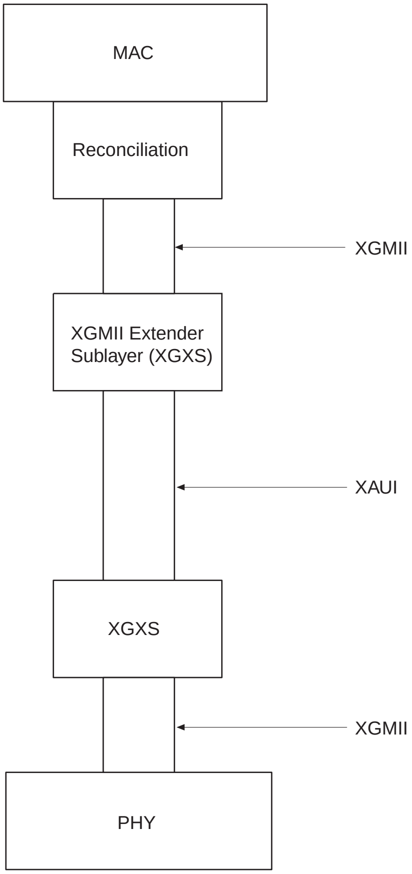
(1) The actual set-up and hold times will be made available after device characterization is complete.

Stratix devices support DDR data with clock rates of up to 200 MHz, well above the XGMII clock rate of 156.25 MHz. For the HSTL Class I I/O standard, Stratix device I/O drivers provide a 1.0-V/ns slew rate at the input buffer of the receiving device.

## XAUI

XAUI (pronounced Zowie) is located between the XGMII at the reconciliation sublayer and the XGMII at the PHY layer. Figure 10–16 shows the location of XAUI. XAUI is designed to either extend or replace XGMII in chip-to-chip applications of most Ethernet MAC to PHY interconnects.

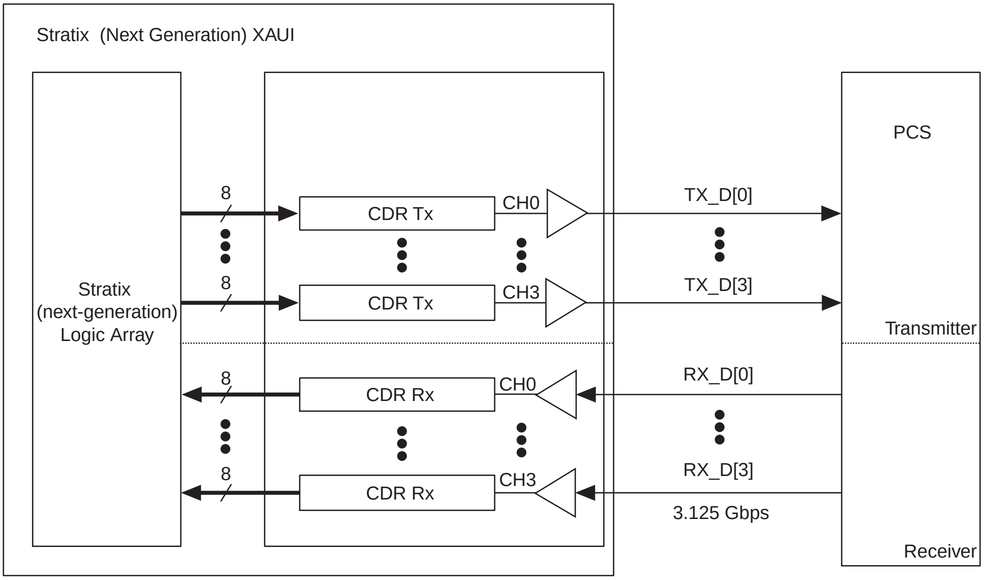
*Figure 10–16. XAUI Location*



### *Functional Description*

XAUI can replace the 32 bits of parallel data required by XGMII for transmission with just 4 lanes of serial data. XAUI uses clock data recovery (CDR) to eliminate the need for separate clock signals. 8b/10b encoding is employed on the data stream to embed the clock in the data. The 8b/10b protocol to encode an 8-bit word stream to 10-bit codes that results in a DC-balanced serial stream and eases the receiver synchronization. To support 10-Gigabit Ethernet, each lane must run at a speed of at least 2.5 Gbps. Using 8b/10b encoding increases the rate for each lane to 3.125 Gbps, which will be supported in next-generation Stratix devices. Figure 10–17 shows how XAUI will be implemented.

*Figure 10–17. Next-Generation Stratix XAUI Implementation*



## I/O Characteristics for XSBI, XGMII & XAUI

The three interfaces of 10-Gigabit Ethernet (XSBI, XGMII, and XAUI) each have different rates and I/O standards. Table 10–8 shows the characteristics for each interface.

*Table 10–8. 10-Gigabit Ethernet Interfaces Characteristics*

| Interface | Width | Clock Rate (MHz) | Data Rate Per Channel | Clocking Scheme | I/O Type |
|---|---|---|---|---|---|
| XGMII | 32 | 156.25 | 312.5 Mbps | DDR source synchronous | 1.5-V HSTL |
| XSBI | 16 | 644.5 or 622.08 | 644.5 or 622.08 Mbps | SDR source synchronous | LVDS |
| XAUI | 4 | None | 3.125 Gbps | Clock data recovery (CDR) | 1.5-V PCML |

## Software Implementation

You can use the **Assignment Organizer** in the Altera® Quartus® II software to implement the I/O standards for a particular interface. For example, set the I/O standard to LVDS for XSBI and to HSTL Class I for XGMII. You can use the MegaWizard® Plug-In Manager to create the PLLs and transmitter and receiver SERDES blocks for the XSBI implementation and PLLs and DDR input and output circuitry for the XGMII implementation. For more information on the Assignment Organizer or MegaWizard Plug-In Manager, refer to Quartus II Help.

## AC/DC Specifications

Table 10–9 lists the XSBI DC electrical characteristics, similar to Stratix devices, that are based on the ANSI/TIA-644 LVDS specification.

*Table 10–9. XSBI DC Specifications*

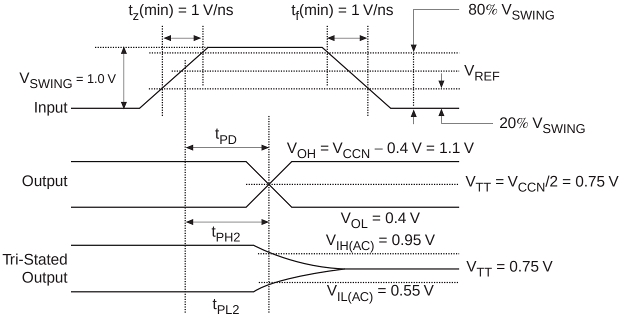
| Parameter | Value | | | Unit |
|---|---|---|---|---|
| | Min | Typ | Max | |
| Output differential voltage ($V_{OD}$) | 250 | | 400 *(1)* | mV |
| Output offset voltage ($V_{OS}$) | 1,125 | | 1,375 | mV |
| Output Impedance, single ended | 40 | | 140 | W |
| Change in $V_{OD}$ between ‘0’ and ‘1’ | | | 50 | mV |
| Change in $V_{OS}$ between ‘0’ and ‘1’ | | | 50 | mV |
| Input voltage range ($V_I$) | 900 | | 1,600 | mV |
| Differential impedance | | 100 | | W |
| Input differential voltage ($V_{ID}$) | 100 | | 600 | mV |
| Receiver differential input impedance | 70 | | 130 | W |
| Ground potential difference (between PCS and PMA) | | | 50 | mV |
| Rise and fall times (20% to 80%) | 100 | | 400 | ps |

*Note to Table 10–9:*

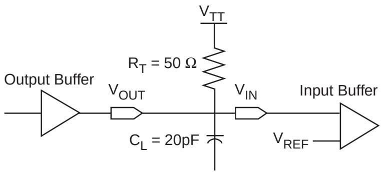
(1) Larger $V_{OD}$ is possible for better signal intensity.

I/O characteristics for the 1.5-V HSTL standard for Stratix devices are shown in Figure 10–18 and comply with XGMII electrical specifications available in 10-Gigabit Ethernet draft IEEE P802.3ae.

*Figure 10–18. Electrical Characteristics for Stratix Devices (1.5-V HSTL Class I)*



HSTL AC Load Circuit for Class I



HSTL AC Waveform & I/O Interface

Table 10–10 lists the DC specifications for Stratix devices (1.5-V HSTL Class I).

*Table 10–10. DC Specifications for Stratix Devices (1.5-V HSTL Class I) Note (1)*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | I/O supply voltage | | 1.4 | 1.5 | 1.6 | V |
| $V_{REF}$ | Input reference voltage | | 0.68 | 0.75 | 0.9 | V |
| $V_{TT}$ | Termination voltage | | 0.7 | 0.75 | 0.8 | V |
| $V_{IH}$ (DC) | DC high-level input voltage | | $V_{REF} + 0.1$ | | | V |
| $V_{IL}$ (DC) | DC low-level input voltage | | –0.3 | | $V_{REF} - 0.1$ | V |
| $V_{IH}$ (AC) | AC high-level input voltage | | $V_{REF} + 0.2$ | | | V |
| $V_{IL}$ (AC) | AC low-level input voltage | | | | $V_{REF} - 0.2$ | V |
| $I_I$ | Input pin leakage current | $0 < V_{IN} < V_{CCIO}$ | –10 | | 10 | µA |
| $V_{OH}$ | High-level output voltage | $I_{OH} = -8$ mA | $V_{CCIO} - 0.4$ | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL} = 8$ mA | | | 0.4 | V |
| $I_O$ | Output leakage current (when output is high Z) | $GND \leq V_{OUT} \leq V_{CCIO}$ | –10 | | 10 | µA |

***Note to Table 10–10:***

(1) Drive strength is programmable according to values shown in Section I, Stratix Device Family Data Sheet of the *Stratix Device Handbook, Volume 1*.

## 10-Gigabit Ethernet MAC Core

As an Altera Megafunction Partners Program (AMPP$^{SM}$) member, MorethanIP provides a 10-Gigabit Ethernet MAC core for Altera customers. MorethanIP’s 10-Gigabit Ethernet MAC core implements the RS, the MAC layer, and user-programmable FIFO buffers for clock and data decoupling.

### *Core Features*

MorethanIP’s 10-Gigabit Ethernet MAC core provides the following features:

- Includes automatic pause frame generation (per IEEE 802.3 ×31) with user-programmable pause quanta and pause-frame termination
- Includes a programmable 48-bit MAC address with a promiscuous mode option, and a programmable Ethernet frame length that supports IEEE 802.1Q VLAN-tagged frames or jumbo Ethernet frames

- Supports broadcast traffic and multi-cast address resolution with a 64-entry hash table
- Compliant with the IEEE802.3ae Draft 4.0
- Implements XGMII, allowing it to interface to XAUI through a 10-Gigabit commercial SERDES

## Conclusion

10-Gigabit Ethernet takes advantage of the existing Gigabit Ethernet standard. With its rich I/O features, Stratix devices supports the components of 10-Gigabit Ethernet as well as XSBI and XGMII. With the next-generation of Stratix devices, XAUI will also be supported. These interfaces are easily implemented using Stratix's core architecture, differential I/O capabilities, and superior PLLs.

# 11. Implementing SFI-4 in Stratix Devices

S52011-1.0

Chapter 11, Implementing SFI-4 in Stratix Devices replaces *AN 219: Implementing SFI-4 in Stratix Devices.*

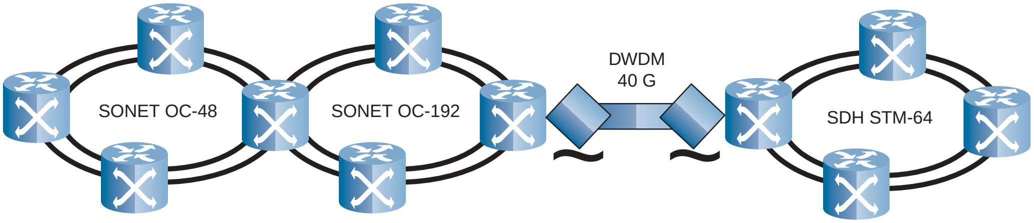
## Introduction

The growth of the Internet has created huge bandwidth demands as voice, video, and data push the limits of the existing wide area network (WAN) backbones. To facilitate this bandwidth growth, speeds of OC-192 and higher are being deployed in WAN backbones (see Figure 11–1). Today's carrier backbone networks are supported by SONET/SDH transmission technology. SONET/SDH is a transmission technology for transporting optical signals at speeds ranging from 51 megabits per second (Mbps) up to 40 gigabits per second (Gbps). SONET/SDH rings make up the majority of the existing backbone infrastructure of the Internet and the public switched telephone network (PSTN).

The Optical Internetworking Forum (OIF) standard SFI-4 is a 16-bit LVDS interface used in an OC-192 SONET system to link the framer and the serializer/deserializer (SERDES). Stratix™ devices support the required data rates of up to 622.08 Mbps along with the one-to-one relationship required between clock frequency and data rate. The Stratix fast phase-locked loop (PLL) was designed to support the high clock frequencies and the one-to-one relationship (between clock and data rate) needed for interfaces such as XSBI and SFI-4. Support for SFI-4 extends the reach of high-density programmable logic from the backplane to the physical layer (PHY) devices.

This chapter will focus on the implementation of the interface between the SERDES and the framer.

*Figure 11–1. WAN Backbone*



A SONET/SDH transmission network is composed of several pieces of equipment, including terminal multiplexers, add-drop multiplexers, and repeater and digital cross-connect systems. SONET is the standard used in North America and SDH is the standard used outside North America. The SONET/SDH specification outlines the frame format, multiplexing method, synchronization method, and optical interface between the equipment, as well as the specific optical interface.

SONET/SDH continues to play a key role in the next generation of networks for many carriers. In the core network, the carriers offer services such as telephone, dedicated leased lines, and Internet protocol (IP) data, which are continuously transmitted. The individual data channels are not transmitted on separate lines; instead, they are multiplexed into higher speeds and transmitted on SONET/SDH networks at the corresponding transmission speed.

Figure 11–2 shows a typical SONET/SDH line card. The system operates as follows:

1. The SONET/SDH line card first takes a high-speed serial optical signal and converts it into a high-speed serial electrical signal. The devices are called physical media dependent (PMD) devices.

2. The system then recovers the clock from the electrical data using a clock data recovery (CDR) unit.

3. The SERDES parallelizes the data so that it can be manipulated easily at lower clock rates.

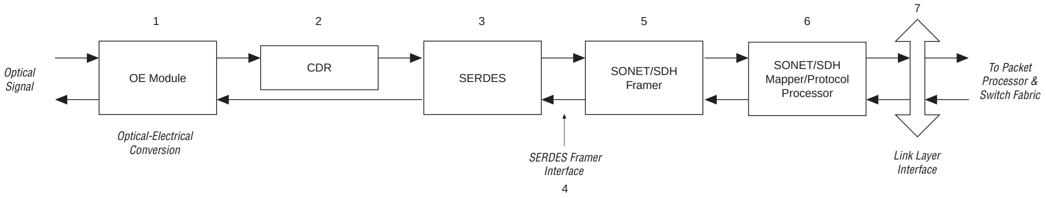
4. The interface between the SERDES and framer is called the SERDES framer interface. The interface requirements are defined by the OIF.

5. The framer identifies the beginning of the SONET/SDH frames and monitors the performance of the system.

6. The mapper following the framer maps asynchronous transfer mode (ATM) cells, IP packets, or T/E carrier signals into the SONET frame.

7. The PHY-link layer interface provides a bus interface to packet/cell processors or other link-layer devices.

*Figure 11–2. SONET/SDH Line Card*

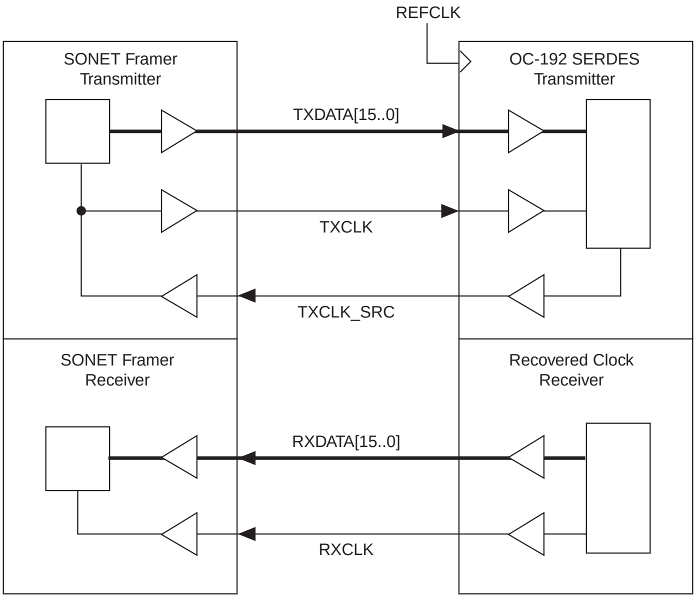


The OIF has defined the electrical interface (SFI) between the SONET/SDH framer and high-speed SERDES devices. To keep up with evolving transmission speeds and technology enhancements, different versions of electrical interfaces are defined. SFI-4 is the version of SFI that acts as an interface between an OC-192 SERDES and SONET framer, as shown in Figure 11–2. An aggregate of 9953.28 Mbps is transferred in each direction. With their differential I/O capabilities, Stratix devices are ideally suited to support the framer side of the SFI-4 interface. Support for SFI-4 extends the reach of high-density programmable logic from the backplane to the PHY devices.

## System Topology

The SFI-4 interface uses 16 channels of source-synchronous LVDS to interface between a SONET framer and an OC-192 SERDES. Figure 11–3 shows the SFI-4 interface.

*Figure 11–3. SFI-4 Interface Signals*



The framer transmits outbound data via `TXDATA[15..0]` and is received at the SERDES using `TXCLK`. `TXCLK` is derived from `TXCLK_SRC`, which is provided by the OC-192 SERDES. The framer receives incoming data on `RXDATA[15..0]` from the OC-192 SERDES. The data received is latched on the rising edge of `RXCLK`. Table 11–1 provides the data rates and clock frequencies specified by SFI-4. The modes of `TXCLK` are specified by the SFI-4 standard. In required mode (622 MHz clock mode or ×1 mode), `TXCLK` should run at 622.08 MHz. In optional mode (311 MHz clock mode or ×2 mode), `TXCLK` should run at 311.04 MHz.

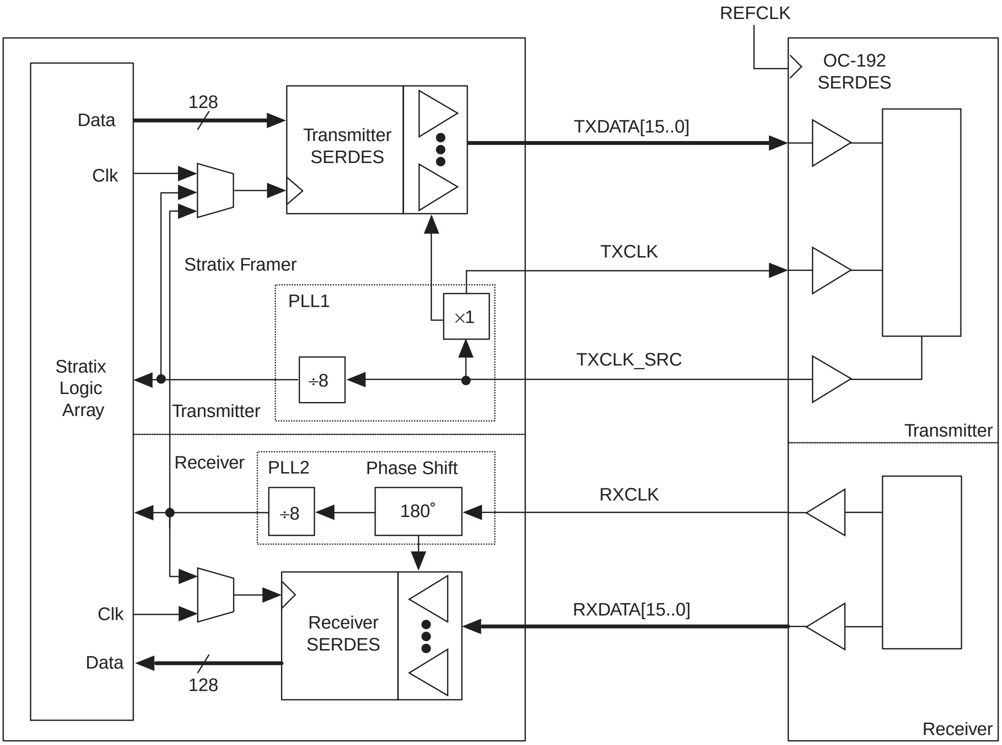
*Table 11–1. SFI-4 Interface Data Rates & Clock Frequencies*

| Signal | Performance |
|---|---|
| `TXDATA[15..0]` | 622.08 Mbps |
| `TXCLK` | 622.08 MHz or 311.04 MHz |
| `TXCLK_SRC` | 622.08 MHz |
| `RXDATA[15..0]` | 622.08 Mbps |
| `RXCLK` | 622.08 MHz |
| `REFCLK` | 622.08 MHz |

## Interface Implementation in Stratix Devices

The 16-bit full-duplex LVDS implementation of the framer part of the SFI-4 interface is shown in Figure 11–4. Stratix devices support source-synchronous interfacing and LVDS differential signaling up to 840 Mbps. Stratix devices have embedded SERDES circuitry for serial and parallel data conversion. The Stratix fast PLL enables 622.08 Mbps data transmission by transmitting and receiving a differential clock at rates of up to 645 MHz. The clocks required in the SERDES for parallel and serial data conversion can be configured from the received `RXCLK` (divided down), the `TXCLK_SRC` (divided down), or the asynchronous core clock. See Figure 11–4.

*Figure 11–4. Implementation of SFI-4 Interface Using Stratix Devices*



For details on differential I/O buffers, SERDES, and clock dividers using PLLs, refer to Chapter 5, Using High-Speed Differential I/O Interfaces in Stratix Devices.

Figure 11–5 shows the transmitter block (from Figure 11–4) of the SFI-4 framer interface implemented in Stratix devices. The data starts in the logic array and goes into the Stratix SERDES block. The transmitter SERDES of the framer converts the parallel data to serial data for the 16 `TXDATA` channels (`TXDATA[15..0]`). A fast PLL is used to generate `TXCLK` from `TXCLK_SRC`. The fast PLL keeps the `TXDATA` and `TXCLK` edge-aligned. A divided down (÷8) clock generated from `TXCLK_SRC` is used to convert the parallel data to serial in the transmitter SERDES. The divided down clock also clocks some of the logic in the logic array.

*Figure 11–5. Framer Transmitter Interface in Stratix Devices*

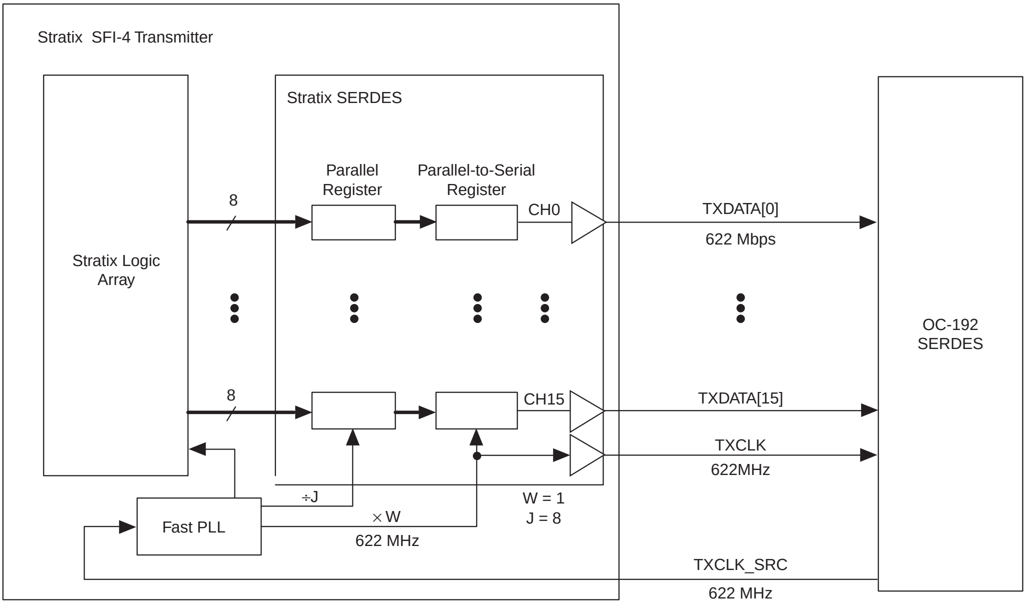
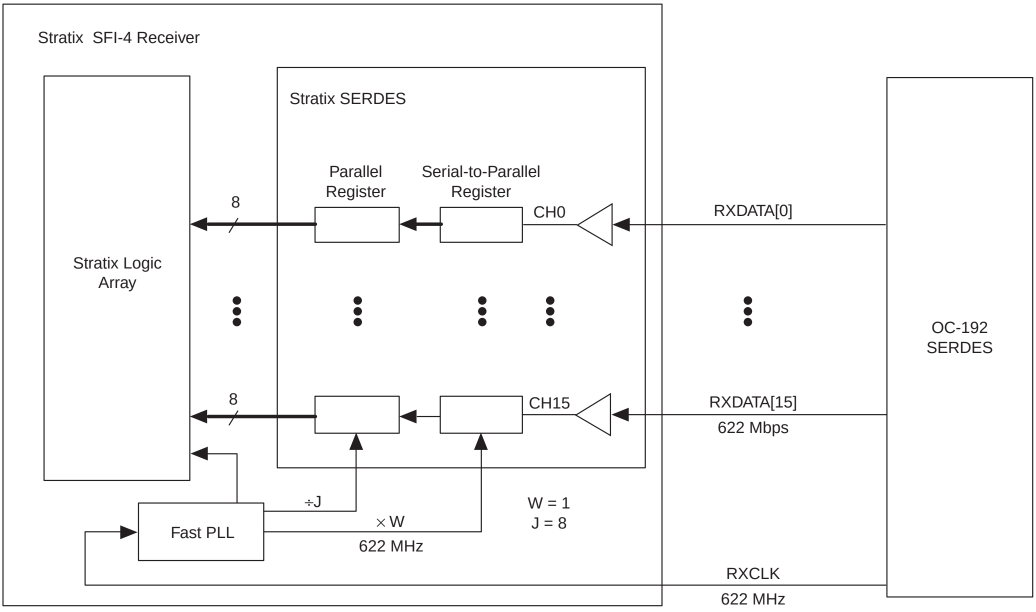


Figure 11–6 shows the receiver block (from Figure 11–4) of the SFI-4 framer interface implemented in Stratix devices. `RXDATA[15..0]` is received from the OC-192 SERDES on the differential I/O pins of the Stratix device. The receiver SERDES converts the high-speed serial data to parallel. You can generate the clocks required in the SERDES for parallel and serial data conversion from the received `RXCLK`. `RXCLK` is inverted (phase-shifted by 180°) to capture received data. While normal I/O operation guarantees that data is captured, it does not guarantee the parallelization boundary, which is randomly determined based on the power up of both communicating devices. The SERDES in Stratix devices has embedded data realignment capability, which can be used to save logic elements (LEs).

*Figure 11–6. Framer Receiver Interface in Stratix Devices*



For more information on the byte-alignment feature in Stratix devices, refer to Chapter 5, Using High-Speed Differential I/O Interfaces in Stratix Devices.

Table 11–2 lists the number of SFI-4 cores that can be implemented in a Stratix device. Refer to Chapter 5, Using High-Speed Differential I/O Interfaces in Stratix Devices for the package type and the maximum number of channels supported by each package.

***Table 11–2. Stratix SFI-4 Core Support***

| Stratix Device | Number of LVDS Channels (Receiver/Transmitter) *(1), (2)* | Number of PLLs | Number of SFI-4 Interfaces (Maximum) |
|---|---|---|---|
| EP1S10 | 44/44 | 4 | 2 |
| EP1S20 | 66/66 | 4 | 2 |
| EP1S25 | 78/78 | 4 | 2 |
| EP1S30 | 82/82 | 8 | 4 |
| EP1S40 | 90/90 | 8 | 4 |
| EP1S60 | 116/116 | 8 | 4 |
| EP1S80 | 80/40 | 8 | 4 |

***Notes to Table 11–2:***

(1) Preliminary data.

(2) The LVDS channels can go up to 840 Mbps.

## AC Timing Specifications

Figures 11–7 through 11–9 and Tables 11–3 through 11–5 illustrate the timing characteristics of SFI-4 at the framer. Stratix devices support all the timing requirements needed to support transmitter and receiver functions of a SFI-4 framer; only framer-related timing specifications are applicable.

For details on the timing specifications of LVDS I/O standards in Stratix devices, refer to Section I, Stratix Device Family Data Sheet of the *Stratix Device Handbook, Volume 1* and Chapter 5, Using High-Speed Differential I/O Interfaces in Stratix Devices.

Figure 11–7 shows the timing diagram for Stratix framer transmitter ×1 (622 MHz clock) mode.

*Figure 11–7. Framer Transmitter ×1 (622 MHz Clock) Mode Timing Diagram*

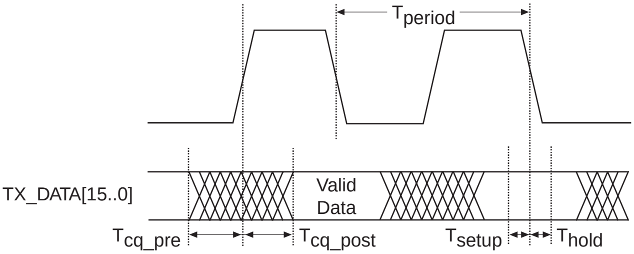


Table 11–3 lists the timing specifications for the SFI-4 framer transmitter in ×1 (622 MHz clock) mode.

*Table 11–3. SFI-4 Framer Transmitter ×1 (622 MHz Clock) Mode Timing Specifications*

| Parameter | Value | | | Unit |
|---|---|---|---|---|
| | Min | Typ | Max | |
| `TX_CLK` ($T_{period}$) | | 1,608 | | ps |
| Data invalid window before the rising edge ($T_{cq\_pre}$) | | | 200 | ps |
| Data invalid window after the rising edge ($T_{cq\_post}$) | | | 200 | ps |
| `TX_CLK` duty cycle | 40 | | 60 | % |
| Framer transmitter channel-to-channel skew | | | 400 | ps |

Figure 11–8 shows the timing diagram for the SFI-4 framer transmitter in ×2 (311 MHz clock) mode

*Figure 11–8. Framer Transmitter ×2 (311 MHz Clock) Mode Timing Diagram*

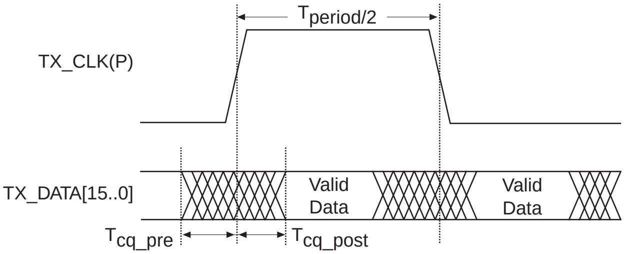


Table 11–4 lists the timing specifications for the SFI-4 framer transmitter in ×2 (311 MHz clock) mode.

*Table 11–4. SFI-4 Framer Transmitter ×2 (311 MHz Clock) Mode Timing Specifications*

| Parameter | Value | | | Unit |
|---|---|---|---|---|
| | Min | Typ | Max | |
| `TX_CLK` ($T_{period}$) | | 3,215 | | ps |
| Data invalid window before the rising edge ($T_{cq\_pre}$) | | | 200 | ps |
| Data invalid window after the rising edge ($T_{cq\_post}$) | | | 200 | ps |
| `TX_CLK` duty cycle | 48 | | 52 | % |
| Framer transmitter channel-to-channel skew | | | 400 | ps |

Figure 11–9 shows the timing diagram for the SFI-4 framer receiver.

*Figure 11–9. Framer Receiver Timing Diagram*

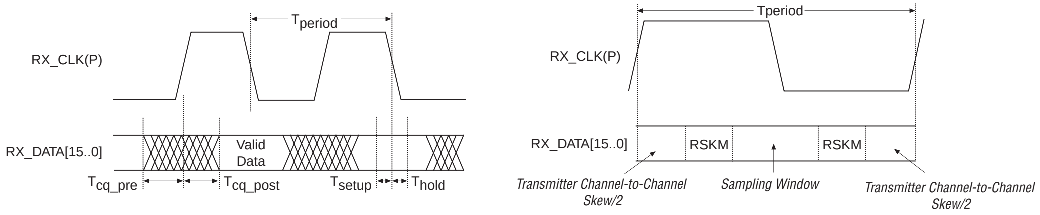


Table 11–5 lists the timing specifications for the SFI-4 framer receiver.

*Table 11–5. Framer Receiver Timing Specifications*

| Parameter | Value | | | Unit |
|---|---|---|---|---|
| | Min | Typ | Max | |
| `RX_CLK` ($T_{period}$) | | 1,608 | | ps |
| Data invalid window before the rising edge ($T_{cq\_pre}$) | | | 200 | ps |
| Data invalid window after the rising edge ($T_{cq\_post}$) | | | 200 | ps |
| `RX_CLK` duty cycle | 45 | | 55 | % |
| Data set-up time ($T_{setup}$) | 300 | | | ps |
| Data hold time ($T_{hold}$) | 300 | | | ps |
| Framer sampling window | 600 | | | ps |
| Receiver skew margin (RSKM) | | | 304 | ps |

## Electrical Specifications

SFI-4 uses LVDS as a high-speed data transfer mechanism to implement the SFI-4 interface. Table 11–6 lists the DC electrical characteristics for the interface, which are based on the IEEE Std. 1596.3-1996 7 specification. For more information on the voltage specification of LVDS I/O standards in Stratix devices, refer to Section I, Stratix Device Family Data Sheet of the *Stratix Device Handbook, Volume 1* and Chapter 5, Using High-Speed Differential I/O Interfaces in Stratix Devices.

*Table 11–6. Framer LDVS DC Specifications*

| Parameter | Value | | | Unit |
|---|---|---|---|---|
| | Min | Typ | Max | |
| Output differential voltage ($V_{OD}$) | 250 | | 600 *(1)* | mV |
| Output offset voltage ($V_{OS}$) | 1,125 | | 1,375 | mV |
| Output Impedance, single ended | 40 | | 140 | W |
| Change in $V_{OD}$ between ‘0’ and '1' | | | 50 | mV |
| Change in $V_{OD}$ between '1' and '0' | | | 50 | mV |
| Input voltage range ($V_I$) | 0 | | 2,400 | mV |
| Differential impedance | | 100 | | W |
| Input differential voltage ($V_{ID}$) | 100 | | 600 | mV |
| Receiver differential input impedance | 70 | | 130 | W |
| Ground potential difference (between PCS and PMA) | | | 50 | mV |
| Rise and fall times (20% to 80%) | 100 | | 400 | ps |

***Note to Table 11–6:***

(1) The IEEE standard requires 400 mV. A larger swing is encouraged, but not required.

## Software Implementation

The SFI-4 interface uses a 16-bit LVDS I/O interface. The Altera® Quartus® II software version 2.0 supports Stratix devices, allowing you to implement LVDS I/O buffers through the Quartus II Assignment Organizer.

For information on the Quartus II Assignment Organizer, refer to the Quartus II Help.

## Conclusion

SFI-4 is the standard interface between SONET framers and optical SERDES for OC-192 interfaces. With embedded SERDES and fast PLLs, Stratix devices can easily support the SFI-4 framer interface, enabling 10-Gbps (OC-192) data transfer rates. Stratix I/O supports the required data rates of up to 622.08 Mbps. Stratix fast PLLs are designed to support the high clock frequencies and one-to-one relationship needed for interfaces such as XSBI and SFI-4. Stratix devices can support multiple SFI-4 functions on one device.

# 12. Transitioning APEX Designs to Stratix Devices

S52012-1.0

Chapter 12, Transitioning APEX Designs to Stratix Devices replaces *AN 206: Transitioning APEX Designs to Stratix Devices*.

## Introduction

The Stratix™ device family is Altera's next-generation, system-on-a-programmable-chip (SOPC) solution. Stratix devices simplify the block-based design methodology and bridge the gap between system bandwidth requirements and programmable logic performance.

This application note highlights the new features in the Stratix device family and provides assistance when transitioning designs from APEX™ II or APEX 20K devices to the Stratix architecture. Designers using this application note should be familiar with the APEX II or APEX 20K architecture and available device features. Use this application note in conjunction with Section I, Stratix Device Family Data Sheet of the *Stratix Device Handbook, Volume 1*.

## General Architecture

The Stratix device family offers many new features and architectural enhancements. Enhanced logic elements (LEs) and the MultiTrack™ interconnect structure offer reduced resource utilization and considerable design performance improvement. The MultiTrack interconnect uses DirectDrive™ technology to ensure the availability of deterministic routing resources for any design block, regardless of its placement within the device.

All architectural changes between Stratix and APEX II or APEX 20K devices described in this section do not require any design changes. However, you must resynthesize your design and recompile in the Quartus® II software to target the Stratix device family.

## Logic Elements

Stratix device LEs include several new, advanced features that improve design performance and reduce logic resource consumption (see Table 12–1). The Quartus II software automatically uses these new LE features to improve device utilization.

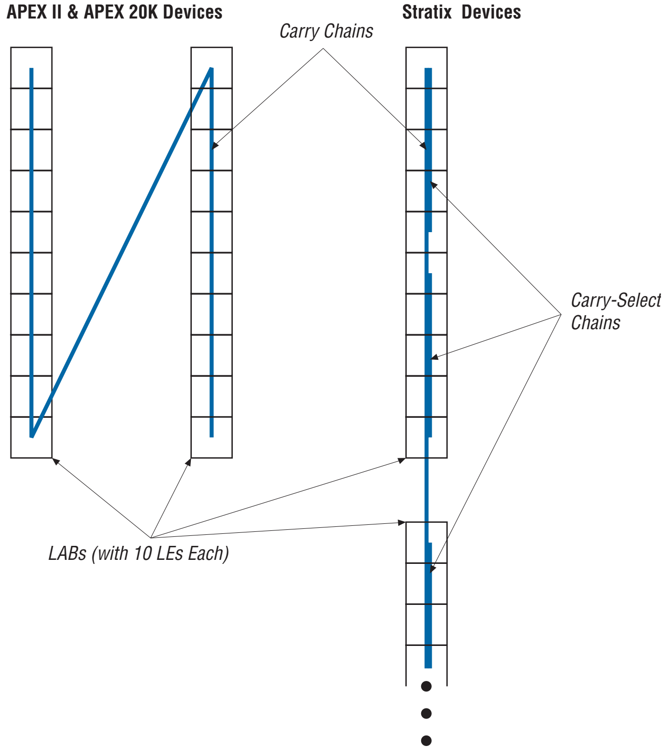
*Table 12–1. Stratix LE Features*

| Feature | Function | Benefit |
|---|---|---|
| Register chain interconnects | Direct path between the register output of an LE and the register input of an adjacent LE within the same logic array block (LAB) | ■ Conserves LE resources<br>■ Provides fast shift register implementation<br>■ Saves local interconnect routing resources within an LAB |
| Look-up table (LUT) chain interconnects | Direct path between the combinatorial output of an LE and the fast LUT input of an adjacent LE within the same LAB | ■ Allows LUTs within the same LAB to cascade together for high-speed wide fan-in functions, such as wide `XOR` operations<br>■ Bypasses local interconnect for faster performance |
| Register-to-LUT feedback path | Allows the register output to feed back into the LUT of the same LE, such that the register is packed with its own fan-out LUT | ■ Enhanced register packing mode<br>■ Uses resources more efficiently |
| Dynamic arithmetic mode | Uses one set of LEs for implementing both an adder and subtractor | ■ Improves performance for functions that switch between addition and subtraction frequently, such as correlators |
| Carry-select chain | Calculates outputs for a possible carry-in of 1 or 0 in parallel | ■ Gives immediate access to result for both a carry-in of 1 or 0<br>■ Increases speed of carry functions for high-speed operations, such as counters, adders, and comparators |
| Asynchronous clear and asynchronous preset function | Supports direct asynchronous clear and preset functions | ■ Conserves LE resources<br>■ Does not require additional logic resources to implement NOT-gate push-back |

In addition to the new LE features described in Table 12–1, there are enhancements to the chains that connect LEs together. Carry chains are implemented vertically in Stratix devices, instead of horizontally as in APEX II and APEX 20K devices, and continue across rows, instead of across columns, as shown in Figure 12–1. Also note that the Stratix architecture does not support the cascade primitive. Therefore, the Quartus II Compiler automatically converts cascade primitives in

APEX II and APEX 20K designs to a wire primitive when compiled for Stratix devices. These architectural changes are transparent to the user and do not require design changes.

*Figure 12–1. Carry Chain Implementation in APEX II & APEX 20K Devices vs. Stratix Devices*



## MultiTrack Interconnect

Stratix devices use the MultiTrack interconnect structure to provide a high-speed connection between logic resources using performance-optimized routing channels of different lengths. This feature maximizes overall design performance by placing critical paths on routing lines with greater speed, resulting in minimal propagation delay.

Stratix device MultiTrack interconnect resources are described in Table 12–2.

*Table 12–2. Stratix Device MultiTrack Interconnect Resources*

| Routing Type | Interconnect | Span |
|---|---|---|
| Row | Direct link | Adjacent LABs and/or blocks |
| Row | R4 | Four LAB units horizontally |
| Row | R8 | Eight LAB units horizontally |
| Row | R24 | Horizontal routing across the width of the device |
| Column | C4 | Four LAB units vertically |
| Column | C8 | Eight LAB units vertically |
| Column | C16 | Vertical routing across the length of the device |

Direct link routing saves row routing resources while providing fast communication paths between resource blocks. Direct link interconnects allow an LAB, digital signal processing (DSP) block, or TriMatrix™ memory block to drive data into the local interconnect of its left and right neighbors. LABs, DSP blocks, and TriMatrix memory blocks can also use direct link interconnects to drive data back into themselves for feedback.

The Quartus II software automatically uses these routing resources to enhance design performance.

For more information about LE architecture and the MultiTrack interconnect structure in Stratix devices, refer to Section I, Stratix Device Family Data Sheet of the *Stratix Device Handbook, Volume 1*.

## DirectDrive Technology

When using APEX II or APE 20K devices, you must place critical paths in the same MegaLAB™ column to improve performance. Additionally, you should place critical paths in the same MegaLAB structure for optimal performance. However, this restriction does not exist in Stratix devices because the devices do not contain MegaLAB structures. With the new DirectDrive™ technology in Stratix devices, the actual distance between the source and destination of a path is the most important criteria for meeting timing performance. DirectDrive technology ensures that the same routing resources are available to each design block, regardless of its location in the device.

## Architectural Element Names

The architectural element naming system within the Stratix device family differs from the row-column coordinate system (e.g., `LC1_A2`, `LAB_B1`) used in previous Altera device families. The Stratix device family uses a new naming system based on the X-Y coordinate system, (`X`, `Y`). A number (`N`) designates the location within the block where the logic resides, such as LEs within an LAB. Since the Stratix architecture is column-based, this naming simplifies location assignments. Stratix architectural blocks include:

- `LAB`: logic array block
- `DSP`: digital signal processing block
- `DSPOUT`: adder/subtractor/accumulator or summation block of the DSP block
- `M512`: 512-bit memory block
- `M4K`: 4-Kbit memory block
- `M-RAM`: 512-Kbit memory block

Elements within architectural blocks include:

- `LE`: logic element
- `IOC`: I/O element
- `PLL`: phase-locked loop
- `DSPMULT`: DSP block multiplier
- `SERDESTX`: transmitter serializer/deserializer
- `SERDESRX`: receiver serializer/deserializer

Table 12–3 highlights the new location syntax used for the Stratix device family.

*Table 12–3. Stratix Location Assignment Syntax*

| Architectural Elements | Element Name | Location Syntax | Example of Location Syntax | |
|---|---|---|---|---|
| | | | Location | Description |
| Blocks | `LAB`, `DSP`, `DSPOUT`, `M512`, `M4K`, `M-RAM` | *<element_name>*`_X`*<number>*`_Y`*<number>* | `LAB_X1_Y1` | Designates the LAB in row 1, column 1 |
| Logic | `LE`, `IOC`, `PLL`, `DSPMULT`, `SERDESTX`, `SERDESRX` | *<element_name>*`_X`*<number>*`_Y`*<number>*`_N`*<number>* | `LC_X1_Y1_N0` | Designates the first LE, N0, in the LAB located in row 1, column 1 |
| Pins *(1)* | I/O pins | `pin_`*<pin_label>* | `pin_5` | Pin 5 |

***Note to Table 12–3:***

(1) You can make assignments to I/O pads using `IOC_X`*<number>*`_Y`*<number>*`_N`*<number>*.

Use the following guidelines with the new naming system:

- The anchor point, or origin, in Stratix devices is in the bottom-left corner, instead of the top-left corner as in APEX II and APEX 20K devices.
- The anchor point, or origin, of a large block element (e.g., a M-RAM or DSP block) is also the bottom-left corner.
- All numbers are zero-based, meaning the origin at the bottom-left of the device is `X0`, `Y0`.
- The I/O pins constitute the first and last rows and columns in the X-Y coordinates. Therefore, the bottom row of pins resides in `X`<*number*>, `Y0`, and the first left column of pins resides in `X0`, `Y`<*number*>.
- The sub-location of elements, N, numbering begins at the top. Therefore, the LEs in an LAB are still numbered from top to bottom, but start at zero.

Figure 12–2 show the Stratix architectural element numbering convention. Figure 12–3 displays the floorplan view in the Quartus II software.

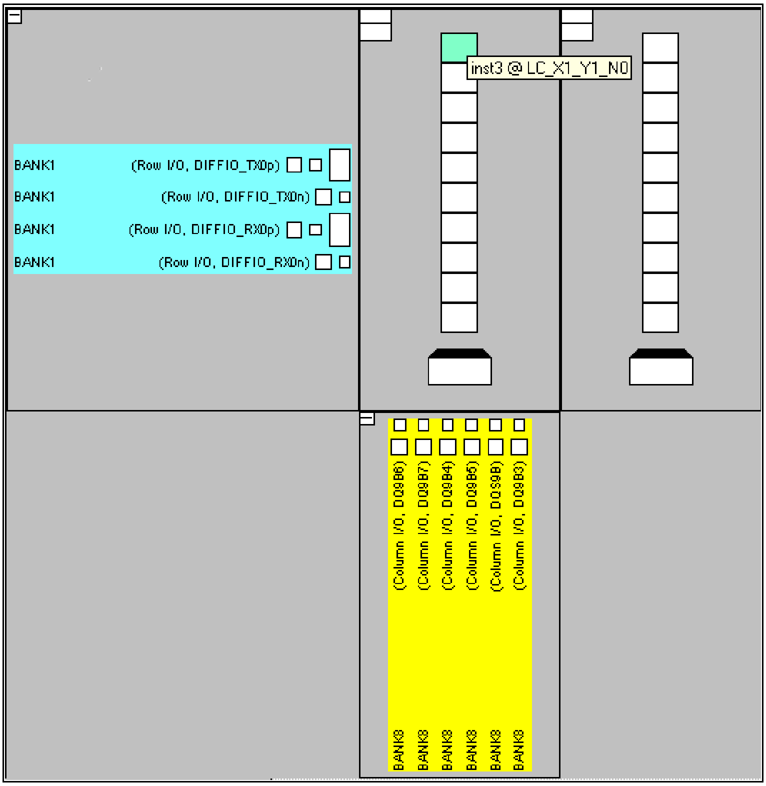
**Figure 12–2. Stratix Architectural Elements** Note (1)

*Notes to Figure 12–2:*

(1) Figure 12–2 shows part of a Stratix device.

(2) Large block elements use their lower-left corner for the coordinate location.

*Figure 12–3. LE Numbering as Shown in the Quartus II Software*



## TriMatrix Memory

TriMatrix memory has three different sizes of memory blocks, each optimized for a different purpose or application. M512 blocks consist of 512 bits plus parity (576 bits), M4K blocks consist of 4K bits plus parity (4,608 bits), and M-RAM blocks consist of 512K bits plus parity (589,824 bits). This new structure differs from APEX II and APEX 20K devices, which feature uniformly sized embedded system blocks (ESBs) either 4 Kbits (APEX II devices) or 2 Kbits (APEX 20K devices) large. Stratix TriMatrix memory blocks give you advanced control of each memory block, with features such as byte enables, parity bit storage, and shift-register mode, as well as mixed-port width support and true dual-port mode operation.

Table 12–4 compares TriMatrix memory with ESBs.

*Table 12–4. Stratix TriMatrix Memory Blocks vs. APEX II & APEX 20K ESBs*

| Features | Stratix | | | APEX II ESB | APEX 20K ESB |
|---|---|---|---|---|---|
| | M512 RAM | M4K RAM | M-RAM | | |
| Size (bits) | 576 | 4,608 | 589,824 | 4,096 | 2,048 |
| Parity bits | Yes | Yes | Yes | No | No |
| Byte enable | No | Yes | Yes | No | No |
| True dual-port mode | No | Yes<br>Includes support for mixed width | Yes<br>Includes support for mixed width | Yes<br>Includes support for mixed width | No |
| Embedded shift register | Yes | Yes | No | No | No |
| Dedicated content-addressable memory (CAM) support | No | No | No | Yes | Yes |
| Pre-loadable initialization with a **.mif** *(1)* | Yes | Yes | No | Yes | Yes |
| Packed mode *(2)* | No | Yes | No | Yes | Yes |
| Feed-through behavior | Rising edge | Rising edge | Rising edge | Falling edge | Falling edge |
| Output power-up condition | Powers up cleared even if using a **.mif** *(1)* | Powers up cleared even if using a **.mif** *(1)* | Powers up with unknown state | Powers up cleared or to initialized value, if using a **.mif** *(1)* | Powers up cleared or to initialized value, if using a **.mif** *(1)* |

*Notes to Table 12–4:*

(1) **.mif**: Memory Initialization File.

(2) Packed mode refers to combining two single-port RAM blocks into a single RAM block that is placed into true dual-port mode.

Stratix TriMatrix memory blocks only support synchronous mode, while APEX II and APEX 20K ESBs support both synchronous and asynchronous modes. Since all TriMatrix memory blocks are now fully synchronous, all input data and address lines must be registered, while outputs can be either registered or combinatorial. You can use Stratix memory block registers to implement input and output registers without utilizing additional resources. You can compile designs containing fully synchronous memory blocks (inputs registered) for Stratix devices without any modifications. However, if an APEX II or APEX 20K design contains asynchronous memory, you must modify the memory modules to target the Stratix architecture (see "Memory Megafunctions" on page 12–12 for more information).

For more information about TriMatrix Memory and converting asynchronous memory modules to synchronous, see Chapter 3, Using TriMatrix Embedded Memory Blocks in Stratix & Stratix GX Devices and *Application Note 210: Converting Memory from Asynchronous to Synchronous for Stratix Designs.*

## Same-Port Read-During-Write Mode

In same-port read-during-write mode, the RAM block can be in single-port, simple dual-port, or true dual-port mode. One port from the RAM block both reads and writes to the same address location using the same clock. When APEX II or APEX 20K devices perform a same-port read-during-write operation, the new data is available on the falling edge of the clock cycle on which it was written, as shown in Figure 12–4. When Stratix devices perform a same-port read-during-write operation, the new data is available on the rising edge of the same clock cycle on which it was written, as shown in Figure 12–5. This holds true for all TriMatrix memory blocks.

***Figure 12–4. Falling Edge Feed-Through Behavior (APEX II & APEX 20K Devices)*** *Note (1)*

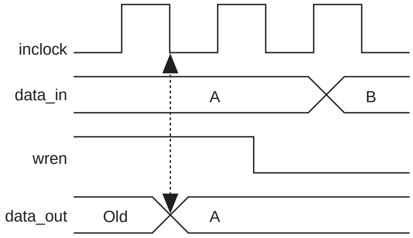
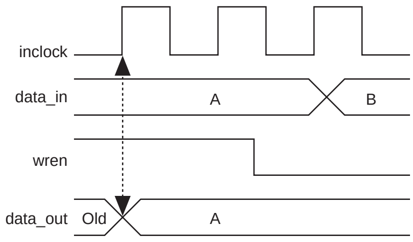


*Figure 12–5. Rising Edge Feed-Through Behavior (Stratix Devices)* *Note (1)*



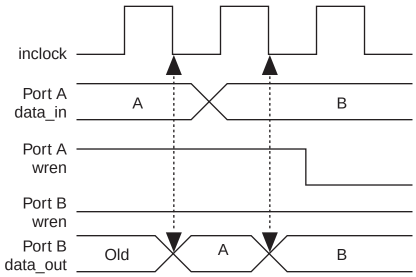
*Note to Figures 12–4 and 12–5:*

(1) Figures 12–4 and 12–5 assume that the address stays constant throughout and that the outputs are not registered.

## Mixed-Port Read-During-Write Mode

Mixed-port read-during-write mode occurs when a RAM block in simple or true dual-port mode has one port reading and the other port writing to the same address location using the same clock. In APEX II and APEX 20K designs, the ESB outputs the old data in the first half of the clock cycle and the new data in the second half of the clock cycle, as indicated by Figure 12–6.

*Figure 12–6. Mixed-Port Feed-Through Behavior (APEX II & APEX 20K Devices)* *Note (1)*



*Note to Figure 12–6:*

(1) Figure 12–6 assumes that outputs are not registered.

Stratix device RAM outputs the new data on the rising edge of the clock cycle immediately after the data was written. When you use Stratix M512 and M4K blocks, you can choose whether to output the old data at the targeted address or output a don't care value during the clock cycle when the new data is written. M-RAM blocks always output a don't care value.

Figures 12–7 and 12–8 show the feed-through behavior of the mixed-port mode. You can use the `altsyncram` megafunction to set the output behavior during mixed-port read-during-write mode.

*Figure 12–7. Mixed-Port Feed-Through Behavior (OLD_DATA)* Note (1)

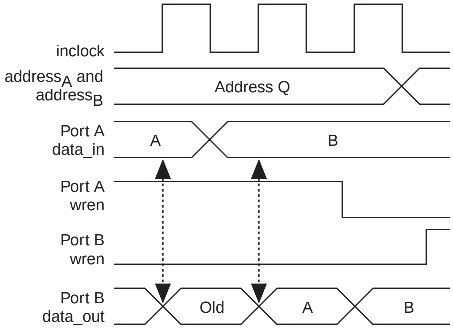
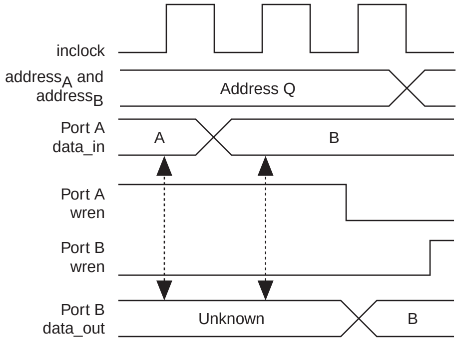


*Figure 12–8. Mixed-Port Feed-Through Behavior (DONT_CARE)* Note (1)



*Note to Figures 12–7 and 12–8:*

(1) Figures 12–7 and 12–8 assume that the address stays constant throughout and that the outputs are not registered.

## Memory Megafunctions

To convert RAM and ROM originally targeting the APEX II or APEX 20K architecture to Stratix memory, specify Stratix as the target device family in the MegaWizard Plug-In Manager. The software updates the memory module for the Stratix architecture and instantiates the new synchronous memory megafunction, `altsyncram`, which supports both RAM and ROM blocks in the Stratix architecture.

## FIFO Conditions

First-in first-out (FIFO) functionality is slightly different in Stratix devices compared to APEX II and APEX 20K devices. Stratix devices do not support simultaneous reads and writes from an empty FIFO buffer. Also, Stratix devices do not support the `lpm_showahead` parameter when targeting a FIFO buffer because the TriMatrix memory blocks are synchronous. The `lpm_showahead` parameter for APEX II and APEX 20K devices puts the FIFO buffer in "read-acknowledge" mode so the first data written into the FIFO buffer immediately flows through to the output. Other than these two differences, all APEX II and APEX 20K FIFO functions are fully compatible with the Stratix architecture.

## Design Migration Mode in Quartus II Software

The Quartus II software features a migration mode for simplifying the process of converting APEX II and APEX 20K memory functions to the Stratix architecture. If the design can use the Stratix `altsyncram` megafunction as a replacement for a previous APEX II or APEX 20K memory function while maintaining functionally similar behavior, the Quartus II software automatically converts the memory. The software produces a warning message during compilation reminding you to verify that the design migrated correctly.

For memory blocks with all inputs registered, the existing megafunction is converted to the new `altsyncram` megafunction. The software generates a warning when the `altsyncram` megafunction is incompatible. For example, a RAM block with all inputs registered except the read enable will compile with a warning message indicating that the read-enable port will be registered.

You can suppress warning messages for the entire project or for individual memory blocks by setting the `SUPPRESS_MEMORY_CONVERSION_WARNINGS` parameter to "on" as a global parameter by selecting **Assignment Organizer** (Tools menu). In the **Assignment Organizer** window, click **Parameters** in the **Assignment Categories** box. Type `SUPPRESS_MEMORY_CONVERSION_WARNINGS` in the **Assignment Name** box and type `ON` in the **Assignment Setting** box. To suppress these warning messages on a per-memory-instance basis, set the `SUPPRESS_MEMORY_CONVERSION_WARNINGS` parameter in the Assignment Organizer to "on" for the memory instance.

If the functionality of the APEX II or APEX 20K memory megafunction differs from the `altsyncram` functionality and at least one clock feeds the memory megafunction, the Quartus II software converts the APEX II or APEX 20K memory megafunction to the Stratix `altsyncram` megafunction. This conversion is useful for an initial evaluation of how a design might perform in Stratix devices and should only be used for evaluation purposes. During this process, the Quartus II software generates a warning that the conversion may be functionally incorrect and timing results may not be accurate. Since the functionality may be incorrect and the compilation is only intended for comparative purposes, the Quartus II software does not generate a programming file. A functionally correct conversion requires manually instantiating the `altsyncram` megafunction and may require additional design changes.

If the previous memory function does not have a clock (fully asynchronous), the fitting-evaluation conversion results in an error message during compilation and will not successfully convert the design. See *Application Note 210: Converting Memory from Asynchronous to Synchronous for Stratix Designs* for more information.

Table 12–5 summarizes the possible scenarios when using design migration mode and the resulting behavior of the Quartus II software.

The most common cases where design-migration mode may have difficulty converting the existing design are when:

- A port is reading from an address that is being written to by another port (mixed-port read-during-write mode). If both ports are using the same clock, the read port in Stratix devices will not see the new data until the next clock cycle, after the new data was written.
- There are differences in power-up behavior between APEX II, APEX 20K, and Stratix devices. You should manually account for these differences to maintain desired operation of the system.

**Table 12–5. Migration Mode Summary (Part 1 of 2)**

| Memory Configuration | Conditions | Possible Instantiated Megafunctions | Quartus II Warning Message(s) | Programming File Generated |
|---|---|---|---|---|
| Single-port | All inputs are registered. | `altram`<br>`altrom`<br>`lpm_ram_dq`<br>`lpm_ram_io`<br>`lpm_rom` | Power-up differences. *(1)* | Yes |
| Multi-port (two-, three-, or four-port functions) | All inputs are registered. | `altdpram`<br>`lpm_ram_dp`<br>`altqpram`<br>`alt3pram` | Power-up differences. Mixed-port read- during-write. *(1)* | Yes |

*Table 12–5. Migration Mode Summary (Part 2 of 2)*

| Memory Configuration | Conditions | Possible Instantiated Megafunctions | Quartus II Warning Message(s) | Programming File Generated |
|---|---|---|---|---|
| Dual-port | Read-enable ports are unregistered.<br>Other inputs registered. | `altdpram`<br>`lpm_ram_dp`<br>`altqpram`<br>`alt3pram` | Power-up differences.<br>Mixed-port read- during-write.<br>Read enable will be registered. *(1)* | Yes |
| Dual-port | Any other unregistered port except read-enable ports.<br>Clock available. | `altdpram`<br>`lpm_ram_dp`<br>`altqpram`<br>`alt3pram` | Compile for fitting- evaluation purposes. | No |
| Single-port | At least one registered input.<br>Clock available. | `altram`<br>`lpm_ram_dq`<br>`lpm_ram_io` | Compile for fitting- evaluation purposes. | No |
| No clock | No clock. | `altram`<br>`altrom`<br>`altdpram`<br>`altqpram`<br>`alt3pram`<br>`altdpram`<br>`lpm_ram_dq`<br>`lpm_ram_io`<br>`lpm_rom`<br>`lpm_ram_dp`<br>`lpm_ram_dp` | Error – no conversion possible. | No |

*Note to Table 12–5:*

(1) If the `SUPPRESS_MEMORY_COUNVERSION_WARNINGS` parameter is turned on, the Quartus II software will not issue these warnings.

## DSP Block

Stratix device DSP blocks outperform LE-based implementations for common DSP functions. Each DSP block contains several multipliers that can be configured for widths of 9, 18, or 36 bits. Depending on the mode of operation, these multipliers can optionally feed an adder/subtractor/accumulator or summation unit.

You can configure the DSP block's input registers to efficiently implement shift registers for serial input sharing, eliminating the need for external shift registers in LEs. You can add pipeline registers to the DSP block for accelerated operation. Registers are available at the input and output of the multiplier, and at the output of the adder/subtractor/accumulator or summation block.

DSP blocks have four modes of operation:

- Simple multiplier mode
- Multiply-accumulator mode
- Two-multipliers adder mode
- Four-multipliers adder mode

Associated megafunctions are available in the Quartus II software to implement each mode of the DSP block.

## DSP Block Megafunctions

You can use the `lpm_mult` megafunction to configure the DSP block for simple multiplier mode. You can set the `lpm_mult` **Multiplier Implementation** option in the MegaWizard Plug-In Manager to either use the default implementation, ESBs, or the DSP blocks. If you select the **Use Default** option, the compiler will first attempt to place the multiplier in the DSP blocks. However, under certain conditions, the compiler may implement the multiplier in LEs. The placement depends on factors such as DSP block resource consumption, the width of the multiplier, whether an operand is a constant, and other options chosen for the megafunction.

Stratix devices do not support the **Use ESBs** option. If you select this option, the Quartus II software will try to place the multiplier in unused DSP blocks.

You can recompile APEX II or APEX 20K designs using the `lpm_mult` megafunction for Stratix devices in the Quartus II software without changing the megafunction. This makes converting `lpm_mult` megafunction designs to Stratix devices straightforward.

APEX II and APEX 20K designs use pipeline stages to improve registered performance of LE-based multipliers at the expense of latency. However, you may not need to use pipeline stages when targeting Stratix high-speed DSP blocks. The DSP blocks offer three sets of dedicated pipeline registers. Therefore, Altera recommends that you reduce the number of pipeline stages to three or fewer and implement them in the DSP blocks. Additional pipeline stages are implemented in LEs, which add latency without providing any performance benefit.

For example, you can configure a DSP block for 36 × 36-bit multiplication using the `lpm_mult` megafunction. If you specify two pipeline stages, the software will use the DSP block input and pipeline registers. If you specify three pipeline stages, the software will place the third pipeline stage in the DSP block output registers. This design will yield the same performance with three pipeline stages because the critical path for a 36 × 36-bit operation is within the multiplier. With four or more pipeline stages, the device will inefficiently use LE resources for the additional pipeline stages. Therefore, if multiplier modules in APEX II or APEX 20K designs are converted to Stratix designs and do not require the same number of pipeline stages, the surrounding circuitry must be modified to preserve the original functionality of the design.

A design with multipliers feeding an accumulator can use the `altmult_accum (MAC)` megafunction to set the DSP block in multiply-accumulator mode. If the APEX II or APEX 20K design already uses LE-based multipliers feeding an accumulator, the Quartus II software will not automatically instantiate the new `altmult_accum (MAC)` megafunction. Therefore, you should use the MegaWizard Plug-In Manager to instantiate the `altmult_accum (MAC)` megafunction. You can also use LeonardoSpectrum or Synplify synthesis tools, which have DSP block inference support, to instantiate the megafunction.

Designs that use multipliers feeding into adders can instantiate the new `altmult_add` megafunction to configure the DSP blocks for two-multipliers adder or four-multipliers adder mode. You can also use the `altmult_add` megafunction for stand-alone multipliers to take advantage of the DSP blocks features such as dynamic sign control of the inputs and the input shift register connections. These features are not accessible through the `lpm_mult` megafunction. If your APEX II or APEX 20K designs already use multipliers feeding an adder/subtractor, the Quartus II software will not automatically infer the new `altmult_add` megafunction. Therefore, you should step through the MegaWizard Plug-In Manager to instantiate the new `altmult_add` megafunction or use LeonardoSpectrum or Synplify synthesis tools, which have DSP block inference support.

Furthermore, the `altmult_add` and `altmult_accum (MAC)` megafunctions are only available for Stratix devices because these megafunctions target Stratix DSP blocks, which are not available in other device families. If you attempt to use these megafunctions in designs that target other Altera device families, the Quartus II software will report an error message. Use `lpm_mult` and an `lpm_add_sub` or an `altaccumulate` megafunction for similar functionality in other device families.

If you use a third-party synthesis tool, you may be able to avoid the megafunction conversion process. LeonardoSpectrum and Synplify provide inference support for `lpm_mult`, `altmult_add`, and `altmult_accum (MAC)` to use the DSP blocks.

If your design does not require you to implement all the multipliers in DSP blocks, you must manually set a global parameter or a parameter for each instance to force the tool to implement the `lpm_mult` megafunction in LEs. Depending on the synthesis tools, inference of DSP blocks will be handled differently.

For more information about using DSP blocks in Stratix devices, see Chapter 6, Using the DSP Blocks in Stratix & Stratix GX Devices.

## PLLs & Clock Networks

Stratix devices provide exceptional clock management with a hierarchical clock network and up to four enhanced phase-locked loops (PLLs) and eight fast PLLs versus the four general-purpose PLLs and four True-LVDS™ PLLs in APEX II devices. By providing superior clock interfacing, numerous advanced clocking features, and significant enhancements over APEX II and APEX 20K PLLs, the Stratix PLLs increase system performance and bandwidth.

### Clock Networks

There are 16 global clock networks available throughout each Stratix device as well as two fast regional and four regional clock networks per device quadrant, resulting in up to 40 unique clock networks per device. The increased number of dedicated clock resources available in Stratix devices eliminate the need to use general-purpose I/O pins as clock inputs.

Stratix EP1S25 and smaller devices have 16 dedicated clock pins and EP1S30 and larger devices have four additional clock pins to feed various clocking networks. In comparison, APEX II devices have eight dedicated clock pins and APEX 20KE and APEX 20KC devices have four dedicated clock pins.

The dedicated clock pins in Stratix devices can feed the PLL clock inputs, the global clock networks, and the regional clock networks. PLL outputs and internally-generated signals can also drive the global clock network. These global clocks are available throughout the entire device to clock all device resources.

Stratix devices are divided into four quadrants, each equipped with four regional clock networks. The regional clock network can be fed by either the dedicated clock pins or the PLL outputs within its device quadrant. The regional clock network can only feed device resources within its particular device quadrant.

Each Stratix device provides eight dedicated fast clock I/O pins `FCLK[7..0]` versus four dedicated fast I/O pins in APEX II and APEX 20K devices. The fast regional clock network can be fed by these dedicated `FCLK[7..0]` pins or by the I/O interconnect. The I/O interconnect allows internal logic or any I/O pin to drive the fast regional clock network. The fast regional clock network is available for general-purpose clocking as well as high fan-out control signals such as clear, preset, enable, `TRDY` and `IRDY` for PCI applications, or bidirectional or output pins.

EP1S25 and smaller devices have eight fast regional clock networks, two per device quadrant. The quadrants in EP1S30 and larger devices are divided in half, and each half-quadrant can be clocked by one of the eight fast regional networks. Additionally, each fast regional clock network can drive its neighboring half-quadrant (within the same device quadrant).

## PLLs

Table 12–6 highlights Stratix PLL enhancements to existing APEX II, APEX 20KE and APEX 20KC PLL features.

***Table 12–6. Stratix PLL vs. APEX II, APEX 20KE & APEX 20KC PLL Features (Part 1 of 2)***

| Feature | Stratix | | APEX II PLLs | APEX 20KE & APEX 20KC PLLs |
|---|---|---|---|---|
| | Enhanced PLLs | Fast PLLs | | |
| Number of PLLs | Two (EP1S30 and smaller devices); four (EP1S40 and larger devices) | Four (EP1S25 and smaller devices); eight (EP1S30 and larger devices) | Four general-purpose PLLs and four LVDS PLLs | Up to four general-purpose PLLs. Up to two LVDS PLLs. *(1)* |
| Minimum input frequency | 3 MHz | 15 MHz | 1.5 MHz | 1.5 MHz |
| Maximum input frequency | 250 to 582 MHz *(2)* | 644.5 MHz | 420 MHz | 420 MHz |
| Internal clock outputs per PLL | 6 | 3 *(3)* | 2 | 2 |
| External clock outputs per PLL | Four differential/eight singled-ended or one single-ended *(4)* | Yes *(5)* | 1 | 1 |
| Phase Shift | Down to 160-ps increments *(6)* | Down to 150-ps increments *(6)* | 500-ps to 1-ns resolution | 0.4- to 1-ns resolution |
| Time shift | 250-ps increments for ± 3 ns *(7)* | No | No | No |
| *M* counter values | 1 to 512 | 1 to 32 | 1 to 160 | 2 to 160 |

*Table 12–6. Stratix PLL vs. APEX II, APEX 20KE & APEX 20KC PLL Features (Part 2 of 2)*

| Feature | Stratix | | APEX II PLLs | APEX 20KE & APEX 20KC PLLs |
|---|---|---|---|---|
| | Enhanced PLLs | Fast PLLs | | |
| *N* counter values | 1 to 512 | N/A | 1 to 16 | 1 to 16 |
| PLL clock input sharing | No | Yes | Yes | Yes |
| T1/E1 rate conversion *(8)* | No | No | Yes | Yes |

***Notes to Table 12–6:***

(1) EP20K200E and smaller devices only have two general-purpose PLLs. EP20K400E and larger devices have two LVDS PLLs and four general-purpose PLLs. For more information, see *Application Note 115: Using the ClockLock & ClockBoost PLL Features in APEX Devices*.

(2) The maximum input frequency for Stratix enhanced PLLs depends on the I/O standard used with that input clock pin. For more information, see Section I, Stratix Device Family Data Sheet of the *Stratix Device Handbook, Volume 1*.

(3) Fast PLLs 1, 2, 3, and 4 have three internal clock output ports per PLL. Fast PLLs 7, 8, 9, and 10 have two internal clock output ports per PLL.

(4) Every Stratix device has two enhanced PLLs with eight single-ended or four differential outputs each. Two additional enhanced PLLs in EP1S80, EP1S60, and EP1S40 devices each have one single-ended output.

(5) Any I/O pin can be driven by the fast PLL global or regional outputs as an external clock output pin.

(6) The smallest phase shift unit is determined by the voltage-controlled oscillator (VCO) period divided by 8.

(7) There is a maximum of 3 ns between any two PLL clock outputs.

(8) The T1 clock frequency is 1.544 MHz and the E1 clock frequency is 2.048 MHz, which violates the minimum clock input frequency requirement of the Stratix PLL.

## Enhanced PLLs

Stratix devices provide up to four enhanced PLLs with advanced PLL features. In addition to the feature changes mentioned in Table 12–6, Stratix device PLLs include many new, advanced features to improve system timing management and performance. Table 12–7 shows some of the new features available in Stratix enhanced PLLs.

*Table 12–7. Stratix Enhanced PLL Features (Part 1 of 2)*

| Feature | Description |
|---|---|
| Programmable duty cycle *(1)* | Allows variable duty cycle for each PLL clock output. |
| PLL clock outputs can feed logic array *(1)* | Allows the PLL clock outputs to feed data ports of registers or combinatorial logic. |
| PLL locked output can feed the logic array *(1)* | Allows the PLL locked port to feed data ports of registers or combinatorial logic. |
| Multiplication allowed in zero-delay buffer mode or external feedback mode | The PLL clock outputs can be a multiplied or divided down ratio of the PLL input clock. |

*Table 12–7. Stratix Enhanced PLL Features (Part 2 of 2)*

| Feature | Description |
|---|---|
| Programmable phase shift allowed in zero-delay buffer mode or external feedback mode *(2)* | The PLL clock outputs can be phase shifted. The phase shift is relative to the PLL clock output. |
| Phase frequency detector (PFD) disable | Allows the VCO to operate at its last set control voltage and frequency with some long term drift. |
| Clock output disable *(3)* | PLL maintains lock with output clocks disabled. *(4)* |
| Programmable lock detect & gated lock | Holds the lock signal low for a programmable number of input clock cycles. |
| Dynamic clock switchover | Enables the PLL to switch between two reference input clocks, either for clock redundancy or dual-clock domain applications. |
| PLL reconfiguration | Allows the counters and delay elements within the PLL to be reconfigured in real-time without reloading a programmer object file (**.pof**). |
| Programmable bandwidth | Provides advanced control of the PLL bandwidth by using the programmable control of the PLL loop characteristics. |
| Spread spectrum | Modulates the target frequency over a frequency range to reduce electromagnetic interference (EMI) emissions. |

*Notes to Table 12–7:*

(1) These features are also available in fast PLLs.

(2) In addition to the delay chains at each counter, you can specify the programmable phase shift for each PLL output at fine and coarse levels.

(3) Each PLL clock output has an associated clock enable signal.

(4) If the PLL is used in external feedback mode, the PLL will need to relock.

### Fast PLLs

Stratix fast PLLs are similar to the APEX II True-LVDS PLLs in that the *W* setting, which governs the relationship between the clock input and the data rate, and the *J* setting, which controls the width of the high-speed differential I/O data bus, do not have to be equal. Additionally, Stratix fast PLLs offer up to three clock outputs, two multiplied high-speed PLL clocks to drive the serializer/deserializer (SERDES) block and/or an external pin, and a low-speed clock to drive the logic array. You can use fast PLLs for both high-speed interfacing and for general-purpose PLL applications.

Table 12–8 shows the differences between Stratix fast PLLs and APEX II and APEX 20K True-LVDS PLLs.

**Table 12–8. Stratix Fast PLL vs. APEX II & APEX 20K True-LVDS PLL**

| Feature | Stratix | APEX II | APEX 20KE<br>APEX 20KC |
|---|---|---|---|
| Number of fast PLLs or True-LVDS PLLs *(1)* | Four (EP1S25 and smaller devices) fast PLLs<br>Eight (EP1S30 and larger devices) fast PLLs | Four True-LVDS PLLs | Two True-LVDS PLLs *(2)* |
| Number of channels per transmitter/receiver block | 20 | 18 | 18 |
| VCO frequency | 300 to 840 MHz | 200 MHz to 1GHz | 200 to 840 MHz |
| Minimum input frequency<br>$M = 4, 5, 6$ | 300 – $M$ MHz | 50 MHz | 50 MHz<br>$M = 4$ *(3)* |
| Minimum input frequency<br>$M = 7, 8, 9, 10$ | 300 – $M$ MHz | 30 MHz | 30 MHz<br>$M = 7, 8$ *(3)* |

***Notes to Table 12–8:***

(1) You can also use Stratix device fast PLLs for general-purpose PLL applications.

(2) EP20K400E and larger devices have two True-LVDS PLLs.

(3) In APEX 20KE and APEX 20KC devices, $M = 4, 7$, or 8.

The Stratix fast PLL VCO frequency range is 300 to 840 MHz, and the APEX II True-LVDS PLL VCO frequency range is 200 MHz to 1 GHz. Therefore, you must update designs that use a data rate of less than 300 megabits per second (Mbps) to use the enhanced PLLs and M512 RAM blocks in SERDES bypass mode. Additionally, you must update designs that use a data rate faster than 840 Mbps.

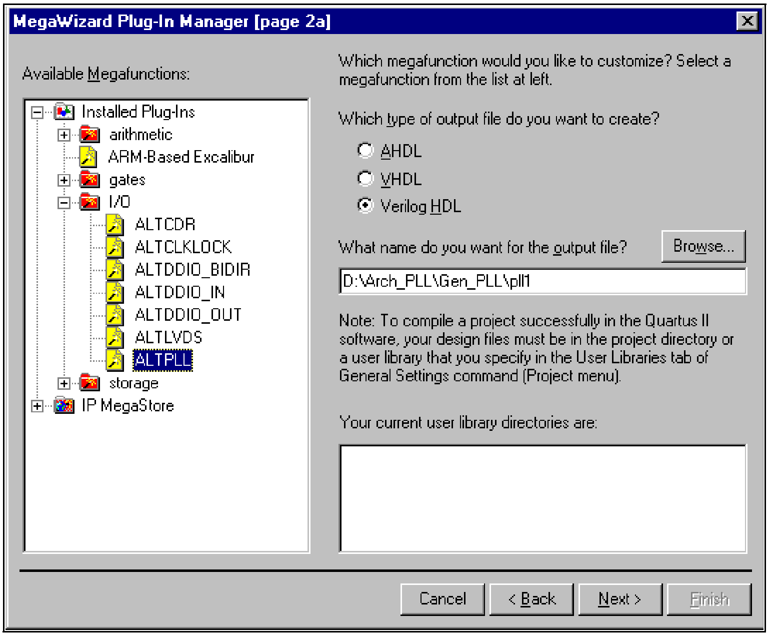
### *altpll Megafunction*

Altera recommends that you replace instances of the `altclklock` megafunction with the `altpll` megafunction to take advantage of new Stratix PLL features. Although in most cases you can retarget your APEX II or APEX 20K design to a Stratix device with the `altclklock` megafunction, there are specific cases where you must use the `altpll` megafunction, as explained in this section.

In the MegaWizard Plug-In Manager, select the `altpll` megafunction in the I/O directory from the **Available Megafunctions** box (see Figure 12–9). The `altclklock` megafunction is also available from the Quartus II software for backward compatibility, but will instantiate the new `altpll` megafunction when targeting Stratix devices. The

Quartus II Compiler automatically selects whether the `altpll` module uses either an enhanced PLL or a fast PLL based on the design's PLL needs and the feature requirements of each PLL.

*Figure 12–9. altpll Megafunction Selection in the MegaWizard Plug-In Manager*



Which megafunction would you like to customize? Select a megafunction from the list at left.

Which type of output file do you want to create?

○ AHDL
○ VHDL
● Verilog HDL

What name do you want for the output file?

D:\Arch_PLL\Gen_PLL\pll1

Note: To compile a project successfully in the Quartus II software, your design files must be in the project directory or a user library that you specify in the User Libraries tab of General Settings command (Project menu).

Your current user library directories are:

You can compile APEX II, APEX 20KE, and APEX 20KC designs using the `altclklock` megafunction in normal mode for Stratix devices without updating the megafunction. However, you should replace the `altclklock` megafunction with the `altpll` megafunction. If the Quartus II software cannot implement the requested clock multiplication and division of the PLL, the compiler will report an error message with the appropriate reason stated.

APEX II, APEX 20KE, and APEX 20KC devices have only one external clock output available per PLL. Therefore, when retargeting an APEX II, APEX 20KE, or APEX 20KC design that uses PLLs in zero delay buffer mode or external feedback mode to a Stratix device, you should replace instances of the `altclklock` megafunction. If an APEX II, APEX 20KE, or APEX 20KC `altclklock` module only uses one PLL clock output (internal or external) and is compiled to target a Stratix device, the design will compile successfully with a warning that the design uses the Stratix PLL external clock output, `extclk0`. However, if the APEX II, APEX 20KE, or APEX 20KC PLL has more than one PLL clock output, you must replace instances of the `altclklock` megafunction with the `altpll` megafunction because the Quartus II Compiler will not know which PLL clock output is fed to an external output pin or fed back to the Stratix device `fbin` pin. For example, if an APEX II, APEX 20KE, or APEX 20KC design with an `altclklock` megafuntion uses the `clock0` output port to feed the external clock output pin and the `clock1` output port to feed the internal logic array, the Quartus II software will generate an error during compilation and you must use the MegaWizard Plug-In Manager to instantiate the `altpll` megafunction. By using the `altpll` megafunction, you can choose which of the four external clock outputs to use and take advantage of the new Stratix PLL features now available in the zero delay buffer mode or external feedback mode.

### *Timing Analysis*

When the Quartus II software performs a timing analysis for APEX II, APEX 20KE, or APEX 20KC designs, PLL clock settings override the project clock settings. However, during timing analysis for Stratix designs using PLLs, the project clock settings override the PLL input clock frequency and duty cycle settings. The MegaWizard Plug-In Manager does not use the project clock settings to determine the `altpll` parameters. This will save time with designs that use features such as clock switchover or PLL reconfiguration because the Quartus II software can perform a timing analysis without recompiling the design. It is important to note the following:

- A warning during compilation will report that the project clock settings overrides the PLL clock settings.
- The project clock setting overrides the PLL clock settings for timing-driven compilation.
- The compiler will check the lock frequency range of the PLL. If the frequency specified in the project clock settings is outside the lock frequency range, the PLL clock settings will not be overridden.
- Performing a timing analysis without recompiling your design will not change the programming files. You must recompile your design to update the programming files.
- A **Default Required $\mathbf{f_{MAX}}$** setting will not override the PLL clock settings. Only individual clock settings will override the PLL clock settings.

Therefore, you can enter different project clock settings corresponding to new PLL settings and accelerate timing analysis by eliminating a full compilation cycle.

For more information about using Stratix PLLs, refer to Chapter 1, Using General-Purpose PLLs in Stratix & Stratix GX Devices.

# I/O Structure

The Stratix I/O element (IOE) architecture is similar to the APEX II architecture, with a total of six registers and a latch in each IOE. The registers are organized in three sets: two output registers to drive a single or double-data rate (DDR) output path, two input registers and a latch to support a single or DDR input path, and two output enable registers to enhance clock-to-output enable timing or for DDR SDRAM interfacing. A new synchronous reset signal is available to each of the three sets of registers for preset or clear, or neither. In addition to the advanced IOE architecture, the Stratix IOE features dedicated circuitry for external RAM interfacing, new I/O standards, on-chip termination (Terminator™ technology), and high-speed differential I/O standard support.

## External RAM Interfacing

The advanced Stratix IOE architecture includes dedicated circuitry to interface with external RAM. This circuitry provides enhanced support for external high-speed memory devices such as DDR SDRAM and FCRAM. The DDR SDRAM interface uses a bidirectional signal, `DQS`, to clock data, `DQ`, at both the transmitting and receiving device. Stratix devices transmit the `DQS` signal with the `DQ` data signals to minimize clock to data skew.

The Stratix device includes groups of programmable `DQS` and `DQ` pins, in the top and bottom I/O banks of the device. Each group consists of a `DQS` pin that supports a fixed number of `DQ` pins. The number of `DQ` pins depends on the `DQ` bus mode. When using the external RAM interfacing circuitry, the `DQS` pin drives a dedicated clock network that feeds the `DQ` pins residing in that bank. The Stratix IOE has programmable delay chains that can phase shift the `DQS` signal by 90° or 72° to ensure data is sampled at the appropriate point in time. Therefore, the Stratix device makes full use of the IOEs, and removes the need to build the input data path in the logic array. You can make these I/O assignments in the Quartus II assignment organizer.

For more information on external RAM interfacing, refer to Section I, Stratix Device Family Data Sheet of the *Stratix Device Handbook, Volume 1*.

## I/O Standard Support

The Stratix device family supports all of the I/O standards that APEX II and APEX 20K devices support, including high-speed differential I/O standards such as LVDS, LVPECL, PCML, and HyperTransport™ technology, differential HSTL on input and output clocks, and differential SSTL on output clocks. Stratix devices also introduce support for SSTL-18 class I & II. Similar to APEX II devices, Stratix devices only support certain I/O standards in designated I/O banks. In addition, `vref` pins are dedicated pins in Stratix devices and now support up to 40 input pins.

For more information about I/O standard support in Stratix devices, refer to Chapter 4, Using Selectable I/O Standards in Stratix & Stratix GX Devices.

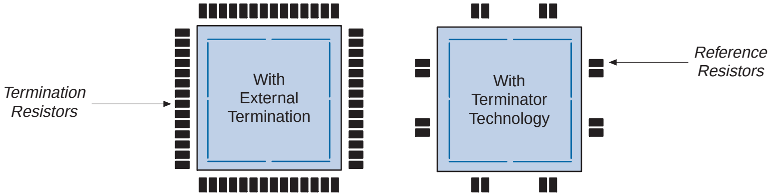
## Terminator Technology

Stratix devices provide source series termination ($R_S$), parallel load termination ($R_T$) for single-ended I/O standards, and differential termination at the LVDS receiver ($R_D$). Stratix devices feature 25-Ω on-chip series termination for SSTL-3 class I and II and SSTL-2 class I and II. You can use this series termination resistor for output driver impedance matching. The impedance of the output driver is matched with the transmission line impedance, allowing you to set the series termination of the output driver to 25 or 50 Ω for use with LVTTL or LVCMOS at 1.8, 2.5, and 3.3 V. Stratix devices support 50-Ω parallel termination for SSTL-2, SSTL-3, HSTL class I & II, GTL/GTL+, and CTT buffers. Differential I/O standards such as LVDS require an on-board 100-Ω termination resistor at the receiver.

Stratix device Terminator technology offers on-chip LVDS termination resistors, eliminating the need for external termination resistors. Use the Quartus II software to set on-chip termination.

Terminator technology features termination resistors that are located inside the device package, which eliminates the need for on-board termination resistors, simplifying board design. APEX II and APEX 20K devices do not support on-chip termination and require external termination resistors. You can use Stratix device Terminator technology to simplify printed circuit board (PCB) routing and footprint layout, prevent reflections, and maintain signal integrity. Figure 12–10 compares a footprint layout of a device needing external termination resistors with a Stratix footprint using the Terminator technology.

*Figure 12–10. Device Footprint Comparison with & without Terminator Technology*



For more information about using the Terminator technology, see Chapter 4, Using Selectable I/O Standards in Stratix & Stratix GX Devices.

## High-Speed Differential I/O Standards

Stratix devices support high-speed differential interfaces at speeds up to 840 Mbps using high-speed PLLs that drive a dedicated clock network to the SERDES. Each fast PLL can drive up to 20 high-speed channels. Stratix devices use enhanced PLLs and M512 RAM blocks to provide up to 462-Mbps performance for SERDES bypass clock interfacing. There is no restriction on the number of channels that can be clocked using this scenario.

Stratix devices have a different number of differential channels than APEX II devices. Table 12–9 highlights the number of differential channels supported in Stratix devices.

*Table 12–9. Number of Dedicated DIfferential Channels in Stratix Devices (Part 1 of 2) Note (1)*

| Device | Pin Count | Number of Receiver Channels | Number of Transmitter Channels |
|---|---|---|---|
| EP1S10 | 672 | 36 | 36 |
| | 780 | 44 | 44 |
| EP1S20 | 672 | 50 | 48 |
| | 780 | 66 | 66 |
| EP1S25 | 672 | 58 | 56 |
| | 780 | 66 | 70 |
| | 1,020 | 78 | 78 |

*Table 12–9. Number of Dedicated DIfferential Channels in Stratix Devices (Part 2 of 2) Note (1)*

| Device | Pin Count | Number of Receiver Channels | Number of Transmitter Channels |
|---|---|---|---|
| EP1S30 | 780 | 66 | 70 |
| | 956 | 80 | 80 |
| | 1,020 | 80 | 80 |
| | | 2 | 2 |
| EP1S40 | 956 | 80 | 80 |
| | 1,020 | 80 | 80 |
| | | 10 | 10 |
| | 1,508 | 80 | 80 |
| | | 10 | 10 |
| EP1S60 | 956 | 80 | 80 |
| | 1,020 | 80 | 80 |
| | | 10 | 12 |
| | 1,508 | 80 | 80 |
| | | 36 | 36 |
| EP1S80 | 956 | 80 | 40 |
| | | 0 | 40 |
| | 1,508 | 80 | 40 |
| | | 56 | 112 |

***Note to Table 12–9:***

(1) For information on channel speeds, see Section I, Stratix Device Family Data Sheet of the *Stratix Device Handbook, Volume 1* and Chapter 5, Using High-Speed Differential I/O Interfaces in Stratix Devices.

If you compile an APEX II LVDS design that uses clock-data synchronization (CDS) for a Stratix device, the Quartus II software will issue a warning during compilation that Stratix devices do not support CDS.

Stratix devices offer a flexible solution using new byte realignment circuitry to correct for byte misalignment by shifting, or slipping, data bits. Stratix devices activate the byte realignment circuitry when an external pin (`rx_data_align`) or an internal custom-made state machine asserts the `SYNC` node high.

APEX II, APEX 20KE, and APEX 20KCdevices have a dedicated transmitter clock output pin (`LVDSTXOUTCLK`). In Stratix devices, a transmitter `dataout` channel with an LVDS clock (fast clock) generates the transmitter clock output. Therefore, you can drive any channel as an output clock to an I/O pin, not just dedicated clock output pins. This solution offers better versatility to address various applications that require more complex clocking schemes.

For more information on differential I/O support, data realignment, and the transmitter clock output in Stratix devices, refer to the Chapter 5, Using High-Speed Differential I/O Interfaces in Stratix Devices.

### altlvds Megafunction

To take full advantage of the high-speed differential I/O standards available in Stratix devices, you should update each instance of the `altlvds` megafunction in APEX II, APEX 20KE, and APEX 20KC designs. In the MegaWizard Plug-In Manager, choose the `altlvds` megafunction, select Stratix as the target device family, update the megafunction, and recompile your design.

The `altlvds` megafunction supports new Stratix parameters that are not available for APEX II, APEX 20KE, and APEX 20KC devices. Tables 12–10 and 12–11 describe the new parameters for the LVDS receiver and LVDS transmitter, respectively.

*Table 12–10. New altlvds Parameters for Stratix LVDS Receiver* *Note (1)*

| Parameter | Function |
|---|---|
| `input_data_rate` *(2)* | Specifies the data rate in Mbps. This parameter replaces the multiplication factor *W*. |
| `inclock_data_alignment` | Indicates the alignment of `rx_inclk` and `rx_in` data. |
| `rx_data_align` | Drives the data alignment port of the fast PLL and enables byte realignment circuitry. |
| `registered_data_align_input` | Registers the `rx_data_align` input port to be clocked by `rx_outclock`. |
| `common_rx_tx_pll` *(3)* | Indicates the fast PLL can be shared between receiver and transmitter applications. |

*Table 12–11. New altlvds Parameters for Stratix LVDS Transmitter (Part 1 of 2)* *Note (1)*

| Parameter | Function |
|---|---|
| `output_data_rate` *(2)* | Specifies the data rate in Mbps. This parameter replaces the multiplication factor *W*. |
| `inclock_data_alignment` | Indicates the alignment of `tx_inclk` and `tx_in` data. |
| `outclock_alignment` | Specifies the alignment of `tx_outclock` and `tx_out` data. |

***Table 12–11. New altlvds Parameters for Stratix LVDS Transmitter (Part 2 of 2)*** *Note (1)*

| Parameter | Function |
|---|---|
| `registered_input` | Specifies the clock source for the input synchronization registers, which can be either `tx_inclock` or `tx_coreclock`. Used only when the **Registered Inputs** option is selected. |
| `common_rx_tx_pll` *(3)* | Indicates the fast PLL can be shared between receiver and transmitter applications. |

***Notes to Tables 12–10 and 12–11:***

(1) You can specify these parameters in the MegaWizard Plug-In Manager.

(2) You must specify a data rate in the MegaWizard Plug-In Manager instead of a *W* factor.

(3) The same fast PLL can be used to clock both the receiver and transmitter only if both are running at the same frequency.

# Configuration

The Stratix device family supports all current configuration schemes, including the use of enhanced configuration devices, passive serial (PS), passive parallel asynchronous (PPA), fast passive parallel (FPP), and JTAG. Stratix devices also provide a number of new configuration enhancements that you can take advantage of when migrating APEX II and APEX 20K designs to the Stratix device family.

## Configuration Speed & Schemes

You can configure Stratix devices at a maximum clock speed of 100 MHz, which is faster than the 66-MHz and 33-MHz maximum configuration speeds for APEX II and APEX 20K devices, respectively. Similar to APEX II devices, you can use 8-bit parallel data to configure Stratix devices (the target device can receive byte-wide configuration data on each clock cycle) significantly speeding up configuration times.

You can select a configuration scheme based on how the `MSEL` pins are driven. Stratix devices have three `MSEL` pins (APEX II and APEX 20K devices have two `MSEL` pins) for determining the configuration scheme.

For more information about Stratix configuration schemes, refer to Chapter 13, Configuring Stratix & Stratix GX Devices.

## Remote Update Configuration

The APEX 20K device family introduced the concept of remote update configuration, where you could send the APEX 20K device new configuration files from a remote source and the device would store the files in flash memory and reconfigure itself with the new configuration data. The Stratix device family enhances support for remote update configuration with new, dedicated circuitry to handle and recover from errors. If an error occurs either during device configuration or in user mode, this new circuitry reconfigures the Stratix device to a known state. Additionally, the Stratix device has a user watchdog timer to ensure the application configuration data executes successfully during user mode. User logic must continually reset this watchdog timer in order to validate that the application configuration data is functioning properly.

For more information about how to use the remote and local update modes, refer to Chapter 15, Using Remote System Configuration with Stratix & Stratix GX Devices.

## JTAG Instruction Support

Stratix devices support two new JTAG instructions, `PULSE_NCONFIG` and `CONFIG_IO`. The `PULSE_NCONFIG` instruction emulates pulsing the `nCONFIG` signal low to trigger reconfiguration, while the actual `nCONFIG` pin on the device is unaffected. The `CONFIG_IO` instruction allows you to use the JTAG chain to configure I/O standards for all pins. Because this instruction will interrupt device configuration, you should reconfigure the Stratix device after you finish JTAG testing to ensure proper device operation. Table 12–12 compares JTAG instruction support in the Stratix device family versus APEX II and APEX 20K devices. For further information about the supported JTAG instructions, see the appropriate device family data sheet.

*Table 12–12. JTAG Instruction Support*

| JTAG Instruction | Stratix | APEX II | APEX 20K |
|---|---|---|---|
| SAMPLE/PRELOAD | ✓ | ✓ | ✓ |
| EXTEST | ✓ | ✓ | ✓ |
| BYPASS | ✓ | ✓ | ✓ |
| USERCODE | ✓ | ✓ | ✓ |
| IDCODE | ✓ | ✓ | ✓ |
| ICR Instructions | ✓ | ✓ | ✓ |
| SignalTap™ II Instructions | ✓ | ✓ | ✓ |
| HIGHZ | ✓ | ✓ | |
| CLAMP | ✓ | ✓ | |
| PULSE_NCONFIG | ✓ | | |
| CONFIG_IO | ✓ | | |

## Conclusion

The Stratix device family extends the advanced features available in the APEX II and APEX 20K device families to deliver a complete system-on-a-programmable-chip (SOPC) solution. By following these guidelines, you can easily transition current APEX II and APEX 20K designs to take advantage of the new features available in the Stratix device family

# Section VI. Configuration
## & Remote System Upgrades

This section provides configuration information for all of the supported configuration schemes for Stratix devices. These configuration schemes use either a microprocessor, configuration device, or download cable. There is detailed information on how to design with Altera enhanced configuration devices which includes information on how to manage multiple configuration files and access the on-chip FLASH memory space. The last chapter shows designers how to perform remote and local upgrades for their designs.

This section contains the following chapters:

- Chapter 13. Configuring Stratix & Stratix GX Devices
- Chapter 14. Using Altera Enhanced Configuration Devices
- Chapter 15. Using Remote System Configuration with Stratix & Stratix GX Devices

## Revision History

The table below shows the revision history for Chapters 13 through 15.

| Chapter(s) | Date / Version | Changes Made |
|---|---|---|
| 13 | April 2003<br>v1.0 | Added document to the Stratix Device Handbook. |
| 14 | April 2003<br>v1.0 | Added document to the Stratix Device Handbook. |
| 15 | April 2003<br>v1.0 | Added document to the Stratix Device Handbook. |

# 13. Configuring Stratix & Stratix GX Devices

S52013-1.0

Chapter 13, Configuring Stratix & Stratix GX Devices replaces *AN 208: Configuring Stratix & Stratix GX Devices*.

## Introduction

You can configure Stratix™ and Stratix GX devices using one of several configuration schemes. All configuration schemes use either a microprocessor, configuration device, or a download cable. See Table 13–1.

*Table 13–1. Stratix & Stratix GX Device Configuration Schemes*

| Configuration Scheme | Typical Use |
|---|---|
| Configuration devices | Configuration with the EPC16, EPC8, EPC4, or EPC2 configuration devices. |
| Passive parallel asynchronous (PPA) | Configuration with a parallel asynchronous microprocessor interface. In this scheme, the microprocessor treats the target device as memory. |
| Fast passive parallel (FPP) | Configuration with a parallel synchronous configuration device or microprocessor interface where eight bits of configuration data are loaded on every clock cycle. |
| Passive serial (PS) | Configuration with a serial synchronous microprocessor interface and the MasterBlaster™ communications cable or ByteBlasterMV™ parallel port download cable. |
| Remote/local update FPP | Configuration using a Nios™ embedded processor. Allows you to update the Stratix or Stratix GX device configuration remotely using the FPP scheme to load data. |
| Remote/local update PPA | Passive parallel synchronous configuration using a Nios embedded processor. In this scheme, the Nios microprocessor treats the target device as memory. Allows you to update the Stratix or Stratix GX device configuration remotely using the PPA scheme to load data. |
| Remote/local update PS | Passive serial synchronous configuration using a Nios embedded processor. Allows you to update the Stratix or Stratix GX device configuration remotely using the PS scheme to load data. |
| Joint Test Action Group (JTAG) | Configuration through the IEEE Std. 1149.1 JTAG pins. You can perform JTAG configuration with either a download cable or an embedded device. |

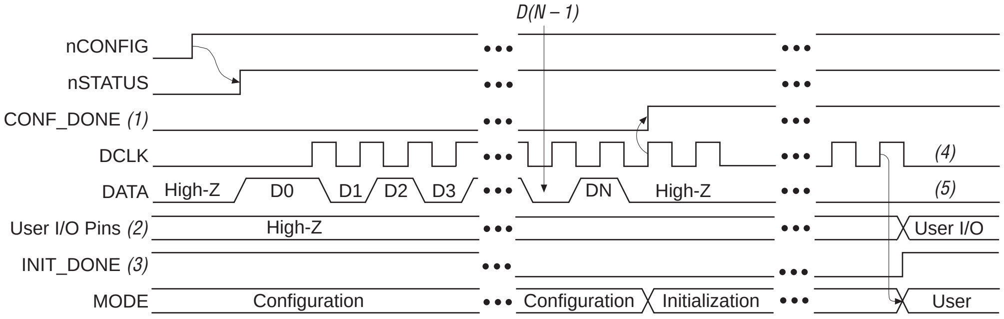
This chapter discusses how to configure one or more Stratix or Stratix GX devices. It should be used together with the following documents:

- *MasterBlaster Serial/USB Communications Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheets*
- *Configuration Devices for SRAM-Based LUT Devices Data Sheet*
- *Enhanced Configuration Devices (EPC4, EPC8, & EPC16) Data Sheet*
- Chapter 15, Using Remote System Configuration with Stratix & Stratix GX Devices

## Device Configuration Overview

During device operation, the FPGA stores configuration data in SRAM cells. Because SRAM memory is volatile, you must load the SRAM cells with the configuration data each time the device powers up. After configuration, the device must initialize its registers and I/O pins. After initialization, the device enters user mode. Figure 13–1 shows the state of the device during the configuration, initialization, and user mode.

***Figure 13–1. Stratix & Stratix GX Configuration Cycle***



*Notes to Figure 13–1:*

(1) During initial power up and configuration, `CONF_DONE` is low. After configuration, `CONF_DONE` goes high. If the device is reconfigured, `CONF_DONE` goes low after `nCONFIG` is driven low.

(2) User I/O pins are tri-stated during configuration. Stratix and Stratix GX devices also have a weak pull-up resistor on I/O pins during configuration. After initialization, the user I/O pins perform the function assigned in the user's design.

(3) When used, the optional `INIT_DONE` signal is high when `nCONFIG` is low before configuration and during the first 136 clock cycles of configuration.

(4) `DCLK` should not be left floating. It should be driven high or low.

(5) `DATA0` should not be left floating. It should be driven high or low.

You can load the configuration data for the Stratix or Stratix GX device using a passive configuration scheme. When using any passive configuration scheme, the Stratix or Stratix GX device is incorporated into a system with an intelligent host, such as a microprocessor, that controls the configuration process. The host supplies configuration data from a storage device (e.g., a hard disk, RAM, or other system memory). When using passive configuration, you can change the target device's functionality while the system is in operation by reconfiguring the device. You can also perform in-field upgrades by distributing a new programming file to system users.

The following sections describe the `MSEL[2..0]`, `VCCSEL`, `PORSEL`, and `nIO_PULLUP` pins used in Stratix and Stratix GX device configuration.

## MSEL[2..0] Pins

You can select a Stratix or Stratix GX device configuration scheme by driving its `MSEL2`, `MSEL1`, and `MSEL0` pins either high or low, as shown in Table 13–2.

**Table 13–2. Stratix & Stratix GX Device Configuration Schemes**

| MSEL2 | MSEL1 | MSEL0 | Description |
|---|---|---|---|
| 0 | 0 | 0 | FPP configuration |
| 0 | 0 | 1 | PPA configuration |
| 0 | 1 | 0 | PS configuration |
| 1 | 0 | 0 | Remote/local update FPP *(1)* |
| 1 | 0 | 1 | Remote/local update PPA *(1)* |
| 1 | 1 | 0 | Remote/local update PS *(1)* |

*Note to Table 13–2:*

(1) These schemes require that you drive a secondary pin `RUnLU` to specify whether to perform Remote Update or Local Update.

## VCCSEL Pins

You can configure Stratix and Stratix GX devices using the 3.3-, 2.5-, 1.8-, or 1.5-V LVTTL I/O standard on configuration and JTAG input pins. `VCCSEL` is a dedicated pin on Stratix and Stratix GX devices that sets the I/O standard voltage level on the input buffers of configuration pins (`DCLK`, `CONF_DONE`, `nSTATUS`, `nCONFIG`, `MSEL0`, `MSEL1`, `MSEL2`, and `nCE`), JTAG pins (`TDI`, `TDO`, `TMS`, `TCK`, and `TRST`), as well as `PLL_ENA` pins. The `VCCSEL` pin configures all programming and JTAG input pins to 3.3/2.5-V Schmidt trigger LVTTL or 1.8-V Schmidt trigger LVTTL (see Table 13–3).

*Table 13–3. VCCSEL Pin Settings*

| VCCSEL | Input Buffer Settings on Configuration & JTAG Pins |
|---|---|
| GND | 3.3/2.5-V Schmidt trigger LVTTL |
| $V_{CCIO}$ | 1.8-V Schmidt trigger LVTTL |

### PORSEL Pins

This dedicated input pin is used to select POR delay times of 2 ms or 100 ms during power-up. When the `PORSEL` pin is connected to `GND`, POR time is 100 ms; when it is connected to `VCC`, the POR time is 2 ms.

### nIO_PULLUP Pins

This input pin must be tied to `VCC` or `GND`. If it is connected to `VCC` during configuration, the weak pull-ups on all user I/O pins are disabled. If connected to `GND`, the pull-ups are enabled during configuration. (The `nIO_PULLUP` pin can be pulled to 1.5 V, 1.8 V, 2.5 V, or 3.3 V for `VCC` level connection.)

## Configuration File Size

Tables 13–4 and 13–5 summarize the approximate configuration file size required for each Stratix and Stratix GX device. To calculate the amount of storage space required for multi-device configurations, add the file size of each device together.

*Table 13–4. Stratix Configuration File Sizes*

| Device | SRAM Object File (.sof) Size (Bits) |
|---|---|
| EP1S10 | 3,534,640 |
| EP1S20 | 5,904,832 |
| EP1S25 | 7,894,144 |
| EP1S30 | 10,379,368 |
| EP1S40 | 12,389,632 |
| EP1S60 | 17,543,968 |
| EP1S80 | 23,834,032 |

*Table 13–5. Stratix GX Configuration File Sizes*

| Device | SRAM Object File (.sof) Size (Bits) |
|---|---|
| EP1SGX10C | 3,579,928 |
| EP1SGX10D | 3,579,928 |
| EP1SGX25C | 7,951,248 |
| EP1SGX25D | 7,951,248 |
| EP1SGX25F | 7,951,248 |
| EP1SGX40D | 12,531,440 |
| EP1SGX40G | 12,531,440 |

You should only use the numbers in Tables 13–4 and 13–5 to estimate the file size before design compilation. The exact file size may vary because different Altera® Quartus® II software versions may add a slightly different number of padding bits during programming. However, for any specific version of the Quartus II software, any design targeted for the same device has the same configuration file size.

Table 13–6 lists Altera configuration devices that you can use to configure Stratix and Stratix GX devices.

*Table 13–6. Configuration Devices*

| Device | Description |
|---|---|
| EPC16 *(1)* | 16,000,000 × 1-bit device with 3.3-V operation *(2)* |
| EPC8 *(1)* | 8,000,000 × 1-bit device with 3.3-V operation *(2)* |
| EPC4 *(1)* | 4,000,000 × 1-bit device with 3.3-V operation *(2)* |
| EPC2 | 1,695,680 × 1-bit device with 5.0-V or 3.3-V operation |

***Notes to Table 13–6:***

(1) EPC16, EPC8, and EPC4 devices are enhanced configuration devices.

(2) This data is measured before compression. With compression, configuration devices can store 1.9 times as much data as the size listed.

You can use the data from Tables 13–4 through 13–6 to determine the number of configuration devices required to configure your device. For example, to configure one Stratix EP1S10 device, you need one EPC4 configuration device. Similarly, one Stratix EP1S80 device requires one EPC16 configuration device.

# Configuration Schemes

This section describes how to configure Stratix and Stratix GX devices with the following configuration schemes:

- Configuration Devices
- PS Configuration with a Download Cable
- PS Configuration with a Microprocessor
- FPP Configuration
- PPA Configuration
- JTAG Programming & Configuration
- JTAG Programming & Configuration of Multiple Devices

## Configuration Devices

The configuration device scheme uses an Altera configuration device to supply data to the Stratix or Stratix GX device in a serial bitstream (see Figure 13–3).

In the configuration device scheme, `nCONFIG` is usually tied to $V_{CC}$ (when using EPC16, EPC8, EPC4, or EPC2 devices, `nCONFIG` may be connected to `nINIT_CONF`). Upon device power-up, the target Stratix or Stratix GX device senses the low-to-high transition on `nCONFIG` and initiates configuration. The target device then drives the open-drain `CONF_DONE` pin low, which in-turn drives the configuration device's `nCS` pin low. When exiting power-on reset (POR), both the target and configuration device release the open-drain `nSTATUS` pin.

Before configuration begins, the configuration device goes through a POR delay of up to 200 ms to allow the power supply to stabilize (power the Stratix or Stratix GX device before or during the POR time of the configuration device). This POR delay has a maximum of 200 ms for EPC2 devices. For enhanced configuration devices, you can select between 2 ms and 100 ms by connecting `PORSEL` pin to `VCC` or `GND`, accordingly. During this time, the configuration device drives its `OE` pin low. This low signal delays configuration because the `OE` pin is connected to the target device's `nSTATUS` pin. When the target and configuration devices complete POR, they release `nSTATUS`, which is then pulled high by a pull-up resistor.

When configuring multiple devices, configuration does not begin until all devices release their `OE` or `nSTATUS` pins. When all devices are ready, the configuration device clocks data out serially to the target devices using an internal oscillator.

After successful configuration, the configuration device starts clocking the target device for initialization. The `CONF_DONE` pin is released by the target device and then pulled high by a pull-up resistor. When initialization is complete, the configuration device enters user mode.

If an error occurs during configuration, the target device drives its `nSTATUS` pin low, resetting itself internally and resetting the configuration device. If the *Auto-Restart Configuration on Frame Error* option—available in the Quartus II **Global Device Options** dialog box (Assign menu)—is turned on, the device reconfigures automatically if an error occurs. To find this option, choose **Compiler Settings** (Processing menu), then click on the **Chips & Devices** tab.

If this option is turned off, the external system must monitor `nSTATUS` for errors and then pulse `nCONFIG` low to restart configuration. The external system can pulse `nCONFIG` if it is under system control rather than tied to $V_{CC}$. When configuration is complete, the target device releases `CONF_DONE`, which disables the configuration device by driving `nCS` high. The configuration device drives `DCLK` low before and after configuration.

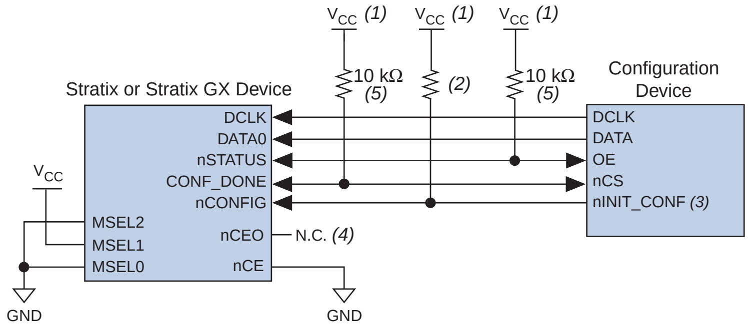
In addition, if the configuration device sends all of its data and then detects that `CONF_DONE` has not gone high, it recognizes that the target device has not configured successfully. In this case, the configuration device pulses its `OE` pin low for a few microseconds, driving the target device's `nSTATUS` pin low. If the *Auto-Restart Configuration on Frame Error* option is set in the software, the target device resets and then pulses its `nSTATUS` pin low. When `nSTATUS` returns high, the configuration device reconfigures the target device. When configuration is complete, the configuration device drives `DCLK` low.

Do not pull `CONF_DONE` low to delay initialization. Instead, use the Quartus II software's *User-Supplied Start-Up Clock* option to synchronize the initialization of multiple devices that are not in the same configuration chain. Devices in the same configuration chain initialize together. When `CONF_DONE` is driven low after device configuration, the configuration device recognizes that the target device has not configured successfully. For more information on this option, see "Device Options" on page 13–51.

☞ If using the EPC16, EPC8, EPC4, or EPC2 device to configure a Stratix or Stratix GX device, connect the `VCCSEL` pin to `GND` to select 3.3 V / 2.5 V input buffer setting. This connection is to make the devices compatible.

Figure 13–2 shows how to configure one Stratix or Stratix GX device with one configuration device.

**Figure 13–2. Single Device Configuration Circuit**



*Notes to Figure 13–2:*

(1) The pull-up resistor should be connected to the same supply voltage as the configuration device.

(2) These pull-up resistors are 1-kΩ resistors. The EPC16, EPC8, EPC4, and EPC2 devices' `OE` and `nCS` pins have internal, user-configurable pull-up resistors. If you use internal pull-up resistors, do not use external pull-up resistors on these pins.

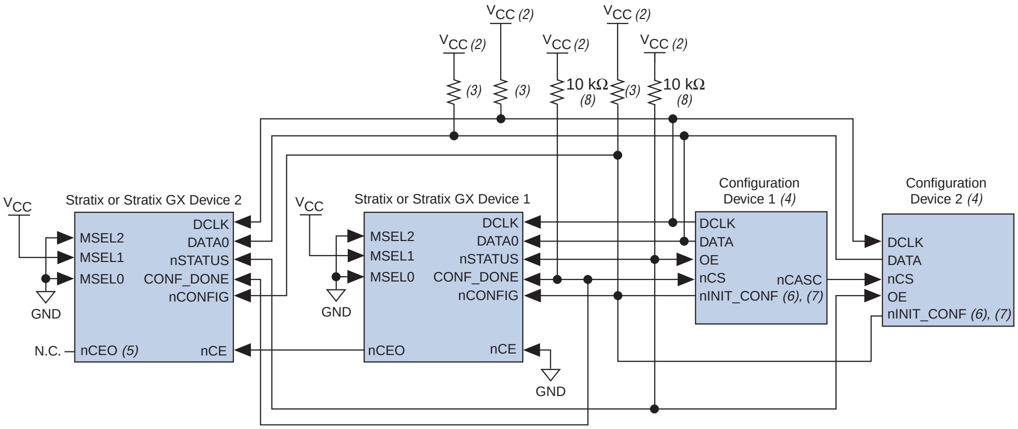
(3) The `nINIT_CONF` pin is available on EPC16, EPC8, EPC4, and EPC2 devices. If `nINIT_CONF` is not used, `nCONFIG` must be pulled to $V_{CC}$ through a resistor.

(4) The `nCEO` pin is left unconnected for the last device in the chain.

(5) If external pull-ups are used on CONF_DONE and nSTATUS pins, they should always be 10 kΩ. You can use the internal pull-ups of the configuration device only if the CONF_DONE and nSTATUS signals are pulled-up to 3.3 V or 2.5 V (not 1.8 V or 1.5 V).

Figure 13–3 shows how to configure multiple Stratix and Stratix GX devices with multiple configuration devices.

*Figure 13–3. Multi-Device Configuration Circuit* Note (1)



*Notes to Figure 13–3:*

(1) When performing multi-device active serial configuration, you must generate the configuration device programmer object file (**.pof**) from each project's SOF. You can combine multiple SOFs using the Quartus II software through the **Device & Pin Option** dialog box (see "Device Options" on page 13–51 for more information). For more information on how to create configuration and programming files, see "Device Configuration Files" on page 13–57.

(2) The pull-up resistor should be connected to the same supply voltage as the configuration device.

(3) These pull-up resistors are 1 kΩ. The EPC16, EPC8, EPC4, and EPC2 devices' `OE` and `nCS` pins have internal, user-configurable pull-up resistors. If you use internal pull-up resistors, do not use external pull-up resistors on these pins.

(4) EPC16, EPC8, and EPC4 configuration devices cannot be cascaded.

(5) The `nCEO` pin is left unconnected for the last device in the chain.

(6) The `nINIT_CONF` pin is available on EPC16, EPC8, EPC4, and EPC2 devices. If `nINIT_CONF` is not used, `nCONFIG` must be pulled to $V_{CC}$ through a resistor.

(7) The `nINIT_CONF` pin has an internal pull-up resistor that is always active in EPC16, EPC8, EPC4, and EPC2 devices. These devices do not need an external pull-up resistor on the `nINIT_CONF` pin.

(8) If external pull-ups are used on CONF_DONE and nSTATUS pins, they should always be 10 kΩ. You can use the internal pull-ups of the configuration device only if the CONF_DONE and nSTATUS signals are pulled-up to 3.3 V or 2.5 V (not 1.8 V or 1.5 V).

After the first Stratix or Stratix GX device completes configuration during multi-device configuration, its `nCEO` pin activates the second device's `nCE` pin, prompting the second device to begin configuration. Because all device `CONF_DONE` pins are tied together, all devices initialize and enter user mode at the same time.

In addition, all `nSTATUS` pins are tied together; thus, if any device (including the configuration devices) detects an error, configuration stops for the entire chain. Also, if the first configuration device does not detect `CONF_DONE` going high at the end of configuration, it resets the chain by pulsing its `OE` pin low for a few microseconds. This low pulse drives the `OE` pin low on the second configuration device and drives `nSTATUS` low on all Stratix and Stratix GX devices, causing them to enter an error state.

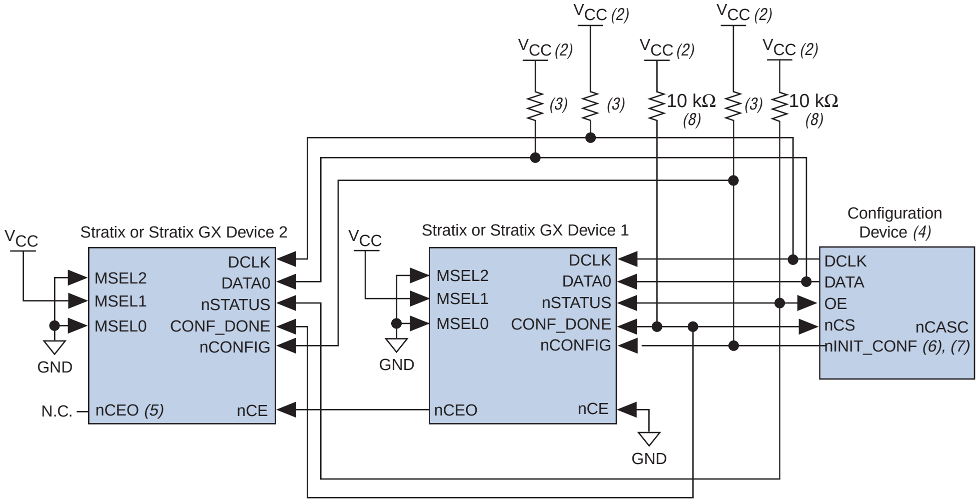
If the *Auto-Restart Configuration on Frame Error* option is turned on in the software, the Stratix or Stratix GX device releases its `nSTATUS` pins after a reset time-out period. When the `nSTATUS` pins are released and pulled high, the configuration devices reconfigure the chain. If the *Auto-Restart Configuration on Frame Error* option is not turned on, the Stratix or Stratix GX devices drive `nSTATUS` low until they are reset with a low pulse on `nCONFIG`.

You can also cascade several EPC2 configuration devices to configure multiple Stratix and Stratix GX devices. When all data from the first configuration device is sent, it drives `nCASC` low, which in turn drives `nCS` on the subsequent configuration device. Because a configuration device requires less than one clock cycle to activate a subsequent configuration device, the data stream is uninterrupted. You cannot cascade EPC16, EPC8, and EPC4 configuration devices.

You can use a single configuration chain to configure multiple Stratix and Stratix GX devices. In this scheme, the `nCEO` pin of the first device is connected to the `nCE` pin of the second device in the chain. If there are additional devices, connect the `nCE` pin of the next device to the `nCEO` pin of the previous device. To configure properly, all of the device `CONF_DONE` and `nSTATUS` pins must be tied together.

Figure 13–4 shows an example of configuring multiple Stratix and Stratix GX devices using a configuration device.

*Figure 13–4. Configuring Multiple Stratix & Stratix GX Devices with A Single Configuration Device* Note (1)



*Notes to Figure 13–4:*

(1) When performing multi-device active serial configuration, you must generate the configuration device programmer object file (**.pof)** from each project's SOF. You can combine multiple SOFs using the Quartus II software through the **Device & Pin Option** dialog box (see "Device Options" on page 13–51 for more information). For more information on how to create configuration and programming files, see "Device Configuration Files" on page 13–57.

(2) The pull-up resistor should be connected to the same supply voltage as the configuration device.

(3) These pull-up resistors are 1 kΩ. The EPC16, EPC8, EPC4, and EPC2 devices' `OE` and `nCS` pins have internal, user-configurable pull-up resistors. If you use internal pull-up resistors, do not use external pull-up resistors on these pins.

(4) EPC16, EPC8, and EPC4 configuration devices cannot be cascaded.

(5) The `nCEO` pin is left unconnected for the last device in the chain.

(6) The `nINIT_CONF` pin is available on EPC16, EPC8, EPC4, and EPC2 devices. If `nINIT_CONF` is not used, `nCONFIG` must be pulled to $V_{CC}$ through a resistor.

(7) The `nINIT_CONF` pin has an internal pull-up resistor that is always active in EPC16, EPC8, EPC4, and EPC2 devices. These devices do not need an external pull-up resistor on the `nINIT_CONF` pin.

(8) If external pull-ups are used on CONF_DONE and nSTATUS pins, they should always be 10 kΩ. You can use the internal pull-ups of the configuration device only if the CONF_DONE and nSTATUS signals are pulled-up to 3.3 V or 2.5 V (not 1.8 V or 1.5 V).

Table 13–7 shows the status of the device `DATA` pins during and after configuration.

*Table 13–7. DATA Pin Status Before & After Configuration*

| Pins | Stratix or Stratix GX Device | |
|---|---|---|
| | During | After |
| `DATA0` *(1)* | Used for configuration | User defined |
| `DATA[7..1]` *(2)* | Used in some configuration modes | User defined |
| I/O Pins | Tri-state | User defined |

***Notes to Table 13–7:***

(1) The status shown is for configuration with a configuration device.

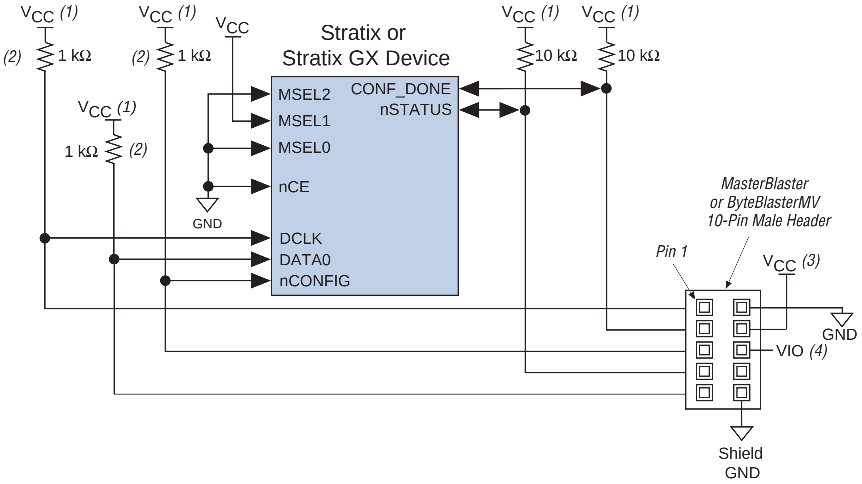
(2) The function of these pins depends upon the settings specified in the Quartus II software using the **Device & Pin Option** dialog box (see "Device Options" on page 13–51 for more information). For more information, refer to the Quartus II Help software.

## PS Configuration with a Download Cable

In PS configuration with a download cable, an intelligent host transfers data from a storage device to the Stratix or Stratix GX device through the MasterBlaster or ByteBlasterMV cable. To initiate configuration in this scheme, the download cable generates a low-to-high transition on the `nCONFIG` pin. The programming hardware then places the configuration data one bit at a time on the device's `DATA0` pin. The data is clocked into the target device until `CONF_DONE` goes high.

When using programming hardware for the Stratix or Stratix GX device, turning on the *Auto-Restart Configuration on Frame Error* option does not affect the configuration cycle because the Quartus II software must restart configuration when an error occurs. Figure 13–5 shows PS configuration for the Stratix or Stratix GX device using a MasterBlaster or ByteBlasterMV cable.

*Figure 13–5. PS Configuration Circuit with MasterBlaster or ByteBlasterMV Cable*



*Notes to Figure 13–5:*

(1) You should connect the pull-up resistor to the same supply voltage as the MasterBlaster (`VIO` pin) or ByteBlasterMV cable.

(2) The pull-up resistors on the `DATA0` and `DCLK` pins are only needed if the download cable is the only configuration scheme used on the board. This is to ensure that the `DATA0` and `DCLK` pins are not left floating after configuration. For example, if the design also uses a configuration device, the pull-up resistors on the `DATA0` and `DCLK` pins are not necessary.

(3) Power supply voltage: $V_{CC}$ = 3.3 V or 5.0 V for the MasterBlaster and ByteBlasterMV cable.

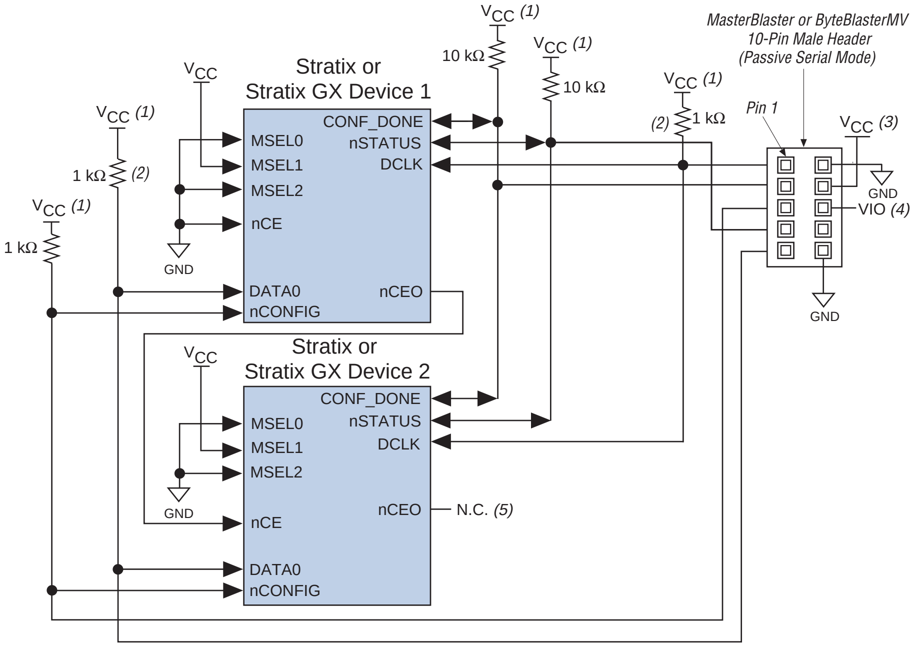
(4) Pin 6 of the header is a $V_{IO}$ reference voltage for the MasterBlaster output driver. $V_{IO}$ should match the device's $V_{CCIO}$. This pin is a no-connect pin for the ByteBlasterMV header.

You can use programming hardware to configure multiple Stratix and Stratix GX devices by connecting each device's `nCEO` pin to the subsequent device's `nCE` pin. All other configuration pins are connected to each device in the chain.

Because all `CONF_DONE` pins are tied together, all devices in the chain initialize and enter user mode at the same time. In addition, because the `nSTATUS` pins are tied together, the entire chain halts configuration if any device detects an error. In this situation, the Quartus II software must restart configuration; the *Auto-Restart Configuration on Frame Error* option does not affect the configuration cycle.

Figure 13–6 shows how to configure multiple Stratix and Stratix GX devices with a MasterBlaster or ByteBlasterMV cable.

*Figure 13–6. Multi-Device PS Configuration with a MasterBlaster or ByteBlasterMV Cable*



*Notes to Figure 13–6:*

(1) You should connect the pull-up resistor to the same supply voltage as the MasterBlaster (`VIO` pin) or ByteBlasterMV cable.

(2) The pull-up resistors on the `DATA0` and `DCLK` pins are only needed if the download cable is the only configuration scheme used on the board. This is to ensure that the `DATA0` and `DCLK` pins are not left floating after configuration. For example, if the design also uses a configuration device, the pull-up resistors on the `DATA0` and `DCLK` pins are not necessary.

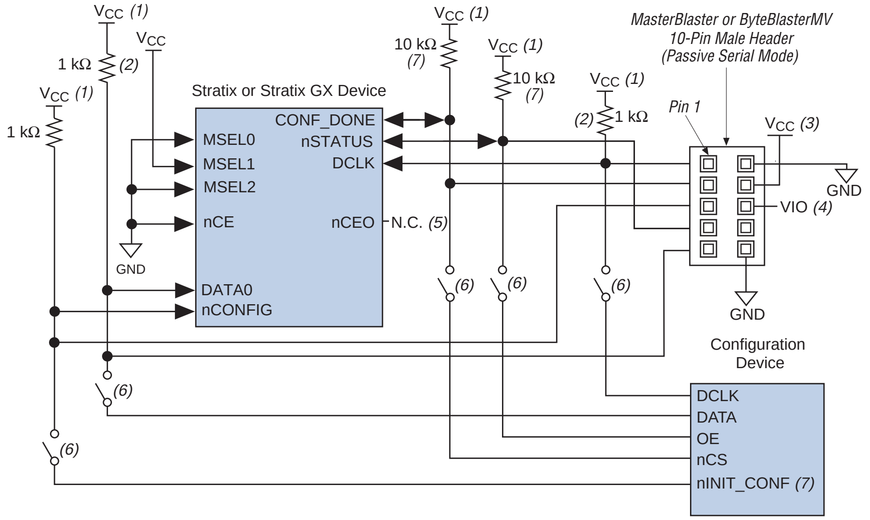
(3) Power supply voltage: $V_{CC}$ = 3.3 V or 5.0 V for the MasterBlaster and ByteBlasterMV cable.

(4) $V_{IO}$ is a reference voltage for the MasterBlaster output driver. $V_{IO}$ should match the device's $V_{CCIO}$. Refer to the *MasterBlaster Serial/USB Communications Cable Data Sheet* for this value.

(5) The `nCEO` pin is left unconnected for the last device in the chain.

If you are using a MasterBlaster or ByteBlasterMV cable to configure device(s) on a board that also has configuration devices, you should electrically isolate the configuration devices from the target device(s) and cable. One way to isolate the configuration devices is to add logic, such as a multiplexer, that can select between the configuration devices and the cable. The multiplexer device should allow bidirectional transfers on the `nSTATUS` and `CONF_DONE` signals. Another option is to add switches to the five common signals (`CONF_DONE`, `nSTATUS`, `DCLK`, `nCONFIG`, and `DATA0`) between the cable and the configuration devices. The last option is to remove the configuration devices from the board when configuring with the cable. Figure 13–7 shows a combination of a configuration device and a MasterBlaster or ByteBlasterMV cable to configure a Stratix or Stratix GX device.

**Figure 13–7. Configuring with a Combined PS & Configuration Device Scheme**



*Notes to Figure 13–7:*

(1) You should connect the pull-up resistor to the same supply voltage as the configuration device.
(2) The pull-up resistors on the `DATA0` and `DCLK` pins are only needed if the download cable is the only configuration scheme used on the board. This is to ensure that the `DATA0` and `DCLK` pins are not left floating after configuration. For example, if the design also uses a configuration device, the pull-up resistors on the `DATA0` and `DCLK` pins are not necessary.
(3) Power supply voltage: $V_{CC}$ = 3.3 V or 5.0 V for the MasterBlaster and ByteBlasterMV cable.
(4) Pin 6 of the header is a $V_{IO}$ reference voltage for the MasterBlaster output driver. $V_{IO}$ should match the target device's $V_{CCIO}$. This is a no-connect pin for the ByteBlasterMV header.
(5) The `nCEO` pin is left unconnected.
(6) You should not attempt configuration with a MasterBlaster or ByteBlasterMV cable while a configuration device is connected to a Stratix or Stratix GX device. Instead, you should either remove the configuration device from its socket when using the download cable or place a switch on the five common signals between the download cable and the configuration device. Remove the MasterBlaster or ByteBlasterMV cable when configuring with a configuration device.
(7) If `nINIT_CONF` is not used, `nCONFIG` must be pulled to $V_{CC}$ either directly or through a resistor.
(8) If external pull-ups are used on `CONF_DONE` and `nSTATUS` pins, they should always be 10 kΩ. You can use the internal pull-ups of the configuration device only if the `CONF_DONE` and `nSTATUS` signals are pulled-up to 3.3 V or 2.5 V (not 1.8 V or 1.5 V).

For more information on how to use the MasterBlaster or ByteBlasterMV cables, see the following documents:

- *MasterBlaster Serial/USB Communications Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*

## PS Configuration with a Microprocessor

In PS configuration with a microprocessor, a microprocessor transfers data from a storage device to the target Stratix or Stratix GX device. To initiate configuration in this scheme, the microprocessor must generate a low-to-high transition on the `nCONFIG` pin and the target device must release `nSTATUS`. The microprocessor or programming hardware then places the configuration data one bit at a time on the `DATA0` pin of the Stratix or Stratix GX device. The least significant bit (LSB) of each data byte must be presented first. Data is clocked continuously into the target device until `CONF_DONE` goes high.

After all configuration data is sent to the Stratix and Stratix GX device, the `CONF_DONE` pin will go high to show successful configuration and the start of initialization. Initialization, by default, uses an internal oscillator, which runs at 10 MHz. If you are using the `clkusr` option, after all data is transferred `clkusr` must be clocked an additional 136 times for the Stratix or Stratix GX device to initialize properly. Driving `DCLK` to the device after configuration is complete does not affect device operation.

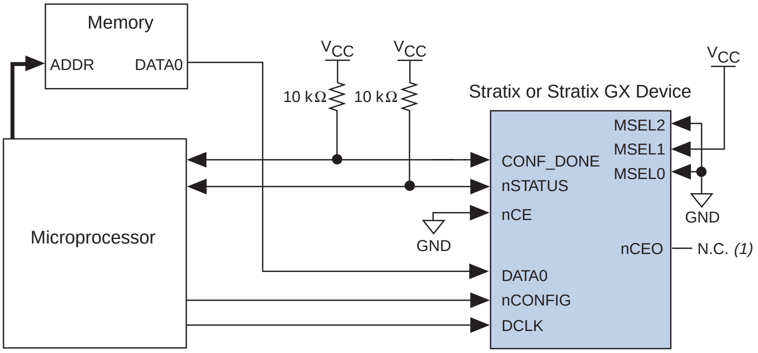
Handshaking signals are not used in PS configuration modes. Therefore, the configuration clock speed must be below the specified frequency to ensure correct configuration. No maximum `DCLK` period exists. You can pause configuration by halting `DCLK` for an indefinite amount of time.

If the target device detects an error during configuration, it drives its `nSTATUS` pin low to alert the microprocessor. The microprocessor can then pulse `nCONFIG` low to restart the configuration process. Alternatively, if the *Auto-Restart Configuration on Frame Error* option is turned on in the Quartus II software, the target device releases `nSTATUS` after a reset time-out period. After `nSTATUS` is released, the microprocessor can reconfigure the target device without needing to pulse `nCONFIG` low.

The microprocessor can also monitor the `CONF_DONE` and `INIT_DONE` pins to ensure successful configuration. If the microprocessor sends all data and the initialization clock starts but `CONF_DONE` and `INIT_DONE` have not gone high, it must reconfigure the target device.

Figure 13–8 shows the circuit for PS configuration with a microprocessor.

**Figure 13–8. PS Configuration Circuit with Microprocessor**



*Note to Figure 13–8:*

(1) The `nCEO` pin is left unconnected.

Figure 13–9 shows the PS configuration timing waveform for Stratix and Stratix GX devices. Table 13–8 shows the PS timing parameters for Stratix and Stratix GX devices.

**Figure 13–9. PS Timing Waveform for Stratix & Stratix GX Devices**

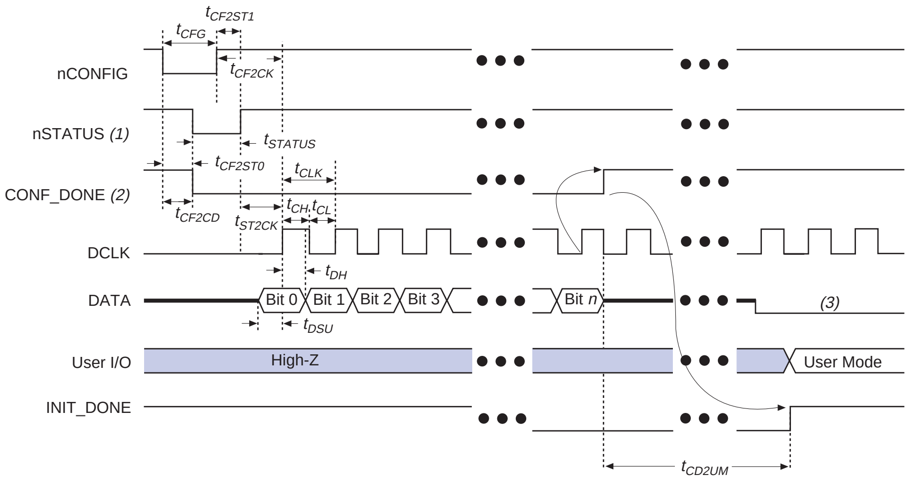


*Table 13–8. PS Timing Parameters for Stratix & Stratix GX Devices*

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $t_{CF2CD}$ | `nCONFIG` low to `CONF_DONE` low | | 800 | ns |
| $t_{CF2ST0}$ | `nCONFIG` low to `nSTATUS` low | | 800 | ns |
| $t_{CF2ST1}$ | `nCONFIG` high to `nSTATUS` high | | 40 *(3)* | µs |
| $t_{CFG}$ | `nCONFIG` low pulse width *(1)* | 40 | | µs |
| $t_{STATUS}$ | `nSTATUS` low pulse width | 10 | 40 *(3)* | µs |
| $t_{CF2CK}$ | `nCONFIG` high to first rising edge on `DCLK` | 40 | | µs |
| $t_{ST2CK}$ | `nSTATUS` high to first rising edge on `DCLK` | 1 | | µs |
| $t_{DSU}$ | Data setup time before rising edge on `DCLK` | 7 | | ns |
| $t_{DH}$ | Data hold time after rising edge on `DCLK` | 0 | | ns |
| $t_{CH}$ | `DCLK` high time | 4 | | ns |
| $t_{CL}$ | `DCLK` low time | 4 | | ns |
| $t_{CLK}$ | `DCLK` period | 10 | | ns |
| $f_{MAX}$ | `DCLK` maximum frequency | | 100 | MHz |
| $t_{CD2UM}$ | `CONF_DONE` high to user mode *(2)* | 6 | 20 | µs |

*Notes to Table 13–8:*

(1) This value applies only if the internal oscillator is selected as the clock source for starting up the device. If the clock source is `CLKUSR` or `DCLK`, multiply the clock period by 270 to obtain this value.

(2) The minimum and maximum numbers apply only if the internal oscillator is chosen as the clock source for starting up the device. If the clock source is `CLKUSR` or `DCLK`, multiply the clock period by 140 to obtain this value.

(3) This value is obtainable if users do not delay configuration by extending the `nSTATUS` low pulse width.

## FPP Configuration

Parallel configuration of Stratix and Stratix GX devices meets the continuously increasing demand for faster configuration times. Stratix and Stratix GX devices can receive byte-wide configuration data per clock cycle, and guarantee a configuration time of less than 100 ms with a 100-MHz configuration clock. Stratix and Stratix GX devices support programming data bandwidth up to 800 megabits per second (Mbps) in this mode. You can use parallel configuration with an EPC16, EPC8, or EPC4 device, or a microprocessor.

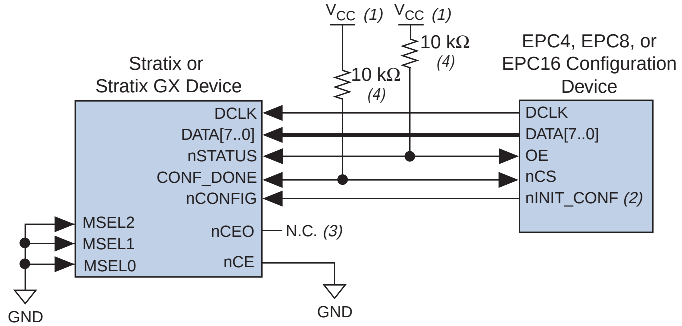
This section discusses the following schemes for FPP configuration in Stratix and Stratix GX devices:

- FPP Configuration Using an Enhanced Configuration Device
- Parallel Configuration Using a Microprocessor

### *FPP Configuration Using an Enhanced Configuration Device*

The enhanced configuration device scheme in a parallel configuration uses an EPC16, EPC8, or EPC4 device to supply data in a byte-wide fashion to the Stratix or Stratix GX device. See Figure 13–10.

***Figure 13–10. FPP Configuration Using Configuration Devices***



***Notes to Figure 13–10:***

(1) The pull-up resistors should be connected to the same supply voltage as the EPC16, EPC8, or EPC4 device.

(2) If `nINIT_CONF` is not used, `nCONFIG` must be pulled to $V_{CC}$ either directly or through a 1-kΩ resistor.

(3) The `nCEO` pin is left unconnected for the last device on the chain.

(4) If external pull-ups are used on `CONF_DONE` and `nSTATUS` pins, they should always be 10 kΩ. You can use the internal pull-ups of the configuration device only if the `CONF_DONE` and `nSTATUS` signals are pulled-up to 3.3 V or 2.5 V (not 1.8 V or 1.5 V).

In the enhanced configuration device scheme, `nCONFIG` is tied to `nINIT_CONF`. On power up, the target Stratix or Stratix GX device senses the low-to-high transition on `nCONFIG` and initiates configuration. The target Stratix or Stratix GX device then drives the open-drain `CONF_DONE` pin low, which in-turn drives the enhanced configuration device's `nCS` pin low.

Before configuration starts, there is a 2-ms POR delay if the `PORSEL` pin is connected to $V_{CC}$ in the enhanced configuration device. If the `PORSEL` pin is connected to ground, the POR delay is 100 ms. When each device determines that its power is stable, it releases its `nSTATUS` or `OE` pin. Because the enhanced configuration device's `OE` pin is connected to the target Stratix or Stratix GX device's `nSTATUS` pin, configuration is delayed until both the `nSTATUS` and `OE` pins are released by each device. The `nSTATUS` and `OE` pins are pulled up by a resistor on their respective devices once they are released. When configuring multiple devices, connect the `nSTATUS` pins together to ensure configuration only happens when all devices release their `OE` or `nSTATUS` pins. The enhanced configuration device then clocks data out in parallel to the Stratix or Stratix GX device using a 66-MHz internal oscillator, or drives it to the Stratix or Stratix GX device through the `EXTCLK` pin.

If there is an error during configuration, the Stratix or Stratix GX device drives the `nSTATUS` pin low, resetting itself internally and resetting the enhanced configuration device. The Quartus II software provides an *Auto-restart configuration after error* option that automatically initiates the reconfiguration whenever an error occurs. See "Device Options" on page 13–51 for information on how to turn this option on or off.

If this option is turned off, you must set monitor `nSTATUS` to check for errors. To initiate reconfiguration, pulse `nCONFIG` low. The external system can pulse `nCONFIG` if it is under system control rather than tied to $V_{CC}$. Therefore, `nCONFIG` must be connected to `nINIT_CONF` if you want to reprogram the Stratix or Stratix GX device on the fly.

When configuration is complete, the Stratix or Stratix GX device releases the `CONF_DONE` pin, which is then pulled up by a resistor. This action disables the EPC16, EPC8, or EPC4 enhanced configuration device as `nCS` is driven high. When initialization is complete, the Stratix or Stratix GX device enters user mode. The enhanced configuration device drives `DCLK` low before and after configuration.

If, after sending out all of its data, the enhanced configuration device does not detect `CONF_DONE` going high, it recognizes that the Stratix or Stratix GX device has not configured successfully. The enhanced configuration device pulses its `OE` pin low for a few microseconds, driving the `nSTATUS` pin on the Stratix or Stratix GX device low. If the *Auto-restart configuration after error* option is on, the Stratix or Stratix GX device resets and then pulses its `nSTATUS` low. When `nSTATUS` returns high, reconfiguration is restarted (see Figure 13–11 on page 13–21).

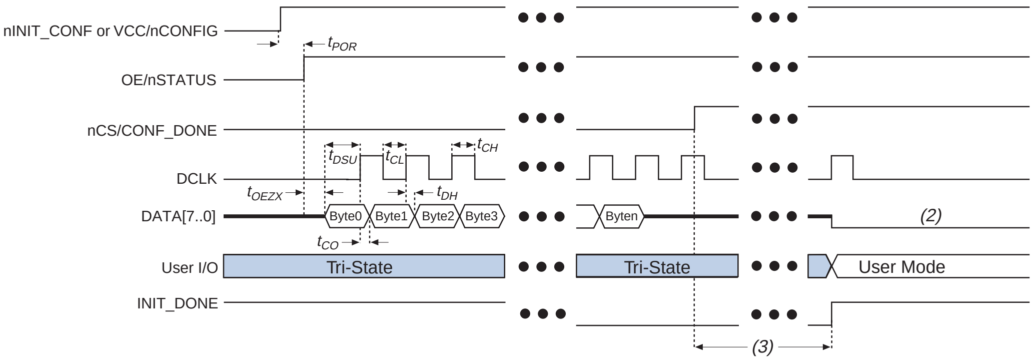
Do not drive `CONF_DONE` low after device configuration to delay initialization. Instead, use the *Enable user-supplied start-up clock* option in the **Device & Pin Options** dialog box. You can use this option to synchronize the initialization of multiple devices that are not in the same configuration chain. Devices in the same configuration chain initialize together.

After the first Stratix or Stratix GX device completes configuration during multi-device configuration, its `nCEO` pin activates the second Stratix or Stratix GX device's `nCE` pin, prompting the second device to begin configuration. Because `CONF_DONE` pins are tied together, all devices initialize and enter user mode at the same time. Because `nSTATUS` pins are tied together, configuration stops for the whole chain if any device (including enhanced configuration devices) detects an error. Also, if the enhanced configuration device does not detect a high on `CONF_DONE` at the end of configuration, it pulses its `OE` low for a few microseconds to reset the chain. The low `OE` pulse drives `nSTATUS` low on all Stratix and Stratix GX devices, causing them to enter an error state. This state is similar to a Stratix or Stratix GX device detecting an error.

If the *Auto-restart configuration after error* option is on, the Stratix and Stratix GX devices release their `nSTATUS` pins after a reset time-out period. When the `nSTATUS` pins are released and pulled high, the configuration device reconfigures the chain. If the *Auto-restart configuration after error* option is off, `nSTATUS` stays low until the Stratix and Stratix GX devices are reset with a low pulse on `nCONFIG`.

Figure 13–11 shows the FPP configuration with a configuration device timing waveform for Stratix and Stratix GX devices.

*Figure 13–11. FPP Configuration with a Configuration Device Timing Waveform* *Note (1)*



*Notes to Figure 13–11*

(1) For timing information, refer to the *Enhanced Configuration Devices (EPC4, EPC8 & EPC16) Data Sheet*.

(2) The configuration device drives `DATA` low after configuration.

(3) Stratix and Stratix GX devices enter user mode 136 clock cycles after `CONF_DONE` goes high.

### *Parallel Configuration Using a Microprocessor*

When using a microprocessor for parallel configuration, the microprocessor transfers data from a storage device to the Stratix or Stratix GX device through configuration hardware. To initiate configuration, the microprocessor needs to generate a low-to-high transition on the `nCONFIG` pin and the Stratix or Stratix GX device must release `nSTATUS`. The microprocessor then places the configuration data to the `DATA[7..0]` pins of the Stratix or Stratix GX device. Data is clocked continuously into the Stratix or Stratix GX device until `CONF_DONE` goes high.

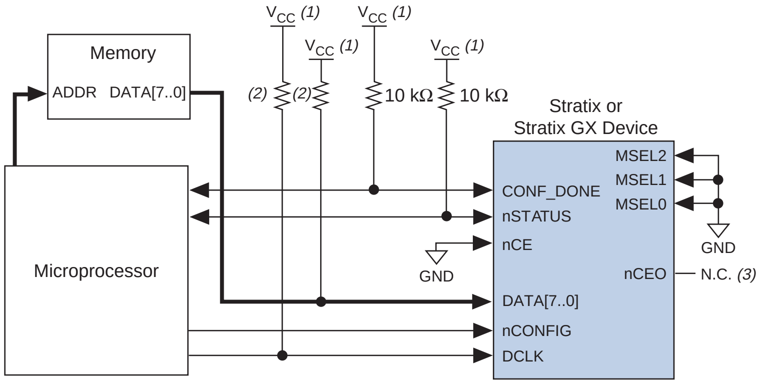
After all configuration data is sent to the Stratix or Stratix GX device, the `CONF_DONE` pin will go high to show successful configuration and the start of initialization. Initialization, by default, uses an internal oscillator, which runs at 10 MHz. If you are using the `clkusr` option, after all data is transferred `clkusr` must be clocked an additional 136 times for the Stratix or Stratix GX device to initialize properly. Driving `DCLK` to the device after configuration is complete does not affect device operation.

If the Stratix or Stratix GX device detects an error during configuration, it drives `nSTATUS` low to alert the microprocessor. The pin on the microprocessor connected to `nSTATUS` must be open drain. The microprocessor can then pulse `nCONFIG` low to restart the configuration error. With the *Auto-restart configuration after error* option on, the Stratix or Stratix GX device releases `nSTATUS` after a reset time-out period. After `nSTATUS` is released, the microprocessor can reconfigure the Stratix or Stratix GX device without pulsing `nCONFIG` low.

The microprocessor can also monitor the `CONF_DONE` and `INIT_DONE` pins to ensure successful configuration. If the microprocessor sends all the data and the initialization clock starts but `CONF_DONE` and `INIT_DONE` have not gone high, it must reconfigure the Stratix or Stratix GX device. After waiting the specified 136 `DCLK` cycles, the microprocessor should restart configuration by pulsing `nCONFIG` low.

Figure 13–12 shows the circuit for Stratix and Stratix GX parallel configuration using a microprocessor.

*Figure 13–12. Parallel Configuration Using a Microprocessor*



*Notes to Figure 13–12:*

(1) The pull-up resistors should be connected to any $V_{CC}$ that meets the Stratix high-level input voltage ($V_{IH}$) specification.

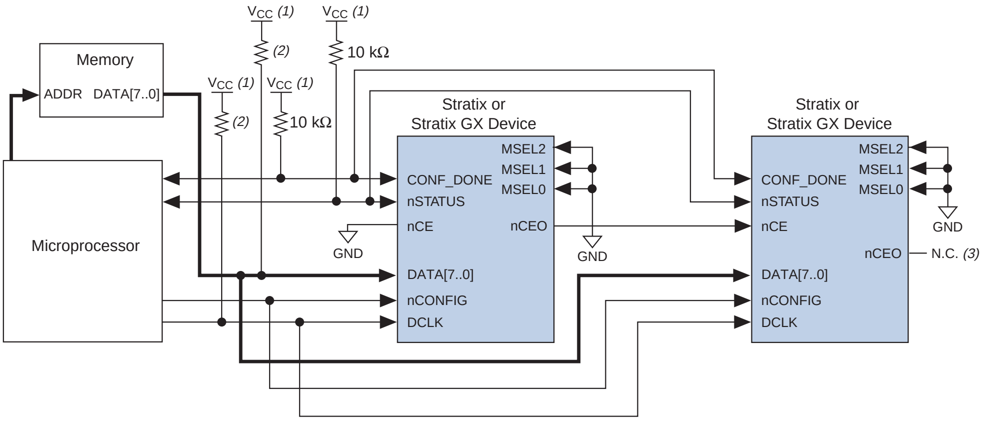
(2) These pull-up resistors are 1 kΩ.

(3) The `nCEO` pin is left unconnected.

For multi-device parallel configuration with a microprocessor, the `nCEO` pin of the first Stratix or Stratix GX device is cascaded to the second device's `nCE` pin. The second device in the chain begins configuration within one clock cycle; therefore, the transfer of data destinations is transparent to the microprocessor. Because the `CONF_DONE` pins of the devices are connected together, all devices initialize and enter user mode at the same time.

Because the `nSTATUS` pins are also tied together, if any of the devices detects an error, the entire chain halts configuration and drives `nSTATUS` low. The microprocessor can then pulse `nCONFIG` low to restart configuration. If the *Auto-restart configuration after error* option is on, the Stratix and Stratix GX devices release `nSTATUS` after a reset time-out period. The microprocessor can then reconfigure the devices once `nSTATUS` is released. Figure 13–13 shows multi-device configuration using a microprocessor. Figure 13–14 shows multi-device configuration when both Stratix and Stratix GX devices are receiving the same data. In this case, the microprocessor sends the data to both devices simultaneously, and the devices configure simultaneously.

### Figure 13–13. Parallel Data Transfer in Serial Configuration with a Microprocessor



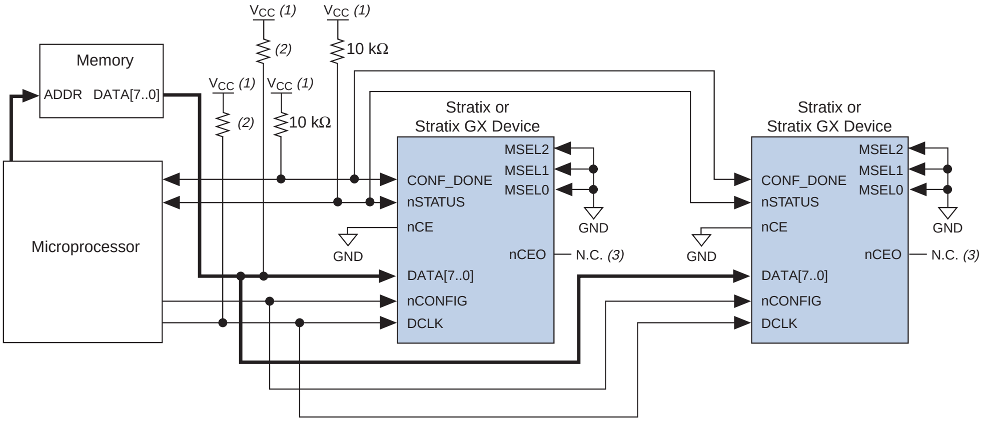
*Notes to* *Figure 13–13*:

(1) You should connect the pull-up resistors to any $V_{CC}$ that meets the Stratix high-level input voltage ($V_{IH}$) specification.

(2) These pull-up resistors are 1 kΩ.

(3) The `nCEO` pin of the last device is left unconnected.

### Figure 13–14. Multiple Device Parallel Configuration with the Same Data Using a Microprocessor



*Notes to* *Figure 13–14*:

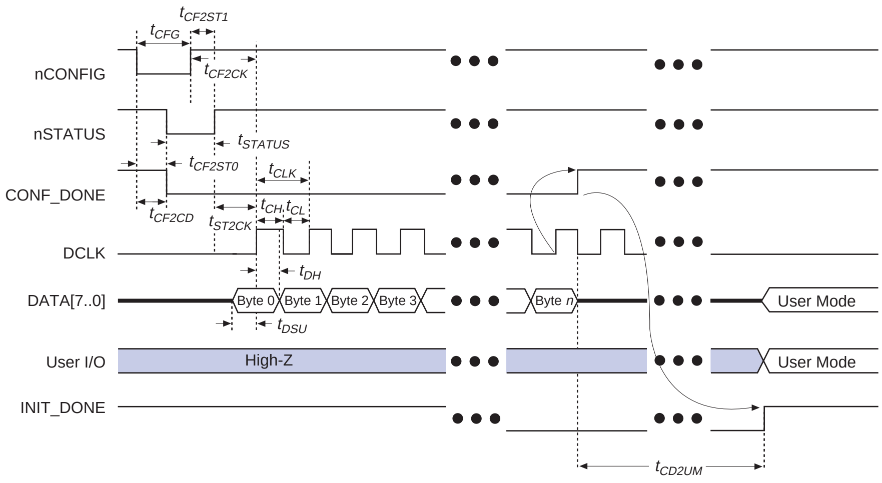
(1) You should connect the pull-up resistors to any $V_{CC}$ that meets the Stratix high-level input voltage ($V_{IH}$) specification.

(2) These pull up resistors are 1 kΩ.

(3) The `nCEO` pins are left unconnected when configuring the same data into multiple Stratix or Stratix GX devices.

Figure 13–15 shows FPP timing waveforms for configuring a Stratix or Stratix GX device in FPP mode. Table 13–9 shows the FPP timing parameters for Stratix or Stratix GX devices.

*Figure 13–15. Timing Waveform for Configuring Devices in FPP Mode*



| *Table 13–9. FPP Timing Parameters for Stratix & Stratix GX Devices (Part 1 of 2)* | | | | |
|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min** | **Max** | **Units** |
| $t_{CF2CK}$ | `nCONFIG` high to first rising edge on `DCLK` | 40 | | µs |
| $t_{DSU}$ | Data setup time before rising edge on `DCLK` | 7 | | ns |
| $t_{DH}$ | Data hold time after rising edge on `DCLK` | 0 | | ns |
| $t_{CFG}$ | `nCONFIG` low pulse width *(1)* | 40 | | µs |
| $t_{CH}$ | `DCLK` high time | 4 | | ns |
| $t_{CL}$ | `DCLK` low time | 4 | | ns |
| $t_{CLK}$ | `DCLK` period | 10 | | ns |
| $f_{MAX}$ | `DCLK` frequency | | 100 | MHz |
| $t_{CD2UM}$ | `CONF_DONE` high to user mode *(2)* | 6 | 20 | µs |
| $t_{CF2CD}$ | `nCONFIG` low to `CONF_DONE` low | | 800 | ns |
| $t_{CF2ST0}$ | `nCONFIG` low to `nSTATUS` low | | 800 | ns |
| $t_{CF2ST1}$ | `nCONFIG` high to `nSTATUS` high | | 40 *(3)* | µs |

*Table 13–9. FPP Timing Parameters for Stratix & Stratix GX Devices (Part 2 of 2)*

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $t_{STATUS}$ | `nSTATUS` low pulse width | 10 | 40 *(3)* | µs |
| $t_{ST2CK}$ | `nSTATUS` high to firstrising edge of `DCLK` | 1 | | µs |

*Notes to Table 13–9:*

(1) This value applies only if the internal oscillator is selected as the clock source for starting up the device. If the clock source is `CLKUSR` or `DCLK`, multiply the clock period by 270 to obtain this value.

(2) The minimum and maximum numbers apply only if the internal oscillator is chosen as the clock source for starting up the device. If the clock source is `CLKUSR` or `DCLK`, multiply the clock period by 140 to obtain this value.

(3) This value is obtainable if users do not delay configuration by extending the `nSTATUS` low pulse width.

## PPA Configuration

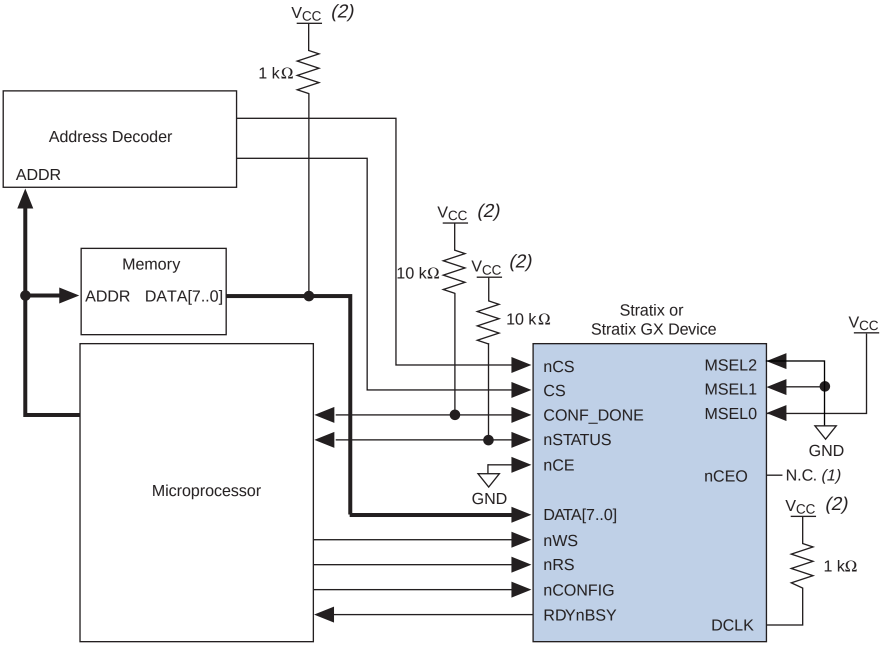
In PPA schemes, a microprocessor drives data to the Stratix or Stratix GX device through a download cable. When using a PPA scheme, use a 1-kΩ pull-up resistor to pull the `DCLK` pin high to prevent unused configuration pins from floating.

To begin configuration, the microprocessor drives `nCONFIG` high and then asserts the target device's `nCS` pin low and `CS` pin high. Next, the microprocessor places an 8-bit configuration word on the target device's data inputs and pulses `nWS` low. On the rising edge of `nWS`, the target device latches a byte of configuration data and then drives its `RDYnBSY` signal low, indicating that it is processing the byte of configuration data. The microprocessor then performs other system functions while the Stratix or Stratix GX device is processing the byte of configuration data.

Next, the microprocessor checks `nSTATUS` and `CONF_DONE`. If `nSTATUS` is high and `CONF_DONE` is low, the microprocessor sends the next data byte. If `nSTATUS` is low, the device is signaling an error and the microprocessor should restart configuration. However, if `nSTATUS` is high and all the configuration data is received, the device is ready for initialization. At the beginning of initialization, `CONF_DONE` goes high to indicate that configuration is complete.

Figure 13–16 shows the PPA configuration circuit. An optional address decoder controls the device's `nCS` and `CS` pins. This decoder allows the microprocessor to select the Stratix or Stratix GX device by accessing a particular address, simplifying the configuration process.

*Figure 13–16. PPA Configuration Circuit*



*Notes to Figure 13–16:*

(1) The `nCEO` pin is left unconnected.

(2) The pull-up resistor should be connected to the same supply voltage as the Stratix or Stratix GX device.

The device's `nCS` or `CS` pins can be toggled during PPA configuration if the design meets the specifications for $t_{CSSU}$, $t_{WSP}$, and $t_{CSH}$ given in Table 13–10 on page 13–31. The microprocessor can also directly control the `nCS` and `CS` signals. You can tie one of the `nCS` or `CS` signals to its active state (i.e., `nCS` may be tied low) and toggle the other signal to control configuration.

Stratix and Stratix GX devices can serialize data internally without the microprocessor. When the Stratix or Stratix GX device is ready for the next byte of configuration data, it drives `RDYnBSY` high. If the microprocessor senses a high signal when it polls `RDYnBSY`, the microprocessor strobes the next byte of configuration data into the device. Alternatively, the `nRS` signal can be strobed, causing the `RDYnBSY` signal to appear on `DATA7`. Because `RDYnBSY` does not need to be monitored, reading the state of the configuration data by strobing nRS low saves a system I/O port. Do not drive data onto the data bus while `nRS` is low because it causes contention on `DATA7`. If the `nRS` pin is not used to monitor configuration, you should tie it high. To simplify configuration, the microprocessor can wait for the total time of $t_{BUSY}$ (max) + $t_{RDY2WS}$ + $t_{W2SB}$ before sending the next data bit.

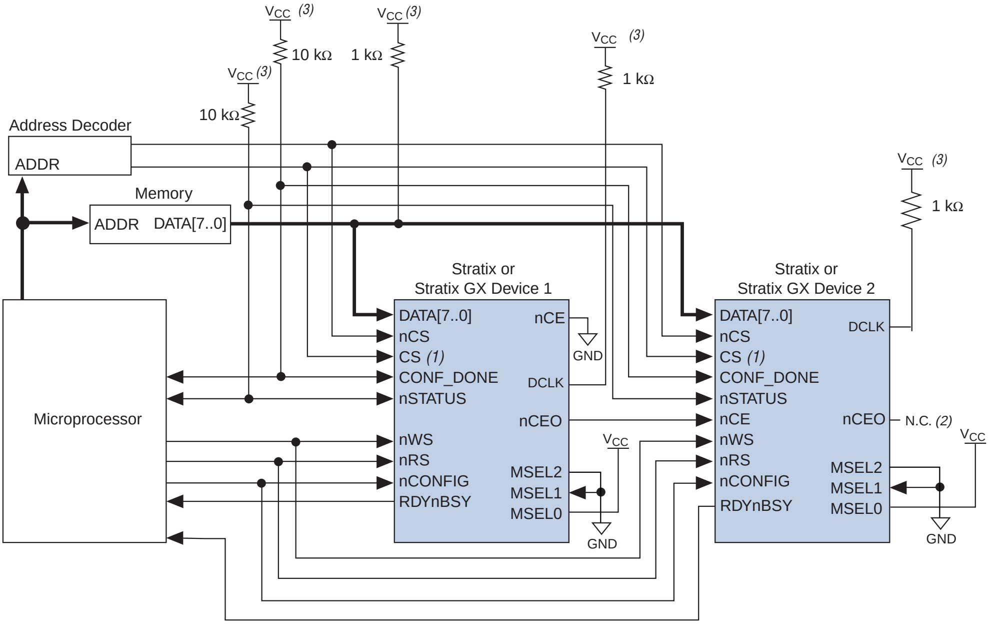
After configuration, the `nCS`, `CS`, `nRS`, `nWS`, and `RDYnBSY` pins act as user I/O pins. However, if the PPA scheme is chosen in the Quartus II software, these I/O pins are tri-stated by default in user mode and should be driven by the microprocessor. To change the default settings in the Quartus II software, select **Device & Pin Option** (Compiler Setting menu).

If the Stratix or Stratix GX device detects an error during configuration, it drives `nSTATUS` low to alert the microprocessor. The microprocessor can then pulse `nCONFIG` low to restart the configuration process. Alternatively, if the *Auto-Restart Configuration on Frame Error* option is turned on, the Stratix or Stratix GX device releases `nSTATUS` after a reset time-out period. After `nSTATUS` is released, the microprocessor can reconfigure the Stratix or Stratix GX device. At this point, the microprocessor does not need to pulse `nCONFIG` low.

The microprocessor can also monitor the `CONF_DONE` and `INIT_DONE` pins to ensure successful configuration. The microprocessor must monitor the `CONF_DONE` pin to detect errors and determine when programming completes. If the microprocessor sends all configuration data and starts initialization but `CONF_DONE` is not asserted, the microprocessor must reconfigure the Stratix or Stratix GX device.

You can also use PPA mode to configure multiple Stratix and Stratix GX devices. Multi-device PPA configuration is similar to single-device PPA configuration, except that the Stratix and Stratix GX devices are cascaded. After you configure the first Stratix or Stratix GX device, `nCEO` is asserted, which asserts the `nCE` pin on the second device, initiating configuration. Because the second Stratix or Stratix GX device begins configuration within one write cycle of the first device, the transfer of data destinations is transparent to the microprocessor. All Stratix and Stratix GX device `CONF_DONE` pins are tied together; therefore, all devices initialize and enter user mode at the same time. See Figure 13–17.

*Figure 13–17. PPA Multi-Device Configuration Circuit*



*Notes to Figure 13–17:*

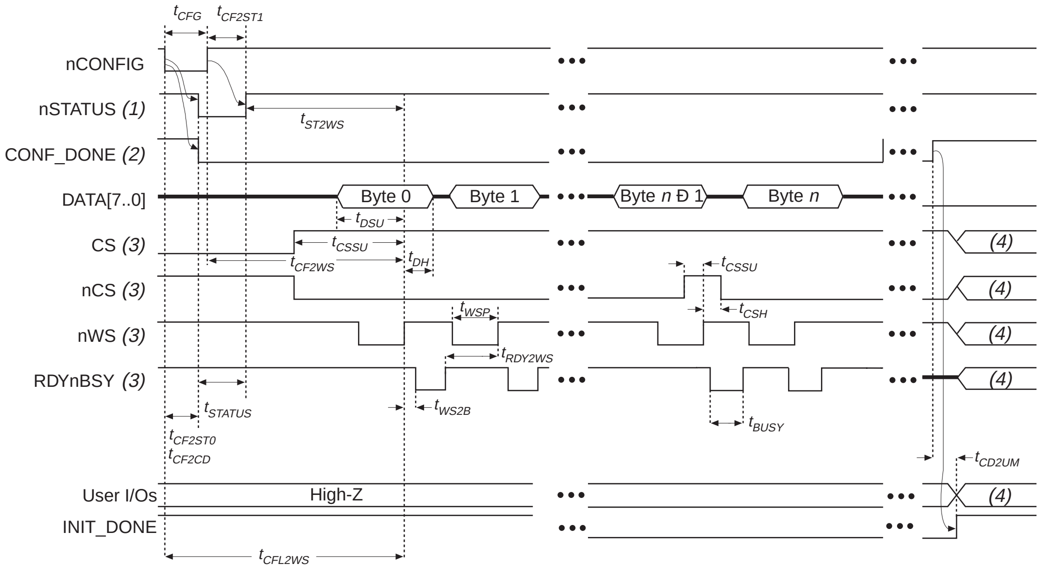
(1) If not used, you can connect the `CS` pin to $V_{CC}$ directly.

(2) The `nCEO` pin is left unconnected for the last device in the chain.

(3) Connect the pull-up resistor to the same supply voltage as the Stratix or Stratix GX device.

Figure 13–18 shows the Stratix and Stratix GX device timing waveforms for PPA configuration.

*Figure 13–18. PPA Timing Waveforms for Stratix & Stratix GX Devices*



*Notes to Figure 13–18:*

(1) Upon power-up, nSTATUS is held low not more than 5 µs when $V_{CC}$ reaches its minimum requirement.

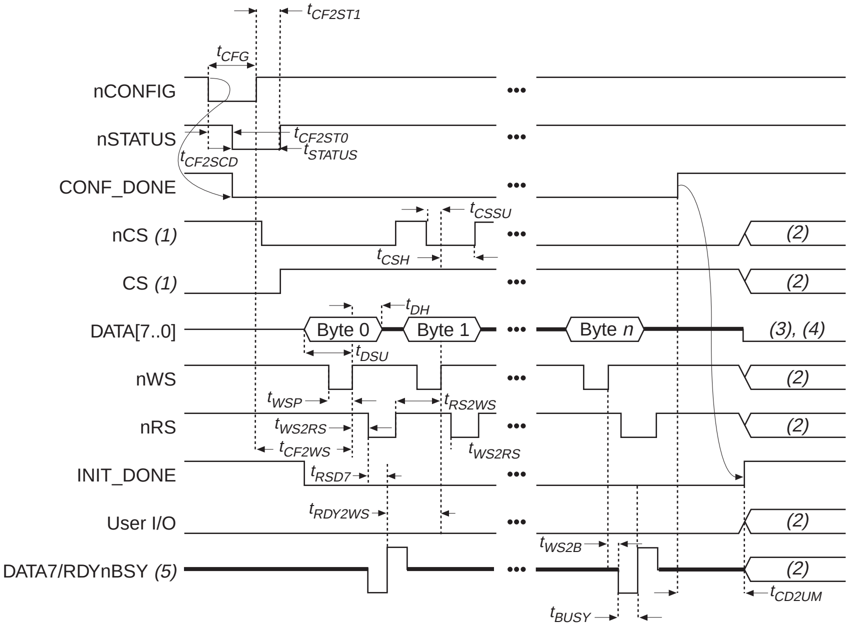
(2) Upon power-up, CONF_DONE is low.

(3) After configuration, the state of CS, nCS, nWS, and RDYnBSY depends on the design programmed into the Stratix or Stratix GX device.

(4) Device I/O pins are in user mode.

Figure 13–19 shows the Stratix and Stratix GX timing waveforms when using strobed nRS and nWS signals.

*Figure 13–19. PPA Timing Waveforms Using Strobed nRS & nWS Signals*



*Notes to Figure 13–19:*

(1) The user can toggle `nCS` or `CS` during configuration if the design meets the specification for $t_{CSSU}$, $t_{WSP}$, and $t_{CSH}$.
(2) Device I/O pins are in user mode.
(3) Do not leave `DATA0` floating. Drive it high or low, whichever is more convenient.
(4) Only the `DATA[7..1]` pins are I/O pins during user mode. `DATA0` is only input in user mode.
(5) `DATA7` is a bidirectional pin. It represents an input for data input, but represents an output to show the status of `RDYnBSY`.

Table 13–10 defines the Stratix and Stratix GX timing parameters for PPA configuration

*Table 13–10. PPA Timing Parameters for Stratix & Stratix GX Devices (Part 1 of 2)*

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $t_{CF2WS}$ | `nCONFIG` high to first rising edge on `nWS` | 40 | | µs |
| $t_{DSU}$ | Data setup time before rising edge on `nWS` | 10 | | ns |
| $t_{DH}$ | Data hold time after rising edge on `nWS` | 0 | | ns |
| $t_{CSSU}$ | Chip select setup time before rising edge on `nWS` | 10 | | ns |
| $t_{CSH}$ | Chip select hold time after rising edge on `nWS` | 0 | | ns |
| $t_{WSP}$ | `nWS` low pulse width | 15 | | ns |

*Table 13–10. PPA Timing Parameters for Stratix & Stratix GX Devices (Part 2 of 2)*

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $t_{CFG}$ | `nCONFIG` low pulse width *(1)* | 40 | | µs |
| $t_{WS2B}$ | `nWS` rising edge to `RDYnBSY` low | | 20 | ns |
| $t_{BUSY}$ | `RDYnBSY` low pulse width | 7 | 45 | ns |
| $t_{RDY2WS}$ | `RDYnBSY` rising edge to `nWS` rising edge | 15 | | ns |
| $t_{WS2RS}$ | `nWS` rising edge to `nRS` falling edge | 15 | | ns |
| $t_{RS2WS}$ | `nRS` rising edge to `nWS` rising edge | 15 | | ns |
| $t_{RSD7}$ | `nRS` falling edge to `DATA7` valid with `RDYnBSY` signal | | 20 | ns |
| $t_{CD2UM}$ | `CONF_DONE` high to user mode *(2)* | 6 | 20 | µs |
| $t_{STATUS}$ | `nSTATUS` low pulse width | 10 | 40 *(3)* | µs |
| $t_{CF2CD}$ | `nCONFIG` low to `CONF_DONE` low | | 800 | ns |
| $t_{CF2ST0}$ | `nCONFIG` low to `nSTATUS` low | | 800 | ns |
| $t_{CF2ST1}$ | `nCONFIG` high to `nSTATUS` high | | 40 *(3)* | µs |

*Notes to Table 13–10:*

(1) This value applies only if the internal oscillator is selected as the clock source for starting up the device. If the clock source is `clkusr` or `dclk`, multiply the clock period by 270 to obtain this value.

(2) The minimum and maximum numbers apply only if the internal oscillator is chosen as the clock source for starting up the device. If the clock source is `CLKUSR` or `DCLK`, multiply the clock period by 140 to obtain this value.

(3) This value is obtained if you do not delay configuration by extending the `nstatus` to low pulse width.

For information on how to create configuration and programming files for this configuration scheme, see "Device Configuration Files" on page 13–57.

## JTAG Programming & Configuration

The JTAG has developed a specification for boundary-scan testing. This boundary-scan test (BST) architecture offers the capability to efficiently test components on printed circuit boards (PCBs) with tight lead spacing. The BST architecture can test pin connections without using physical test probes and capture functional data while a device is operating normally. You can also use the JTAG circuitry to shift configuration data into the device.

For more information on JTAG boundary-scan testing, see *AN 39: IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices*.

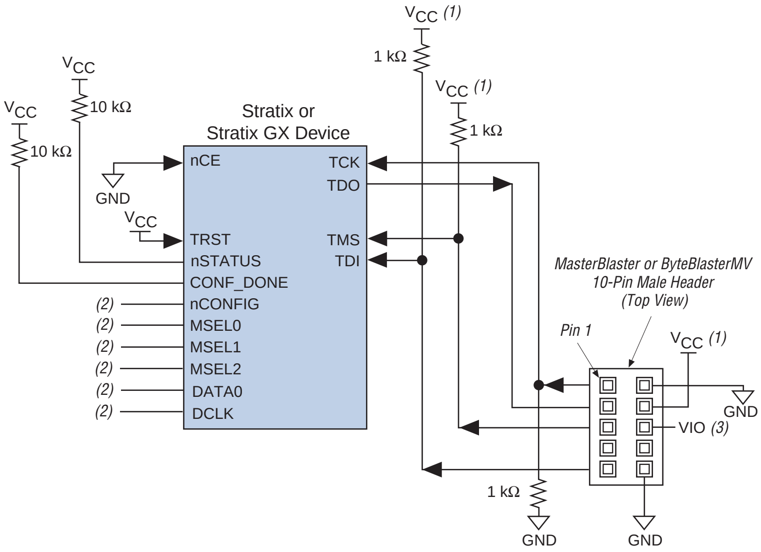
A device operating in JTAG mode uses four required pins, TDI, TDO, TMS, and TCK, and one optional pin, TRST. All other pins are tri-stated during JTAG configuration. Do not begin JTAG configuration until all other configuration is complete. Table 13–11 shows each JTAG pin's function.

*Table 13–11. JTAG Pin Descriptions*

| Pin | Description | Function |
|---|---|---|
| TDI | Test data input | Serial input pin for instructions as well as test and programming data. Data is shifted in on the rising edge of `TCK`. |
| TDO | Test data output | Serial data output pin for instructions as well as test and programming data. Data is shifted out on the falling edge of `TCK`. The pin is tri-stated if data is not being shifted out of the device. |
| TMS | Test mode select | Input pin that provides the control signal to determine the transitions of the Test Access Port (TAP) controller state machine. Transitions within the state machine occur on the rising edge of `TCK`. Therefore, `TMS` must be set up before the rising edge of `TCK`. `TMS` is evaluated on the rising edge of `TCK`. |
| TCK | Test clock input | The clock input to the BST circuitry. Some operations occur at the rising edge, while others occur at the falling edge. |
| TRST | Test reset input (optional) | Active-low input to asynchronously reset the boundary-scan circuit. The `TRST` pin is optional according to IEEE Std. 1149.1. |

During JTAG configuration, data is downloaded to the device on the PCB through the MasterBlaster or ByteBlasterMV header. Configuring devices through a cable is similar to programming devices in-system. One difference is to connect the `TRST` pin to $V_{CC}$ to ensure that the TAP controller is not reset. See Figure 13–20.

*Figure 13–20. JTAG Configuration of a Single Device*



***Notes to Figure 13–20:***

(1) You should connect the pull-up resistor to the same supply voltage as the download cable.

(2) You should connect the `nCONFIG`, `MSEL0`, and `MSEL1` pins to support a non-JTAG configuration scheme. If you only use JTAG configuration, connect `nCONFIG` to $V_{CC}$, and `MSEL0`, `MSEL1`, and `MSEL2` to ground. Pull `DATA0` and `DCLK` to high or low.

(3) $V_{IO}$ is a reference voltage for the MasterBlaster output driver. $V_{IO}$ should match the device's $V_{CCIO}$. Refer to the *MasterBlaster Serial/USB Communications Cable Data Sheet* for this value.

To configure a single device in a JTAG chain, the programming software places all other devices in BYPASS mode. In BYPASS mode, devices pass programming data from the `TDI` pin to the `TDO` pin through a single bypass register without being affected internally. This scheme enables the programming software to program or verify the target device. Configuration data driven into the device appears on the `TDO` pin one clock cycle later.

Stratix and Stratix GX devices have dedicated JTAG pins. You can perform JTAG testing on Stratix and Stratix GX devices before and after, but not during configuration. The chip-wide reset and output enable pins on Stratix and Stratix GX devices do not affect JTAG boundary-scan or programming operations. Toggling these pins does not affect JTAG operations (other than the usual boundary-scan operation).

When designing a board for JTAG configuration of Stratix and Stratix GX devices, you should consider the regular configuration pins. Table 13–12 shows how you should connect these pins during JTAG configuration.

*Table 13–12. JTAG Termination of Unused Pins*

| Signal | Description |
|---|---|
| `nCE` | Drive all Stratix and Stratix GX devices in the chain low by connecting `nCE` to ground, pulling it down via a resistor, or driving it by some control circuitry. |
| `nSTATUS` | Pulled to $V_{CC}$ through a 1-kΩ resistor. When configuring multiple devices in the same JTAG chain, pull up each `nSTATUS` pin to $V_{CC}$ individually. *(1)* |
| `CONF_DONE` | Pulled to $V_{CC}$ through a 1-kΩ resistor. When configuring multiple devices in the same JTAG chain, pull up each `CONF_DONE` pin to $V_{CC}$ individually. *(1)* |
| `nCONFIG` | Driven high by connecting to $V_{CC}$, pulling up through a resistor, or driven by some control circuitry. |
| `MSEL0`,<br>`MSEL1`,<br>`MSEL2` | Do not leave these pins floating. These pins support whichever non-JTAG configuration is used in production. If only JTAG configuration is used, you should tie these pins to ground. |
| `DCLK` | Do not leave these pins floating. Drive low or high, whichever is more convenient. |
| `DATA0` | Do not leave these pins floating. Drive low or high, whichever is more convenient. |
| `TRST` | This JTAG pin is not connected to the download cable. Drive this pin to logic high. |

***Note to Table 13–12:***

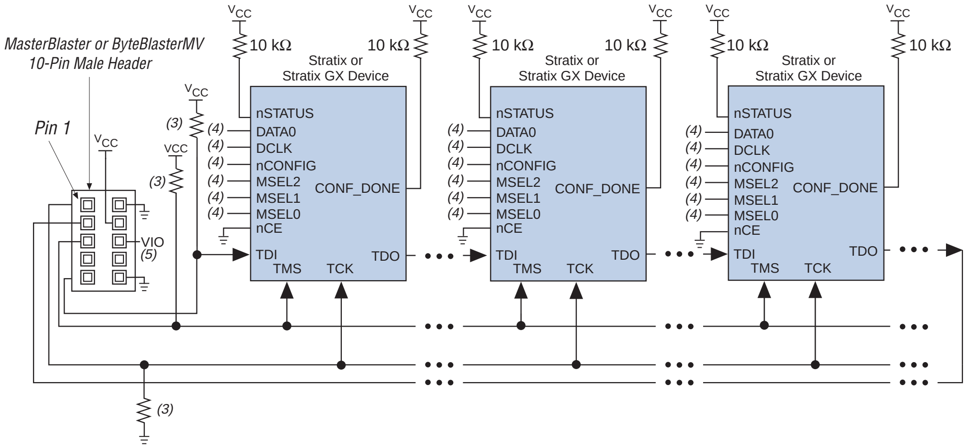
(1) `nSTATUS` must be driven high throughout JTAG configuration. You can drive `nSTATUS` high by connecting it directly to $V_{CC}$ through a pull-up resistor or by control circuitry.

## JTAG Programming & Configuration of Multiple Devices

When programming a JTAG device chain, one JTAG-compatible header, such as the ByteBlasterMV header, is connected to several devices. The number of devices in the JTAG chain is limited only by the drive capacity of the download cable. However, when more than five devices are connected in a JTAG chain, Altera recommends buffering the `TCK`, `TDI`, and `TMS` pins with an on-board buffer.

JTAG-chain device programming is ideal when the PCB contains multiple devices, or when testing the PCB using JTAG BST circuitry. Figure 13–21 shows multi-device JTAG configuration.

**Figure 13–21. Multi-Device JTAG Configuration** Notes (1), (2)



*Notes to Figure 13–21:*

(1) Stratix, Stratix GX, APEX™ II, APEX 20K, Mercury™, ACEX® 1K, and FLEX® 10K devices can be placed within the same JTAG chain for device programming and configuration.

(2) For more information on all configuration pins connected in this mode, refer to Table 13–11 on page 13–33.

(3) These pull-up/pull-down resistors are 1 kΩ.

(4) Connect the `nCONFIG`, `MSEL0`, `MSEL1`, and `MSEL2` pins to support a non-JTAG configuration scheme. If only JTAG configuration is used, connect `nCONFIG` to $V_{CC}$, and `MSEL0`, `MSEL1`, and `MSEL2` to ground. Pull `DATA0` and `DCLK` to either high or low.

(5) $V_{IO}$ is a reference voltage for the MasterBlaster output driver. $V_{IO}$ should match the device's $V_{CCIO}$. Refer to the *MasterBlaster Serial/USB Communications Cable Data Sheet* for this value.

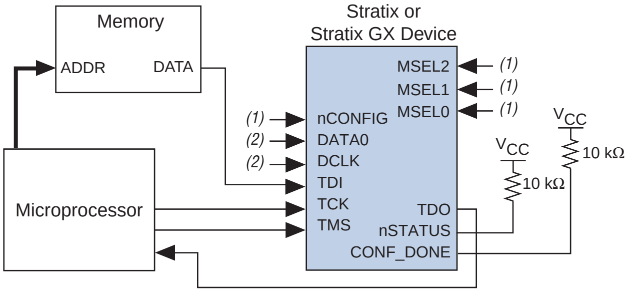
The Quartus II software verifies successful JTAG configuration upon completion. The software checks the state of `CONF_DONE` through the JTAG port. If `CONF_DONE` is not in the correct state, the Quartus II software indicates that configuration has failed. If `CONF_DONE` is in the correct state, the software indicates that configuration was successful.

If `VCCIO` is tied to 3.3 V, both the I/O pins and JTAG `TDO` port drive at 3.3-V levels.

Do not attempt JTAG and non-JTAG configuration simultaneously. When configuring through JTAG, allow any non-JTAG configuration to complete first.

Figure 13–22 shows the JTAG configuration of a Stratix or Stratix GX device with a microprocessor.

*Figure 13–22. JTAG Configuration of Stratix & Stratix GX Devices with a Microprocessor*



*Notes to Figure 13–22:*

(1) Connect the `nCONFIG`, `MSEL2`, `MSEL1`, and `MSEL0` pins to support a non-JTAG configuration scheme. If your design only uses JTAG configuration, connect the `nCONFIG` pin to $V_{CC}$ and the `MSEL2`, `MSEL1`, and `MSEL0` pins to ground.

(2) Pull `DATA0` and `DCLK` to either high or low.

## Configuration with JRunner Software Driver

JRunner is a software deriver that allows you to configure Altera FPGAs through the ByteBlasterMV download cable in JTAG mode. The programming input file supported is in Raw Binary File (**.rbf**) format. JRunner also requires a Chain Description File (**.cdf**) generated by the Quartus II software. JRunner is targeted for embedded JTAG configuration. The source code has been developed for the Windows NT operating system. You can customize the code to make it run on other platforms.

For more information on the JRunner software driver, refer to the *JRunner Software Driver: An Embedded Solution to the JTAG Configuration White Paper* and zip file.

## Jam STAPL Programming & Test Language

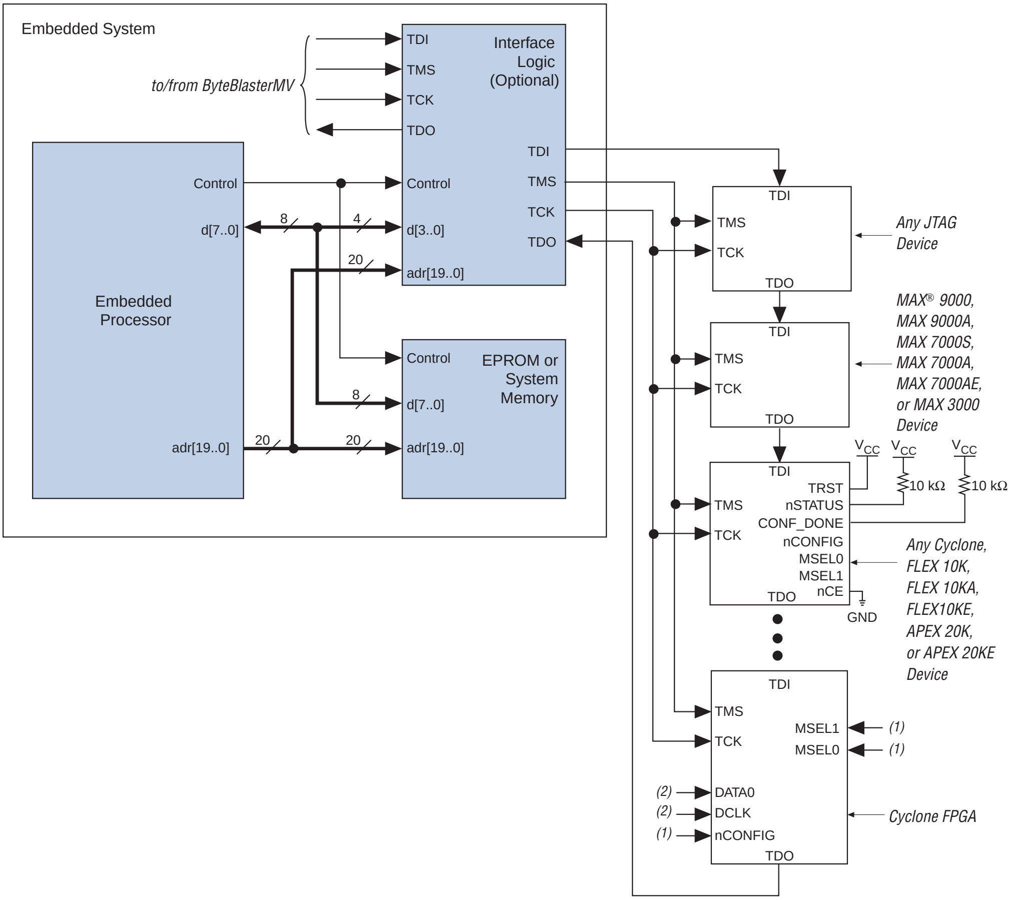
The Jam™ Standard Test and Programming Language (STAPL), JEDEC standard JESD-71, is a standard file format for in-system programmability (ISP) purposes. Jam STAPL supports programming or configuration of programmable devices and testing of electronic systems, using the IEEE 1149.1 JTAG interface. Jam STAPL is a freely licensed open standard.

### *Connecting the JTAG Chain to the Embedded Processor*

There are two ways to connect the JTAG chain to the embedded processor. The most straightforward method is to connect the embedded processor directly to the JTAG chain. In this method, four of the processor pins are dedicated to the JTAG interface, saving board space but reducing the number of available embedded processor pins.

Figure 13–23 illustrates the second method, which is to connect the JTAG chain to an existing bus through an interface PLD. In this method, the JTAG chain becomes an address on the existing bus. The processor then reads from or writes to the address representing the JTAG chain.

*Figure 13–23. Embedded System Block Diagram*



*Notes to Figure 13–23:*

(1) Connect the `nCONFIG`, `MSEL2`, `MSEL1`, and `MSEL0` pins to support a non-JTAG configuration scheme. If your design only uses JTAG configuration, connect the `nCONFIG` pin to $V_{CC}$ and the `MSEL2`, `MSEL1`, and `MSEL0` pins to ground.

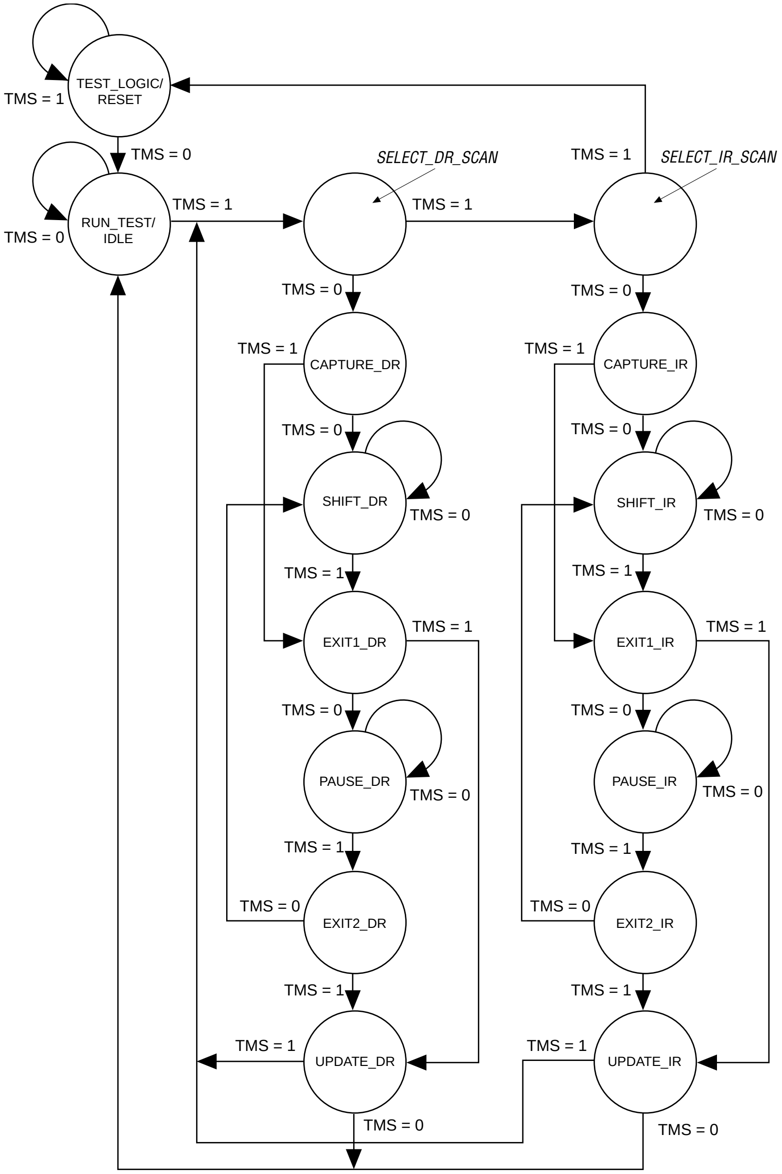
(2) Pull `DATA0` and `DCLK` to either high or low.

Both JTAG connection methods should include space for the MasterBlaster or ByteBlasterMV header connection. The header is useful during prototyping because it allows you to verify or modify the Stratix or Stratix GX device's contents. During production, you can remove the header to save cost.

### *Program Flow*

The Jam Player provides an interface for manipulating the IEEE Std. 1149.1 JTAG TAP state machine. The TAP controller is a 16-state state machine that is clocked on the rising edge of `TCK`, and uses the `TMS` pin to control JTAG operation in a device. Figure 13–24 shows the flow of an IEEE Std. 1149.1 TAP controller state machine.

*Figure 13–24. JTAG TAP Controller State Machine*



While the Jam Player provides a driver that manipulates the TAP controller, the Jam Byte-Code File (**.jbc**) provides the high-level intelligence needed to program a given device. All Jam instructions that send JTAG data to the device involve moving the TAP controller through either the data register leg or the instruction register leg of the state machine. For example, loading a JTAG instruction involves moving the TAP controller to the `SHIFT_IR` state and shifting the instruction into the instruction register through the `TDI` pin. Next, the TAP controller is moved to the `RUN_TEST/IDLE` state where a delay is implemented to allow the instruction time to be latched. This process is identical for data register scans, except that the data register leg of the state machine is traversed.

The high-level Jam instructions are the `DRSCAN` instruction for scanning the JTAG data register, the `IRSCAN` instruction for scanning the instruction register, and the `WAIT` command that causes the state machine to sit idle for a specified period of time. Each leg of the TAP controller is scanned repeatedly, according to instructions in the JBC file, until all of the target devices are programmed.

Figure 13–25 illustrates the functional behavior of the Jam Player when it parses the JBC file. When the Jam Player encounters a `DRSCAN`, `IRSCAN`, or `WAIT` instruction, it generates the proper data on `TCK`, `TMS`, and `TDI` to complete the instruction. The flow diagram shows branches for the `DRSCAN`, `IRSCAN`, and `WAIT` instructions. Although the Jam Player supports other instructions, they are omitted from the flow diagram for simplicity.

*Figure 13–25. Jam Player Flow Diagram (Part 1 of 2)*

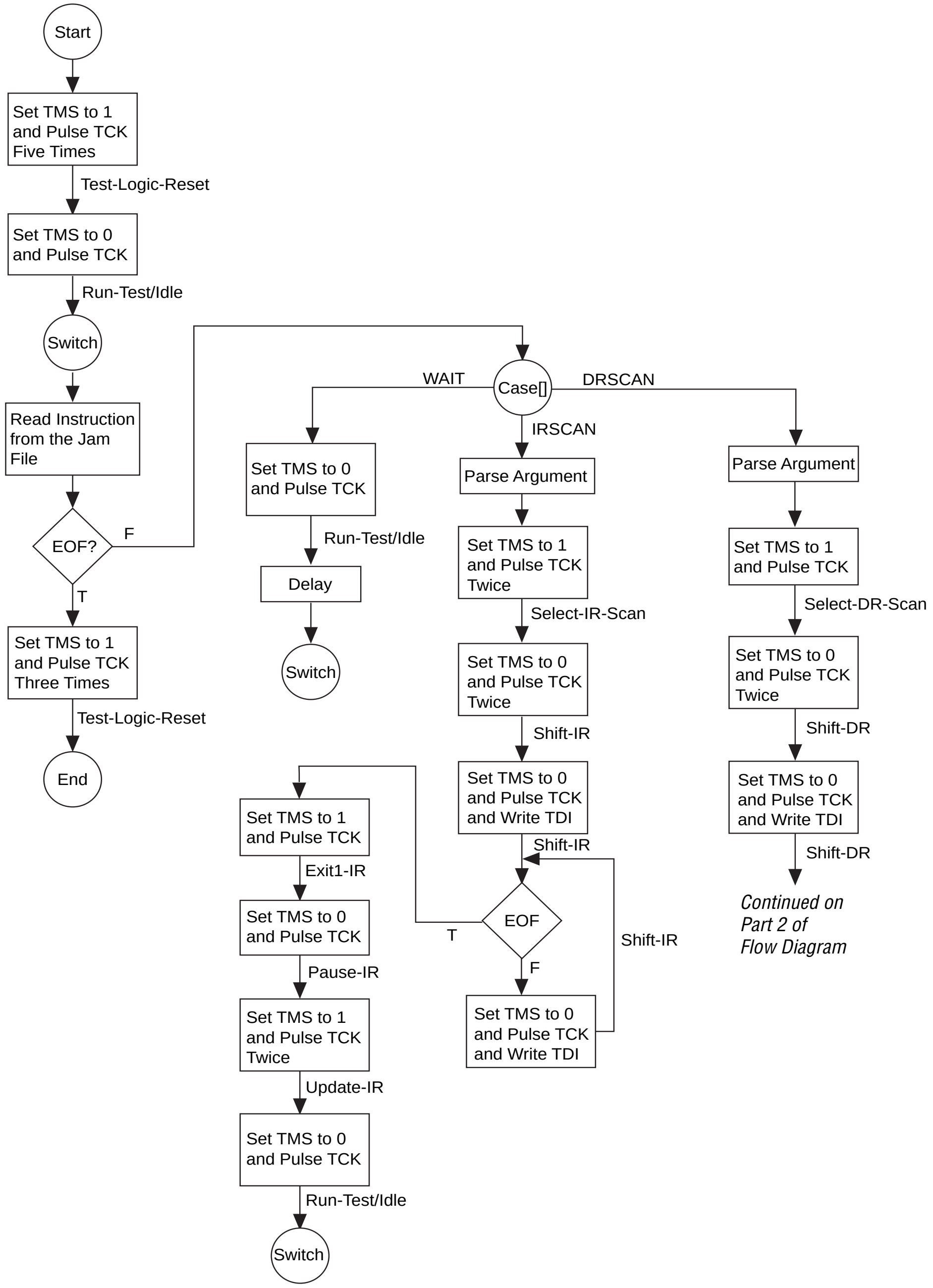
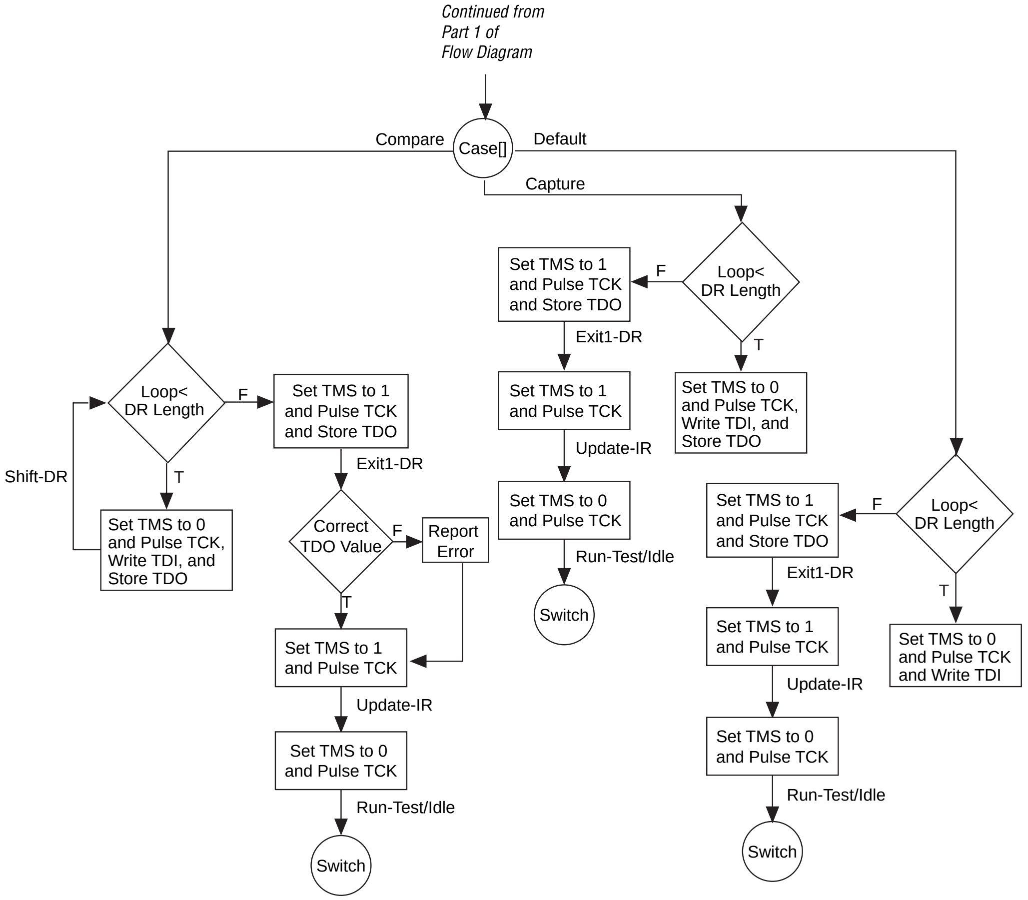


*Figure 13–26. Jam Player Flow Diagram (Part 2 of 2)*



Execution of a Jam program starts at the beginning of the program. The program flow is controlled using `GOTO`, `CALL/RETURN`, and `FOR/NEXT` structures. The `GOTO` and `CALL` statements refer to labels that are symbolic names for program statements located elsewhere in the Jam program. The language itself enforces almost no constraints on the organizational structure or control flow of a program.

☞ The Jam language does not support linking multiple Jam programs together or including the contents of another file into a Jam program.

### Jam Instructions

Each Jam statement begins with one of the instruction names listed in Table 13–13. The instruction names, including the names of the optional instructions, are reserved keywords that you cannot use as variable or label identifiers in a Jam program.

**Table 13–13. Instruction Names**

| | | |
|---|---|---|
| `BOOLEAN` | `INTEGER` | `PREIR` |
| `CALL` | `IRSCAN` | `PRINT` |
| `CRC` | `IRSTOP` | `PUSH` |
| `DRSCAN` | `LET` | `RETURN` |
| `DRSTOP` | `NEXT` | `STATE` |
| `EXIT` | `NOTE` | `WAIT` |
| `EXPORT` | `POP` | `VECTOR` *(1)* |
| `FOR` | `POSTDR` | `VMAP` *(1)* |
| `GOTO` | `POSTIR` | – |
| `IF` | `PREDR` | – |

***Note to Table 13–13:***

(1) This instruction name is an optional language extension.

Table 13–14 shows the state names that are reserved keywords in the Jam language. These keywords correspond to the state names specified in the IEEE Std. 1149.1 JTAG specification.

**Table 13–14. Reserved Keywords (Part 1 of 2)**

| IEEE Std. 1149.1 JTAG State Names | Jam Reserved State Names |
|---|---|
| `Test-Logic-Reset` | `RESET` |
| `Run-Test-Idle` | `IDLE` |
| `Select-DR-Scan` | `DRSELECT` |
| `Capture-DR` | `DRCAPTURE` |
| `Shift-DR` | `DRSHIFT` |
| `Exit1-DR` | `DREXIT1` |
| `Pause-DR` | `DRPAUSE` |
| `Exit2-DR` | `DREXIT2` |
| `Update-DR` | `DRUPDATE` |
| `Select-IR-Scan` | `IRSELECT` |

*Table 13–14. Reserved Keywords (Part 2 of 2)*

| IEEE Std. 1149.1 JTAG State Names | Jam Reserved State Names |
|---|---|
| `Capture-IR` | `IRCAPTURE` |
| `Shift-IR` | `IRSHIFT` |
| `Exit1-IR` | `IREXIT1` |
| `Pause-IR` | `IRPAUSE` |
| `Exit2-IR` | `IREXIT2` |
| `Update-IR` | `IRUPDATE` |

## *Example Jam File that Reads the IDCODE*

Figure 13–27 illustrates the flexibility and utility of the Jam STAPL. The example reads the IDCODE out of a single device in a JTAG chain.

☞ The array variable, `I_IDCODE`, is initialized with the IDCODE instruction bits ordered the LSB first (on the left) to most significant bit (MSB) (on the right). This order is important because the array field in the IRSCAN instruction is always interpreted, and sent, MSB to LSB.

*Figure 13–27. Example Jam File Reading IDCODE*

```
BOOLEAN read_data[32];
BOOLEAN I_IDCODE[10] = BIN 1001101000; ‘assumed
BOOLEAN ONES_DATA[32] = HEX FFFFFFFF;
INTEGER i;
‘Set up stop state for IRSCAN
IRSTOP IRPAUSE;
‘Initialize device
STATE RESET;
IRSCAN 10, I_IDCODE[0..9]; ‘LOAD IDCODE INSTRUCTION
STATE IDLE;
WAIT 5 USEC, 3 CYCLES;
DRSCAN 32, ONES_DATA[0..31], CAPTURE
read_data[0..31];
‘CAPTURE IDCODE
PRINT “IDCODE:”;
FOR i=0 to 31;
PRINT read_data[i];
NEXT i;
EXIT 0;
```

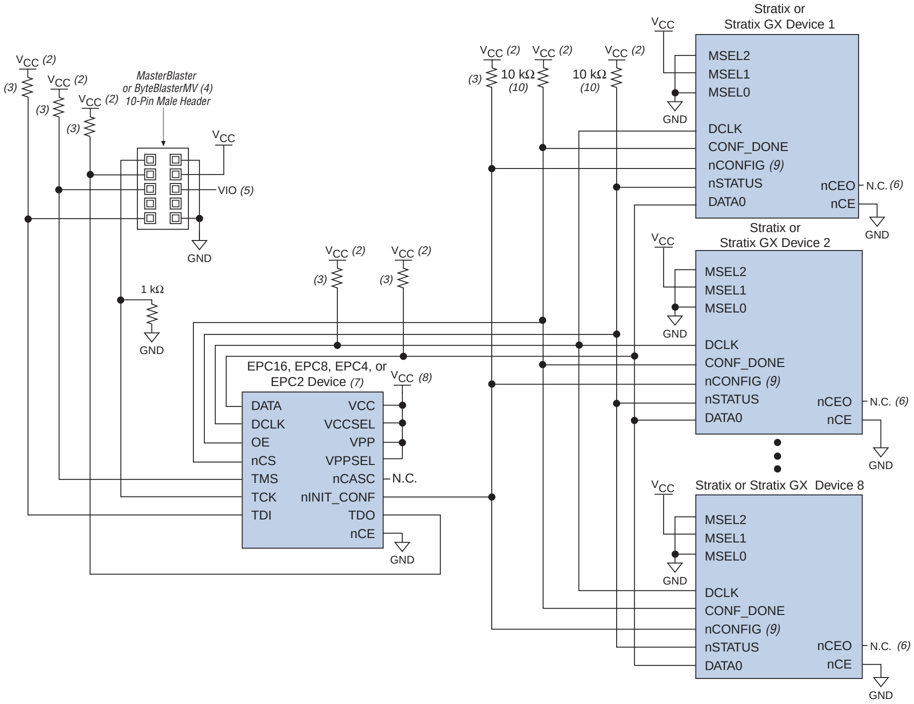
## Configuring Using the MicroBlaster Driver

The MicroBlaster™ software driver allows you to configure Altera's PLDs through the ByteBlasterMV cable in PS mode. The MicroBlaster software driver supports a Raw Binary File (**.rbf**) programming input file and is targeted for embedded passive serial configuration. The source code is developed for the Windows NT operating system, although you can customize it to run on other operating systems. For more information on the MicroBlaster software driver, go to the Altera web site (**http://www.altera.com**).

## Combining Configuration Schemes

This section shows you how to configure Stratix and Stratix GX devices using multiple configuration schemes on the same board (without using Jam STAPL). Figure 13–28 shows a setup to program the configuration device with JTAG and then configure multiple devices with the same configuration file.

**Figure 13–28. Device Configuration with a Download Cable & Configuration Device** *Note (1)*



*Notes to Figure 13–28:*

(1) Eight Stratix and Stratix GX devices are simultaneously configured with the same data.

(2) Connect $V_{CC}$ to the same supply voltage as the configuration device.

(3) These pull-up resistors are 1 kΩ. The `OE`, `nCS` and `nINIT_CONF` pins on EPC16, EPC8, EPC4, and EPC2 devices have internal user-configurable pull-up resistors. If you use internal pull-up resistors, do not use external pull-up resistors on these pins.

(4) The download cable programs the configuration device (EPC16, EPC8, EPC4, or EPC2 device).

(5) $V_{IO}$ is a reference voltage for the MasterBlaster output driver. $V_{IO}$ should match the device's $V_{CCIO}$. Refer to the *MasterBlaster Serial/USB Communications Cable Data Sheet* for this value.

(6) The `nCEO` pin is left unconnected for single-device configuration.

(7) The configuration device configures the Stratix or Stratix GX device. Figure 13–28 shows the pin connections for an EPC16, EPC8, EPC4, or EPC2 configuration device. For any other configuration device, connect the pins appropriately.

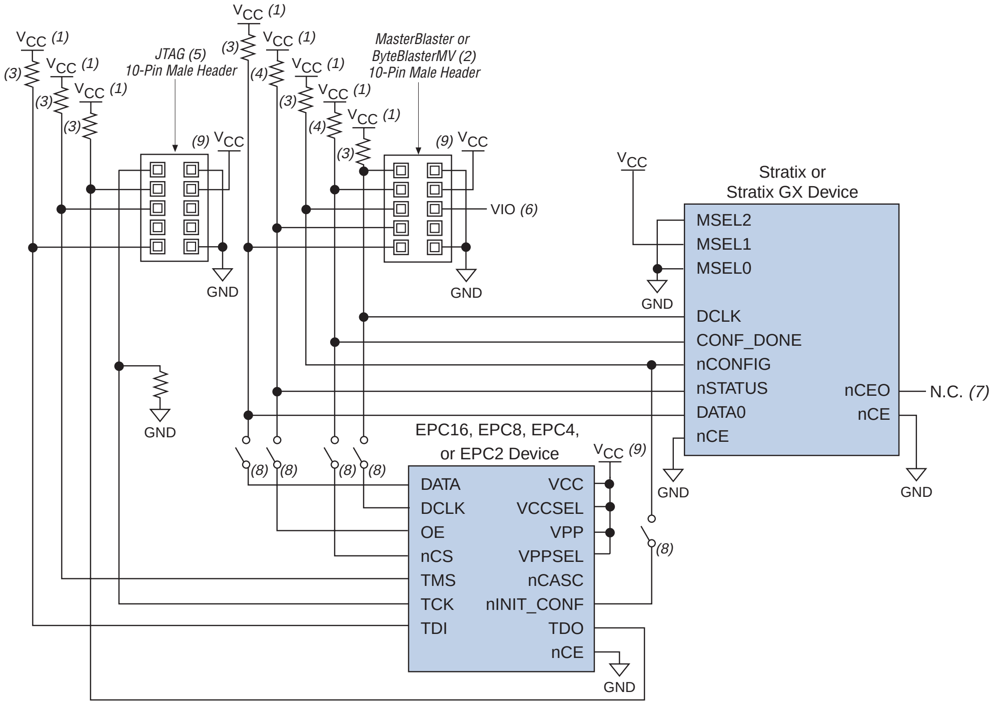
(8) If a 3.3-V supply voltage is used, connect the `VCC`, `VCCSEL`, `VPP`, and `VPPSEL` pins to a 3.3-V supply. If a 5.0-V supply voltage is used, connect the `VCC` and `VPP` pins to a 5.0-V supply, and connect the `VCCSEL` and `VPPSEL` pins to ground. To improve in-system programming times, you can connect `VPP` to 5.0 V, `VCC` to 3.3 V, and `VPPSEL` to ground. For more information on these pins, see Section I, Stratix Device Family Data Sheet of the *Stratix Device Handbook, Volume 1*.

(9) To ensure that the configuration device successfully configures the Stratix or Stratix GX device in all possible power-up sequences, use a resistor to pull `nCONFIG` up to $V_{CCINT}$.

(10) If external pull-ups are used on `CONF_DONE` and `nSTATUS` pins, they should always be 10 kΩ. You can use the internal pull-ups of the configuration device only if the `CONF_DONE` and `nSTATUS` signals are pulled-up to 3.3 V or 2.5 V (not 1.8 V or 1.5 V).

Figure 13–29 shows a schematic for configuring Stratix and Stratix GX devices using either PS configuration with an EPC16, EPC8, EPC4, or EPC2 configuration device or a download cable.

*Figure 13–29. Device Configuration with a Download Cable & an EPC2, EPC4, EPC8, or EPC16 Device*



*Notes to Figure 13–29:*

(1) Connect $V_{CC}$ to the same supply voltage as the configuration device.

(2) Configure the target Stratix or Stratix GX device by either the configuration device or the download cable.

(3) These pull-up resistors are 1 kΩ.

(4) You can use the internal pull-ups of the configuration device only if the CONF_DONE and nSTATUS signals pulled-up to 3.3 V or 2.5 V (not 1.8 or 1.5 V).

(5) The download cable programs the configuration device through the JTAG circuitry.

(6) $V_{IO}$ is a reference voltage for the MasterBlaster output driver. $V_{IO}$ should match the device's $V_{CCIO}$. Refer to the *MasterBlaster Serial/USB Communications Cable Data Sheet* for this value.

(7) The `nCEO` pin is left unconnected.

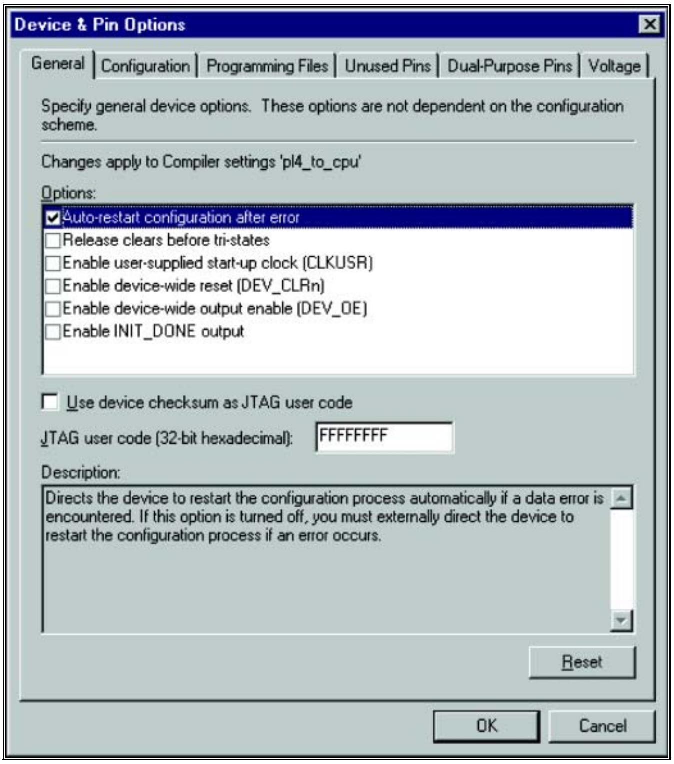
(8) Do not attempt configuration with a download cable while a configuration device is connected to a Stratix or Stratix GX device. To perform this operation, you should either remove the configuration device from its socket when using the download cable, or place a switch on the five common signals between the download cable and the configuration device.

(9) If a 3.3-V supply voltage is used, connect the `VCC`, `VCCSEL`, `VPP`, and `VPPSEL` pins to a 3.3-V supply voltage. If a 5.0-V supply voltage is used, connect the `VCC` and `VPP` pins to a 5.0-V supply voltage, and connect the `VCCSEL` and `VPPSEL` pins to ground. To improve in-system programming times, you can connect `VPP` to 5.0 V, `VCC` to 3.3 V, and `VPPSEL` to ground. For more information on these pins, see Section I, Stratix Device Family Data Sheet of the *Stratix Device Handbook, Volume 1*.

## Device Options

You can set Stratix and Stratix GX device options in Altera's Quartus II development software by choosing **Global Project Device Options** (Assign menu). You can also set device options in the Quartus II software using the **Device & Pin Options** dialog box. To find this option, choose the **Processing** menu, choose **Compiler Settings**, then click the **Chips & Devices** tab. Figure 13–30 shows the **Device & Pin Options** dialog box.

*Figure 13–30. Configuration Options Dialog Box*



Specify general device options. These options are not dependent on the configuration scheme.

Changes apply to Compiler settings 'pl4_to_cpu'

Options:

☑ Auto-restart configuration after error
☐ Release clears before tri-states
☐ Enable user-supplied start-up clock (CLKUSR)
☐ Enable device-wide reset (DEV_CLRn)
☐ Enable device-wide output enable (DEV_OE)
☐ Enable INIT_DONE output

☐ Use device checksum as JTAG user code

JTAG user code (32-bit hexadecimal): FFFFFFFF

Description:

Directs the device to restart the configuration process automatically if a data error is encountered. If this option is turned off, you must externally direct the device to restart the configuration process if an error occurs.

Table 13–15 summarizes each of these options.

*Table 13–15. Stratix & Stratix GX Configuration Option Bits (Part 1 of 2)*

| Device Option | Option Usage | Default Configuration (Option Off) | Modified Configuration (Option On) |
|---|---|---|---|
| Auto-restart configuration on frame error | If a data error occurs during configuration, you can choose how to restart configuration. | The configuration process stops until you direct the device to restart configuration. The `nSTATUS` pin is driven low when an error occurs. When `nCONFIG` is pulled low and then high, the device begins to reconfigure. | The configuration process restarts automatically. The `nSTATUS` pin drives low and releases. The `nSTATUS` pin is then pulled to $V_{CC}$ by the pull-up resistor, indicating that configuration can restart.<br>In the configuration device scheme, if the target device's `nSTATUS` pin is tied to the configuration device's `OE` pin, the `nSTATUS` reset pulse resets the configuration device automatically. The configuration device then releases its `OE` pin (which is pulled high) and reconfiguration begins.<br>If an error occurs during passive configuration, the device can be reconfigured without the system having to pulse `nCONFIG`. After `nSTATUS` goes high, reconfiguration can begin. |
| Release clears before tri-states | During configuration, the device I/O pins are tri-stated. During initialization, you choose the order for releasing the tri-states and clearing the registers. | The device releases the tri-states on its I/O pins before releasing the clear signal on its registers. | The device releases the clear signals on its registers before releasing the tri-states. You can use this option to allow the design to operate before it drives out, so all outputs do not start up low. |
| Enable chip-wide reset | Enables a single pin to reset all device registers. | Chip-wide reset is not enabled. The `DEV_CLRn` pin is available as a user I/O pin. | Chip-wide reset is enabled for all registers in the device. All registers are cleared when the `DEV_CLRn` pin is driven low. |

*Table 13–15. Stratix & Stratix GX Configuration Option Bits (Part 2 of 2)*

| Device Option | Option Usage | Default Configuration (Option Off) | Modified Configuration (Option On) |
|---|---|---|---|
| Enable chip-wide output enable | Enables a single pin to control all device tri-states. | Chip-wide output enable is not enabled. The `DEV_OE` pin is available as a user I/O pin. | Chip-wide output enable is enabled for all device tri-states. After configuration, all user I/O pins are tri-stated when `DEV_OE` is low. |
| Enable INIT_DONE output | Enables a pin to drive out a signal when the initialization process is complete and the device has entered user mode. | The `INIT_DONE` signal is not available. The `INIT_DONE` pin is available as a user I/O pin. | The `INIT_DONE` signal is available on the open-drain `INIT_DONE` pin. This pin drives low during configuration. After initialization, it is released and pulled high externally. The `INIT_DONE` pin must be connected to a 10-kΩ pull-up resistor. If the `INIT_DONE` output is used, the `INIT_DONE` pin cannot be used as a user I/O pin. |

## Device Configuration Pins

Table 13–16 summarizes the Stratix and Stratix GX device configuration pins.

*Table 13–16. Pin Functions (Part 1 of 4)*

| Pin Name | User Mode | Configuration Scheme | Pin Type | Description |
|---|---|---|---|---|
| `MSEL2`<br>`MSEL1`<br>`MSEL0` | – | All | Input | 3-bit configuration input. Sets the Stratix or Stratix GX device configuration scheme. For more information, see Table 13–2. |
| `nSTATUS` | – | All | Bidirectional open-drain | The device drives `nSTATUS` low immediately after power-up and releases it within 5 µs. (When using a configuration device, the configuration device holds `nSTATUS` low for up to 200 ms.) If external pull-up resistors are used on the `nSTATUS` pin, they must be 10-kΩ resistors. If an error occurs during configuration, `nSTATUS` is pulled low by the target device. If an external source drives the `nSTATUS` pin low during configuration or initialization, the target device enters an error state. Driving `nSTATUS` low after configuration and initialization does not affect the configured device. However, if a configuration device is used, driving `nSTATUS` low will cause that device to attempt to configure the Stratix or Stratix GX device. |
| `nCONFIG` | – | All | Input | Configuration control input. A low transition resets the target device; a low-to-high transition begins configuration. All I/O pins go tri-state when setting `nCONFIG` low. |

*Table 13–16. Pin Functions (Part 2 of 4)*

| Pin Name | User Mode | Configuration Scheme | Pin Type | Description |
|---|---|---|---|---|
| `CONF_DONE` | – | All | Bidirectional open-drain | Status output. The target device drives the `CONF_DONE` pin low before and during configuration. Once all configuration data is received without error and the initialization clock cycle starts, the target device releases `CONF_DONE`.<br>Status input. After all data is received and `CONF_DONE` goes high, the target device initializes and enters user mode.<br>If external pull-up resistors are used on the `CONF_DONE` pin, they must be 10-kΩ resistors. An external source can drive this pin low to delay the initialization process, except when configuring with a configuration device. Driving `CONF_DONE` low after configuration and initialization does not affect the configured device. |
| `DCLK` | – | Configuration devices<br>PS<br>FPP | Input | Clock input used to clock data from an external source into the target device. In PPA schemes, `DCLK` should be held high to prevent this pin from floating. |
| `nCE` | – | All | Input | Active-low chip enables. The `nCE` pin activates the device with a low signal to allow configuration and should be tied low for single device configuration. The `nCE` pin must be held low during configuration, initialization, and user mode. |
| `nCEO` | I/O | Multi-device | Output | Output that drives low when device configuration is complete. During multi-device configuration, this pin feeds a subsequent device’s `nCE` pin. |
| `nWS` | I/O | PPA | Input | Write strobe input. A low-to-high transition causes the device to latch a byte of data on the `DATA[7..0]` pins. |
| `nRS` | I/O | PPA | Input | Read strobe input. A low input directs the device to drive the `RDYnBSY` signal on the `DATA7` pin. If the `nRS` pin is not used, it should be tied high. |
| `RDYnBSY` | I/O | PPA | Output | Ready output. A high output indicates that the target device is ready to accept another data byte. A low output indicates that the target device is not ready to receive another data byte. |

*Table 13–16. Pin Functions (Part 3 of 4)*

| Pin Name | User Mode | Configuration Scheme | Pin Type | Description |
|---|---|---|---|---|
| `nCS`<br>`CS` | I/O | PPA | Input | Chip-select inputs. A low on `nCS` and a high on `CS` select the target device for configuration. If only one chip-select input is used, the other must be tied to the active value (e.g., `nCS` can be tied to ground if `CS` is used). The `nCS` and `CS` pins must be held active during configuration and initialization. |
| `CLKUSR` | I/O | All | Input | Optional user-supplied clock input. Synchronizes the initialization of one or more devices. |
| `DATA[7..1]` | I/O | FPP<br>PPA | Inputs | Data inputs. Byte-wide configuration data is presented to the target device on `DATA[7..0]`. |
| `DATA0` | I/O | Configuration device<br>PS<br>PPA<br>FPP | Input | Data input. In serial configuration modes, bit-wide configuration data is presented to the target device on the `DATA0` pin. |
| `DATA7` | I/O | PPA | Output | In the PPA configuration scheme, the `DATA7` pin presents the `RDYnBSY` signal after the `nRS` signal has been strobed, which may be more convenient for microprocessors than using the `RDYnBSY` pin. |
| `INIT_DONE` | I/O | All | Output open-drain | Status pin. Can be used to indicate when the device has initialized and is in user mode. The `INIT_DONE` pin drives low during configuration. Before and after configuration, the `INIT_DONE` pin is released and is pulled to $V_{CC}$ by an external pull-up resistor. Because `INIT_DONE` is tri-stated before configuration, it is pulled high by the external pull-up resistor. Thus, the monitoring circuitry must be able to detect a low-to-high transition. This option is set in the Quartus II software. |
| `DEV_OE` | I/O | All | Input | Optional pin that allows the user to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as programmed. This option is set in the Quartus II software. |
| `DEV_CLRn` | I/O | All | Input | Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed. This option is set in the Quartus II software. |

*Table 13–16. Pin Functions (Part 4 of 4)*

| Pin Name | User Mode | Configuration Scheme | Pin Type | Description |
|---|---|---|---|---|
| `TDI` | I/O or JTAG pins | All | Input | JTAG pins. When used as user I/O pins, JTAG pins must be kept stable before and during configuration. JTAG pin stability prevents accidental loading of JTAG instructions. |
| `TDO` | | | Output | |
| `TMS` | | | Input | |
| `TCK` | | | Input | |
| `TRST` | | | Input | |

## Device Configuration Files

The Quartus II software can create one or more configuration and programming files to support the configuration schemes discussed in this application note. This section describes these files.

### SRAM Object File (.sof)

You should use an SRAM Object File (**.sof**) during PS configuration when the data is downloaded directly from the Altera programming hardware with a MasterBlaster or ByteBlasterMV cable. For Stratix and Stratix GX devices, the Quartus II Compiler's Assembler module automatically creates the SOF for each device in your design. The Quartus II software controls the configuration sequence and automatically inserts the appropriate headers into the configuration data stream. All other configuration files are created from the SOF.

### Programmer Object File (.pof)

A Programmer Object File (**.pof**) is used by the Altera programming hardware to program a configuration device. A POF is generated automatically when a Stratix or Stratix GX project is compiled.

### Raw Binary File (.rbf)

The RBF is a binary file, e.g., one byte of RBF data is 8 configured bits `10000101` (85 Hex), containing the configuration data. Data must be stored so that the LSB of each data byte is loaded first. The converted image can be stored on a mass storage device. The microprocessor can then read data from the binary file and load it into device. You can also use the microprocessor to perform real-time conversion during configuration. In the PPA and FPP configuration schemes, the target device receives its information in parallel from the data bus, a data port on the microprocessor, or some other byte-wide channel. In PS configuration schemes, the data is shifted in serially, LSB first.

## Hexadecimal (Intel-Format) File (.hex)

A Hex File (**.hex**) is an ASCII file in the Intel Hex format. This file is used by third-party programmers to program Altera's serial configuration devices. Hex files are also used to program parallel configuration devices with third-party programming hardware. You can use parallel configuration devices in the FPP or PPA configuration schemes, in which a microprocessor uses the parallel configuration device as the data source.

## Tabular Text File (.ttf)

The Tabular Text File (**.ttf**) is a tabular ASCII file that provides a comma-separated version of the configuration data for the PPA, FPP, and bit-wide PS configuration schemes. In some applications, the storage device containing the configuration data is neither dedicated to nor connected directly to the target device. For example, a configuration device can also contain executable code for a system (e.g., BIOS routines) and other data. The TTF allows you to include the configuration data as part of the microprocessor's source code using the `include` or `source` commands. The microprocessor can access this data from a configuration device or mass-storage device and load it into the target device. A TTF can be imported into nearly any assembly language or high-level language compiler.

## Jam File (.jam)

A Jam File (**.jam**) is an ASCII text file in the Jam device programming language that stores device programming information. These files are used to program, verify, and blank-check one or more devices in the Quartus II Programmer or in an embedded processor-type environment.

## Jam Byte-Code File (.jbc)

A Jam Byte-Code File (**.jbc**) is a binary version of a Jam file in a byte-code representation. JBC file stores device programming information used to program, verify, and blank-check one or more devices.

## Programming Configuration Devices

You can configure Stratix and Stratix GX devices using data stored in either a configuration device or the Quartus II software.

You can program configuration devices using the Quartus II software, the Altera Programming Unit (APU), and the appropriate configuration device programming adapter. Table 13–17 shows which programming adapter to use with each configuration device.

*Table 13–17. Programming Adapters*

| Device | Package | Adapter |
|---|---|---|
| EPC16 | 88-pin Ultra FineLine™ BGA<br>100-pin PQFP | PLMUEPC-88<br>PLMQEPC-100 |
| EPC8 | 100-pin PQFP | PLMQEPC-100 |
| EPC4 | 100-pin PQFP | PLMQEPC-100 |
| EPC2 | 20-pin J-Lead<br>32-pin TQFP | PLMJ1213<br>PLMT1213 |

## Configuration Reliability

The Stratix and Stratix GX architectures are designed to minimize the effects of power supply and data noise in a system, and to ensure that the configuration data is not corrupted during configuration or normal user-mode operation. A number of circuit design features ensure the highest possible level of reliability from this SRAM technology.

Cyclic redundancy code (CRC) circuitry validates each data frame (i.e., sequence of data bits) as it is loaded into the target device. If the CRC generated by the device does not match the data stored in the data stream, the configuration process is halted, and the `nSTATUS` pin is pulled and held low to indicate an error condition. CRC circuitry ensures that noisy systems will not cause errors that yield an incorrect or incomplete configuration.

The Stratix and Stratix GX device architectures also provide a very high level of reliability in low-voltage brown-out conditions. Stratix and Stratix GX device SRAM cells require a certain $V_{CC}$ level to maintain accurate data. This voltage threshold is significantly lower than the voltage required to activate the device's POR circuitry. Therefore, the target device stops operating if the $V_{CC}$ starts to fail, and indicates an operation error by pulling and holding the `nSTATUS` pin low. You must then reconfigure the device before it can resume operation as a logic device. In active configuration schemes in which `nCONFIG` is tied to $V_{CC}$, reconfiguration begins as soon as $V_{CC}$ returns to an acceptable level. The low pulse on `nSTATUS` resets the configuration device by driving `OE` low. In passive configuration schemes, the host system starts the reconfiguration process.

These device features ensure that Stratix and Stratix GX devices have the highest possible reliability in a wide variety of environments, and provide the same high level of system reliability that exists in other Altera PLDs.

## Board Layout Tips

Even though the `DCLK` signal (used in configuration device, PS, and FPP configuration schemes) is fairly low-frequency, it drives edge-triggered pins on the Stratix or Stratix GX device. Therefore, any overshoot, undershoot, ringing, or other noise can affect configuration. When designing the board, lay out the `DCLK` trace using the same techniques as laying out a clock line, including appropriate buffering. If more than five devices are used, Altera recommends using buffers to split the fan-out on the `DCLK` signal.

# 14. Using Altera Enhanced Configuration Devices

S52014-1.0

Chapter 14, Using Altera Enhanced Configuration Devices replaces *AN 218: Using Altera Enhanced Configuration Devices*.

## Introduction

Altera's latest enhanced configuration devices address the need for a high-density configuration solution by combining industry-standard flash memory with a feature-rich configuration controller. A single-chip configuration solution provides designers with several new and advanced features that significantly reduce configuration times. This application note discusses the hardware and software implementation of enhanced configuration device features such as concurrent and dynamic configuration, data compression, clock division, and an external flash memory interface. Enhanced configuration devices include EPC4, EPC8, and EPC16 devices.

## Concurrent Configuration

Configuration data is transmitted from the enhanced configuration device to the SRAM-based device on the `DATA` lines. The `DATA` lines are outputs on the enhanced configuration devices, and inputs to the SRAM-based devices.

These `DATA` lines correspond to the `Bitn` lines in the **Convert Programming Files** window in the Altera® Quartus® II software. For example, if you specify a SRAM Object File (**.sof**) to use `Bit0` in the Quartus II software, that **.sof** will be transmitted on the `DATA[0]` line from the enhanced configuration device to the SRAM-based device.

Enhanced configuration devices can concurrently configure a number of devices with a variety of supported configuration schemes.

### Supported Schemes & Guidelines

By using enhanced configuration devices, there are several different ways to configure Altera® SRAM-based programmable logic devices (PLDs):

- 1-bit passive serial (PS)
- 2-bit PS
- 4-bit PS
- 8-bit PS
- Fast passive parallel (FPP)

Additionally, you can use these configuration schemes in conjunction with the dynamic configuration option (previously called page mode operation) for sophisticated configuration setups.

FPP configuration mode uses the eight `DATA [7..0]` lines from the enhanced configuration device, which can be used to configure Stratix™, Stratix GX, and APEX™ II devices. To decrease configuration time, FPP configuration provides eight bits of configuration data per clock cycle to the target device.

For more information on configuration schemes, refer to the *Enhanced Configuration Devices Data Sheet*, *Application Note 116: Configuring SRAM-Based LUT Devices*, or Chapter 13, Configuring Stratix & Stratix GX Devices.

## Concurrent Configuration Using *n*-Bit PS Modes

The *n*-bit (*n* = 1, 2, 4, and 8) PS configuration mode allows enhanced configuration devices to concurrently configure SRAM-based devices or device chains. In addition, these devices do not have to be the same device family or density; they can be any combination of Altera SRAM-based devices. An individual enhanced configuration device `DATA` line is available for each targeted device. Each `DATA` line can also feed a daisy chain of devices.

The Quartus II software only allows the selection of *n*-bit PS configuration modes. However, you can use these modes to configure any number of devices from 1 to 8. When configuring SRAM-based devices using *n*-bit PS modes, use Table 14–1 to select the appropriate configuration mode for the fastest configuration times.

☞ Mode selection has an impact on the amount of memory used, as described in "Calculating the Size of Configuration Space" on page 14–18.

***Table 14–1. Recommended Configuration Using n-Bit PS Modes***

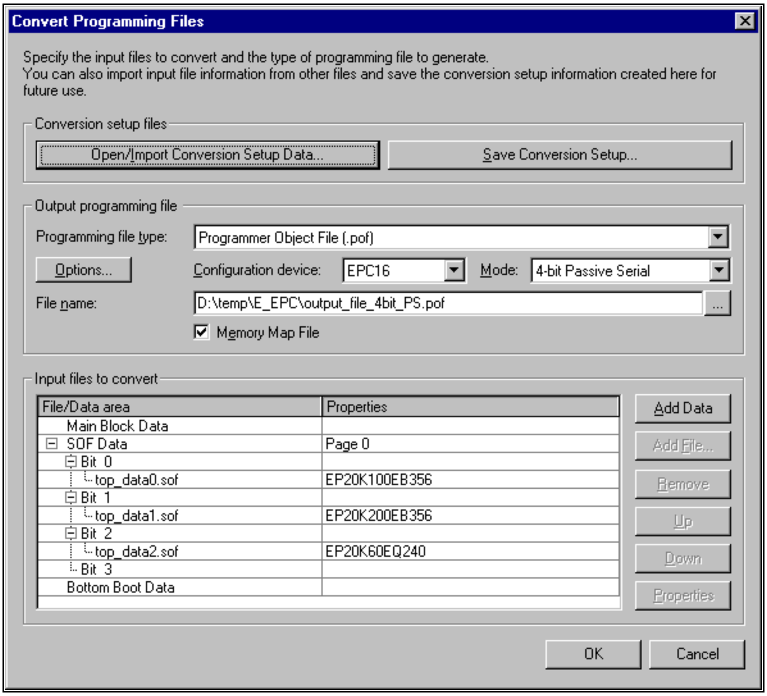
| Number of Devices *(1)* | Recommended Configuration Mode |
|---|---|
| 1 | 1-bit PS |
| 2 | 2-bit PS |
| 3 | 4-bit PS |
| 4 | 4-bit PS |
| 5 | 8-bit PS |
| 6 | 8-bit PS |
| 7 | 8-bit PS |
| 8 | 8-bit PS |

***Note to Table 14–1:***

(1) Assume that each `DATA` line is only configuring one device, not a daisy chain of devices.

For example, if you configure three SRAM-based devices, you would use the 4-bit PS mode. For the `DATA0`, `DATA1`, and `DATA2` lines, the corresponding **.sof** data will be transmitted from the configuration device to the SRAM-based PLD. For `DATA3`, you can leave the corresponding `Bit3` line blank in the Quartus II software. On the printed circuit board (PCB), leave the `DATA3` line from the enhanced configuration device unconnected. Figure 14–1 shows the **Quartus II Convert Programming Files** window (Tools menu) setup for this scheme.

Figure 14–1. Software Settings for Configuring Devices Using n-Bit PS Modes



Convert Programming Files

Specify the input files to convert and the type of programming file to generate.
You can also import input file information from other files and save the conversion setup information created here for future use.

Conversion setup files

Output programming file

Programming file type: Programmer Object File (.pof)

Configuration device: EPC16

Mode: 4-bit Passive Serial

File name: D:\temp\E_EPC\output_file_4bit_PS.pof

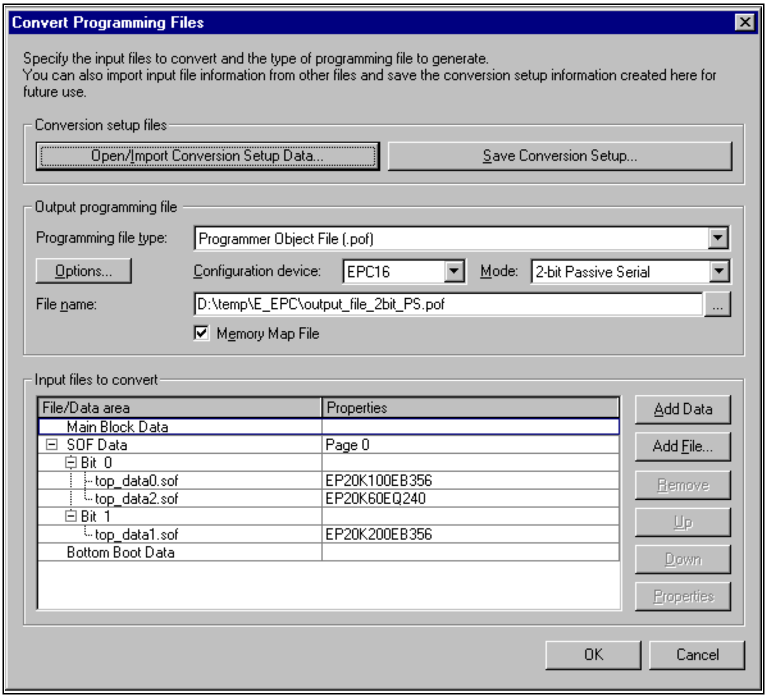
☑ Memory Map File

Input files to convert

| File/Data area | Properties |
|---|---|
| Main Block Data | |
| ⊟ SOF Data | Page 0 |
| ⊟ Bit 0 | |
| top_data0.sof | EP20K100EB356 |
| ⊟ Bit 1 | |
| top_data1.sof | EP20K200EB356 |
| ⊟ Bit 2 | |
| top_data2.sof | EP20K60EQ240 |
| Bit 3 | |
| Bottom Boot Data | |

Alternatively, you can daisy chain two SRAM-based devices to one `DATA` line while the other `DATA` lines drive one device each. For example, you could use the 2-bit PS mode to drive two SRAM-based devices with `DATA Bit0` (EP20K100E and EP20K60E devices) and the third device (the EP20K200E device) with `DATA Bit1`. This 2-bit PS configuration scheme requires less space in the configuration flash memory, but may increase the total system configuration time. See Figure 14–2.

*Figure 14–2. Setup for Daisy Chaining Two SRAM-Based Devices to One DATA Line*



Specify the input files to convert and the type of programming file to generate.
You can also import input file information from other files and save the conversion setup information created here for future use.

Programming file type: Programmer Object File (.pof)

Configuration device: EPC16

Mode: 2-bit Passive Serial

File name: D:\temp\E_EPC\output_file_2bit_PS.pof

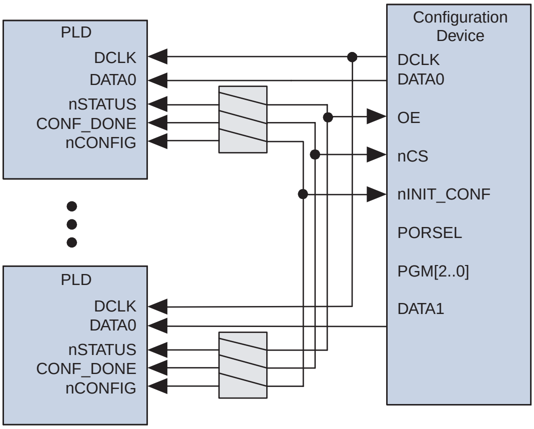
☑ Memory Map File

| File/Data area | Properties |
|---|---|
| Main Block Data | |
| SOF Data | Page 0 |
| Bit 0 | |
| top_data0.sof | EP20K100EB356 |
| top_data2.sof | EP20K60EQ240 |
| Bit 1 | |
| top_data1.sof | EP20K200EB356 |
| Bottom Boot Data | |

## Design Guidelines

For debugging, Altera recommends keeping the control lines such as `nSTATUS`, `nCONFIG`, and `CONF_DONE` between each PLD and the configuration device separate. You can keep control lines separate by using a switch to manage which control signals are fed back into the enhanced configuration device. Figure 14–3 shows an example of the connections between the enhanced configuration device and the targeted PLDs.

*Figure 14–3. Example of Using Debugging Switches for Control Lines*



## Dynamic Configuration (Page Mode) Implementation Overview

Pages in enhanced configuration devices allow you to organize and store various configurations for entire systems that use one or more Altera PLDs. This dynamic configuration (or page mode) feature allows systems to dynamically reconfigure their PLDs with different configuration files.

You can use different pages to store configuration files that support different standards (e.g., I/O standards, memory). Alternatively, the different pages can place the system in different modes. For instance, page 0 could contain a configuration file (**.sof**) for the PLD that only processes data packets; page 1 could contain a configuration file for the same PLD that processes data and voice packets.

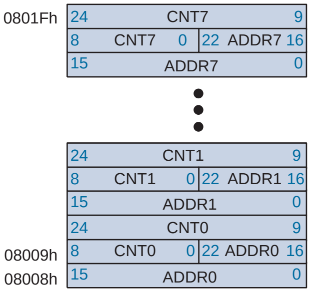
With the ability to dynamically switch pages, you can also configure Altera devices with various revisions for debugging without having to reprogram the configuration device. For example, you can configure a device that is on “stand-by” to perform another function and then reconfigure it back with the original configuration file.

A page is a section of the flash memory space that contains configuration data for all PLDs in the system. One page stores one system configuration regardless of the number of PLDs in the system. The size of each page is dynamic and can change each time the enhanced configuration device is reprogrammed. Enhanced configuration devices support a maximum of eight pages of configuration data, or eight system configurations. The number of pages is also limited to the density of the configuration device.

The number of pages required in a system is not dependent on the number of PLDs in the system, but depends on the number of unique system configurations.

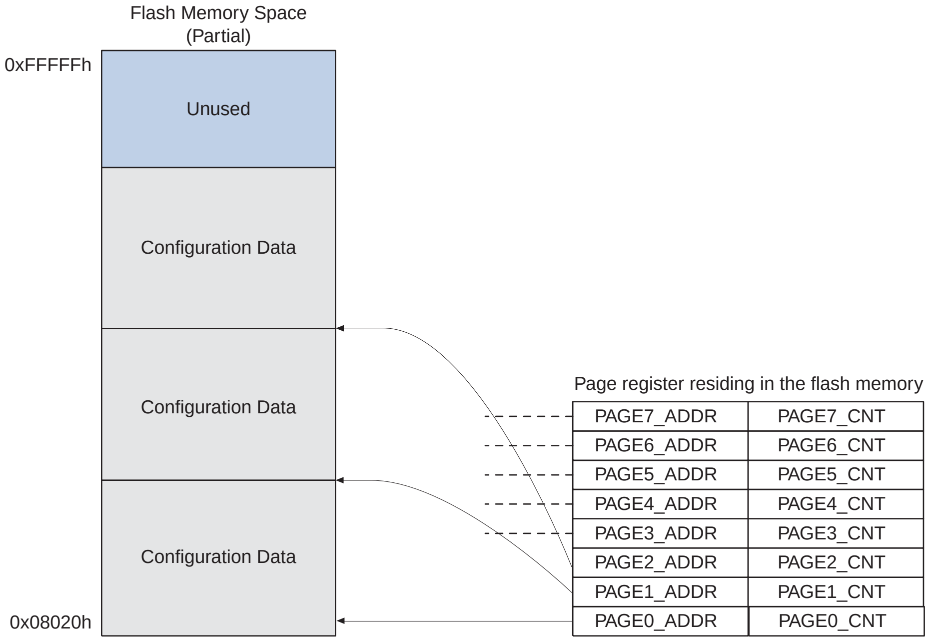
External page mode input pins `PGM[2..0]` determine which page to use during PLD configuration, and page pointers determine the data location. Each page pointer consists of a starting address register and a length count register. The word-addressable starting address register (23 bits) is used to determine where the page begins in the flash memory. The count register (25 bits) determines the length of the page counted in nibbles (group of 4 bits equaling half of a byte). Figure 14–4 shows a block diagram of the option-bit space and its address locations.

*Figure 14–4. Option-Bit Memory Map*



For instance, a page for the EPC16 configuration device must start between word addresses `0x08020h` and `0xFFFFFh` and cannot overlap with other pages. See Figure 14–5 for an EPC16 page mode example using three pages.

*Figure 14–5. EPC16 Page Mode Implementation Example*



During configuration, different pages are selected by the `PGM[2..0]` pins. These pins are used to select one out of eight pages (or eight system configurations). `PGM[2..0]` pins are sampled once before the configuration data is sent to the target PLDs.

Within each page, you can store as many configuration files as your system needs. There is no limitation to the length of a page except for the physical limitation determined by the size of the flash memory (e.g., `0xFFFFFFh` for EPC16 devices). However, all pages must be contiguous.

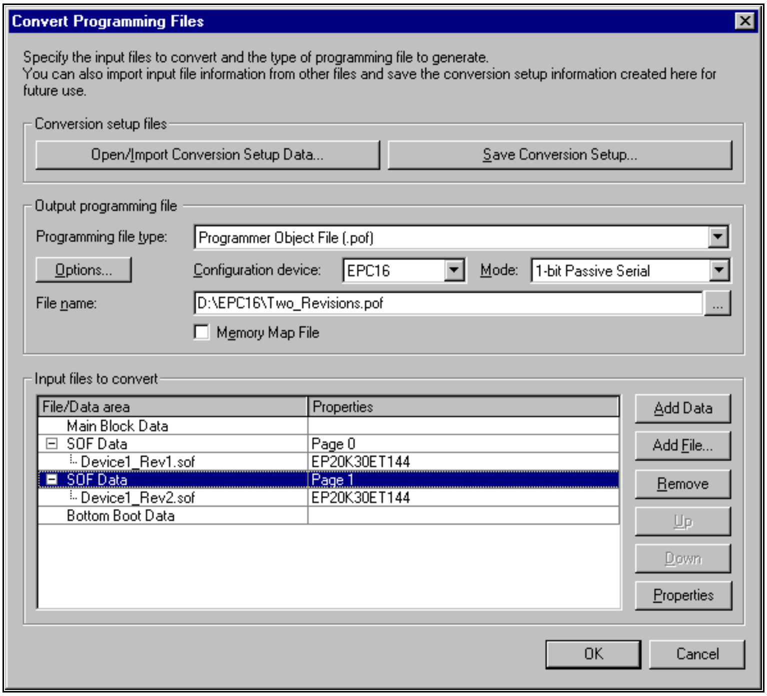
## Software Implementation (Convert Programming Files)

The **Convert Programming Files** window (Tools menu) in the Quartus II software allows you to create enhanced configuration device programmer object files (**.pof**) and enable the dynamic configuration feature.

Passive parallel asynchronous (PPA) and passive parallel synchronous (PPS) configuration modes are not supported by enhanced configuration devices. If you choose one of these modes, the Quartus II software reports an error message when the enhanced configuration device's **.pof** is generated.

In the **Convert Programming Files** window, there are **SOF Data** entries (**.sof**), located in the **Input files to convert** dialog box. Each **SOF Data** entry refers to a unique system configuration. Figure 14–6 shows the setup for a system that has one APEX device and uses two pages, 0 and 1. Each of the two pages has a different version of the configuration file for the same APEX device.

*Figure 14–6. Using Page Mode Example*



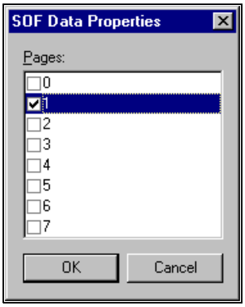
Specify the input files to convert and the type of programming file to generate.
You can also import input file information from other files and save the conversion setup information created here for future use.

Programming file type: Programmer Object File (.pof)
Configuration device: EPC16
Mode: 1-bit Passive Serial
File name: D:\EPC16\Two_Revisions.pof
☐ Memory Map File

| File/Data area | Properties |
|---|---|
| Main Block Data | |
| ⊟ SOF Data | Page 0 |
| Device1_Rev1.sof | EP20K30ET144 |
| ⊟ SOF Data | Page 1 |
| Device1_Rev2.sof | EP20K30ET144 |
| Bottom Boot Data | |

To set which page pointer(s) will point to a particular page or **SOF Data** entry, select **SOF Data** and click **Properties**. Clicking **Properties** launches the **SOF Data Properties** window where you can select page pointers to point to the **SOF Data** chosen. If you do not use the **SOF Data Properties** window to make changes, the default page is 0. Each **SOF Data** entry for your configuration device must have a unique page number(s). Figure 14–7 shows page pointer 1 being assigned to the **SOF Data** section containing **Device1_Rev2.sof** (from Figure 14–6).

*Figure 14–7. Software Setting for Selecting Pages*



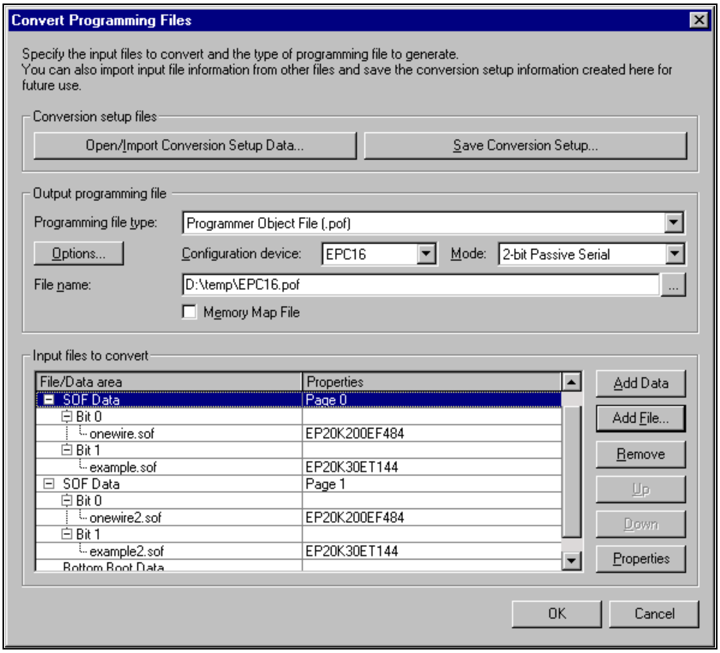
SOF Data Properties

Pages:

☐ 0
☑ 1
☐ 2
☐ 3
☐ 4
☐ 5
☐ 6
☐ 7

Figure 14–8 shows a more complex setup that uses the 2-bit PS configuration mode to concurrently configure two different APEX devices with multiple pages storing two revisions of each design. Two configurations for the entire system requires four configuration files (i.e., the number of devices multiplied by the number of unique system configurations).

*Figure 14–8. Concurrent Configuration of Two Devices with Two System Configurations*



Specify the input files to convert and the type of programming file to generate.
You can also import input file information from other files and save the conversion setup information created here for future use.

Programming file type: Programmer Object File (.pof)

Configuration device: EPC16

Mode: 2-bit Passive Serial

File name: D:\temp\EPC16.pof

☐ Memory Map File

| File/Data area | Properties |
|---|---|
| SOF Data | Page 0 |
| Bit 0 | |
| onewire.sof | EP20K200EF484 |
| Bit 1 | |
| example.sof | EP20K30ET144 |
| SOF Data | Page 1 |
| Bit 0 | |
| onewire2.sof | EP20K200EF484 |
| Bit 1 | |
| example2.sof | EP20K30ET144 |
| Bottom Boot Data | |

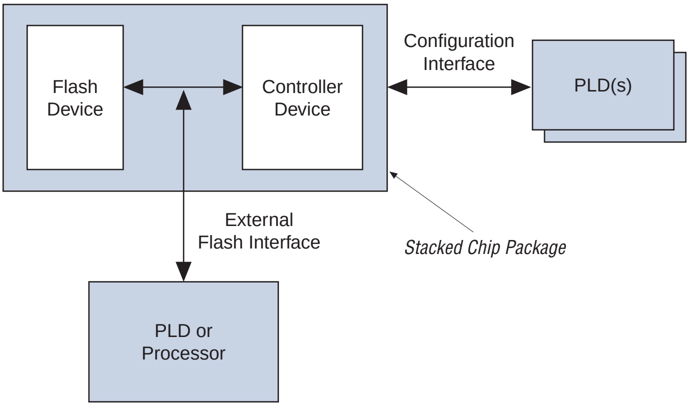
By selecting the *Memory Map File* option, the Quartus II Memory Map output file (**.map**) describing the flash memory address locations is generated. This information is typically useful when using the external flash interface feature.

## External Flash Memory Interface

Enhanced configuration devices support an external flash interface that allows devices external to the controller access to the enhanced configuration device’s flash memory. You can use the flash memory to store boot or application code for processors, or as general-purpose memory for processors and PLDs.

Figure 14–9 shows the interfaces available on the enhanced configuration device.

*Figure 14–9. Enhanced Configuration Device Interfaces*



Applications that require remote update capabilities for on-board programmable logic (Stratix and Stratix GX devices), and applications that use soft embedded processor cores (e.g., the Nios® embedded processor) typically use the external flash memory interface feature.

For soft core embedded processor applications, the controller configures the programmable logic by using configuration data stored in the flash memory. On successful configuration, the embedded processor uses the external flash interface to boot up and run code from the same flash memory, eliminating the need for a stand-alone flash memory device.

For applications requiring remote system configuration capabilities, a processor or PLD can use the external flash interface to store an updated configuration image into a new page in flash memory (the external flash interface coupled with dynamic configuration). You can obtain new configuration data from a local intelligent host or through the Internet. Reconfiguring the system with the new page updates the system configuration.

For more information on implementing remote and local system updates with enhanced configuration devices, refer to Chapter 15, Using Remote System Configuration with Stratix & Stratix GX Devices.

Currently, EPC4 and EPC16 configuration devices support the external flash interface. For support of this feature in other enhanced configuration devices, contact Altera Applications.

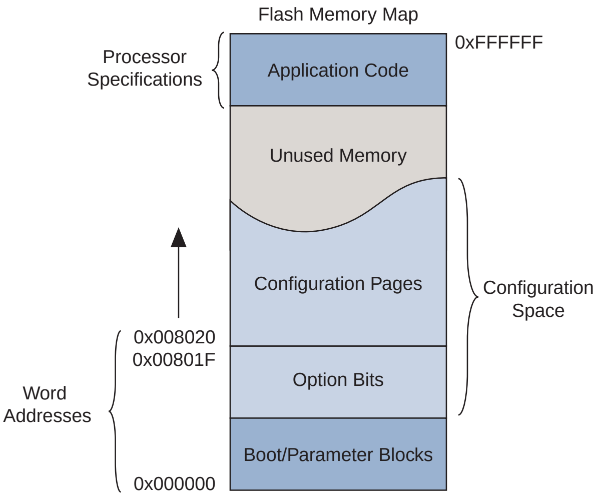
## Flash Memory Map

You can divide an enhanced configuration device's flash memory into two categories: logical (configuration and processor space) and physical (flash data block boundaries). Configuration space consists of portions of memory used to store configuration option bits and configuration data. Processor space consists of portions of memory used to store boot and application code.

### *Logical Divisions*

In all enhanced configuration devices, configuration option bits are stored ranging from word address `0x008000` to `0x00801F` (i.e., byte address `0x010000` to `0x01003F`). These bits are used to enable various controller features such as configuration mode selection, compression mode selection, and clock divider selection. In all enhanced configuration devices, configuration data is stored starting from word address location `0x008020` or byte address `0x010040`. The ending address of configuration space is not fixed and depends on the number and density of PLDs configured using the enhanced configuration device as well as the number of pages. All remaining address locations above the configuration space are available for processor application code. The boot space spans addresses `0x000000` to `0x007FFF`. Both boot and application code spaces are intended for use by an external processor or PLD. Figure 14–10 shows the flash memory map inside an EPC16 device.

***Figure 14–10. EPC16 Flash Memory Map***



### *Physical Divisions*

Conversely, physical divisions are flash data blocks that can be individually written to and erased. For instance, the EPC16 device contains 16-Mbit Sharp flash memory that is divided into 2 boot blocks, 6 parameter blocks, and 31 main data blocks. These physical divisions vary from one flash memory or vendor to another and must be considered if the external flash interface is used to erase or write flash memory. These divisions are not significant if the interface is used as a read-only interface after initial programming.

For detailed information on enhanced configuration device flash memories, refer to the corresponding flash memory data sheet. The SHARP and Micron data sheets include flash command details, timing diagrams, and flash memory map information, and are available at **http://www.altera.com**.

## Interface Availability & Connections

Flash memory ports are shared between the internal controller and the external device. A processor or PLD can use the external flash interface to access flash memory only when the controller is not using the interface. Therefore, the internal controller is the primary master of the bus, while the external device is the secondary master.

Flash memory ports (address, data, and control) are internally connected to the controller device. Additionally, these ports are connected to pins on the package providing the external interface. During in-system programming of the enhanced configuration device as well as configuration of the PLDs, the controller uses the internal interface to flash memory, rendering the external interface unavailable. External devices should tri-state all connections (address, data, and control) for the entire duration of in-system programming and configuration to prevent contention.

On completion of in-system programming and configuration, the internal controller tri-states its interface to the flash memory and enables weak internal pull-up resistors on address and control lines as well as bus-hold circuits on the data lines. The internal flash interface is now disabled and the external flash interface is available.

☞ If you do not use the external flash interface feature, most flash-related pins must be left unconnected on the board to avoid contention. There are a few exceptions to this guideline outlined in the data sheet and pin-out tables.

For detailed schematics, refer to the *Enhanced Configuration Device Data Sheet*.

## Quartus II Software Support

You can use the **Convert Programming Files** window to generate flash memory programming files. You can program flash memory in-system using Joint Test Action Group (JTAG) or through the external flash interface. Select the **.pof** when programming the flash memory in-system. You can also convert this **.pof** to a Jam™ standard test and programming language (STAPL) file (**.jam**) or Jam Byte-Code file (**.jbc**) for in-system programming. When programming the flash memory through the external flash interface, you can create a **.hexpof** from this window.

☞ The **.hexpof** used for programming enhanced configuration devices is different from the **.hexout** configuration file generated for SRAM PLDs.

Along with PLD configuration files, you can program processor boot and application code into flash memory through the **Convert Programming Files** window. You can add a **.hex** file containing boot code to the **Bottom Boot Data** section of the window. Similarly, you can add a **.hex** file containing application code to the **Main Block Data** section. You can store these files in the flash memory using relative or absolute addressing. For selecting the type of addressing, highlight the **Bottom Boot Data** or **Main Block Data** section and click **Properties** (**Convert Programming Files** window).

Relative addressing mode allows the Quartus II software to pick the location of the file in memory. For instance, the Quartus II software always stores boot code starting at address location `0x000000`. This data increases to higher addresses.

☞ The maximum boot file size for the EPC16 configuration device is 32 K words or 64 Kbytes. The boot code is limited to the boot and flash memory parameter blocks.

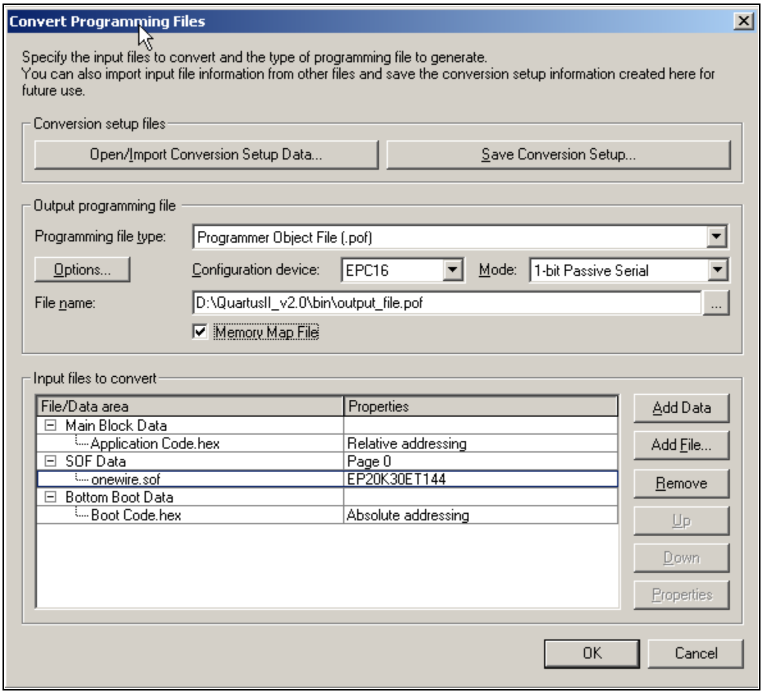
When you select relative addressing mode for **Main Block Data**, the Quartus II software aligns the last byte of information with the highest address (i.e., `0x1FFFFF`). Therefore, the starting address is dependent on the size of the **.hex** file. You can easily obtain the starting address of the application code by using the **.map** file discussed below.

Conversely, the absolute addressing mode forces the Quartus II software to store the boot or application **.hex** file data in address locations specified inside the **.hex** file itself. When this mode is selected, create **.hex** files with the correct offsets and ensure there is no overlap with addresses used for storing configuration data.

Figure 14–11 shows a screen shot of the **Convert Programming Files** window setup to create a **.pof** and **.map** file for an enhanced configuration device.

> ☞ Only one **.hex** file can be added to the **Bottom Boot Data** and **Main Block Data** sections of this window.

***Figure 14–11. Storing Boot & Application Code in Flash Memory***



Convert Programming Files

Specify the input files to convert and the type of programming file to generate.
You can also import input file information from other files and save the conversion setup information created here for future use.

Conversion setup files

Output programming file

Programming file type: Programmer Object File (.pof)

Configuration device: EPC16

Mode: 1-bit Passive Serial

File name: D:\QuartusII_v2.0\bin\output_file.pof

☑ Memory Map File

Input files to convert

| File/Data area | Properties |
|---|---|
| ⊟ Main Block Data | |
| Application Code.hex | Relative addressing |
| ⊟ SOF Data | Page 0 |
| onewire.sof | EP20K30ET144 |
| ⊟ Bottom Boot Data | |
| Boot Code.hex | Absolute addressing |

You can use the **Quartus II Convert Programming Files** window to create two files specific to the external flash interface feature—the **.hexpof** and the **.map** files. The **.hexpof** contains an image of the flash memory and the **.map** file contains memory map information. The **.hexpof** can be used by an external processor or PLD to program the flash memory via the external flash interface. The **.map** file contains starting and ending addresses for boot code, configuration page data, and application code.

You can use the **.hexpof** to program blank enhanced configuration devices and/or update portions of the flash memory (e.g., a new configuration page). This file uses the Intel hexadecimal file format and contains 16 Mbits or 2 Mbytes of data. The format of the **.map** file is shown in Table 14–2.

*Table 14–2. File Format (.map)* *Note (1)*

| Block | Start Address | End Address |
|---|---|---|
| `BOTTOM BOOT` | `0x00000000` | `0x0000001F` |
| `OPTION BITS` | `0x00010000` | `0x0001003F` |
| `PAGE 0` | `0x00010040` | `0x0001AD7F` |
| `MAIN` | `0x001FFFE0` | `0x001FFFFF` |

***Note to Table 14–2:***

(1) All the addresses in this file are byte addresses.

To perform partial flash memory updates, select the relevant portions of the **.hexpof** using memory map information provided in the **.map** file.

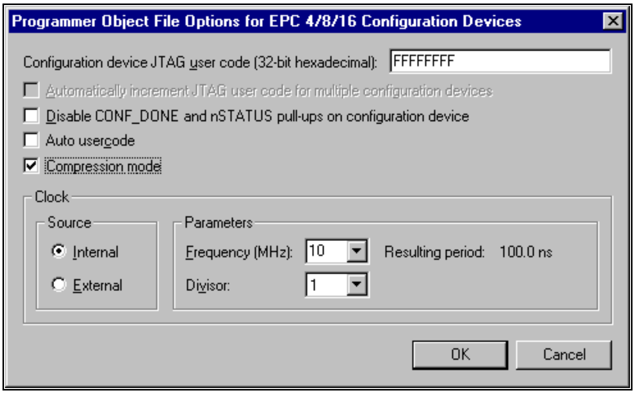
Configuration data and processor space data could exist within the same physical data block. In such cases, erasing the physical data block would affect both configuration and processor data, requiring you to update both. You can avoid this situation by storing application data starting from the next available whole data block.

## Data Compression

Enhanced configuration devices support an efficient compression algorithm that compresses configuration data by 1.9× for typical designs, effectively doubling the size of the device. To select the right density for enhanced configuration devices, you should pre-calculate the total size of uncompressed configuration space.

By clicking **Options** (Convert Programming Files window), you can turn on the *Compression mode* option in the **Programming Object File Options** window with **pof** selected as the programming file type, as shown in Figure 14–12.

*Figure 14–12. Selecting Compression Mode*



Programmer Object File Options for EPC 4/8/16 Configuration Devices

Configuration device JTAG user code (32-bit hexadecimal): FFFFFFFF

☐ Automatically increment JTAG user code for multiple configuration devices

☐ Disable CONF_DONE and nSTATUS pull-ups on configuration device

☐ Auto usercode

☑ Compression mode

Clock

Source

● Internal

○ External

Parameters

Frequency (MHz): 10

Resulting period: 100.0 ns

Divisor: 1

## Calculating the Size of Configuration Space

When using 1-bit PS configuration mode to serially configure multiple devices, all configuration data is transmitted through the same `DATA` line and the devices are daisy-chained together. Therefore, the total size of the uncompressed configuration data is equal to the sum of the SRAM-based device's configuration file size multiplied by the number of pages used.

When using *n*-bit PS configuration mode to concurrently configure multiple devices, each SRAM-based device has its own `DATA` line from the enhanced configuration devices. The total size of the uncompressed configuration space is equal to the size of the largest device's configuration file size multiplied by *n* (where *n* = 1, 2, 4, or 8), which is then multiplied by the number of pages used. For example, if three devices are concurrently configured using 4-bit PS configuration mode, the total size of the uncompressed configuration space is equal to the size of the largest device's configuration file multiplied by four.

When using FPP configuration mode, the total size of the uncompressed configuration space is equal to the sum of the SRAM-based device's configuration file size multiplied by the number of pages used

For configuration file sizes of SRAM-based devices, refer to *Application Note 116: Configuring SRAM-Based LUT Devices*.

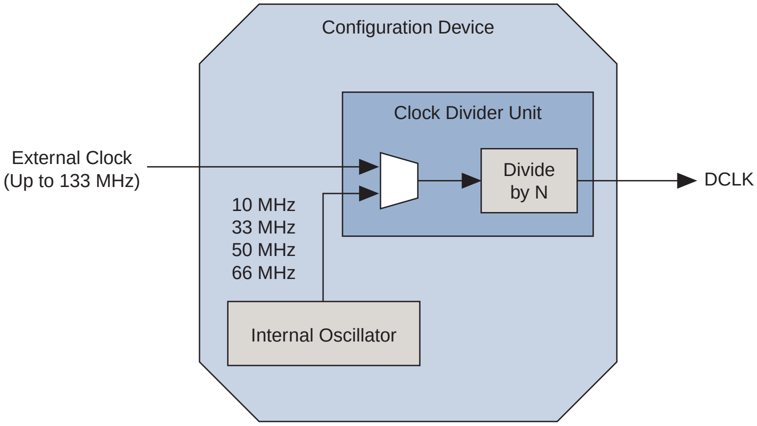
## Clock Divider

The clock divider value specifies the clock frequency divisor, which is used to determine the `DCLK` frequency, or how fast the data is clocked into the SRAM-based device. You must consider the maximum `DCLK` input frequency of the targeted SRAM device family while selecting the clock input and divider settings. For `DCLK` timing specifications of SRAM-based devices, refer to *Application Note 116: Configuring SRAM-Based LUT Devices*.

## Settings & Guidelines

Enhanced configuration devices can use either the internal oscillator or an external clock source to clock data into SRAM-based devices, as shown in Figure 14–13. The enhanced configuration device's internal oscillator runs at nominal speeds of 10, 33, 50, or 66 MHz. The minimum and maximum speeds are shown in the *Enhanced Configuration Device Data Sheet*. Additionally, the enhanced configuration device can accept an external clock source running at speeds of up to 133 MHz.

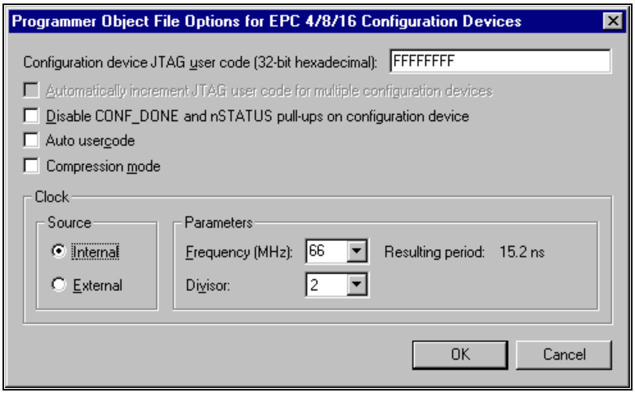
*Figure 14–13. Clock Divider Unit in Enhanced Configuration Devices*



## Software Implementations

You can select the clock source and the clock speed in the **Programming Object File Options** window with **pof** selected as the programming file type (Convert Programming Files window), as shown in Figure 14–14. You can type the appropriate external clock frequency in the **Frequency (MHz)** drop-down menu, and select any value from the divisor list regardless of the clock source setting.

*Figure 14–14. Software for Setting Clock Source & Clock Divisor*



Programmer Object File Options for EPC 4/8/16 Configuration Devices

Configuration device JTAG user code (32-bit hexadecimal): FFFFFFFF

☐ Automatically increment JTAG user code for multiple configuration devices

☐ Disable CONF_DONE and nSTATUS pull-ups on configuration device

☐ Auto usercode

☐ Compression mode

Clock

Source

● Internal

○ External

Parameters

Frequency (MHz): 66

Resulting period: 15.2 ns

Divisor: 2

## Conclusion

The enhanced configuration device is a single-chip configuration solution that provides designers with increased configuration flexibility and faster time-to-market. Features such as data compression, multiple clock sources, clock division, and parallel or concurrent programming significantly reduce configuration times, while the dynamic configuration mode and the external flash interface take intelligent system configuration to a higher level.

# 15. Using Remote System Configuration with Stratix & Stratix GX Devices

S52015-1.0

Chapter 15, Using Remote System Configuration with Stratix & Stratix GX Devices replaces *AN 217: Using Remote System Configuration with Stratix & Stratix GX Devices*.

## Introduction

Altera® Stratix™ and Stratix GX devices are the first programmable logic devices (PLDs) featuring dedicated support for remote system configuration. Using remote system configuration, a Stratix or Stratix GX device can receive new configuration data from a remote source, update the flash memory content (through enhanced configuration devices or any other storage device), and then reconfigure itself with the new data.

Like all Altera SRAM-based devices, Stratix and Stratix GX devices support standard configuration modes such as passive serial (PS), fast passive parallel (FPP), and passive parallel asynchronous (PPA). You can use the standard configuration modes with remote system configuration.

This application note discusses remote system configuration of Stratix and Stratix GX devices, and how to interface them with enhanced configuration devices to enable this capability. This document also explains some related remote system configuration topics, such as the watchdog timer, remote system configuration registers, and factory or application configurations files. The Quartus® II software (version 2.1 and later) supports remote system configuration.

## Remote Configuration Operation

Remote system configuration has three major parts:

- The Stratix or Stratix GX device receives updated or new data from a remote source over a network (or through any other source that can transfer data). You can implement a Nios™ embedded processor within either a Stratix or Stratix GX device or an external processor to control the read and write functions of configuration files from the remote source to the memory device.
- The new or updated information is stored into the memory device, which can be an enhanced configuration device, industry-standard flash memory device, or any other storage device (see Figure 15–2).
- The Stratix or Stratix GX device updates itself with the new data from the memory.

Figure 15–1 shows the concept of remote system configuration in Stratix and Stratix GX devices.

*Figure 15–1. Remote System Configuration with Stratix & Stratix GX Devices*

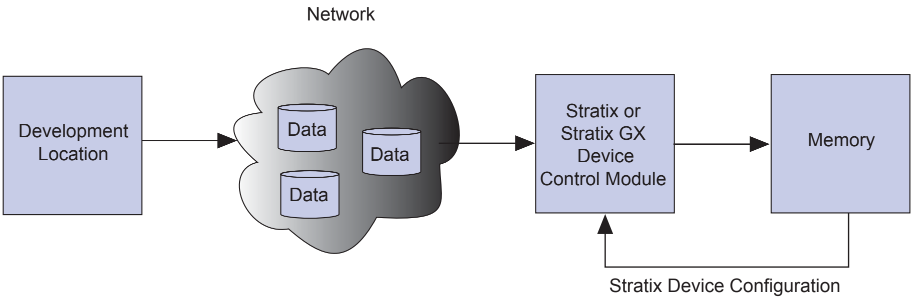
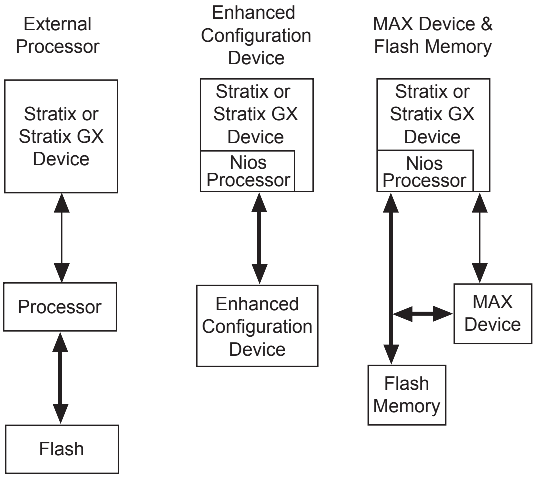


*Figure 15–2. Different Options for Remote System Configuration*



## Remote System Configuration Modes

Stratix and Stratix GX device remote system configuration has two modes: remote configuration mode and local configuration mode. Table 15–1 shows the pin selection settings for each configuration mode.

*Table 15–1. Standard, Remote & Local Configuration Options* Note (1)

| `RUnLU` (2) | `MSEL[2]` (3) | `MSEL[1..0]` | System Configuration Mode | Configuration Mode |
|---|---|---|---|---|
| – | 0 | 00 | Standard | FPP |
| – | 0 | 01 | Standard | PPA |
| – | 0 | 10 | Standard | PS |
| 1 | 1 | 00 | Remote | FPP |
| 1 | 1 | 01 | Remote | PPA |
| 1 | 1 | 10 | Remote | PS |
| 0 | 1 | 00 | Local | FPP |
| 0 | 1 | 01 | Local | PPA |
| 0 | 1 | 10 | Local | PS |

*Notes to Table 15–1:*

(1) For detailed information on standard PS, FPP, and PPA models, refer to Chapter 13, Configuring Stratix & Stratix GX Devices.

(2) In Stratix and Stratix GX devices, the `RUnLU` (remote update/local update) pin, selects between local or remote configuration mode.

(3) The `MSEL[2]` select mode selects between standard or remote system configuration mode.

### *Remote Configuration Mode*

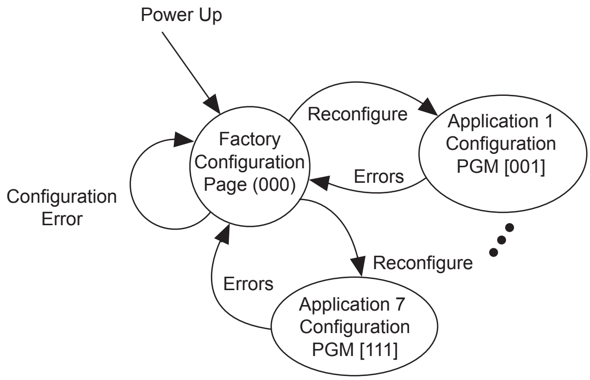
Using remote configuration mode, you can manage up to seven different application configurations for Stratix and Stratix GX devices. The seven-configuration-file limit is due to the number of pages that the `PGM[]` pins in the Stratix or Stratix GX device and enhanced configuration devices can select.

> If more than seven files are sent to a system using remote configuration mode, previous files will be overwritten.

Stratix and Stratix GX devices support remote configuration mode for PS, FPP, and PPA modes. Specify remote configuration mode by setting the `MSEL2` and `RUnLU` pins to high. (See Table 15–1).

On power-up in remote configuration mode, the Stratix or Stratix GX device loads the user-specified factory configuration file, located in the default page address `000` in the enhanced configuration device. After the device configures, the remote configuration control register points to the page address of the application configuration that should be loaded into the Stratix or Stratix GX device. If an error occurs during user mode of an application configuration, the device reloads the default factory configuration page. Figure 15–3 shows a diagram of remote configuration mode.

***Figure 15–3. Remote Configuration Mode***



## *Local Configuration Mode*

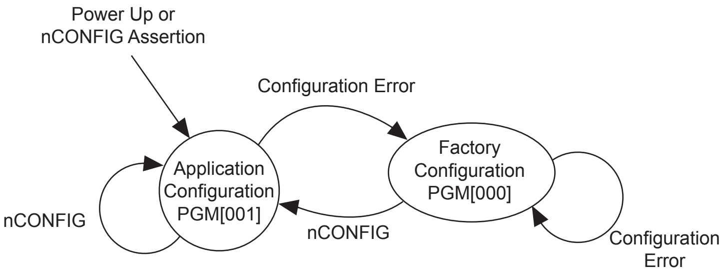
Local configuration mode—a simplified version of remote configuration mode—is suitable for systems that load an application immediately upon power-up. In this mode you can only use one application configuration, which you can update either remotely or locally.

In local configuration mode, upon power-up, or when `nCONFIG` is asserted, the Stratix or Stratix GX device loads the application configuration immediately. Factory configuration loads only if an error occurs during the application configuration's user mode. If you use an enhanced configuration device, page address `001` is the location for the application configuration data, and page address `000` is the location for the factory configuration data.

If the configuration data at page address `001` does not load correctly due to cyclic redundancy code (CRC) failure, or it times-out of the enhanced configuration device, or the external processor times-out, then the factory configuration located at the default page (page address `000`) loads into the Stratix or Stratix GX device.

In local configuration mode (shown in Figure 15–4), the user watchdog timer is disabled. For more information on the watchdog timer, see "Watchdog Timer" on page 15–7.

*Figure 15–4. Local Configuration Mode*



In local configuration mode, one application configuration is available to the device. For remote or local configuration mode selection, refer to Table 15–1.

## Remote System Configuration Components

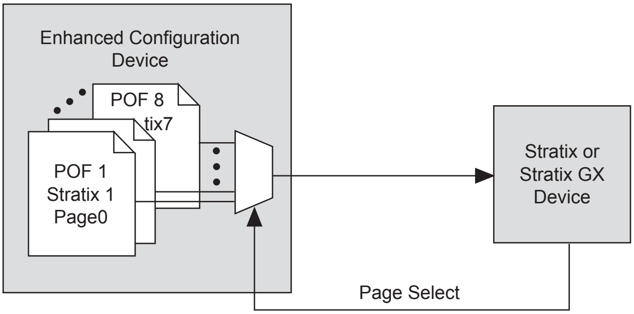
The following components are used in Stratix and Stratix GX devices to support remote and local configuration modes. A description of each component follows.

- Page mode feature
- Factory configuration
- Application configuration
- Watchdog timer
- Remote update sub-block
- Remote configuration registers

### *Page Mode Feature*

The page mode feature enables Stratix and Stratix GX devices to select a location to read back data for configuration. The enhanced configuration device can receive and store up to eight different configuration files (one factory and seven application files). Selection of pages to read from is performed through the `PGM[2..0]` pins on the Stratix or Stratix GX device and enhanced configuration devices. These pins in the Stratix or Stratix GX device can be designated user I/O pins during standard configuration mode, but in remote system configuration mode, they are dedicated output pins. Figure 15–5 shows the page mode feature in Stratix or Stratix GX devices and enhanced configuration devices.

*Figure 15–5. Page Mode Feature in Stratix or Stratix GX Devices & Enhanced Configuration Devices*



Upon power-up in remote configuration mode, the factory configuration (see description below) selects the user-specified page address through the Stratix or Stratix GX `PGM[2..0]` output pins. These pins drive the `PGM[2..0]` input pins of the enhanced configuration device and select the requested page in the memory.

If an intelligent host is used instead of an enhanced configuration device, you should create logic in the intelligent host to support page mode settings similar to that in enhanced configuration devices.

### Factory Configuration

Factory configuration is the default configuration data setup. In enhanced configuration devices, this default page address is `000`. Factory configuration data is written into the memory device only once by the system manufacturer and should not be remotely updated or altered. In remote configuration mode, the factory configuration loads into the Stratix or Stratix GX device upon power-up.

The factory configuration specifications are as follows:

- Receives new configuration data and writes it to the enhanced configuration or other memory devices
- Determines the page address for the next application configuration that should be loaded to the Stratix or Stratix GX device
- Upon an error in the application configuration, the system reverts to the factory configuration
- Determines the reason for any application configuration error
- Determines whether to enable or disable the user watchdog timer for application configurations

- Determines the user watchdog timer’s settings if the timer is enabled (remote configuration mode)
- If the user watchdog timer is not reset after a predetermined amount of time, it times-out and the system loads the factory configuration data back to the Stratix or Stratix GX device

If a system encounters an error while loading application configuration data, or if the device re-configures due to `nCONFIG` assertion, the Stratix or Stratix GX device loads the factory configuration. The remote system configuration register determines the reason for factory re-configuration. Based on this information, the factory configuration determines which application configuration needs to be loaded.

### *Application Configuration*

The application configuration is the configuration data received from the remote source and updated into different locations or pages of the memory storage device (excluding the factory default page).

### *Watchdog Timer*

A watchdog timer is a circuit that determines whether another mechanism functions properly. The watchdog timer functions like a time-delay relay that remains in the reset state while an application runs properly. This action periodically sends a reset command from the working application to the watchdog timer. Stratix and Stratix GX devices are equipped with a built-in watchdog timer for remote system configuration.

A user watchdog timer prevents a faulty application configuration from indefinitely stalling the Stratix or Stratix GX device. The timer functions as a counter that counts down from an initial value, which is loaded into the device from the factory configuration. This is a 29-bit counter, but you will use only the upper 12 bits to set the value for the watchdog timer. You specify the counter value according to your design needs.

The timer begins counting once the Stratix or Stratix GX device goes into user mode. If the application configuration does not reset the user watchdog timer after the specified time, then the timer times-out. At this point, the Stratix or Stratix GX device will be re-configured by loading the factory configuration and resetting the user watchdog timer.

☞ The watchdog timer is disabled in local configuration mode.

### *Remote Update Sub-Block*

The remote update sub-block is responsible for administrating the remote configuration feature. This sub-block, which is controlled by a remote configuration state machine, generates the control signals required to control different remote configuration registers.

### *Remote Configuration Registers*

Remote configuration registers are a series of registers required to keep track of page addresses and the cause of configuration errors. Table 15–2 gives descriptions of the registers' functions. You can control both the update and shift registers; the status and control registers are controlled by internal logic, but can be read via the shift register.

***Table 15–2. Remote Configuration Registers***

| Register | Description |
|---|---|
| Control register | This register contains the current page address, the watchdog timer setting, and one bit specifying if the current configuration is a factory or application configuration. During a capture in an application configuration, this register is read into the shift register. |
| Update register | This register contains the same data as the control register, except that it is updated by the factory configuration. The factory configuration updates the register with the values to be used in the control register on the next re-configuration. During capture in a factory configuration, this register is read into the shift register. |
| Shift register | This register is accessible by the core logic and allows the update, status, and control registers to be written and sampled by the user logic. The update register can only be updated in factory application or remote configuration. |
| Status register | This register is written into by the remote configuration block on every re-configuration to record the cause of the re-configuration. This information will be used by factory configuration to determine the appropriate action following a re-configuration. |

Figure 15–6 shows the control, update, shift, and status registers and the data path used to control remote system configuration.

*Figure 15–6. Remote Configuration Registers & Related Data Path*

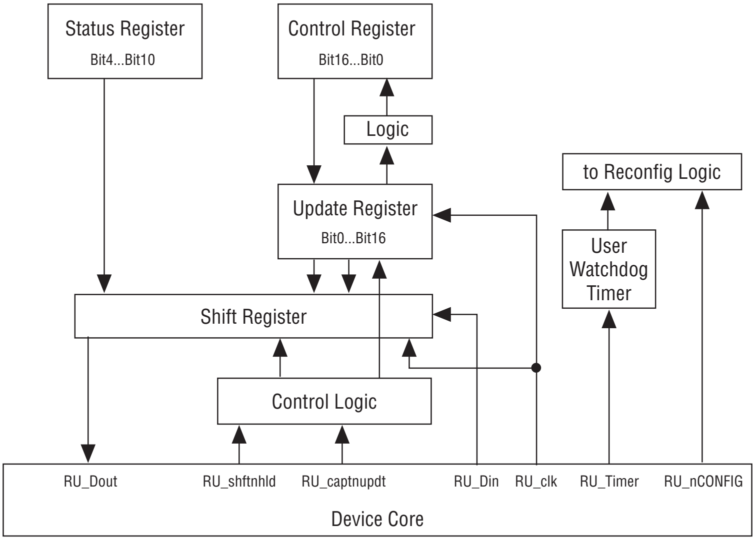


Table 15–3 describes the user configuration signals that are driven to/from the device logic array. The remote configuration logic has one input signal to the device logic array and six output signals from the device logic array.

*Table 15–3. User Configuration Signals To/From Device Core (Part 1 of 2)*

| Signal Name | To/From Device Core | Description |
|---|---|---|
| `RU_Timer` | Output from the core to the remote update block | Request from the application to reset the user watchdog timer with its initial count. A falling edge of this signal triggers a reset of the user watchdog timer. |
| `RU_nCONFIG` | Output from the core to the remote update block | When driven low, this signal triggers the device to reconfigure. If requested by the factory configuration, the application configuration specified in the remote update control register is loaded. If requested by the application configuration, the factory configuration is loaded. |
| `RU_Clk` | Output from the core to the remote update block | Clocks the remote configuration shift register so that the contents of the status and control registers can be read out, and the contents of update register can be loaded. The shift register latches data on the rising edge of the `RU_Clk`. |

*Table 15–3. User Configuration Signals To/From Device Core (Part 2 of 2)*

| Signal Name | To/From Device Core | Description |
|---|---|---|
| `RU_shftnhld` | Output from the core to the remote update block | If its value is “1”, the remote configuration shift register shifts data on the rising edge of `RU_Clk`. It its value is “0” and `RU_captnupdt` is “0”, the shift register will update the update register. If its value is “0”, and `RU_captnupdt` is “1”, the shift register will capture the status register and either the control or update register (depending on whether the configuration is factory or application). |
| `RU_captnupdt` | Output from the core to the remote update block | When `RU_captnupdt` is at value “1” and `RU_shftnhld` is at value”0”, the system specifies that the remote configuration shift register should be written with the content of the status register and either the update register (in a factory configuration) or the control register (in an application configuration). This shift register is loaded on the rising edge of `RU_Clk`. When `RU_captnupdt` is at value “0” and `RU_shftnhld` is at value”0”, the system specifies that the remote configuration update register should be written with the content of the shift register in a factory configuration. The update register is loaded on the rising edge of `RU_Clk`. This pin is enabled only for factory configuration in remote configuration mode (it is disabled for the application configuration in remote configuration or for local configuration modes). If `RU_shftnhld` is at value “1”, `RU_captnupdt` has no function. |
| `RU_Din` | Output from the core to the remote update block | Data to be written into the remote configuration shift register on the rising edge of `RU_Clk`. To load into the shift register, `RU_shftnhld` must be asserted. |
| `RU_Dout` | Input to the core from the remote update block | Output of the remote configuration shift register to be read by core logic. New data arrives on each rising edge of `RU_Clk`. |

All of the seven device core signals (see Figure 6), are enabled for both remote and local configuration for both factory and application configuration, except `RU_Timer` and `RU_captnupdt`. Figure 15–7 and Table 15–4 specify the content of control register upon power-on reset (POR).

The difference between local configuration and remote configuration is how the control register is updated during a re-configuration and which core signals are enabled.

*Figure 15–7. Remote System Configuration Control Register*

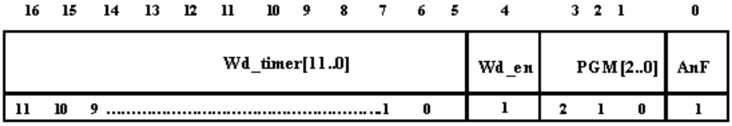


Table 15–4 shows the content of the control register upon POR.

*Table 15–4. Control Register Contents*

| Parameter | Definition | POR Reset Value | Comment |
|---|---|---|---|
| `AnF` | Current configuration is factory or applications | 1 bit ‘1’ | Applications |
| | | 1 bit ‘0’ | Factory |
| `PGM[2..0]` | Page mode selection | 3 bits ‘001’ | Local configuration |
| | | 3 bits ‘000’ | Remote configuration |
| `Wd_en` | User watchdog timer enable | 1 bit ‘0’ | – |
| `Wd_timer [11..0]` | User watchdog timer time-out value | 12 bits ‘0’ | High order bits of 29 bit counter |

The status register specifies the reason why re-configuration has occurred and determines if the re-configuration was due to a `CRC` error, `nSTATUS` pulled low due to an error, the device core caused an error, `nCONFIG` was reset, or the watchdog timer timed-out. Figure 15–8 and Table 15–5 specify the content of the status register.

*Figure 15–8. Remote System Configuration Status Register*

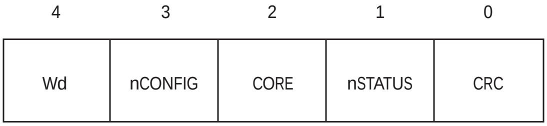


Table 15–5 shows the content of the status register upon POR.

*Table 15–5. Status Register Contents*

| Parameter | Definition | POR Reset Value |
|---|---|---|
| `CRC` (from configuration) | `CRC` caused re-configuration | 1 bit '0' |
| `nSTATUS` | `nSTATUS` caused re-configuration | 1 bit '0' |
| `CORE` *(1)* | Device core caused re-configuration | 1 bit '0' |
| `nCONFIG` | `NCONFIG` caused re-configuration | 1 bit '0' |
| `Wd` | Watchdog Timer caused re-configuration | 1 bit '0' |

*Note to Table 15–5:*

(1) Core re-configuration enforces the system to load the application configuration data into the Stratix or Stratix GX device. This occurs after factory configuration specifies the appropriate application configuration data.

## Quartus II Software Support

The Quartus II software version 2.1 supports remote and local configuration modes. To access Stratix and Stratix GX devices for remote configuration with the Quartus II software version 2.1, insert a what-you-see-is-what-you-get (WYSIWYG) atom into the design. Without this ATOM, you will not be able to access the Stratix or Stratix GX device core and perform remote configuration with the Quartus II software.

To specify in the software that a remote or local configuration is planned, select the remote or local update mode under Compiler Settings, prior to the compilation. This selection will reserve the `RUnLU` and `PGM` pins for remote/local configuration.

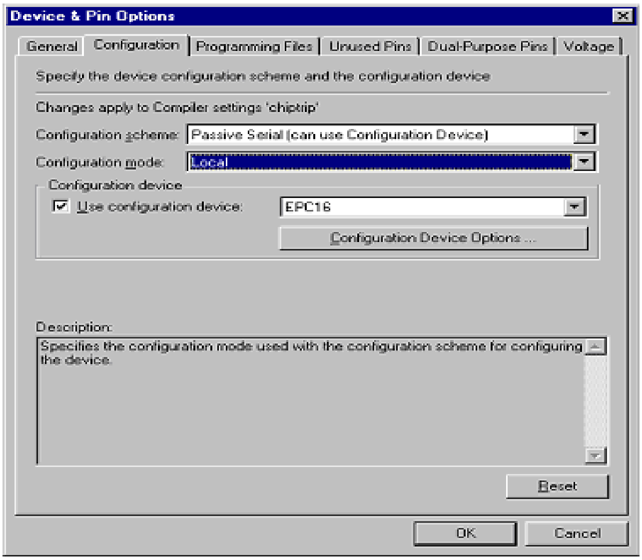
### Quartus II Support for Local Configuration Scheme

To set the local configuration scheme, follow these steps:

1. Click the **Chips & Devices** tab in the **Compiler Settings** dialog box (**Processing** menu). The **Compiler Settings** dialog box is displayed.
2. Click the **Device & Pin Options** button. The **Device & Pin Options** dialog box is displayed.
3. Click the **Configuration** tab.
4. In the **Configuration mode** list, select **Local**.

Figure 15–9 shows the **Device & Pin Options** dialog box. After compilation, the Quartus II software will reserve `RUnLU`, along with other configuration pins. For local configuration, the `MSEL[2]` pin should be connected to `VCC`, and the `RUnLU` pin should be connected to `GND` (see Table 15–1).

*Figure 15–9. Compiler Setting for Local Configuration Scheme*



Device & Pin Options

Specify the device configuration scheme and the configuration device

Changes apply to Compiler settings 'chiptrip'

Configuration scheme: Passive Serial (can use Configuration Device)

Configuration mode: Local

Configuration device

☑ Use configuration device: EPC16

Description:

Specifies the configuration mode used with the configuration scheme for configuring the device.

### Local Configuration Set-Up

To target an enhanced configuration device for remote and local configuration, the SRAM Object File (**.sof**) should convert to a Programming Object File (**.pof**) or Hexadecimal File (**.hex**) format, by following these steps:

1. Go to **Convert Programming File** (Tools menu).
2. Select “Programming Object File (.pof)” from the drop-down list under **Programming file type**.
3. Select “EPC16 (or EPC8)” from the drop-down list under **Configuration device**.
4. Select the required configuration mode (“1-bit Passive Serial” or “Fast Passive Parallel”) from the drop-down menu under **Mode**.

5. In the **File name** box, type the POF file name for the factory page. (The first conversion is for the factory configuration file, which resides at `page0` of the enhanced configuration device.)

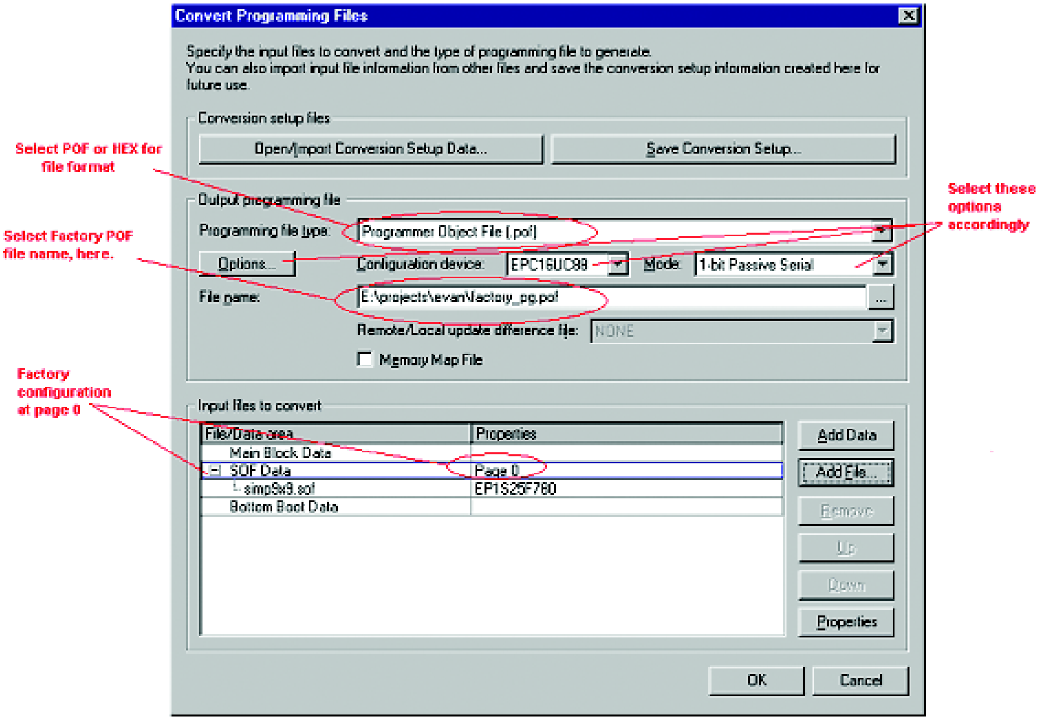
6. Click **Options** and select any required settings (such as compression mode, clock setting, and so on). Only during the factory configuration file conversion can you specify the **Options**, **Configuration device**, or **Mode** settings. While generating the application configuration file, all of these settings are grayed out and inaccessible.

7. In the **Input files to convert** box, highlight "SOF Data" at "Page0" and click **Add File**.

8. Click **OK**. This will generate the POF for the factory image at "Page 0".

Figure 15–10 shows the options in the **Convert Programming Files** dialog box for the factory configuration file in local configuration scheme.

*Figure 15–10. Factory Configuration Set-Up in Local Configuration Scheme*



Convert Programming Files

Specify the input files to convert and the type of programming file to generate. You can also import input file information from other files and save the conversion setup information created here for future use.

Conversion setup files

Output programming file

Programming file type: Programmer Object File (.pof)

Configuration device: EPC16UC88

Mode: 1-bit Passive Serial

File name: E:\projects\evan\factory_pg.pof

Remote/Local update difference file: NONE

☐ Memory Map File

Input files to convert

| File/Data area | Properties |
|---|---|
| Main Block Data | |
| − SOF Data | Page 0 |
| simp9x9.sof | EP1S25F780 |
| Bottom Boot Data | |

Select POF or HEX for file format

Select Factory POF file name, here.

Factory configuration at page 0

Select these options accordingly

To add the application configuration file to the next page in the enhanced configuration device, perform the following steps:

1. Open the **Convert Programming Files** dialog box (Tools menu).

2. Under **Programming file type** select "Programmer Object File for Local Update (.pof)". The **Options**, **Configuration device**, and **Mode** settings are grayed out and inaccessible for application configuration because these settings are for the factory configuration file.

3. There is an optional selection called **Remote/Local update Difference file**. This box will be available only when "Programmer Object File for Local Update (.pof)" or "Programmer Object File for Remote Update (.pof)" is selected. For local update, the difference file contains the data added to page 1 of a POF. The output difference file can be in **.hexout**, **.jbc** or **.jam** file format.

4. Go to **Input files to convert** and highlight the "SOF Data" at "Page 1" and click **Add File**. This will load the application configuration data at page 1.

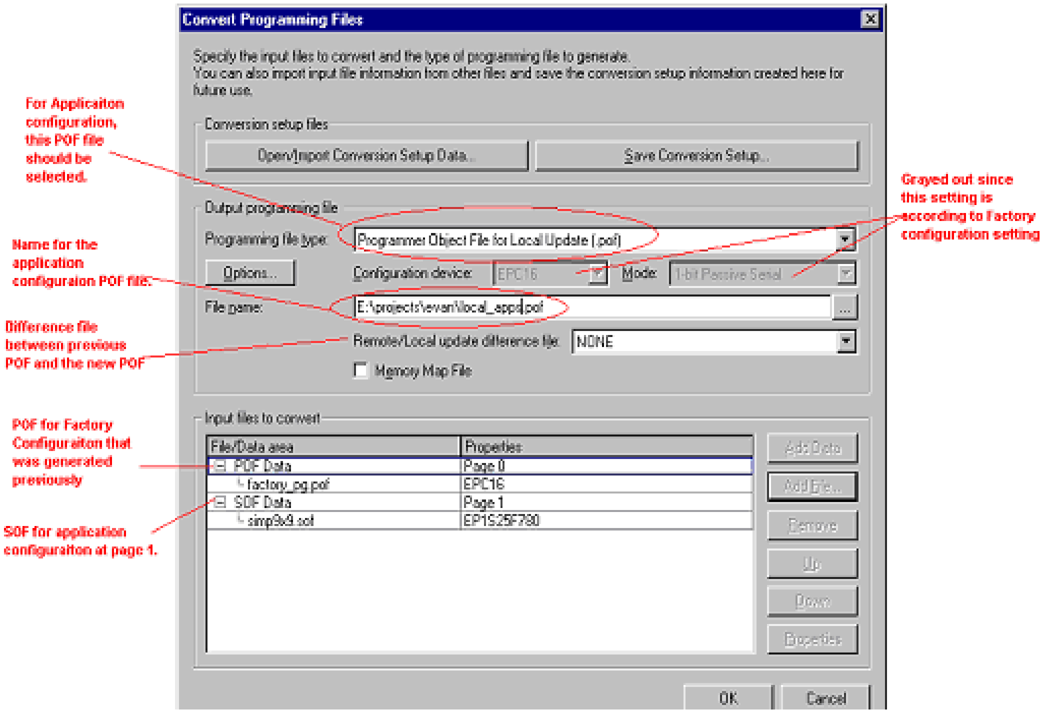
5. Highlight "POF Data" at "Page 0" and click **Add File**. Select the POF file generated for the factory configuration at "Page 0".

6. After uploading both programming files, specify a name for this new POF file in the **File Name** box.

7. Click **OK** to generate the POF file.

Figure 15–11 shows the **Convert Programming File** dialog box and its various selections for the application configuration file in local update.

*Figure 15–11. Application Configuration Set-Up in Local Configuration Scheme*



Specify the input files to convert and the type of programming file to generate.
You can also import input file information from other files and save the conversion setup information created here for future use.

Programming file type: Programmer Object File for Local Update (.pof)

Configuration device: EPC16

Mode: 1-bit Passive Serial

File name: E:\projects\evan\local_apps.pof

Remote/Local update difference file: NONE

☐ Memory Map File

| File/Data area | Properties |
|---|---|
| ⊟ POF Data | Page 0 |
| factory_pg.pof | EPC16 |
| ⊟ SOF Data | Page 1 |
| simp9x9.sof | EP1S25F780 |

For Applicaiton configuration, this POF file should be selected.

Name for the application configuraion POF file.

Difference file between previous POF and the new POF

POF for Factory Configuraiton that was generated previously

SOF for application configuraiton at page 1.

Grayed out since this setting is according to Factory configuration setting

## Quartus II Support for Remote Configuration Scheme

When using the remote configuration scheme in the Quartus II software version 2.1, add the remote update WYSIWYG atom to your design in order to access the core of the Stratix or Stratix GX device. This atom should be included in the factory configuration design or any other application configuration designs that need to enable this scheme. Without this atom, you will not be able to use this scheme.

### *Remote Update WYSIWYG Atom*

This section describes the remote update WYSIWYG atom in detail. The following items should be considered when implementing the atom:

1. Only one atom can be used in the circuit; more than one will give a no-fit.

2. All signals for the cell must be connected. The clock port (`CLK`) must be connected to a live cell. The others can be constant `VCC` or `GND`.

3. The `pgmout` port must be connected and must feed `PGM[2.0]` output pins (it cannot be connected to anything else but output pins).

4. The Quartus II software will reserve `RUnLU` as an input pin, and you must connect it to `VCC`.

### *Remote Update Primitives*

The following shows the remote update primitives:

**Stratix_rublock** <*rublock_name*>
(
**.clk(**<*clock source*>**),**
**.shiftnld(**<*shiftnld source*>**),**
**.captnupdt(**<*shiftnld source*>**),**
**.regin(<***regin input source from the core*>**)**,
**.rsttimer**(<*input signal to reset the watchdog timer*>**),**
**.config**(<*input signal to initiate configuration*>**)**,
**.regout(**<*data output destination to core*>**),**
**.pgmout(<***program output destinations to pins*>**)**,
);

Table 15–6 shows the remote update block input and output port names and descriptions of each.

*Table 15–6. Remote Update Block Input & Output Ports (Part 1 of 2)*

| Ports | Definition |
|---|---|
| <*rublock_name*> | The unique identifier for the instance. This identifier name can be anything as long as it is legal for the given description language (i.e., Verilog, VHDL, AHDL, etc.). This field is required. |
| **.clk**(<*clock source*>) | Designates the clock input of this cell. All operation is with respect to the rising edge of this clock. This field is required. |
| **.shiftnld**(<*shiftnld source*>) | An input into the remote configuration block. When .**shiftnld** = 1, the data shifts from the internal shift registers to the `regout` port at each rising edge of `clk`, and the data also shifts into the internal shift registers from `regin` port. This field is required. |
| **.captnupdt**(<*shiftnld source*>) | An input into the remote configuration block. This controls the protocol of when to read the configuration mode or when to write into the registers that control the configuration. This field is required. |
| **.regin**(<*regin input source from the core*>) | An input into the configuration block for all data loading into the core. The data shifts into the internal registers at the rising edge of `clk`. This field is required. |

***Table 15–6. Remote Update Block Input & Output Ports (Part 2 of 2)***

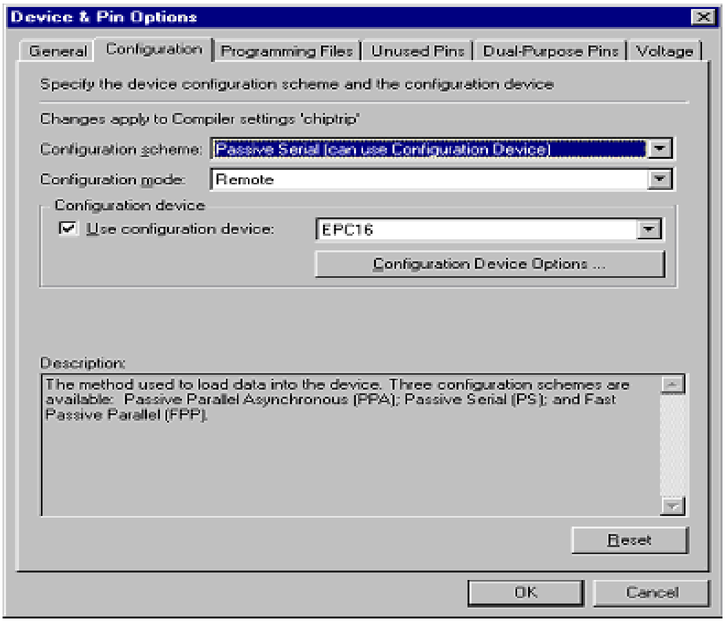
| Ports | Definition |
|---|---|
| **.rsttimer**(<*input signal to reset the watchdog timer*>) | An input into the watchdog timer of the remote update block. When this is high, it resets the watchdog timer. This field is required. |
| **.config**(<*input signal to initiate configuration*>) | An input into the configuration section of the remote update block. When this signal goes high, the part initiates a re-configuration. This field is required. |
| **.regout**(<*data output destination to core*>) | A 1-bit output, which is the output of the internal shift register, and updated every rising edge of `clk`. The data coming out depends on the control signals. This field is required. |
| **.pgmout**(<*program output destinations to pins*>) | A 3-bit bus. It should always be connected only to output pins (not `bidir` pins). This bus gives the page address (000 to 111) of the configuration data to be loaded when the device is getting configured. This field is required. |

For more information on the control signals for the remote update block see Table 15–3 on page 15–9.

### *Remote Configuration Set Up*

For remote configuration, select **Remote** under **Configuration mode** in the **Configuration** tab located in the **Device & Pin Options** dialog box (Processing menu). Figure 15–12 shows the **Device & Pin Options** dialog box. After compilation, the Quartus II software will reserve `RUnLU`, along with other configuration pins. For remote configuration scheme, both `MSEL[2]` and the `RUnLU` pins should be connected to `VCC` (see Table 15–1).

*Figure 15–12. Compiler Setting for Remote Configuration Scheme*



Specify the device configuration scheme and the configuration device

Changes apply to Compiler settings 'chiptrip'

Configuration scheme: Passive Serial (can use Configuration Device)

Configuration mode: Remote

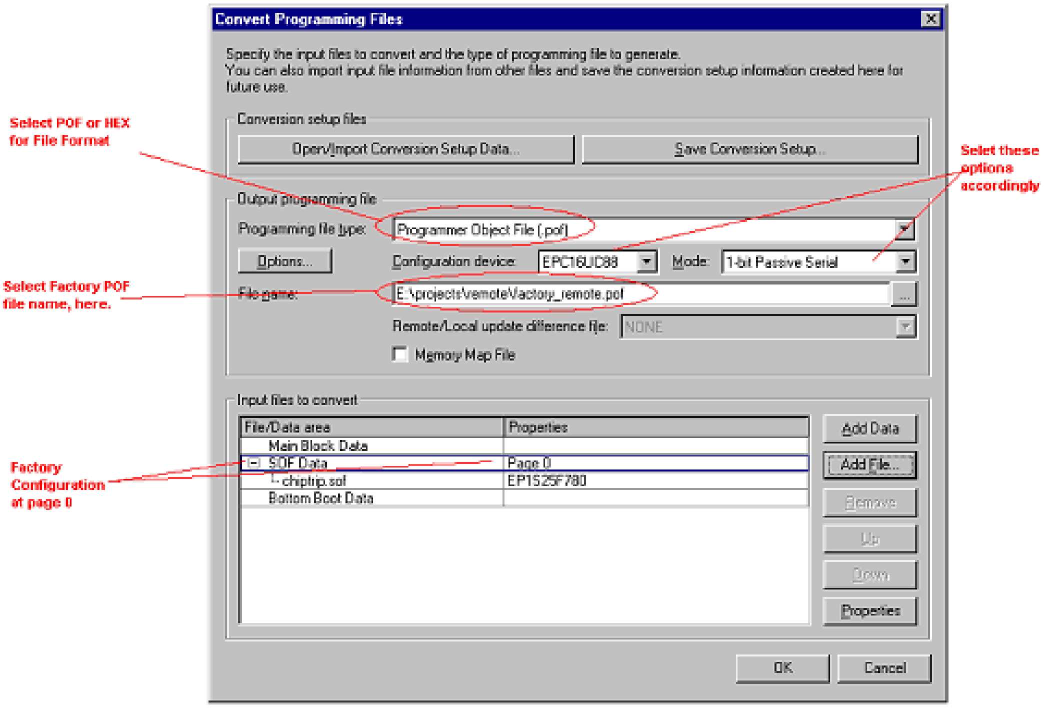
☑ Use configuration device: EPC16

The method used to load data into the device. Three configuration schemes are available: Passive Parallel Asynchronous (PPA); Passive Serial (PS); and Fast Passive Parallel (FPP).

To target an enhanced configuration device for remote and local configuration, follow the steps found under the section, "Local Configuration Set-Up" on page 15–13.

Figure 15–13 shows the options in the **Convert Programming Files** dialog box for the factory configuration file in remote configuration scheme.

*Figure 15–13. Factory Configuration Set-Up in Remote Configuration Scheme*



Select POF or HEX for File Format

Select Factory POF file name, here.

Factory Configuration at page 0

Selet these options accordingly

Convert Programming Files

Specify the input files to convert and the type of programming file to generate.
You can also import input file information from other files and save the conversion setup information created here for future use.

Conversion setup files

Output programming file

Programming file type: Programmer Object File (.pof)

Configuration device: EPC16UC88

Mode: 1-bit Passive Serial

File name: E:\projects\remote\factory_remote.pof

Remote/Local update difference file: NONE

☐ Memory Map File

Input files to convert

| File/Data area | Properties |
|---|---|
| Main Block Data | |
| SOF Data | Page 0 |
| chiptrip.sof | EP1S25F780 |
| Bottom Boot Data | |

To add the application configuration file (or files) to the next page in the enhanced configuration device, perform the following steps:

1. Open the **Convert Programming Files** dialog box (Tools menu).

2. Under **Programming file type** select “Programmer Object File for Local Update (.pof)”. The **Options**, **Configuration device**, and **Mode** settings are grayed out and inaccessible for application configuration because these settings are for the factory configuration file.

3. There is an optional selection called **Remote/Local update Difference file**. This box will be available only when “Programmer Object File for Local Update (.pof)” or “Programmer Object File for Remote Update (.pof)” is selected. For remote update, the difference file contains the data for new pages added to a POF. The output difference file can be in **.hexout**, **.jbc** or **.jam** file format.

4. Go to **Input files to convert** and highlight the "SOF Data" at "Page 1" and click **Add File**. This will load the application configuration data at page 1.

5. If there is more than one applications configuration file, repeat step 4 for all the existing files. When adding a new SOF, click **Properties** in the **Convert Programming Files** dialog box and specify the page that the file should load to.

☞ Keep in mind the density of the targeted enhanced configuration devices and the number of programming files allowed for that density. If you exceed the device's capacity, an error message will appear: "Size of file/s in main block exceed memory capacity".

6. Highlight "POF Data" at "Page 0" and click **Add File**. Select the POF file generated for the factory configuration at "Page 0".

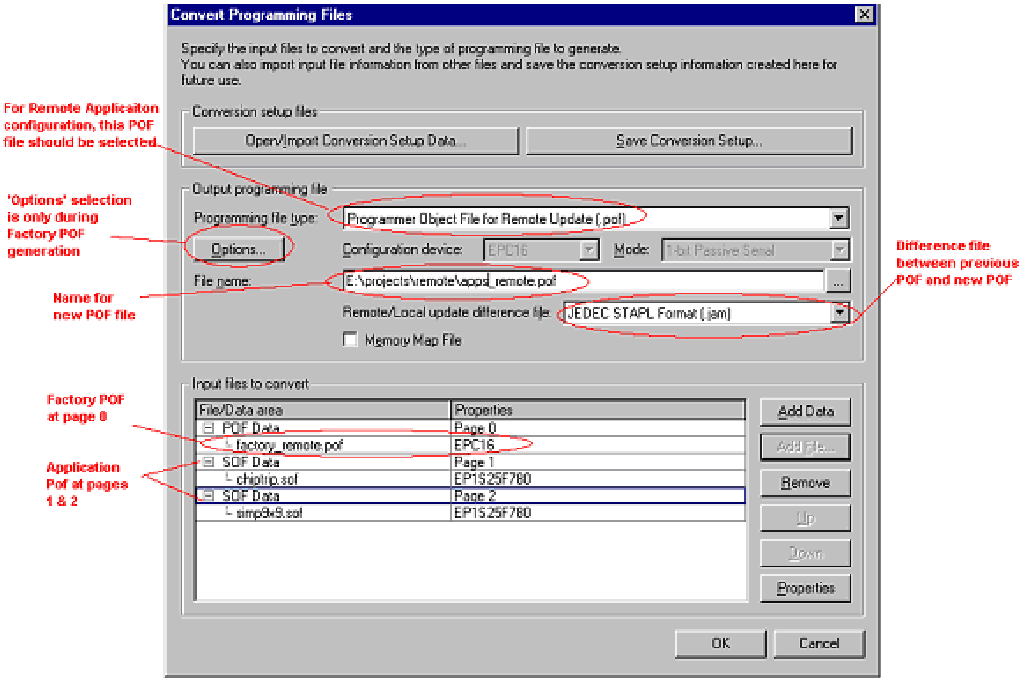
7. After uploading both programming files, specify a name for this new POF file in the **File Name** box.

8. Click **OK** to generate the POF file.

If the **Compression** option is not selected while generating factory POF file, you may not be able to fit more than one or two programming files in the enhanced configuration device.

Figure 15–14 shows the **Convert Programming Files** dialog box for three configuration files in remote configuration scheme. For this setup, the **Compression** option is selected during factory configuration POF generation.

*Figure 15–14. Application Configuration Set-Up in Remote Configuration Mode*



Convert Programming Files

Specify the input files to convert and the type of programming file to generate.
You can also import input file information from other files and save the conversion setup information created here for future use.

Conversion setup files

Output programming file

Programming file type: Programmer Object File for Remote Update (.pof)

Configuration device: EPC16

Mode: 1-bit Passive Serial

File name: E:\projects\remote\apps_remote.pof

Remote/Local update difference file: JEDEC STAPL Format (.jam)

☐ Memory Map File

Input files to convert

| File/Data area | Properties |
|---|---|
| ⊟ POF Data | Page 0 |
| └ factory_remote.pof | EPC16 |
| ⊟ SOF Data | Page 1 |
| └ chiptrip.sof | EP1S25F780 |
| ⊟ SOF Data | Page 2 |
| └ simp9x9.sof | EP1S25F780 |

For Remote Applicaiton configuration, this POF file should be selected.

'Options' selection is only during Factory POF generation

Name for new POF file

Factory POF at page 0

Application Pof at pages 1 & 2

Difference file between previous POF and new POF

## Using Enhanced Configuration Devices

This section describes remote system configuration of Stratix and Stratix GX devices with the Nios embedded processor using enhanced configuration devices. Enhanced configuration devices are composed of a standard flash memory and a controller. The flash memory stores configuration data, and the controller reads and writes to the flash memory.

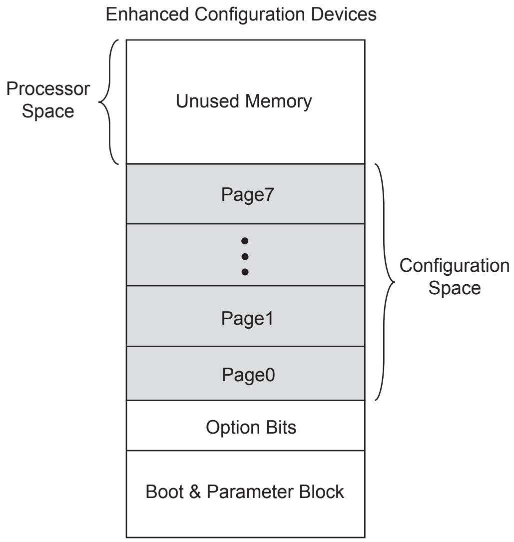
In remote system configuration, only PS and FPP modes are supported using an enhanced configuration device. A Stratix or Stratix GX device running a Nios embedded processor can receive data from a remote source through a network or any other appropriate media. A specific page of the enhanced configuration device stores the received data.

This scheme uses the page mode option in Stratix and Stratix GX devices. Up to eight pages can be stored in each enhanced configuration device, each of which can store a configuration file.

In enhanced configuration devices, a page is a section of the flash memory space. Its boundary is determined by the Quartus II software (the page size is programmable). In the software, you can specify which configuration file should be stored in which page within the flash memory. To access the configuration file on each page, set the three input pins (`PGM[2..0]`), which provide access to all eight pages. Because the `PGM[2..0]` pins of an enhanced configuration device connect to the same pins of the Stratix or Stratix GX device, the Stratix or Stratix GX device selects one of the eight memory pages as a target location to read from. Figure 15–15 shows the allocation of different pages in the enhanced configuration device.

For more information on enhanced configuration devices, refer to the *Enhanced Configuration Devices (EPC4, EPC8 & EPC16) Data Sheet* and Chapter 14, Using Altera Enhanced Configuration Devices.

*Figure 15–15. Memory Map in Enhanced Configuration Device*

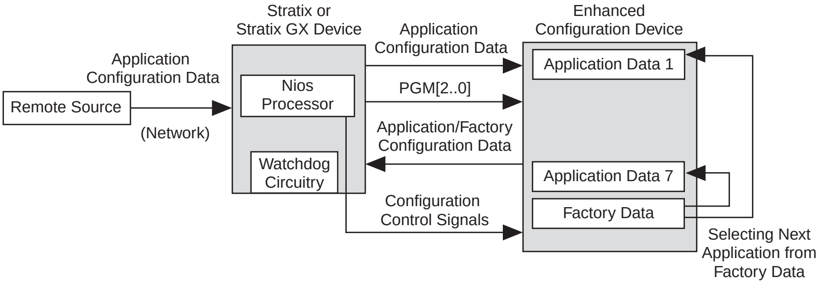


When the Stratix or Stratix GX device powers-up in remote configuration mode, the devices loads configuration data located at page address `000`. You should always load the factory default configuration data at this location and make sure this information is not altered.

The factory configuration contains information to determine the next application configuration to load into the Stratix or Stratix GX device. When the Stratix or Stratix GX device successfully loads the application configuration from the page selected by the `PGM[2..0]` pins, it enters user mode.

In user mode, the Nios embedded processor (or any other logic) assists the Stratix or Stratix GX device in detecting remote system configuration information. In remote system configuration, the Nios embedded processor receives the incoming data from the remote source via the network, writes it to the ECP16 enhanced configuration device, and then initiates loading of the factory configuration into the Stratix or Stratix GX device. Factory configuration reads the remote configuration status register and determines the appropriate application configuration to load into the Stratix or Stratix GX device. Figure 15–16 shows the remote system configuration.

*Figure 15–16. Remote System Configuration Using Enhanced Configuration Devices*



The user watchdog timer in Stratix and Stratix GX devices ensures that an application configuration has loaded successfully and checks if the application configuration is operating correctly in user mode. The watchdog timer must be continually reset by the user logic. If an error occurs while the application configuration loads, or if the watchdog timer times-out during user mode, the factory configuration is reloaded to prevent the system from halting in an erroneous state. Figure 15–3 on page 15–4 illustrates the remote configuration mode.

Upon power-up in local configuration scheme, the application configuration at page `001` (`PGM[001]` of the enhanced configuration device) loads into the Stratix or Stratix GX device. This application can be remotely or locally updated. If an error occurs during loading of the configuration data, the factory configuration loads automatically (see Figure 15–4 on page 15–5). The rest is identical to remote configuration mode.

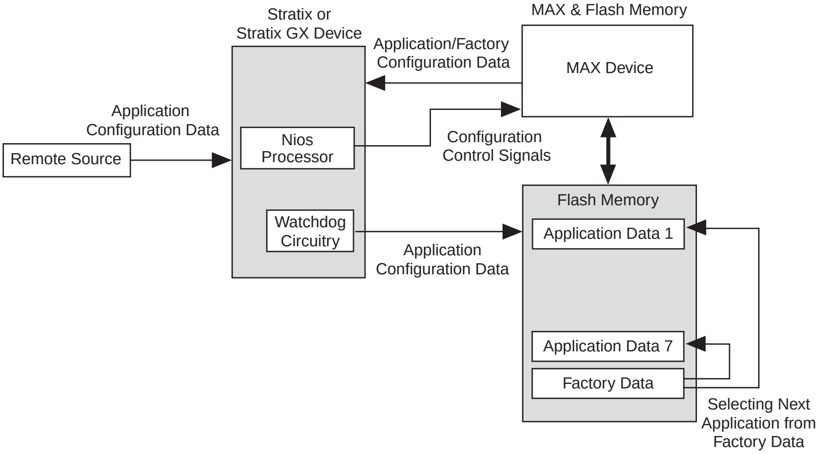
## Combining MAX Devices & Flash Memory

This section describes remote system configuration with the Stratix or Stratix GX device and the Nios embedded processor, using a combination of MAX® devices and flash memory.

You can use MAX 3000 or MAX 7000 devices and an industry-standard flash memory device instead of enhanced configuration devices. In this scheme, flash memory stores configuration data, and the MAX device controls reading and writing to the flash memory, keeping track of address locations.

The MAX device determines which address location and at what length to store configuration data in flash memory. The Nios embedded processor, running in the Stratix or Stratix GX device, receives the incoming data from the remote source and writes it to the address location in flash memory. The Nios embedded processor initiates loading of factory configuration into the Stratix or Stratix GX device. Figure 15–17 shows remote system configuration using a MAX device and flash memory combination.

*Figure 15–17. Remote System Configuration Using a MAX Device & Flash Memory*



You can use both remote and local configuration modes in this scheme. You should specify a default page for factory configuration and make sure it is not altered or removed at any time. In remote system configuration mode, PS, FPP, and PPA modes are supported when configuring with MAX and flash devices.

## Using an External Processor

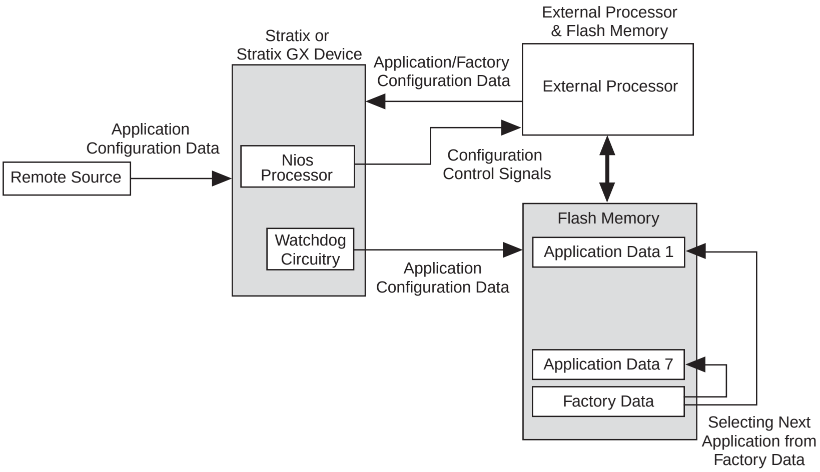
This section describes remote system configuration with Stratix or Stratix GX devices and the Nios embedded processor, using an external processor and flash memory devices.

In this scheme, the external processor and flash memory device replace the enhanced configuration device. Flash memory stores configuration data, and the processor controls reading and writing to the flash memory and also keeps track of the address location. This type of remote system configuration supports PS, FPP, and PPA modes.

The processor determines at which address which length to store the configuration data in flash memory. The Nios embedded processor receives the incoming data from a remote source and writes it to the address location in the flash memory, and then initiates loading of factory configuration data into the Stratix or Stratix GX device. Figure 15–18 shows the remote system configuration using a Nios embedded processor and flash memory.

You can use both remote and local configuration modes in this scheme. You should specify a default page for factory configuration and make sure it is not altered or removed at any time.

*Figure 15–18. Remote System Configuration Using External Processor & Flash Memory*



## Conclusion

Stratix and Stratix GX devices are the first PLDs with dedicated support for remote system configuration. By allowing real-time system upgrades from a remote source, you can use Stratix and Stratix GX devices in a variety of applications that require automatic configuration updates. With the built-in watchdog timer circuitry, Stratix and Stratix GX devices avoid incorrect or erroneous states. Using Stratix and Stratix GX devices with remote system configuration enhances design flexibility and reduces time to market.

# Index

# Stratix Device Handbook, Volume 3

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# Contents

## Section I. Device Pin Information

### Chapter 1. Stratix EP1S10 Device Pin Information

### Chapter 2. Stratix EP1S20 Device Pin Information

### Chapter 3. Stratix EP1S25 Device Pin Information

### Chapter 4. Stratix EP1S30 Device Pin Information

### Chapter 5. Stratix EP1S40 Device Pin Information

## Section II. PCB Layout Guidelines

# Chapter Revision Dates

The chapters in this book, *Stratix Device Handbook, Volume 2*, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

Chapter 1. Stratix EP1S10 Device Pin Information
Revised: *April 2003*
Part number: *S5V3001-1.0*

Chapter 2. Stratix EP1S20 Device Pin Information
Revised: *April 2003*
Part number: *S5V3002-1.0*

Chapter 3. Stratix EP1S25 Device Pin Information
Revised: *April 2003*
Part number: *S5V3003-1.0*

Chapter 4. Stratix EP1S30 Device Pin Information
Revised: *April 2003*
Part number: *S5V3004-1.0*

Chapter 5. Stratix EP1S40 Device Pin Information
Revised: *April 2003*
Part number: *S5V3005-1.0*

Chapter 6. Stratix EP1S60 Device Pin Information
Revised: *April 2003*
Part number: *S5V3006-1.0*

Chapter 7. Stratix EP1S80 Device Pin Information
Revised: *April 2003*
Part number: *S5V3007-1.0*

Chapter 8. Package Information for Stratix Devices
Revised: *April 2003*
Part number: *S5V3008-1.0*

Chapter 9. Designing with FineLine BGA Packages
Revised: *April 2003*
Part number: *S5V3009-1.0*

# About this Handbook

This handbook provides comprehensive information about the Altera® Stratix family of devices.

## How to Find Information

You can find more information in the following ways:

- The Adobe Acrobat Find feature, which searches the text of a PDF document. Click the binoculars toolbar icon to open the Find dialog box.
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***Note to table:***

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# Typographic Conventions

This document uses the typographic conventions shown below.

| Visual Cue | Meaning |
|---|---|
| **Bold Type with Initial Capital Letters** | Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: **Save As** dialog box. |
| **bold type** | External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: $\mathbf{f_{MAX}}$, **\qdesigns** directory, **d:** drive, **chiptrip.gdf** file. |
| *Italic Type with Initial Capital Letters* | Document titles are shown in italic type with initial capital letters. Example: *AN 75: High-Speed Board Design.* |
| *Italic type* | Internal timing parameters and variables are shown in italic type. Examples: $t_{PIA}$, $n + 1$.<br>Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: <*file name*>, <*project name*>**.pof** file. |
| Initial Capital Letters | Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu. |
| “Subheading Title” | References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: “Typographic Conventions.” |
| `Courier type` | Signal and port names are shown in lowercase Courier type. Examples: `data1`, `tdi`, `input.` Active-low signals are denoted by suffix `n`, e.g., `resetn`.<br>Anything that must be typed exactly as it appears is shown in Courier type. For example: `c:\qdesigns\tutorial\chiptrip.gdf`. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword `SUBDESIGN`), as well as logic function names (e.g., `TRI`) are shown in Courier. |
| 1., 2., 3., and<br>a., b., c., etc. | Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure. |
| ■ ● • | Bullets are used in a list of items when the sequence of the items is not important. |
| ✓ | The checkmark indicates a procedure that consists of one step only. |
| ☞ | The hand points to information that requires special attention. |
| ↵ | The angled arrow indicates you should press the Enter key. |
| 👣 | The feet direct you to more information on a particular topic. |

# Section I. Device Pin Information

This section provides information for board layout designers to successfully layout their boards for Stratix devices. They contain the required PCB layout guidelines, device pin tables, and package specifications.

This section contains the following chapters:

- Chapter 1. Stratix EP1S10 Device Pin Information
- Chapter 2. Stratix EP1S20 Device Pin Information
- Chapter 3. Stratix EP1S25 Device Pin Information
- Chapter 4. Stratix EP1S30 Device Pin Information
- Chapter 5. Stratix EP1S40 Device Pin Information
- Chapter 6. Stratix EP1S60 Device Pin Information
- Chapter 7, Stratix EP1S80 Device Pin Information

## Revision History

The table below shows the revision history for Chapter 9.

| Chapter(s) | Date / Version | Changes Made |
|---|---|---|
| 7 | August 2001<br>v1.1 | Updated Table 9–6. |
|  | v1.03 | Updated the “PCB Layout for FineLine BGA Packages” section and Table 9–6. |
|  | v1.02 | Minor updates. |
|  | v1.01 | Updated Table 9–6. |
| 1 through 7 | April 2003<br>v.1.0 | Split Pin Information from Volume 1 into Volume 3 |

# 1. Stratix EP1S10 Device Pin Information

S5V3001-1.0

## Introduction

The following tables contain pin information for the Stratix EP1S10 device, organized into the following sections:

# Pin List

Table 1–1 shows the complete pin list for the EP1S10 device.

*Table 1–1. Pin List for the Stratix EP1S10 Device (Part 1 of 39)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **484-Pin Fineline BGA** | **672-Pin BGA** | **672-Pin Fineline BGA** | **780-Pin FineLine BGA** | **DQS for x32** | **DIFFIO Speed** *Note (1)* |
| IO | DIFFIO_RX21p | | B2 | VREF0B2 | D22 | C1 | C1 | G27 | | HIGH |
| IO | DIFFIO_RX21n | | B2 | VREF0B2 | D21 | D2 | D2 | G28 | | HIGH |
| IO | DIFFIO_TX21p | | B2 | VREF0B2 | E19 | E3 | E3 | K21 | | HIGH |
| IO | DIFFIO_TX21n | | B2 | VREF0B2 | E20 | E4 | E4 | K22 | | HIGH |
| IO | DIFFIO_RX20p/RUP2 | | B2 | VREF0B2 | E21 | K4 | K4 | H26 | | HIGH |
| IO | DIFFIO_RX20n/RDN2 | | B2 | VREF0B2 | E22 | K3 | K3 | H25 | | HIGH |
| IO | DIFFIO_TX20p | | B2 | VREF0B2 | | F3 | F3 | L22 | | HIGH |
| IO | DIFFIO_TX20n | | B2 | VREF0B2 | F18 | F4 | F4 | L21 | | HIGH |
| IO | DIFFIO_RX19p | | B2 | VREF0B2 | | F1 | F1 | H27 | | HIGH |
| IO | DIFFIO_RX19n | | B2 | VREF0B2 | | F2 | F2 | H28 | | HIGH |
| IO | DIFFIO_TX19p | | B2 | VREF0B2 | | G5 | G5 | L23 | | HIGH |
| IO | DIFFIO_TX19n | | B2 | VREF0B2 | G18 | G6 | G6 | L24 | | HIGH |
| VREF0B2 | | | B2 | VREF0B2 | H18 | H8 | H8 | E24 | | |
| IO | DIFFIO_RX18p | | B2 | VREF0B2 | | G1 | G1 | J25 | | HIGH |
| IO | DIFFIO_RX18n | | B2 | VREF0B2 | J17 | G2 | G2 | J26 | | HIGH |
| IO | DIFFIO_TX18p | | B2 | VREF0B2 | G19 | G3 | G3 | L20 | | HIGH |
| IO | DIFFIO_TX18n | | B2 | VREF0B2 | G20 | G4 | G4 | L19 | | HIGH |
| IO | DIFFIO_RX17p | | B2 | VREF0B2 | | K6 | K6 | J27 | | HIGH |
| IO | DIFFIO_RX17n | | B2 | VREF0B2 | | K5 | K5 | J28 | | HIGH |
| IO | DIFFIO_TX17p | | B2 | VREF0B2 | | H3 | H3 | M22 | | HIGH |

**Table 1–1. Pin List for the Stratix EP1S10 Device (Part 2 of 39)**

| Device | | | | | Package | | | | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **484-Pin Fineline BGA** | **672-Pin BGA** | **672-Pin Fineline BGA** | **780-Pin FineLine BGA** | | |
| IO | DIFFIO_TX17n | | B2 | VREF0B2 | J19 | H4 | H4 | M21 | | HIGH |
| IO | DIFFIO_RX16p | | B2 | VREF0B2 | | L3 | L3 | K26 | | HIGH |
| IO | DIFFIO_RX16n | | B2 | VREF0B2 | | L2 | L2 | K25 | | HIGH |
| IO | DIFFIO_TX16p | | B2 | VREF0B2 | | L5 | L5 | M24 | | HIGH |
| IO | DIFFIO_TX16n | | B2 | VREF0B2 | H17 | L4 | L4 | M23 | | HIGH |
| IO | DIFFIO_RX15p | | B2 | VREF1B2 | | | | K27 | | HIGH |
| IO | DIFFIO_RX15n | | B2 | VREF1B2 | | | | K28 | | HIGH |
| IO | DIFFIO_TX15p | | B2 | VREF1B2 | H19 | L7 | L7 | M20 | | HIGH |
| IO | DIFFIO_TX15n | | B2 | VREF1B2 | H20 | L6 | L6 | M19 | | HIGH |
| IO | DIFFIO_RX14p | | B2 | VREF1B2 | F21 | M6 | M6 | L25 | | HIGH |
| IO | DIFFIO_RX14n | | B2 | VREF1B2 | F22 | M7 | M7 | L26 | | HIGH |
| IO | DIFFIO_TX14p | | B2 | VREF1B2 | | | | N26 | | HIGH |
| IO | DIFFIO_TX14n | | B2 | VREF1B2 | K17 | | | N25 | | HIGH |
| IO | DIFFIO_RX13p | | B2 | VREF1B2 | G22 | M4 | M4 | L27 | | HIGH |
| IO | DIFFIO_RX13n | | B2 | VREF1B2 | G21 | M5 | M5 | L28 | | HIGH |
| IO | DIFFIO_TX13p | | B2 | VREF1B2 | L17 | | | N24 | | HIGH |
| IO | DIFFIO_TX13n | | B2 | VREF1B2 | | | | N23 | | HIGH |
| VREF1B2 | | | B2 | VREF1B2 | J18 | L8 | L8 | K20 | | |
| IO | DIFFIO_RX12p | | B2 | VREF1B2 | H21 | N6 | N6 | M25 | | HIGH |
| IO | DIFFIO_RX12n | | B2 | VREF1B2 | H22 | N7 | N7 | M26 | | HIGH |
| IO | DIFFIO_TX12p | | B2 | VREF1B2 | J20 | M8 | M8 | N22 | | HIGH |
| IO | DIFFIO_TX12n | | B2 | VREF1B2 | J21 | M9 | M9 | N21 | | HIGH |

*Table 1–1. Pin List for the Stratix EP1S10 Device (Part 3 of 39)*

| Device | | | | | Package | | | | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **484-Pin Fineline BGA** | **672-Pin BGA** | **672-Pin Fineline BGA** | **780-Pin FineLine BGA** | | |
| IO | DIFFIO_RX11p | | B2 | VREF1B2 | | | | M27 | | HIGH |
| IO | DIFFIO_RX11n | | B2 | VREF1B2 | | | | N28 | | HIGH |
| IO | DIFFIO_TX11p | | B2 | VREF1B2 | K20 | P8 | P8 | N20 | | HIGH |
| IO | DIFFIO_TX11n | | B2 | VREF1B2 | K21 | N8 | N8 | N19 | | HIGH |
| CLK0n | | | B2 | VREF1B2 | L22 | N2 | N2 | N27 | | |
| CLK0p | | | B2 | VREF1B2 | L21 | N3 | N3 | P27 | | |
| IO | CLK1n | | B2 | VREF1B2 | | | | P26 | | |
| CLK1p | | | B2 | VREF1B2 | L20 | M1 | M1 | P25 | | |
| VCCINT | | | | | VCC | | | VCC | | |
| VCCA_PLL1 | | | | | K19 | M3 | M3 | P23 | | |
| GND | | | | | GND | | | GND | | |
| GNDA_PLL1 | | | | | L19 | N5 | N5 | P24 | | |
| VCCG_PLL1 | | | | | K18 | M2 | M2 | P21 | | |
| GNDG_PLL1 | | | | | L18 | N4 | N4 | P22 | | |
| VCCINT | | | | | | | | | | |
| VCCA_PLL2 | | | | | M18 | P5 | P5 | R23 | | |
| GND | | | | | | | | | | |
| GNDA_PLL2 | | | | | M19 | P3 | P3 | R24 | | |
| VCCG_PLL2 | | | | | N18 | P4 | P4 | R21 | | |
| GNDG_PLL2 | | | | | N19 | P2 | P2 | R22 | | |
| CLK2p | | | B1 | VREF0B1 | M21 | R1 | R1 | R27 | | |
| CLK2n | | | B1 | VREF0B1 | M22 | R2 | R2 | T27 | | |

**Table 1–1. Pin List for the Stratix EP1S10 Device (Part 4 of 39)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin Fineline BGA | 672-Pin BGA | 672-Pin Fineline BGA | 780-Pin FineLine BGA | DQS for x32 | DIFFIO Speed *Note (1)* |
| CLK3p | | | B1 | VREF0B1 | M20 | R3 | R3 | R25 | | |
| IO | CLK3n | | B1 | VREF0B1 | | | | R26 | | |
| IO | DIFFIO_RX10p | | B1 | VREF0B1 | | | | T28 | | HIGH |
| IO | DIFFIO_RX10n | | B1 | VREF0B1 | | | | U27 | | HIGH |
| IO | DIFFIO_TX10p | | B1 | VREF0B1 | N21 | P6 | P6 | T21 | | HIGH |
| IO | DIFFIO_TX10n | | B1 | VREF0B1 | N20 | P7 | P7 | T22 | | HIGH |
| IO | DIFFIO_RX9p | | B1 | VREF0B1 | R22 | R6 | R6 | U26 | | HIGH |
| IO | DIFFIO_RX9n | | B1 | VREF0B1 | R21 | R7 | R7 | U25 | | HIGH |
| IO | DIFFIO_TX9p | | B1 | VREF0B1 | P21 | R8 | R8 | T19 | | HIGH |
| IO | DIFFIO_TX9n | | B1 | VREF0B1 | P20 | R9 | R9 | T20 | | HIGH |
| VREF0B1 | | | B1 | VREF0B1 | P18 | T8 | T8 | R19 | | |
| IO | DIFFIO_RX8p | | B1 | VREF0B1 | T22 | R4 | R4 | V27 | | HIGH |
| IO | DIFFIO_RX8n | | B1 | VREF0B1 | T21 | R5 | R5 | V28 | | HIGH |
| IO | DIFFIO_TX8p | | B1 | VREF0B1 | | | | T23 | | HIGH |
| IO | DIFFIO_TX8n | | B1 | VREF0B1 | M17 | | | T24 | | HIGH |
| IO | DIFFIO_RX7p | | B1 | VREF0B1 | U21 | T3 | T3 | V26 | | HIGH |
| IO | DIFFIO_RX7n | | B1 | VREF0B1 | U22 | T2 | T2 | V25 | | HIGH |
| IO | DIFFIO_TX7p | | B1 | VREF0B1 | | | | T26 | | HIGH |
| IO | DIFFIO_TX7n | | B1 | VREF0B1 | N17 | | | T25 | | HIGH |
| IO | DIFFIO_RX6p | | B1 | VREF0B1 | | | | W28 | | HIGH |
| IO | DIFFIO_RX6n | | B1 | VREF0B1 | | | | W27 | | HIGH |
| IO | DIFFIO_TX6p | | B1 | VREF0B1 | R20 | T7 | T7 | U19 | | HIGH |

***Table 1–1. Pin List for the Stratix EP1S10 Device (Part 5 of 39)***

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **484-Pin Fineline BGA** | **672-Pin BGA** | **672-Pin Fineline BGA** | **780-Pin FineLine BGA** | **DQS for x32** | **DIFFIO Speed** *Note (1)* |
| IO | DIFFIO_TX6n | | B1 | VREF0B1 | R19 | T6 | T6 | U20 | | HIGH |
| IO | DIFFIO_RX5p | | B1 | VREF1B1 | V22 | T5 | T5 | W26 | | HIGH |
| IO | DIFFIO_RX5n | | B1 | VREF1B1 | V21 | T4 | T4 | W25 | | HIGH |
| IO | DIFFIO_TX5p | | B1 | VREF1B1 | T20 | U6 | U6 | U24 | | HIGH |
| IO | DIFFIO_TX5n | | B1 | VREF1B1 | T19 | U5 | U5 | U23 | | HIGH |
| IO | DIFFIO_RX4p | | B1 | VREF1B1 | | U2 | U2 | Y28 | | HIGH |
| IO | DIFFIO_RX4n | | B1 | VREF1B1 | | U1 | U1 | Y27 | | HIGH |
| IO | DIFFIO_TX4p | | B1 | VREF1B1 | | Y6 | Y6 | U21 | | HIGH |
| IO | DIFFIO_TX4n | | B1 | VREF1B1 | P17 | Y5 | Y5 | U22 | | HIGH |
| IO | DIFFIO_RX3p | | B1 | VREF1B1 | | Y2 | Y2 | Y26 | | HIGH |
| IO | DIFFIO_RX3n | | B1 | VREF1B1 | | Y1 | Y1 | Y25 | | HIGH |
| IO | DIFFIO_TX3p | | B1 | VREF1B1 | | AA6 | AA6 | V19 | | HIGH |
| IO | DIFFIO_TX3n | | B1 | VREF1B1 | P19 | AA5 | AA5 | V20 | | HIGH |
| VREF1B1 | | | B1 | VREF1B1 | R17 | V7 | V7 | W20 | | |
| IO | DIFFIO_RX2p | | B1 | VREF1B1 | | AA2 | AA2 | AA28 | | HIGH |
| IO | DIFFIO_RX2n | | B1 | VREF1B1 | | AA1 | AA1 | AA27 | | HIGH |
| IO | DIFFIO_TX2p | | B1 | VREF1B1 | | AA4 | AA4 | V24 | | HIGH |
| IO | DIFFIO_TX2n | | B1 | VREF1B1 | U18 | AA3 | AA3 | V23 | | HIGH |
| IO | DIFFIO_RX1p/RUP1 | | B1 | VREF1B1 | W21 | V6 | V6 | AA25 | | HIGH |
| IO | DIFFIO_RX1n/RDN1 | | B1 | VREF1B1 | W22 | V5 | V5 | AA26 | | HIGH |
| IO | DIFFIO_TX1p | | B1 | VREF1B1 | | AB4 | AB4 | V22 | | HIGH |
| IO | DIFFIO_TX1n | | B1 | VREF1B1 | T18 | AB3 | AB3 | V21 | | HIGH |

*Table 1–1. Pin List for the Stratix EP1S10 Device (Part 6 of 39)*

| Device | | | | | Package | | | | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin Fineline BGA | 672-Pin BGA | 672-Pin Fineline BGA | 780-Pin FineLine BGA | | |
| IO | DIFFIO_RX0p | | B1 | VREF1B1 | | AC2 | AC2 | AB28 | | HIGH |
| IO | DIFFIO_RX0n | | B1 | VREF1B1 | | AD1 | AD1 | AB27 | | HIGH |
| IO | DIFFIO_TX0p | | B1 | VREF1B1 | U20 | AC4 | AC4 | W23 | | HIGH |
| IO | DIFFIO_TX0n | | B1 | VREF1B1 | U19 | AC3 | AC3 | W24 | | HIGH |
| IO | DQ9B7 | | B8 | VREF0B8 | W20 | AD5 | AD5 | AG26 | DQ1B31 | |
| IO | DQ9B6 | | B8 | VREF0B8 | W19 | AD2 | AD2 | AH26 | DQ1B30 | |
| IO | DQ9B5 | | B8 | VREF0B8 | AA21 | AE2 | AE2 | AG25 | DQ1B29 | |
| IO | DQ9B4 | | B8 | VREF0B8 | AA20 | AD3 | AD3 | AH25 | DQ1B28 | |
| IO | DQ9B3 | | B8 | VREF0B8 | Y21 | AE4 | AE4 | AF25 | DQ1B27 | |
| IO | DQS9B | | B8 | VREF0B8 | Y20 | AD4 | AD4 | AF24 | | |
| IO | DQ9B2 | | B8 | VREF0B8 | Y19 | AE3 | AE3 | AG24 | DQ1B26 | |
| IO | DQ8B7 | | B8 | VREF0B8 | W18 | AC7 | AC7 | AG23 | DQ1B23 | |
| IO | DQ9B1 | | B8 | VREF0B8 | AA19 | AB5 | AB5 | AE24 | DQ1B25 | |
| IO | DQ8B6 | | B8 | VREF0B8 | AA18 | AD6 | AD6 | AD23 | DQ1B22 | |
| IO | DQ9B0 | | B8 | VREF0B8 | AB19 | AF3 | AF3 | AH24 | DQ1B24 | |
| IO | DQ8B5 | | B8 | VREF0B8 | AA17 | AE7 | AE7 | AF23 | DQ1B21 | |
| VREF0B8 | | | B8 | VREF0B8 | R18 | AE5 | AE5 | AD22 | | |
| IO | DQ8B4 | | B8 | VREF0B8 | AB18 | AB7 | AB7 | AH23 | DQ1B20 | |
| IO | DQ8B3 | | B8 | VREF0B8 | V18 | AD7 | AD7 | AE22 | DQ1B19 | |
| IO | DQS8B | | B8 | VREF0B8 | Y18 | AE6 | AE6 | AE23 | | |
| IO | DQ8B2 | | B8 | VREF0B8 | W17 | AA7 | AA7 | AF22 | DQ1B18 | |
| IO | DQ8B1 | | B8 | VREF0B8 | Y17 | AF7 | AF7 | AH22 | DQ1B17 | |

**Table 1–1. Pin List for the Stratix EP1S10 Device (Part 7 of 39)**

| Device | | | | | Package | | | | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin Fineline BGA | 672-Pin BGA | 672-Pin Fineline BGA | 780-Pin FineLine BGA | | |
| IO | DQ8B0 | | B8 | VREF0B8 | AB17 | AF6 | AF6 | AG22 | DQ1B16 | |
| IO | DQ7B2 | | B8 | VREF0B8 | T16 | | | AF20 | DQ1B10 | |
| IO | DQ7B7 | | B8 | VREF0B8 | U17 | | | AD21 | DQ1B15 | |
| IO | DQ7B6 | | B8 | VREF0B8 | U16 | | | AE21 | DQ1B14 | |
| IO | DQ7B5 | | B8 | VREF0B8 | V17 | | | AG21 | DQ1B13 | |
| IO | DQ7B4 | | B8 | VREF0B8 | V16 | | | AF21 | DQ1B12 | |
| IO | DQ7B3 | | B8 | VREF0B8 | Y16 | AF8 | AF8 | AE20 | DQ1B11 | |
| IO | DQS7B | | B8 | VREF0B8 | AA16 | | | AG20 | DQS1B | |
| IO | | | B8 | VREF0B8 | N16 | Y8 | Y8 | AB18 | | |
| IO | DQ7B1 | | B8 | VREF0B8 | W16 | W9 | W9 | AH21 | DQ1B9 | |
| IO | | | B8 | VREF0B8 | N13 | AA8 | AA8 | V18 | | |
| IO | DQ7B0 | | B8 | VREF0B8 | AB16 | | | AH20 | DQ1B8 | |
| IO | DQ6B7 | | B8 | VREF0B8 | Y15 | AC9 | AC9 | AE19 | DQ1B7 | |
| IO | DQ6B6 | | B8 | VREF1B8 | AA15 | AF9 | AF9 | AD19 | DQ1B6 | |
| IO | DQ6B5 | | B8 | VREF1B8 | AB15 | AD10 | AD10 | AF19 | DQ1B5 | |
| IO | DQ6B4 | | B8 | VREF1B8 | V15 | AE10 | AE10 | AG19 | DQ1B4 | |
| IO | | PGM2 | B8 | VREF1B8 | R15 | AA9 | AA9 | AB19 | | |
| IO | FCLK3 | | B8 | VREF1B8 | P16 | AD9 | AD9 | AC21 | | |
| IO | FCLK2 | | B8 | VREF1B8 | T15 | AB9 | AB9 | AC19 | | |
| IO | DQ6B3 | | B8 | VREF1B8 | U15 | AC10 | AC10 | AH19 | DQ1B3 | |
| IO | DQS6B | | B8 | VREF1B8 | W15 | Y10 | Y10 | AF18 | | |
| IO | DQ6B2 | | B8 | VREF1B8 | U14 | AA10 | AA10 | AD18 | DQ1B2 | |

*Table 1–1. Pin List for the Stratix EP1S10 Device (Part 8 of 39)*

| Device | | | | | Package | | | | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin Fineline BGA | 672-Pin BGA | 672-Pin Fineline BGA | 780-Pin FineLine BGA | | |
| IO | | | B8 | VREF1B8 | N14 | W10 | W10 | AA20 | | |
| IO | DQ6B1 | | B8 | VREF1B8 | W14 | AB10 | AB10 | AE18 | DQ1B1 | |
| IO | DQ6B0 | | B8 | VREF1B8 | V14 | AF10 | AF10 | AG18 | DQ1B0 | |
| IO | RDN8 | | B8 | VREF1B8 | P15 | AB11 | AB11 | Y19 | | |
| IO | RUP8 | | B8 | VREF1B8 | N15 | AE11 | AE11 | W19 | | |
| IO | | | B8 | VREF1B8 | | | | W18 | | |
| IO | | RDYnBSY | B8 | VREF1B8 | P14 | AC11 | AC11 | AA19 | | |
| IO | | nCS | B8 | VREF1B8 | T14 | Y11 | Y11 | Y18 | | |
| IO | | CS | B8 | VREF1B8 | P13 | AA11 | AA11 | AA18 | | |
| VREF1B8 | | | B8 | VREF1B8 | R16 | AE9 | AE9 | AD20 | | |
| IO | CLK5n | | B8 | VREF1B8 | W13 | AD12 | AD12 | Y17 | | |
| CLK5p | | | B8 | VREF1B8 | V13 | AC12 | AC12 | AA17 | | |
| IO | CLK4n | | B8 | VREF1B8 | Y14 | AF12 | AF12 | AB17 | | |
| CLK4p | | | B8 | VREF1B8 | AA14 | AE12 | AE12 | AC17 | | |
| PLL_ENA | | PLL_ENA | B8 | VREF1B8 | R13 | W12 | W12 | AC18 | | |
| MSEL0 | | MSEL0 | B8 | VREF1B8 | T13 | Y12 | Y12 | AC16 | | |
| MSEL1 | | MSEL1 | B8 | VREF1B8 | P12 | Y13 | Y13 | W17 | | |
| MSEL2 | | MSEL2 | B8 | VREF1B8 | R12 | W13 | W13 | AB15 | | |
| IO | PLL6_OUT3n | | B12 | VREF1B8 | | | | Y16 | | |
| IO | PLL6_OUT3p | | B12 | VREF1B8 | | | | W16 | | |
| IO | PLL6_OUT2n | | B12 | VREF1B8 | | | | AG15 | | |
| IO | PLL6_OUT2p | | B12 | VREF1B8 | | | | AF15 | | |

**Table 1–1. Pin List for the Stratix EP1S10 Device (Part 9 of 39)**

| Device | | | | | Package | | | | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin Fineline BGA | 672-Pin BGA | 672-Pin Fineline BGA | 780-Pin FineLine BGA | | |
| IO | PLL6_FBn | | B11 | VREF1B8 | Y12 | AB12 | AB12 | AA15 | | |
| IO | PLL6_FBp | | B11 | VREF1B8 | W12 | AA12 | AA12 | AA14 | | |
| IO | PLL6_OUT1n | | B11 | VREF1B8 | AB12 | AB14 | AB14 | W15 | | |
| IO | PLL6_OUT1p | | B11 | VREF1B8 | AA12 | AA14 | AA14 | W14 | | |
| IO | PLL6_OUT0n | | B11 | VREF1B8 | Y13 | AB13 | AB13 | AE15 | | |
| IO | PLL6_OUT0p | | B11 | VREF1B8 | AA13 | AA13 | AA13 | AD15 | | |
| VCC_PLL6_OUTB | | | B12 | | | | | AB16 | | |
| VCC_PLL6_OUTB | | | B12 | | | | | | | |
| VCC_PLL6_OUTA | | | B11 | | | | | AC14 | | |
| VCC_PLL6_OUTA | | | B11 | | U13 | AE13 | AE13 | | | |
| VCCINT | | | | | | | | | | |
| VCCA_PLL6 | | | | | T12 | AD14 | AD14 | AG14 | | |
| GND | | | | | | | | | | |
| GNDA_PLL6 | | | | | U12 | AC14 | AC14 | AF14 | | |
| GNDA_PLL6 | | | | | | | | | | |
| VCCG_PLL6 | | | | | U11 | AD13 | AD13 | AA13 | | |
| GNDG_PLL6 | | | | | T11 | AE14 | AE14 | AB14 | | |
| CLK7p | | | B7 | VREF0B7 | AA11 | AE15 | AE15 | W13 | | |
| IO | CLK7n | | B7 | VREF0B7 | | | | Y13 | | |
| CLK6p | | | B7 | VREF0B7 | AB11 | AF15 | AF15 | AD14 | | |
| IO | CLK6n | | B7 | VREF0B7 | | | | AE14 | | |
| nCE | | nCE | B7 | VREF0B7 | R11 | Y14 | Y14 | AB13 | | |

*Table 1–1. Pin List for the Stratix EP1S10 Device (Part 10 of 39)*

| Device | | | | | Package | | | | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **484-Pin Fineline BGA** | **672-Pin BGA** | **672-Pin Fineline BGA** | **780-Pin FineLine BGA** | | |
| nCEO | | nCEO | B7 | VREF0B7 | P11 | W14 | W14 | AC13 | | |
| IO | | | B7 | VREF0B7 | | | | Y9 | | |
| IO | | | B7 | VREF0B7 | R8 | | | AE4 | | |
| IO | | PGM0 | B7 | VREF0B7 | N10 | W15 | W15 | W12 | | |
| nIO_PULLUP | | nIO_PULLUP | B7 | VREF0B7 | N9 | AA15 | AA15 | Y12 | | |
| VCCSEL | | VCCSEL | B7 | VREF0B7 | R10 | Y15 | Y15 | AA12 | | |
| PORSEL | | PORSEL | B7 | VREF0B7 | U10 | W16 | W16 | AC12 | | |
| IO | | INIT_DONE | B7 | VREF0B7 | P10 | AC15 | AC15 | W11 | | |
| IO | | nRS | B7 | VREF0B7 | T10 | Y16 | Y16 | AC11 | | |
| IO | | RUnLU | B7 | VREF0B7 | P9 | AD15 | AD15 | W10 | | |
| IO | | PGM1 | B7 | VREF0B7 | M8 | AC16 | AC16 | AA11 | | |
| IO | RDN7 | | B7 | VREF0B7 | T9 | AB16 | AB16 | AC10 | | |
| IO | RUP7 | | B7 | VREF0B7 | N8 | AD16 | AD16 | AB11 | | |
| VREF0B7 | | | B7 | VREF0B7 | R9 | AB15 | AB15 | AD11 | | |
| IO | DQ3B7 | | B7 | VREF0B7 | AA8 | W17 | W17 | AG11 | DQ0B31 | |
| IO | DQ3B6 | | B7 | VREF0B7 | Y9 | AE16 | AE16 | AH11 | DQ0B30 | |
| IO | DQ3B5 | | B7 | VREF0B7 | Y8 | Y17 | Y17 | AE11 | DQ0B29 | |
| IO | DEV_CLRn | | B7 | VREF0B7 | P8 | AF17 | AF17 | AC9 | | |
| IO | DQ3B4 | | B7 | VREF0B7 | U9 | AA17 | AA17 | AF11 | DQ0B28 | |
| IO | DQ3B3 | | B7 | VREF0B7 | V9 | Y18 | Y18 | AE10 | DQ0B27 | |
| IO | DQS3B | | B7 | VREF0B7 | W8 | AE17 | AE17 | AG10 | | |
| IO | DQ3B2 | | B7 | VREF0B7 | W9 | W18 | W18 | AH10 | DQ0B26 | |

*Table 1–1. Pin List for the Stratix EP1S10 Device (Part 11 of 39)*

| Device | | | | | Package | | | | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin Fineline BGA | 672-Pin BGA | 672-Pin Fineline BGA | 780-Pin FineLine BGA | | |
| IO | DQ3B1 | | B7 | VREF0B7 | V8 | AB17 | AB17 | AF10 | DQ0B25 | |
| IO | DQ3B0 | | B7 | VREF0B7 | U8 | AA18 | AA18 | AD10 | DQ0B24 | |
| IO | FCLK5 | | B7 | VREF0B7 | T8 | AC17 | AC17 | AC8 | | |
| IO | FCLK4 | | B7 | VREF0B7 | M7 | AD17 | AD17 | AB10 | | |
| IO | DQ2B7 | | B7 | VREF1B7 | W7 | AF18 | AF18 | AG9 | DQ0B23 | |
| IO | DQ2B6 | | B7 | VREF1B7 | U6 | | | AF9 | DQ0B22 | |
| IO | DQ2B5 | | B7 | VREF1B7 | AB8 | AF19 | AF19 | AE9 | DQ0B21 | |
| IO | DQ2B4 | | B7 | VREF1B7 | V6 | Y20 | Y20 | AH8 | DQ0B20 | |
| IO | DQ2B3 | | B7 | VREF1B7 | AB7 | AA19 | AA19 | AH9 | DQ0B19 | |
| IO | DQS2B | | B7 | VREF1B7 | AA7 | AB19 | AB19 | AE8 | DQS0B | |
| IO | DQ2B2 | | B7 | VREF1B7 | U7 | | | AD8 | DQ0B18 | |
| IO | DQ1B7 | | B7 | VREF1B7 | Y6 | AE20 | AE20 | AF6 | DQ0B15 | |
| IO | DQ2B1 | | B7 | VREF1B7 | V7 | | | AF8 | DQ0B17 | |
| IO | DQ1B6 | | B7 | VREF1B7 | V5 | AA20 | AA20 | AG7 | DQ0B14 | |
| IO | DQ2B0 | | B7 | VREF1B7 | Y7 | | | AG8 | DQ0B16 | |
| IO | DQ1B5 | | B7 | VREF1B7 | AA6 | AB20 | AB20 | AH7 | DQ0B13 | |
| IO | DQ1B4 | | B7 | VREF1B7 | W6 | AF21 | AF21 | AF7 | DQ0B12 | |
| IO | DQ1B3 | | B7 | VREF1B7 | AB6 | AC20 | AC20 | AD6 | DQ0B11 | |
| IO | DQS1B | | B7 | VREF1B7 | AB5 | AA21 | AA21 | AE7 | | |
| IO | DQ1B2 | | B7 | VREF1B7 | W5 | AE21 | AE21 | AH6 | DQ0B10 | |
| IO | DQ1B1 | | B7 | VREF1B7 | Y5 | AD20 | AD20 | AG6 | DQ0B9 | |
| IO | DQ1B0 | | B7 | VREF1B7 | AA5 | AC21 | AC21 | AE6 | DQ0B8 | |

**Table 1–1. Pin List for the Stratix EP1S10 Device (Part 12 of 39)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin Fineline BGA | 672-Pin BGA | 672-Pin Fineline BGA | 780-Pin FineLine BGA | DQS for x32 | DIFFIO Speed *Note (1)* |
| VREF1B7 | | | B7 | VREF1B7 | R7 | AB18 | AB18 | AD9 | | |
| IO | | | B7 | VREF1B7 | N7 | | | V11 | | |
| IO | | | B7 | VREF1B7 | P7 | | | Y11 | | |
| IO | DQ0B7 | | B7 | VREF1B7 | AA4 | AE25 | AE25 | AF5 | DQ0B7 | |
| IO | DQ0B6 | | B7 | VREF1B7 | AB4 | AF22 | AF22 | AH5 | DQ0B6 | |
| IO | DQ0B5 | | B7 | VREF1B7 | Y2 | AF24 | AF24 | AF4 | DQ0B5 | |
| IO | DQ0B4 | | B7 | VREF1B7 | Y4 | AE22 | AE22 | AG4 | DQ0B4 | |
| IO | DQ0B3 | | B7 | VREF1B7 | AA3 | AB22 | AB22 | AG5 | DQ0B3 | |
| IO | DQS0B | | B7 | VREF1B7 | AA2 | AE23 | AE23 | AH3 | | |
| IO | DQ0B2 | | B7 | VREF1B7 | W3 | AC23 | AC23 | AG3 | DQ0B2 | |
| IO | DQ0B1 | | B7 | VREF1B7 | W4 | AC22 | AC22 | AE5 | DQ0B1 | |
| IO | DQ0B0 | | B7 | VREF1B7 | Y3 | AE24 | AE24 | AH4 | DQ0B0 | |
| IO | | | B7 | VREF1B7 | T7 | AB21 | AB21 | AB7 | | |
| IO | DIFFIO_TX43n | | B6 | VREF0B6 | V4 | AD25 | AD25 | W5 | | HIGH |
| IO | DIFFIO_TX43p | | B6 | VREF0B6 | V3 | AC24 | AC24 | W6 | | HIGH |
| IO | DIFFIO_RX43n | | B6 | VREF0B6 | | AD26 | AD26 | AB2 | | HIGH |
| IO | DIFFIO_RX43p | | B6 | VREF0B6 | | AC25 | AC25 | AB1 | | HIGH |
| IO | DIFFIO_TX42n | | B6 | VREF0B6 | T5 | AB24 | AB24 | V8 | | HIGH |
| IO | DIFFIO_TX42p | | B6 | VREF0B6 | | AB23 | AB23 | V7 | | HIGH |
| IO | DIFFIO_RX42n/RDN6 | | B6 | VREF0B6 | W1 | U24 | U24 | AA3 | | HIGH |
| IO | DIFFIO_RX42p/RUP6 | | B6 | VREF0B6 | W2 | U23 | U23 | AA4 | | HIGH |
| IO | DIFFIO_TX41n | | B6 | VREF0B6 | U5 | AA24 | AA24 | V6 | | HIGH |

**Table 1–1. Pin List for the Stratix EP1S10 Device (Part 13 of 39)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin Fineline BGA | 672-Pin BGA | 672-Pin Fineline BGA | 780-Pin FineLine BGA | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_TX41p | | B6 | VREF0B6 | | AA23 | AA23 | V5 | | HIGH |
| IO | DIFFIO_RX41n | | B6 | VREF0B6 | | AA26 | AA26 | AA2 | | HIGH |
| IO | DIFFIO_RX41p | | B6 | VREF0B6 | | AA25 | AA25 | AA1 | | HIGH |
| VREF0B6 | | | B6 | VREF0B6 | R6 | Y21 | Y21 | AE3 | | |
| IO | DIFFIO_TX40n | | B6 | VREF0B6 | T4 | AA22 | AA22 | V9 | | HIGH |
| IO | DIFFIO_TX40p | | B6 | VREF0B6 | T3 | Y22 | Y22 | V10 | | HIGH |
| IO | DIFFIO_RX40n | | B6 | VREF0B6 | | Y26 | Y26 | Y4 | | HIGH |
| IO | DIFFIO_RX40p | | B6 | VREF0B6 | | Y25 | Y25 | Y3 | | HIGH |
| IO | DIFFIO_TX39n | | B6 | VREF0B6 | P6 | Y24 | Y24 | U7 | | HIGH |
| IO | DIFFIO_TX39p | | B6 | VREF0B6 | | Y23 | Y23 | U8 | | HIGH |
| IO | DIFFIO_RX39n | | B6 | VREF0B6 | V2 | U22 | U22 | Y2 | | HIGH |
| IO | DIFFIO_RX39p | | B6 | VREF0B6 | V1 | U21 | U21 | Y1 | | HIGH |
| IO | DIFFIO_TX38n | | B6 | VREF0B6 | P4 | T21 | T21 | U6 | | HIGH |
| IO | DIFFIO_TX38p | | B6 | VREF0B6 | | T20 | T20 | U5 | | HIGH |
| IO | DIFFIO_RX38n | | B6 | VREF0B6 | | T25 | T25 | W4 | | HIGH |
| IO | DIFFIO_RX38p | | B6 | VREF0B6 | | T24 | T24 | W3 | | HIGH |
| IO | DIFFIO_TX37n | | B6 | VREF1B6 | R3 | T19 | T19 | U9 | | HIGH |
| IO | DIFFIO_TX37p | | B6 | VREF1B6 | R4 | R19 | R19 | U10 | | HIGH |
| IO | DIFFIO_RX37n | | B6 | VREF1B6 | | | | W2 | | HIGH |
| IO | DIFFIO_RX37p | | B6 | VREF1B6 | | | | W1 | | HIGH |
| IO | DIFFIO_TX36n | | B6 | VREF1B6 | N6 | | | T6 | | HIGH |
| IO | DIFFIO_TX36p | | B6 | VREF1B6 | | | | T5 | | HIGH |

*Table 1–1. Pin List for the Stratix EP1S10 Device (Part 14 of 39)*

| Device | | | | | Package | | | | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin Fineline BGA | 672-Pin BGA | 672-Pin Fineline BGA | 780-Pin FineLine BGA | | |
| IO | DIFFIO_RX36n | | B6 | VREF1B6 | U1 | T23 | T23 | V4 | | HIGH |
| IO | DIFFIO_RX36p | | B6 | VREF1B6 | U2 | T22 | T22 | V3 | | HIGH |
| IO | DIFFIO_TX35n | | B6 | VREF1B6 | M6 | | | T10 | | HIGH |
| IO | DIFFIO_TX35p | | B6 | VREF1B6 | | | | T9 | | HIGH |
| IO | DIFFIO_RX35n | | B6 | VREF1B6 | T2 | R22 | R22 | V1 | | HIGH |
| IO | DIFFIO_RX35p | | B6 | VREF1B6 | T1 | R23 | R23 | V2 | | HIGH |
| VREF1B6 | | | B6 | VREF1B6 | P5 | V20 | V20 | W9 | | |
| IO | DIFFIO_TX34n | | B6 | VREF1B6 | P3 | P20 | P20 | T7 | | HIGH |
| IO | DIFFIO_TX34p | | B6 | VREF1B6 | P2 | P21 | P21 | T8 | | HIGH |
| IO | DIFFIO_RX34n | | B6 | VREF1B6 | R2 | R20 | R20 | U4 | | HIGH |
| IO | DIFFIO_RX34p | | B6 | VREF1B6 | R1 | R21 | R21 | U3 | | HIGH |
| IO | DIFFIO_TX33n | | B6 | VREF1B6 | N3 | P19 | P19 | T4 | | HIGH |
| IO | DIFFIO_TX33p | | B6 | VREF1B6 | N2 | N19 | N19 | T3 | | HIGH |
| IO | DIFFIO_RX33n | | B6 | VREF1B6 | | | | U2 | | HIGH |
| IO | DIFFIO_RX33p | | B6 | VREF1B6 | | | | T1 | | HIGH |
| IO | CLK8n | | B6 | VREF1B6 | | | | R3 | | |
| CLK8p | | | B6 | VREF1B6 | M3 | P24 | P24 | R4 | | |
| CLK9n | | | B6 | VREF1B6 | M1 | P25 | P25 | T2 | | |
| CLK9p | | | B6 | VREF1B6 | M2 | R26 | R26 | R2 | | |
| GNDG_PLL3 | | | | | N4 | R25 | R25 | R7 | | |
| VCCG_PLL3 | | | | | N5 | P23 | P23 | R8 | | |
| GNDA_PLL3 | | | | | M4 | R24 | R24 | R5 | | |

**Table 1–1. Pin List for the Stratix EP1S10 Device (Part 15 of 39)**

| Device | | | | | Package | | | | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin Fineline BGA | 672-Pin BGA | 672-Pin Fineline BGA | 780-Pin FineLine BGA | | |
| GND | | | | | | | | | | |
| VCCA_PLL3 | | | | | M5 | P22 | P22 | R6 | | |
| VCCINT | | | | | | | | | | |
| GNDG_PLL4 | | | | | L5 | N22 | N22 | P7 | | |
| VCCG_PLL4 | | | | | K5 | N24 | N24 | P8 | | |
| GNDA_PLL4 | | | | | L4 | N23 | N23 | P5 | | |
| GND | | | | | | | | | | |
| VCCA_PLL4 | | | | | K4 | N25 | N25 | P6 | | |
| VCCINT | | | | | | | | | | |
| CLK10p | | | B5 | VREF0B5 | L3 | M26 | M26 | P4 | | |
| IO | CLK10n | | B5 | VREF0B5 | | | | P3 | | |
| CLK11p | | | B5 | VREF0B5 | L2 | M24 | M24 | P2 | | |
| CLK11n | | | B5 | VREF0B5 | L1 | M25 | M25 | N2 | | |
| IO | DIFFIO_TX32n | | B5 | VREF0B5 | K2 | N20 | N20 | N10 | | HIGH |
| IO | DIFFIO_TX32p | | B5 | VREF0B5 | K3 | N21 | N21 | N9 | | HIGH |
| IO | DIFFIO_RX32n | | B5 | VREF0B5 | | | | M2 | | HIGH |
| IO | DIFFIO_RX32p | | B5 | VREF0B5 | | | | N1 | | HIGH |
| IO | DIFFIO_TX31n | | B5 | VREF0B5 | J2 | M18 | M18 | N5 | | HIGH |
| IO | DIFFIO_TX31p | | B5 | VREF0B5 | J3 | M19 | M19 | N6 | | HIGH |
| IO | DIFFIO_RX31n | | B5 | VREF0B5 | H1 | M20 | M20 | M3 | | HIGH |
| IO | DIFFIO_RX31p | | B5 | VREF0B5 | H2 | M21 | M21 | M4 | | HIGH |
| VREF0B5 | | | B5 | VREF0B5 | J5 | L19 | L19 | P10 | | |

**Table 1–1. Pin List for the Stratix EP1S10 Device (Part 16 of 39)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin Fineline BGA | 672-Pin BGA | 672-Pin Fineline BGA | 780-Pin FineLine BGA | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_TX30n | | B5 | VREF0B5 | L6 | | | N7 | | HIGH |
| IO | DIFFIO_TX30p | | B5 | VREF0B5 | | | | N8 | | HIGH |
| IO | DIFFIO_RX30n | | B5 | VREF0B5 | G2 | M22 | M22 | L1 | | HIGH |
| IO | DIFFIO_RX30p | | B5 | VREF0B5 | G1 | M23 | M23 | L2 | | HIGH |
| IO | DIFFIO_TX29n | | B5 | VREF0B5 | K6 | | | N4 | | HIGH |
| IO | DIFFIO_TX29p | | B5 | VREF0B5 | | | | N3 | | HIGH |
| IO | DIFFIO_RX29n | | B5 | VREF0B5 | F1 | L22 | L22 | L3 | | HIGH |
| IO | DIFFIO_RX29p | | B5 | VREF0B5 | F2 | L23 | L23 | L4 | | HIGH |
| IO | DIFFIO_TX28n | | B5 | VREF0B5 | H3 | L21 | L21 | M10 | | HIGH |
| IO | DIFFIO_TX28p | | B5 | VREF0B5 | H4 | L20 | L20 | M9 | | HIGH |
| IO | DIFFIO_RX28n | | B5 | VREF0B5 | | | | K1 | | HIGH |
| IO | DIFFIO_RX28p | | B5 | VREF0B5 | | | | K2 | | HIGH |
| IO | DIFFIO_TX27n | | B5 | VREF1B5 | J4 | K20 | K20 | M6 | | HIGH |
| IO | DIFFIO_TX27p | | B5 | VREF1B5 | | K19 | K19 | M5 | | HIGH |
| IO | DIFFIO_RX27n | | B5 | VREF1B5 | | L25 | L25 | K4 | | HIGH |
| IO | DIFFIO_RX27p | | B5 | VREF1B5 | | L24 | L24 | K3 | | HIGH |
| IO | DIFFIO_TX26n | | B5 | VREF1B5 | J6 | G21 | G21 | M8 | | HIGH |
| IO | DIFFIO_TX26p | | B5 | VREF1B5 | | G22 | G22 | M7 | | HIGH |
| IO | DIFFIO_RX26n | | B5 | VREF1B5 | | K24 | K24 | J1 | | HIGH |
| IO | DIFFIO_RX26p | | B5 | VREF1B5 | | K23 | K23 | J2 | | HIGH |
| IO | DIFFIO_TX25n | | B5 | VREF1B5 | G3 | G23 | G23 | L10 | | HIGH |
| IO | DIFFIO_TX25p | | B5 | VREF1B5 | G4 | G24 | G24 | L9 | | HIGH |

**Table 1–1. Pin List for the Stratix EP1S10 Device (Part 17 of 39)**

| Device | | | | | Package | | | | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **484-Pin Fineline BGA** | **672-Pin BGA** | **672-Pin Fineline BGA** | **780-Pin FineLine BGA** | | |
| IO | DIFFIO_RX25n | | B5 | VREF1B5 | | G25 | G25 | J3 | | HIGH |
| IO | DIFFIO_RX25p | | B5 | VREF1B5 | | G26 | G26 | J4 | | HIGH |
| VREF1B5 | | | B5 | VREF1B5 | H5 | J18 | J18 | K9 | | |
| IO | DIFFIO_TX24n | | B5 | VREF1B5 | G5 | F23 | F23 | L5 | | HIGH |
| IO | DIFFIO_TX24p | | B5 | VREF1B5 | | F24 | F24 | L6 | | HIGH |
| IO | DIFFIO_RX24n | | B5 | VREF1B5 | | F25 | F25 | H1 | | HIGH |
| IO | DIFFIO_RX24p | | B5 | VREF1B5 | | F26 | F26 | H2 | | HIGH |
| IO | DIFFIO_TX23n | | B5 | VREF1B5 | F5 | E23 | E23 | L8 | | HIGH |
| IO | DIFFIO_TX23p | | B5 | VREF1B5 | | E24 | E24 | L7 | | HIGH |
| IO | DIFFIO_RX23n/RDN5 | | B5 | VREF1B5 | E1 | J22 | J22 | H3 | | HIGH |
| IO | DIFFIO_RX23p/RUP5 | | B5 | VREF1B5 | E2 | J21 | J21 | H4 | | HIGH |
| IO | DIFFIO_TX22n | | B5 | VREF1B5 | F3 | D24 | D24 | K7 | | HIGH |
| IO | DIFFIO_TX22p | | B5 | VREF1B5 | F4 | C25 | C25 | K8 | | HIGH |
| IO | DIFFIO_RX22n | | B5 | VREF1B5 | D2 | D25 | D25 | G1 | | HIGH |
| IO | DIFFIO_RX22p | | B5 | VREF1B5 | D1 | C26 | C26 | G2 | | HIGH |
| IO | | | B4 | VREF0B4 | G7 | C23 | C23 | G7 | | |
| IO | DQ0T0 | | B4 | VREF0B4 | B3 | B24 | B24 | A4 | DQ0T0 | |
| IO | DQ0T1 | | B4 | VREF0B4 | B2 | D23 | D23 | A3 | DQ0T1 | |
| IO | DQ0T2 | | B4 | VREF0B4 | D3 | D22 | D22 | B3 | DQ0T2 | |
| IO | DQS0T | | B4 | VREF0B4 | C2 | C24 | C24 | D5 | | |
| IO | DQ0T3 | | B4 | VREF0B4 | B4 | E22 | E22 | B5 | DQ0T3 | |
| IO | DQ0T4 | | B4 | VREF0B4 | C3 | B22 | B22 | B4 | DQ0T4 | |

*Table 1–1. Pin List for the Stratix EP1S10 Device (Part 18 of 39)*

| Device | | | | | Package | | | | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **484-Pin Fineline BGA** | **672-Pin BGA** | **672-Pin Fineline BGA** | **780-Pin FineLine BGA** | | |
| IO | DQ0T5 | | B4 | VREF0B4 | C4 | A24 | A24 | C4 | DQ0T5 | |
| IO | DQ0T6 | | B4 | VREF0B4 | D4 | A22 | A22 | A5 | DQ0T6 | |
| IO | DQ0T7 | | B4 | VREF0B4 | A4 | C22 | C22 | C5 | DQ0T7 | |
| IO | | | B4 | VREF0B4 | J7 | | | L11 | | |
| IO | | | B4 | VREF0B4 | K7 | | | M11 | | |
| VREF0B4 | | | B4 | VREF0B4 | H6 | F22 | F22 | E7 | | |
| IO | DQ1T0 | | B4 | VREF0B4 | C5 | C20 | C20 | E6 | DQ0T8 | |
| IO | DQ1T1 | | B4 | VREF0B4 | D5 | D21 | D21 | A6 | DQ0T9 | |
| IO | DQ1T2 | | B4 | VREF0B4 | B5 | D20 | D20 | B7 | DQ0T10 | |
| IO | DQS1T | | B4 | VREF0B4 | A5 | A21 | A21 | B6 | | |
| IO | DQ1T3 | | B4 | VREF0B4 | C6 | C21 | C21 | D6 | DQ0T11 | |
| IO | DQ1T4 | | B4 | VREF0B4 | E5 | B20 | B20 | A7 | DQ0T12 | |
| IO | DQ1T5 | | B4 | VREF0B4 | D6 | E21 | E21 | D7 | DQ0T13 | |
| IO | DQ2T0 | | B4 | VREF0B4 | B7 | | | D8 | DQ0T16 | |
| IO | DQ1T6 | | B4 | VREF0B4 | A6 | A20 | A20 | C6 | DQ0T14 | |
| IO | DQ2T1 | | B4 | VREF0B4 | E6 | | | C8 | DQ0T17 | |
| IO | DQ1T7 | | B4 | VREF0B4 | B6 | F21 | F21 | C7 | DQ0T15 | |
| IO | DQ2T2 | | B4 | VREF0B4 | F7 | | | E8 | DQ0T18 | |
| IO | DQS2T | | B4 | VREF0B4 | A7 | A19 | A19 | C9 | DQS0T | |
| IO | DQ2T3 | | B4 | VREF0B4 | A8 | C18 | C18 | D9 | DQ0T19 | |
| IO | DQ2T4 | | B4 | VREF0B4 | D7 | B18 | B18 | B9 | DQ0T20 | |
| IO | DQ2T5 | | B4 | VREF0B4 | C7 | D18 | D18 | B8 | DQ0T21 | |

*Table 1–1. Pin List for the Stratix EP1S10 Device (Part 19 of 39)*

| Device | | | | | Package | | | | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin Fineline BGA | 672-Pin BGA | 672-Pin Fineline BGA | 780-Pin FineLine BGA | | |
| IO | DQ2T6 | | B4 | VREF0B4 | F6 | | | A8 | DQ0T22 | |
| IO | DQ2T7 | | B4 | VREF0B4 | E7 | G20 | G20 | A9 | DQ0T23 | |
| IO | FCLK6 | | B4 | VREF1B4 | G8 | G19 | G19 | G10 | | |
| IO | FCLK7 | | B4 | VREF1B4 | H8 | E18 | E18 | F10 | | |
| IO | DQ3T0 | | B4 | VREF1B4 | E8 | F19 | F19 | E10 | DQ0T24 | |
| IO | DQ3T1 | | B4 | VREF1B4 | C8 | C17 | C17 | A10 | DQ0T25 | |
| IO | DQ3T2 | | B4 | VREF1B4 | F8 | G18 | G18 | C10 | DQ0T26 | |
| IO | DQS3T | | B4 | VREF1B4 | D8 | B17 | B17 | D10 | | |
| IO | DQ3T3 | | B4 | VREF1B4 | B8 | E17 | E17 | B10 | DQ0T27 | |
| IO | DQ3T4 | | B4 | VREF1B4 | C9 | F17 | F17 | A11 | DQ0T28 | |
| IO | DQ3T5 | | B4 | VREF1B4 | D9 | D17 | D17 | C11 | DQ0T29 | |
| IO | DEV_OE | | B4 | VREF1B4 | L7 | G17 | G17 | J11 | | |
| IO | DQ3T6 | | B4 | VREF1B4 | E9 | A17 | A17 | D11 | DQ0T30 | |
| IO | DQ3T7 | | B4 | VREF1B4 | F9 | H18 | H18 | B11 | DQ0T31 | |
| VREF1B4 | | | B4 | VREF1B4 | H7 | F18 | F18 | E9 | | |
| IO | RUP4 | | B4 | VREF1B4 | J8 | D16 | D16 | H11 | | |
| IO | RDN4 | | B4 | VREF1B4 | K8 | C16 | C16 | G11 | | |
| IO | | nWS | B4 | VREF1B4 | F10 | E16 | E16 | K11 | | |
| IO | | DATA0 | B4 | VREF1B4 | L8 | F16 | F16 | H12 | | |
| IO | | DATA1 | B4 | VREF1B4 | J9 | C15 | C15 | F12 | | |
| IO | | DATA2 | B4 | VREF1B4 | H10 | H16 | H16 | J12 | | |
| TMS | | TMS | B4 | VREF1B4 | G10 | E15 | E15 | F13 | | |

*Table 1–1. Pin List for the Stratix EP1S10 Device (Part 20 of 39)*

| Device | | | | | Package | | | | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin Fineline BGA | 672-Pin BGA | 672-Pin Fineline BGA | 780-Pin FineLine BGA | | |
| TRST | | TRST | B4 | VREF1B4 | J10 | D15 | D15 | L12 | | |
| TCK | | TCK | B4 | VREF1B4 | K9 | G15 | G15 | K12 | | |
| IO | | DATA3 | B4 | VREF1B4 | K10 | F15 | F15 | M12 | | |
| IO | | | B4 | VREF1B4 | G9 | | | F8 | | |
| IO | | | B4 | VREF1B4 | | | | J9 | | |
| TDI | | TDI | B4 | VREF1B4 | J11 | H15 | H15 | G13 | | |
| TDO | | TDO | B4 | VREF1B4 | H11 | G14 | G14 | H13 | | |
| IO | CLK12n | | B4 | VREF1B4 | | | | J13 | | |
| CLK12p | | | B4 | VREF1B4 | A11 | B15 | B15 | K13 | | |
| IO | CLK13n | | B4 | VREF1B4 | | | | L13 | | |
| CLK13p | | | B4 | VREF1B4 | B11 | A15 | A15 | M13 | | |
| TEMPDIODEp | | | | | G12 | H14 | H14 | B14 | | |
| TEMPDIODEn | | | | | H12 | G13 | G13 | C14 | | |
| VCCINT | | | | | | | | | | |
| VCCA_PLL5 | | | | | G13 | D14 | D14 | F14 | | |
| GND | | | | | | | | | | |
| GNDA_PLL5 | | | | | F12 | B14 | B14 | G14 | | |
| GNDA_PLL5 | | | | | | | | | | |
| VCCG_PLL5 | | | | | F11 | C14 | C14 | D14 | | |
| GNDG_PLL5 | | | | | G11 | B13 | B13 | E14 | | |
| VCC_PLL5_OUTA | | | B9 | | F13 | D13 | D13 | F15 | | |
| VCC_PLL5_OUTA | | | B9 | | | | | | | |

*Table 1–1. Pin List for the Stratix EP1S10 Device (Part 21 of 39)*

| Device | | | | | Package | | | | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin Fineline BGA | 672-Pin BGA | 672-Pin Fineline BGA | 780-Pin FineLine BGA | | |
| VCC_PLL5_OUTB | | | B10 | | | | | G16 | | |
| VCC_PLL5_OUTB | | | B10 | | | | | | | |
| IO | PLL5_OUT0p | | B9 | VREF0B3 | C13 | F13 | F13 | E15 | | |
| IO | PLL5_OUT0n | | B9 | VREF0B3 | B13 | E13 | E13 | D15 | | |
| IO | PLL5_OUT1p | | B9 | VREF0B3 | B12 | F14 | F14 | K14 | | |
| IO | PLL5_OUT1n | | B9 | VREF0B3 | A12 | E14 | E14 | K15 | | |
| IO | PLL5_FBp | | B9 | VREF0B3 | D12 | F12 | F12 | H14 | | |
| IO | PLL5_FBn | | B9 | VREF0B3 | C12 | E12 | E12 | H15 | | |
| IO | PLL5_OUT2p | | B10 | VREF0B3 | | | | C15 | | |
| IO | PLL5_OUT2n | | B10 | VREF0B3 | | | | B15 | | |
| IO | PLL5_OUT3p | | B10 | VREF0B3 | | | | K16 | | |
| IO | PLL5_OUT3n | | B10 | VREF0B3 | | | | J16 | | |
| nSTATUS | | nSTATUS | B3 | VREF0B3 | J12 | H13 | H13 | M16 | | |
| nCONFIG | | nCONFIG | B3 | VREF0B3 | H13 | H12 | H12 | L16 | | |
| DCLK | | DCLK | B3 | VREF0B3 | J13 | G12 | G12 | F16 | | |
| CONF_DONE | | CONF_DONE | B3 | VREF0B3 | K13 | H11 | H11 | G17 | | |
| CLK14p | | | B3 | VREF0B3 | B14 | B12 | B12 | K17 | | |
| IO | CLK14n | | B3 | VREF0B3 | C14 | A12 | A12 | J17 | | |
| CLK15p | | | B3 | VREF0B3 | E13 | D12 | D12 | M17 | | |
| IO | CLK15n | | B3 | VREF0B3 | D13 | C12 | C12 | L17 | | |
| VREF0B3 | | | B3 | VREF0B3 | H14 | F11 | F11 | E18 | | |
| IO | | DATA4 | B3 | VREF0B3 | K14 | E11 | E11 | H17 | | |

*Table 1–1. Pin List for the Stratix EP1S10 Device (Part 22 of 39)*

| Device | | | | | Package | | | | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin Fineline BGA | 672-Pin BGA | 672-Pin Fineline BGA | 780-Pin FineLine BGA | | |
| IO | | DATA5 | B3 | VREF0B3 | G14 | G11 | G11 | K18 | | |
| IO | | DATA6 | B3 | VREF0B3 | K15 | H10 | H10 | H18 | | |
| IO | RUP3 | | B3 | VREF0B3 | M15 | C11 | C11 | J18 | | |
| IO | RDN3 | | B3 | VREF0B3 | L15 | D11 | D11 | K19 | | |
| IO | DQ6T0 | | B3 | VREF0B3 | A15 | A10 | A10 | A18 | DQ1T0 | |
| IO | DQ6T1 | | B3 | VREF0B3 | C15 | E10 | E10 | C18 | DQ1T1 | |
| IO | | DATA7 | B3 | VREF0B3 | J15 | G10 | G10 | G18 | | |
| IO | DQ6T2 | | B3 | VREF0B3 | D14 | F10 | F10 | D18 | DQ1T2 | |
| IO | DQS6T | | B3 | VREF0B3 | F14 | G9 | G9 | B18 | | |
| IO | DQ6T3 | | B3 | VREF0B3 | E14 | F9 | F9 | A19 | DQ1T3 | |
| IO | | CLKUSR | B3 | VREF0B3 | L16 | D10 | D10 | J19 | | |
| GND | | | B3 | | | GND | GND | | | |
| GND | | | B3 | | | | | | | |
| GND | | | B3 | | G15 | F8 | F8 | G20 | | |
| IO | FCLK0 | | B3 | VREF0B3 | K16 | E9 | E9 | F19 | | |
| IO | FCLK1 | | B3 | VREF0B3 | J16 | B9 | B9 | G19 | | |
| IO | DQ6T4 | | B3 | VREF0B3 | D15 | C10 | C10 | B19 | DQ1T4 | |
| IO | DQ6T5 | | B3 | VREF0B3 | E15 | B10 | B10 | C19 | DQ1T5 | |
| IO | DQ6T6 | | B3 | VREF0B3 | F15 | A9 | A9 | E19 | DQ1T6 | |
| IO | DQ6T7 | | B3 | VREF0B3 | B15 | C9 | C9 | D19 | DQ1T7 | |
| IO | DQ7T0 | | B3 | VREF1B3 | A16 | A8 | A8 | B20 | DQ1T8 | |
| IO | DQ7T1 | | B3 | VREF1B3 | E16 | A7 | A7 | A20 | DQ1T9 | |

*Table 1–1. Pin List for the Stratix EP1S10 Device (Part 23 of 39)*

| Device | | | | | Package | | | | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin Fineline BGA | 672-Pin BGA | 672-Pin Fineline BGA | 780-Pin FineLine BGA | | |
| IO | DQ7T2 | | B3 | VREF1B3 | G16 | B8 | B8 | C20 | DQ1T10 | |
| IO | DQS7T | | B3 | VREF1B3 | B16 | | | D20 | DQS1T | |
| IO | DQ7T3 | | B3 | VREF1B3 | C16 | | | A21 | DQ1T11 | |
| IO | DQ7T4 | | B3 | VREF1B3 | D16 | | | B21 | DQ1T12 | |
| IO | DQ7T5 | | B3 | VREF1B3 | F16 | | | C21 | DQ1T13 | |
| IO | DQ8T0 | | B3 | VREF1B3 | A17 | B6 | B6 | B22 | DQ1T16 | |
| IO | DQ7T6 | | B3 | VREF1B3 | E17 | | | D21 | DQ1T14 | |
| IO | DQ8T1 | | B3 | VREF1B3 | B17 | A6 | A6 | A22 | DQ1T17 | |
| IO | DQ7T7 | | B3 | VREF1B3 | F17 | | | E21 | DQ1T15 | |
| IO | DQ8T2 | | B3 | VREF1B3 | C17 | F6 | F6 | C22 | DQ1T18 | |
| IO | DQS8T | | B3 | VREF1B3 | C18 | F5 | F5 | D23 | | |
| IO | DQ8T3 | | B3 | VREF1B3 | D17 | D6 | D6 | D22 | DQ1T19 | |
| IO | DQ8T4 | | B3 | VREF1B3 | E18 | E6 | E6 | A23 | DQ1T20 | |
| IO | DQ8T5 | | B3 | VREF1B3 | A18 | A5 | A5 | C23 | DQ1T21 | |
| IO | DQ8T6 | | B3 | VREF1B3 | B18 | E5 | E5 | E23 | DQ1T22 | |
| IO | DQ8T7 | | B3 | VREF1B3 | D18 | C7 | C7 | B23 | DQ1T23 | |
| VREF1B3 | | | B3 | VREF1B3 | H15 | D9 | D9 | E20 | | |
| IO | | | B3 | VREF1B3 | J14 | | | L18 | | |
| IO | | | B3 | VREF1B3 | | | | M18 | | |
| IO | DQ9T0 | | B3 | VREF1B3 | A19 | C3 | C3 | A24 | DQ1T24 | |
| IO | DQ9T1 | | B3 | VREF1B3 | B19 | A3 | A3 | C25 | DQ1T25 | |
| IO | DQ9T2 | | B3 | VREF1B3 | C19 | D5 | D5 | A25 | DQ1T26 | |

*Table 1–1. Pin List for the Stratix EP1S10 Device (Part 24 of 39)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **484-Pin Fineline BGA** | **672-Pin BGA** | **672-Pin Fineline BGA** | **780-Pin FineLine BGA** | **DQS for x32** | **DIFFIO Speed** *Note (1)* |
| IO | DQS9T | | B3 | VREF1B3 | C21 | B4 | B4 | C24 | | |
| IO | DQ9T3 | | B3 | VREF1B3 | D19 | C2 | C2 | D24 | DQ1T27 | |
| IO | DQ9T4 | | B3 | VREF1B3 | B20 | B3 | B3 | B24 | DQ1T28 | |
| IO | DQ9T5 | | B3 | VREF1B3 | B21 | D4 | D4 | B25 | DQ1T29 | |
| IO | DQ9T6 | | B3 | VREF1B3 | C20 | C4 | C4 | A26 | DQ1T30 | |
| IO | DQ9T7 | | B3 | VREF1B3 | D20 | D3 | D3 | B26 | DQ1T31 | |
| IO | | | B3 | VREF1B3 | M16 | | | F17 | | |
| VCCIO2 | | | | | C22 | D1 | D1 | B28 | | |
| VCCIO2 | | | | | K22 | L1 | L1 | M28 | | |
| VCCIO2 | | | | | | L9 | L9 | P20 | | |
| VCCIO1 | | | | | N22 | T1 | T1 | R20 | | |
| VCCIO1 | | | | | Y22 | AC1 | AC1 | U28 | | |
| VCCIO1 | | | | | | T9 | T9 | AG28 | | |
| VCCIO8 | | | | | AB20 | AF4 | AF4 | Y15 | | |
| VCCIO8 | | | | | AB13 | AF11 | AF11 | AH17 | | |
| VCCIO8 | | | | | | V11 | V11 | AH27 | | |
| VCCIO8 | | | | | | V12 | V12 | | | |
| VCCIO7 | | | | | AB10 | V15 | V15 | Y14 | | |
| VCCIO7 | | | | | AB3 | V16 | V16 | AH2 | | |
| VCCIO7 | | | | | | AF16 | AF16 | AH12 | | |
| VCCIO7 | | | | | | AF23 | AF23 | | | |
| VCCIO6 | | | | | Y1 | T18 | T18 | R9 | | |

*Table 1–1. Pin List for the Stratix EP1S10 Device (Part 25 of 39)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **484-Pin Fineline BGA** | **672-Pin BGA** | **672-Pin Fineline BGA** | **780-Pin FineLine BGA** | **DQS for x32** | **DIFFIO Speed** *Note (1)* |
| VCCIO6 | | | | | N1 | AC26 | AC26 | U1 | | |
| VCCIO6 | | | | | | T26 | T26 | AG1 | | |
| VCCIO5 | | | | | | L26 | L26 | B1 | | |
| VCCIO5 | | | | | K1 | L18 | L18 | M1 | | |
| VCCIO5 | | | | | C1 | D26 | D26 | P9 | | |
| VCCIO4 | | | | | | A23 | A23 | A2 | | |
| VCCIO4 | | | | | A3 | A16 | A16 | A12 | | |
| VCCIO4 | | | | | A10 | J15 | J15 | J14 | | |
| VCCIO4 | | | | | | J16 | J16 | | | |
| VCCIO3 | | | | | A13 | A4 | A4 | A17 | | |
| VCCIO3 | | | | | A20 | A11 | A11 | A27 | | |
| VCCIO3 | | | | | | J11 | J11 | J15 | | |
| VCCIO3 | | | | | | J12 | J12 | | | |
| VCCINT | | | | | A1 | K11 | K11 | M14 | | |
| VCCINT | | | | | A22 | K13 | K13 | N11 | | |
| VCCINT | | | | | AB1 | K15 | K15 | N13 | | |
| VCCINT | | | | | AB22 | K17 | K17 | N15 | | |
| VCCINT | | | | | K12 | L10 | L10 | N17 | | |
| VCCINT | | | | | L11 | L12 | L12 | P12 | | |
| VCCINT | | | | | L13 | L14 | L14 | P14 | | |
| VCCINT | | | | | L9 | L16 | L16 | P16 | | |
| VCCINT | | | | | M10 | M11 | M11 | R13 | | |

**Table 1–1. Pin List for the Stratix EP1S10 Device (Part 26 of 39)**

| Device | | | | | Package | | | | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin Fineline BGA | 672-Pin BGA | 672-Pin Fineline BGA | 780-Pin FineLine BGA | | |
| VCCINT | | | | | M12 | M13 | M13 | R15 | | |
| VCCINT | | | | | M14 | M15 | M15 | R17 | | |
| VCCINT | | | | | N11 | M17 | M17 | T12 | | |
| VCCINT | | | | | | N10 | N10 | T14 | | |
| VCCINT | | | | | | N12 | N12 | T16 | | |
| VCCINT | | | | | | N14 | N14 | T18 | | |
| VCCINT | | | | | | N16 | N16 | U11 | | |
| VCCINT | | | | | | P11 | P11 | U13 | | |
| VCCINT | | | | | | P13 | P13 | U15 | | |
| VCCINT | | | | | | P15 | P15 | U17 | | |
| VCCINT | | | | | | P17 | P17 | V12 | | |
| VCCINT | | | | | | R10 | R10 | V16 | | |
| VCCINT | | | | | | R12 | R12 | | | |
| VCCINT | | | | | | R14 | R14 | | | |
| VCCINT | | | | | | R16 | R16 | | | |
| VCCINT | | | | | | T11 | T11 | | | |
| VCCINT | | | | | | T13 | T13 | | | |
| VCCINT | | | | | | T15 | T15 | | | |
| VCCINT | | | | | | T17 | T17 | | | |
| VCCINT | | | | | | U10 | U10 | | | |
| VCCINT | | | | | | U12 | U12 | | | |
| VCCINT | | | | | | U14 | U14 | | | |

*Table 1–1. Pin List for the Stratix EP1S10 Device (Part 27 of 39)*

| Device | | | | | Package | | | | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **484-Pin Fineline BGA** | **672-Pin BGA** | **672-Pin Fineline BGA** | **780-Pin FineLine BGA** | | |
| VCCINT | | | | | | U16 | U16 | | | |
| GND | | | | | A14 | A13 | A13 | A14 | | |
| GND | | | | | A2 | A14 | A14 | A15 | | |
| GND | | | | | A21 | A2 | A2 | AA16 | | |
| GND | | | | | A9 | A25 | A25 | AC15 | | |
| GND | | | | | AA1 | AC13 | AC13 | AF26 | | |
| GND | | | | | AA22 | AE1 | AE1 | AF3 | | |
| GND | | | | | AB14 | AE26 | AE26 | AG2 | | |
| GND | | | | | AB2 | AF13 | AF13 | AG27 | | |
| GND | | | | | AB21 | AF14 | AF14 | AH14 | | |
| GND | | | | | AB9 | AF2 | AF2 | AH15 | | |
| GND | | | | | B1 | AF25 | AF25 | B2 | | |
| GND | | | | | B22 | B1 | B1 | B27 | | |
| GND | | | | | G17 | B2 | B2 | C26 | | |
| GND | | | | | G6 | B26 | B26 | C3 | | |
| GND | | | | | J1 | C13 | C13 | G15 | | |
| GND | | | | | J22 | G8 | G8 | H16 | | |
| GND | | | | | K11 | H17 | H17 | L14 | | |
| GND | | | | | L10 | H9 | H9 | L15 | | |
| GND | | | | | L12 | J10 | J10 | M15 | | |
| GND | | | | | L14 | J13 | J13 | N12 | | |
| GND | | | | | M11 | J14 | J14 | N14 | | |

*Table 1–1. Pin List for the Stratix EP1S10 Device (Part 28 of 39)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin Fineline BGA | 672-Pin BGA | 672-Pin Fineline BGA | 780-Pin FineLine BGA | DQS for x32 | DIFFIO Speed *Note (1)* |
| GND | | | | | M13 | J17 | J17 | N16 | | |
| GND | | | | | M9 | J9 | J9 | N18 | | |
| GND | | | | | N12 | K10 | K10 | P1 | | |
| GND | | | | | P1 | K12 | K12 | P11 | | |
| GND | | | | | P22 | K14 | K14 | P13 | | |
| GND | | | | | T17 | K16 | K16 | P15 | | |
| GND | | | | | T6 | K18 | K18 | P17 | | |
| GND | | | | | | L11 | L11 | P18 | | |
| GND | | | | | | L13 | L13 | P28 | | |
| GND | | | | | | L15 | L15 | R1 | | |
| GND | | | | | | L17 | L17 | R11 | | |
| GND | | | | | | M10 | M10 | R12 | | |
| GND | | | | | | M12 | M12 | R14 | | |
| GND | | | | | | M14 | M14 | R16 | | |
| GND | | | | | | M16 | M16 | R18 | | |
| GND | | | | | | N1 | N1 | R28 | | |
| GND | | | | | | N11 | N11 | T11 | | |
| GND | | | | | | N13 | N13 | T13 | | |
| GND | | | | | | N15 | N15 | T15 | | |
| GND | | | | | | N17 | N17 | T17 | | |
| GND | | | | | | N18 | N18 | U12 | | |
| GND | | | | | | N26 | N26 | U14 | | |

*Table 1–1. Pin List for the Stratix EP1S10 Device (Part 29 of 39)*

| Device | | | | | Package | | | | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin Fineline BGA | 672-Pin BGA | 672-Pin Fineline BGA | 780-Pin FineLine BGA | | |
| GND | | | | | | N9 | N9 | U16 | | |
| GND | | | | | | P1 | P1 | U18 | | |
| GND | | | | | | P10 | P10 | V13 | | |
| GND | | | | | | P12 | P12 | V14 | | |
| GND | | | | | | P14 | P14 | V15 | | |
| GND | | | | | | P16 | P16 | V17 | | |
| GND | | | | | | P18 | P18 | | | |
| GND | | | | | | P26 | P26 | | | |
| GND | | | | | | P9 | P9 | | | |
| GND | | | | | | R11 | R11 | | | |
| GND | | | | | | R13 | R13 | | | |
| GND | | | | | | R15 | R15 | | | |
| GND | | | | | | R17 | R17 | | | |
| GND | | | | | | T10 | T10 | | | |
| GND | | | | | | T12 | T12 | | | |
| GND | | | | | | T14 | T14 | | | |
| GND | | | | | | T16 | T16 | | | |
| GND | | | | | | U11 | U11 | | | |
| GND | | | | | | U13 | U13 | | | |
| GND | | | | | | U15 | U15 | | | |
| GND | | | | | | U17 | U17 | | | |
| GND | | | | | | V10 | V10 | | | |

**Table 1–1. Pin List for the Stratix EP1S10 Device (Part 30 of 39)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin Fineline BGA | 672-Pin BGA | 672-Pin Fineline BGA | 780-Pin FineLine BGA | DQS for x32 | DIFFIO Speed *Note (1)* |
| GND | | | | | | V13 | V13 | | | |
| GND | | | | | | V14 | V14 | | | |
| GND | | | | | | V17 | V17 | | | |
| GND | | | | | | V18 | V18 | | | |
| GND | | | | | | V9 | V9 | | | |
| No connection | | | | | AA10 | A18 | A18 | A13 | | |
| No connection | | | | | AA9 | AA16 | AA16 | A16 | | |
| No connection | | | | | B10 | AB1 | AB1 | AA10 | | |
| No connection | | | | | B9 | AB2 | AB2 | AA21 | | |
| No connection | | | | | C10 | AB25 | AB25 | AA22 | | |
| No connection | | | | | C11 | AB26 | AB26 | AA23 | | |
| No connection | | | | | D10 | AB6 | AB6 | AA24 | | |
| No connection | | | | | D11 | AB8 | AB8 | AA5 | | |
| No connection | | | | | E10 | AC18 | AC18 | AA6 | | |
| No connection | | | | | E11 | AC19 | AC19 | AA7 | | |
| No connection | | | | | E12 | AC5 | AC5 | AA8 | | |
| No connection | | | | | E3 | AC6 | AC6 | AA9 | | |
| No connection | | | | | E4 | AC8 | AC8 | AB12 | | |
| No connection | | | | | F19 | AD11 | AD11 | AB20 | | |
| No connection | | | | | F20 | AD18 | AD18 | AB21 | | |
| No connection | | | | | H16 | AD19 | AD19 | AB22 | | |
| No connection | | | | | H9 | AD21 | AD21 | AB23 | | |

**Table 1–1. Pin List for the Stratix EP1S10 Device (Part 31 of 39)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin Fineline BGA | 672-Pin BGA | 672-Pin Fineline BGA | 780-Pin FineLine BGA | DQS for x32 | DIFFIO Speed *Note (1)* |
| No connection | | | | | R14 | AD22 | AD22 | AB24 | | |
| No connection | | | | | R5 | AD23 | AD23 | AB25 | | |
| No connection | | | | | U3 | AD24 | AD24 | AB26 | | |
| No connection | | | | | U4 | AD8 | AD8 | AB3 | | |
| No connection | | | | | V10 | AE18 | AE18 | AB4 | | |
| No connection | | | | | V11 | AE19 | AE19 | AB5 | | |
| No connection | | | | | V12 | AE8 | AE8 | AB6 | | |
| No connection | | | | | V19 | AF20 | AF20 | AB8 | | |
| No connection | | | | | V20 | AF5 | AF5 | AB9 | | |
| No connection | | | | | W10 | B11 | B11 | AC1 | | |
| No connection | | | | | W11 | B16 | B16 | AC2 | | |
| No connection | | | | | Y10 | B19 | B19 | AC20 | | |
| No connection | | | | | Y11 | B21 | B21 | AC22 | | |
| No connection | | | | | | B23 | B23 | AC23 | | |
| No connection | | | | | | B25 | B25 | AC24 | | |
| No connection | | | | | | B5 | B5 | AC25 | | |
| No connection | | | | | | B7 | B7 | AC26 | | |
| No connection | | | | | | C19 | C19 | AC27 | | |
| No connection | | | | | | C5 | C5 | AC28 | | |
| No connection | | | | | | C6 | C6 | AC3 | | |
| No connection | | | | | | C8 | C8 | AC4 | | |
| No connection | | | | | | D19 | D19 | AC5 | | |

Table 1–1. Pin List for the Stratix EP1S10 Device (Part 32 of 39)

| Device | | | | | Package | | | | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **484-Pin Fineline BGA** | **672-Pin BGA** | **672-Pin Fineline BGA** | **780-Pin FineLine BGA** | | |
| No connection | | | | | | D7 | D7 | AC6 | | |
| No connection | | | | | | D8 | D8 | AC7 | | |
| No connection | | | | | | E1 | E1 | AD1 | | |
| No connection | | | | | | E19 | E19 | AD12 | | |
| No connection | | | | | | E2 | E2 | AD13 | | |
| No connection | | | | | | E20 | E20 | AD16 | | |
| No connection | | | | | | E25 | E25 | AD17 | | |
| No connection | | | | | | E26 | E26 | AD2 | | |
| No connection | | | | | | E7 | E7 | AD24 | | |
| No connection | | | | | | E8 | E8 | AD25 | | |
| No connection | | | | | | F20 | F20 | AD26 | | |
| No connection | | | | | | F7 | F7 | AD27 | | |
| No connection | | | | | | G16 | G16 | AD28 | | |
| No connection | | | | | | G7 | G7 | AD3 | | |
| No connection | | | | | | H1 | H1 | AD4 | | |
| No connection | | | | | | H19 | H19 | AD5 | | |
| No connection | | | | | | H2 | H2 | AD7 | | |
| No connection | | | | | | H20 | H20 | AE1 | | |
| No connection | | | | | | H21 | H21 | AE12 | | |
| No connection | | | | | | H22 | H22 | AE13 | | |
| No connection | | | | | | H23 | H23 | AE16 | | |
| No connection | | | | | | H24 | H24 | AE17 | | |

*Table 1–1. Pin List for the Stratix EP1S10 Device  (Part 33 of 39)*

| Device | | | | | Package | | | | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **484-Pin Fineline BGA** | **672-Pin BGA** | **672-Pin Fineline BGA** | **780-Pin FineLine BGA** | | |
| No connection | | | | | | H25 | H25 | AE2 | | |
| No connection | | | | | | H26 | H26 | AE25 | | |
| No connection | | | | | | H5 | H5 | AE26 | | |
| No connection | | | | | | H6 | H6 | AE27 | | |
| No connection | | | | | | H7 | H7 | AE28 | | |
| No connection | | | | | | J1 | J1 | AF1 | | |
| No connection | | | | | | J19 | J19 | AF12 | | |
| No connection | | | | | | J2 | J2 | AF13 | | |
| No connection | | | | | | J20 | J20 | AF16 | | |
| No connection | | | | | | J23 | J23 | AF17 | | |
| No connection | | | | | | J24 | J24 | AF2 | | |
| No connection | | | | | | J25 | J25 | AF27 | | |
| No connection | | | | | | J26 | J26 | AF28 | | |
| No connection | | | | | | J3 | J3 | AG12 | | |
| No connection | | | | | | J4 | J4 | AG13 | | |
| No connection | | | | | | J5 | J5 | AG16 | | |
| No connection | | | | | | J6 | J6 | AG17 | | |
| No connection | | | | | | J7 | J7 | AH13 | | |
| No connection | | | | | | J8 | J8 | AH16 | | |
| No connection | | | | | | K1 | K1 | AH18 | | |
| No connection | | | | | | K2 | K2 | B12 | | |
| No connection | | | | | | K21 | K21 | B13 | | |

**Table 1–1. Pin List for the Stratix EP1S10 Device (Part 34 of 39)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin Fineline BGA | 672-Pin BGA | 672-Pin Fineline BGA | 780-Pin FineLine BGA | DQS for x32 | DIFFIO Speed *Note (1)* |
| No connection | | | | | | K22 | K22 | B16 | | |
| No connection | | | | | | K25 | K25 | B17 | | |
| No connection | | | | | | K26 | K26 | C1 | | |
| No connection | | | | | | K7 | K7 | C12 | | |
| No connection | | | | | | K8 | K8 | C13 | | |
| No connection | | | | | | K9 | K9 | C16 | | |
| No connection | | | | | | R18 | R18 | C17 | | |
| No connection | | | | | | U18 | U18 | C2 | | |
| No connection | | | | | | U19 | U19 | C27 | | |
| No connection | | | | | | U20 | U20 | C28 | | |
| No connection | | | | | | U25 | U25 | D1 | | |
| No connection | | | | | | U26 | U26 | D12 | | |
| No connection | | | | | | U3 | U3 | D13 | | |
| No connection | | | | | | U4 | U4 | D16 | | |
| No connection | | | | | | U7 | U7 | D17 | | |
| No connection | | | | | | U8 | U8 | D2 | | |
| No connection | | | | | | U9 | U9 | D25 | | |
| No connection | | | | | | V1 | V1 | D26 | | |
| No connection | | | | | | V19 | V19 | D27 | | |
| No connection | | | | | | V2 | V2 | D28 | | |
| No connection | | | | | | V21 | V21 | D3 | | |
| No connection | | | | | | V22 | V22 | D4 | | |

*Table 1–1. Pin List for the Stratix EP1S10 Device (Part 35 of 39)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin Fineline BGA | 672-Pin BGA | 672-Pin Fineline BGA | 780-Pin FineLine BGA | DQS for x32 | DIFFIO Speed *Note (1)* |
| No connection | | | | | | V23 | V23 | E1 | | |
| No connection | | | | | | V24 | V24 | E11 | | |
| No connection | | | | | | V25 | V25 | E12 | | |
| No connection | | | | | | V26 | V26 | E13 | | |
| No connection | | | | | | V3 | V3 | E16 | | |
| No connection | | | | | | V4 | V4 | E17 | | |
| No connection | | | | | | V8 | V8 | E2 | | |
| No connection | | | | | | W1 | W1 | E22 | | |
| No connection | | | | | | W11 | W11 | E25 | | |
| No connection | | | | | | W19 | W19 | E26 | | |
| No connection | | | | | | W2 | W2 | E27 | | |
| No connection | | | | | | W20 | W20 | E28 | | |
| No connection | | | | | | W21 | W21 | E3 | | |
| No connection | | | | | | W22 | W22 | E4 | | |
| No connection | | | | | | W23 | W23 | E5 | | |
| No connection | | | | | | W24 | W24 | F1 | | |
| No connection | | | | | | W25 | W25 | F11 | | |
| No connection | | | | | | W26 | W26 | F18 | | |
| No connection | | | | | | W3 | W3 | F2 | | |
| No connection | | | | | | W4 | W4 | F20 | | |
| No connection | | | | | | W5 | W5 | F21 | | |
| No connection | | | | | | W6 | W6 | F22 | | |

Table 1–1. Pin List for the Stratix EP1S10 Device (Part 36 of 39)

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin Fineline BGA | 672-Pin BGA | 672-Pin Fineline BGA | 780-Pin FineLine BGA | DQS for x32 | DIFFIO Speed Note (1) |
| No connection | | | | | | W7 | W7 | F23 | | |
| No connection | | | | | | W8 | W8 | F24 | | |
| No connection | | | | | | Y19 | Y19 | F25 | | |
| No connection | | | | | | Y3 | Y3 | F26 | | |
| No connection | | | | | | Y4 | Y4 | F27 | | |
| No connection | | | | | | Y7 | Y7 | F28 | | |
| No connection | | | | | | Y9 | Y9 | F3 | | |
| No connection | | | | | | | | F4 | | |
| No connection | | | | | | | | F5 | | |
| No connection | | | | | | | | F6 | | |
| No connection | | | | | | | | F7 | | |
| No connection | | | | | | | | F9 | | |
| No connection | | | | | | | | G12 | | |
| No connection | | | | | | | | G21 | | |
| No connection | | | | | | | | G22 | | |
| No connection | | | | | | | | G23 | | |
| No connection | | | | | | | | G24 | | |
| No connection | | | | | | | | G25 | | |
| No connection | | | | | | | | G26 | | |
| No connection | | | | | | | | G3 | | |
| No connection | | | | | | | | G4 | | |
| No connection | | | | | | | | G5 | | |

*Table 1–1. Pin List for the Stratix EP1S10 Device (Part 37 of 39)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin Fineline BGA | 672-Pin BGA | 672-Pin Fineline BGA | 780-Pin FineLine BGA | DQS for x32 | DIFFIO Speed *Note (1)* |
| No connection | | | | | | | | G6 | | |
| No connection | | | | | | | | G8 | | |
| No connection | | | | | | | | G9 | | |
| No connection | | | | | | | | H10 | | |
| No connection | | | | | | | | H19 | | |
| No connection | | | | | | | | H20 | | |
| No connection | | | | | | | | H21 | | |
| No connection | | | | | | | | H22 | | |
| No connection | | | | | | | | H23 | | |
| No connection | | | | | | | | H24 | | |
| No connection | | | | | | | | H5 | | |
| No connection | | | | | | | | H6 | | |
| No connection | | | | | | | | H7 | | |
| No connection | | | | | | | | H8 | | |
| No connection | | | | | | | | H9 | | |
| No connection | | | | | | | | J10 | | |
| No connection | | | | | | | | J20 | | |
| No connection | | | | | | | | J21 | | |
| No connection | | | | | | | | J22 | | |
| No connection | | | | | | | | J23 | | |
| No connection | | | | | | | | J24 | | |
| No connection | | | | | | | | J5 | | |

Table 1–1. Pin List for the Stratix EP1S10 Device (Part 38 of 39)

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin Fineline BGA | 672-Pin BGA | 672-Pin Fineline BGA | 780-Pin FineLine BGA | DQS for x32 | DIFFIO Speed *Note (1)* |
| No connection | | | | | | | | J6 | | |
| No connection | | | | | | | | J7 | | |
| No connection | | | | | | | | J8 | | |
| No connection | | | | | | | | K10 | | |
| No connection | | | | | | | | K23 | | |
| No connection | | | | | | | | K24 | | |
| No connection | | | | | | | | K5 | | |
| No connection | | | | | | | | K6 | | |
| No connection | | | | | | | | P19 | | |
| No connection | | | | | | | | R10 | | |
| No connection | | | | | | | | W21 | | |
| No connection | | | | | | | | W22 | | |
| No connection | | | | | | | | W7 | | |
| No connection | | | | | | | | W8 | | |
| No connection | | | | | | | | Y10 | | |
| No connection | | | | | | | | Y20 | | |
| No connection | | | | | | | | Y21 | | |
| No connection | | | | | | | | Y22 | | |
| No connection | | | | | | | | Y23 | | |
| No connection | | | | | | | | Y24 | | |
| No connection | | | | | | | | Y5 | | |
| No connection | | | | | | | | Y6 | | |

**Table 1–1. Pin List for the Stratix EP1S10 Device (Part 39 of 39)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin Fineline BGA | 672-Pin BGA | 672-Pin Fineline BGA | 780-Pin FineLine BGA | DQS for x32 | DIFFIO Speed *Note (1)* |
| No connection | | | | | | | | Y7 | | |
| No connection | | | | | | | | Y8 | | |

*Note to Table 1–1:*

(1) The wire bond and flip-chip packages have different data rates for the high speed differential I/O channels. Table 1–2 shows the data rates as supported for each package.

**Table 1–2. High Speed Differential I/O Channel Data Rates**

| Package | Package Type | High Speed Differential I/O Channel Performance (DIFFIO Speed) | | Units |
|---|---|---|---|---|
| | | High | Low | |
| 484-pin FineLine BGA | flip chip | 840 | N/A | Mbps |
| 672-pin BGA | wire bond | 462 | N/A | Mbps |
| 672-pin FineLine BGA | wire bond | 462 | N/A | Mbps |
| 780-pin FineLine BGA | flip chip | 840 | N/A | Mbps |

## Pin Definitions

Table 1–3 shows pin definitions for the EP1S10 device.

*Table 1–3. Pin Definitions (Part 1 of 5)*

| Pin Name | Pin Type (1st, 2nd, & 3rd Function) | Pin Description |
|---|---|---|
| **Supply and Reference Pins** | | |
| VREF[1..4]B[1..8] | Input | Input reference voltage for each I/O bank. If a bank is used for a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for that bank. All of the VREF pins within a bank are shorted together. Each VREF pin can support up to 20 inputs on each side. If VREF pins are not used, designers should connect them to either VCC or Gnd. |
| VCCIO[1..8] | Power | These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards. VCCIO also supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5-V, 1.8-V, 2.5-V, 3.3-V PCI, and 3.3-V PCI-X I/O standards. |
| VCCINT | Power | These are internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVDS, LVPECL, 3.3-V PCML, HyperTransport™ technology, differential HSTL, GTL, GTL+, HSTL, SSTL, CTT, and 3.3-V AGP I/O standards. |
| VCC_PLL5_OUTA | Power | External clock output buffer power for PLL5 clock outputs PLL5_OUT[1..0]. The designer must connect this pin to the VCCIO of bank 9. |
| VCC_PLL5_OUTB | Power | External clock output buffer power for PLL5 clock outputs PLL5_OUT[3..2]. The designer must connect this pin to the VCCIO of bank 10. |
| VCC_PLL6_OUTA | Power | External clock output buffer power for PLL6 clock outputs PLL6_OUT[1..0]. The designer must connect this pin to the VCCIO of bank 11. |
| VCC_PLL6_OUTB | Power | External clock output buffer power for PLL6 clock outputs PLL6_OUT[3..2]. The designer must connect this pin to the VCCIO of bank 12. |
| VCCA_PLL[1..12] | Power | Analog power for PLLs[1..12]. The designer must connect this pin to 1.5 V, even if the PLL is not used. |
| GNDA_PLL[1..12] | Ground | Analog ground for PLLs[1..12]. The designer can connect this pin to the GND plane on the board. |
| VCCG_PLL[1..12] | Power | Guard ring power for PLLs[1..12]. The designer must connect this pin to 1.5 V, even if the PLL is not used. |
| GNDG_PLL[1..12] | Ground | Guard ring ground for PLLs[1..12]. The designer can connect this pin to the GND plane on the board. |

*Table 1–3. Pin Definitions (Part 2 of 5)*

| Pin Name | Pin Type (1st, 2nd, & 3rd Function) | Pin Description |
|---|---|---|
| **Dedicated & Configuration/JTAG Pins** | | |
| CONF_DONE | Bidirectional (open-drain) | This is a dedicated configuration status pin; it is not available as a user I/O pin. |
| nSTATUS | Bidirectional (open-drain) | This is a dedicated configuration status pin; it is not available as a user I/O pin. |
| nCONFIG | Input | Dedicated configuration control input. A low transition resets the target device; a low-to-high transition begins configuration. All I/O pins tri-state when nCONFIG is driven low. |
| DCLK | Input | Clock input used to clock configuration data from an external source into the Stratix device. This is a dedicated pin used for configuration. |
| nIO_PULLUP | Input | IF nIO_PULLUP is driven high during configuration, the weak pull-ups on all user I/O pins are disabled. If driven low, the weak pull-ups are enabled during configuration. nIO_PULLUP can be pulled up to either 1.5, 1.8, 2.5, or 3.3 V. |
| PORSEL | Input | Dedicated input pin used to select POR delay times of 2 ms or 100 ms during powerup. When PORSEL is connected to ground, the POR time is 100 ms. When PORSEL is connected to 3.3 V, the POR time is 2 ms. |
| VCCSEL | Input | VCCSEL is used to select which input buffer is used on all configuration pins. VCCSEL will control whether the 3.3-/2.5-V input buffer or the 1.8-/1.5-V input buffer is used. A "0" means 3.3/2.5 V and a "1" means 1.8-/1.5 V. At powerup, VCCSEL accepts 3.3V and 2.5V TTL Levels. VCCSEL affects the following pins: TDI, TMS, TCK, TRST, MSEL0, MSEL1, MSEL2, nCONFIG, nCE, DCLK, CONF_DONE, nSTATUS, and PLL_ENA. |
| nCE | Input | Active-low chip enables. Dedicated chip enable input used to detect which device is active in a chain of devices. When nCE is low, the device is enabled. When nCE is high, the device is disabled. |
| nCEO | Output | Output that drives low when device configuration is complete. During multi-device configuration, this pin feeds a subsequent device’s nCE pin. |
| TMS | Input | This is a dedicated JTAG input pin. |
| TDI | Input | This is a dedicated JTAG input pin. |
| TCK | Input | This is a dedicated JTAG input pin. |
| TDO | Output | This is a dedicated JTAG input pin. |

**Table 1–3. Pin Definitions (Part 3 of 5)**

| Pin Name | Pin Type (1st, 2nd, & 3rd Function) | Pin Description |
|---|---|---|
| TRST | Input | This is a dedicated JTAG input pin. Active low input, used to asynchronously reset the JTAG boundary scan circuit. |
| MSEL[2..0] | Input | Dedicated mode select control pins that set the configuration mode for the device. |
| TEMPDIODEp | Input | Pin used in conjunction with the temperature sensing diode (bias-high input) inside the Stratix device. If the temperature sensing diode is not used then connect this pin to GND. |
| TEMPDIODEn | Input | Pin used in conjunction with the temperature sensing diode (bias-low input) inside the Stratix device. If the temperature sensing diode is not used then connect this pin to GND. |
| **Clock and PLL Pins** | | |
| PLL_ENA | Input | Dedicated input pin that drives the optional pllena port of all or a set of PLLs. If a PLL uses the pllena port, drive the PLL_ENA pin low to reset all PLLs including the counters to their default state. If VCCSEL = 0, then you must drive the PLL_ENA with a 3.3/2.5 V signal to enable the PLLs. If VCCSEL = 1, connect PLL_ENA to 1.8/1.5 V to enable the PLLs. |
| FCLK[7..0] | Bidirectional | Optional fast regional clock pins. FCLK pins can also be used as type input, output, or as bidirectional pins. |
| CLK[15..0]p | Input | Dedicated global clock inputs 0 to 15. |
| CLK[15..0]n | I/O, Input | Optional negative terminal input for differential global clock input. |
| PLL6_OUT[3..0]p | I/O, Output | Optional external clock outputs [3..0] from enhanced PLL 6. These pins can be differential (four output pin pairs) or single ended (eight clock outputs from PLL6). |
| PLL6_OUT[3..0]n | I/O, Output | Optional negative terminal for external clock outputs [3..0] from PLL6. If the clock outputs are single ended, then each pair of pins (i.e., PLL6_OUT0p and PLL6_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase. |
| PLL5_OUT[3..0]p | I/O, Output | Optional external clock outputs [3..0] from enhanced PLL 5. These pins can be differential (four output pin pairs) or single ended (eight clock outputs from PLL5). |
| PLL5_OUT[3..0]n | I/O, Output | Optional negative terminal for external clock outputs [3..0] from PLL 5. If the clock outputs are single ended, then each pair of pins (i.e., PLL5_OUT0p and PLL5_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase. |

*Table 1–3. Pin Definitions (Part 4 of 5)*

| Pin Name | Pin Type (1st, 2nd, & 3rd Function) | Pin Description |
|---|---|---|
| **Optional/Dual-Purpose Pins** | | |
| DATA0 | I/O, Input | Dual-purpose configuration data input pin. Can be used as an I/O pin after configuration is complete. |
| DIFFIO_TX[0..151]n | I/O, Output | This pin can be used as the complementary signal of the differential inputs and outputs. If not used for the differential pair, these pins are regular I/O pins. Pins with an n suffix carry the negative signal for the differential channel. Pins with a p suffix carry the positive signal for the differential channel. |
| PLL5_FBp | I/O, Input | External feedback input pin for PLL5. This pin can be used as a user I/O pin if external feedback mode is not used. |
| PLL5_FBn | I/O, Input | Negative terminal input for external feedback input PLL5_FBp |
| PLL6_FBp | I/O, Input | External feedback input pin for PLL6 |
| PLL6_FBn | I/O, Input | Negative terminal input for external feedback input PLL6_FBp |
| INIT_DONE | I/O, Output | This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration. |
| DATA[7..1] | I/O, Input | Dual-purpose configuration input data pins. These pins can be used for configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration. |
| nRS | I/O, Input | Read strobe input pin. This pin can be used as a user I/O pin after configuration. |
| DEV_CLRn | I/O, Input | Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as defined in the users design. |
| DEV_OE | I/O, Input | Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design. |
| CLKUSR | I/O, Input | Optional user-supplied clock input. Synchronizes the initialization of one or more devices. This pin can be used as a user I/O pin after configuration. |
| RDYnBSY | I/O, Output | Ready not busy output. A high output indicates that the target device is ready to accept another data byte. A low output indicates that the target device is not ready to receive another data byte. This pin can be used as a user I/O pin after configuration |

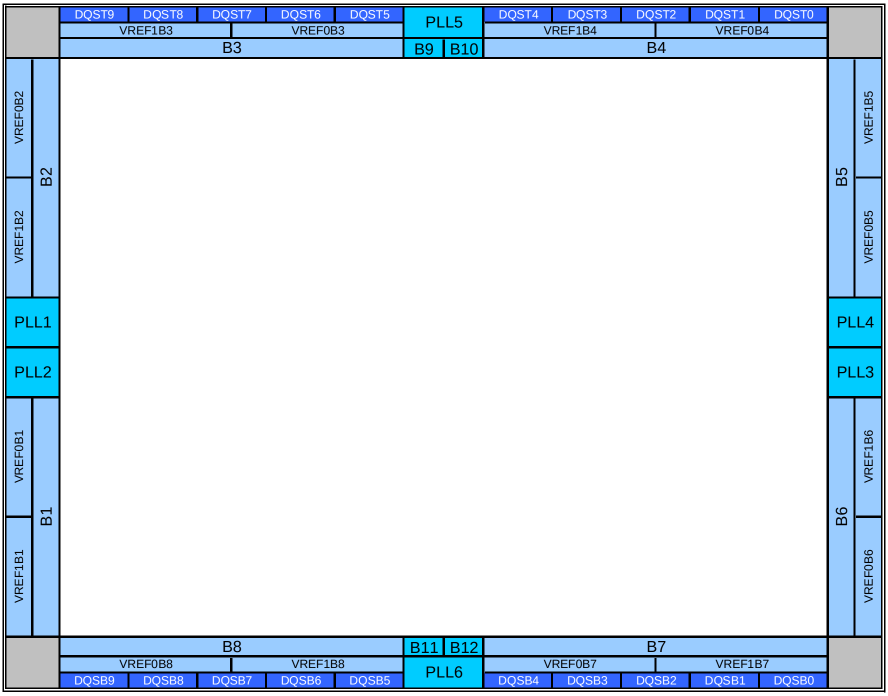
*Table 1–3. Pin Definitions (Part 5 of 5)*

| Pin Name | Pin Type (1st, 2nd, & 3rd Function) | Pin Description |
|---|---|---|
| nCS,CS | I/O, Input | These are chip-select inputs that enable the Stratix device in the passive parallel asynchronous configuration mode. Drive nCS low and CS high to target a device for configuration. If a design requires an active high enable, use the CS pin and drive the nCS pin low. If a design requires an active low enable, use the nCS pin and drive the CS pin high. Configuration will be paused when either signal is inactive. Hold the nCS and CS pins active during configuration and initialization. The design can use these pins as user I/O pins after configuration. |
| nWS | I/O, Input | Active-low write strobe input to latch a byte of data on the DATA pins. This pin can be used as a user I/O pin after configuration. |
| PGM[2..0] | I/O, Output | These output pins control one of eight pages in the EPC16 configuration device when using remote update or local update configuration modes. When not using remote update or local update configuration modes, these pins are user I/O pins. |
| RUP[8..1] | I/O, Input | Reference pins for banks 8 to 1. The external precision resistors $R_{UP}$ must be connected to the designated RUP pin on that I/O bank. If not required, these pins are regular I/O pins. |
| RDN[8..1] | I/O, Input | Reference pins for banks 8 to 1. The external precision resistors RDN must be connected to the designated RDN pin on that I/O bank. If not required, these pins are regular I/O pins. |
| RUnLU | I/O, Input | Input control pin to select remote update or local update modes. If MSEL2 = 1, this is a input control pin to select remote update (RUnLU =1) or local update (RUnLU =0) modes. If MSEL2 = 0, the RUnLU pin is a user I/O pin. |

## PLL & Bank Diagram

Figure 1–1 shows the PLL and bank locations for the EP1S10 device.

*Figure 1–1. PLL and Bank Diagram Notes (1), (2)*



*Notes for Figure 1–1:*

(1) This is a top view of the silicon die. The die is mounted upside down in flip-chip packages and rightside up in wire-bond packages.

(2) This is a pictoral representation only, to give an idea of placement on the device. Refer to the pinlist and the Quartus II software for exact locations.

## Fast PLL to High-Speed I/O Connections

Table 1–4 shows the number of shows the number of high-speed differential I/O channels that can be driven by each Fast PLL for the EP1S10 device.

*Table 1–4. Fast PLL Connections for the EP1S10 Device*

| Device | Pin Count | FAST PLL Source Location | Number of Rx Channels *(1) (5)* | Number of Tx Channels *(2) (5)* | Number of Overlapped Rx Channels *(3)* | Number of Overlapped Tx Channels *(4)* |
|---|---|---|---|---|---|---|
| EP1S10 | 484 | PLL1 | 5/0 | 5/0 | | |
| | | PLL2 | 5/0 | 5/0 | | |
| | | PLL3 | 5/0 | 5/0 | | |
| | | PLL4 | 5/0 | 5/0 | | |
| | 672 | PLL1 | 0/9 | 0/9 | | |
| | | PLL2 | 0/9 | 0/9 | | |
| | | PLL3 | 0/9 | 0/9 | | |
| | | PLL4 | 0/9 | 0/9 | | |
| | 780 | PLL1 | 11/0 | 11/0 | | |
| | | PLL2 | 11/0 | 11/0 | | |
| | | PLL3 | 11/0 | 11/0 | | |
| | | PLL4 | 11/0 | 11/0 | | |

*Notes for Table 1–4:*

(1) This is the total number of Rx channels that the PLL listed in the "FAST PLL Source location" column can drive.

(2) This is the total number of Tx channels that the PLL listed in the "FAST PLL Source location" column can drive.

(3) This is the number of Rx channels that can be driven by the PLL listed in the "FAST PLL Source location" that could alternatively be driven by the other adjacent FAST PLL.

(4) This is the number of Tx channels that can be driven by the PLL listed in the "FAST PLL Source location" that could alternatively be driven by the other adjacent FAST PLL.

(5) The counts are reported in the format of (high speed channels)/(low speed channels).

# 2. Stratix EP1S20 Device Pin Information

S5V3002-1.0

## Introduction

The following tables contain pin information for the Stratix EP1S20 device, organized into the following sections:

**Section** **Page**

# Pin List

Table 2–1 shows the complete pin list for the EP1S20 device:

*Table 2–1. Pin List for the Stratix EP1S20 Device (Part 1 of 39)*

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin FBGA | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | | | |
| IO | DIFFIO_RX32p | | B2 | VREF0B2 | | C1 | C1 | C27 | | | HIGH |
| IO | DIFFIO_RX32n | | B2 | VREF0B2 | F18 | D2 | D2 | C28 | | | HIGH |
| IO | DIFFIO_TX32p | | B2 | VREF0B2 | E19 | E3 | E3 | G23 | | | HIGH |
| IO | DIFFIO_TX32n | | B2 | VREF0B2 | E20 | E4 | E4 | G24 | | | HIGH |
| IO | DIFFIO_RX31p | | B2 | VREF0B2 | | E1 | E1 | D27 | | | HIGH |
| IO | DIFFIO_RX31n | | B2 | VREF0B2 | | E2 | E2 | D28 | | | HIGH |
| IO | DIFFIO_TX31p | | B2 | VREF0B2 | | F3 | F3 | H24 | | | HIGH |
| IO | DIFFIO_TX31n | | B2 | VREF0B2 | G18 | F4 | F4 | H23 | | | HIGH |
| IO | DIFFIO_RX30p | | B2 | VREF0B2 | | F1 | F1 | E27 | | | HIGH |
| IO | DIFFIO_RX30n | | B2 | VREF0B2 | | F2 | F2 | E28 | | | HIGH |
| IO | DIFFIO_TX30p | | B2 | VREF0B2 | | G5 | G5 | H22 | | | HIGH |
| IO | DIFFIO_TX30n | | B2 | VREF0B2 | H17 | G6 | G6 | H21 | | | HIGH |
| IO | DIFFIO_RX29p | | B2 | VREF0B2 | | G1 | G1 | F25 | | | HIGH |
| IO | DIFFIO_RX29n | | B2 | VREF0B2 | | G2 | G2 | F26 | | | HIGH |
| IO | DIFFIO_TX29p | | B2 | VREF0B2 | | G3 | G3 | J24 | | | HIGH |
| IO | DIFFIO_TX29n | | B2 | VREF0B2 | J17 | G4 | G4 | J23 | | | HIGH |
| VREF0B2 | | | B2 | VREF0B2 | H18 | H8 | H8 | E24 | | | |
| IO | DIFFIO_RX28p | | B2 | VREF0B2 | | H1 | H1 | F27 | | | HIGH |
| IO | DIFFIO_RX28n | | B2 | VREF0B2 | | H2 | H2 | F28 | | | HIGH |
| IO | DIFFIO_TX28p | | B2 | VREF0B2 | | H3 | H3 | K23 | | | HIGH |

Table 2–1. Pin List for the Stratix EP1S20 Device (Part 2 of 39)

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin FBGA | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | | | |
| IO | DIFFIO_TX28n | | B2 | VREF0B2 | J19 | H4 | H4 | K24 | | | HIGH |
| IO | DIFFIO_RX27p | | B2 | VREF0B2 | | | | G26 | | | HIGH |
| IO | DIFFIO_RX27n | | B2 | VREF0B2 | | | | G25 | | | HIGH |
| IO | DIFFIO_TX27p | | B2 | VREF0B2 | F19 | H6 | H6 | J21 | | | HIGH |
| IO | DIFFIO_TX27n | | B2 | VREF0B2 | F20 | H5 | H5 | J22 | | | HIGH |
| IO | DIFFIO_RX26p | | B2 | VREF0B2 | D22 | J4 | J4 | G27 | | | HIGH |
| IO | DIFFIO_RX26n | | B2 | VREF0B2 | D21 | J3 | J3 | G28 | | | HIGH |
| IO | DIFFIO_TX26p | | B2 | VREF0B2 | | | | K21 | | | HIGH |
| IO | DIFFIO_TX26n | | B2 | VREF0B2 | | | | K22 | | | HIGH |
| IO | DIFFIO_RX25p/RUP2 | | B2 | VREF0B2 | E21 | K4 | K4 | H26 | | | HIGH |
| IO | DIFFIO_RX25n/RDN2 | | B2 | VREF0B2 | E22 | K3 | K3 | H25 | | | HIGH |
| IO | DIFFIO_TX25p | | B2 | VREF0B2 | | | | L22 | | | HIGH |
| IO | DIFFIO_TX25n | | B2 | VREF0B2 | | | | L21 | | | HIGH |
| IO | DIFFIO_RX24p | | B2 | VREF0B2 | | | | H27 | | | HIGH |
| IO | DIFFIO_RX24n | | B2 | VREF0B2 | | | | H28 | | | HIGH |
| IO | DIFFIO_TX24p | | B2 | VREF0B2 | | | | L23 | | | HIGH |
| IO | DIFFIO_TX24n | | B2 | VREF0B2 | | | | L24 | | | HIGH |
| IO | DIFFIO_RX23p | | B2 | VREF1B2 | | K2 | K2 | J25 | | | HIGH |
| IO | DIFFIO_RX23n | | B2 | VREF1B2 | | K1 | K1 | J26 | | | HIGH |
| IO | DIFFIO_TX23p | | B2 | VREF1B2 | G19 | K9 | K9 | L20 | | | HIGH |
| IO | DIFFIO_TX23n | | B2 | VREF1B2 | G20 | J8 | J8 | L19 | | | HIGH |
| IO | DIFFIO_RX22p | | B2 | VREF1B2 | | K6 | K6 | J27 | | | HIGH |

*Table 2–1. Pin List for the Stratix EP1S20 Device (Part 3 of 39)*

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin FBGA | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
| IO | DIFFIO_RX22n | | B2 | VREF1B2 | | K5 | K5 | J28 | | | HIGH |
| IO | DIFFIO_TX22p | | B2 | VREF1B2 | | K8 | K8 | M22 | | | HIGH |
| IO | DIFFIO_TX22n | | B2 | VREF1B2 | L17 | K7 | K7 | M21 | | | HIGH |
| IO | DIFFIO_RX21p | | B2 | VREF1B2 | | L3 | L3 | K26 | | | HIGH |
| IO | DIFFIO_RX21n | | B2 | VREF1B2 | | L2 | L2 | K25 | | | HIGH |
| IO | DIFFIO_TX21p | | B2 | VREF1B2 | | L5 | L5 | M24 | | | HIGH |
| IO | DIFFIO_TX21n | | B2 | VREF1B2 | K17 | L4 | L4 | M23 | | | HIGH |
| IO | DIFFIO_RX20p | | B2 | VREF1B2 | | | | K27 | | | HIGH |
| IO | DIFFIO_RX20n | | B2 | VREF1B2 | | | | K28 | | | HIGH |
| IO | DIFFIO_TX20p | | B2 | VREF1B2 | H19 | L7 | L7 | M20 | | | HIGH |
| IO | DIFFIO_TX20n | | B2 | VREF1B2 | H20 | L6 | L6 | M19 | | | HIGH |
| IO | DIFFIO_RX19p | | B2 | VREF1B2 | F21 | M6 | M6 | L25 | | | HIGH |
| IO | DIFFIO_RX19n | | B2 | VREF1B2 | F22 | M7 | M7 | L26 | | | HIGH |
| IO | DIFFIO_TX19p | | B2 | VREF1B2 | | | | N26 | | | HIGH |
| IO | DIFFIO_TX19n | | B2 | VREF1B2 | | | | N25 | | | HIGH |
| VREF1B2 | | | B2 | VREF1B2 | J18 | L8 | L8 | K20 | | | |
| IO | DIFFIO_RX18p | | B2 | VREF1B2 | G22 | M4 | M4 | L27 | | | HIGH |
| IO | DIFFIO_RX18n | | B2 | VREF1B2 | G21 | M5 | M5 | L28 | | | HIGH |
| IO | DIFFIO_TX18p | | B2 | VREF1B2 | | | | N24 | | | HIGH |
| IO | DIFFIO_TX18n | | B2 | VREF1B2 | | | | N23 | | | HIGH |
| IO | DIFFIO_RX17p | | B2 | VREF1B2 | H21 | N6 | N6 | M25 | | | HIGH |
| IO | DIFFIO_RX17n | | B2 | VREF1B2 | H22 | N7 | N7 | M26 | | | HIGH |

*Table 2–1. Pin List for the Stratix EP1S20 Device (Part 4 of 39)*

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin FBGA | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
| IO | DIFFIO_TX17p | | B2 | VREF1B2 | J20 | M8 | M8 | N22 | | | HIGH |
| IO | DIFFIO_TX17n | | B2 | VREF1B2 | J21 | M9 | M9 | N21 | | | HIGH |
| IO | DIFFIO_RX16p | | B2 | VREF1B2 | | | | M27 | | | HIGH |
| IO | DIFFIO_RX16n | | B2 | VREF1B2 | | | | N28 | | | HIGH |
| IO | DIFFIO_TX16p | | B2 | VREF1B2 | K20 | P8 | P8 | N20 | | | HIGH |
| IO | DIFFIO_TX16n | | B2 | VREF1B2 | K21 | N8 | N8 | N19 | | | HIGH |
| CLK0n | | | B2 | VREF1B2 | L22 | N2 | N2 | N27 | | | |
| CLK0p | | | B2 | VREF1B2 | L21 | N3 | N3 | P27 | | | |
| IO | CLK1n | | B2 | VREF1B2 | | | | P26 | | | |
| CLK1p | | | B2 | VREF1B2 | L20 | M1 | M1 | P25 | | | |
| VCCINT | | | | | VCC | | | VCC | | | |
| VCCA_PLL1 | | | | | K19 | M3 | M3 | P23 | | | |
| GND | | | | | GND | | | GND | | | |
| GNDA_PLL1 | | | | | L19 | N5 | N5 | P24 | | | |
| VCCG_PLL1 | | | | | K18 | M2 | M2 | P21 | | | |
| GNDG_PLL1 | | | | | L18 | N4 | N4 | P22 | | | |
| VCCINT | | | | | | | | | | | |
| VCCA_PLL2 | | | | | M18 | P5 | P5 | R23 | | | |
| GND | | | | | | | | | | | |
| GNDA_PLL2 | | | | | M19 | P3 | P3 | R24 | | | |
| VCCG_PLL2 | | | | | N18 | P4 | P4 | R21 | | | |
| GNDG_PLL2 | | | | | N19 | P2 | P2 | R22 | | | |

*Table 2–1. Pin List for the Stratix EP1S20 Device (Part 5 of 39)*

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin FBGA | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
| CLK2p | | | B1 | VREF0B1 | M21 | R1 | R1 | R27 | | | |
| CLK2n | | | B1 | VREF0B1 | M22 | R2 | R2 | T27 | | | |
| CLK3p | | | B1 | VREF0B1 | M20 | R3 | R3 | R25 | | | |
| IO | CLK3n | | B1 | VREF0B1 | | | | R26 | | | |
| IO | DIFFIO_RX15p | | B1 | VREF0B1 | | | | T28 | | | HIGH |
| IO | DIFFIO_RX15n | | B1 | VREF0B1 | | | | U27 | | | HIGH |
| IO | DIFFIO_TX15p | | B1 | VREF0B1 | N21 | P6 | P6 | T21 | | | HIGH |
| IO | DIFFIO_TX15n | | B1 | VREF0B1 | N20 | P7 | P7 | T22 | | | HIGH |
| IO | DIFFIO_RX14p | | B1 | VREF0B1 | R22 | R6 | R6 | U26 | | | HIGH |
| IO | DIFFIO_RX14n | | B1 | VREF0B1 | R21 | R7 | R7 | U25 | | | HIGH |
| IO | DIFFIO_TX14p | | B1 | VREF0B1 | P21 | R8 | R8 | T19 | | | HIGH |
| IO | DIFFIO_TX14n | | B1 | VREF0B1 | P20 | R9 | R9 | T20 | | | HIGH |
| IO | DIFFIO_RX13p | | B1 | VREF0B1 | T22 | R4 | R4 | V27 | | | HIGH |
| IO | DIFFIO_RX13n | | B1 | VREF0B1 | T21 | R5 | R5 | V28 | | | HIGH |
| IO | DIFFIO_TX13p | | B1 | VREF0B1 | | | | T23 | | | HIGH |
| IO | DIFFIO_TX13n | | B1 | VREF0B1 | | | | T24 | | | HIGH |
| IO | DIFFIO_RX12p | | B1 | VREF0B1 | U21 | T3 | T3 | V26 | | | HIGH |
| IO | DIFFIO_RX12n | | B1 | VREF0B1 | U22 | T2 | T2 | V25 | | | HIGH |
| IO | DIFFIO_TX12p | | B1 | VREF0B1 | | | | T26 | | | HIGH |
| IO | DIFFIO_TX12n | | B1 | VREF0B1 | | | | T25 | | | HIGH |
| VREF0B1 | | | B1 | VREF0B1 | P18 | T8 | T8 | R19 | | | |
| IO | DIFFIO_RX11p | | B1 | VREF0B1 | | | | W28 | | | HIGH |

*Table 2–1. Pin List for the Stratix EP1S20 Device (Part 6 of 39)*

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin FBGA | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | | | |
| IO | DIFFIO_RX11n | | B1 | VREF0B1 | | | | W27 | | | HIGH |
| IO | DIFFIO_TX11p | | B1 | VREF0B1 | R20 | T7 | T7 | U19 | | | HIGH |
| IO | DIFFIO_TX11n | | B1 | VREF0B1 | R19 | T6 | T6 | U20 | | | HIGH |
| IO | DIFFIO_RX10p | | B1 | VREF0B1 | V22 | T5 | T5 | W26 | | | HIGH |
| IO | DIFFIO_RX10n | | B1 | VREF0B1 | V21 | T4 | T4 | W25 | | | HIGH |
| IO | DIFFIO_TX10p | | B1 | VREF0B1 | T20 | U6 | U6 | U24 | | | HIGH |
| IO | DIFFIO_TX10n | | B1 | VREF0B1 | T19 | U5 | U5 | U23 | | | HIGH |
| IO | DIFFIO_RX9p | | B1 | VREF0B1 | | U2 | U2 | Y28 | | | HIGH |
| IO | DIFFIO_RX9n | | B1 | VREF0B1 | | U1 | U1 | Y27 | | | HIGH |
| IO | DIFFIO_TX9p | | B1 | VREF0B1 | | U8 | U8 | U21 | | | HIGH |
| IO | DIFFIO_TX9n | | B1 | VREF0B1 | N17 | U7 | U7 | U22 | | | HIGH |
| IO | DIFFIO_RX8p | | B1 | VREF0B1 | | U4 | U4 | Y26 | | | HIGH |
| IO | DIFFIO_RX8n | | B1 | VREF0B1 | | U3 | U3 | Y25 | | | HIGH |
| IO | DIFFIO_TX8p | | B1 | VREF0B1 | | U9 | U9 | V19 | | | HIGH |
| IO | DIFFIO_TX8n | | B1 | VREF0B1 | M17 | V8 | V8 | V20 | | | HIGH |
| IO | DIFFIO_RX7p | | B1 | VREF1B1 | | | | AA28 | | | HIGH |
| IO | DIFFIO_RX7n | | B1 | VREF1B1 | | | | AA27 | | | HIGH |
| IO | DIFFIO_TX7p | | B1 | VREF1B1 | | | | V24 | | | HIGH |
| IO | DIFFIO_TX7n | | B1 | VREF1B1 | | | | V23 | | | HIGH |
| IO | DIFFIO_RX6p/RUP1 | | B1 | VREF1B1 | W21 | V6 | V6 | AA25 | | | HIGH |
| IO | DIFFIO_RX6n/RDN1 | | B1 | VREF1B1 | W22 | V5 | V5 | AA26 | | | HIGH |
| IO | DIFFIO_TX6p | | B1 | VREF1B1 | | | | V22 | | | HIGH |

*Table 2–1. Pin List for the Stratix EP1S20 Device (Part 7 of 39)*

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin FBGA | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
| IO | DIFFIO_TX6n | | B1 | VREF1B1 | | | | V21 | | | HIGH |
| IO | DIFFIO_RX5p | | B1 | VREF1B1 | | | | AB28 | | | HIGH |
| IO | DIFFIO_RX5n | | B1 | VREF1B1 | | | | AB27 | | | HIGH |
| IO | DIFFIO_TX5p | | B1 | VREF1B1 | U20 | Y3 | Y3 | W23 | | | HIGH |
| IO | DIFFIO_TX5n | | B1 | VREF1B1 | U19 | Y4 | Y4 | W24 | | | HIGH |
| IO | DIFFIO_RX4p | | B1 | VREF1B1 | | W3 | W3 | AB26 | | | HIGH |
| IO | DIFFIO_RX4n | | B1 | VREF1B1 | | W4 | W4 | AB25 | | | HIGH |
| IO | DIFFIO_TX4p | | B1 | VREF1B1 | | Y6 | Y6 | W21 | | | HIGH |
| IO | DIFFIO_TX4n | | B1 | VREF1B1 | P17 | Y5 | Y5 | W22 | | | HIGH |
| VREF1B1 | | | B1 | VREF1B1 | R17 | V7 | V7 | W20 | | | |
| IO | DIFFIO_RX3p | | B1 | VREF1B1 | | Y2 | Y2 | AC28 | | | HIGH |
| IO | DIFFIO_RX3n | | B1 | VREF1B1 | | Y1 | Y1 | AC27 | | | HIGH |
| IO | DIFFIO_TX3p | | B1 | VREF1B1 | | AA6 | AA6 | Y21 | | | HIGH |
| IO | DIFFIO_TX3n | | B1 | VREF1B1 | P19 | AA5 | AA5 | Y22 | | | HIGH |
| IO | DIFFIO_RX2p | | B1 | VREF1B1 | | AA2 | AA2 | AD28 | | | HIGH |
| IO | DIFFIO_RX2n | | B1 | VREF1B1 | | AA1 | AA1 | AD27 | | | HIGH |
| IO | DIFFIO_TX2p | | B1 | VREF1B1 | | AA4 | AA4 | Y24 | | | HIGH |
| IO | DIFFIO_TX2n | | B1 | VREF1B1 | T18 | AA3 | AA3 | Y23 | | | HIGH |
| IO | DIFFIO_RX1p | | B1 | VREF1B1 | | AB2 | AB2 | AE28 | | | HIGH |
| IO | DIFFIO_RX1n | | B1 | VREF1B1 | | AB1 | AB1 | AE27 | | | HIGH |
| IO | DIFFIO_TX1p | | B1 | VREF1B1 | | AB4 | AB4 | AA23 | | | HIGH |
| IO | DIFFIO_TX1n | | B1 | VREF1B1 | U18 | AB3 | AB3 | AA24 | | | HIGH |

*Table 2–1. Pin List for the Stratix EP1S20 Device (Part 8 of 39)*

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin FBGA | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
| IO | DIFFIO_RX0p | | B1 | VREF1B1 | | AC2 | AC2 | AF28 | | | HIGH |
| IO | DIFFIO_RX0n | | B1 | VREF1B1 | | AD1 | AD1 | AF27 | | | HIGH |
| IO | DIFFIO_TX0p | | B1 | VREF1B1 | V19 | AC4 | AC4 | AA21 | | | HIGH |
| IO | DIFFIO_TX0n | | B1 | VREF1B1 | V20 | AC3 | AC3 | AA22 | | | HIGH |
| IO | | | B8 | VREF0B8 | | | | AC23 | | | |
| IO | DQ9B7 | | B8 | VREF0B8 | W20 | AD5 | AD5 | AG26 | DQ3B15 | DQ1B31 | |
| IO | | | B8 | VREF0B8 | N16 | AB6 | AB6 | AB22 | | | |
| IO | DQ9B6 | | B8 | VREF0B8 | W19 | AD2 | AD2 | AH26 | DQ3B14 | DQ1B30 | |
| IO | DQ9B5 | | B8 | VREF0B8 | AA21 | AE2 | AE2 | AG25 | DQ3B13 | DQ1B29 | |
| IO | DQ9B4 | | B8 | VREF0B8 | AA20 | AD3 | AD3 | AH25 | DQ3B12 | DQ1B28 | |
| IO | | | B8 | VREF0B8 | | | | AE25 | | | |
| IO | DQ9B3 | | B8 | VREF0B8 | Y21 | AE4 | AE4 | AF25 | DQ3B11 | DQ1B27 | |
| IO | DQS9B | | B8 | VREF0B8 | Y20 | AD4 | AD4 | AF24 | | | |
| IO | DQ9B2 | | B8 | VREF0B8 | Y19 | AE3 | AE3 | AG24 | DQ3B10 | DQ1B26 | |
| IO | DQ9B1 | | B8 | VREF0B8 | AA19 | AB5 | AB5 | AE24 | DQ3B9 | DQ1B25 | |
| IO | DQ9B0 | | B8 | VREF0B8 | AB19 | AF3 | AF3 | AH24 | DQ3B8 | DQ1B24 | |
| VREF0B8 | | | B8 | VREF0B8 | R18 | AE5 | AE5 | AD22 | | | |
| IO | | | B8 | VREF0B8 | | | | AD24 | | | |
| IO | | | B8 | VREF0B8 | | | | AB21 | | | |
| IO | DQ8B7 | | B8 | VREF0B8 | W18 | AC7 | AC7 | AG23 | DQ3B7 | DQ1B23 | |
| IO | DQ8B6 | | B8 | VREF0B8 | AA18 | AD6 | AD6 | AD23 | DQ3B6 | DQ1B22 | |
| IO | DQ8B5 | | B8 | VREF0B8 | AA17 | AE7 | AE7 | AF23 | DQ3B5 | DQ1B21 | |

**Table 2–1. Pin List for the Stratix EP1S20 Device (Part 9 of 39)**

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin FBGA | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
| IO | DQ8B4 | | B8 | VREF0B8 | AB18 | AB7 | AB7 | AH23 | DQ3B4 | DQ1B20 | |
| IO | DQ8B3 | | B8 | VREF0B8 | V18 | AD7 | AD7 | AE22 | DQ3B3 | DQ1B19 | |
| IO | DQS8B | | B8 | VREF0B8 | Y18 | AE6 | AE6 | AE23 | DQS3B | | |
| IO | DQ8B2 | | B8 | VREF0B8 | W17 | AA7 | AA7 | AF22 | DQ3B2 | DQ1B18 | |
| IO | DQ8B1 | | B8 | VREF0B8 | Y17 | AF7 | AF7 | AH22 | DQ3B1 | DQ1B17 | |
| IO | DQ8B0 | | B8 | VREF0B8 | AB17 | AF6 | AF6 | AG22 | DQ3B0 | DQ1B16 | |
| IO | | | B8 | VREF0B8 | | | | AB20 | | | |
| IO | DQ7B7 | | B8 | VREF1B8 | U17 | AC8 | AC8 | AD21 | DQ2B15 | DQ1B15 | |
| IO | DQ7B6 | | B8 | VREF1B8 | U16 | AB8 | AB8 | AE21 | DQ2B14 | DQ1B14 | |
| IO | DQ7B5 | | B8 | VREF1B8 | V17 | AD8 | AD8 | AG21 | DQ2B13 | DQ1B13 | |
| IO | DQ7B4 | | B8 | VREF1B8 | V16 | AE8 | AE8 | AF21 | DQ2B12 | DQ1B12 | |
| IO | DQ7B3 | | B8 | VREF1B8 | Y16 | AF8 | AF8 | AE20 | DQ2B11 | DQ1B11 | |
| IO | DQS7B | | B8 | VREF1B8 | AA16 | Y9 | Y9 | AG20 | | DQS1B | |
| IO | DQ7B2 | | B8 | VREF1B8 | T16 | Y8 | Y8 | AF20 | DQ2B10 | DQ1B10 | |
| IO | DQ6B7 | | B8 | VREF1B8 | Y15 | AC9 | AC9 | AE19 | DQ2B7 | DQ1B7 | |
| IO | DQ7B1 | | B8 | VREF1B8 | W16 | W9 | W9 | AH21 | DQ2B9 | DQ1B9 | |
| IO | DQ6B6 | | B8 | VREF1B8 | AA15 | AF9 | AF9 | AD19 | DQ2B6 | DQ1B6 | |
| IO | DQ7B0 | | B8 | VREF1B8 | AB16 | AA8 | AA8 | AH20 | DQ2B8 | DQ1B8 | |
| IO | DQ6B5 | | B8 | VREF1B8 | AB15 | AD10 | AD10 | AF19 | DQ2B5 | DQ1B5 | |
| VREF1B8 | | | B8 | VREF1B8 | R16 | AE9 | AE9 | AD20 | | | |
| IO | DQ6B4 | | B8 | VREF1B8 | V15 | AE10 | AE10 | AG19 | DQ2B4 | DQ1B4 | |
| IO | DQ6B3 | | B8 | VREF1B8 | U15 | AC10 | AC10 | AH19 | DQ2B3 | DQ1B3 | |

*Table 2–1. Pin List for the Stratix EP1S20 Device (Part 10 of 39)*

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin FBGA | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | | | |
| IO | DQS6B | | B8 | VREF1B8 | W15 | Y10 | Y10 | AF18 | DQS2B | | |
| IO | | PGM2 | B8 | VREF1B8 | R15 | AA9 | AA9 | AB19 | | | |
| IO | FCLK3 | | B8 | VREF1B8 | P16 | AD9 | AD9 | AC21 | | | |
| IO | FCLK2 | | B8 | VREF1B8 | T15 | AB9 | AB9 | AC19 | | | |
| IO | DQ6B2 | | B8 | VREF1B8 | U14 | AA10 | AA10 | AD18 | DQ2B2 | DQ1B2 | |
| IO | | | B8 | VREF1B8 | N14 | W10 | W10 | AA20 | | | |
| IO | DQ6B1 | | B8 | VREF1B8 | W14 | AB10 | AB10 | AE18 | DQ2B1 | DQ1B1 | |
| IO | DQ6B0 | | B8 | VREF1B8 | V14 | AF10 | AF10 | AG18 | DQ2B0 | DQ1B0 | |
| IO | RDN8 | | B8 | VREF1B8 | P15 | AB11 | AB11 | Y19 | | | |
| IO | RUP8 | | B8 | VREF1B8 | N15 | AE11 | AE11 | W19 | | | |
| IO | DQ5B7 | | B8 | VREF1B8 | | | | AF17 | | | |
| IO | DQ5B6 | | B8 | VREF1B8 | | | | AG17 | | | |
| IO | DQ5B5 | | B8 | VREF1B8 | | | | AE17 | | | |
| IO | DQ5B4 | | B8 | VREF1B8 | | | | AD17 | | | |
| IO | | RDYnBSY | B8 | VREF1B8 | P14 | AC11 | AC11 | AA19 | | | |
| IO | DQ5B3 | | B8 | VREF1B8 | | | | AG16 | | | |
| IO | DQS5B | | B8 | VREF2B8 | | | | AH16 | | | |
| IO | DQ5B2 | | B8 | VREF2B8 | | | | AD16 | | | |
| IO | | nCS | B8 | VREF2B8 | T14 | Y11 | Y11 | Y18 | | | |
| IO | DQ5B1 | | B8 | VREF2B8 | | | | AF16 | | | |
| IO | DQ5B0 | | B8 | VREF2B8 | | | | AE16 | | | |
| IO | | | B8 | VREF2B8 | | | | Y20 | | | |

*Table 2–1. Pin List for the Stratix EP1S20 Device (Part 11 of 39)*

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **484-Pin FBGA** | **672-Pin BGA** | **672-Pin FBGA** | **780-Pin FBGA** | **DQS for x16** | **DQS for x32** | **DIFFIO Speed (1)** |
| IO | | | B8 | VREF2B8 | | | | AC22 | | | |
| IO | | | B8 | VREF2B8 | | | | AC20 | | | |
| IO | | | B8 | VREF2B8 | N13 | AD11 | AD11 | AB18 | | | |
| IO | | CS | B8 | VREF2B8 | P13 | AA11 | AA11 | AA18 | | | |
| IO | | | B8 | VREF2B8 | | | | V18 | | | |
| IO | | | B8 | VREF2B8 | | | | W18 | | | |
| VREF2B8 | | | B8 | VREF2B8 | R14 | W11 | W11 | AH18 | | | |
| IO | CLK5n | | B8 | VREF2B8 | W13 | AD12 | AD12 | Y17 | | | |
| CLK5p | | | B8 | VREF2B8 | V13 | AC12 | AC12 | AA17 | | | |
| IO | CLK4n | | B8 | VREF2B8 | Y14 | AF12 | AF12 | AB17 | | | |
| CLK4p | | | B8 | VREF2B8 | AA14 | AE12 | AE12 | AC17 | | | |
| PLL_ENA | | PLL_ENA | B8 | VREF2B8 | R13 | W12 | W12 | AC18 | | | |
| MSEL0 | | MSEL0 | B8 | VREF2B8 | T13 | Y12 | Y12 | AC16 | | | |
| MSEL1 | | MSEL1 | B8 | VREF2B8 | P12 | Y13 | Y13 | W17 | | | |
| MSEL2 | | MSEL2 | B8 | VREF2B8 | R12 | W13 | W13 | AB15 | | | |
| IO | PLL6_OUT3n | | B12 | VREF2B8 | | | | Y16 | | | |
| IO | PLL6_OUT3p | | B12 | VREF2B8 | | | | W16 | | | |
| IO | PLL6_OUT2n | | B12 | VREF2B8 | | | | AG15 | | | |
| IO | PLL6_OUT2p | | B12 | VREF2B8 | | | | AF15 | | | |
| IO | PLL6_FBn | | B11 | VREF2B8 | Y12 | AB12 | AB12 | AA15 | | | |
| IO | PLL6_FBp | | B11 | VREF2B8 | W12 | AA12 | AA12 | AA14 | | | |
| IO | PLL6_OUT1n | | B11 | VREF2B8 | AB12 | AB14 | AB14 | W15 | | | |

Table 2–1. Pin List for the Stratix EP1S20 Device (Part 12 of 39)

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin FBGA | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | | | |
| IO | PLL6_OUT1p | | B11 | VREF2B8 | AA12 | AA14 | AA14 | W14 | | | |
| IO | PLL6_OUT0n | | B11 | VREF2B8 | Y13 | AB13 | AB13 | AE15 | | | |
| IO | PLL6_OUT0p | | B11 | VREF2B8 | AA13 | AA13 | AA13 | AD15 | | | |
| VCC_PLL6_OUTB | | | B12 | | | | | AB16 | | | |
| VCC_PLL6_OUTB | | | B12 | | | | | | | | |
| VCC_PLL6_OUTA | | | B11 | | | | | AC14 | | | |
| VCC_PLL6_OUTA | | | B11 | | U13 | AE13 | AE13 | | | | |
| VCCINT | | | | | | | | | | | |
| VCCA_PLL6 | | | | | T12 | AD14 | AD14 | AG14 | | | |
| GND | | | | | | | | | | | |
| GNDA_PLL6 | | | | | U12 | AC14 | AC14 | AF14 | | | |
| GNDA_PLL6 | | | | | | | | | | | |
| VCCG_PLL6 | | | | | U11 | AD13 | AD13 | AA13 | | | |
| GNDG_PLL6 | | | | | T11 | AE14 | AE14 | AB14 | | | |
| CLK7p | | | B7 | VREF0B7 | AA11 | AE15 | AE15 | W13 | | | |
| IO | CLK7n | | B7 | VREF0B7 | | | | Y13 | | | |
| CLK6p | | | B7 | VREF0B7 | AB11 | AF15 | AF15 | AD14 | | | |
| IO | CLK6n | | B7 | VREF0B7 | | | | AE14 | | | |
| nCE | | nCE | B7 | VREF0B7 | R11 | Y14 | Y14 | AB13 | | | |
| nCEO | | nCEO | B7 | VREF0B7 | P11 | W14 | W14 | AC13 | | | |
| IO | | | B7 | VREF0B7 | | | | V11 | | | |
| IO | | | B7 | VREF0B7 | | | | Y11 | | | |

*Table 2–1. Pin List for the Stratix EP1S20 Device (Part 13 of 39)*

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin FBGA | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | | | |
| IO | | PGM0 | B7 | VREF0B7 | N10 | W15 | W15 | W12 | | | |
| nIO_PULLUP | | nIO_PULLUP | B7 | VREF0B7 | N9 | AA15 | AA15 | Y12 | | | |
| VCCSEL | | VCCSEL | B7 | VREF0B7 | R10 | Y15 | Y15 | AA12 | | | |
| PORSEL | | PORSEL | B7 | VREF0B7 | U10 | W16 | W16 | AC12 | | | |
| IO | | INIT_DONE | B7 | VREF0B7 | P10 | AC15 | AC15 | W11 | | | |
| IO | DQ4B7 | | B7 | VREF0B7 | V12 | | | AD13 | | | |
| IO | DQ4B6 | | B7 | VREF0B7 | V11 | | | AE13 | | | |
| IO | | nRS | B7 | VREF0B7 | T10 | Y16 | Y16 | AC11 | | | |
| IO | DQ4B5 | | B7 | VREF0B7 | W11 | | | AF13 | | | |
| IO | DQ4B4 | | B7 | VREF0B7 | Y11 | | | AD12 | | | |
| VREF0B7 | | | B7 | VREF0B7 | R9 | AB15 | AB15 | AD11 | | | |
| IO | DQ4B3 | | B7 | VREF0B7 | V10 | | | AG13 | | | |
| IO | | RUnLU | B7 | VREF0B7 | P9 | AD15 | AD15 | W10 | | | |
| IO | DQS4B | | B7 | VREF0B7 | W10 | | | AH13 | | | |
| IO | DQ4B2 | | B7 | VREF0B7 | AA9 | | | AE12 | | | |
| IO | DQ4B1 | | B7 | VREF0B7 | Y10 | | | AF12 | | | |
| IO | DQ4B0 | | B7 | VREF0B7 | AA10 | | | AG12 | | | |
| IO | | PGM1 | B7 | VREF0B7 | M8 | AC16 | AC16 | AA11 | | | |
| IO | RDN7 | | B7 | VREF0B7 | T9 | AB16 | AB16 | AC10 | | | |
| IO | RUP7 | | B7 | VREF0B7 | N8 | AD16 | AD16 | AB11 | | | |
| IO | DQ3B7 | | B7 | VREF0B7 | AA8 | W17 | W17 | AG11 | DQ1B15 | DQ0B31 | |
| IO | DQ3B6 | | B7 | VREF0B7 | Y9 | AE16 | AE16 | AH11 | DQ1B14 | DQ0B30 | |

**Table 2–1. Pin List for the Stratix EP1S20 Device (Part 14 of 39)**

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin FBGA | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | | | |
| IO | DQ3B5 | | B7 | VREF0B7 | Y8 | Y17 | Y17 | AE11 | DQ1B13 | DQ0B29 | |
| IO | DEV_CLRn | | B7 | VREF1B7 | P8 | AF17 | AF17 | AC9 | | | |
| IO | DQ3B4 | | B7 | VREF1B7 | U9 | AA17 | AA17 | AF11 | DQ1B12 | DQ0B28 | |
| IO | DQ3B3 | | B7 | VREF1B7 | V9 | Y18 | Y18 | AE10 | DQ1B11 | DQ0B27 | |
| IO | DQS3B | | B7 | VREF1B7 | W8 | AE17 | AE17 | AG10 | DQS1B | | |
| IO | | | B7 | VREF1B7 | | | | Y10 | | | |
| IO | DQ3B2 | | B7 | VREF1B7 | W9 | W18 | W18 | AH10 | DQ1B10 | DQ0B26 | |
| IO | DQ3B1 | | B7 | VREF1B7 | V8 | AB17 | AB17 | AF10 | DQ1B9 | DQ0B25 | |
| IO | DQ3B0 | | B7 | VREF1B7 | U8 | AA18 | AA18 | AD10 | DQ1B8 | DQ0B24 | |
| IO | | | B7 | VREF1B7 | R8 | AF20 | AF20 | AA10 | | | |
| IO | | | B7 | VREF1B7 | | | | AB9 | | | |
| IO | FCLK5 | | B7 | VREF1B7 | T8 | AC17 | AC17 | AC8 | | | |
| IO | FCLK4 | | B7 | VREF1B7 | M7 | AD17 | AD17 | AB10 | | | |
| VREF1B7 | | | B7 | VREF1B7 | R7 | AB18 | AB18 | AD9 | | | |
| IO | DQ2B7 | | B7 | VREF1B7 | W7 | AF18 | AF18 | AG9 | DQ1B7 | DQ0B23 | |
| IO | DQ2B6 | | B7 | VREF1B7 | U6 | AE18 | AE18 | AF9 | DQ1B6 | DQ0B22 | |
| IO | DQ2B5 | | B7 | VREF1B7 | AB8 | AF19 | AF19 | AE9 | DQ1B5 | DQ0B21 | |
| IO | DQ2B4 | | B7 | VREF1B7 | V6 | Y20 | Y20 | AH8 | DQ1B4 | DQ0B20 | |
| IO | DQ2B3 | | B7 | VREF1B7 | AB7 | AA19 | AA19 | AH9 | DQ1B3 | DQ0B19 | |
| IO | DQS2B | | B7 | VREF1B7 | AA7 | AB19 | AB19 | AE8 | | DQS0B | |
| IO | DQ2B2 | | B7 | VREF1B7 | U7 | AD19 | AD19 | AD8 | DQ1B2 | DQ0B18 | |
| IO | | | B7 | VREF1B7 | | | | AA9 | | | |

*Table 2–1. Pin List for the Stratix EP1S20 Device (Part 15 of 39)*

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin FBGA | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
| IO | DQ2B1 | | B7 | VREF1B7 | V7 | AC19 | AC19 | AF8 | DQ1B1 | DQ0B17 | |
| IO | | | B7 | VREF1B7 | | | | AB8 | | | |
| IO | DQ2B0 | | B7 | VREF1B7 | Y7 | AE19 | AE19 | AG8 | DQ1B0 | DQ0B16 | |
| IO | | | B7 | VREF1B7 | | | | AC7 | | | |
| IO | DQ1B7 | | B7 | VREF2B7 | Y6 | AE20 | AE20 | AF6 | DQ0B15 | DQ0B15 | |
| IO | DQ1B6 | | B7 | VREF2B7 | V5 | AA20 | AA20 | AG7 | DQ0B14 | DQ0B14 | |
| IO | DQ1B5 | | B7 | VREF2B7 | AA6 | AB20 | AB20 | AH7 | DQ0B13 | DQ0B13 | |
| IO | DQ1B4 | | B7 | VREF2B7 | W6 | AF21 | AF21 | AF7 | DQ0B12 | DQ0B12 | |
| IO | DQ1B3 | | B7 | VREF2B7 | AB6 | AC20 | AC20 | AD6 | DQ0B11 | DQ0B11 | |
| IO | DQS1B | | B7 | VREF2B7 | AB5 | AA21 | AA21 | AE7 | DQS0B | | |
| IO | DQ1B2 | | B7 | VREF2B7 | W5 | AE21 | AE21 | AH6 | DQ0B10 | DQ0B10 | |
| IO | | | B7 | VREF2B7 | | | | AD5 | | | |
| IO | DQ1B1 | | B7 | VREF2B7 | Y5 | AD20 | AD20 | AG6 | DQ0B9 | DQ0B9 | |
| IO | DQ0B7 | | B7 | VREF2B7 | AA4 | AE25 | AE25 | AF5 | DQ0B7 | DQ0B7 | |
| IO | DQ1B0 | | B7 | VREF2B7 | AA5 | AC21 | AC21 | AE6 | DQ0B8 | DQ0B8 | |
| IO | DQ0B6 | | B7 | VREF2B7 | AB4 | AF22 | AF22 | AH5 | DQ0B6 | DQ0B6 | |
| VREF2B7 | | | B7 | VREF2B7 | R5 | AD21 | AD21 | AD7 | | | |
| IO | | | B7 | VREF2B7 | | | | Y9 | | | |
| IO | DQ0B5 | | B7 | VREF2B7 | Y2 | AF24 | AF24 | AF4 | DQ0B5 | DQ0B5 | |
| IO | DQ0B4 | | B7 | VREF2B7 | Y4 | AE22 | AE22 | AG4 | DQ0B4 | DQ0B4 | |
| IO | | | B7 | VREF2B7 | T7 | Y19 | Y19 | AE4 | | | |
| IO | DQ0B3 | | B7 | VREF2B7 | AA3 | AB22 | AB22 | AG5 | DQ0B3 | DQ0B3 | |

*Table 2–1. Pin List for the Stratix EP1S20 Device (Part 16 of 39)*

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin FBGA | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
| IO | DQS0B | | B7 | VREF2B7 | AA2 | AE23 | AE23 | AH3 | | | |
| IO | | | B7 | VREF2B7 | P7 | AD22 | AD22 | AB12 | | | |
| IO | DQ0B2 | | B7 | VREF2B7 | W3 | AC23 | AC23 | AG3 | DQ0B2 | DQ0B2 | |
| IO | DQ0B1 | | B7 | VREF2B7 | W4 | AC22 | AC22 | AE5 | DQ0B1 | DQ0B1 | |
| IO | | | B7 | VREF2B7 | N7 | AB21 | AB21 | AC5 | | | |
| IO | DQ0B0 | | B7 | VREF2B7 | Y3 | AE24 | AE24 | AH4 | DQ0B0 | DQ0B0 | |
| IO | | | B7 | VREF2B7 | | | | AB7 | | | |
| IO | DIFFIO_TX65n | | B6 | VREF0B6 | V4 | AD25 | AD25 | AA7 | | | HIGH |
| IO | DIFFIO_TX65p | | B6 | VREF0B6 | V3 | AC24 | AC24 | AA8 | | | HIGH |
| IO | DIFFIO_RX65n | | B6 | VREF0B6 | | AD26 | AD26 | AF2 | | | HIGH |
| IO | DIFFIO_RX65p | | B6 | VREF0B6 | | AC25 | AC25 | AF1 | | | HIGH |
| IO | DIFFIO_TX64n | | B6 | VREF0B6 | U5 | AB24 | AB24 | AA5 | | | HIGH |
| IO | DIFFIO_TX64p | | B6 | VREF0B6 | | AB23 | AB23 | AA6 | | | HIGH |
| IO | DIFFIO_RX64n | | B6 | VREF0B6 | | AB26 | AB26 | AE2 | | | HIGH |
| IO | DIFFIO_RX64p | | B6 | VREF0B6 | | AB25 | AB25 | AE1 | | | HIGH |
| IO | DIFFIO_TX63n | | B6 | VREF0B6 | T5 | AA24 | AA24 | Y6 | | | HIGH |
| IO | DIFFIO_TX63p | | B6 | VREF0B6 | | AA23 | AA23 | Y5 | | | HIGH |
| IO | DIFFIO_RX63n | | B6 | VREF0B6 | | AA26 | AA26 | AD2 | | | HIGH |
| IO | DIFFIO_RX63p | | B6 | VREF0B6 | | AA25 | AA25 | AD1 | | | HIGH |
| IO | DIFFIO_TX62n | | B6 | VREF0B6 | P4 | AA22 | AA22 | Y7 | | | HIGH |
| IO | DIFFIO_TX62p | | B6 | VREF0B6 | | Y22 | Y22 | Y8 | | | HIGH |
| IO | DIFFIO_RX62n | | B6 | VREF0B6 | | Y26 | Y26 | AC2 | | | HIGH |

*Table 2–1. Pin List for the Stratix EP1S20 Device (Part 17 of 39)*

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin FBGA | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
| IO | DIFFIO_RX62p | | B6 | VREF0B6 | | Y25 | Y25 | AC1 | | | HIGH |
| VREF0B6 | | | B6 | VREF0B6 | R6 | Y21 | Y21 | AE3 | | | |
| IO | DIFFIO_TX61n | | B6 | VREF0B6 | U4 | Y24 | Y24 | W7 | | | HIGH |
| IO | DIFFIO_TX61p | | B6 | VREF0B6 | U3 | Y23 | Y23 | W8 | | | HIGH |
| IO | DIFFIO_RX61n | | B6 | VREF0B6 | | W23 | W23 | AB4 | | | HIGH |
| IO | DIFFIO_RX61p | | B6 | VREF0B6 | | W24 | W24 | AB3 | | | HIGH |
| IO | DIFFIO_TX60n | | B6 | VREF0B6 | P6 | W21 | W21 | W5 | | | HIGH |
| IO | DIFFIO_TX60p | | B6 | VREF0B6 | | W22 | W22 | W6 | | | HIGH |
| IO | DIFFIO_RX60n | | B6 | VREF0B6 | | | | AB2 | | | HIGH |
| IO | DIFFIO_RX60p | | B6 | VREF0B6 | | | | AB1 | | | HIGH |
| IO | DIFFIO_TX59n | | B6 | VREF0B6 | | | | V8 | | | HIGH |
| IO | DIFFIO_TX59p | | B6 | VREF0B6 | | | | V7 | | | HIGH |
| IO | DIFFIO_RX59n/RDN6 | | B6 | VREF0B6 | W1 | U24 | U24 | AA3 | | | HIGH |
| IO | DIFFIO_RX59p/RUP6 | | B6 | VREF0B6 | W2 | U23 | U23 | AA4 | | | HIGH |
| IO | DIFFIO_TX58n | | B6 | VREF0B6 | | | | V6 | | | HIGH |
| IO | DIFFIO_TX58p | | B6 | VREF0B6 | | | | V5 | | | HIGH |
| IO | DIFFIO_RX58n | | B6 | VREF0B6 | | | | AA2 | | | HIGH |
| IO | DIFFIO_RX58p | | B6 | VREF0B6 | | | | AA1 | | | HIGH |
| IO | DIFFIO_TX57n | | B6 | VREF1B6 | T4 | V19 | V19 | V9 | | | HIGH |
| IO | DIFFIO_TX57p | | B6 | VREF1B6 | T3 | U20 | U20 | V10 | | | HIGH |
| IO | DIFFIO_RX57n | | B6 | VREF1B6 | | U26 | U26 | Y4 | | | HIGH |
| IO | DIFFIO_RX57p | | B6 | VREF1B6 | | U25 | U25 | Y3 | | | HIGH |

*Table 2–1. Pin List for the Stratix EP1S20 Device (Part 18 of 39)*

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin FBGA | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
| IO | DIFFIO_TX56n | | B6 | VREF1B6 | N6 | U19 | U19 | U7 | | | HIGH |
| IO | DIFFIO_TX56p | | B6 | VREF1B6 | | U18 | U18 | U8 | | | HIGH |
| IO | DIFFIO_RX56n | | B6 | VREF1B6 | V2 | U22 | U22 | Y2 | | | HIGH |
| IO | DIFFIO_RX56p | | B6 | VREF1B6 | V1 | U21 | U21 | Y1 | | | HIGH |
| IO | DIFFIO_TX55n | | B6 | VREF1B6 | M6 | T21 | T21 | U6 | | | HIGH |
| IO | DIFFIO_TX55p | | B6 | VREF1B6 | | T20 | T20 | U5 | | | HIGH |
| IO | DIFFIO_RX55n | | B6 | VREF1B6 | | T25 | T25 | W4 | | | HIGH |
| IO | DIFFIO_RX55p | | B6 | VREF1B6 | | T24 | T24 | W3 | | | HIGH |
| IO | DIFFIO_TX54n | | B6 | VREF1B6 | R3 | T19 | T19 | U9 | | | HIGH |
| IO | DIFFIO_TX54p | | B6 | VREF1B6 | R4 | R19 | R19 | U10 | | | HIGH |
| IO | DIFFIO_RX54n | | B6 | VREF1B6 | | | | W2 | | | HIGH |
| IO | DIFFIO_RX54p | | B6 | VREF1B6 | | | | W1 | | | HIGH |
| VREF1B6 | | | B6 | VREF1B6 | P5 | V20 | V20 | W9 | | | |
| IO | DIFFIO_TX53n | | B6 | VREF1B6 | | | | T6 | | | HIGH |
| IO | DIFFIO_TX53p | | B6 | VREF1B6 | | | | T5 | | | HIGH |
| IO | DIFFIO_RX53n | | B6 | VREF1B6 | U1 | T23 | T23 | V4 | | | HIGH |
| IO | DIFFIO_RX53p | | B6 | VREF1B6 | U2 | T22 | T22 | V3 | | | HIGH |
| IO | DIFFIO_TX52n | | B6 | VREF1B6 | | | | T10 | | | HIGH |
| IO | DIFFIO_TX52p | | B6 | VREF1B6 | | | | T9 | | | HIGH |
| IO | DIFFIO_RX52n | | B6 | VREF1B6 | T2 | R22 | R22 | V1 | | | HIGH |
| IO | DIFFIO_RX52p | | B6 | VREF1B6 | T1 | R23 | R23 | V2 | | | HIGH |
| IO | DIFFIO_TX51n | | B6 | VREF1B6 | P3 | P20 | P20 | T7 | | | HIGH |

Table 2–1. Pin List for the Stratix EP1S20 Device (Part 19 of 39)

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin FBGA | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | | | |
| IO | DIFFIO_TX51p | | B6 | VREF1B6 | P2 | P21 | P21 | T8 | | | HIGH |
| IO | DIFFIO_RX51n | | B6 | VREF1B6 | R2 | R20 | R20 | U4 | | | HIGH |
| IO | DIFFIO_RX51p | | B6 | VREF1B6 | R1 | R21 | R21 | U3 | | | HIGH |
| IO | DIFFIO_TX50n | | B6 | VREF1B6 | N3 | P19 | P19 | T4 | | | HIGH |
| IO | DIFFIO_TX50p | | B6 | VREF1B6 | N2 | N19 | N19 | T3 | | | HIGH |
| IO | DIFFIO_RX50n | | B6 | VREF1B6 | | | | U2 | | | HIGH |
| IO | DIFFIO_RX50p | | B6 | VREF1B6 | | | | T1 | | | HIGH |
| IO | CLK8n | | B6 | VREF1B6 | | | | R3 | | | |
| CLK8p | | | B6 | VREF1B6 | M3 | P24 | P24 | R4 | | | |
| CLK9n | | | B6 | VREF1B6 | M1 | P25 | P25 | T2 | | | |
| CLK9p | | | B6 | VREF1B6 | M2 | R26 | R26 | R2 | | | |
| GNDG_PLL3 | | | | | N4 | R25 | R25 | R7 | | | |
| VCCG_PLL3 | | | | | N5 | P23 | P23 | R8 | | | |
| GNDA_PLL3 | | | | | M4 | R24 | R24 | R5 | | | |
| GND | | | | | | | | | | | |
| VCCA_PLL3 | | | | | M5 | P22 | P22 | R6 | | | |
| VCCINT | | | | | | | | | | | |
| GNDG_PLL4 | | | | | L5 | N22 | N22 | P7 | | | |
| VCCG_PLL4 | | | | | K5 | N24 | N24 | P8 | | | |
| GNDA_PLL4 | | | | | L4 | N23 | N23 | P5 | | | |
| GND | | | | | | | | | | | |
| VCCA_PLL4 | | | | | K4 | N25 | N25 | P6 | | | |

*Table 2–1. Pin List for the Stratix EP1S20 Device (Part 20 of 39)*

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin FBGA | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | | | |
| VCCINT | | | | | | | | | | | |
| CLK10p | | | B5 | VREF0B5 | L3 | M26 | M26 | P4 | | | |
| IO | CLK10n | | B5 | VREF0B5 | | | | P3 | | | |
| CLK11p | | | B5 | VREF0B5 | L2 | M24 | M24 | P2 | | | |
| CLK11n | | | B5 | VREF0B5 | L1 | M25 | M25 | N2 | | | |
| IO | DIFFIO_TX49n | | B5 | VREF0B5 | K2 | N20 | N20 | N10 | | | HIGH |
| IO | DIFFIO_TX49p | | B5 | VREF0B5 | K3 | N21 | N21 | N9 | | | HIGH |
| IO | DIFFIO_RX49n | | B5 | VREF0B5 | | | | M2 | | | HIGH |
| IO | DIFFIO_RX49p | | B5 | VREF0B5 | | | | N1 | | | HIGH |
| IO | DIFFIO_TX48n | | B5 | VREF0B5 | J2 | M18 | M18 | N5 | | | HIGH |
| IO | DIFFIO_TX48p | | B5 | VREF0B5 | J3 | M19 | M19 | N6 | | | HIGH |
| IO | DIFFIO_RX48n | | B5 | VREF0B5 | H1 | M20 | M20 | M3 | | | HIGH |
| IO | DIFFIO_RX48p | | B5 | VREF0B5 | H2 | M21 | M21 | M4 | | | HIGH |
| IO | DIFFIO_TX47n | | B5 | VREF0B5 | | | | N7 | | | HIGH |
| IO | DIFFIO_TX47p | | B5 | VREF0B5 | | | | N8 | | | HIGH |
| IO | DIFFIO_RX47n | | B5 | VREF0B5 | G2 | M22 | M22 | L1 | | | HIGH |
| IO | DIFFIO_RX47p | | B5 | VREF0B5 | G1 | M23 | M23 | L2 | | | HIGH |
| VREF0B5 | | | B5 | VREF0B5 | J5 | L19 | L19 | P10 | | | |
| IO | DIFFIO_TX46n | | B5 | VREF0B5 | | | | N4 | | | HIGH |
| IO | DIFFIO_TX46p | | B5 | VREF0B5 | | | | N3 | | | HIGH |
| IO | DIFFIO_RX46n | | B5 | VREF0B5 | F1 | L22 | L22 | L3 | | | HIGH |
| IO | DIFFIO_RX46p | | B5 | VREF0B5 | F2 | L23 | L23 | L4 | | | HIGH |

**Table 2–1. Pin List for the Stratix EP1S20 Device (Part 21 of 39)**

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin FBGA | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | | | |
| IO | DIFFIO_TX45n | | B5 | VREF0B5 | H3 | L21 | L21 | M10 | | | HIGH |
| IO | DIFFIO_TX45p | | B5 | VREF0B5 | H4 | L20 | L20 | M9 | | | HIGH |
| IO | DIFFIO_RX45n | | B5 | VREF0B5 | | | | K1 | | | HIGH |
| IO | DIFFIO_RX45p | | B5 | VREF0B5 | | | | K2 | | | HIGH |
| IO | DIFFIO_TX44n | | B5 | VREF0B5 | K6 | K20 | K20 | M6 | | | HIGH |
| IO | DIFFIO_TX44p | | B5 | VREF0B5 | | K19 | K19 | M5 | | | HIGH |
| IO | DIFFIO_RX44n | | B5 | VREF0B5 | | L25 | L25 | K4 | | | HIGH |
| IO | DIFFIO_RX44p | | B5 | VREF0B5 | | L24 | L24 | K3 | | | HIGH |
| IO | DIFFIO_TX43n | | B5 | VREF0B5 | L6 | K22 | K22 | M8 | | | HIGH |
| IO | DIFFIO_TX43p | | B5 | VREF0B5 | | K21 | K21 | M7 | | | HIGH |
| IO | DIFFIO_RX43n | | B5 | VREF0B5 | | K24 | K24 | J1 | | | HIGH |
| IO | DIFFIO_RX43p | | B5 | VREF0B5 | | K23 | K23 | J2 | | | HIGH |
| IO | DIFFIO_TX42n | | B5 | VREF0B5 | G3 | J20 | J20 | L10 | | | HIGH |
| IO | DIFFIO_TX42p | | B5 | VREF0B5 | G4 | J19 | J19 | L9 | | | HIGH |
| IO | DIFFIO_RX42n | | B5 | VREF0B5 | | K26 | K26 | J3 | | | HIGH |
| IO | DIFFIO_RX42p | | B5 | VREF0B5 | | K25 | K25 | J4 | | | HIGH |
| IO | DIFFIO_TX41n | | B5 | VREF1B5 | | | | L5 | | | HIGH |
| IO | DIFFIO_TX41p | | B5 | VREF1B5 | | | | L6 | | | HIGH |
| IO | DIFFIO_RX41n | | B5 | VREF1B5 | | | | H1 | | | HIGH |
| IO | DIFFIO_RX41p | | B5 | VREF1B5 | | | | H2 | | | HIGH |
| IO | DIFFIO_TX40n | | B5 | VREF1B5 | | | | L8 | | | HIGH |
| IO | DIFFIO_TX40p | | B5 | VREF1B5 | | | | L7 | | | HIGH |

*Table 2–1. Pin List for the Stratix EP1S20 Device (Part 22 of 39)*

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin FBGA | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | | | |
| IO | DIFFIO_RX40n/RDN5 | | B5 | VREF1B5 | E1 | J22 | J22 | H3 | | | HIGH |
| IO | DIFFIO_RX40p/RUP5 | | B5 | VREF1B5 | E2 | J21 | J21 | H4 | | | HIGH |
| IO | DIFFIO_TX39n | | B5 | VREF1B5 | | | | K7 | | | HIGH |
| IO | DIFFIO_TX39p | | B5 | VREF1B5 | | | | K8 | | | HIGH |
| IO | DIFFIO_RX39n | | B5 | VREF1B5 | D2 | J24 | J24 | G1 | | | HIGH |
| IO | DIFFIO_RX39p | | B5 | VREF1B5 | D1 | J23 | J23 | G2 | | | HIGH |
| IO | DIFFIO_TX38n | | B5 | VREF1B5 | J6 | H24 | H24 | J7 | | | HIGH |
| IO | DIFFIO_TX38p | | B5 | VREF1B5 | | H23 | H23 | J8 | | | HIGH |
| IO | DIFFIO_RX38n | | B5 | VREF1B5 | | | | G4 | | | HIGH |
| IO | DIFFIO_RX38p | | B5 | VREF1B5 | | | | G3 | | | HIGH |
| VREF1B5 | | | B5 | VREF1B5 | H5 | J18 | J18 | K9 | | | |
| IO | DIFFIO_TX37n | | B5 | VREF1B5 | J4 | G21 | G21 | K5 | | | HIGH |
| IO | DIFFIO_TX37p | | B5 | VREF1B5 | | G22 | G22 | K6 | | | HIGH |
| IO | DIFFIO_RX37n | | B5 | VREF1B5 | | H25 | H25 | F1 | | | HIGH |
| IO | DIFFIO_RX37p | | B5 | VREF1B5 | | H26 | H26 | F2 | | | HIGH |
| IO | DIFFIO_TX36n | | B5 | VREF1B5 | G5 | G23 | G23 | J6 | | | HIGH |
| IO | DIFFIO_TX36p | | B5 | VREF1B5 | | G24 | G24 | J5 | | | HIGH |
| IO | DIFFIO_RX36n | | B5 | VREF1B5 | | G25 | G25 | F3 | | | HIGH |
| IO | DIFFIO_RX36p | | B5 | VREF1B5 | | G26 | G26 | F4 | | | HIGH |
| IO | DIFFIO_TX35n | | B5 | VREF1B5 | F5 | F23 | F23 | H8 | | | HIGH |
| IO | DIFFIO_TX35p | | B5 | VREF1B5 | | F24 | F24 | H7 | | | HIGH |
| IO | DIFFIO_RX35n | | B5 | VREF1B5 | | F25 | F25 | E1 | | | HIGH |

**Table 2–1. Pin List for the Stratix EP1S20 Device (Part 23 of 39)**

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin FBGA | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | | | |
| IO | DIFFIO_RX35p | | B5 | VREF1B5 | | F26 | F26 | E2 | | | HIGH |
| IO | DIFFIO_TX34n | | B5 | VREF1B5 | F3 | E23 | E23 | H6 | | | HIGH |
| IO | DIFFIO_TX34p | | B5 | VREF1B5 | F4 | E24 | E24 | H5 | | | HIGH |
| IO | DIFFIO_RX34n | | B5 | VREF1B5 | | E25 | E25 | D1 | | | HIGH |
| IO | DIFFIO_RX34p | | B5 | VREF1B5 | | E26 | E26 | D2 | | | HIGH |
| IO | DIFFIO_TX33n | | B5 | VREF1B5 | E3 | D24 | D24 | G5 | | | HIGH |
| IO | DIFFIO_TX33p | | B5 | VREF1B5 | E4 | C25 | C25 | G6 | | | HIGH |
| IO | DIFFIO_RX33n | | B5 | VREF1B5 | | D25 | D25 | C1 | | | HIGH |
| IO | DIFFIO_RX33p | | B5 | VREF1B5 | | C26 | C26 | C2 | | | HIGH |
| IO | | | B4 | VREF0B4 | | | | G7 | | | |
| IO | DQ0T0 | | B4 | VREF0B4 | B3 | B24 | B24 | A4 | | DQ0T0 | |
| IO | | | B4 | VREF0B4 | K7 | C23 | C23 | G12 | | | |
| IO | DQ0T1 | | B4 | VREF0B4 | B2 | D23 | D23 | A3 | | DQ0T1 | |
| IO | DQ0T2 | | B4 | VREF0B4 | D3 | D22 | D22 | B3 | | DQ0T2 | |
| IO | DQS0T | | B4 | VREF0B4 | C2 | C24 | C24 | D5 | | | |
| IO | | | B4 | VREF0B4 | J7 | C19 | C19 | G8 | | | |
| IO | DQ0T3 | | B4 | VREF0B4 | B4 | E22 | E22 | B5 | | DQ0T3 | |
| IO | DQ0T4 | | B4 | VREF0B4 | C3 | B22 | B22 | B4 | | DQ0T4 | |
| IO | DQ0T5 | | B4 | VREF0B4 | C4 | A24 | A24 | C4 | | DQ0T5 | |
| IO | | | B4 | VREF0B4 | | | | F8 | | | |
| IO | DQ0T6 | | B4 | VREF0B4 | D4 | A22 | A22 | A5 | | DQ0T6 | |
| VREF0B4 | | | B4 | VREF0B4 | H6 | F22 | F22 | E7 | | | |

*Table 2–1. Pin List for the Stratix EP1S20 Device (Part 24 of 39)*

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin FBGA | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | | | |
| IO | DQ0T7 | | B4 | VREF0B4 | A4 | C22 | C22 | C5 | | DQ0T7 | |
| IO | | | B4 | VREF0B4 | | | | J9 | | | |
| IO | | | B4 | VREF0B4 | G7 | B21 | B21 | H9 | | | |
| IO | DQ1T0 | | B4 | VREF0B4 | C5 | C20 | C20 | E6 | | DQ0T8 | |
| IO | | | B4 | VREF0B4 | | | | G9 | | | |
| IO | DQ1T1 | | B4 | VREF0B4 | D5 | D21 | D21 | A6 | | DQ0T9 | |
| IO | DQ1T2 | | B4 | VREF0B4 | B5 | D20 | D20 | B7 | | DQ0T10 | |
| IO | DQS1T | | B4 | VREF0B4 | A5 | A21 | A21 | B6 | | | |
| IO | | | B4 | VREF0B4 | | | | F9 | | | |
| IO | DQ1T3 | | B4 | VREF0B4 | C6 | C21 | C21 | D6 | | DQ0T11 | |
| IO | DQ1T4 | | B4 | VREF0B4 | E5 | B20 | B20 | A7 | | DQ0T12 | |
| IO | DQ1T5 | | B4 | VREF0B4 | D6 | E21 | E21 | D7 | | DQ0T13 | |
| IO | DQ1T6 | | B4 | VREF1B4 | A6 | A20 | A20 | C6 | | DQ0T14 | |
| IO | DQ2T0 | | B4 | VREF1B4 | B7 | D19 | D19 | D8 | DQ1T0 | DQ0T16 | |
| IO | DQ1T7 | | B4 | VREF1B4 | B6 | F21 | F21 | C7 | | DQ0T15 | |
| IO | DQ2T1 | | B4 | VREF1B4 | E6 | E20 | E20 | C8 | DQ1T1 | DQ0T17 | |
| IO | | | B4 | VREF1B4 | | | | H10 | | | |
| IO | DQ2T2 | | B4 | VREF1B4 | F7 | E19 | E19 | E8 | DQ1T2 | DQ0T18 | |
| IO | DQS2T | | B4 | VREF1B4 | A7 | A19 | A19 | C9 | | DQS0T | |
| IO | DQ2T3 | | B4 | VREF1B4 | A8 | C18 | C18 | D9 | DQ1T3 | DQ0T19 | |
| IO | DQ2T4 | | B4 | VREF1B4 | D7 | B18 | B18 | B9 | DQ1T4 | DQ0T20 | |
| IO | DQ2T5 | | B4 | VREF1B4 | C7 | D18 | D18 | B8 | DQ1T5 | DQ0T21 | |

*Table 2–1. Pin List for the Stratix EP1S20 Device (Part 25 of 39)*

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin FBGA | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | | | |
| IO | DQ2T6 | | B4 | VREF1B4 | F6 | F20 | F20 | A8 | DQ1T6 | DQ0T22 | |
| IO | DQ2T7 | | B4 | VREF1B4 | E7 | G20 | G20 | A9 | DQ1T7 | DQ0T23 | |
| VREF1B4 | | | B4 | VREF1B4 | H7 | F18 | F18 | E9 | | | |
| IO | FCLK6 | | B4 | VREF1B4 | G8 | G19 | G19 | G10 | | | |
| IO | FCLK7 | | B4 | VREF1B4 | H8 | E18 | E18 | F10 | | | |
| IO | DQ3T0 | | B4 | VREF1B4 | E8 | F19 | F19 | E10 | DQ1T8 | DQ0T24 | |
| IO | DQ3T1 | | B4 | VREF1B4 | C8 | C17 | C17 | A10 | DQ1T9 | DQ0T25 | |
| IO | DQ3T2 | | B4 | VREF1B4 | F8 | G18 | G18 | C10 | DQ1T10 | DQ0T26 | |
| IO | DQS3T | | B4 | VREF1B4 | D8 | B17 | B17 | D10 | DQS1T | | |
| IO | DQ3T3 | | B4 | VREF1B4 | B8 | E17 | E17 | B10 | DQ1T11 | DQ0T27 | |
| IO | | | B4 | VREF1B4 | | | | J10 | | | |
| IO | DQ3T4 | | B4 | VREF1B4 | C9 | F17 | F17 | A11 | DQ1T12 | DQ0T28 | |
| IO | DQ3T5 | | B4 | VREF1B4 | D9 | D17 | D17 | C11 | DQ1T13 | DQ0T29 | |
| IO | DQ3T6 | | B4 | VREF1B4 | E9 | A17 | A17 | D11 | DQ1T14 | DQ0T30 | |
| IO | DQ3T7 | | B4 | VREF1B4 | F9 | H18 | H18 | B11 | DQ1T15 | DQ0T31 | |
| IO | DEV_OE | | B4 | VREF2B4 | L7 | G17 | G17 | J11 | | | |
| IO | | | B4 | VREF2B4 | G9 | B16 | B16 | F11 | | | |
| IO | | | B4 | VREF2B4 | | | | K10 | | | |
| IO | RUP4 | | B4 | VREF2B4 | J8 | D16 | D16 | H11 | | | |
| IO | RDN4 | | B4 | VREF2B4 | K8 | C16 | C16 | G11 | | | |
| IO | DQ4T0 | | B4 | VREF2B4 | B9 | | | B12 | | | |
| IO | | nWS | B4 | VREF2B4 | F10 | E16 | E16 | K11 | | | |

*Table 2–1. Pin List for the Stratix EP1S20 Device (Part 26 of 39)*

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin FBGA | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
| IO | DQ4T1 | | B4 | VREF2B4 | C10 | | | C12 | | | |
| IO | DQ4T2 | | B4 | VREF2B4 | B10 | | | D12 | | | |
| IO | DQS4T | | B4 | VREF2B4 | D10 | | | A13 | | | |
| IO | | DATA0 | B4 | VREF2B4 | L8 | F16 | F16 | H12 | | | |
| IO | DQ4T3 | | B4 | VREF2B4 | E10 | | | B13 | | | |
| VREF2B4 | | | B4 | VREF2B4 | H9 | G16 | G16 | E11 | | | |
| IO | DQ4T4 | | B4 | VREF2B4 | C11 | | | E12 | | | |
| IO | DQ4T5 | | B4 | VREF2B4 | D11 | | | C13 | | | |
| IO | | DATA1 | B4 | VREF2B4 | J9 | C15 | C15 | F12 | | | |
| IO | DQ4T6 | | B4 | VREF2B4 | E11 | | | D13 | | | |
| IO | DQ4T7 | | B4 | VREF2B4 | E12 | | | E13 | | | |
| IO | | DATA2 | B4 | VREF2B4 | H10 | H16 | H16 | J12 | | | |
| TMS | | TMS | B4 | VREF2B4 | G10 | E15 | E15 | F13 | | | |
| TRST | | TRST | B4 | VREF2B4 | J10 | D15 | D15 | L12 | | | |
| TCK | | TCK | B4 | VREF2B4 | K9 | G15 | G15 | K12 | | | |
| IO | | DATA3 | B4 | VREF2B4 | K10 | F15 | F15 | M12 | | | |
| IO | | | B4 | VREF2B4 | | | | L11 | | | |
| IO | | | B4 | VREF2B4 | | | | M11 | | | |
| TDI | | TDI | B4 | VREF2B4 | J11 | H15 | H15 | G13 | | | |
| TDO | | TDO | B4 | VREF2B4 | H11 | G14 | G14 | H13 | | | |
| IO | CLK12n | | B4 | VREF2B4 | | | | J13 | | | |
| CLK12p | | | B4 | VREF2B4 | A11 | B15 | B15 | K13 | | | |

*Table 2–1. Pin List for the Stratix EP1S20 Device (Part 27 of 39)*

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin FBGA | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | | | |
| IO | CLK13n | | B4 | VREF2B4 | | | | L13 | | | |
| CLK13p | | | B4 | VREF2B4 | B11 | A15 | A15 | M13 | | | |
| TEMPDIODEp | | | | | G12 | H14 | H14 | B14 | | | |
| TEMPDIODEn | | | | | H12 | G13 | G13 | C14 | | | |
| VCCINT | | | | | | | | | | | |
| VCCA_PLL5 | | | | | G13 | D14 | D14 | F14 | | | |
| GND | | | | | | | | | | | |
| GNDA_PLL5 | | | | | F12 | B14 | B14 | G14 | | | |
| GNDA_PLL5 | | | | | | | | | | | |
| VCCG_PLL5 | | | | | F11 | C14 | C14 | D14 | | | |
| GNDG_PLL5 | | | | | G11 | B13 | B13 | E14 | | | |
| VCC_PLL5_OUTA | | | B9 | | F13 | D13 | D13 | F15 | | | |
| VCC_PLL5_OUTA | | | B9 | | | | | | | | |
| VCC_PLL5_OUTB | | | B10 | | | | | G16 | | | |
| VCC_PLL5_OUTB | | | B10 | | | | | | | | |
| IO | PLL5_OUT0p | | B9 | VREF0B3 | C13 | F13 | F13 | E15 | | | |
| IO | PLL5_OUT0n | | B9 | VREF0B3 | B13 | E13 | E13 | D15 | | | |
| IO | PLL5_OUT1p | | B9 | VREF0B3 | B12 | F14 | F14 | K14 | | | |
| IO | PLL5_OUT1n | | B9 | VREF0B3 | A12 | E14 | E14 | K15 | | | |
| IO | PLL5_FBp | | B9 | VREF0B3 | D12 | F12 | F12 | H14 | | | |
| IO | PLL5_FBn | | B9 | VREF0B3 | C12 | E12 | E12 | H15 | | | |
| IO | PLL5_OUT2p | | B10 | VREF0B3 | | | | C15 | | | |

*Table 2–1. Pin List for the Stratix EP1S20 Device (Part 28 of 39)*

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin FBGA | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | | | |
| IO | PLL5_OUT2n | | B10 | VREF0B3 | | | | B15 | | | |
| IO | PLL5_OUT3p | | B10 | VREF0B3 | | | | K16 | | | |
| IO | PLL5_OUT3n | | B10 | VREF0B3 | | | | J16 | | | |
| nSTATUS | | nSTATUS | B3 | VREF0B3 | J12 | H13 | H13 | M16 | | | |
| nCONFIG | | nCONFIG | B3 | VREF0B3 | H13 | H12 | H12 | L16 | | | |
| DCLK | | DCLK | B3 | VREF0B3 | J13 | G12 | G12 | F16 | | | |
| CONF_DONE | | CONF_DONE | B3 | VREF0B3 | K13 | H11 | H11 | G17 | | | |
| CLK14p | | | B3 | VREF0B3 | B14 | B12 | B12 | K17 | | | |
| IO | CLK14n | | B3 | VREF0B3 | C14 | A12 | A12 | J17 | | | |
| CLK15p | | | B3 | VREF0B3 | E13 | D12 | D12 | M17 | | | |
| IO | CLK15n | | B3 | VREF0B3 | D13 | C12 | C12 | L17 | | | |
| VREF0B3 | | | B3 | VREF0B3 | H14 | F11 | F11 | E18 | | | |
| IO | | | B3 | VREF0B3 | | | | L18 | | | |
| IO | | | B3 | VREF0B3 | | | | M18 | | | |
| IO | | DATA4 | B3 | VREF0B3 | K14 | E11 | E11 | H17 | | | |
| IO | | | B3 | VREF0B3 | J14 | B11 | B11 | F17 | | | |
| IO | | | B3 | VREF0B3 | | | | F18 | | | |
| IO | DQ5T0 | | B3 | VREF0B3 | | | | D16 | | | |
| IO | DQ5T1 | | B3 | VREF0B3 | | | | C16 | | | |
| IO | DQ5T2 | | B3 | VREF0B3 | | | | E16 | | | |
| IO | | DATA5 | B3 | VREF0B3 | G14 | G11 | G11 | K18 | | | |
| IO | DQS5T | | B3 | VREF0B3 | | | | A16 | | | |

*Table 2–1. Pin List for the Stratix EP1S20 Device (Part 29 of 39)*

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin FBGA | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | | | |
| IO | DQ5T3 | | B3 | VREF0B3 | | | | B16 | | | |
| IO | DQ5T4 | | B3 | VREF0B3 | | | | E17 | | | |
| IO | | DATA6 | B3 | VREF1B3 | K15 | H10 | H10 | H18 | | | |
| IO | DQ5T5 | | B3 | VREF1B3 | | | | D17 | | | |
| IO | DQ5T6 | | B3 | VREF1B3 | | | | B17 | | | |
| IO | DQ5T7 | | B3 | VREF1B3 | | | | C17 | | | |
| IO | RUP3 | | B3 | VREF1B3 | M15 | C11 | C11 | J18 | | | |
| IO | RDN3 | | B3 | VREF1B3 | L15 | D11 | D11 | K19 | | | |
| IO | DQ6T0 | | B3 | VREF1B3 | A15 | A10 | A10 | A18 | DQ2T0 | DQ1T0 | |
| IO | DQ6T1 | | B3 | VREF1B3 | C15 | E10 | E10 | C18 | DQ2T1 | DQ1T1 | |
| IO | DQ6T2 | | B3 | VREF1B3 | D14 | F10 | F10 | D18 | DQ2T2 | DQ1T2 | |
| IO | | DATA7 | B3 | VREF1B3 | J15 | G10 | G10 | G18 | | | |
| IO | DQS6T | | B3 | VREF1B3 | F14 | G9 | G9 | B18 | DQS2T | | |
| IO | DQ6T3 | | B3 | VREF1B3 | E14 | F9 | F9 | A19 | DQ2T3 | DQ1T3 | |
| GND | | | B3 | | | GND | GND | | | | |
| GND | | | B3 | | | | | | | | |
| GND | | | B3 | | G15 | F8 | F8 | G20 | | | |
| IO | FCLK0 | | B3 | VREF1B3 | K16 | E9 | E9 | F19 | | | |
| IO | FCLK1 | | B3 | VREF1B3 | J16 | B9 | B9 | G19 | | | |
| IO | | CLKUSR | B3 | VREF1B3 | L16 | D10 | D10 | J19 | | | |
| IO | DQ6T4 | | B3 | VREF1B3 | D15 | C10 | C10 | B19 | DQ2T4 | DQ1T4 | |
| IO | DQ6T5 | | B3 | VREF1B3 | E15 | B10 | B10 | C19 | DQ2T5 | DQ1T5 | |

*Table 2–1. Pin List for the Stratix EP1S20 Device (Part 30 of 39)*

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin FBGA | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | | | |
| IO | DQ6T6 | | B3 | VREF1B3 | F15 | A9 | A9 | E19 | DQ2T6 | DQ1T6 | |
| VREF1B3 | | | B3 | VREF1B3 | H15 | D9 | D9 | E20 | | | |
| IO | DQ6T7 | | B3 | VREF1B3 | B15 | C9 | C9 | D19 | DQ2T7 | DQ1T7 | |
| IO | DQ7T0 | | B3 | VREF1B3 | A16 | A8 | A8 | B20 | DQ2T8 | DQ1T8 | |
| IO | | | B3 | VREF1B3 | | | | H19 | | | |
| IO | DQ7T1 | | B3 | VREF1B3 | E16 | A7 | A7 | A20 | DQ2T9 | DQ1T9 | |
| IO | | | B3 | VREF1B3 | | | | J20 | | | |
| IO | DQ7T2 | | B3 | VREF1B3 | G16 | B8 | B8 | C20 | DQ2T10 | DQ1T10 | |
| IO | DQS7T | | B3 | VREF1B3 | B16 | E8 | E8 | D20 | | DQS1T | |
| IO | DQ7T3 | | B3 | VREF1B3 | C16 | F7 | F7 | A21 | DQ2T11 | DQ1T11 | |
| IO | DQ7T4 | | B3 | VREF1B3 | D16 | B7 | B7 | B21 | DQ2T12 | DQ1T12 | |
| IO | DQ7T5 | | B3 | VREF1B3 | F16 | C8 | C8 | C21 | DQ2T13 | DQ1T13 | |
| IO | DQ7T6 | | B3 | VREF1B3 | E17 | D8 | D8 | D21 | DQ2T14 | DQ1T14 | |
| IO | DQ7T7 | | B3 | VREF1B3 | F17 | E7 | E7 | E21 | DQ2T15 | DQ1T15 | |
| IO | DQ8T0 | | B3 | VREF2B3 | A17 | B6 | B6 | B22 | DQ3T0 | DQ1T16 | |
| IO | DQ8T1 | | B3 | VREF2B3 | B17 | A6 | A6 | A22 | DQ3T1 | DQ1T17 | |
| IO | DQ8T2 | | B3 | VREF2B3 | C17 | F6 | F6 | C22 | DQ3T2 | DQ1T18 | |
| IO | DQS8T | | B3 | VREF2B3 | C18 | F5 | F5 | D23 | DQS3T | | |
| IO | DQ8T3 | | B3 | VREF2B3 | D17 | D6 | D6 | D22 | DQ3T3 | DQ1T19 | |
| IO | DQ8T4 | | B3 | VREF2B3 | E18 | E6 | E6 | A23 | DQ3T4 | DQ1T20 | |
| IO | DQ8T5 | | B3 | VREF2B3 | A18 | A5 | A5 | C23 | DQ3T5 | DQ1T21 | |
| IO | DQ8T6 | | B3 | VREF2B3 | B18 | E5 | E5 | E23 | DQ3T6 | DQ1T22 | |

*Table 2–1. Pin List for the Stratix EP1S20 Device (Part 31 of 39)*

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin FBGA | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | | | |
| IO | | | B3 | VREF2B3 | | | | H20 | | | |
| IO | DQ8T7 | | B3 | VREF2B3 | D18 | C7 | C7 | B23 | DQ3T7 | DQ1T23 | |
| IO | | | B3 | VREF2B3 | | | | F20 | | | |
| IO | | | B3 | VREF2B3 | | | | F21 | | | |
| VREF2B3 | | | B3 | VREF2B3 | H16 | D7 | D7 | E22 | | | |
| IO | DQ9T0 | | B3 | VREF2B3 | A19 | C3 | C3 | A24 | DQ3T8 | DQ1T24 | |
| IO | DQ9T1 | | B3 | VREF2B3 | B19 | A3 | A3 | C25 | DQ3T9 | DQ1T25 | |
| IO | DQ9T2 | | B3 | VREF2B3 | C19 | D5 | D5 | A25 | DQ3T10 | DQ1T26 | |
| IO | DQS9T | | B3 | VREF2B3 | C21 | B4 | B4 | C24 | | | |
| IO | DQ9T3 | | B3 | VREF2B3 | D19 | C2 | C2 | D24 | DQ3T11 | DQ1T27 | |
| IO | | | B3 | VREF2B3 | | | | G21 | | | |
| IO | DQ9T4 | | B3 | VREF2B3 | B20 | B3 | B3 | B24 | DQ3T12 | DQ1T28 | |
| IO | DQ9T5 | | B3 | VREF2B3 | B21 | D4 | D4 | B25 | DQ3T13 | DQ1T29 | |
| IO | DQ9T6 | | B3 | VREF2B3 | C20 | C4 | C4 | A26 | DQ3T14 | DQ1T30 | |
| IO | | | B3 | VREF2B3 | M16 | C5 | C5 | G22 | | | |
| IO | DQ9T7 | | B3 | VREF2B3 | D20 | D3 | D3 | B26 | DQ3T15 | DQ1T31 | |
| IO | | | B3 | VREF2B3 | | | | F22 | | | |
| VCCIO2 | | | | | C22 | D1 | D1 | B28 | | | |
| VCCIO2 | | | | | K22 | L1 | L1 | M28 | | | |
| VCCIO2 | | | | | | L9 | L9 | P20 | | | |
| VCCIO1 | | | | | N22 | T1 | T1 | R20 | | | |
| VCCIO1 | | | | | Y22 | AC1 | AC1 | U28 | | | |

*Table 2–1. Pin List for the Stratix EP1S20 Device (Part 32 of 39)*

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin FBGA | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
| VCCIO1 | | | | | | T9 | T9 | AG28 | | | |
| VCCIO8 | | | | | AB20 | AF4 | AF4 | Y15 | | | |
| VCCIO8 | | | | | AB13 | AF11 | AF11 | AH17 | | | |
| VCCIO8 | | | | | | V11 | V11 | AH27 | | | |
| VCCIO8 | | | | | | V12 | V12 | | | | |
| VCCIO7 | | | | | AB10 | V15 | V15 | Y14 | | | |
| VCCIO7 | | | | | AB3 | V16 | V16 | AH2 | | | |
| VCCIO7 | | | | | | AF16 | AF16 | AH12 | | | |
| VCCIO7 | | | | | | AF23 | AF23 | | | | |
| VCCIO6 | | | | | Y1 | T18 | T18 | R9 | | | |
| VCCIO6 | | | | | N1 | AC26 | AC26 | U1 | | | |
| VCCIO6 | | | | | | T26 | T26 | AG1 | | | |
| VCCIO5 | | | | | K1 | L26 | L26 | B1 | | | |
| VCCIO5 | | | | | C1 | L18 | L18 | M1 | | | |
| VCCIO5 | | | | | | D26 | D26 | P9 | | | |
| VCCIO4 | | | | | A3 | A23 | A23 | A2 | | | |
| VCCIO4 | | | | | A10 | A16 | A16 | A12 | | | |
| VCCIO4 | | | | | | J15 | J15 | J14 | | | |
| VCCIO4 | | | | | | J16 | J16 | | | | |
| VCCIO3 | | | | | A13 | A4 | A4 | A17 | | | |
| VCCIO3 | | | | | A20 | A11 | A11 | A27 | | | |
| VCCIO3 | | | | | | J11 | J11 | J15 | | | |

**Table 2–1. Pin List for the Stratix EP1S20 Device (Part 33 of 39)**

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin FBGA | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
| VCCIO3 | | | | | | J12 | J12 | | | | |
| VCCINT | | | | | A1 | K11 | K11 | M14 | | | |
| VCCINT | | | | | A22 | K13 | K13 | N11 | | | |
| VCCINT | | | | | AB1 | K15 | K15 | N13 | | | |
| VCCINT | | | | | AB22 | K17 | K17 | N15 | | | |
| VCCINT | | | | | K12 | L10 | L10 | N17 | | | |
| VCCINT | | | | | L11 | L12 | L12 | P12 | | | |
| VCCINT | | | | | L13 | L14 | L14 | P14 | | | |
| VCCINT | | | | | L9 | L16 | L16 | P16 | | | |
| VCCINT | | | | | M10 | M11 | M11 | R13 | | | |
| VCCINT | | | | | M12 | M13 | M13 | R15 | | | |
| VCCINT | | | | | M14 | M15 | M15 | R17 | | | |
| VCCINT | | | | | N11 | M17 | M17 | T12 | | | |
| VCCINT | | | | | | N10 | N10 | T14 | | | |
| VCCINT | | | | | | N12 | N12 | T16 | | | |
| VCCINT | | | | | | N14 | N14 | T18 | | | |
| VCCINT | | | | | | N16 | N16 | U11 | | | |
| VCCINT | | | | | | P11 | P11 | U13 | | | |
| VCCINT | | | | | | P13 | P13 | U15 | | | |
| VCCINT | | | | | | P15 | P15 | U17 | | | |
| VCCINT | | | | | | P17 | P17 | V12 | | | |
| VCCINT | | | | | | R10 | R10 | V16 | | | |

Table 2–1. Pin List for the Stratix EP1S20 Device (Part 34 of 39)

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin FBGA | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | | | |
| VCCINT | | | | | | R12 | R12 | | | | |
| VCCINT | | | | | | R14 | R14 | | | | |
| VCCINT | | | | | | R16 | R16 | | | | |
| VCCINT | | | | | | T11 | T11 | | | | |
| VCCINT | | | | | | T13 | T13 | | | | |
| VCCINT | | | | | | T15 | T15 | | | | |
| VCCINT | | | | | | T17 | T17 | | | | |
| VCCINT | | | | | | U10 | U10 | | | | |
| VCCINT | | | | | | U12 | U12 | | | | |
| VCCINT | | | | | | U14 | U14 | | | | |
| VCCINT | | | | | | U16 | U16 | | | | |
| GND | | | | | A14 | A13 | A13 | A14 | | | |
| GND | | | | | A2 | A14 | A14 | A15 | | | |
| GND | | | | | A21 | A2 | A2 | AA16 | | | |
| GND | | | | | A9 | A25 | A25 | AC15 | | | |
| GND | | | | | AA1 | AC13 | AC13 | AF26 | | | |
| GND | | | | | AA22 | AE1 | AE1 | AF3 | | | |
| GND | | | | | AB14 | AE26 | AE26 | AG2 | | | |
| GND | | | | | AB2 | AF13 | AF13 | AG27 | | | |
| GND | | | | | AB21 | AF14 | AF14 | AH14 | | | |
| GND | | | | | AB9 | AF2 | AF2 | AH15 | | | |
| GND | | | | | B1 | AF25 | AF25 | B2 | | | |

*Table 2–1. Pin List for the Stratix EP1S20 Device (Part 35 of 39)*

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin FBGA | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | | | |
| GND | | | | | B22 | B1 | B1 | B27 | | | |
| GND | | | | | G17 | B2 | B2 | C26 | | | |
| GND | | | | | G6 | B26 | B26 | C3 | | | |
| GND | | | | | J1 | C13 | C13 | G15 | | | |
| GND | | | | | J22 | G8 | G8 | H16 | | | |
| GND | | | | | K11 | H17 | H17 | L14 | | | |
| GND | | | | | L10 | H9 | H9 | L15 | | | |
| GND | | | | | L12 | J10 | J10 | M15 | | | |
| GND | | | | | L14 | J13 | J13 | N12 | | | |
| GND | | | | | M11 | J14 | J14 | N14 | | | |
| GND | | | | | M13 | J17 | J17 | N16 | | | |
| GND | | | | | M9 | J9 | J9 | N18 | | | |
| GND | | | | | N12 | K10 | K10 | P1 | | | |
| GND | | | | | P1 | K12 | K12 | P11 | | | |
| GND | | | | | P22 | K14 | K14 | P13 | | | |
| GND | | | | | T17 | K16 | K16 | P15 | | | |
| GND | | | | | T6 | K18 | K18 | P17 | | | |
| GND | | | | | | L11 | L11 | P18 | | | |
| GND | | | | | | L13 | L13 | P28 | | | |
| GND | | | | | | L15 | L15 | R1 | | | |
| GND | | | | | | L17 | L17 | R11 | | | |
| GND | | | | | | M10 | M10 | R12 | | | |

Table 2–1. Pin List for the Stratix EP1S20 Device (Part 36 of 39)

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin FBGA | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
| GND | | | | | | M12 | M12 | R14 | | | |
| GND | | | | | | M14 | M14 | R16 | | | |
| GND | | | | | | M16 | M16 | R18 | | | |
| GND | | | | | | N1 | N1 | R28 | | | |
| GND | | | | | | N11 | N11 | T11 | | | |
| GND | | | | | | N13 | N13 | T13 | | | |
| GND | | | | | | N15 | N15 | T15 | | | |
| GND | | | | | | N17 | N17 | T17 | | | |
| GND | | | | | | N18 | N18 | U12 | | | |
| GND | | | | | | N26 | N26 | U14 | | | |
| GND | | | | | | N9 | N9 | U16 | | | |
| GND | | | | | | P1 | P1 | U18 | | | |
| GND | | | | | | P10 | P10 | V13 | | | |
| GND | | | | | | P12 | P12 | V14 | | | |
| GND | | | | | | P14 | P14 | V15 | | | |
| GND | | | | | | P16 | P16 | V17 | | | |
| GND | | | | | | P18 | P18 | | | | |
| GND | | | | | | P26 | P26 | | | | |
| GND | | | | | | P9 | P9 | | | | |
| GND | | | | | | R11 | R11 | | | | |
| GND | | | | | | R13 | R13 | | | | |
| GND | | | | | | R15 | R15 | | | | |

**Table 2–1. Pin List for the Stratix EP1S20 Device (Part 37 of 39)**

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin FBGA | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
| GND | | | | | | R17 | R17 | | | | |
| GND | | | | | | T10 | T10 | | | | |
| GND | | | | | | T12 | T12 | | | | |
| GND | | | | | | T14 | T14 | | | | |
| GND | | | | | | T16 | T16 | | | | |
| GND | | | | | | U11 | U11 | | | | |
| GND | | | | | | U13 | U13 | | | | |
| GND | | | | | | U15 | U15 | | | | |
| GND | | | | | | U17 | U17 | | | | |
| GND | | | | | | V10 | V10 | | | | |
| GND | | | | | | V13 | V13 | | | | |
| GND | | | | | | V14 | V14 | | | | |
| GND | | | | | | V17 | V17 | | | | |
| GND | | | | | | V18 | V18 | | | | |
| GND | | | | | | V9 | V9 | | | | |
| No connection | | | | | | A18 | A18 | AB23 | | | |
| No connection | | | | | | AA16 | AA16 | AB24 | | | |
| No connection | | | | | | AC18 | AC18 | AB5 | | | |
| No connection | | | | | | AC5 | AC5 | AB6 | | | |
| No connection | | | | | | AC6 | AC6 | AC24 | | | |
| No connection | | | | | | AD18 | AD18 | AC25 | | | |
| No connection | | | | | | AD23 | AD23 | AC26 | | | |

*Table 2–1. Pin List for the Stratix EP1S20 Device (Part 38 of 39)*

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin FBGA | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
| No connection | | | | | | AD24 | AD24 | AC3 | | | |
| No connection | | | | | | AF5 | AF5 | AC4 | | | |
| No connection | | | | | | B19 | B19 | AC6 | | | |
| No connection | | | | | | B23 | B23 | AD25 | | | |
| No connection | | | | | | B25 | B25 | AD26 | | | |
| No connection | | | | | | B5 | B5 | AD3 | | | |
| No connection | | | | | | C6 | C6 | AD4 | | | |
| No connection | | | | | | G7 | G7 | AE26 | | | |
| No connection | | | | | | H19 | H19 | D25 | | | |
| No connection | | | | | | H20 | H20 | D26 | | | |
| No connection | | | | | | H21 | H21 | D3 | | | |
| No connection | | | | | | H22 | H22 | D4 | | | |
| No connection | | | | | | H7 | H7 | E25 | | | |
| No connection | | | | | | J1 | J1 | E26 | | | |
| No connection | | | | | | J2 | J2 | E3 | | | |
| No connection | | | | | | J25 | J25 | E4 | | | |
| No connection | | | | | | J26 | J26 | E5 | | | |
| No connection | | | | | | J5 | J5 | F23 | | | |
| No connection | | | | | | J6 | J6 | F24 | | | |
| No connection | | | | | | J7 | J7 | F5 | | | |
| No connection | | | | | | R18 | R18 | F6 | | | |
| No connection | | | | | | V1 | V1 | F7 | | | |

**Table 2–1. Pin List for the Stratix EP1S20 Device (Part 39 of 39)**

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 484-Pin FBGA | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | | | |
| No connection | | | | | | V2 | V2 | P19 | | | |
| No connection | | | | | | V21 | V21 | R10 | | | |
| No connection | | | | | | V22 | V22 | | | | |
| No connection | | | | | | V23 | V23 | | | | |
| No connection | | | | | | V24 | V24 | | | | |
| No connection | | | | | | V25 | V25 | | | | |
| No connection | | | | | | V26 | V26 | | | | |
| No connection | | | | | | V3 | V3 | | | | |
| No connection | | | | | | V4 | V4 | | | | |
| No connection | | | | | | W1 | W1 | | | | |
| No connection | | | | | | W19 | W19 | | | | |
| No connection | | | | | | W2 | W2 | | | | |
| No connection | | | | | | W20 | W20 | | | | |
| No connection | | | | | | W25 | W25 | | | | |
| No connection | | | | | | W26 | W26 | | | | |
| No connection | | | | | | W5 | W5 | | | | |
| No connection | | | | | | W6 | W6 | | | | |
| No connection | | | | | | W7 | W7 | | | | |
| No connection | | | | | | W8 | W8 | | | | |
| No connection | | | | | | Y7 | Y7 | | | | |

*Note to Table 2–1:*

(1) The wire bond and flip-chip packages have different data rates for the high speed differential I/O channels. Table 2–2 shows the data rates as supported for each package.

*Table 2–2. High Speed Differential I/O Channel Data Rates*

| Package | Package Type | High Speed Differential I/O Channel Performance (DIFFIO Speed) | | Units |
|---|---|---|---|---|
| | | High | Low | |
| 484-pin FineLine BGA | flip chip | 840 | N/A | Mbps |
| 672-pin BGA | wire bond | 462 | N/A | Mbps |
| 672-pin FineLine BGA | wire bond | 462 | N/A | Mbps |
| 780-pin FineLine BGA | flip chip | 840 | N/A | Mbps |

## Pin Definitions

Table 2–3 shows pin definitions for the EP1S20 device.

*Table 2–3. Pin Definitions for the EP1S20 Device (Part 1 of 5)*

| Pin Name | Pin Type (1st, 2nd, & 3rd Function) | Pin Description |
|---|---|---|
| **Supply and Reference Pins** | | |
| VREF[1..4]B[1..8] | Input | Input reference voltage for each I/O bank. If a bank is used for a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for that bank. All of the VREF pins within a bank are shorted together. Each VREF pin can support up to 20 inputs on each side. If VREF pins are not used, designers should connect them to either VCC or Gnd. |
| VCCIO[1..8] | Power | These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards. VCCIO also supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5-V, 1.8-V, 2.5-V, 3.3-V PCI, and 3.3-V PCI-X I/O standards. |
| VCCINT | Power | These are internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVDS, LVPECL, 3.3-V PCML, HyperTransport™ technology, differential HSTL, GTL, GTL+, HSTL, SSTL, CTT, and 3.3-V AGP I/O standards. |
| VCC_PLL5_OUTA | Power | External clock output buffer power for PLL5 clock outputs PLL5_OUT[1..0]. The designer must connect this pin to the VCCIO of bank 9. |
| VCC_PLL5_OUTB | Power | External clock output buffer power for PLL5 clock outputs PLL5_OUT[3..2]. The designer must connect this pin to the VCCIO of bank 10. |
| VCC_PLL6_OUTA | Power | External clock output buffer power for PLL6 clock outputs PLL6_OUT[1..0]. The designer must connect this pin to the VCCIO of bank 11. |
| VCC_PLL6_OUTB | Power | External clock output buffer power for PLL6 clock outputs PLL6_OUT[3..2]. The designer must connect this pin to the VCCIO of bank 12. |
| VCCA_PLL[1..12] | Power | Analog power for PLLs[1..12]. The designer must connect this pin to 1.5 V, even if the PLL is not used. |
| GNDA_PLL[1..12] | Ground | Analog ground for PLLs[1..12]. The designer can connect this pin to the GND plane on the board. |
| VCCG_PLL[1..12] | Power | Guard ring power for PLLs[1..12]. The designer must connect this pin to 1.5 V, even if the PLL is not used. |
| GNDG_PLL[1..12] | Ground | Guard ring ground for PLLs[1..12]. The designer can connect this pin to the GND plane on the board. |

*Table 2–3. Pin Definitions for the EP1S20 Device (Part 2 of 5)*

| Pin Name | Pin Type (1st, 2nd, & 3rd Function) | Pin Description |
|---|---|---|
| **Dedicated & Configuration/JTAG Pins** | | |
| CONF_DONE | Bidirectional (open-drain) | This is a dedicated configuration status pin; it is not available as a user I/O pin. |
| nSTATUS | Bidirectional (open-drain) | This is a dedicated configuration status pin; it is not available as a user I/O pin. |
| nCONFIG | Input | Dedicated configuration control input. A low transition resets the target device; a low-to-high transition begins configuration. All I/O pins tri-state when nCONFIG is driven low. |
| DCLK | Input | Clock input used to clock configuration data from an external source into the Stratix device. This is a dedicated pin used for configuration. |
| nIO_PULLUP | Input | IF nIO_PULLUP is driven high during configuration, the weak pull-ups on all user I/O pins are disabled. If driven low, the weak pull-ups are enabled during configuration. nIO_PULLUP can be pulled up to either 1.5, 1.8, 2.5, or 3.3 V. |
| PORSEL | Input | Dedicated input pin used to select POR delay times of 2 ms or 100 ms during powerup. When PORSEL is connected to ground, the POR time is 100 ms. When PORSEL is connected to 3.3 V, the POR time is 2 ms. |
| VCCSEL | Input | VCCSEL is used to select which input buffer is used on all configuration pins. VCCSEL will control whether the 3.3-/2.5-V input buffer or the 1.8-/1.5-V input buffer is used. A "0" means 3.3/2.5 V and a "1" means 1.8-/1.5 V. At powerup, VCCSEL accepts 3.3V and 2.5V TTL Levels. VCCSEL affects the following pins: TDI, TMS, TCK, TRST, MSEL0, MSEL1, MSEL2, nCONFIG, nCE, DCLK, CONF_DONE, nSTATUS, and PLL_ENA. |
| nCE | Input | Active-low chip enables. Dedicated chip enable input used to detect which device is active in a chain of devices. When nCE is low, the device is enabled. When nCE is high, the device is disabled. |
| nCEO | Output | Output that drives low when device configuration is complete. During multi-device configuration, this pin feeds a subsequent device's nCE pin. |
| TMS | Input | This is a dedicated JTAG input pin. |
| TDI | Input | This is a dedicated JTAG input pin. |
| TCK | Input | This is a dedicated JTAG input pin. |

*Table 2–3. Pin Definitions for the EP1S20 Device (Part 3 of 5)*

| Pin Name | Pin Type (1st, 2nd, & 3rd Function) | Pin Description |
|---|---|---|
| TDO | Output | This is a dedicated JTAG input pin. |
| TRST | Input | This is a dedicated JTAG input pin. Active low input, used to asynchronously reset the JTAG boundary scan circuit. |
| MSEL[2..0] | Input | Dedicated mode select control pins that set the configuration mode for the device. |
| TEMPDIODEp | Input | Pin used in conjunction with the temperature sensing diode (bias-high input) inside the Stratix device. If the temperature sensing diode is not used then connect this pin to GND. |
| TEMPDIODEn | Input | Pin used in conjunction with the temperature sensing diode (bias-low input) inside the Stratix device. If the temperature sensing diode is not used then connect this pin to GND. |
| **Clock and PLL Pins** | | |
| PLL_ENA | Input | Dedicated input pin that drives the optional pllena port of all or a set of PLLs. If a PLL uses the pllena port, drive the PLL_ENA pin low to reset all PLLs including the counters to their default state. If VCCSEL = 0, then you must drive the PLL_ENA with a 3.3/2.5 V signal to enable the PLLs. If VCCSEL = 1, connect PLL_ENA to 1.8/1.5 V to enable the PLLs. |
| FCLK[7..0] | Bidirectional | Optional fast regional clock pins. FCLK pins can also be used as type input, output, or as bidirectional pins. |
| CLK[15..0]p | Input | Dedicated global clock inputs 0 to 15. |
| CLK[15..0]n | I/O, Input | Optional negative terminal input for differential global clock input. |
| PLL6_OUT[3..0]p | I/O, Output | Optional external clock outputs [3..0] from enhanced PLL 6. These pins can be differential (four output pin pairs) or single ended (eight clock outputs from PLL6). |
| PLL6_OUT[3..0]n | I/O, Output | Optional negative terminal for external clock outputs [3..0] from PLL6. If the clock outputs are single ended, then each pair of pins (i.e., PLL6_OUT0p and PLL6_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase. |
| PLL5_OUT[3..0]p | I/O, Output | Optional external clock outputs [3..0] from enhanced PLL 5. These pins can be differential (four output pin pairs) or single ended (eight clock outputs from PLL5). |
| PLL5_OUT[3..0]n | I/O, Output | Optional negative terminal for external clock outputs [3..0] from PLL 5. If the clock outputs are single ended, then each pair of pins (i.e., PLL5_OUT0p and PLL5_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase. |

*Table 2–3. Pin Definitions for the EP1S20 Device (Part 4 of 5)*

| Pin Name | Pin Type (1st, 2nd, & 3rd Function) | Pin Description |
|---|---|---|
| **Optional/Dual-Purpose Pins** | | |
| DATA0 | I/O, Input | Dual-purpose configuration data input pin. Can be used as an I/O pin after configuration is complete. |
| DIFFIO_TX[0..151]n | I/O, Output | This pin can be used as the complementary signal of the differential inputs and outputs. If not used for the differential pair, these pins are regular I/O pins. Pins with an n suffix carry the negative signal for the differential channel. Pins with a p suffix carry the positive signal for the differential channel. |
| PLL5_FBp | I/O, Input | External feedback input pin for PLL5. This pin can be used as a user I/O pin if external feedback mode is not used. |
| PLL5_FBn | I/O, Input | Negative terminal input for external feedback input PLL5_FBp |
| PLL6_FBp | I/O, Input | External feedback input pin for PLL6 |
| PLL6_FBn | I/O, Input | Negative terminal input for external feedback input PLL6_FBp |
| INIT_DONE | I/O, Output | This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration. |
| DATA[7..1] | I/O, Input | Dual-purpose configuration input data pins. These pins can be used for configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration. |
| nRS | I/O, Input | Read strobe input pin. This pin can be used as a user I/O pin after configuration. |
| DEV_CLRn | I/O, Input | Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as defined in the users design. |
| DEV_OE | I/O, Input | Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design. |
| CLKUSR | I/O, Input | Optional user-supplied clock input. Synchronizes the initialization of one or more devices. This pin can be used as a user I/O pin after configuration. |
| RDYnBSY | I/O, Output | Ready not busy output. A high output indicates that the target device is ready to accept another data byte. A low output indicates that the target device is not ready to receive another data byte. This pin can be used as a user I/O pin after configuration |

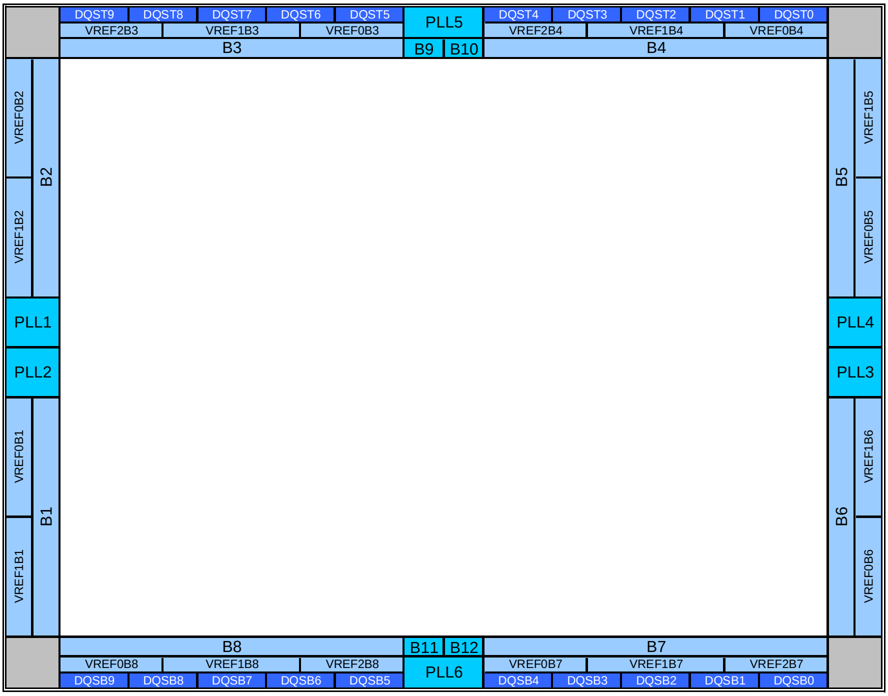
*Table 2–3. Pin Definitions for the EP1S20 Device (Part 5 of 5)*

| Pin Name | Pin Type (1st, 2nd, & 3rd Function) | Pin Description |
|---|---|---|
| nCS,CS | I/O, Input | These are chip-select inputs that enable the Stratix device in the passive parallel asynchronous configuration mode. Drive nCS low and CS high to target a device for configuration. If a design requires an active high enable, use the CS pin and drive the nCS pin low. If a design requires an active low enable, use the nCS pin and drive the CS pin high. Configuration will be paused when either signal is inactive. Hold the nCS and CS pins active during configuration and initialization. The design can use these pins as user I/O pins after configuration. |
| nWS | I/O, Input | Active-low write strobe input to latch a byte of data on the DATA pins. This pin can be used as a user I/O pin after configuration. |
| PGM[2..0] | I/O, Output | These output pins control one of eight pages in the EPC16 configuration device when using remote update or local update configuration modes. When not using remote update or local update configuration modes, these pins are user I/O pins. |
| RUP[8..1] | I/O, Input | Reference pins for banks 8 to 1. The external precision resistors $R_{UP}$ must be connected to the designated RUP pin on that I/O bank. If not required, these pins are regular I/O pins. |
| RDN[8..1] | I/O, Input | Reference pins for banks 8 to 1. The external precision resistors RDN must be connected to the designated RDN pin on that I/O bank. If not required, these pins are regular I/O pins. |
| RUnLU | I/O, Input | Input control pin to select remote update or local update modes. If MSEL2 = 1, this is a input control pin to select remote update (RUnLU =1) or local update (RUnLU =0) modes. If MSEL2 = 0, the RUnLU pin is a user I/O pin. |

# PLL & Bank Diagram

Figure 2–1 shows the PLL and bank locations for the EP1S20 device.

*Figure 2–1. PLL and Bank Diagram* *Notes (1), (2)*



*Notes for Figure 2–1:*

(1) This is a top view of the silicon die. The die is mounted upside down in flip-chip packages and rightside up in wire-bond packages.

(2) This is a pictoral representation only, to give an idea of placement on the device. Refer to the pinlist and the Quartus II software for exact locations.

## Fast PLL to High-Speed I/O Connections

Table 2–4 shows the number of shows the number of high-speed differential I/O channels that can be driven by each Fast PLL for the EP1S20 device.

*Table 2–4. Fast PLL Connections for the EP1S20 Device*

| Device | Pin Count | FAST PLL Source Location | Number of Rx Channels *(1) (5)* | Number of Tx Channels *(2) (5)* | Number of Overlapped Rx Channels *(3)* | Number of Overlapped Tx Channels *(4)* |
|---|---|---|---|---|---|---|
| EP1S20 | 484 | PLL1 | 5/0 | 6/0 | | |
| | | PLL2 | 5/0 | 6/0 | | |
| | | PLL3 | 5/0 | 6/0 | | |
| | | PLL4 | 5/0 | 6/0 | | |
| | 672 | PLL1 | 0/13 | 0/12 | | |
| | | PLL2 | 0/12 | 0/12 | | |
| | | PLL3 | 0/12 | 0/12 | | |
| | | PLL4 | 0/13 | 0/12 | | |
| | 780 | PLL1 | 17/0 | 17/0 | | |
| | | PLL2 | 16/0 | 16/0 | | |
| | | PLL3 | 16/0 | 16/0 | | |
| | | PLL4 | 17/0 | 17/0 | | |

*Notes for Table 2–4:*

(1) This is the total number of Rx channels that the PLL listed in the "FAST PLL Source location" column can drive.

(2) This is the total number of Tx channels that the PLL listed in the "FAST PLL Source location" column can drive.

(3) This is the number of Rx channels that can be driven by the PLL listed in the "FAST PLL Source location" that could alternatively be driven by the other adjacent FAST PLL.

(4) This is the number of Tx channels that can be driven by the PLL listed in the "FAST PLL Source location" that could alternatively be driven by the other adjacent FAST PLL.

(5) The counts are reported in the format of (high speed channels)/(low speed channels).

# 3. Stratix EP1S25 Device Pin Information

S5V3003-1.0

## Introduction

The following tables contain pin information for the Stratix EP1S25 device, organized into the following sections:

# Pin List

Table 3–1 shows the complete pin list for the EP1S25 device:

*Table 3–1. Pin List for the Stratix EP1S25 Device (Part 1 of 51)*

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | | | |
| IO | DIFFIO_RX38p | | B2 | VREF0B2 | C1 | C1 | | F31 | | | HIGH |
| IO | DIFFIO_RX38n | | B2 | VREF0B2 | D2 | D2 | | F32 | | | HIGH |
| IO | DIFFIO_TX38p | | B2 | VREF0B2 | E3 | E3 | | G28 | | | HIGH |
| IO | DIFFIO_TX38n | | B2 | VREF0B2 | E4 | E4 | | G27 | | | HIGH |
| IO | DIFFIO_RX37p | | B2 | VREF0B2 | E1 | E1 | | G29 | | | HIGH |
| IO | DIFFIO_RX37n | | B2 | VREF0B2 | E2 | E2 | | G30 | | | HIGH |
| IO | DIFFIO_TX37p | | B2 | VREF0B2 | F3 | F3 | F24 | H28 | | | HIGH |
| IO | DIFFIO_TX37n | | B2 | VREF0B2 | F4 | F4 | F23 | H27 | | | HIGH |
| IO | DIFFIO_RX36p | | B2 | VREF0B2 | F1 | F1 | C27 | H30 | | | HIGH |
| IO | DIFFIO_RX36n | | B2 | VREF0B2 | F2 | F2 | C28 | H29 | | | HIGH |
| IO | DIFFIO_TX36p | | B2 | VREF0B2 | G5 | G5 | G23 | J27 | | | HIGH |
| IO | DIFFIO_TX36n | | B2 | VREF0B2 | G6 | G6 | G24 | J28 | | | HIGH |
| IO | DIFFIO_RX35p | | B2 | VREF0B2 | G1 | G1 | D27 | G31 | | | HIGH |
| IO | DIFFIO_RX35n | | B2 | VREF0B2 | G2 | G2 | D28 | G32 | | | HIGH |
| IO | DIFFIO_TX35p | | B2 | VREF0B2 | G3 | G3 | H24 | H25 | | | HIGH |
| IO | DIFFIO_TX35n | | B2 | VREF0B2 | G4 | G4 | H23 | H26 | | | HIGH |
| IO | DIFFIO_RX34p | | B2 | VREF0B2 | H1 | H1 | E27 | H31 | | | HIGH |
| IO | DIFFIO_RX34n | | B2 | VREF0B2 | H2 | H2 | E28 | H32 | | | HIGH |
| IO | DIFFIO_TX34p | | B2 | VREF0B2 | H3 | H3 | H22 | J25 | | | HIGH |
| IO | DIFFIO_TX34n | | B2 | VREF0B2 | H4 | H4 | H21 | J26 | | | HIGH |

*Table 3–1. Pin List for the Stratix EP1S25 Device (Part 2 of 51)*

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| VREF0B2 | | | B2 | VREF0B2 | H8 | H8 | E24 | F27 | | | |
| IO | DIFFIO_RX33p | | B2 | VREF0B2 | | | F25 | J29 | | | HIGH |
| IO | DIFFIO_RX33n | | B2 | VREF0B2 | | | F26 | J30 | | | HIGH |
| IO | DIFFIO_TX33p | | B2 | VREF0B2 | H6 | H6 | J24 | K28 | | | HIGH |
| IO | DIFFIO_TX33n | | B2 | VREF0B2 | H5 | H5 | J23 | K27 | | | HIGH |
| IO | DIFFIO_RX32p | | B2 | VREF0B2 | | | F27 | K30 | | | HIGH |
| IO | DIFFIO_RX32n | | B2 | VREF0B2 | | | F28 | K29 | | | HIGH |
| IO | DIFFIO_TX32p | | B2 | VREF0B2 | J7 | J7 | K23 | K26 | | | HIGH |
| IO | DIFFIO_TX32n | | B2 | VREF0B2 | H7 | H7 | K24 | K25 | | | HIGH |
| IO | DIFFIO_RX31p | | B2 | VREF0B2 | J4 | J4 | G26 | J32 | | | HIGH |
| IO | DIFFIO_RX31n | | B2 | VREF0B2 | J3 | J3 | G25 | J31 | | | HIGH |
| IO | DIFFIO_TX31p | | B2 | VREF0B2 | | | J21 | L27 | | | HIGH |
| IO | DIFFIO_TX31n | | B2 | VREF0B2 | | | J22 | L26 | | | HIGH |
| IO | DIFFIO_RX30p | | B2 | VREF0B2 | J2 | J2 | G27 | K31 | | | HIGH |
| IO | DIFFIO_RX30n | | B2 | VREF0B2 | J1 | J1 | G28 | L32 | | | HIGH |
| IO | DIFFIO_TX30p | | B2 | VREF0B2 | J6 | J6 | K21 | M26 | | | HIGH |
| IO | DIFFIO_TX30n | | B2 | VREF0B2 | J5 | J5 | K22 | M27 | | | HIGH |
| IO | DIFFIO_RX29p/RUP2 | | B2 | VREF0B2 | K4 | K4 | H26 | M28 | | | HIGH |
| IO | DIFFIO_RX29n/RDN2 | | B2 | VREF0B2 | K3 | K3 | H25 | M29 | | | HIGH |
| IO | DIFFIO_TX29p | | B2 | VREF0B2 | | | L22 | M24 | | | HIGH |
| IO | DIFFIO_TX29n | | B2 | VREF0B2 | | | L21 | M25 | | | HIGH |
| IO | DIFFIO_RX28p | | B2 | VREF1B2 | | | H27 | L30 | | | HIGH |

**Table 3–1. Pin List for the Stratix EP1S25 Device (Part 3 of 51)**

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_RX28n | | B2 | VREF1B2 | | | H28 | L31 | | | HIGH |
| IO | DIFFIO_TX28p | | B2 | VREF1B2 | | | L23 | N24 | | | HIGH |
| IO | DIFFIO_TX28n | | B2 | VREF1B2 | | | L24 | N23 | | | HIGH |
| IO | DIFFIO_RX27p | | B2 | VREF1B2 | K2 | K2 | J25 | M31 | | | HIGH |
| IO | DIFFIO_RX27n | | B2 | VREF1B2 | K1 | K1 | J26 | M30 | | | HIGH |
| IO | DIFFIO_TX27p | | B2 | VREF1B2 | K9 | K9 | L20 | N27 | | | HIGH |
| IO | DIFFIO_TX27n | | B2 | VREF1B2 | J8 | J8 | L19 | N28 | | | HIGH |
| IO | DIFFIO_RX26p | | B2 | VREF1B2 | K6 | K6 | J27 | N29 | | | HIGH |
| IO | DIFFIO_RX26n | | B2 | VREF1B2 | K5 | K5 | J28 | N30 | | | HIGH |
| IO | DIFFIO_TX26p | | B2 | VREF1B2 | K8 | K8 | M22 | P23 | | | HIGH |
| IO | DIFFIO_TX26n | | B2 | VREF1B2 | K7 | K7 | M21 | P24 | | | HIGH |
| IO | DIFFIO_RX25p | | B2 | VREF1B2 | L3 | L3 | K26 | N31 | | | HIGH |
| IO | DIFFIO_RX25n | | B2 | VREF1B2 | L2 | L2 | K25 | N32 | | | HIGH |
| IO | DIFFIO_TX25p | | B2 | VREF1B2 | L5 | L5 | M24 | N25 | | | HIGH |
| IO | DIFFIO_TX25n | | B2 | VREF1B2 | L4 | L4 | M23 | N26 | | | HIGH |
| IO | DIFFIO_RX24p | | B2 | VREF1B2 | | | K27 | P29 | | | HIGH |
| IO | DIFFIO_RX24n | | B2 | VREF1B2 | | | K28 | P30 | | | HIGH |
| IO | DIFFIO_TX24p | | B2 | VREF1B2 | L7 | L7 | M20 | P28 | | | HIGH |
| IO | DIFFIO_TX24n | | B2 | VREF1B2 | L6 | L6 | M19 | P27 | | | HIGH |
| VREF1B2 | | | B2 | VREF1B2 | L8 | L8 | K20 | L25 | | | |
| IO | DIFFIO_RX23p | | B2 | VREF1B2 | M6 | M6 | L25 | P31 | | | HIGH |
| IO | DIFFIO_RX23n | | B2 | VREF1B2 | M7 | M7 | L26 | P32 | | | HIGH |

**Table 3–1. Pin List for the Stratix EP1S25 Device (Part 4 of 51)**

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_TX23p | | B2 | VREF1B2 | | | N26 | R28 | | | HIGH |
| IO | DIFFIO_TX23n | | B2 | VREF1B2 | | | N25 | R27 | | | HIGH |
| IO | DIFFIO_RX22p | | B2 | VREF1B2 | M4 | M4 | L27 | R32 | | | HIGH |
| IO | DIFFIO_RX22n | | B2 | VREF1B2 | M5 | M5 | L28 | R31 | | | HIGH |
| IO | DIFFIO_TX22p | | B2 | VREF1B2 | | | N24 | P25 | | | HIGH |
| IO | DIFFIO_TX22n | | B2 | VREF1B2 | | | N23 | P26 | | | HIGH |
| IO | DIFFIO_RX21p | | B2 | VREF1B2 | N6 | N6 | M25 | R30 | | | HIGH |
| IO | DIFFIO_RX21n | | B2 | VREF1B2 | N7 | N7 | M26 | R29 | | | HIGH |
| IO | DIFFIO_TX21p | | B2 | VREF1B2 | M8 | M8 | N22 | R23 | | | HIGH |
| IO | DIFFIO_TX21n | | B2 | VREF1B2 | M9 | M9 | N21 | R24 | | | HIGH |
| IO | DIFFIO_RX20p | | B2 | VREF1B2 | | | M27 | T32 | | | HIGH |
| IO | DIFFIO_RX20n | | B2 | VREF1B2 | | | N28 | T31 | | | HIGH |
| IO | DIFFIO_TX20p | | B2 | VREF1B2 | P8 | P8 | N20 | R25 | | | HIGH |
| IO | DIFFIO_TX20n | | B2 | VREF1B2 | N8 | N8 | N19 | R26 | | | HIGH |
| CLK0n | | | B2 | VREF1B2 | N2 | N2 | N27 | T30 | | | |
| CLK0p | | | B2 | VREF1B2 | N3 | N3 | P27 | T29 | | | |
| IO | CLK1n | | B2 | VREF1B2 | | | P26 | T28 | | | |
| CLK1p | | | B2 | VREF1B2 | M1 | M1 | P25 | T27 | | | |
| VCCINT | | | | | | | VCC | VCC | | | |
| VCCA_PLL1 | | | | | M3 | M3 | P23 | T25 | | | |
| GND | | | | | | | GND | GND | | | |
| GNDA_PLL1 | | | | | N5 | N5 | P24 | T26 | | | |

**Table 3–1. Pin List for the Stratix EP1S25 Device (Part 5 of 51)**

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | | | |
| VCCG_PLL1 | | | | | M2 | M2 | P21 | R22 | | | |
| GNDG_PLL1 | | | | | N4 | N4 | P22 | T22 | | | |
| VCCINT | | | | | | | | | | | |
| VCCA_PLL2 | | | | | P5 | P5 | R23 | U25 | | | |
| GND | | | | | | | | | | | |
| GNDA_PLL2 | | | | | P3 | P3 | R24 | U26 | | | |
| VCCG_PLL2 | | | | | P4 | P4 | R21 | U24 | | | |
| GNDG_PLL2 | | | | | P2 | P2 | R22 | T24 | | | |
| CLK2p | | | B1 | VREF0B1 | R1 | R1 | R27 | U31 | | | |
| CLK2n | | | B1 | VREF0B1 | R2 | R2 | T27 | U32 | | | |
| CLK3p | | | B1 | VREF0B1 | R3 | R3 | R25 | U29 | | | |
| IO | CLK3n | | B1 | VREF0B1 | | | R26 | U30 | | | |
| IO | DIFFIO_RX19p | | B1 | VREF0B1 | | | T28 | U28 | | | HIGH |
| IO | DIFFIO_RX19n | | B1 | VREF0B1 | | | U27 | U27 | | | HIGH |
| IO | DIFFIO_TX19p | | B1 | VREF0B1 | P6 | P6 | T21 | V26 | | | HIGH |
| IO | DIFFIO_TX19n | | B1 | VREF0B1 | P7 | P7 | T22 | V25 | | | HIGH |
| IO | DIFFIO_RX18p | | B1 | VREF0B1 | R6 | R6 | U26 | V32 | | | HIGH |
| IO | DIFFIO_RX18n | | B1 | VREF0B1 | R7 | R7 | U25 | V31 | | | HIGH |
| IO | DIFFIO_TX18p | | B1 | VREF0B1 | R8 | R8 | T19 | V28 | | | HIGH |
| IO | DIFFIO_TX18n | | B1 | VREF0B1 | R9 | R9 | T20 | V27 | | | HIGH |
| IO | DIFFIO_RX17p | | B1 | VREF0B1 | R4 | R4 | V27 | V30 | | | HIGH |
| IO | DIFFIO_RX17n | | B1 | VREF0B1 | R5 | R5 | V28 | V29 | | | HIGH |

*Table 3–1. Pin List for the Stratix EP1S25 Device (Part 6 of 51)*

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | | | |
| IO | DIFFIO_TX17p | | B1 | VREF0B1 | | | T23 | W25 | | | HIGH |
| IO | DIFFIO_TX17n | | B1 | VREF0B1 | | | T24 | W26 | | | HIGH |
| VREF0B1 | | | B1 | VREF0B1 | T8 | T8 | R19 | V21 | | | |
| IO | DIFFIO_RX16p | | B1 | VREF0B1 | T3 | T3 | V26 | W32 | | | HIGH |
| IO | DIFFIO_RX16n | | B1 | VREF0B1 | T2 | T2 | V25 | W31 | | | HIGH |
| IO | DIFFIO_TX16p | | B1 | VREF0B1 | | | T26 | W27 | | | HIGH |
| IO | DIFFIO_TX16n | | B1 | VREF0B1 | | | T25 | W28 | | | HIGH |
| IO | DIFFIO_RX15p | | B1 | VREF0B1 | | | W28 | W30 | | | HIGH |
| IO | DIFFIO_RX15n | | B1 | VREF0B1 | | | W27 | W29 | | | HIGH |
| IO | DIFFIO_TX15p | | B1 | VREF0B1 | T7 | T7 | U19 | V24 | | | HIGH |
| IO | DIFFIO_TX15n | | B1 | VREF0B1 | T6 | T6 | U20 | V23 | | | HIGH |
| IO | DIFFIO_RX14p | | B1 | VREF0B1 | T5 | T5 | W26 | Y32 | | | HIGH |
| IO | DIFFIO_RX14n | | B1 | VREF0B1 | T4 | T4 | W25 | Y31 | | | HIGH |
| IO | DIFFIO_TX14p | | B1 | VREF0B1 | U6 | U6 | U24 | Y26 | | | HIGH |
| IO | DIFFIO_TX14n | | B1 | VREF0B1 | U5 | U5 | U23 | Y25 | | | HIGH |
| IO | DIFFIO_RX13p | | B1 | VREF1B1 | U2 | U2 | Y28 | Y30 | | | HIGH |
| IO | DIFFIO_RX13n | | B1 | VREF1B1 | U1 | U1 | Y27 | Y29 | | | HIGH |
| IO | DIFFIO_TX13p | | B1 | VREF1B1 | U8 | U8 | U21 | Y28 | | | HIGH |
| IO | DIFFIO_TX13n | | B1 | VREF1B1 | U7 | U7 | U22 | Y27 | | | HIGH |
| IO | DIFFIO_RX12p | | B1 | VREF1B1 | U4 | U4 | Y26 | AA31 | | | HIGH |
| IO | DIFFIO_RX12n | | B1 | VREF1B1 | U3 | U3 | Y25 | AA30 | | | HIGH |
| IO | DIFFIO_TX12p | | B1 | VREF1B1 | U9 | U9 | V19 | W23 | | | HIGH |

*Table 3–1. Pin List for the Stratix EP1S25 Device (Part 7 of 51)*

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | | | |
| IO | DIFFIO_TX12n | | B1 | VREF1B1 | V8 | V8 | V20 | W24 | | | HIGH |
| IO | DIFFIO_RX11p | | B1 | VREF1B1 | | | AA28 | AB31 | | | HIGH |
| IO | DIFFIO_RX11n | | B1 | VREF1B1 | | | AA27 | AB30 | | | HIGH |
| IO | DIFFIO_TX11p | | B1 | VREF1B1 | | | V24 | Y23 | | | HIGH |
| IO | DIFFIO_TX11n | | B1 | VREF1B1 | | | V23 | Y24 | | | HIGH |
| IO | DIFFIO_RX10p/RUP1 | | B1 | VREF1B1 | V6 | V6 | AA25 | AA28 | | | HIGH |
| IO | DIFFIO_RX10n/RDN1 | | B1 | VREF1B1 | V5 | V5 | AA26 | AA29 | | | HIGH |
| IO | DIFFIO_TX10p | | B1 | VREF1B1 | | | V22 | AA25 | | | HIGH |
| IO | DIFFIO_TX10n | | B1 | VREF1B1 | | | V21 | AA24 | | | HIGH |
| VREF1B1 | | | B1 | VREF1B1 | V7 | V7 | W20 | AA23 | | | |
| IO | DIFFIO_RX9p | | B1 | VREF1B1 | | | AB28 | AB32 | | | HIGH |
| IO | DIFFIO_RX9n | | B1 | VREF1B1 | | | AB27 | AC31 | | | HIGH |
| IO | DIFFIO_TX9p | | B1 | VREF1B1 | | | W23 | AA27 | | | HIGH |
| IO | DIFFIO_TX9n | | B1 | VREF1B1 | | | W24 | AA26 | | | HIGH |
| IO | DIFFIO_RX8p | | B1 | VREF1B1 | V1 | V1 | AB26 | AD32 | | | HIGH |
| IO | DIFFIO_RX8n | | B1 | VREF1B1 | V2 | V2 | AB25 | AD31 | | | HIGH |
| IO | DIFFIO_TX8p | | B1 | VREF1B1 | W5 | W5 | W21 | AB27 | | | HIGH |
| IO | DIFFIO_TX8n | | B1 | VREF1B1 | W6 | W6 | W22 | AB26 | | | HIGH |
| IO | DIFFIO_RX7p | | B1 | VREF1B1 | V3 | V3 | AC28 | AC29 | | | HIGH |
| IO | DIFFIO_RX7n | | B1 | VREF1B1 | V4 | V4 | AC27 | AC30 | | | HIGH |
| IO | DIFFIO_TX7p | | B1 | VREF1B1 | W7 | W7 | Y21 | AC25 | | | HIGH |
| IO | DIFFIO_TX7n | | B1 | VREF1B1 | W8 | W8 | Y22 | AC26 | | | HIGH |

*Table 3–1. Pin List for the Stratix EP1S25 Device (Part 8 of 51)*

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_RX6p | | B1 | VREF2B1 | W1 | W1 | AD28 | AD30 | | | HIGH |
| IO | DIFFIO_RX6n | | B1 | VREF2B1 | W2 | W2 | AD27 | AD29 | | | HIGH |
| IO | DIFFIO_TX6p | | B1 | VREF2B1 | | | Y24 | AC27 | | | HIGH |
| IO | DIFFIO_TX6n | | B1 | VREF2B1 | | | Y23 | AC28 | | | HIGH |
| IO | DIFFIO_RX5p | | B1 | VREF2B1 | | | AE28 | AE32 | | | HIGH |
| IO | DIFFIO_RX5n | | B1 | VREF2B1 | | | AE27 | AE31 | | | HIGH |
| IO | DIFFIO_TX5p | | B1 | VREF2B1 | Y3 | Y3 | AA23 | AD28 | | | HIGH |
| IO | DIFFIO_TX5n | | B1 | VREF2B1 | Y4 | Y4 | AA24 | AD27 | | | HIGH |
| IO | DIFFIO_RX4p | | B1 | VREF2B1 | W3 | W3 | AF28 | AE30 | | | HIGH |
| IO | DIFFIO_RX4n | | B1 | VREF2B1 | W4 | W4 | AF27 | AE29 | | | HIGH |
| IO | DIFFIO_TX4p | | B1 | VREF2B1 | Y6 | Y6 | AA21 | AD26 | | | HIGH |
| IO | DIFFIO_TX4n | | B1 | VREF2B1 | Y5 | Y5 | AA22 | AD25 | | | HIGH |
| IO | DIFFIO_RX3p | | B1 | VREF2B1 | Y2 | Y2 | | AF32 | | | HIGH |
| IO | DIFFIO_RX3n | | B1 | VREF2B1 | Y1 | Y1 | | AF31 | | | HIGH |
| IO | DIFFIO_TX3p | | B1 | VREF2B1 | AA6 | AA6 | AB23 | AE28 | | | HIGH |
| IO | DIFFIO_TX3n | | B1 | VREF2B1 | AA5 | AA5 | AB24 | AE27 | | | HIGH |
| VREF2B1 | | | B1 | VREF2B1 | Y7 | Y7 | AE26 | AB25 | | | |
| IO | DIFFIO_RX2p | | B1 | VREF2B1 | AA2 | AA2 | | AF30 | | | HIGH |
| IO | DIFFIO_RX2n | | B1 | VREF2B1 | AA1 | AA1 | | AF29 | | | HIGH |
| IO | DIFFIO_TX2p | | B1 | VREF2B1 | AA4 | AA4 | | AE25 | | | HIGH |
| IO | DIFFIO_TX2n | | B1 | VREF2B1 | AA3 | AA3 | | AE26 | | | HIGH |
| IO | DIFFIO_RX1p | | B1 | VREF2B1 | AB2 | AB2 | | AG31 | | | HIGH |

*Table 3–1. Pin List for the Stratix EP1S25 Device (Part 9 of 51)*

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_RX1n | | B1 | VREF2B1 | AB1 | AB1 | | AG32 | | | HIGH |
| IO | DIFFIO_TX1p | | B1 | VREF2B1 | AB4 | AB4 | | AF27 | | | HIGH |
| IO | DIFFIO_TX1n | | B1 | VREF2B1 | AB3 | AB3 | | AF28 | | | HIGH |
| IO | DIFFIO_RX0p | | B1 | VREF2B1 | AC2 | AC2 | | AG30 | | | HIGH |
| IO | DIFFIO_RX0n | | B1 | VREF2B1 | AD1 | AD1 | | AG29 | | | HIGH |
| IO | DIFFIO_TX0p | | B1 | VREF2B1 | AC4 | AC4 | | AF26 | | | HIGH |
| IO | DIFFIO_TX0n | | B1 | VREF2B1 | AC3 | AC3 | | AF25 | | | HIGH |
| IO | | | B8 | VREF0B8 | | | AC24 | AB24 | | | |
| IO | DQ9B7 | | B8 | VREF0B8 | AD5 | AD5 | AG26 | AH28 | DQ3B15 | DQ1B31 | |
| IO | | | B8 | VREF0B8 | AC5 | AC5 | AC23 | AC24 | | | |
| IO | DQ9B6 | | B8 | VREF0B8 | AD2 | AD2 | AH26 | AK30 | DQ3B14 | DQ1B30 | |
| IO | DQ9B5 | | B8 | VREF0B8 | AE2 | AE2 | AG25 | AJ28 | DQ3B13 | DQ1B29 | |
| IO | DQ9B4 | | B8 | VREF0B8 | AD3 | AD3 | AH25 | AJ29 | DQ3B12 | DQ1B28 | |
| IO | | | B8 | VREF0B8 | | | AB22 | AC23 | | | |
| IO | DQ9B3 | | B8 | VREF0B8 | AE4 | AE4 | AF25 | AK29 | DQ3B11 | DQ1B27 | |
| IO | | | B8 | VREF0B8 | | | | AD24 | | | |
| IO | DQS9B | | B8 | VREF0B8 | AD4 | AD4 | AF24 | AK28 | | | |
| IO | DQ9B2 | | B8 | VREF0B8 | AE3 | AE3 | AG24 | AL30 | DQ3B10 | DQ1B26 | |
| IO | | | B8 | VREF0B8 | | | AE25 | AD23 | | | |
| IO | DQ9B1 | | B8 | VREF0B8 | AB5 | AB5 | AE24 | AL29 | DQ3B9 | DQ1B25 | |
| IO | | | B8 | VREF0B8 | | | | AE24 | | | |
| IO | DQ9B0 | | B8 | VREF0B8 | AF3 | AF3 | AH24 | AM29 | DQ3B8 | DQ1B24 | |

*Table 3–1. Pin List for the Stratix EP1S25 Device (Part 10 of 51)*

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | | | |
| IO | | | B8 | VREF0B8 | AB6 | AB6 | AD24 | AE23 | | | |
| IO | | | B8 | VREF0B8 | AC6 | AC6 | | AF24 | | | |
| IO | DQ8B7 | | B8 | VREF0B8 | AC7 | AC7 | AG23 | AH26 | DQ3B7 | DQ1B23 | |
| VREF0B8 | | | B8 | VREF0B8 | AE5 | AE5 | AD22 | AH27 | | | |
| IO | DQ8B6 | | B8 | VREF0B8 | AD6 | AD6 | AD23 | AJ27 | DQ3B6 | DQ1B22 | |
| IO | DQ8B5 | | B8 | VREF0B8 | AE7 | AE7 | AF23 | AL28 | DQ3B5 | DQ1B21 | |
| IO | | | B8 | VREF0B8 | AF5 | AF5 | AB21 | AC22 | | | |
| IO | DQ8B4 | | B8 | VREF0B8 | AB7 | AB7 | AH23 | AK27 | DQ3B4 | DQ1B20 | |
| IO | DQ8B3 | | B8 | VREF0B8 | AD7 | AD7 | AE22 | AJ26 | DQ3B3 | DQ1B19 | |
| IO | | | B8 | VREF0B8 | | | | AG24 | | | |
| IO | DQS8B | | B8 | VREF0B8 | AE6 | AE6 | AE23 | AL27 | DQS3B | | |
| IO | DQ8B2 | | B8 | VREF0B8 | AA7 | AA7 | AF22 | AM27 | DQ3B2 | DQ1B18 | |
| IO | | | B8 | VREF0B8 | | | AB20 | AB22 | | | |
| IO | DQ8B1 | | B8 | VREF0B8 | AF7 | AF7 | AH22 | AM28 | DQ3B1 | DQ1B17 | |
| IO | DQ8B0 | | B8 | VREF0B8 | AF6 | AF6 | AG22 | AK26 | DQ3B0 | DQ1B16 | |
| IO | | | B8 | VREF0B8 | | | | AF23 | | | |
| IO | | | B8 | VREF1B8 | | | Y20 | AA21 | | | |
| IO | DQ7B7 | | B8 | VREF1B8 | AC8 | AC8 | AD21 | AH24 | DQ2B15 | DQ1B15 | |
| IO | | | B8 | VREF1B8 | | | | AB21 | | | |
| IO | DQ7B6 | | B8 | VREF1B8 | AB8 | AB8 | AE21 | AJ24 | DQ2B14 | DQ1B14 | |
| IO | DQ7B5 | | B8 | VREF1B8 | AD8 | AD8 | AG21 | AJ25 | DQ2B13 | DQ1B13 | |
| IO | | | B8 | VREF1B8 | | | AC22 | AD22 | | | |

**Table 3–1. Pin List for the Stratix EP1S25 Device (Part 11 of 51)**

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | | | |
| IO | DQ7B4 | | B8 | VREF1B8 | AE8 | AE8 | AF21 | AK25 | DQ2B12 | DQ1B12 | |
| IO | DQ7B3 | | B8 | VREF1B8 | AF8 | AF8 | AE20 | AL25 | DQ2B11 | DQ1B11 | |
| IO | | | B8 | VREF1B8 | | | | AC21 | | | |
| IO | DQS7B | | B8 | VREF1B8 | Y9 | Y9 | AG20 | AL26 | | DQS1B | |
| IO | DQ7B2 | | B8 | VREF1B8 | Y8 | Y8 | AF20 | AK24 | DQ2B10 | DQ1B10 | |
| IO | | | B8 | VREF1B8 | | | AC20 | AG23 | | | |
| IO | DQ7B1 | | B8 | VREF1B8 | W9 | W9 | AH21 | AM25 | DQ2B9 | DQ1B9 | |
| IO | | | B8 | VREF1B8 | | | | AD21 | | | |
| IO | DQ7B0 | | B8 | VREF1B8 | AA8 | AA8 | AH20 | AM26 | DQ2B8 | DQ1B8 | |
| IO | DQ6B7 | | B8 | VREF1B8 | AC9 | AC9 | AE19 | AJ23 | DQ2B7 | DQ1B7 | |
| IO | FCLK3 | | B8 | VREF1B8 | AD9 | AD9 | AC21 | AE21 | | | |
| IO | FCLK2 | | B8 | VREF1B8 | AB9 | AB9 | AC19 | AF21 | | | |
| VREF1B8 | | | B8 | VREF1B8 | AE9 | AE9 | AD20 | AH25 | | | |
| IO | DQ6B6 | | B8 | VREF1B8 | AF9 | AF9 | AD19 | AL24 | DQ2B6 | DQ1B6 | |
| IO | DQ6B5 | | B8 | VREF1B8 | AD10 | AD10 | AF19 | AH22 | DQ2B5 | DQ1B5 | |
| IO | | | B8 | VREF1B8 | | | | AF22 | | | |
| IO | DQ6B4 | | B8 | VREF1B8 | AE10 | AE10 | AG19 | AM24 | DQ2B4 | DQ1B4 | |
| IO | | PGM2 | B8 | VREF1B8 | AA9 | AA9 | AB19 | AA20 | | | |
| IO | DQ6B3 | | B8 | VREF1B8 | AC10 | AC10 | AH19 | AK23 | DQ2B3 | DQ1B3 | |
| IO | | | B8 | VREF1B8 | | | | AB20 | | | |
| IO | DQS6B | | B8 | VREF1B8 | Y10 | Y10 | AF18 | AJ22 | DQS2B | | |
| IO | DQ6B2 | | B8 | VREF1B8 | AA10 | AA10 | AD18 | AL23 | DQ2B2 | DQ1B2 | |

*Table 3–1. Pin List for the Stratix EP1S25 Device (Part 12 of 51)*

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | | | |
| IO | | | B8 | VREF1B8 | W10 | W10 | AA20 | AF20 | | | |
| IO | DQ6B1 | | B8 | VREF1B8 | AB10 | AB10 | AE18 | AK22 | DQ2B1 | DQ1B1 | |
| IO | DQ6B0 | | B8 | VREF1B8 | AF10 | AF10 | AG18 | AL22 | DQ2B0 | DQ1B0 | |
| IO | RDN8 | | B8 | VREF1B8 | AB11 | AB11 | Y19 | AC20 | | | |
| IO | RUP8 | | B8 | VREF1B8 | AE11 | AE11 | W19 | AH19 | | | |
| IO | DQ5B7 | | B8 | VREF1B8 | | | AF17 | AM22 | | | |
| IO | | | B8 | VREF1B8 | | | | AG22 | | | |
| IO | DQ5B6 | | B8 | VREF1B8 | | | AG17 | AJ21 | | | |
| IO | DQ5B5 | | B8 | VREF1B8 | | | AE17 | AK21 | | | |
| IO | | | B8 | VREF2B8 | | | | AB19 | | | |
| IO | DQ5B4 | | B8 | VREF2B8 | | | AD17 | AL21 | | | |
| IO | | RDYnBSY | B8 | VREF2B8 | AC11 | AC11 | AA19 | AA19 | | | |
| IO | DQ5B3 | | B8 | VREF2B8 | | | AG16 | AH20 | | | |
| IO | | | B8 | VREF2B8 | | | AB18 | AD20 | | | |
| IO | DQS5B | | B8 | VREF2B8 | | | AH16 | AJ20 | | | |
| IO | DQ5B2 | | B8 | VREF2B8 | | | AD16 | AK20 | | | |
| IO | | nCS | B8 | VREF2B8 | Y11 | Y11 | Y18 | AC19 | | | |
| IO | DQ5B1 | | B8 | VREF2B8 | | | AF16 | AL20 | | | |
| IO | DQ5B0 | | B8 | VREF2B8 | | | AE16 | AM20 | | | |
| IO | | | B8 | VREF2B8 | AD11 | AD11 | | AG21 | | | |
| IO | | | B8 | VREF2B8 | | | | AG20 | | | |
| IO | | | B8 | VREF2B8 | | | V18 | AE20 | | | |

*Table 3–1. Pin List for the Stratix EP1S25 Device (Part 13 of 51)*

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | | | |
| IO | | | B8 | VREF2B8 | | | W18 | AD19 | | | |
| IO | | CS | B8 | VREF2B8 | AA11 | AA11 | AA18 | AG19 | | | |
| IO | | | B8 | VREF2B8 | | | | AJ18 | | | |
| IO | | | B8 | VREF2B8 | | | | AH18 | | | |
| IO | | | B8 | VREF2B8 | | | | AK18 | | | |
| VREF2B8 | | | B8 | VREF2B8 | W11 | W11 | AH18 | AH23 | | | |
| IO | CLK5n | | B8 | VREF2B8 | AD12 | AD12 | Y17 | AJ19 | | | |
| CLK5p | | | B8 | VREF2B8 | AC12 | AC12 | AA17 | AK19 | | | |
| IO | CLK4n | | B8 | VREF2B8 | AF12 | AF12 | AB17 | AL19 | | | |
| CLK4p | | | B8 | VREF2B8 | AE12 | AE12 | AC17 | AM19 | | | |
| PLL_ENA | | PLL_ENA | B8 | VREF2B8 | W12 | W12 | AC18 | AF19 | | | |
| MSEL0 | | MSEL0 | B8 | VREF2B8 | Y12 | Y12 | AC16 | AG18 | | | |
| MSEL1 | | MSEL1 | B8 | VREF2B8 | Y13 | Y13 | W17 | AE18 | | | |
| MSEL2 | | MSEL2 | B8 | VREF2B8 | W13 | W13 | AB15 | AE19 | | | |
| IO | PLL6_OUT3n | | B12 | VREF2B8 | | | Y16 | AM18 | | | |
| IO | PLL6_OUT3p | | B12 | VREF2B8 | | | W16 | AL18 | | | |
| IO | PLL6_OUT2n | | B12 | VREF2B8 | | | AG15 | AK17 | | | |
| IO | PLL6_OUT2p | | B12 | VREF2B8 | | | AF15 | AJ17 | | | |
| IO | PLL6_FBn | | B11 | VREF2B8 | AB12 | AB12 | AA15 | AM17 | | | |
| IO | PLL6_FBp | | B11 | VREF2B8 | AA12 | AA12 | AA14 | AL17 | | | |
| IO | PLL6_OUT1n | | B11 | VREF2B8 | AB14 | AB14 | W15 | AK16 | | | |
| IO | PLL6_OUT1p | | B11 | VREF2B8 | AA14 | AA14 | W14 | AJ16 | | | |

*Table 3–1. Pin List for the Stratix EP1S25 Device (Part 14 of 51)*

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | PLL6_OUT0n | | B11 | VREF2B8 | AB13 | AB13 | AE15 | AM16 | | | |
| IO | PLL6_OUT0p | | B11 | VREF2B8 | AA13 | AA13 | AD15 | AL16 | | | |
| VCC_PLL6_ OUTB | | | B12 | | | | AB16 | AB17 | | | |
| VCC_PLL6_ OUTB | | | B12 | | | | | | | | |
| VCC_PLL6_ OUTA | | | B11 | | | | AC14 | AE17 | | | |
| VCC_PLL6_ OUTA | | | B11 | | AE13 | AE13 | | | | | |
| VCCINT | | | | | | | | | | | |
| VCCA_PLL6 | | | | | AD14 | AD14 | AG14 | AG17 | | | |
| GND | | | | | | | | | | | |
| GNDA_PLL6 | | | | | AC14 | AC14 | AF14 | AH17 | | | |
| GNDA_PLL6 | | | | | | | | | | | |
| VCCG_PLL6 | | | | | AD13 | AD13 | AA13 | AD16 | | | |
| GNDG_PLL6 | | | | | AE14 | AE14 | AB14 | AB16 | | | |
| CLK7p | | | B7 | VREF0B7 | AE15 | AE15 | W13 | AM15 | | | |
| IO | CLK7n | | B7 | VREF0B7 | | | Y13 | AL15 | | | |
| CLK6p | | | B7 | VREF0B7 | AF15 | AF15 | AD14 | AK15 | | | |
| IO | CLK6n | | B7 | VREF0B7 | | | AE14 | AJ15 | | | |
| nCE | | nCE | B7 | VREF0B7 | Y14 | Y14 | AB13 | AF18 | | | |
| nCEO | | nCEO | B7 | VREF0B7 | W14 | W14 | AC13 | AH15 | | | |

*Table 3–1. Pin List for the Stratix EP1S25 Device (Part 15 of 51)*

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | | | |
| IO | | | B7 | VREF0B7 | | | | AA18 | | | |
| IO | | | B7 | VREF0B7 | | | | AB15 | | | |
| IO | | PGM0 | B7 | VREF0B7 | W15 | W15 | W12 | AD18 | | | |
| nIO_PULLUP | | nIO_PULLUP | B7 | VREF0B7 | AA15 | AA15 | Y12 | AF15 | | | |
| VCCSEL | | VCCSEL | B7 | VREF0B7 | Y15 | Y15 | AA12 | AJ14 | | | |
| PORSEL | | PORSEL | B7 | VREF0B7 | W16 | W16 | AC12 | AG15 | | | |
| IO | | | B7 | VREF0B7 | | | | AA15 | | | |
| IO | | | B7 | VREF0B7 | | | | AD15 | | | |
| IO | | | B7 | VREF0B7 | | | | AC15 | | | |
| IO | | | B7 | VREF0B7 | | | | AK14 | | | |
| IO | | | B7 | VREF0B7 | | | | AC18 | | | |
| IO | | | B7 | VREF0B7 | | | | AL14 | | | |
| VREF0B7 | | | B7 | VREF0B7 | AB15 | AB15 | AD11 | AH12 | | | |
| IO | | INIT_DONE | B7 | VREF0B7 | AC15 | AC15 | W11 | AE15 | | | |
| IO | | | B7 | VREF0B7 | | | V11 | AB14 | | | |
| IO | DQ4B7 | | B7 | VREF0B7 | | | AD13 | AL13 | | | |
| IO | DQ4B6 | | B7 | VREF0B7 | | | AE13 | AM13 | | | |
| IO | | nRS | B7 | VREF0B7 | Y16 | Y16 | AC11 | AB18 | | | |
| IO | DQ4B5 | | B7 | VREF0B7 | | | AF13 | AH13 | | | |
| IO | | | B7 | VREF0B7 | | | Y11 | AA14 | | | |
| IO | DQ4B4 | | B7 | VREF0B7 | | | AD12 | AJ13 | | | |
| IO | DQ4B3 | | B7 | VREF0B7 | | | AG13 | AK13 | | | |

**Table 3–1. Pin List for the Stratix EP1S25 Device (Part 16 of 51)**

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | | | |
| IO | | RUnLU | B7 | VREF0B7 | AD15 | AD15 | W10 | AF14 | | | |
| IO | DQS4B | | B7 | VREF0B7 | | | AH13 | AJ12 | | | |
| IO | | | B7 | VREF0B7 | AA16 | AA16 | AB12 | AE14 | | | |
| IO | DQ4B2 | | B7 | VREF1B7 | | | AE12 | AK12 | | | |
| IO | DQ4B1 | | B7 | VREF1B7 | | | AF12 | AL12 | | | |
| IO | | PGM1 | B7 | VREF1B7 | AC16 | AC16 | AA11 | AG14 | | | |
| IO | DQ4B0 | | B7 | VREF1B7 | | | AG12 | AM11 | | | |
| IO | RDN7 | | B7 | VREF1B7 | AB16 | AB16 | AC10 | AC14 | | | |
| IO | RUP7 | | B7 | VREF1B7 | AD16 | AD16 | AB11 | AF13 | | | |
| IO | DQ3B7 | | B7 | VREF1B7 | W17 | W17 | AG11 | AL10 | DQ1B15 | DQ0B31 | |
| IO | | | B7 | VREF1B7 | | | | AD14 | | | |
| IO | DQ3B6 | | B7 | VREF1B7 | AE16 | AE16 | AH11 | AK11 | DQ1B14 | DQ0B30 | |
| IO | DQ3B5 | | B7 | VREF1B7 | Y17 | Y17 | AE11 | AL11 | DQ1B13 | DQ0B29 | |
| IO | DEV_CLRn | | B7 | VREF1B7 | AF17 | AF17 | AC9 | AH14 | | | |
| IO | DQ3B4 | | B7 | VREF1B7 | AA17 | AA17 | AF11 | AK10 | DQ1B12 | DQ0B28 | |
| IO | DQ3B3 | | B7 | VREF1B7 | Y18 | Y18 | AE10 | AM9 | DQ1B11 | DQ0B27 | |
| IO | | | B7 | VREF1B7 | | | | AB13 | | | |
| IO | DQS3B | | B7 | VREF1B7 | AE17 | AE17 | AG10 | AJ11 | DQS1B | | |
| IO | | | B7 | VREF1B7 | | | Y10 | AG13 | | | |
| IO | DQ3B2 | | B7 | VREF1B7 | W18 | W18 | AH10 | AL9 | DQ1B10 | DQ0B26 | |
| IO | DQ3B1 | | B7 | VREF1B7 | AB17 | AB17 | AF10 | AJ10 | DQ1B9 | DQ0B25 | |
| VREF1B7 | | | B7 | VREF1B7 | AB18 | AB18 | AD9 | AH10 | | | |

Table 3–1. Pin List for the Stratix EP1S25 Device (Part 17 of 51)

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DQ3B0 | | B7 | VREF1B7 | AA18 | AA18 | AD10 | AH11 | DQ1B8 | DQ0B24 | |
| IO | | | B7 | VREF1B7 | Y19 | Y19 | | AC13 | | | |
| IO | | | B7 | VREF1B7 | | | AA10 | AE13 | | | |
| IO | DQ2B7 | | B7 | VREF1B7 | AF18 | AF18 | AG9 | AL8 | DQ1B7 | DQ0B23 | |
| IO | FCLK5 | | B7 | VREF1B7 | AC17 | AC17 | AC8 | AM14 | | | |
| IO | FCLK4 | | B7 | VREF1B7 | AD17 | AD17 | AB10 | AF12 | | | |
| IO | DQ2B6 | | B7 | VREF1B7 | AE18 | AE18 | AF9 | AJ9 | DQ1B6 | DQ0B22 | |
| IO | DQ2B5 | | B7 | VREF1B7 | AF19 | AF19 | AE9 | AK9 | DQ1B5 | DQ0B21 | |
| IO | | | B7 | VREF1B7 | | | AB9 | AD13 | | | |
| IO | DQ2B4 | | B7 | VREF1B7 | Y20 | Y20 | AH8 | AM8 | DQ1B4 | DQ0B20 | |
| IO | DQ2B3 | | B7 | VREF1B7 | AA19 | AA19 | AH9 | AH9 | DQ1B3 | DQ0B19 | |
| IO | | | B7 | VREF1B7 | AD18 | AD18 | | AG12 | | | |
| IO | DQS2B | | B7 | VREF2B7 | AB19 | AB19 | AE8 | AK8 | | DQS0B | |
| IO | DQ2B2 | | B7 | VREF2B7 | AD19 | AD19 | AD8 | AM7 | DQ1B2 | DQ0B18 | |
| IO | | | B7 | VREF2B7 | AC18 | AC18 | AA9 | AE12 | | | |
| IO | DQ2B1 | | B7 | VREF2B7 | AC19 | AC19 | AF8 | AJ8 | DQ1B1 | DQ0B17 | |
| IO | DQ2B0 | | B7 | VREF2B7 | AE19 | AE19 | AG8 | AL7 | DQ1B0 | DQ0B16 | |
| IO | | | B7 | VREF2B7 | | | | AC12 | | | |
| IO | | | B7 | VREF2B7 | AF20 | AF20 | AB8 | AA12 | | | |
| IO | DQ1B7 | | B7 | VREF2B7 | AE20 | AE20 | AF6 | AL6 | DQ0B15 | DQ0B15 | |
| IO | DQ1B6 | | B7 | VREF2B7 | AA20 | AA20 | AG7 | AM6 | DQ0B14 | DQ0B14 | |
| IO | | | B7 | VREF2B7 | | | AC7 | AD12 | | | |

**Table 3–1. Pin List for the Stratix EP1S25 Device (Part 18 of 51)**

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | | | |
| IO | DQ1B5 | | B7 | VREF2B7 | AB20 | AB20 | AH7 | AJ7 | DQ0B13 | DQ0B13 | |
| IO | DQ1B4 | | B7 | VREF2B7 | AF21 | AF21 | AF7 | AM5 | DQ0B12 | DQ0B12 | |
| IO | | | B7 | VREF2B7 | | | | AB11 | | | |
| IO | DQ1B3 | | B7 | VREF2B7 | AC20 | AC20 | AD6 | AK7 | DQ0B11 | DQ0B11 | |
| IO | DQS1B | | B7 | VREF2B7 | AA21 | AA21 | AE7 | AH7 | DQS0B | | |
| IO | | | B7 | VREF2B7 | AB21 | AB21 | AD5 | AE11 | | | |
| IO | DQ1B2 | | B7 | VREF2B7 | AE21 | AE21 | AH6 | AL5 | DQ0B10 | DQ0B10 | |
| IO | DQ1B1 | | B7 | VREF2B7 | AD20 | AD20 | AG6 | AK6 | DQ0B9 | DQ0B9 | |
| VREF2B7 | | | B7 | VREF2B7 | AD21 | AD21 | AD7 | AH8 | | | |
| IO | DQ1B0 | | B7 | VREF2B7 | AC21 | AC21 | AE6 | AJ6 | DQ0B8 | DQ0B8 | |
| IO | | | B7 | VREF2B7 | | | Y9 | AF10 | | | |
| IO | | | B7 | VREF2B7 | | | | AG10 | | | |
| IO | DQ0B7 | | B7 | VREF2B7 | AE25 | AE25 | AF5 | AL3 | DQ0B7 | DQ0B7 | |
| IO | | | B7 | VREF2B7 | | | AE4 | AG11 | | | |
| IO | DQ0B6 | | B7 | VREF2B7 | AF22 | AF22 | AH5 | AL4 | DQ0B6 | DQ0B6 | |
| IO | | | B7 | VREF2B7 | | | AC6 | AD9 | | | |
| IO | DQ0B5 | | B7 | VREF2B7 | AF24 | AF24 | AF4 | AM4 | DQ0B5 | DQ0B5 | |
| IO | DQ0B4 | | B7 | VREF2B7 | AE22 | AE22 | AG4 | AJ4 | DQ0B4 | DQ0B4 | |
| IO | | | B7 | VREF2B7 | AD23 | AD23 | | AG9 | | | |
| IO | DQ0B3 | | B7 | VREF2B7 | AB22 | AB22 | AG5 | AJ5 | DQ0B3 | DQ0B3 | |
| IO | DQS0B | | B7 | VREF2B7 | AE23 | AE23 | AH3 | AK5 | | | |
| IO | | | B7 | VREF2B7 | AD24 | AD24 | AC5 | AC9 | | | |

*Table 3–1. Pin List for the Stratix EP1S25 Device (Part 19 of 51)*

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DQ0B2 | | B7 | VREF2B7 | AC23 | AC23 | AG3 | AH5 | DQ0B2 | DQ0B2 | |
| IO | DQ0B1 | | B7 | VREF2B7 | AC22 | AC22 | AE5 | AK3 | DQ0B1 | DQ0B1 | |
| IO | | | B7 | VREF2B7 | AD22 | AD22 | AB7 | AE9 | | | |
| IO | DQ0B0 | | B7 | VREF2B7 | AE24 | AE24 | AH4 | AK4 | DQ0B0 | DQ0B0 | |
| IO | | | B7 | VREF2B7 | | | | AF9 | | | |
| IO | DIFFIO_TX77n | | B6 | VREF0B6 | AD25 | AD25 | | AF8 | | | HIGH |
| IO | DIFFIO_TX77p | | B6 | VREF0B6 | AC24 | AC24 | | AF7 | | | HIGH |
| IO | DIFFIO_RX77n | | B6 | VREF0B6 | AD26 | AD26 | | AG4 | | | HIGH |
| IO | DIFFIO_RX77p | | B6 | VREF0B6 | AC25 | AC25 | | AG3 | | | HIGH |
| IO | DIFFIO_TX76n | | B6 | VREF0B6 | AB24 | AB24 | | AF5 | | | HIGH |
| IO | DIFFIO_TX76p | | B6 | VREF0B6 | AB23 | AB23 | | AF6 | | | HIGH |
| IO | DIFFIO_RX76n | | B6 | VREF0B6 | AB26 | AB26 | | AG1 | | | HIGH |
| IO | DIFFIO_RX76p | | B6 | VREF0B6 | AB25 | AB25 | | AG2 | | | HIGH |
| IO | DIFFIO_TX75n | | B6 | VREF0B6 | AA24 | AA24 | | AE7 | | | HIGH |
| IO | DIFFIO_TX75p | | B6 | VREF0B6 | AA23 | AA23 | | AE8 | | | HIGH |
| IO | DIFFIO_RX75n | | B6 | VREF0B6 | AA26 | AA26 | | AF4 | | | HIGH |
| IO | DIFFIO_RX75p | | B6 | VREF0B6 | AA25 | AA25 | | AF3 | | | HIGH |
| VREF0B6 | | | B6 | VREF0B6 | Y21 | Y21 | AE3 | AG6 | | | |
| IO | DIFFIO_TX74n | | B6 | VREF0B6 | AA22 | AA22 | AB5 | AD6 | | | HIGH |
| IO | DIFFIO_TX74p | | B6 | VREF0B6 | Y22 | Y22 | AB6 | AD5 | | | HIGH |
| IO | DIFFIO_RX74n | | B6 | VREF0B6 | Y26 | Y26 | | AF2 | | | HIGH |
| IO | DIFFIO_RX74p | | B6 | VREF0B6 | Y25 | Y25 | | AF1 | | | HIGH |

**Table 3–1. Pin List for the Stratix EP1S25 Device (Part 20 of 51)**

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_TX73n | | B6 | VREF0B6 | Y24 | Y24 | AA7 | AE6 | | | HIGH |
| IO | DIFFIO_TX73p | | B6 | VREF0B6 | Y23 | Y23 | AA8 | AE5 | | | HIGH |
| IO | DIFFIO_RX73n | | B6 | VREF0B6 | W23 | W23 | AF2 | AE4 | | | HIGH |
| IO | DIFFIO_RX73p | | B6 | VREF0B6 | W24 | W24 | AF1 | AE3 | | | HIGH |
| IO | DIFFIO_TX72n | | B6 | VREF0B6 | W21 | W21 | AA5 | AD8 | | | HIGH |
| IO | DIFFIO_TX72p | | B6 | VREF0B6 | W22 | W22 | AA6 | AD7 | | | HIGH |
| IO | DIFFIO_RX72n | | B6 | VREF0B6 | | | AE2 | AE2 | | | HIGH |
| IO | DIFFIO_RX72p | | B6 | VREF0B6 | | | AE1 | AE1 | | | HIGH |
| IO | DIFFIO_TX71n | | B6 | VREF0B6 | | | Y6 | AC5 | | | HIGH |
| IO | DIFFIO_TX71p | | B6 | VREF0B6 | | | Y5 | AC6 | | | HIGH |
| IO | DIFFIO_RX71n | | B6 | VREF0B6 | W25 | W25 | AD2 | AC3 | | | HIGH |
| IO | DIFFIO_RX71p | | B6 | VREF0B6 | W26 | W26 | AD1 | AC4 | | | HIGH |
| IO | DIFFIO_TX70n | | B6 | VREF1B6 | W19 | W19 | Y7 | AC7 | | | HIGH |
| IO | DIFFIO_TX70p | | B6 | VREF1B6 | W20 | W20 | Y8 | AC8 | | | HIGH |
| IO | DIFFIO_RX70n | | B6 | VREF1B6 | V23 | V23 | AC2 | AD3 | | | HIGH |
| IO | DIFFIO_RX70p | | B6 | VREF1B6 | V24 | V24 | AC1 | AD4 | | | HIGH |
| IO | DIFFIO_TX69n | | B6 | VREF1B6 | V21 | V21 | W7 | AB7 | | | HIGH |
| IO | DIFFIO_TX69p | | B6 | VREF1B6 | V22 | V22 | W8 | AB6 | | | HIGH |
| IO | DIFFIO_RX69n | | B6 | VREF1B6 | V25 | V25 | AB4 | AD2 | | | HIGH |
| IO | DIFFIO_RX69p | | B6 | VREF1B6 | V26 | V26 | AB3 | AD1 | | | HIGH |
| IO | DIFFIO_TX68n | | B6 | VREF1B6 | | | W5 | AA6 | | | HIGH |
| IO | DIFFIO_TX68p | | B6 | VREF1B6 | | | W6 | AA7 | | | HIGH |

**Table 3–1. Pin List for the Stratix EP1S25 Device (Part 21 of 51)**

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | | | |
| IO | DIFFIO_RX68n | | B6 | VREF1B6 | | | AB2 | AC2 | | | HIGH |
| IO | DIFFIO_RX68p | | B6 | VREF1B6 | | | AB1 | AB1 | | | HIGH |
| VREF1B6 | | | B6 | VREF1B6 | V20 | V20 | W9 | AB8 | | | |
| IO | DIFFIO_TX67n | | B6 | VREF1B6 | | | V8 | AA9 | | | HIGH |
| IO | DIFFIO_TX67p | | B6 | VREF1B6 | | | V7 | AA8 | | | HIGH |
| IO | DIFFIO_RX67n/RDN6 | | B6 | VREF1B6 | U24 | U24 | AA3 | AA4 | | | HIGH |
| IO | DIFFIO_RX67p/RUP6 | | B6 | VREF1B6 | U23 | U23 | AA4 | AA5 | | | HIGH |
| IO | DIFFIO_TX66n | | B6 | VREF1B6 | | | V6 | Y5 | | | HIGH |
| IO | DIFFIO_TX66p | | B6 | VREF1B6 | | | V5 | Y6 | | | HIGH |
| IO | DIFFIO_RX66n | | B6 | VREF1B6 | | | AA2 | AB3 | | | HIGH |
| IO | DIFFIO_RX66p | | B6 | VREF1B6 | | | AA1 | AB2 | | | HIGH |
| IO | DIFFIO_TX65n | | B6 | VREF1B6 | V19 | V19 | V9 | Y7 | | | HIGH |
| IO | DIFFIO_TX65p | | B6 | VREF1B6 | U20 | U20 | V10 | Y8 | | | HIGH |
| IO | DIFFIO_RX65n | | B6 | VREF1B6 | U26 | U26 | Y4 | AA3 | | | HIGH |
| IO | DIFFIO_RX65p | | B6 | VREF1B6 | U25 | U25 | Y3 | AA2 | | | HIGH |
| IO | DIFFIO_TX64n | | B6 | VREF1B6 | U19 | U19 | U7 | W5 | | | HIGH |
| IO | DIFFIO_TX64p | | B6 | VREF1B6 | U18 | U18 | U8 | W6 | | | HIGH |
| IO | DIFFIO_RX64n | | B6 | VREF1B6 | U22 | U22 | Y2 | Y4 | | | HIGH |
| IO | DIFFIO_RX64p | | B6 | VREF1B6 | U21 | U21 | Y1 | Y3 | | | HIGH |
| IO | DIFFIO_TX63n | | B6 | VREF2B6 | T21 | T21 | U6 | Y10 | | | HIGH |
| IO | DIFFIO_TX63p | | B6 | VREF2B6 | T20 | T20 | U5 | Y9 | | | HIGH |
| IO | DIFFIO_RX63n | | B6 | VREF2B6 | T25 | T25 | W4 | Y2 | | | HIGH |

*Table 3–1. Pin List for the Stratix EP1S25 Device (Part 22 of 51)*

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | | | |
| IO | DIFFIO_RX63p | | B6 | VREF2B6 | T24 | T24 | W3 | Y1 | | | HIGH |
| IO | DIFFIO_TX62n | | B6 | VREF2B6 | T19 | T19 | U9 | W10 | | | HIGH |
| IO | DIFFIO_TX62p | | B6 | VREF2B6 | R19 | R19 | U10 | W9 | | | HIGH |
| IO | DIFFIO_RX62n | | B6 | VREF2B6 | | | W2 | W4 | | | HIGH |
| IO | DIFFIO_RX62p | | B6 | VREF2B6 | | | W1 | W3 | | | HIGH |
| IO | DIFFIO_TX61n | | B6 | VREF2B6 | | | T6 | V9 | | | HIGH |
| IO | DIFFIO_TX61p | | B6 | VREF2B6 | | | T5 | V10 | | | HIGH |
| IO | DIFFIO_RX61n | | B6 | VREF2B6 | T23 | T23 | V4 | W2 | | | HIGH |
| IO | DIFFIO_RX61p | | B6 | VREF2B6 | T22 | T22 | V3 | W1 | | | HIGH |
| VREF2B6 | | | B6 | VREF2B6 | R18 | R18 | R10 | AA10 | | | |
| IO | DIFFIO_TX60n | | B6 | VREF2B6 | | | T10 | V5 | | | HIGH |
| IO | DIFFIO_TX60p | | B6 | VREF2B6 | | | T9 | V6 | | | HIGH |
| IO | DIFFIO_RX60n | | B6 | VREF2B6 | R22 | R22 | V1 | V4 | | | HIGH |
| IO | DIFFIO_RX60p | | B6 | VREF2B6 | R23 | R23 | V2 | V3 | | | HIGH |
| IO | DIFFIO_TX59n | | B6 | VREF2B6 | P20 | P20 | T7 | V8 | | | HIGH |
| IO | DIFFIO_TX59p | | B6 | VREF2B6 | P21 | P21 | T8 | V7 | | | HIGH |
| IO | DIFFIO_RX59n | | B6 | VREF2B6 | R20 | R20 | U4 | V2 | | | HIGH |
| IO | DIFFIO_RX59p | | B6 | VREF2B6 | R21 | R21 | U3 | V1 | | | HIGH |
| IO | DIFFIO_TX58n | | B6 | VREF2B6 | P19 | P19 | T4 | W8 | | | HIGH |
| IO | DIFFIO_TX58p | | B6 | VREF2B6 | N19 | N19 | T3 | W7 | | | HIGH |
| IO | DIFFIO_RX58n | | B6 | VREF2B6 | | | U2 | U5 | | | HIGH |
| IO | DIFFIO_RX58p | | B6 | VREF2B6 | | | T1 | U6 | | | HIGH |

**Table 3–1. Pin List for the Stratix EP1S25 Device (Part 23 of 51)**

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | | | |
| IO | CLK8n | | B6 | VREF2B6 | | | R3 | U3 | | | |
| CLK8p | | | B6 | VREF2B6 | P24 | P24 | R4 | U4 | | | |
| CLK9n | | | B6 | VREF2B6 | P25 | P25 | T2 | U1 | | | |
| CLK9p | | | B6 | VREF2B6 | R26 | R26 | R2 | U2 | | | |
| GNDG_PLL3 | | | | | R25 | R25 | R7 | U11 | | | |
| VCCG_PLL3 | | | | | P23 | P23 | R8 | V11 | | | |
| GNDA_PLL3 | | | | | R24 | R24 | R5 | U7 | | | |
| GND | | | | | | | | | | | |
| VCCA_PLL3 | | | | | P22 | P22 | R6 | U8 | | | |
| VCCINT | | | | | | | | | | | |
| GNDG_PLL4 | | | | | N22 | N22 | P7 | U9 | | | |
| VCCG_PLL4 | | | | | N24 | N24 | P8 | T9 | | | |
| GNDA_PLL4 | | | | | N23 | N23 | P5 | T7 | | | |
| GND | | | | | | | | | | | |
| VCCA_PLL4 | | | | | N25 | N25 | P6 | T8 | | | |
| VCCINT | | | | | | | | | | | |
| CLK10p | | | B5 | VREF0B5 | M26 | M26 | P4 | T6 | | | |
| IO | CLK10n | | B5 | VREF0B5 | | | P3 | T5 | | | |
| CLK11p | | | B5 | VREF0B5 | M24 | M24 | P2 | T4 | | | |
| CLK11n | | | B5 | VREF0B5 | M25 | M25 | N2 | T3 | | | |
| IO | DIFFIO_TX57n | | B5 | VREF0B5 | N20 | N20 | N10 | R7 | | | HIGH |
| IO | DIFFIO_TX57p | | B5 | VREF0B5 | N21 | N21 | N9 | R8 | | | HIGH |

*Table 3–1. Pin List for the Stratix EP1S25 Device (Part 24 of 51)*

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_RX57n | | B5 | VREF0B5 | | | M2 | T2 | | | HIGH |
| IO | DIFFIO_RX57p | | B5 | VREF0B5 | | | N1 | T1 | | | HIGH |
| IO | DIFFIO_TX56n | | B5 | VREF0B5 | M18 | M18 | N5 | P7 | | | HIGH |
| IO | DIFFIO_TX56p | | B5 | VREF0B5 | M19 | M19 | N6 | P8 | | | HIGH |
| IO | DIFFIO_RX56n | | B5 | VREF0B5 | M20 | M20 | M3 | R1 | | | HIGH |
| IO | DIFFIO_RX56p | | B5 | VREF0B5 | M21 | M21 | M4 | R2 | | | HIGH |
| IO | DIFFIO_TX55n | | B5 | VREF0B5 | | | N7 | R5 | | | HIGH |
| IO | DIFFIO_TX55p | | B5 | VREF0B5 | | | N8 | R6 | | | HIGH |
| IO | DIFFIO_RX55n | | B5 | VREF0B5 | M22 | M22 | L1 | R3 | | | HIGH |
| IO | DIFFIO_RX55p | | B5 | VREF0B5 | M23 | M23 | L2 | R4 | | | HIGH |
| IO | DIFFIO_TX54n | | B5 | VREF0B5 | | | N4 | R10 | | | HIGH |
| IO | DIFFIO_TX54p | | B5 | VREF0B5 | | | N3 | R9 | | | HIGH |
| IO | DIFFIO_RX54n | | B5 | VREF0B5 | L22 | L22 | L3 | P1 | | | HIGH |
| IO | DIFFIO_RX54p | | B5 | VREF0B5 | L23 | L23 | L4 | P2 | | | HIGH |
| VREF0B5 | | | B5 | VREF0B5 | L19 | L19 | P10 | R12 | | | |
| IO | DIFFIO_TX53n | | B5 | VREF0B5 | L21 | L21 | M10 | P6 | | | HIGH |
| IO | DIFFIO_TX53p | | B5 | VREF0B5 | L20 | L20 | M9 | P5 | | | HIGH |
| IO | DIFFIO_RX53n | | B5 | VREF0B5 | | | K1 | P3 | | | HIGH |
| IO | DIFFIO_RX53p | | B5 | VREF0B5 | | | K2 | P4 | | | HIGH |
| IO | DIFFIO_TX52n | | B5 | VREF0B5 | K20 | K20 | M6 | N7 | | | HIGH |
| IO | DIFFIO_TX52p | | B5 | VREF0B5 | K19 | K19 | M5 | N8 | | | HIGH |
| IO | DIFFIO_RX52n | | B5 | VREF0B5 | L25 | L25 | K4 | N1 | | | HIGH |

*Table 3–1. Pin List for the Stratix EP1S25 Device (Part 25 of 51)*

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_RX52p | | B5 | VREF0B5 | L24 | L24 | K3 | N2 | | | HIGH |
| IO | DIFFIO_TX51n | | B5 | VREF0B5 | K22 | K22 | M8 | P9 | | | HIGH |
| IO | DIFFIO_TX51p | | B5 | VREF0B5 | K21 | K21 | M7 | P10 | | | HIGH |
| IO | DIFFIO_RX51n | | B5 | VREF0B5 | K24 | K24 | J1 | N3 | | | HIGH |
| IO | DIFFIO_RX51p | | B5 | VREF0B5 | K23 | K23 | J2 | N4 | | | HIGH |
| IO | DIFFIO_TX50n | | B5 | VREF0B5 | J20 | J20 | L10 | N5 | | | HIGH |
| IO | DIFFIO_TX50p | | B5 | VREF0B5 | J19 | J19 | L9 | N6 | | | HIGH |
| IO | DIFFIO_RX50n | | B5 | VREF0B5 | K26 | K26 | J3 | M2 | | | HIGH |
| IO | DIFFIO_RX50p | | B5 | VREF0B5 | K25 | K25 | J4 | M3 | | | HIGH |
| IO | DIFFIO_TX49n | | B5 | VREF0B5 | | | L5 | N10 | | | HIGH |
| IO | DIFFIO_TX49p | | B5 | VREF0B5 | | | L6 | N9 | | | HIGH |
| IO | DIFFIO_RX49n | | B5 | VREF0B5 | | | H1 | L2 | | | HIGH |
| IO | DIFFIO_RX49p | | B5 | VREF0B5 | | | H2 | L3 | | | HIGH |
| IO | DIFFIO_TX48n | | B5 | VREF1B5 | | | L8 | M8 | | | HIGH |
| IO | DIFFIO_TX48p | | B5 | VREF1B5 | | | L7 | M9 | | | HIGH |
| IO | DIFFIO_RX48n/RDN5 | | B5 | VREF1B5 | J22 | J22 | H3 | M4 | | | HIGH |
| IO | DIFFIO_RX48p/RUP5 | | B5 | VREF1B5 | J21 | J21 | H4 | M5 | | | HIGH |
| IO | DIFFIO_TX47n | | B5 | VREF1B5 | H20 | H20 | K7 | M6 | | | HIGH |
| IO | DIFFIO_TX47p | | B5 | VREF1B5 | H19 | H19 | K8 | M7 | | | HIGH |
| IO | DIFFIO_RX47n | | B5 | VREF1B5 | J26 | J26 | G1 | L1 | | | HIGH |
| IO | DIFFIO_RX47p | | B5 | VREF1B5 | J25 | J25 | G2 | K2 | | | HIGH |
| IO | DIFFIO_TX46n | | B5 | VREF1B5 | | | J7 | L6 | | | HIGH |

*Table 3–1. Pin List for the Stratix EP1S25 Device (Part 26 of 51)*

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_TX46p | | B5 | VREF1B5 | | | J8 | L7 | | | HIGH |
| IO | DIFFIO_RX46n | | B5 | VREF1B5 | J24 | J24 | G4 | J2 | | | HIGH |
| IO | DIFFIO_RX46p | | B5 | VREF1B5 | J23 | J23 | G3 | J1 | | | HIGH |
| IO | DIFFIO_TX45n | | B5 | VREF1B5 | H22 | H22 | K5 | K5 | | | HIGH |
| IO | DIFFIO_TX45p | | B5 | VREF1B5 | H21 | H21 | K6 | K6 | | | HIGH |
| IO | DIFFIO_RX45n | | B5 | VREF1B5 | | | F1 | K4 | | | HIGH |
| IO | DIFFIO_RX45p | | B5 | VREF1B5 | | | F2 | K3 | | | HIGH |
| IO | DIFFIO_TX44n | | B5 | VREF1B5 | H24 | H24 | J6 | K8 | | | HIGH |
| IO | DIFFIO_TX44p | | B5 | VREF1B5 | H23 | H23 | J5 | K7 | | | HIGH |
| IO | DIFFIO_RX44n | | B5 | VREF1B5 | | | F3 | J3 | | | HIGH |
| IO | DIFFIO_RX44p | | B5 | VREF1B5 | | | F4 | J4 | | | HIGH |
| VREF1B5 | | | B5 | VREF1B5 | J18 | J18 | K9 | L8 | | | |
| IO | DIFFIO_TX43n | | B5 | VREF1B5 | G21 | G21 | H8 | J5 | | | HIGH |
| IO | DIFFIO_TX43p | | B5 | VREF1B5 | G22 | G22 | H7 | J6 | | | HIGH |
| IO | DIFFIO_RX43n | | B5 | VREF1B5 | H25 | H25 | E1 | H1 | | | HIGH |
| IO | DIFFIO_RX43p | | B5 | VREF1B5 | H26 | H26 | E2 | H2 | | | HIGH |
| IO | DIFFIO_TX42n | | B5 | VREF1B5 | G23 | G23 | H6 | J7 | | | HIGH |
| IO | DIFFIO_TX42p | | B5 | VREF1B5 | G24 | G24 | H5 | J8 | | | HIGH |
| IO | DIFFIO_RX42n | | B5 | VREF1B5 | G25 | G25 | D1 | G1 | | | HIGH |
| IO | DIFFIO_RX42p | | B5 | VREF1B5 | G26 | G26 | D2 | G2 | | | HIGH |
| IO | DIFFIO_TX41n | | B5 | VREF1B5 | F23 | F23 | G5 | H5 | | | HIGH |
| IO | DIFFIO_TX41p | | B5 | VREF1B5 | F24 | F24 | G6 | H6 | | | HIGH |

Table 3–1. Pin List for the Stratix EP1S25 Device (Part 27 of 51)

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | | | |
| IO | DIFFIO_RX41n | | B5 | VREF1B5 | F25 | F25 | C1 | H3 | | | HIGH |
| IO | DIFFIO_RX41p | | B5 | VREF1B5 | F26 | F26 | C2 | H4 | | | HIGH |
| IO | DIFFIO_TX40n | | B5 | VREF1B5 | E23 | E23 | F6 | H8 | | | HIGH |
| IO | DIFFIO_TX40p | | B5 | VREF1B5 | E24 | E24 | F5 | H7 | | | HIGH |
| IO | DIFFIO_RX40n | | B5 | VREF1B5 | E25 | E25 | | F1 | | | HIGH |
| IO | DIFFIO_RX40p | | B5 | VREF1B5 | E26 | E26 | | F2 | | | HIGH |
| IO | DIFFIO_TX39n | | B5 | VREF1B5 | D24 | D24 | | G6 | | | HIGH |
| IO | DIFFIO_TX39p | | B5 | VREF1B5 | C25 | C25 | | G5 | | | HIGH |
| IO | DIFFIO_RX39n | | B5 | VREF1B5 | D25 | D25 | | G3 | | | HIGH |
| IO | DIFFIO_RX39p | | B5 | VREF1B5 | C26 | C26 | | G4 | | | HIGH |
| IO | | | B4 | VREF0B4 | | | | F7 | | | |
| IO | DQ0T0 | | B4 | VREF0B4 | B24 | B24 | A4 | D5 | DQ0T0 | DQ0T0 | |
| IO | | | B4 | VREF0B4 | B25 | B25 | G7 | K9 | | | |
| IO | DQ0T1 | | B4 | VREF0B4 | D23 | D23 | A3 | C3 | DQ0T1 | DQ0T1 | |
| IO | DQ0T2 | | B4 | VREF0B4 | D22 | D22 | B3 | E5 | DQ0T2 | DQ0T2 | |
| IO | DQS0T | | B4 | VREF0B4 | C24 | C24 | D5 | C5 | | | |
| IO | | | B4 | VREF0B4 | B23 | B23 | F7 | F8 | | | |
| IO | DQ0T3 | | B4 | VREF0B4 | E22 | E22 | B5 | C4 | DQ0T3 | DQ0T3 | |
| IO | | | B4 | VREF0B4 | C23 | C23 | | J9 | | | |
| IO | DQ0T4 | | B4 | VREF0B4 | B22 | B22 | B4 | D4 | DQ0T4 | DQ0T4 | |
| IO | DQ0T5 | | B4 | VREF0B4 | A24 | A24 | C4 | A4 | DQ0T5 | DQ0T5 | |
| IO | | | B4 | VREF0B4 | | | G8 | M10 | | | |

Table 3–1. Pin List for the Stratix EP1S25 Device (Part 28 of 51)

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed Note (1) |
| IO | DQ0T6 | | B4 | VREF0B4 | A22 | A22 | A5 | B4 | DQ0T6 | DQ0T6 | |
| IO | | | B4 | VREF0B4 | | | F8 | G9 | | | |
| IO | DQ0T7 | | B4 | VREF0B4 | C22 | C22 | C5 | B3 | DQ0T7 | DQ0T7 | |
| IO | | | B4 | VREF0B4 | | | | H9 | | | |
| IO | | | B4 | VREF0B4 | | | J9 | L9 | | | |
| IO | DQ1T0 | | B4 | VREF0B4 | C20 | C20 | E6 | D6 | DQ0T8 | DQ0T8 | |
| VREF0B4 | | | B4 | VREF0B4 | F22 | F22 | E7 | E6 | | | |
| IO | DQ1T1 | | B4 | VREF0B4 | D21 | D21 | A6 | C6 | DQ0T9 | DQ0T9 | |
| IO | DQ1T2 | | B4 | VREF0B4 | D20 | D20 | B7 | B5 | DQ0T10 | DQ0T10 | |
| IO | | | B4 | VREF0B4 | B21 | B21 | | K11 | | | |
| IO | DQS1T | | B4 | VREF0B4 | A21 | A21 | B6 | E7 | DQS0T | | |
| IO | | | B4 | VREF0B4 | | | H9 | L11 | | | |
| IO | DQ1T3 | | B4 | VREF0B4 | C21 | C21 | D6 | C7 | DQ0T11 | DQ0T11 | |
| IO | DQ1T4 | | B4 | VREF0B4 | B20 | B20 | A7 | A5 | DQ0T12 | DQ0T12 | |
| IO | | | B4 | VREF0B4 | | | | J11 | | | |
| IO | DQ1T5 | | B4 | VREF0B4 | E21 | E21 | D7 | D7 | DQ0T13 | DQ0T13 | |
| IO | | | B4 | VREF0B4 | | | G9 | F9 | | | |
| IO | DQ1T6 | | B4 | VREF0B4 | A20 | A20 | C6 | A6 | DQ0T14 | DQ0T14 | |
| IO | DQ1T7 | | B4 | VREF0B4 | F21 | F21 | C7 | B6 | DQ0T15 | DQ0T15 | |
| IO | | | B4 | VREF0B4 | C19 | C19 | F9 | G10 | | | |
| IO | | | B4 | VREF0B4 | | | | F10 | | | |
| IO | DQ2T0 | | B4 | VREF0B4 | D19 | D19 | D8 | B7 | DQ1T0 | DQ0T16 | |

*Table 3–1. Pin List for the Stratix EP1S25 Device (Part 29 of 51)*

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | | | |
| IO | DQ2T1 | | B4 | VREF0B4 | E20 | E20 | C8 | D8 | DQ1T1 | DQ0T17 | |
| IO | | | B4 | VREF0B4 | B19 | B19 | H10 | L12 | | | |
| IO | DQ2T2 | | B4 | VREF0B4 | E19 | E19 | E8 | B8 | DQ1T2 | DQ0T18 | |
| IO | DQS2T | | B4 | VREF1B4 | A19 | A19 | C9 | A7 | | DQS0T | |
| IO | | | B4 | VREF1B4 | | | | H11 | | | |
| IO | DQ2T3 | | B4 | VREF1B4 | C18 | C18 | D9 | E9 | DQ1T3 | DQ0T19 | |
| IO | DQ2T4 | | B4 | VREF1B4 | B18 | B18 | B9 | A8 | DQ1T4 | DQ0T20 | |
| IO | DQ2T5 | | B4 | VREF1B4 | D18 | D18 | B8 | C9 | DQ1T5 | DQ0T21 | |
| IO | DQ2T6 | | B4 | VREF1B4 | F20 | F20 | A8 | C8 | DQ1T6 | DQ0T22 | |
| IO | FCLK6 | | B4 | VREF1B4 | G19 | G19 | G10 | G12 | | | |
| IO | FCLK7 | | B4 | VREF1B4 | E18 | E18 | F10 | A14 | | | |
| IO | DQ2T7 | | B4 | VREF1B4 | G20 | G20 | A9 | D9 | DQ1T7 | DQ0T23 | |
| IO | | | B4 | VREF1B4 | | | | J12 | | | |
| IO | | | B4 | VREF1B4 | A18 | A18 | J10 | K12 | | | |
| IO | DQ3T0 | | B4 | VREF1B4 | F19 | F19 | E10 | E11 | DQ1T8 | DQ0T24 | |
| VREF1B4 | | | B4 | VREF1B4 | F18 | F18 | E9 | E8 | | | |
| IO | DQ3T1 | | B4 | VREF1B4 | C17 | C17 | A10 | B9 | DQ1T9 | DQ0T25 | |
| IO | | | B4 | VREF1B4 | | | F11 | H12 | | | |
| IO | DQ3T2 | | B4 | VREF1B4 | G18 | G18 | C10 | D10 | DQ1T10 | DQ0T26 | |
| IO | | | B4 | VREF1B4 | | | K10 | K13 | | | |
| IO | DQS3T | | B4 | VREF1B4 | B17 | B17 | D10 | D11 | DQS1T | | |
| IO | DQ3T3 | | B4 | VREF1B4 | E17 | E17 | B10 | C10 | DQ1T11 | DQ0T27 | |

*Table 3–1. Pin List for the Stratix EP1S25 Device (Part 30 of 51)*

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | | | |
| IO | | | B4 | VREF1B4 | | | | F12 | | | |
| IO | DQ3T4 | | B4 | VREF1B4 | F17 | F17 | A11 | A9 | DQ1T12 | DQ0T28 | |
| IO | DQ3T5 | | B4 | VREF1B4 | D17 | D17 | C11 | B11 | DQ1T13 | DQ0T29 | |
| IO | DEV_OE | | B4 | VREF1B4 | G17 | G17 | J11 | L13 | | | |
| IO | DQ3T6 | | B4 | VREF1B4 | A17 | A17 | D11 | C11 | DQ1T14 | DQ0T30 | |
| IO | DQ3T7 | | B4 | VREF1B4 | H18 | H18 | B11 | B10 | DQ1T15 | DQ0T31 | |
| IO | RUP4 | | B4 | VREF1B4 | D16 | D16 | H11 | G13 | | | |
| IO | RDN4 | | B4 | VREF1B4 | C16 | C16 | G11 | J13 | | | |
| IO | DQ4T0 | | B4 | VREF1B4 | | | B12 | A11 | | | |
| IO | | nWS | B4 | VREF1B4 | E16 | E16 | K11 | D14 | | | |
| IO | DQ4T1 | | B4 | VREF1B4 | | | C12 | B12 | | | |
| IO | DQ4T2 | | B4 | VREF1B4 | | | D12 | C12 | | | |
| IO | | | B4 | VREF2B4 | B16 | B16 | G12 | F13 | | | |
| IO | DQS4T | | B4 | VREF2B4 | | | A13 | D12 | | | |
| IO | | DATA0 | B4 | VREF2B4 | F16 | F16 | H12 | E14 | | | |
| IO | DQ4T3 | | B4 | VREF2B4 | | | B13 | C13 | | | |
| IO | DQ4T4 | | B4 | VREF2B4 | | | E12 | D13 | | | |
| IO | | | B4 | VREF2B4 | | | L11 | L14 | | | |
| IO | DQ4T5 | | B4 | VREF2B4 | | | C13 | E13 | | | |
| IO | | DATA1 | B4 | VREF2B4 | C15 | C15 | F12 | F14 | | | |
| IO | DQ4T6 | | B4 | VREF2B4 | | | D13 | A13 | | | |
| IO | DQ4T7 | | B4 | VREF2B4 | | | E13 | B13 | | | |

**Table 3–1. Pin List for the Stratix EP1S25 Device (Part 31 of 51)**

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **672-Pin BGA** | **672-Pin FBGA** | **780-Pin FBGA** | **1020-Pin FBGA** | | | |
| IO | | | B4 | VREF2B4 | | | M11 | H13 | | | |
| IO | | DATA2 | B4 | VREF2B4 | H16 | H16 | J12 | F15 | | | |
| VREF2B4 | | | B4 | VREF2B4 | G16 | G16 | E11 | E10 | | | |
| IO | | | B4 | VREF2B4 | | | | C14 | | | |
| IO | | | B4 | VREF2B4 | | | | B14 | | | |
| IO | | | B4 | VREF2B4 | | | | H14 | | | |
| IO | | | B4 | VREF2B4 | | | | J15 | | | |
| IO | | | B4 | VREF2B4 | | | | J14 | | | |
| IO | | | B4 | VREF2B4 | | | | K14 | | | |
| TMS | | TMS | B4 | VREF2B4 | E15 | E15 | F13 | E15 | | | |
| TRST | | TRST | B4 | VREF2B4 | D15 | D15 | L12 | G15 | | | |
| TCK | | TCK | B4 | VREF2B4 | G15 | G15 | K12 | G14 | | | |
| IO | | DATA3 | B4 | VREF2B4 | F15 | F15 | M12 | C16 | | | |
| IO | | | B4 | VREF2B4 | | | | K15 | | | |
| IO | | | B4 | VREF2B4 | | | | L15 | | | |
| TDI | | TDI | B4 | VREF2B4 | H15 | H15 | G13 | D16 | | | |
| TDO | | TDO | B4 | VREF2B4 | G14 | G14 | H13 | F16 | | | |
| IO | CLK12n | | B4 | VREF2B4 | | | J13 | A15 | | | |
| CLK12p | | | B4 | VREF2B4 | B15 | B15 | K13 | B15 | | | |
| IO | CLK13n | | B4 | VREF2B4 | | | L13 | C15 | | | |
| CLK13p | | | B4 | VREF2B4 | A15 | A15 | M13 | D15 | | | |
| TEMPDIODEp | | | | | H14 | H14 | B14 | E18 | | | |

*Table 3–1. Pin List for the Stratix EP1S25 Device (Part 32 of 51)*

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **672-Pin BGA** | **672-Pin FBGA** | **780-Pin FBGA** | **1020-Pin FBGA** | **DQS for x16** | **DQS for x32** | **DIFFIO Speed** *Note (1)* |
| TEMPDIODEn | | | | | G13 | G13 | C14 | F18 | | | |
| VCCINT | | | | | | | | | | | |
| VCCA_PLL5 | | | | | D14 | D14 | F14 | G17 | | | |
| GND | | | | | | | | | | | |
| GNDA_PLL5 | | | | | B14 | B14 | G14 | F17 | | | |
| GNDA_PLL5 | | | | | | | | | | | |
| VCCG_PLL5 | | | | | C14 | C14 | D14 | J16 | | | |
| GNDG_PLL5 | | | | | B13 | B13 | E14 | L16 | | | |
| VCC_PLL5_ OUTA | | | B9 | | D13 | D13 | F15 | H17 | | | |
| VCC_PLL5_ OUTA | | | B9 | | | | | | | | |
| VCC_PLL5_ OUTB | | | B10 | | | | G16 | L17 | | | |
| VCC_PLL5_ OUTB | | | B10 | | | | | | | | |
| IO | PLL5_OUT0p | | B9 | VREF0B3 | F13 | F13 | E15 | B16 | | | |
| IO | PLL5_OUT0n | | B9 | VREF0B3 | E13 | E13 | D15 | A16 | | | |
| IO | PLL5_OUT1p | | B9 | VREF0B3 | F14 | F14 | K14 | B17 | | | |
| IO | PLL5_OUT1n | | B9 | VREF0B3 | E14 | E14 | K15 | A17 | | | |
| IO | PLL5_FBp | | B9 | VREF0B3 | F12 | F12 | H14 | D17 | | | |
| IO | PLL5_FBn | | B9 | VREF0B3 | E12 | E12 | H15 | C17 | | | |
| IO | PLL5_OUT2p | | B10 | VREF0B3 | | | C15 | B18 | | | |

*Table 3–1. Pin List for the Stratix EP1S25 Device (Part 33 of 51)*

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **672-Pin BGA** | **672-Pin FBGA** | **780-Pin FBGA** | **1020-Pin FBGA** | **DQS for x16** | **DQS for x32** | **DIFFIO Speed** *Note (1)* |
| IO | PLL5_OUT2n | | B10 | VREF0B3 | | | B15 | A18 | | | |
| IO | PLL5_OUT3p | | B10 | VREF0B3 | | | K16 | D18 | | | |
| IO | PLL5_OUT3n | | B10 | VREF0B3 | | | J16 | C18 | | | |
| nSTATUS | | nSTATUS | B3 | VREF0B3 | H13 | H13 | M16 | G16 | | | |
| nCONFIG | | nCONFIG | B3 | VREF0B3 | H12 | H12 | L16 | J18 | | | |
| DCLK | | DCLK | B3 | VREF0B3 | G12 | G12 | F16 | E19 | | | |
| CONF_DONE | | CONF_DONE | B3 | VREF0B3 | H11 | H11 | G17 | G18 | | | |
| CLK14p | | | B3 | VREF0B3 | B12 | B12 | K17 | A19 | | | |
| IO | CLK14n | | B3 | VREF0B3 | A12 | A12 | J17 | B19 | | | |
| CLK15p | | | B3 | VREF0B3 | D12 | D12 | M17 | C19 | | | |
| IO | CLK15n | | B3 | VREF0B3 | C12 | C12 | L17 | D19 | | | |
| VREF0B3 | | | B3 | VREF0B3 | F11 | F11 | E18 | E21 | | | |
| IO | | | B3 | VREF0B3 | | | | K18 | | | |
| IO | | | B3 | VREF0B3 | | | | F19 | | | |
| IO | | DATA4 | B3 | VREF0B3 | E11 | E11 | H17 | G19 | | | |
| IO | | | B3 | VREF0B3 | | | L18 | F20 | | | |
| IO | | | B3 | VREF0B3 | | | M18 | L18 | | | |
| IO | | | B3 | VREF0B3 | | | | K20 | | | |
| IO | | | B3 | VREF0B3 | | | | H19 | | | |
| IO | | | B3 | VREF0B3 | B11 | B11 | F17 | G20 | | | |
| IO | DQ5T0 | | B3 | VREF0B3 | | | D16 | A20 | | | |
| IO | DQ5T1 | | B3 | VREF0B3 | | | C16 | B20 | | | |

*Table 3–1. Pin List for the Stratix EP1S25 Device (Part 34 of 51)*

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | | | |
| IO | | DATA5 | B3 | VREF0B3 | G11 | G11 | K18 | J19 | | | |
| IO | DQ5T2 | | B3 | VREF0B3 | | | E16 | C20 | | | |
| IO | DQS5T | | B3 | VREF0B3 | | | A16 | D20 | | | |
| IO | | | B3 | VREF0B3 | | | | H20 | | | |
| IO | DQ5T3 | | B3 | VREF0B3 | | | B16 | E20 | | | |
| IO | | DATA6 | B3 | VREF0B3 | H10 | H10 | H18 | K19 | | | |
| IO | DQ5T4 | | B3 | VREF0B3 | | | E17 | B21 | | | |
| IO | DQ5T5 | | B3 | VREF0B3 | | | D17 | C21 | | | |
| IO | | | B3 | VREF1B3 | | | F18 | G21 | | | |
| IO | DQ5T6 | | B3 | VREF1B3 | | | B17 | D21 | | | |
| IO | | | B3 | VREF1B3 | | | | F23 | | | |
| IO | DQ5T7 | | B3 | VREF1B3 | | | C17 | A22 | | | |
| IO | RUP3 | | B3 | VREF1B3 | C11 | C11 | J18 | F21 | | | |
| IO | RDN3 | | B3 | VREF1B3 | D11 | D11 | K19 | L19 | | | |
| IO | DQ6T0 | | B3 | VREF1B3 | A10 | A10 | A18 | B22 | DQ2T0 | DQ1T0 | |
| IO | DQ6T1 | | B3 | VREF1B3 | E10 | E10 | C18 | C22 | DQ2T1 | DQ1T1 | |
| IO | | DATA7 | B3 | VREF1B3 | G10 | G10 | G18 | J20 | | | |
| IO | DQ6T2 | | B3 | VREF1B3 | F10 | F10 | D18 | B23 | DQ2T2 | DQ1T2 | |
| IO | DQS6T | | B3 | VREF1B3 | G9 | G9 | B18 | D22 | DQS2T | | |
| IO | | | B3 | VREF1B3 | | | | L20 | | | |
| IO | DQ6T3 | | B3 | VREF1B3 | F9 | F9 | A19 | C23 | DQ2T3 | DQ1T3 | |
| IO | | CLKUSR | B3 | VREF1B3 | D10 | D10 | J19 | H21 | | | |

*Table 3–1. Pin List for the Stratix EP1S25 Device (Part 35 of 51)*

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | | | |
| IO | DQ6T4 | | B3 | VREF1B3 | C10 | C10 | B19 | A24 | DQ2T4 | DQ1T4 | |
| IO | | | B3 | VREF1B3 | | | | J21 | | | |
| IO | DQ6T5 | | B3 | VREF1B3 | B10 | B10 | C19 | E22 | DQ2T5 | DQ1T5 | |
| IO | DQ6T6 | | B3 | VREF1B3 | A9 | A9 | E19 | B24 | DQ2T6 | DQ1T6 | |
| VREF1B3 | | | B3 | VREF1B3 | D9 | D9 | E20 | E23 | | | |
| IO | FCLK0 | | B3 | VREF1B3 | E9 | E9 | F19 | F22 | | | |
| IO | FCLK1 | | B3 | VREF1B3 | B9 | B9 | G19 | G22 | | | |
| IO | DQ6T7 | | B3 | VREF1B3 | C9 | C9 | D19 | D23 | DQ2T7 | DQ1T7 | |
| IO | | | B3 | VREF1B3 | G7 | G7 | H19 | K21 | | | |
| IO | | | B3 | VREF1B3 | | | | L21 | | | |
| IO | DQ7T0 | | B3 | VREF1B3 | A8 | A8 | B20 | D24 | DQ2T8 | DQ1T8 | |
| GND | | | B3 | | GND | GND | | | | | |
| GND | | | B3 | | | | | | | | |
| GND | | | B3 | | F8 | F8 | G20 | H24 | | | |
| IO | DQ7T1 | | B3 | VREF1B3 | A7 | A7 | A20 | A25 | DQ2T9 | DQ1T9 | |
| IO | DQ7T2 | | B3 | VREF1B3 | B8 | B8 | C20 | C24 | DQ2T10 | DQ1T10 | |
| IO | | | B3 | VREF1B3 | | | | H22 | | | |
| IO | DQS7T | | B3 | VREF1B3 | E8 | E8 | D20 | B26 | | DQS1T | |
| IO | DQ7T3 | | B3 | VREF1B3 | F7 | F7 | A21 | B25 | DQ2T11 | DQ1T11 | |
| IO | | | B3 | VREF1B3 | | | J20 | K22 | | | |
| IO | DQ7T4 | | B3 | VREF1B3 | B7 | B7 | B21 | C25 | DQ2T12 | DQ1T12 | |
| IO | DQ7T5 | | B3 | VREF1B3 | C8 | C8 | C21 | D25 | DQ2T13 | DQ1T13 | |

**Table 3–1. Pin List for the Stratix EP1S25 Device (Part 36 of 51)**

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | | | B3 | VREF1B3 | | | | J22 | | | |
| IO | DQ7T6 | | B3 | VREF1B3 | D8 | D8 | D21 | A26 | DQ2T14 | DQ1T14 | |
| IO | DQ7T7 | | B3 | VREF1B3 | E7 | E7 | E21 | E24 | DQ2T15 | DQ1T15 | |
| IO | | | B3 | VREF1B3 | | | H20 | L22 | | | |
| IO | | | B3 | VREF2B3 | | | | G23 | | | |
| IO | DQ8T0 | | B3 | VREF2B3 | B6 | B6 | B22 | C26 | DQ3T0 | DQ1T16 | |
| IO | DQ8T1 | | B3 | VREF2B3 | A6 | A6 | A22 | A28 | DQ3T1 | DQ1T17 | |
| IO | | | B3 | VREF2B3 | | | | H23 | | | |
| IO | DQ8T2 | | B3 | VREF2B3 | F6 | F6 | C22 | A27 | DQ3T2 | DQ1T18 | |
| IO | DQS8T | | B3 | VREF2B3 | F5 | F5 | D23 | B27 | DQS3T | | |
| IO | | | B3 | VREF2B3 | | | | F24 | | | |
| IO | DQ8T3 | | B3 | VREF2B3 | D6 | D6 | D22 | D26 | DQ3T3 | DQ1T19 | |
| IO | DQ8T4 | | B3 | VREF2B3 | E6 | E6 | A23 | C27 | DQ3T4 | DQ1T20 | |
| IO | | | B3 | VREF2B3 | | | | J24 | | | |
| IO | DQ8T5 | | B3 | VREF2B3 | A5 | A5 | C23 | B28 | DQ3T5 | DQ1T21 | |
| IO | DQ8T6 | | B3 | VREF2B3 | E5 | E5 | E23 | D27 | DQ3T6 | DQ1T22 | |
| VREF2B3 | | | B3 | VREF2B3 | D7 | D7 | E22 | E25 | | | |
| IO | DQ8T7 | | B3 | VREF2B3 | C7 | C7 | B23 | E26 | DQ3T7 | DQ1T23 | |
| IO | | | B3 | VREF2B3 | C6 | C6 | F20 | G24 | | | |
| IO | | | B3 | VREF2B3 | B5 | B5 | | J23 | | | |
| IO | DQ9T0 | | B3 | VREF2B3 | C3 | C3 | A24 | A29 | DQ3T8 | DQ1T24 | |
| IO | | | B3 | VREF2B3 | | | | K23 | | | |

**Table 3–1. Pin List for the Stratix EP1S25 Device (Part 37 of 51)**

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | | | |
| IO | DQ9T1 | | B3 | VREF2B3 | A3 | A3 | C25 | B29 | DQ3T9 | DQ1T25 | |
| IO | | | B3 | VREF2B3 | | | F21 | F25 | | | |
| IO | DQ9T2 | | B3 | VREF2B3 | D5 | D5 | A25 | B30 | DQ3T10 | DQ1T26 | |
| IO | DQS9T | | B3 | VREF2B3 | B4 | B4 | C24 | C28 | | | |
| IO | | | B3 | VREF2B3 | | | G21 | F26 | | | |
| IO | DQ9T3 | | B3 | VREF2B3 | C2 | C2 | D24 | C29 | DQ3T11 | DQ1T27 | |
| IO | | | B3 | VREF2B3 | | | G22 | L23 | | | |
| IO | DQ9T4 | | B3 | VREF2B3 | B3 | B3 | B24 | D29 | DQ3T12 | DQ1T28 | |
| IO | DQ9T5 | | B3 | VREF2B3 | D4 | D4 | B25 | D28 | DQ3T13 | DQ1T29 | |
| IO | DQ9T6 | | B3 | VREF2B3 | C4 | C4 | A26 | C30 | DQ3T14 | DQ1T30 | |
| IO | | | B3 | VREF2B3 | C5 | C5 | F22 | K24 | | | |
| IO | DQ9T7 | | B3 | VREF2B3 | D3 | D3 | B26 | E28 | DQ3T15 | DQ1T31 | |
| IO | | | B3 | VREF2B3 | | | | L24 | | | |
| VCCIO2 | | | | | D1 | D1 | B28 | C31 | | | |
| VCCIO2 | | | | | L1 | L1 | M28 | C32 | | | |
| VCCIO2 | | | | | L9 | L9 | P20 | M32 | | | |
| VCCIO2 | | | | | | | | T23 | | | |
| VCCIO2 | | | | | | | | | | | |
| VCCIO2 | | | | | | | | | | | |
| VCCIO2 | | | | | | | | | | | |
| VCCIO2 | | | | | | | | | | | |
| VCCIO2 | | | | | | | | | | | |

**Table 3–1. Pin List for the Stratix EP1S25 Device (Part 38 of 51)**

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| VCCIO2 | | | | | | | | | | | |
| VCCIO2 | | | | | | | | | | | |
| VCCIO1 | | | | | T1 | T1 | R20 | AA32 | | | |
| VCCIO1 | | | | | AC1 | AC1 | U28 | AK31 | | | |
| VCCIO1 | | | | | T9 | T9 | AG28 | AK32 | | | |
| VCCIO1 | | | | | | | | U23 | | | |
| VCCIO1 | | | | | | | | | | | |
| VCCIO1 | | | | | | | | | | | |
| VCCIO1 | | | | | | | | | | | |
| VCCIO1 | | | | | | | | | | | |
| VCCIO1 | | | | | | | | | | | |
| VCCIO1 | | | | | | | | | | | |
| VCCIO1 | | | | | | | | | | | |
| VCCIO8 | | | | | AF4 | AF4 | Y15 | AC17 | | | |
| VCCIO8 | | | | | AF11 | AF11 | AH17 | AM21 | | | |
| VCCIO8 | | | | | V11 | V11 | AH27 | AM30 | | | |
| VCCIO8 | | | | | V12 | V12 | | | | | |
| VCCIO8 | | | | | | | | | | | |
| VCCIO8 | | | | | | | | | | | |
| VCCIO8 | | | | | | | | | | | |
| VCCIO8 | | | | | | | | | | | |
| VCCIO8 | | | | | | | | | | | |

**Table 3–1. Pin List for the Stratix EP1S25 Device (Part 39 of 51)**

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | | | |
| VCCIO8 | | | | | | | | | | | |
| VCCIO7 | | | | | V15 | V15 | Y14 | AC16 | | | |
| VCCIO7 | | | | | V16 | V16 | AH2 | AM12 | | | |
| VCCIO7 | | | | | AF16 | AF16 | AH12 | AM3 | | | |
| VCCIO7 | | | | | AF23 | AF23 | | | | | |
| VCCIO7 | | | | | | | | | | | |
| VCCIO7 | | | | | | | | | | | |
| VCCIO7 | | | | | | | | | | | |
| VCCIO7 | | | | | | | | | | | |
| VCCIO7 | | | | | | | | | | | |
| VCCIO7 | | | | | | | | | | | |
| VCCIO6 | | | | | T18 | T18 | R9 | AA1 | | | |
| VCCIO6 | | | | | AC26 | AC26 | U1 | AK1 | | | |
| VCCIO6 | | | | | T26 | T26 | AG1 | AK2 | | | |
| VCCIO6 | | | | | | | | U10 | | | |
| VCCIO6 | | | | | | | | | | | |
| VCCIO6 | | | | | | | | | | | |
| VCCIO6 | | | | | | | | | | | |
| VCCIO6 | | | | | | | | | | | |
| VCCIO6 | | | | | | | | | | | |
| VCCIO6 | | | | | | | | | | | |
| VCCIO6 | | | | | | | | | | | |

**Table 3–1. Pin List for the Stratix EP1S25 Device (Part 40 of 51)**

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| VCCIO5 | | | | | L26 | L26 | B1 | C1 | | | |
| VCCIO5 | | | | | L18 | L18 | M1 | C2 | | | |
| VCCIO5 | | | | | D26 | D26 | P9 | M1 | | | |
| VCCIO5 | | | | | | | | T10 | | | |
| VCCIO5 | | | | | | | | | | | |
| VCCIO5 | | | | | | | | | | | |
| VCCIO5 | | | | | | | | | | | |
| VCCIO5 | | | | | | | | | | | |
| VCCIO5 | | | | | | | | | | | |
| VCCIO5 | | | | | | | | | | | |
| VCCIO5 | | | | | | | | | | | |
| VCCIO4 | | | | | A23 | A23 | A2 | A12 | | | |
| VCCIO4 | | | | | A16 | A16 | A12 | A3 | | | |
| VCCIO4 | | | | | J15 | J15 | J14 | K16 | | | |
| VCCIO4 | | | | | J16 | J16 | | | | | |
| VCCIO4 | | | | | | | | | | | |
| VCCIO4 | | | | | | | | | | | |
| VCCIO4 | | | | | | | | | | | |
| VCCIO4 | | | | | | | | | | | |
| VCCIO4 | | | | | | | | | | | |
| VCCIO4 | | | | | | | | | | | |
| VCCIO3 | | | | | A4 | A4 | A17 | A21 | | | |

Table 3–1. Pin List for the Stratix EP1S25 Device (Part 41 of 51)

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed Note (1) |
| VCCIO3 | | | | | A11 | A11 | A27 | A30 | | | |
| VCCIO3 | | | | | J11 | J11 | J15 | K17 | | | |
| VCCIO3 | | | | | J12 | J12 | | | | | |
| VCCIO3 | | | | | | | | | | | |
| VCCIO3 | | | | | | | | | | | |
| VCCIO3 | | | | | | | | | | | |
| VCCIO3 | | | | | | | | | | | |
| VCCIO3 | | | | | | | | | | | |
| VCCIO3 | | | | | | | | | | | |
| VCCINT | | | | | K11 | K11 | M14 | M12 | | | |
| VCCINT | | | | | M15 | M15 | N11 | M14 | | | |
| VCCINT | | | | | P17 | P17 | N13 | M19 | | | |
| VCCINT | | | | | U10 | U10 | N15 | M21 | | | |
| VCCINT | | | | | K13 | K13 | N17 | N13 | | | |
| VCCINT | | | | | M17 | M17 | P12 | N15 | | | |
| VCCINT | | | | | R10 | R10 | P14 | N18 | | | |
| VCCINT | | | | | U12 | U12 | P16 | N20 | | | |
| VCCINT | | | | | K15 | K15 | R13 | P12 | | | |
| VCCINT | | | | | N10 | N10 | R15 | P14 | | | |
| VCCINT | | | | | R12 | R12 | R17 | P16 | | | |
| VCCINT | | | | | U14 | U14 | T12 | P17 | | | |
| VCCINT | | | | | K17 | K17 | T14 | P19 | | | |

Table 3–1. Pin List for the Stratix EP1S25 Device (Part 42 of 51)

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed Note (1) |
| VCCINT | | | | | N12 | N12 | T16 | P21 | | | |
| VCCINT | | | | | R14 | R14 | T18 | R13 | | | |
| VCCINT | | | | | U16 | U16 | U11 | R15 | | | |
| VCCINT | | | | | L10 | L10 | U13 | R18 | | | |
| VCCINT | | | | | N14 | N14 | U15 | R20 | | | |
| VCCINT | | | | | R16 | R16 | U17 | T14 | | | |
| VCCINT | | | | | L12 | L12 | V12 | T16 | | | |
| VCCINT | | | | | N16 | N16 | V16 | T17 | | | |
| VCCINT | | | | | T11 | T11 | | T19 | | | |
| VCCINT | | | | | L14 | L14 | | U14 | | | |
| VCCINT | | | | | P11 | P11 | | U16 | | | |
| VCCINT | | | | | T13 | T13 | | U17 | | | |
| VCCINT | | | | | L16 | L16 | | U19 | | | |
| VCCINT | | | | | P13 | P13 | | V13 | | | |
| VCCINT | | | | | T15 | T15 | | V15 | | | |
| VCCINT | | | | | M11 | M11 | | V18 | | | |
| VCCINT | | | | | P15 | P15 | | V20 | | | |
| VCCINT | | | | | T17 | T17 | | W14 | | | |
| VCCINT | | | | | M13 | M13 | | W16 | | | |
| VCCINT | | | | | | | | W17 | | | |
| VCCINT | | | | | | | | W19 | | | |
| VCCINT | | | | | | | | Y13 | | | |

**Table 3–1. Pin List for the Stratix EP1S25 Device (Part 43 of 51)**

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | | | |
| VCCINT | | | | | | | | Y15 | | | |
| VCCINT | | | | | | | | Y18 | | | |
| VCCINT | | | | | | | | Y20 | | | |
| GND | | | | | A13 | A13 | C3 | AA16 | | | |
| GND | | | | | B1 | B1 | C26 | AA17 | | | |
| GND | | | | | J17 | J17 | L14 | AC1 | | | |
| GND | | | | | L17 | L17 | L15 | AC32 | | | |
| GND | | | | | N17 | N17 | M15 | AL1 | | | |
| GND | | | | | P26 | P26 | N12 | AL2 | | | |
| GND | | | | | U11 | U11 | N14 | AL31 | | | |
| GND | | | | | V18 | V18 | N16 | AL32 | | | |
| GND | | | | | A14 | A14 | N18 | AM10 | | | |
| GND | | | | | B2 | B2 | P1 | AM2 | | | |
| GND | | | | | K10 | K10 | P11 | AM23 | | | |
| GND | | | | | M10 | M10 | P13 | AM31 | | | |
| GND | | | | | N18 | N18 | P15 | B1 | | | |
| GND | | | | | R11 | R11 | P17 | B2 | | | |
| GND | | | | | U13 | U13 | P18 | B31 | | | |
| GND | | | | | A2 | A2 | P28 | B32 | | | |
| GND | | | | | AF25 | AF25 | R1 | K1 | | | |
| GND | | | | | J14 | J14 | R11 | K32 | | | |
| GND | | | | | L15 | L15 | R12 | M13 | | | |

Table 3–1. Pin List for the Stratix EP1S25 Device (Part 44 of 51)

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | | | |
| GND | | | | | N15 | N15 | R14 | M15 | | | |
| GND | | | | | P18 | P18 | R16 | M16 | | | |
| GND | | | | | T16 | T16 | R18 | M17 | | | |
| GND | | | | | V17 | V17 | AA16 | AD17 | | | |
| GND | | | | | A25 | A25 | AC15 | AF17 | | | |
| GND | | | | | B26 | B26 | G15 | J17 | | | |
| GND | | | | | K12 | K12 | H16 | H18 | | | |
| GND | | | | | M12 | M12 | R28 | M18 | | | |
| GND | | | | | N26 | N26 | T11 | M20 | | | |
| GND | | | | | R13 | R13 | T13 | N12 | | | |
| GND | | | | | U15 | U15 | T15 | N14 | | | |
| GND | | | | | AE1 | AE1 | T17 | N16 | | | |
| GND | | | | | G8 | G8 | U12 | N17 | | | |
| GND | | | | | K14 | K14 | U14 | N19 | | | |
| GND | | | | | M14 | M14 | U16 | N21 | | | |
| GND | | | | | P1 | P1 | U18 | P13 | | | |
| GND | | | | | R15 | R15 | V13 | P15 | | | |
| GND | | | | | U17 | U17 | V14 | P18 | | | |
| GND | | | | | AE26 | AE26 | V15 | P20 | | | |
| GND | | | | | H9 | H9 | V17 | R14 | | | |
| GND | | | | | K16 | K16 | AF3 | R16 | | | |
| GND | | | | | M16 | M16 | AF26 | R17 | | | |

*Table 3–1. Pin List for the Stratix EP1S25 Device (Part 45 of 51)*

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **672-Pin BGA** | **672-Pin FBGA** | **780-Pin FBGA** | **1020-Pin FBGA** | **DQS for x16** | **DQS for x32** | **DIFFIO Speed** *Note (1)* |
| GND | | | | | P9 | P9 | AG2 | R19 | | | |
| GND | | | | | R17 | R17 | AG27 | T12 | | | |
| GND | | | | | V9 | V9 | AH14 | T13 | | | |
| GND | | | | | AF2 | AF2 | AH15 | T15 | | | |
| GND | | | | | H17 | H17 | | T18 | | | |
| GND | | | | | K18 | K18 | | T20 | | | |
| GND | | | | | N1 | N1 | | T21 | | | |
| GND | | | | | P10 | P10 | | U12 | | | |
| GND | | | | | T10 | T10 | | U13 | | | |
| GND | | | | | V10 | V10 | | U15 | | | |
| GND | | | | | AF13 | AF13 | | U18 | | | |
| GND | | | | | J9 | J9 | | U20 | | | |
| GND | | | | | L11 | L11 | | U21 | | | |
| GND | | | | | N9 | N9 | | V14 | | | |
| GND | | | | | P12 | P12 | | V16 | | | |
| GND | | | | | T12 | T12 | | V17 | | | |
| GND | | | | | V13 | V13 | | V19 | | | |
| GND | | | | | AF14 | AF14 | | W13 | | | |
| GND | | | | | J10 | J10 | | W15 | | | |
| GND | | | | | L13 | L13 | | W18 | | | |
| GND | | | | | N11 | N11 | | W20 | | | |
| GND | | | | | P14 | P14 | | Y14 | | | |

Table 3–1. Pin List for the Stratix EP1S25 Device (Part 46 of 51)

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | | | |
| GND | | | | | T14 | T14 | | Y16 | | | |
| GND | | | | | V14 | V14 | | Y17 | | | |
| GND | | | | | J13 | J13 | | Y19 | | | |
| GND | | | | | N13 | N13 | | | | | |
| GND | | | | | P16 | P16 | | | | | |
| GND | | | | | C13 | C13 | | | | | |
| GND | | | | | AC13 | AC13 | | | | | |
| GND | | | | | | | | | | | |
| GND | | | | | | | | | | | |
| GND | | | | | | | | | | | |
| GND | | | | | | | | | | | |
| GND | | | | | | | | | | | |
| GND | | | | | | | | | | | |
| GND | | | | | | | | | | | |
| GND | | | | | | | | | | | |
| GND | | | | | | | A14 | A10 | | | |
| GND | | | | | | | A15 | A2 | | | |
| GND | | | | | | | B2 | A23 | | | |
| GND | | | | | | | B27 | A31 | | | |
| No connection | | | | | | | P19 | AA11 | | | |
| No connection | | | | | | | E5 | AB23 | | | |
| No connection | | | | | | | E26 | AE16 | | | |

**Table 3–1. Pin List for the Stratix EP1S25 Device (Part 47 of 51)**

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| No connection | | | | | | | E25 | AG25 | | | |
| No connection | | | | | | | D26 | AH16 | | | |
| No connection | | | | | | | D25 | AJ3 | | | |
| No connection | | | | | | | AC26 | D32 | | | |
| No connection | | | | | | | AC25 | E30 | | | |
| No connection | | | | | | | AD26 | F30 | | | |
| No connection | | | | | | | AD25 | K10 | | | |
| No connection | | | | | | | AC3 | N22 | | | |
| No connection | | | | | | | AD3 | W11 | | | |
| No connection | | | | | | | AC4 | AB5 | | | |
| No connection | | | | | | | AD4 | AC11 | | | |
| No connection | | | | | | | E3 | AG5 | | | |
| No connection | | | | | | | E4 | AH1 | | | |
| No connection | | | | | | | D3 | AH31 | | | |
| No connection | | | | | | | D4 | D1 | | | |
| No connection | | | | | | | | E4 | | | |
| No connection | | | | | | | | F4 | | | |
| No connection | | | | | | | | G25 | | | |
| No connection | | | | | | | | L28 | | | |
| No connection | | | | | | | | R21 | | | |
| No connection | | | | | | | | Y11 | | | |
| No connection | | | | | | | | AA22 | | | |

Table 3–1. Pin List for the Stratix EP1S25 Device (Part 48 of 51)

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| No connection | | | | | | | | AB29 | | | |
| No connection | | | | | | | | AF11 | | | |
| No connection | | | | | | | | AG27 | | | |
| No connection | | | | | | | | AH29 | | | |
| No connection | | | | | | | | AJ31 | | | |
| No connection | | | | | | | | E2 | | | |
| No connection | | | | | | | | E32 | | | |
| No connection | | | | | | | | G8 | | | |
| No connection | | | | | | | | L5 | | | |
| No connection | | | | | | | | P22 | | | |
| No connection | | | | | | | | W21 | | | |
| No connection | | | | | | | | AB10 | | | |
| No connection | | | | | | | | AD11 | | | |
| No connection | | | | | | | | AG8 | | | |
| No connection | | | | | | | | AH3 | | | |
| No connection | | | | | | | | AJ1 | | | |
| No connection | | | | | | | | D3 | | | |
| No connection | | | | | | | | E16 | | | |
| No connection | | | | | | | | F6 | | | |
| No connection | | | | | | | | H10 | | | |
| No connection | | | | | | | | M11 | | | |
| No connection | | | | | | | | U22 | | | |

*Table 3–1. Pin List for the Stratix EP1S25 Device (Part 49 of 51)*

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **672-Pin BGA** | **672-Pin FBGA** | **780-Pin FBGA** | **1020-Pin FBGA** | **DQS for x16** | **DQS for x32** | **DIFFIO Speed** *Note (1)* |
| No connection | | | | | | | | Y21 | | | |
| No connection | | | | | | | | AA13 | | | |
| No connection | | | | | | | | AB28 | | | |
| No connection | | | | | | | | AE22 | | | |
| No connection | | | | | | | | AG26 | | | |
| No connection | | | | | | | | AH21 | | | |
| No connection | | | | | | | | AJ30 | | | |
| No connection | | | | | | | | E1 | | | |
| No connection | | | | | | | | E31 | | | |
| No connection | | | | | | | | G7 | | | |
| No connection | | | | | | | | L4 | | | |
| No connection | | | | | | | | P11 | | | |
| No connection | | | | | | | | W12 | | | |
| No connection | | | | | | | | AB9 | | | |
| No connection | | | | | | | | AD10 | | | |
| No connection | | | | | | | | AG7 | | | |
| No connection | | | | | | | | AH2 | | | |
| No connection | | | | | | | | AH32 | | | |
| No connection | | | | | | | | D2 | | | |
| No connection | | | | | | | | E12 | | | |
| No connection | | | | | | | | F5 | | | |
| No connection | | | | | | | | G26 | | | |

Table 3–1. Pin List for the Stratix EP1S25 Device (Part 50 of 51)

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | | | |
| No connection | | | | | | | | L29 | | | |
| No connection | | | | | | | | T11 | | | |
| No connection | | | | | | | | Y12 | | | |
| No connection | | | | | | | | AB4 | | | |
| No connection | | | | | | | | AC10 | | | |
| No connection | | | | | | | | AF16 | | | |
| No connection | | | | | | | | AG28 | | | |
| No connection | | | | | | | | AH30 | | | |
| No connection | | | | | | | | AJ32 | | | |
| No connection | | | | | | | | E3 | | | |
| No connection | | | | | | | | F3 | | | |
| No connection | | | | | | | | G11 | | | |
| No connection | | | | | | | | L10 | | | |
| No connection | | | | | | | | R11 | | | |
| No connection | | | | | | | | W22 | | | |
| No connection | | | | | | | | AB12 | | | |
| No connection | | | | | | | | AE10 | | | |
| No connection | | | | | | | | AG16 | | | |
| No connection | | | | | | | | AH4 | | | |
| No connection | | | | | | | | AJ2 | | | |
| No connection | | | | | | | | D30 | | | |
| No connection | | | | | | | | E17 | | | |

**Table 3–1. Pin List for the Stratix EP1S25 Device (Part 51 of 51)**

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 672-Pin BGA | 672-Pin FBGA | 780-Pin FBGA | 1020-Pin FBGA | | | |
| No connection | | | | | | | | F11 | | | |
| No connection | | | | | | | | H15 | | | |
| No connection | | | | | | | | M22 | | | |
| No connection | | | | | | | | V12 | | | |
| No connection | | | | | | | | Y22 | | | |
| No connection | | | | | | | | AH6 | | | |
| No connection | | | | | | | | D31 | | | |
| No connection | | | | | | | | E27 | | | |
| No connection | | | | | | | | F28 | | | |
| No connection | | | | | | | | H16 | | | |
| No connection | | | | | | | | M23 | | | |
| No connection | | | | | | | | V22 | | | |
| No connection | | | | | | | | E29 | | | |
| No connection | | | | | | | | F29 | | | |
| No connection | | | | | | | | J10 | | | |
| No connection | | | | | | | | N11 | | | |

*Note to Table 3–1:*

(1) The wire bond and flip-chip packages have different data rates for the high speed differential I/O channels. Table 3–2 shows the data rates as supported for each package.

**Table 3–2. High Speed Differential I/O Channel Data Rates**

| Package | Package Type | High Speed Differential I/O Channel Performance (DIFFIO Speed) | | Units |
|---|---|---|---|---|
| | | High | Low | |
| 672-pin BGA | wire bond | 462 | N/A | Mbps |
| 672-pin FineLine BGA | wire bond | 462 | N/A | Mbps |
| 780-pin FineLine BGA | flip chip | 840 | N/A | Mbps |
| 1020-pin FineLine BGA | flip chip | 840 | N/A | Mbps |

## Pin Definitions

Table 3–3 shows pin definitions for the EP1S25 device.

*Table 3–3. Pin Definitions for the EP1S25 Device (Part 1 of 5)*

| Pin Name | Pin Type (1st, 2nd, & 3rd Function) | Pin Description |
|---|---|---|
| **Supply and Reference Pins** | | |
| VREF[1..4]B[1..8] | Input | Input reference voltage for each I/O bank. If a bank is used for a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for that bank. All of the VREF pins within a bank are shorted together. Each VREF pin can support up to 20 inputs on each side. If VREF pins are not used, designers should connect them to either VCC or Gnd. |
| VCCIO[1..8] | Power | These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards. VCCIO also supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5-V, 1.8-V, 2.5-V, 3.3-V PCI, and 3.3-V PCI-X I/O standards. |
| VCCINT | Power | These are internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVDS, LVPECL, 3.3-V PCML, HyperTransportô technology, differential HSTL, GTL, GTL+, HSTL, SSTL, CTT, and 3.3-V AGP I/O standards. |
| VCC_PLL5_OUTA | Power | External clock output buffer power for PLL5 clock outputs PLL5_OUT[1..0]. The designer must connect this pin to the VCCIO of bank 9. |
| VCC_PLL5_OUTB | Power | External clock output buffer power for PLL5 clock outputs PLL5_OUT[3..2]. The designer must connect this pin to the VCCIO of bank 10. |
| VCC_PLL6_OUTA | Power | External clock output buffer power for PLL6 clock outputs PLL6_OUT[1..0]. The designer must connect this pin to the VCCIO of bank 11. |
| VCC_PLL6_OUTB | Power | External clock output buffer power for PLL6 clock outputs PLL6_OUT[3..2]. The designer must connect this pin to the VCCIO of bank 12. |
| VCCA_PLL[1..12] | Power | Analog power for PLLs[1..12]. The designer must connect this pin to 1.5 V, even if the PLL is not used. |
| GNDA_PLL[1..12] | Ground | Analog ground for PLLs[1..12]. The designer can connect this pin to the GND plane on the board. |
| VCCG_PLL[1..12] | Power | Guard ring power for PLLs[1..12]. The designer must connect this pin to 1.5 V, even if the PLL is not used. |
| GNDG_PLL[1..12] | Ground | Guard ring ground for PLLs[1..12]. The designer can connect this pin to the GND plane on the board. |

*Table 3–3. Pin Definitions for the EP1S25 Device (Part 2 of 5)*

| Pin Name | Pin Type (1st, 2nd, & 3rd Function) | Pin Description |
|---|---|---|
| **Dedicated & Configuration/JTAG Pins** | | |
| CONF_DONE | Bidirectional (open-drain) | This is a dedicated configuration status pin; it is not available as a user I/O pin. |
| nSTATUS | Bidirectional (open-drain) | This is a dedicated configuration status pin; it is not available as a user I/O pin. |
| nCONFIG | Input | Dedicated configuration control input. A low transition resets the target device; a low-to-high transition begins configuration. All I/O pins tri-state when nCONFIG is driven low. |
| DCLK | Input | Clock input used to clock configuration data from an external source into the Stratix device. This is a dedicated pin used for configuration. |
| nIO_PULLUP | Input | IF nIO_PULLUP is driven high during configuration, the weak pull-ups on all user I/O pins are disabled. If driven low, the weak pull-ups are enabled during configuration. nIO_PULLUP can be pulled up to either 1.5, 1.8, 2.5, or 3.3 V. |
| PORSEL | Input | Dedicated input pin used to select POR delay times of 2 ms or 100 ms during powerup. When PORSEL is connected to ground, the POR time is 100 ms. When PORSEL is connected to 3.3 V, the POR time is 2 ms. |
| VCCSEL | Input | VCCSEL is used to select which input buffer is used on all configuration pins. VCCSEL will control whether the 3.3-/2.5-V input buffer or the 1.8-/1.5-V input buffer is used. A "0" means 3.3/2.5 V and a "1" means 1.8-/1.5 V. At powerup, VCCSEL accepts 3.3V and 2.5V TTL Levels. VCCSEL affects the following pins: TDI, TMS, TCK, TRST, MSEL0, MSEL1, MSEL2, nCONFIG, nCE, DCLK, CONF_DONE, nSTATUS, and PLL_ENA. |
| nCE | Input | Active-low chip enables. Dedicated chip enable input used to detect which device is active in a chain of devices. When nCE is low, the device is enabled. When nCE is high, the device is disabled. |
| nCEO | Output | Output that drives low when device configuration is complete. During multi-device configuration, this pin feeds a subsequent deviceís nCE pin. |
| TMS | Input | This is a dedicated JTAG input pin. |
| TDI | Input | This is a dedicated JTAG input pin. |
| TCK | Input | This is a dedicated JTAG input pin. |

*Table 3–3. Pin Definitions for the EP1S25 Device (Part 3 of 5)*

| Pin Name | Pin Type (1st, 2nd, & 3rd Function) | Pin Description |
|---|---|---|
| TDO | Output | This is a dedicated JTAG input pin. |
| TRST | Input | This is a dedicated JTAG input pin. Active low input, used to asynchronously reset the JTAG boundary scan circuit. |
| MSEL[2..0] | Input | Dedicated mode select control pins that set the configuration mode for the device. |
| TEMPDIODEp | Input | Pin used in conjunction with the temperature sensing diode (bias-high input) inside the Stratix device. If the temperature sensing diode is not used then connect this pin to GND. |
| TEMPDIODEn | Input | Pin used in conjunction with the temperature sensing diode (bias-low input) inside the Stratix device. If the temperature sensing diode is not used then connect this pin to GND. |
| **Clock and PLL Pins** | | |
| PLL_ENA | Input | Dedicated input pin that drives the optional pllena port of all or a set of PLLs. If a PLL uses the pllena port, drive the PLL_ENA pin low to reset all PLLs including the counters to their default state. If VCCSEL = 0, then you must drive the PLL_ENA with a 3.3/2.5 V signal to enable the PLLs. If VCCSEL = 1, connect PLL_ENA to 1.8/1.5 V to enable the PLLs. |
| FCLK[7..0] | Bidirectional | Optional fast regional clock pins. FCLK pins can also be used as type input, output, or as bidirectional pins. |
| CLK[15..0]p | Input | Dedicated global clock inputs 0 to 15. |
| CLK[15..0]n | I/O, Input | Optional negative terminal input for differential global clock input. |
| PLL6_OUT[3..0]p | I/O, Output | Optional external clock outputs [3..0] from enhanced PLL 6. These pins can be differential (four output pin pairs) or single ended (eight clock outputs from PLL6). |
| PLL6_OUT[3..0]n | I/O, Output | Optional negative terminal for external clock outputs [3..0] from PLL6. If the clock outputs are single ended, then each pair of pins (i.e., PLL6_OUT0p and PLL6_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase. |
| PLL5_OUT[3..0]p | I/O, Output | Optional external clock outputs [3..0] from enhanced PLL 5. These pins can be differential (four output pin pairs) or single ended (eight clock outputs from PLL5). |
| PLL5_OUT[3..0]n | I/O, Output | Optional negative terminal for external clock outputs [3..0] from PLL 5. If the clock outputs are single ended, then each pair of pins (i.e., PLL5_OUT0p and PLL5_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase. |

*Table 3–3. Pin Definitions for the EP1S25 Device (Part 4 of 5)*

| Pin Name | Pin Type (1st, 2nd, & 3rd Function) | Pin Description |
|---|---|---|
| **Optional/Dual-Purpose Pins** | | |
| DATA0 | I/O, Input | Dual-purpose configuration data input pin. Can be used as an I/O pin after configuration is complete. |
| DIFFIO_TX[0..151]n | I/O, Output | This pin can be used as the complementary signal of the differential inputs and outputs. If not used for the differential pair, these pins are regular I/O pins. Pins with an n suffix carry the negative signal for the differential channel. Pins with a p suffix carry the positive signal for the differential channel. |
| PLL5_FBp | I/O, Input | External feedback input pin for PLL5. This pin can be used as a user I/O pin if external feedback mode is not used. |
| PLL5_FBn | I/O, Input | Negative terminal input for external feedback input PLL5_FBp |
| PLL6_FBp | I/O, Input | External feedback input pin for PLL6 |
| PLL6_FBn | I/O, Input | Negative terminal input for external feedback input PLL6_FBp |
| INIT_DONE | I/O, Output | This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration. |
| DATA[7..1] | I/O, Input | Dual-purpose configuration input data pins. These pins can be used for configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration. |
| nRS | I/O, Input | Read strobe input pin. This pin can be used as a user I/O pin after configuration. |
| DEV_CLRn | I/O, Input | Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as defined in the users design. |
| DEV_OE | I/O, Input | Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design. |
| CLKUSR | I/O, Input | Optional user-supplied clock input. Synchronizes the initialization of one or more devices. This pin can be used as a user I/O pin after configuration. |
| RDYnBSY | I/O, Output | Ready not busy output. A high output indicates that the target device is ready to accept another data byte. A low output indicates that the target device is not ready to receive another data byte. This pin can be used as a user I/O pin after configuration |

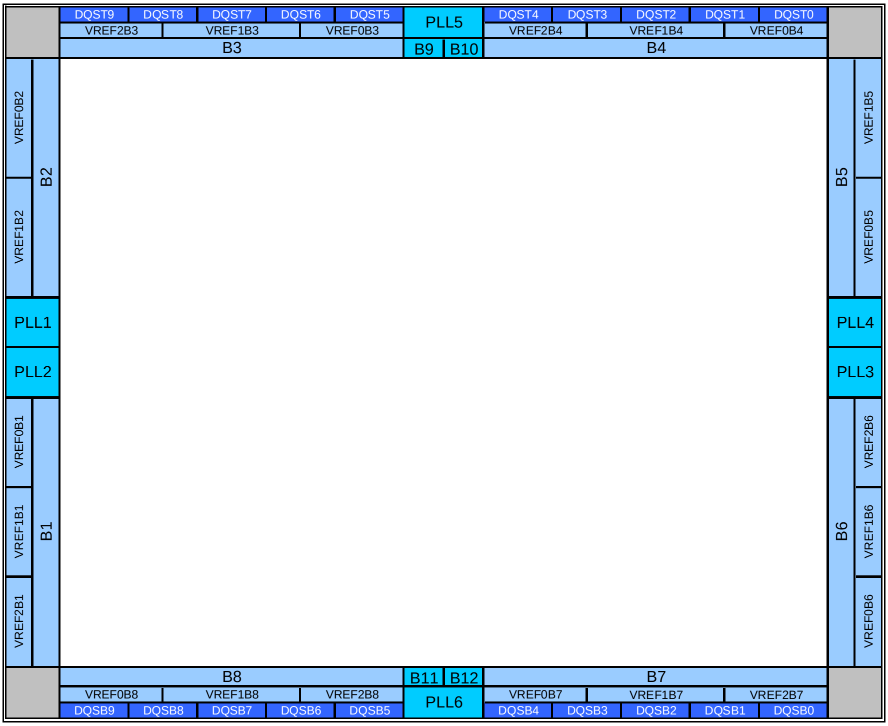
*Table 3–3. Pin Definitions for the EP1S25 Device (Part 5 of 5)*

| Pin Name | Pin Type (1st, 2nd, & 3rd Function) | Pin Description |
|---|---|---|
| nCS,CS | I/O, Input | These are chip-select inputs that enable the Stratix device in the passive parallel asynchronous configuration mode. Drive nCS low and CS high to target a device for configuration. If a design requires an active high enable, use the CS pin and drive the nCS pin low. If a design requires an active low enable, use the nCS pin and drive the CS pin high. Configuration will be paused when either signal is inactive. Hold the nCS and CS pins active during configuration and initialization. The design can use these pins as user I/O pins after configuration. |
| nWS | I/O, Input | Active-low write strobe input to latch a byte of data on the DATA pins. This pin can be used as a user I/O pin after configuration. |
| PGM[2..0] | I/O, Output | These output pins control one of eight pages in the EPC16 configuration device when using remote update or local update configuration modes. When not using remote update or local update configuration modes, these pins are user I/O pins. |
| RUP[8..1] | I/O, Input | Reference pins for banks 8 to 1. The external precision resistors $R_{UP}$ must be connected to the designated RUP pin on that I/O bank. If not required, these pins are regular I/O pins. |
| RDN[8..1] | I/O, Input | Reference pins for banks 8 to 1. The external precision resistors RDN must be connected to the designated RDN pin on that I/O bank. If not required, these pins are regular I/O pins. |
| RUnLU | I/O, Input | Input control pin to select remote update or local update modes. If MSEL2 = 1, this is a input control pin to select remote update (RUnLU =1) or local update (RUnLU =0) modes. If MSEL2 = 0, the RUnLU pin is a user I/O pin. |

## PLL & Bank Diagram

Figure 3–1 shows the PLL and bank locations for the EP1S25 device.

*Figure 3–1. PLL and Bank Diagram Notes (1), (2)*



*Notes for Figure 3–1:*

(1) This is a top view of the silicon die. For flip chip packages the die is mounted upside down in the package.

(2) This is a pictoral representation only, to give an idea of placement on the device. Refer to the pinlist and the Quartus II software for exact locations.

## Fast PLL to High-Speed I/O Connections

Table 3–4 shows the number of shows the number of high-speed differential I/O channels that can be driven by each Fast PLL for the EP1S25 device.

*Table 3–4. Fast PLL Connections for the EP1S25 Device*

| Device | Pin Count | FAST PLL Source Location | Number of Rx Channels *(1) (5)* | Number of Tx Channels *(2) (5)* | Number of Overlapped Rx Channels *(3)* | Number of Overlapped Tx Channels *(4)* |
|---|---|---|---|---|---|---|
| EP1S25 | 672 | PLL1 | 0/14 | 0/14 | | |
| | | PLL2 | 0/15 | 0/14 | | |
| | | PLL3 | 0/15 | 0/14 | | |
| | | PLL4 | 0/14 | 0/14 | | |
| | 780 | PLL1 | 17/0 | 18/0 | | |
| | | PLL2 | 16/0 | 17/0 | | |
| | | PLL3 | 16/0 | 17/0 | | |
| | | PLL4 | 17/0 | 18/0 | | |
| | 1020 | PLL1 | 19/0 | 19/0 | | |
| | | PLL2 | 20/0 | 20/0 | | |
| | | PLL3 | 20/0 | 20/0 | | |
| | | PLL4 | 19/0 | 19/0 | | |

*Notes for Table 3–4:*

(1) This is the total number of Rx channels that the PLL listed in the "FAST PLL Source location" column can drive.

(2) This is the total number of Tx channels that the PLL listed in the "FAST PLL Source location" column can drive.

(3) This is the number of Rx channels that can be driven by the PLL listed in the "FAST PLL Source location" that could alternatively be driven by the other adjacent FAST PLL.

(4) This is the number of Tx channels that can be driven by the PLL listed in the "FAST PLL Source location" that could alternatively be driven by the other adjacent FAST PLL.

(5) The counts are reported in the format of (high speed channels)/(low speed channels).

# 4. Stratix EP1S30 Device Pin Information

S5V3004-1.0

## Introduction

The following tables contain pin information for the Stratix EP1S30 device, organized into the following sections:

# Pin List

Table 4–1 shows the complete pin list for the EP1S30 device:

*Table 4–1. Pin List for the Stratix EP1S30 Device (Part 1 of 52)*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **780-Pin FineLine BGA** | **956-Pin BGA** | **1020-Pin FineLine BGA** | | | |
| VCCINT | | | | | VCC | VCC | VCC | | | |
| VCCA_PLL7 | | | | | | L23 | D31 | | | |
| GND | | | | | GND | GND | GND | | | |
| GNDA_PLL7 | | | | | | M23 | D32 | | | |
| VCCG_PLL7 | | | | | | J23 | D30 | | | |
| GNDG_PLL7 | | | | | | K23 | E30 | | | |
| FPLL7CLKp | | | B2 | VREF0B2 | | E31 | L29 | | | |
| FPLL7CLKn | | | B2 | VREF0B2 | | D31 | L28 | | | |
| IO | | | B2 | VREF0B2 | | | | | | |
| IO | | | B2 | VREF0B2 | | | | | | |
| IO | DIFFIO_RX40p | | B2 | VREF0B2 | | | E32 | | | LOW |
| IO | DIFFIO_RX40n | | B2 | VREF0B2 | | | E31 | | | LOW |
| IO | DIFFIO_TX40p | | B2 | VREF0B2 | | K24 | G25 | | | HIGH |
| IO | DIFFIO_TX40n | | B2 | VREF0B2 | | J24 | G26 | | | HIGH |
| IO | DIFFIO_RX39p | | B2 | VREF0B2 | | F28 | F29 | | | HIGH |
| IO | DIFFIO_RX39n | | B2 | VREF0B2 | | G28 | F30 | | | HIGH |
| IO | DIFFIO_TX39p | | B2 | VREF0B2 | | K25 | G28 | | | HIGH |
| IO | DIFFIO_TX39n | | B2 | VREF0B2 | | J25 | G27 | | | HIGH |
| IO | DIFFIO_RX38p | | B2 | VREF0B2 | | J28 | F31 | | | HIGH |

**Table 4–1. Pin List for the Stratix EP1S30 Device (Part 2 of 52)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_RX38n | | B2 | VREF0B2 | | H28 | F32 | | | HIGH |
| IO | DIFFIO_TX38p | | B2 | VREF0B2 | F24 | H24 | H28 | | | HIGH |
| IO | DIFFIO_TX38n | | B2 | VREF0B2 | F23 | G24 | H27 | | | HIGH |
| VREF0B2 | | | B2 | VREF0B2 | E24 | L22 | F27 | | | |
| IO | DIFFIO_RX37p | | B2 | VREF0B2 | | D29 | G29 | | | HIGH |
| IO | DIFFIO_RX37n | | B2 | VREF0B2 | | E29 | G30 | | | HIGH |
| IO | DIFFIO_TX37p | | B2 | VREF0B2 | G23 | H25 | J27 | | | HIGH |
| IO | DIFFIO_TX37n | | B2 | VREF0B2 | G24 | G25 | J28 | | | HIGH |
| IO | DIFFIO_RX36p | | B2 | VREF0B2 | C27 | F29 | H30 | | | HIGH |
| IO | DIFFIO_RX36n | | B2 | VREF0B2 | C28 | G29 | H29 | | | HIGH |
| IO | DIFFIO_TX36p | | B2 | VREF0B2 | H24 | K26 | H25 | | | HIGH |
| IO | DIFFIO_TX36n | | B2 | VREF0B2 | H23 | L26 | H26 | | | HIGH |
| IO | DIFFIO_RX35p | | B2 | VREF0B2 | D27 | H29 | G31 | | | HIGH |
| IO | DIFFIO_RX35n | | B2 | VREF0B2 | D28 | J29 | G32 | | | HIGH |
| IO | DIFFIO_TX35p | | B2 | VREF0B2 | H22 | J26 | J25 | | | HIGH |
| IO | DIFFIO_TX35n | | B2 | VREF0B2 | H21 | H26 | J26 | | | HIGH |
| IO | DIFFIO_RX34p | | B2 | VREF0B2 | E27 | D30 | H31 | | | HIGH |
| IO | DIFFIO_RX34n | | B2 | VREF0B2 | E28 | E30 | H32 | | | HIGH |
| IO | DIFFIO_TX34p | | B2 | VREF0B2 | J24 | G26 | K28 | | | HIGH |
| IO | DIFFIO_TX34n | | B2 | VREF0B2 | J23 | F26 | K27 | | | HIGH |
| IO | DIFFIO_RX33p | | B2 | VREF1B2 | F25 | F30 | J29 | | | HIGH |

*Table 4–1. Pin List for the Stratix EP1S30 Device (Part 3 of 52)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_RX33n | | B2 | VREF1B2 | F26 | G30 | J30 | | | HIGH |
| IO | DIFFIO_TX33p | | B2 | VREF1B2 | K23 | F27 | K26 | | | HIGH |
| IO | DIFFIO_TX33n | | B2 | VREF1B2 | K24 | G27 | K25 | | | HIGH |
| IO | DIFFIO_RX32p | | B2 | VREF1B2 | F27 | H30 | K30 | | | HIGH |
| IO | DIFFIO_RX32n | | B2 | VREF1B2 | F28 | J30 | K29 | | | HIGH |
| IO | DIFFIO_TX32p | | B2 | VREF1B2 | J21 | H27 | L27 | | | HIGH |
| IO | DIFFIO_TX32n | | B2 | VREF1B2 | J22 | J27 | L26 | | | HIGH |
| IO | DIFFIO_RX31p | | B2 | VREF1B2 | G26 | F31 | J32 | | | HIGH |
| IO | DIFFIO_RX31n | | B2 | VREF1B2 | G25 | G31 | J31 | | | HIGH |
| IO | DIFFIO_TX31p | | B2 | VREF1B2 | K21 | K27 | M26 | | | HIGH |
| IO | DIFFIO_TX31n | | B2 | VREF1B2 | K22 | L27 | M27 | | | HIGH |
| IO | DIFFIO_RX30p | | B2 | VREF1B2 | G27 | H31 | K31 | | | HIGH |
| IO | DIFFIO_RX30n | | B2 | VREF1B2 | G28 | J31 | L32 | | | HIGH |
| IO | DIFFIO_TX30p | | B2 | VREF1B2 | L22 | L24 | M24 | | | HIGH |
| IO | DIFFIO_TX30n | | B2 | VREF1B2 | L21 | M24 | M25 | | | HIGH |
| VREF1B2 | | | B2 | VREF1B2 | K20 | M22 | L25 | | | |
| IO | DIFFIO_RX29p/RUP2 | | B2 | VREF1B2 | H26 | K28 | M28 | | | HIGH |
| IO | DIFFIO_RX29n/RDN2 | | B2 | VREF1B2 | H25 | K29 | M29 | | | HIGH |
| IO | DIFFIO_TX29p | | B2 | VREF1B2 | L23 | L25 | N24 | | | HIGH |
| IO | DIFFIO_TX29n | | B2 | VREF1B2 | L24 | M25 | N23 | | | HIGH |
| IO | DIFFIO_RX28p | | B2 | VREF1B2 | H27 | M28 | L30 | | | HIGH |

*Table 4–1. Pin List for the Stratix EP1S30 Device (Part 4 of 52)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_RX28n | | B2 | VREF1B2 | H28 | L28 | L31 | | | HIGH |
| IO | DIFFIO_TX28p | | B2 | VREF1B2 | L20 | P24 | N27 | | | HIGH |
| IO | DIFFIO_TX28n | | B2 | VREF1B2 | L19 | N24 | N28 | | | HIGH |
| IO | DIFFIO_RX27p | | B2 | VREF1B2 | J25 | M29 | M31 | | | HIGH |
| IO | DIFFIO_RX27n | | B2 | VREF1B2 | J26 | L29 | M30 | | | HIGH |
| IO | DIFFIO_TX27p | | B2 | VREF1B2 | M22 | N25 | P23 | | | HIGH |
| IO | DIFFIO_TX27n | | B2 | VREF1B2 | M21 | P25 | P24 | | | HIGH |
| IO | DIFFIO_RX26p | | B2 | VREF1B2 | J27 | P28 | N29 | | | HIGH |
| IO | DIFFIO_RX26n | | B2 | VREF1B2 | J28 | N28 | N30 | | | HIGH |
| IO | DIFFIO_TX26p | | B2 | VREF1B2 | M24 | M26 | N25 | | | HIGH |
| IO | DIFFIO_TX26n | | B2 | VREF1B2 | M23 | N26 | N26 | | | HIGH |
| IO | DIFFIO_RX25p | | B2 | VREF2B2 | K26 | N29 | N31 | | | HIGH |
| IO | DIFFIO_RX25n | | B2 | VREF2B2 | K25 | P29 | N32 | | | HIGH |
| IO | DIFFIO_TX25p | | B2 | VREF2B2 | M20 | M27 | P28 | | | HIGH |
| IO | DIFFIO_TX25n | | B2 | VREF2B2 | M19 | N27 | P27 | | | HIGH |
| IO | DIFFIO_RX24p | | B2 | VREF2B2 | K27 | L30 | P29 | | | HIGH |
| IO | DIFFIO_RX24n | | B2 | VREF2B2 | K28 | K30 | P30 | | | HIGH |
| IO | DIFFIO_TX24p | | B2 | VREF2B2 | N26 | P27 | R28 | | | HIGH |
| IO | DIFFIO_TX24n | | B2 | VREF2B2 | N25 | R27 | R27 | | | HIGH |
| IO | DIFFIO_RX23p | | B2 | VREF2B2 | L25 | N30 | P31 | | | HIGH |
| IO | DIFFIO_RX23n | | B2 | VREF2B2 | L26 | M30 | P32 | | | HIGH |

*Table 4–1. Pin List for the Stratix EP1S30 Device (Part 5 of 52)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_TX23p | | B2 | VREF2B2 | N24 | R26 | P25 | | | HIGH |
| IO | DIFFIO_TX23n | | B2 | VREF2B2 | N23 | P26 | P26 | | | HIGH |
| IO | DIFFIO_RX22p | | B2 | VREF2B2 | L27 | L31 | R32 | | | HIGH |
| IO | DIFFIO_RX22n | | B2 | VREF2B2 | L28 | K31 | R31 | | | HIGH |
| IO | DIFFIO_TX22p | | B2 | VREF2B2 | N22 | N23 | R23 | | | HIGH |
| IO | DIFFIO_TX22n | | B2 | VREF2B2 | N21 | P23 | R24 | | | HIGH |
| VREF2B2 | | | B2 | VREF2B2 | P19 | N22 | R21 | | | |
| IO | DIFFIO_RX21p | | B2 | VREF2B2 | M25 | R30 | R30 | | | HIGH |
| IO | DIFFIO_RX21n | | B2 | VREF2B2 | M26 | P30 | R29 | | | HIGH |
| IO | DIFFIO_TX21p | | B2 | VREF2B2 | N20 | T25 | R25 | | | HIGH |
| IO | DIFFIO_TX21n | | B2 | VREF2B2 | N19 | R25 | R26 | | | HIGH |
| IO | DIFFIO_RX20p | | B2 | VREF2B2 | M27 | P31 | T32 | | | HIGH |
| IO | DIFFIO_RX20n | | B2 | VREF2B2 | N28 | R31 | T31 | | | HIGH |
| IO | DIFFIO_TX20p | | B2 | VREF2B2 | | | M23 | | | LOW |
| IO | DIFFIO_TX20n | | B2 | VREF2B2 | | | M22 | | | LOW |
| CLK0n | | | B2 | VREF2B2 | N27 | R28 | T30 | | | |
| CLK0p | | | B2 | VREF2B2 | P27 | R29 | T29 | | | |
| IO | CLK1n | | B2 | VREF2B2 | P26 | T30 | T28 | | | |
| CLK1p | | | B2 | VREF2B2 | P25 | T31 | T27 | | | |
| VCCINT | | | | | | | | | | |
| VCCA_PLL1 | | | | | P23 | R24 | T25 | | | |

*Table 4–1. Pin List for the Stratix EP1S30 Device (Part 6 of 52)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| GND | | | | | | | | | | |
| GNDA_PLL1 | | | | | P24 | T24 | T26 | | | |
| VCCG_PLL1 | | | | | P21 | R22 | R22 | | | |
| GNDG_PLL1 | | | | | P22 | R23 | T22 | | | |
| VCCINT | | | | | | | | | | |
| VCCA_PLL2 | | | | | R23 | U24 | U25 | | | |
| GND | | | | | | | | | | |
| GNDA_PLL2 | | | | | R24 | V24 | U26 | | | |
| VCCG_PLL2 | | | | | R21 | U23 | U24 | | | |
| GNDG_PLL2 | | | | | R22 | V23 | T24 | | | |
| CLK2p | | | B1 | VREF0B1 | R27 | T29 | U31 | | | |
| CLK2n | | | B1 | VREF0B1 | T27 | T28 | U32 | | | |
| CLK3p | | | B1 | VREF0B1 | R25 | U29 | U29 | | | |
| IO | CLK3n | | B1 | VREF0B1 | R26 | U28 | U30 | | | |
| IO | DIFFIO_RX19p | | B1 | VREF0B1 | T28 | U31 | U28 | | | HIGH |
| IO | DIFFIO_RX19n | | B1 | VREF0B1 | U27 | V31 | U27 | | | HIGH |
| IO | DIFFIO_TX19p | | B1 | VREF0B1 | T21 | V25 | V26 | | | HIGH |
| IO | DIFFIO_TX19n | | B1 | VREF0B1 | T22 | U25 | V25 | | | HIGH |
| IO | DIFFIO_RX18p | | B1 | VREF0B1 | U26 | AB31 | V32 | | | HIGH |
| IO | DIFFIO_RX18n | | B1 | VREF0B1 | U25 | AA31 | V31 | | | HIGH |
| IO | DIFFIO_TX18p | | B1 | VREF0B1 | T19 | U26 | V28 | | | HIGH |

**Table 4–1. Pin List for the Stratix EP1S30 Device (Part 7 of 52)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_TX18n | | B1 | VREF0B1 | T20 | T26 | V27 | | | HIGH |
| VREF0B1 | | | B1 | VREF0B1 | R19 | V22 | V21 | | | |
| IO | DIFFIO_RX17p | | B1 | VREF0B1 | V27 | V30 | V30 | | | HIGH |
| IO | DIFFIO_RX17n | | B1 | VREF0B1 | V28 | U30 | V29 | | | HIGH |
| IO | DIFFIO_TX17p | | B1 | VREF0B1 | T23 | T27 | W25 | | | HIGH |
| IO | DIFFIO_TX17n | | B1 | VREF0B1 | T24 | U27 | W26 | | | HIGH |
| IO | DIFFIO_RX16p | | B1 | VREF0B1 | V26 | W30 | W32 | | | HIGH |
| IO | DIFFIO_RX16n | | B1 | VREF0B1 | V25 | Y30 | W31 | | | HIGH |
| IO | DIFFIO_TX16p | | B1 | VREF0B1 | T26 | V26 | W27 | | | HIGH |
| IO | DIFFIO_TX16n | | B1 | VREF0B1 | T25 | W26 | W28 | | | HIGH |
| IO | DIFFIO_RX15p | | B1 | VREF0B1 | W28 | AA30 | W30 | | | HIGH |
| IO | DIFFIO_RX15n | | B1 | VREF0B1 | W27 | AB30 | W29 | | | HIGH |
| IO | DIFFIO_TX15p | | B1 | VREF0B1 | U19 | W24 | V24 | | | HIGH |
| IO | DIFFIO_TX15n | | B1 | VREF0B1 | U20 | Y24 | V23 | | | HIGH |
| IO | DIFFIO_RX14p | | B1 | VREF0B1 | W26 | V29 | Y32 | | | HIGH |
| IO | DIFFIO_RX14n | | B1 | VREF0B1 | W25 | W29 | Y31 | | | HIGH |
| IO | DIFFIO_TX14p | | B1 | VREF0B1 | U24 | W25 | Y26 | | | HIGH |
| IO | DIFFIO_TX14n | | B1 | VREF0B1 | U23 | Y25 | Y25 | | | HIGH |
| IO | DIFFIO_RX13p | | B1 | VREF1B1 | Y28 | Y29 | Y30 | | | HIGH |
| IO | DIFFIO_RX13n | | B1 | VREF1B1 | Y27 | AA29 | Y29 | | | HIGH |
| IO | DIFFIO_TX13p | | B1 | VREF1B1 | U21 | Y26 | Y28 | | | HIGH |

*Table 4–1. Pin List for the Stratix EP1S30 Device (Part 8 of 52)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_TX13n | | B1 | VREF1B1 | U22 | AA26 | Y27 | | | HIGH |
| IO | DIFFIO_RX12p | | B1 | VREF1B1 | Y26 | V28 | AA31 | | | HIGH |
| IO | DIFFIO_RX12n | | B1 | VREF1B1 | Y25 | W28 | AA30 | | | HIGH |
| IO | DIFFIO_TX12p | | B1 | VREF1B1 | V19 | W23 | W23 | | | HIGH |
| IO | DIFFIO_TX12n | | B1 | VREF1B1 | V20 | Y23 | W24 | | | HIGH |
| IO | DIFFIO_RX11p | | B1 | VREF1B1 | AA28 | Y28 | AB31 | | | HIGH |
| IO | DIFFIO_RX11n | | B1 | VREF1B1 | AA27 | AA28 | AB30 | | | HIGH |
| IO | DIFFIO_TX11p | | B1 | VREF1B1 | V24 | V27 | Y23 | | | HIGH |
| IO | DIFFIO_TX11n | | B1 | VREF1B1 | V23 | W27 | Y24 | | | HIGH |
| IO | DIFFIO_RX10p/RUP1 | | B1 | VREF1B1 | AA25 | AB29 | AA28 | | | HIGH |
| IO | DIFFIO_RX10n/RDN1 | | B1 | VREF1B1 | AA26 | AB28 | AA29 | | | HIGH |
| IO | DIFFIO_TX10p | | B1 | VREF1B1 | V22 | Y27 | AA25 | | | HIGH |
| IO | DIFFIO_TX10n | | B1 | VREF1B1 | V21 | AA27 | AA24 | | | HIGH |
| VREF1B1 | | | B1 | VREF1B1 | W20 | W22 | AA23 | | | |
| IO | DIFFIO_RX9p | | B1 | VREF1B1 | AB28 | AC31 | AB32 | | | HIGH |
| IO | DIFFIO_RX9n | | B1 | VREF1B1 | AB27 | AD31 | AC31 | | | HIGH |
| IO | DIFFIO_TX9p | | B1 | VREF1B1 | W23 | AB27 | AA27 | | | HIGH |
| IO | DIFFIO_TX9n | | B1 | VREF1B1 | W24 | AC27 | AA26 | | | HIGH |
| IO | DIFFIO_RX8p | | B1 | VREF1B1 | AB26 | AE31 | AD32 | | | HIGH |
| IO | DIFFIO_RX8n | | B1 | VREF1B1 | AB25 | AF31 | AD31 | | | HIGH |
| IO | DIFFIO_TX8p | | B1 | VREF1B1 | W21 | AE27 | AB27 | | | HIGH |

**Table 4–1. Pin List for the Stratix EP1S30 Device (Part 9 of 52)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_TX8n | | B1 | VREF1B1 | W22 | AD27 | AB26 | | | HIGH |
| IO | DIFFIO_RX7p | | B1 | VREF1B1 | AC28 | AC30 | AC29 | | | HIGH |
| IO | DIFFIO_RX7n | | B1 | VREF1B1 | AC27 | AD30 | AC30 | | | HIGH |
| IO | DIFFIO_TX7p | | B1 | VREF1B1 | Y21 | AG27 | AC25 | | | HIGH |
| IO | DIFFIO_TX7n | | B1 | VREF1B1 | Y22 | AF27 | AC26 | | | HIGH |
| IO | DIFFIO_RX6p | | B1 | VREF1B1 | AD28 | AF30 | AD30 | | | HIGH |
| IO | DIFFIO_RX6n | | B1 | VREF1B1 | AD27 | AE30 | AD29 | | | HIGH |
| IO | DIFFIO_TX6p | | B1 | VREF1B1 | Y24 | AB26 | AC27 | | | HIGH |
| IO | DIFFIO_TX6n | | B1 | VREF1B1 | Y23 | AC26 | AC28 | | | HIGH |
| IO | DIFFIO_RX5p | | B1 | VREF2B1 | AE28 | AG30 | AE32 | | | HIGH |
| IO | DIFFIO_RX5n | | B1 | VREF2B1 | AE27 | AH30 | AE31 | | | HIGH |
| IO | DIFFIO_TX5p | | B1 | VREF2B1 | AA23 | AD26 | AD28 | | | HIGH |
| IO | DIFFIO_TX5n | | B1 | VREF2B1 | AA24 | AE26 | AD27 | | | HIGH |
| IO | DIFFIO_RX4p | | B1 | VREF2B1 | AF28 | AC29 | AE30 | | | HIGH |
| IO | DIFFIO_RX4n | | B1 | VREF2B1 | AF27 | AD29 | AE29 | | | HIGH |
| IO | DIFFIO_TX4p | | B1 | VREF2B1 | AA21 | AA25 | AD26 | | | HIGH |
| IO | DIFFIO_TX4n | | B1 | VREF2B1 | AA22 | AB25 | AD25 | | | HIGH |
| IO | DIFFIO_RX3p | | B1 | VREF2B1 | | AE29 | AF32 | | | HIGH |
| IO | DIFFIO_RX3n | | B1 | VREF2B1 | | AF29 | AF31 | | | HIGH |
| IO | DIFFIO_TX3p | | B1 | VREF2B1 | AB23 | AD25 | AE28 | | | HIGH |
| IO | DIFFIO_TX3n | | B1 | VREF2B1 | AB24 | AC25 | AE27 | | | HIGH |

**Table 4–1. Pin List for the Stratix EP1S30 Device (Part 10 of 52)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_RX2p | | B1 | VREF2B1 | | AH29 | AF30 | | | HIGH |
| IO | DIFFIO_RX2n | | B1 | VREF2B1 | | AG29 | AF29 | | | HIGH |
| IO | DIFFIO_TX2p | | B1 | VREF2B1 | | AA24 | AE25 | | | HIGH |
| IO | DIFFIO_TX2n | | B1 | VREF2B1 | | AB24 | AE26 | | | HIGH |
| VREF2B1 | | | B1 | VREF2B1 | AE26 | Y22 | AB25 | | | |
| IO | DIFFIO_RX1p | | B1 | VREF2B1 | | AC28 | AG31 | | | HIGH |
| IO | DIFFIO_RX1n | | B1 | VREF2B1 | | AD28 | AG32 | | | HIGH |
| IO | DIFFIO_TX1p | | B1 | VREF2B1 | | AD24 | AF27 | | | HIGH |
| IO | DIFFIO_TX1n | | B1 | VREF2B1 | | AC24 | AF28 | | | HIGH |
| IO | DIFFIO_RX0p | | B1 | VREF2B1 | | AE28 | AG30 | | | HIGH |
| IO | DIFFIO_RX0n | | B1 | VREF2B1 | | AF28 | AG29 | | | HIGH |
| IO | DIFFIO_TX0p | | B1 | VREF2B1 | | AE25 | AF26 | | | HIGH |
| IO | DIFFIO_TX0n | | B1 | VREF2B1 | | AF25 | AF25 | | | HIGH |
| FPLL8CLKn | | | B1 | VREF2B1 | | AG31 | AB29 | | | |
| FPLL8CLKp | | | B1 | VREF2B1 | | AH31 | AB28 | | | |
| IO | | | B1 | VREF2B1 | | | AA22 | | | |
| IO | | | B1 | VREF2B1 | | | AB23 | | | |
| VCCINT | | | | | | | | | | |
| VCCA_PLL8 | | | | | | AB23 | AJ31 | | | |
| GND | | | | | | | | | | |
| GNDA_PLL8 | | | | | | AA23 | AJ32 | | | |

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 11 of 52)

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| VCCG_PLL8 | | | | | | AD23 | AJ30 | | | |
| GNDG_PLL8 | | | | | | AC23 | AH30 | | | |
| IO | | | B8 | VREF0B8 | AC24 | AG28 | AC24 | | | |
| IO | DQ9B7 | | B8 | VREF0B8 | AG26 | AK29 | AH28 | DQ3B15 | DQ1B31 | |
| IO | | | B8 | VREF0B8 | AC23 | AJ30 | AD24 | | | |
| IO | DQ9B6 | | B8 | VREF0B8 | AH26 | AJ29 | AK30 | DQ3B14 | DQ1B30 | |
| IO | DQ9B5 | | B8 | VREF0B8 | AG25 | AJ28 | AJ28 | DQ3B13 | DQ1B29 | |
| IO | DQ9B4 | | B8 | VREF0B8 | AH25 | AL28 | AJ29 | DQ3B12 | DQ1B28 | |
| IO | | | B8 | VREF0B8 | AB22 | AA21 | AB24 | | | |
| IO | DQ9B3 | | B8 | VREF0B8 | AF25 | AH27 | AK29 | DQ3B11 | DQ1B27 | |
| IO | | | B8 | VREF0B8 | | AF26 | AE24 | | | |
| IO | DQS9B | | B8 | VREF0B8 | AF24 | AK28 | AK28 | | | |
| IO | DQ9B2 | | B8 | VREF0B8 | AG24 | AL27 | AL30 | DQ3B10 | DQ1B26 | |
| IO | | | B8 | VREF0B8 | AE25 | AE24 | AF24 | | | |
| IO | DQ9B1 | | B8 | VREF0B8 | AE24 | AJ27 | AL29 | DQ3B9 | DQ1B25 | |
| IO | | | B8 | VREF0B8 | | | AC23 | | | |
| IO | DQ9B0 | | B8 | VREF0B8 | AH24 | AK27 | AM29 | DQ3B8 | DQ1B24 | |
| IO | | | B8 | VREF0B8 | AD24 | AC22 | AE23 | | | |
| IO | | | B8 | VREF0B8 | | AD22 | AG24 | | | |
| IO | DQ8B7 | | B8 | VREF0B8 | AG23 | AH26 | AH26 | DQ3B7 | DQ1B23 | |
| VREF0B8 | | | B8 | VREF0B8 | AD22 | AB22 | AH27 | | | |

*Table 4–1. Pin List for the Stratix EP1S30 Device (Part 12 of 52)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DQ8B6 | | B8 | VREF0B8 | AD23 | AG26 | AJ27 | DQ3B6 | DQ1B22 | |
| IO | DQ8B5 | | B8 | VREF0B8 | AF23 | AK26 | AL28 | DQ3B5 | DQ1B21 | |
| IO | | | B8 | VREF0B8 | AB21 | AH28 | AD23 | | | |
| IO | DQ8B4 | | B8 | VREF0B8 | AH23 | AL26 | AK27 | DQ3B4 | DQ1B20 | |
| IO | DQ8B3 | | B8 | VREF0B8 | AE22 | AH25 | AJ26 | DQ3B3 | DQ1B19 | |
| IO | | | B8 | VREF0B8 | | AE22 | AF23 | | | |
| IO | DQS8B | | B8 | VREF0B8 | AE23 | AJ26 | AL27 | DQS3B | | |
| IO | DQ8B2 | | B8 | VREF0B8 | AF22 | AK25 | AM27 | DQ3B2 | DQ1B18 | |
| IO | | | B8 | VREF0B8 | AB20 | AC21 | AC22 | | | |
| IO | DQ8B1 | | B8 | VREF0B8 | AH22 | AJ25 | AM28 | DQ3B1 | DQ1B17 | |
| IO | DQ8B0 | | B8 | VREF0B8 | AG22 | AL25 | AK26 | DQ3B0 | DQ1B16 | |
| IO | | | B8 | VREF0B8 | | | AG23 | | | |
| IO | | | B8 | VREF1B8 | Y20 | AD21 | AB22 | | | |
| IO | DQ7B7 | | B8 | VREF1B8 | AD21 | AG24 | AH24 | DQ2B15 | DQ1B15 | |
| IO | | | B8 | VREF1B8 | | AC20 | AD22 | | | |
| IO | DQ7B6 | | B8 | VREF1B8 | AE21 | AH23 | AJ24 | DQ2B14 | DQ1B14 | |
| IO | DQ7B5 | | B8 | VREF1B8 | AG21 | AK24 | AJ25 | DQ2B13 | DQ1B13 | |
| IO | | | B8 | VREF1B8 | AC22 | AD20 | AF22 | | | |
| IO | DQ7B4 | | B8 | VREF1B8 | AF21 | AH24 | AK25 | DQ2B12 | DQ1B12 | |
| IO | DQ7B3 | | B8 | VREF1B8 | AE20 | AJ23 | AL25 | DQ2B11 | DQ1B11 | |
| IO | | | B8 | VREF1B8 | | | AC21 | | | |

**Table 4–1. Pin List for the Stratix EP1S30 Device (Part 13 of 52)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DQS7B | | B8 | VREF1B8 | AG20 | AJ24 | AL26 | | DQS1B | |
| IO | DQ7B2 | | B8 | VREF1B8 | AF20 | AL24 | AK24 | DQ2B10 | DQ1B10 | |
| IO | | | B8 | VREF1B8 | AC20 | AE20 | AG22 | | | |
| IO | DQ7B1 | | B8 | VREF1B8 | AH21 | AK23 | AM25 | DQ2B9 | DQ1B9 | |
| IO | | | B8 | VREF1B8 | | | AB21 | | | |
| IO | DQ7B0 | | B8 | VREF1B8 | AH20 | AL23 | AM26 | DQ2B8 | DQ1B8 | |
| IO | DQ6B7 | | B8 | VREF1B8 | AE19 | AG22 | AJ23 | DQ2B7 | DQ1B7 | |
| IO | FCLK3 | | B8 | VREF1B8 | AC21 | AF23 | AE21 | | | |
| IO | FCLK2 | | B8 | VREF1B8 | AC19 | AF22 | AF21 | | | |
| VREF1B8 | | | B8 | VREF1B8 | AD20 | AB21 | AH25 | | | |
| IO | DQ6B6 | | B8 | VREF1B8 | AD19 | AH22 | AL24 | DQ2B6 | DQ1B6 | |
| IO | DQ6B5 | | B8 | VREF1B8 | AF19 | AK22 | AH22 | DQ2B5 | DQ1B5 | |
| IO | | | B8 | VREF1B8 | | AC19 | AD21 | | | |
| IO | DQ6B4 | | B8 | VREF1B8 | AG19 | AG21 | AM24 | DQ2B4 | DQ1B4 | |
| IO | | PGM2 | B8 | VREF1B8 | AB19 | AF24 | AA20 | | | |
| IO | DQ6B3 | | B8 | VREF1B8 | AH19 | AH21 | AK23 | DQ2B3 | DQ1B3 | |
| IO | | | B8 | VREF1B8 | | AA19 | AA21 | | | |
| IO | DQS6B | | B8 | VREF1B8 | AF18 | AJ22 | AJ22 | DQS2B | | |
| IO | DQ6B2 | | B8 | VREF1B8 | AD18 | AL22 | AL23 | DQ2B2 | DQ1B2 | |
| IO | | | B8 | VREF1B8 | AA20 | AE21 | AF20 | | | |
| IO | DQ6B1 | | B8 | VREF1B8 | AE18 | AJ21 | AK22 | DQ2B1 | DQ1B1 | |

**Table 4–1. Pin List for the Stratix EP1S30 Device (Part 14 of 52)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DQ6B0 | | B8 | VREF1B8 | AG18 | AK21 | AL22 | DQ2B0 | DQ1B0 | |
| IO | RDN8 | | B8 | VREF1B8 | Y19 | AE23 | AC20 | | | |
| IO | RUP8 | | B8 | VREF1B8 | W19 | AG25 | AH19 | | | |
| IO | DQ5B7 | | B8 | VREF1B8 | AF17 | AG20 | AM22 | | | |
| IO | | | B8 | VREF1B8 | | AE19 | AD20 | | | |
| IO | DQ5B6 | | B8 | VREF1B8 | AG17 | AH20 | AJ21 | | | |
| IO | DQ5B5 | | B8 | VREF1B8 | AE17 | AK20 | AK21 | | | |
| IO | | | B8 | VREF2B8 | | AD19 | AB20 | | | |
| IO | DQ5B4 | | B8 | VREF2B8 | AD17 | AL20 | AL21 | | | |
| IO | | RDYnBSY | B8 | VREF2B8 | AA19 | AG23 | AA19 | | | |
| IO | DQ5B3 | | B8 | VREF2B8 | AG16 | AG19 | AH20 | | | |
| IO | | | B8 | VREF2B8 | AB18 | AE18 | AE20 | | | |
| IO | DQS5B | | B8 | VREF2B8 | AH16 | AJ20 | AJ20 | | | |
| IO | DQ5B2 | | B8 | VREF2B8 | AD16 | AH19 | AK20 | | | |
| IO | | nCS | B8 | VREF2B8 | Y18 | AF20 | AC19 | | | |
| IO | DQ5B1 | | B8 | VREF2B8 | AF16 | AJ19 | AL20 | | | |
| IO | DQ5B0 | | B8 | VREF2B8 | AE16 | AK19 | AM20 | | | |
| IO | | | B8 | VREF2B8 | | | AG21 | | | |
| IO | | | B8 | VREF2B8 | | | AG20 | | | |
| IO | | | B8 | VREF2B8 | V18 | | AB19 | | | |
| IO | | | B8 | VREF2B8 | W18 | | AD19 | | | |

**Table 4–1. Pin List for the Stratix EP1S30 Device (Part 15 of 52)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | | CS | B8 | VREF2B8 | AA18 | AF21 | AG19 | | | |
| IO | | | B8 | VREF2B8 | | | AJ18 | | | |
| IO | | | B8 | VREF2B8 | | | AH18 | | | |
| IO | | | B8 | VREF2B8 | | | AK18 | | | |
| VREF2B8 | | | B8 | VREF2B8 | AH18 | AB20 | AH23 | | | |
| IO | CLK5n | | B8 | VREF2B8 | Y17 | AH18 | AJ19 | | | |
| CLK5p | | | B8 | VREF2B8 | AA17 | AJ18 | AK19 | | | |
| IO | CLK4n | | B8 | VREF2B8 | AB17 | AK18 | AL19 | | | |
| CLK4p | | | B8 | VREF2B8 | AC17 | AL18 | AM19 | | | |
| PLL_ENA | | PLL_ENA | B8 | VREF2B8 | AC18 | AF19 | AF19 | | | |
| MSEL0 | | MSEL0 | B8 | VREF2B8 | AC16 | AF18 | AG18 | | | |
| MSEL1 | | MSEL1 | B8 | VREF2B8 | W17 | AG18 | AE18 | | | |
| MSEL2 | | MSEL2 | B8 | VREF2B8 | AB15 | AG17 | AE19 | | | |
| IO | PLL6_OUT3n | | B12 | VREF2B8 | Y16 | AL17 | AM18 | | | |
| IO | PLL6_OUT3p | | B12 | VREF2B8 | W16 | AK17 | AL18 | | | |
| IO | PLL6_OUT2n | | B12 | VREF2B8 | AG15 | AJ17 | AK17 | | | |
| IO | PLL6_OUT2p | | B12 | VREF2B8 | AF15 | AH17 | AJ17 | | | |
| IO | PLL6_FBn | | B11 | VREF2B8 | AA15 | AJ15 | AM17 | | | |
| IO | PLL6_FBp | | B11 | VREF2B8 | AA14 | AH15 | AL17 | | | |
| IO | PLL6_OUT1n | | B11 | VREF2B8 | W15 | AL15 | AK16 | | | |
| IO | PLL6_OUT1p | | B11 | VREF2B8 | W14 | AK15 | AJ16 | | | |

**Table 4–1. Pin List for the Stratix EP1S30 Device (Part 16 of 52)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | PLL6_OUT0n | | B11 | VREF2B8 | AE15 | AL16 | AM16 | | | |
| IO | PLL6_OUT0p | | B11 | VREF2B8 | AD15 | AK16 | AL16 | | | |
| VCC_PLL6_OUTB | | | B12 | | AB16 | AC18 | AB17 | | | |
| VCC_PLL6_OUTB | | | B12 | | | | | | | |
| VCC_PLL6_OUTA | | | B11 | | AC14 | AD17 | AE17 | | | |
| VCC_PLL6_OUTA | | | B11 | | | | | | | |
| VCCINT | | | | | | | | | | |
| VCCA_PLL6 | | | | | AG14 | AB17 | AG17 | | | |
| GND | | | | | | | | | | |
| GNDA_PLL6 | | | | | AF14 | AC17 | AH17 | | | |
| VCCG_PLL6 | | | | | AA13 | AD15 | AD16 | | | |
| GNDG_PLL6 | | | | | AB14 | AD16 | AB16 | | | |
| CLK7p | | | B7 | VREF0B7 | W13 | AJ14 | AM15 | | | |
| IO | CLK7n | | B7 | VREF0B7 | Y13 | AH14 | AL15 | | | |
| CLK6p | | | B7 | VREF0B7 | AD14 | AL14 | AK15 | | | |
| IO | CLK6n | | B7 | VREF0B7 | AE14 | AK14 | AJ15 | | | |
| nCE | | nCE | B7 | VREF0B7 | AB13 | AF17 | AF18 | | | |
| nCEO | | nCEO | B7 | VREF0B7 | AC13 | AF16 | AH15 | | | |
| IO | | | B7 | VREF0B7 | | AA16 | AA18 | | | |
| IO | | | B7 | VREF0B7 | | AA15 | AC18 | | | |
| IO | | PGM0 | B7 | VREF0B7 | W12 | AE17 | AD18 | | | |

**Table 4–1. Pin List for the Stratix EP1S30 Device (Part 17 of 52)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| nIO_PULLUP | | nIO_PULLUP | B7 | VREF0B7 | Y12 | AE16 | AF15 | | | |
| VCCSEL | | VCCSEL | B7 | VREF0B7 | AA12 | AE15 | AJ14 | | | |
| PORSEL | | PORSEL | B7 | VREF0B7 | AC12 | AG16 | AG15 | | | |
| IO | | | B7 | VREF0B7 | | AH16 | AC15 | | | |
| IO | | | B7 | VREF0B7 | | | AB15 | | | |
| IO | | | B7 | VREF0B7 | | | AD15 | | | |
| IO | | | B7 | VREF0B7 | | | AE14 | | | |
| IO | | | B7 | VREF0B7 | | | AL14 | | | |
| IO | | | B7 | VREF0B7 | | AE13 | AK14 | | | |
| VREF0B7 | | | B7 | VREF0B7 | AD11 | AB14 | AH12 | | | |
| IO | | INIT_DONE | B7 | VREF0B7 | W11 | AF15 | AE15 | | | |
| IO | | | B7 | VREF0B7 | V11 | AC13 | AA15 | | | |
| IO | DQ4B7 | | B7 | VREF0B7 | AD13 | AK13 | AL13 | | | |
| IO | DQ4B6 | | B7 | VREF0B7 | AE13 | AG13 | AM13 | | | |
| IO | | nRS | B7 | VREF0B7 | AC11 | AE14 | AB18 | | | |
| IO | DQ4B5 | | B7 | VREF0B7 | AF13 | AH13 | AH13 | | | |
| IO | | | B7 | VREF0B7 | Y11 | AE12 | AB14 | | | |
| IO | DQ4B4 | | B7 | VREF0B7 | AD12 | AJ13 | AJ13 | | | |
| IO | DQ4B3 | | B7 | VREF0B7 | AG13 | AK12 | AK13 | | | |
| IO | | RUnLU | B7 | VREF0B7 | W10 | AJ16 | AF14 | | | |
| IO | DQS4B | | B7 | VREF0B7 | AH13 | AJ12 | AJ12 | | | |

*Table 4–1. Pin List for the Stratix EP1S30 Device (Part 18 of 52)*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | | | |
| IO | | | B7 | VREF0B7 | AB12 | AD13 | AD14 | | | |
| IO | DQ4B2 | | B7 | VREF1B7 | AE12 | AL12 | AK12 | | | |
| IO | DQ4B1 | | B7 | VREF1B7 | AF12 | AG12 | AL12 | | | |
| IO | | PGM1 | B7 | VREF1B7 | AA11 | AG15 | AG14 | | | |
| IO | DQ4B0 | | B7 | VREF1B7 | AG12 | AH12 | AM11 | | | |
| IO | RDN7 | | B7 | VREF1B7 | AC10 | AG14 | AC14 | | | |
| IO | RUP7 | | B7 | VREF1B7 | AB11 | AF13 | AF13 | | | |
| IO | DQ3B7 | | B7 | VREF1B7 | AG11 | AL10 | AL10 | DQ1B15 | DQ0B31 | |
| IO | | | B7 | VREF1B7 | | AE11 | AA14 | | | |
| IO | DQ3B6 | | B7 | VREF1B7 | AH11 | AJ11 | AK11 | DQ1B14 | DQ0B30 | |
| IO | DQ3B5 | | B7 | VREF1B7 | AE11 | AK11 | AL11 | DQ1B13 | DQ0B29 | |
| IO | DEV_CLRn | | B7 | VREF1B7 | AC9 | AF14 | AH14 | | | |
| IO | DQ3B4 | | B7 | VREF1B7 | AF11 | AG11 | AK10 | DQ1B12 | DQ0B28 | |
| IO | DQ3B3 | | B7 | VREF1B7 | AE10 | AH11 | AM9 | DQ1B11 | DQ0B27 | |
| IO | | | B7 | VREF1B7 | | AD11 | AB13 | | | |
| IO | DQS3B | | B7 | VREF1B7 | AG10 | AJ10 | AJ11 | DQS1B | | |
| IO | | | B7 | VREF1B7 | Y10 | AD12 | AD13 | | | |
| IO | DQ3B2 | | B7 | VREF1B7 | AH10 | AG10 | AL9 | DQ1B10 | DQ0B26 | |
| IO | DQ3B1 | | B7 | VREF1B7 | AF10 | AH10 | AJ10 | DQ1B9 | DQ0B25 | |
| VREF1B7 | | | B7 | VREF1B7 | AD9 | AB13 | AH10 | | | |
| IO | DQ3B0 | | B7 | VREF1B7 | AD10 | AK10 | AH11 | DQ1B8 | DQ0B24 | |

*Table 4–1. Pin List for the Stratix EP1S30 Device (Part 19 of 52)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | | | B7 | VREF1B7 | | AA13 | AC13 | | | |
| IO | | | B7 | VREF1B7 | AA10 | AF10 | AG13 | | | |
| IO | DQ2B7 | | B7 | VREF1B7 | AG9 | AL8 | AL8 | DQ1B7 | DQ0B23 | |
| IO | FCLK5 | | B7 | VREF1B7 | AC8 | AF12 | AM14 | | | |
| IO | FCLK4 | | B7 | VREF1B7 | AB10 | AF11 | AF12 | | | |
| IO | DQ2B6 | | B7 | VREF1B7 | AF9 | AK9 | AJ9 | DQ1B6 | DQ0B22 | |
| IO | DQ2B5 | | B7 | VREF1B7 | AE9 | AL9 | AK9 | DQ1B5 | DQ0B21 | |
| IO | | | B7 | VREF1B7 | AB9 | AC12 | AE13 | | | |
| IO | DQ2B4 | | B7 | VREF1B7 | AH8 | AH8 | AM8 | DQ1B4 | DQ0B20 | |
| IO | DQ2B3 | | B7 | VREF1B7 | AH9 | AK8 | AH9 | DQ1B3 | DQ0B19 | |
| IO | | | B7 | VREF1B7 | | AG9 | AG12 | | | |
| IO | DQS2B | | B7 | VREF2B7 | AE8 | AJ8 | AK8 | | DQS0B | |
| IO | DQ2B2 | | B7 | VREF2B7 | AD8 | AG8 | AM7 | DQ1B2 | DQ0B18 | |
| IO | | | B7 | VREF2B7 | AA9 | AC11 | AD12 | | | |
| IO | DQ2B1 | | B7 | VREF2B7 | AF8 | AH9 | AJ8 | DQ1B1 | DQ0B17 | |
| IO | DQ2B0 | | B7 | VREF2B7 | AG8 | AJ9 | AL7 | DQ1B0 | DQ0B16 | |
| IO | | | B7 | VREF2B7 | | AE10 | AE12 | | | |
| IO | | | B7 | VREF2B7 | AB8 | AE9 | AC12 | | | |
| IO | DQ1B7 | | B7 | VREF2B7 | AF6 | AK7 | AL6 | DQ0B15 | DQ0B15 | |
| IO | DQ1B6 | | B7 | VREF2B7 | AG7 | AL7 | AM6 | DQ0B14 | DQ0B14 | |
| IO | | | B7 | VREF2B7 | AC7 | AD10 | AG11 | | | |

*Table 4–1. Pin List for the Stratix EP1S30 Device (Part 20 of 52)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DQ1B5 | | B7 | VREF2B7 | AH7 | AH6 | AJ7 | DQ0B13 | DQ0B13 | |
| IO | DQ1B4 | | B7 | VREF2B7 | AF7 | AK6 | AM5 | DQ0B12 | DQ0B12 | |
| IO | | | B7 | VREF2B7 | | AC10 | AA12 | | | |
| IO | DQ1B3 | | B7 | VREF2B7 | AD6 | AL6 | AK7 | DQ0B11 | DQ0B11 | |
| IO | DQS1B | | B7 | VREF2B7 | AE7 | AJ6 | AH7 | DQS0B | | |
| IO | | | B7 | VREF2B7 | AD5 | AG7 | AE11 | | | |
| IO | DQ1B2 | | B7 | VREF2B7 | AH6 | AH7 | AL5 | DQ0B10 | DQ0B10 | |
| IO | DQ1B1 | | B7 | VREF2B7 | AG6 | AJ7 | AK6 | DQ0B9 | DQ0B9 | |
| VREF2B7 | | | B7 | VREF2B7 | AD7 | AB12 | AH8 | | | |
| IO | DQ1B0 | | B7 | VREF2B7 | AE6 | AG6 | AJ6 | DQ0B8 | DQ0B8 | |
| IO | | | B7 | VREF2B7 | Y9 | AA11 | AB11 | | | |
| IO | | | B7 | VREF2B7 | | AF8 | AF10 | | | |
| IO | DQ0B7 | | B7 | VREF2B7 | AF5 | AL4 | AL3 | DQ0B7 | DQ0B7 | |
| IO | | | B7 | VREF2B7 | AE4 | AF9 | AG10 | | | |
| IO | DQ0B6 | | B7 | VREF2B7 | AH5 | AL5 | AL4 | DQ0B6 | DQ0B6 | |
| IO | | | B7 | VREF2B7 | AC6 | AF6 | AC9 | | | |
| IO | DQ0B5 | | B7 | VREF2B7 | AF4 | AJ4 | AM4 | DQ0B5 | DQ0B5 | |
| IO | DQ0B4 | | B7 | VREF2B7 | AG4 | AK3 | AJ4 | DQ0B4 | DQ0B4 | |
| IO | | | B7 | VREF2B7 | | AH4 | AG9 | | | |
| IO | DQ0B3 | | B7 | VREF2B7 | AG5 | AK5 | AJ5 | DQ0B3 | DQ0B3 | |
| IO | DQS0B | | B7 | VREF2B7 | AH3 | AK4 | AK5 | | | |

**Table 4–1. Pin List for the Stratix EP1S30 Device (Part 21 of 52)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | | | B7 | VREF2B7 | AC5 | AG4 | AD9 | | | |
| IO | DQ0B2 | | B7 | VREF2B7 | AG3 | AH5 | AH5 | DQ0B2 | DQ0B2 | |
| IO | DQ0B1 | | B7 | VREF2B7 | AE5 | AJ5 | AK3 | DQ0B1 | DQ0B1 | |
| IO | | | B7 | VREF2B7 | AB7 | AJ2 | AE9 | | | |
| IO | DQ0B0 | | B7 | VREF2B7 | AH4 | AJ3 | AK4 | DQ0B0 | DQ0B0 | |
| IO | | | B7 | VREF2B7 | | AE8 | AF9 | | | |
| GNDG_PLL9 | | | | | | AC9 | AH3 | | | |
| VCCG_PLL9 | | | | | | AD9 | AJ3 | | | |
| GNDA_PLL9 | | | | | | AA9 | AJ1 | | | |
| GND | | | | | | | | | | |
| VCCA_PLL9 | | | | | | AB9 | AJ2 | | | |
| VCCINT | | | | | | | | | | |
| IO | | | B6 | VREF0B6 | | | AB9 | | | |
| IO | | | B6 | VREF0B6 | | | AC10 | | | |
| FPLL9CLKp | | | B6 | VREF0B6 | | AH1 | AB5 | | | |
| FPLL9CLKn | | | B6 | VREF0B6 | | AG1 | AB4 | | | |
| IO | DIFFIO_TX81n | | B6 | VREF0B6 | | AC8 | AF8 | | | HIGH |
| IO | DIFFIO_TX81p | | B6 | VREF0B6 | | AD8 | AF7 | | | HIGH |
| IO | DIFFIO_RX81n | | B6 | VREF0B6 | | AF4 | AG4 | | | HIGH |
| IO | DIFFIO_RX81p | | B6 | VREF0B6 | | AE4 | AG3 | | | HIGH |
| IO | DIFFIO_TX80n | | B6 | VREF0B6 | | AF7 | AF5 | | | HIGH |

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 22 of 52)

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_TX80p | | B6 | VREF0B6 | | AE7 | AF6 | | | HIGH |
| IO | DIFFIO_RX80n | | B6 | VREF0B6 | | AD4 | AG1 | | | HIGH |
| IO | DIFFIO_RX80p | | B6 | VREF0B6 | | AC4 | AG2 | | | HIGH |
| VREF0B6 | | | B6 | VREF0B6 | AE3 | AA10 | AG6 | | | |
| IO | DIFFIO_TX79n | | B6 | VREF0B6 | | AB8 | AE7 | | | HIGH |
| IO | DIFFIO_TX79p | | B6 | VREF0B6 | | AA8 | AE8 | | | HIGH |
| IO | DIFFIO_RX79n | | B6 | VREF0B6 | | AG3 | AF4 | | | HIGH |
| IO | DIFFIO_RX79p | | B6 | VREF0B6 | | AH3 | AF3 | | | HIGH |
| IO | DIFFIO_TX78n | | B6 | VREF0B6 | AB5 | AC7 | AD6 | | | HIGH |
| IO | DIFFIO_TX78p | | B6 | VREF0B6 | AB6 | AD7 | AD5 | | | HIGH |
| IO | DIFFIO_RX78n | | B6 | VREF0B6 | | AF3 | AF2 | | | HIGH |
| IO | DIFFIO_RX78p | | B6 | VREF0B6 | | AE3 | AF1 | | | HIGH |
| IO | DIFFIO_TX77n | | B6 | VREF0B6 | AA7 | AB7 | AE6 | | | HIGH |
| IO | DIFFIO_TX77p | | B6 | VREF0B6 | AA8 | AA7 | AE5 | | | HIGH |
| IO | DIFFIO_RX77n | | B6 | VREF0B6 | AF2 | AD3 | AE4 | | | HIGH |
| IO | DIFFIO_RX77p | | B6 | VREF0B6 | AF1 | AC3 | AE3 | | | HIGH |
| IO | DIFFIO_TX76n | | B6 | VREF0B6 | AA5 | AE6 | AD8 | | | HIGH |
| IO | DIFFIO_TX76p | | B6 | VREF0B6 | AA6 | AD6 | AD7 | | | HIGH |
| IO | DIFFIO_RX76n | | B6 | VREF0B6 | AE2 | AH2 | AE2 | | | HIGH |
| IO | DIFFIO_RX76p | | B6 | VREF0B6 | AE1 | AG2 | AE1 | | | HIGH |
| IO | DIFFIO_TX75n | | B6 | VREF1B6 | Y6 | AC6 | AC5 | | | HIGH |

**Table 4–1. Pin List for the Stratix EP1S30 Device (Part 23 of 52)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_TX75p | | B6 | VREF1B6 | Y5 | AB6 | AC6 | | | HIGH |
| IO | DIFFIO_RX75n | | B6 | VREF1B6 | AD2 | AE2 | AC3 | | | HIGH |
| IO | DIFFIO_RX75p | | B6 | VREF1B6 | AD1 | AF2 | AC4 | | | HIGH |
| IO | DIFFIO_TX74n | | B6 | VREF1B6 | Y7 | AF5 | AC7 | | | HIGH |
| IO | DIFFIO_TX74p | | B6 | VREF1B6 | Y8 | AG5 | AC8 | | | HIGH |
| IO | DIFFIO_RX74n | | B6 | VREF1B6 | AC2 | AD2 | AD3 | | | HIGH |
| IO | DIFFIO_RX74p | | B6 | VREF1B6 | AC1 | AC2 | AD4 | | | HIGH |
| IO | DIFFIO_TX73n | | B6 | VREF1B6 | W7 | AD5 | AB7 | | | HIGH |
| IO | DIFFIO_TX73p | | B6 | VREF1B6 | W8 | AE5 | AB6 | | | HIGH |
| IO | DIFFIO_RX73n | | B6 | VREF1B6 | AB4 | AF1 | AD2 | | | HIGH |
| IO | DIFFIO_RX73p | | B6 | VREF1B6 | AB3 | AE1 | AD1 | | | HIGH |
| IO | DIFFIO_TX72n | | B6 | VREF1B6 | W5 | AC5 | AA6 | | | HIGH |
| IO | DIFFIO_TX72p | | B6 | VREF1B6 | W6 | AB5 | AA7 | | | HIGH |
| IO | DIFFIO_RX72n | | B6 | VREF1B6 | AB2 | AD1 | AC2 | | | HIGH |
| IO | DIFFIO_RX72p | | B6 | VREF1B6 | AB1 | AC1 | AB1 | | | HIGH |
| VREF1B6 | | | B6 | VREF1B6 | W9 | Y10 | AB8 | | | |
| IO | DIFFIO_TX71n | | B6 | VREF1B6 | V8 | AA6 | AA9 | | | HIGH |
| IO | DIFFIO_TX71p | | B6 | VREF1B6 | V7 | Y6 | AA8 | | | HIGH |
| IO | DIFFIO_RX71n/RDN6 | | B6 | VREF1B6 | AA3 | AB4 | AA4 | | | HIGH |
| IO | DIFFIO_RX71p/RUP6 | | B6 | VREF1B6 | AA4 | AB3 | AA5 | | | HIGH |
| IO | DIFFIO_TX70n | | B6 | VREF1B6 | V6 | Y9 | Y5 | | | HIGH |

*Table 4–1. Pin List for the Stratix EP1S30 Device (Part 24 of 52)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_TX70p | | B6 | VREF1B6 | V5 | W9 | Y6 | | | HIGH |
| IO | DIFFIO_RX70n | | B6 | VREF1B6 | AA2 | Y4 | AB3 | | | HIGH |
| IO | DIFFIO_RX70p | | B6 | VREF1B6 | AA1 | AA4 | AB2 | | | HIGH |
| IO | DIFFIO_TX69n | | B6 | VREF1B6 | V9 | Y8 | Y7 | | | HIGH |
| IO | DIFFIO_TX69p | | B6 | VREF1B6 | V10 | W8 | Y8 | | | HIGH |
| IO | DIFFIO_RX69n | | B6 | VREF1B6 | Y4 | W4 | AA3 | | | HIGH |
| IO | DIFFIO_RX69p | | B6 | VREF1B6 | Y3 | V4 | AA2 | | | HIGH |
| IO | DIFFIO_TX68n | | B6 | VREF1B6 | U7 | AA5 | W5 | | | HIGH |
| IO | DIFFIO_TX68p | | B6 | VREF1B6 | U8 | Y5 | W6 | | | HIGH |
| IO | DIFFIO_RX68n | | B6 | VREF1B6 | Y2 | AA3 | Y4 | | | HIGH |
| IO | DIFFIO_RX68p | | B6 | VREF1B6 | Y1 | Y3 | Y3 | | | HIGH |
| IO | DIFFIO_TX67n | | B6 | VREF2B6 | U6 | Y7 | Y10 | | | HIGH |
| IO | DIFFIO_TX67p | | B6 | VREF2B6 | U5 | W7 | Y9 | | | HIGH |
| IO | DIFFIO_RX67n | | B6 | VREF2B6 | W4 | W3 | Y2 | | | HIGH |
| IO | DIFFIO_RX67p | | B6 | VREF2B6 | W3 | V3 | Y1 | | | HIGH |
| IO | DIFFIO_TX66n | | B6 | VREF2B6 | U9 | U7 | W10 | | | HIGH |
| IO | DIFFIO_TX66p | | B6 | VREF2B6 | U10 | V7 | W9 | | | HIGH |
| IO | DIFFIO_RX66n | | B6 | VREF2B6 | W2 | AB2 | W4 | | | HIGH |
| IO | DIFFIO_RX66p | | B6 | VREF2B6 | W1 | AA2 | W3 | | | HIGH |
| IO | DIFFIO_TX65n | | B6 | VREF2B6 | T6 | W6 | V9 | | | HIGH |
| IO | DIFFIO_TX65p | | B6 | VREF2B6 | T5 | V6 | V10 | | | HIGH |

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 25 of 52)

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **780-Pin FineLine BGA** | **956-Pin BGA** | **1020-Pin FineLine BGA** | **DQS for x16** | **DQS for x32** | **DIFFIO Speed** *Note (1)* |
| IO | DIFFIO_RX65n | | B6 | VREF2B6 | V4 | Y2 | W2 | | | HIGH |
| IO | DIFFIO_RX65p | | B6 | VREF2B6 | V3 | W2 | W1 | | | HIGH |
| IO | DIFFIO_TX64n | | B6 | VREF2B6 | T10 | U6 | V5 | | | HIGH |
| IO | DIFFIO_TX64p | | B6 | VREF2B6 | T9 | T6 | V6 | | | HIGH |
| IO | DIFFIO_RX64n | | B6 | VREF2B6 | V1 | AA1 | V4 | | | HIGH |
| IO | DIFFIO_RX64p | | B6 | VREF2B6 | V2 | AB1 | V3 | | | HIGH |
| VREF2B6 | | | B6 | VREF2B6 | R10 | W10 | AA10 | | | |
| IO | DIFFIO_TX63n | | B6 | VREF2B6 | T7 | W5 | V8 | | | HIGH |
| IO | DIFFIO_TX63p | | B6 | VREF2B6 | T8 | V5 | V7 | | | HIGH |
| IO | DIFFIO_RX63n | | B6 | VREF2B6 | U4 | V2 | V2 | | | HIGH |
| IO | DIFFIO_RX63p | | B6 | VREF2B6 | U3 | U2 | V1 | | | HIGH |
| IO | DIFFIO_TX62n | | B6 | VREF2B6 | T4 | T5 | W8 | | | HIGH |
| IO | DIFFIO_TX62p | | B6 | VREF2B6 | T3 | U5 | W7 | | | HIGH |
| IO | DIFFIO_RX62n | | B6 | VREF2B6 | U2 | V1 | U5 | | | HIGH |
| IO | DIFFIO_RX62p | | B6 | VREF2B6 | T1 | U1 | U6 | | | HIGH |
| IO | CLK8n | | B6 | VREF2B6 | R3 | U4 | U3 | | | |
| CLK8p | | | B6 | VREF2B6 | R4 | U3 | U4 | | | |
| CLK9n | | | B6 | VREF2B6 | T2 | T3 | U1 | | | |
| CLK9p | | | B6 | VREF2B6 | R2 | T4 | U2 | | | |
| GNDG_PLL3 | | | | | R7 | V9 | U11 | | | |
| VCCG_PLL3 | | | | | R8 | U9 | V11 | | | |

*Table 4–1. Pin List for the Stratix EP1S30 Device (Part 26 of 52)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| GNDA_PLL3 | | | | | R5 | V8 | U7 | | | |
| GND | | | | | | | | | | |
| VCCA_PLL3 | | | | | R6 | U8 | U8 | | | |
| VCCINT | | | | | | | | | | |
| GNDG_PLL4 | | | | | P7 | R9 | U9 | | | |
| VCCG_PLL4 | | | | | P8 | R10 | T9 | | | |
| GNDA_PLL4 | | | | | P5 | R8 | T7 | | | |
| GND | | | | | | | | | | |
| VCCA_PLL4 | | | | | P6 | T8 | T8 | | | |
| VCCINT | | | | | | | | | | |
| CLK10p | | | B5 | VREF0B5 | P4 | T1 | T6 | | | |
| IO | CLK10n | | B5 | VREF0B5 | P3 | T2 | T5 | | | |
| CLK11p | | | B5 | VREF0B5 | P2 | R3 | T4 | | | |
| CLK11n | | | B5 | VREF0B5 | N2 | R4 | T3 | | | |
| IO | DIFFIO_TX61n | | B5 | VREF0B5 | | | T11 | | | LOW |
| IO | DIFFIO_TX61p | | B5 | VREF0B5 | | | R11 | | | LOW |
| IO | DIFFIO_RX61n | | B5 | VREF0B5 | M2 | R1 | T2 | | | HIGH |
| IO | DIFFIO_RX61p | | B5 | VREF0B5 | N1 | P1 | T1 | | | HIGH |
| IO | DIFFIO_TX60n | | B5 | VREF0B5 | N10 | R7 | R7 | | | HIGH |
| IO | DIFFIO_TX60p | | B5 | VREF0B5 | N9 | T7 | R8 | | | HIGH |
| IO | DIFFIO_RX60n | | B5 | VREF0B5 | M3 | P2 | R1 | | | HIGH |

**Table 4–1. Pin List for the Stratix EP1S30 Device (Part 27 of 52)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **780-Pin FineLine BGA** | **956-Pin BGA** | **1020-Pin FineLine BGA** | **DQS for x16** | **DQS for x32** | **DIFFIO Speed** *Note (1)* |
| IO | DIFFIO_RX60p | | B5 | VREF0B5 | M4 | R2 | R2 | | | HIGH |
| VREF0B5 | | | B5 | VREF0B5 | P10 | P10 | R12 | | | |
| IO | DIFFIO_TX59n | | B5 | VREF0B5 | N5 | P8 | P7 | | | HIGH |
| IO | DIFFIO_TX59p | | B5 | VREF0B5 | N6 | N8 | P8 | | | HIGH |
| IO | DIFFIO_RX59n | | B5 | VREF0B5 | L1 | K1 | R3 | | | HIGH |
| IO | DIFFIO_RX59p | | B5 | VREF0B5 | L2 | L1 | R4 | | | HIGH |
| IO | DIFFIO_TX58n | | B5 | VREF0B5 | N7 | R6 | R5 | | | HIGH |
| IO | DIFFIO_TX58p | | B5 | VREF0B5 | N8 | P6 | R6 | | | HIGH |
| IO | DIFFIO_RX58n | | B5 | VREF0B5 | L3 | N2 | P1 | | | HIGH |
| IO | DIFFIO_RX58p | | B5 | VREF0B5 | L4 | M2 | P2 | | | HIGH |
| IO | DIFFIO_TX57n | | B5 | VREF0B5 | N4 | P9 | R10 | | | HIGH |
| IO | DIFFIO_TX57p | | B5 | VREF0B5 | N3 | N9 | R9 | | | HIGH |
| IO | DIFFIO_RX57n | | B5 | VREF0B5 | K1 | L2 | P3 | | | HIGH |
| IO | DIFFIO_RX57p | | B5 | VREF0B5 | K2 | K2 | P4 | | | HIGH |
| IO | DIFFIO_TX56n | | B5 | VREF0B5 | M10 | P7 | P6 | | | HIGH |
| IO | DIFFIO_TX56p | | B5 | VREF0B5 | M9 | N7 | P5 | | | HIGH |
| IO | DIFFIO_RX56n | | B5 | VREF0B5 | K4 | P3 | N1 | | | HIGH |
| IO | DIFFIO_RX56p | | B5 | VREF0B5 | K3 | N3 | N2 | | | HIGH |
| IO | DIFFIO_TX55n | | B5 | VREF1B5 | M6 | N6 | N7 | | | HIGH |
| IO | DIFFIO_TX55p | | B5 | VREF1B5 | M5 | M6 | N8 | | | HIGH |
| IO | DIFFIO_RX55n | | B5 | VREF1B5 | J1 | L3 | N3 | | | HIGH |

*Table 4–1. Pin List for the Stratix EP1S30 Device (Part 28 of 52)*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | | | |
| IO | DIFFIO_RX55p | | B5 | VREF1B5 | J2 | M3 | N4 | | | HIGH |
| IO | DIFFIO_TX54n | | B5 | VREF1B5 | M8 | R5 | P9 | | | HIGH |
| IO | DIFFIO_TX54p | | B5 | VREF1B5 | M7 | P5 | P10 | | | HIGH |
| IO | DIFFIO_RX54n | | B5 | VREF1B5 | J3 | P4 | M2 | | | HIGH |
| IO | DIFFIO_RX54p | | B5 | VREF1B5 | J4 | N4 | M3 | | | HIGH |
| IO | DIFFIO_TX53n | | B5 | VREF1B5 | L10 | M5 | N5 | | | HIGH |
| IO | DIFFIO_TX53p | | B5 | VREF1B5 | L9 | N5 | N6 | | | HIGH |
| IO | DIFFIO_RX53n | | B5 | VREF1B5 | H1 | M4 | L2 | | | HIGH |
| IO | DIFFIO_RX53p | | B5 | VREF1B5 | H2 | L4 | L3 | | | HIGH |
| IO | DIFFIO_TX52n | | B5 | VREF1B5 | L5 | M8 | N10 | | | HIGH |
| IO | DIFFIO_TX52p | | B5 | VREF1B5 | L6 | L8 | N9 | | | HIGH |
| IO | DIFFIO_RX52n/RDN5 | | B5 | VREF1B5 | H3 | K3 | M4 | | | HIGH |
| IO | DIFFIO_RX52p/RUP5 | | B5 | VREF1B5 | H4 | K4 | M5 | | | HIGH |
| VREF1B5 | | | B5 | VREF1B5 | K9 | N10 | L8 | | | |
| IO | DIFFIO_TX51n | | B5 | VREF1B5 | L8 | M7 | M8 | | | HIGH |
| IO | DIFFIO_TX51p | | B5 | VREF1B5 | L7 | L7 | M9 | | | HIGH |
| IO | DIFFIO_RX51n | | B5 | VREF1B5 | G1 | J1 | L1 | | | HIGH |
| IO | DIFFIO_RX51p | | B5 | VREF1B5 | G2 | H1 | K2 | | | HIGH |
| IO | DIFFIO_TX50n | | B5 | VREF1B5 | K7 | L5 | M6 | | | HIGH |
| IO | DIFFIO_TX50p | | B5 | VREF1B5 | K8 | K5 | M7 | | | HIGH |
| IO | DIFFIO_RX50n | | B5 | VREF1B5 | G4 | G1 | J2 | | | HIGH |

**Table 4–1. Pin List for the Stratix EP1S30 Device (Part 29 of 52)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_RX50p | | B5 | VREF1B5 | G3 | F1 | J1 | | | HIGH |
| IO | DIFFIO_TX49n | | B5 | VREF1B5 | J7 | H5 | L6 | | | HIGH |
| IO | DIFFIO_TX49p | | B5 | VREF1B5 | J8 | J5 | L7 | | | HIGH |
| IO | DIFFIO_RX49n | | B5 | VREF1B5 | F1 | H2 | K4 | | | HIGH |
| IO | DIFFIO_RX49p | | B5 | VREF1B5 | F2 | J2 | K3 | | | HIGH |
| IO | DIFFIO_TX48n | | B5 | VREF1B5 | K5 | F5 | K5 | | | HIGH |
| IO | DIFFIO_TX48p | | B5 | VREF1B5 | K6 | G5 | K6 | | | HIGH |
| IO | DIFFIO_RX48n | | B5 | VREF1B5 | F3 | G2 | J3 | | | HIGH |
| IO | DIFFIO_RX48p | | B5 | VREF1B5 | F4 | F2 | J4 | | | HIGH |
| IO | DIFFIO_TX47n | | B5 | VREF2B5 | J6 | L6 | K8 | | | HIGH |
| IO | DIFFIO_TX47p | | B5 | VREF2B5 | J5 | K6 | K7 | | | HIGH |
| IO | DIFFIO_RX47n | | B5 | VREF2B5 | E1 | J3 | H1 | | | HIGH |
| IO | DIFFIO_RX47p | | B5 | VREF2B5 | E2 | H3 | H2 | | | HIGH |
| IO | DIFFIO_TX46n | | B5 | VREF2B5 | H8 | J6 | J5 | | | HIGH |
| IO | DIFFIO_TX46p | | B5 | VREF2B5 | H7 | H6 | J6 | | | HIGH |
| IO | DIFFIO_RX46n | | B5 | VREF2B5 | D1 | G3 | G1 | | | HIGH |
| IO | DIFFIO_RX46p | | B5 | VREF2B5 | D2 | F3 | G2 | | | HIGH |
| IO | DIFFIO_TX45n | | B5 | VREF2B5 | H6 | G6 | J7 | | | HIGH |
| IO | DIFFIO_TX45p | | B5 | VREF2B5 | H5 | F6 | J8 | | | HIGH |
| IO | DIFFIO_RX45n | | B5 | VREF2B5 | C1 | J4 | H3 | | | HIGH |
| IO | DIFFIO_RX45p | | B5 | VREF2B5 | C2 | H4 | H4 | | | HIGH |

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 30 of 52)

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_TX44n | | B5 | VREF2B5 | G5 | K8 | H5 | | | HIGH |
| IO | DIFFIO_TX44p | | B5 | VREF2B5 | G6 | J8 | H6 | | | HIGH |
| IO | DIFFIO_RX44n | | B5 | VREF2B5 | | G4 | F1 | | | HIGH |
| IO | DIFFIO_RX44p | | B5 | VREF2B5 | | F4 | F2 | | | HIGH |
| VREF2B5 | | | B5 | VREF2B5 | E5 | M10 | F6 | | | |
| IO | DIFFIO_TX43n | | B5 | VREF2B5 | F6 | K7 | H8 | | | HIGH |
| IO | DIFFIO_TX43p | | B5 | VREF2B5 | F5 | J7 | H7 | | | HIGH |
| IO | DIFFIO_RX43n | | B5 | VREF2B5 | | E2 | G3 | | | HIGH |
| IO | DIFFIO_RX43p | | B5 | VREF2B5 | | D2 | G4 | | | HIGH |
| IO | DIFFIO_TX42n | | B5 | VREF2B5 | | H7 | G6 | | | HIGH |
| IO | DIFFIO_TX42p | | B5 | VREF2B5 | | G7 | G5 | | | HIGH |
| IO | DIFFIO_RX42n | | B5 | VREF2B5 | | E3 | F3 | | | HIGH |
| IO | DIFFIO_RX42p | | B5 | VREF2B5 | | D3 | F4 | | | HIGH |
| IO | DIFFIO_TX41n | | B5 | VREF2B5 | | G8 | G7 | | | HIGH |
| IO | DIFFIO_TX41p | | B5 | VREF2B5 | | H8 | G8 | | | HIGH |
| IO | DIFFIO_RX41n | | B5 | VREF2B5 | | | E2 | | | LOW |
| IO | DIFFIO_RX41p | | B5 | VREF2B5 | | | E1 | | | LOW |
| IO | | | B5 | VREF2B5 | | | | | | |
| IO | | | B5 | VREF2B5 | | | | | | |
| FPLL10CLKn | | | B5 | VREF2B5 | | D1 | L5 | | | |
| FPLL10CLKp | | | B5 | VREF2B5 | | E1 | L4 | | | |

**Table 4–1. Pin List for the Stratix EP1S30 Device (Part 31 of 52)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| GNDG_PLL10 | | | | | | K9 | E3 | | | |
| VCCG_PLL10 | | | | | | J9 | D3 | | | |
| GNDA_PLL10 | | | | | | M9 | D1 | | | |
| GND | | | | | | | | | | |
| VCCA_PLL10 | | | | | | L9 | D2 | | | |
| VCCINT | | | | | | | | | | |
| IO | | | B4 | VREF0B4 | | F7 | F7 | | | |
| IO | DQ0T0 | | B4 | VREF0B4 | A4 | C4 | D5 | DQ0T0 | DQ0T0 | |
| IO | | | B4 | VREF0B4 | G7 | E4 | K9 | | | |
| IO | DQ0T1 | | B4 | VREF0B4 | A3 | C5 | C3 | DQ0T1 | DQ0T1 | |
| IO | DQ0T2 | | B4 | VREF0B4 | B3 | D5 | E5 | DQ0T2 | DQ0T2 | |
| IO | DQS0T | | B4 | VREF0B4 | D5 | B4 | C5 | | | |
| IO | | | B4 | VREF0B4 | F7 | H9 | H9 | | | |
| IO | DQ0T3 | | B4 | VREF0B4 | B5 | B5 | C4 | DQ0T3 | DQ0T3 | |
| IO | | | B4 | VREF0B4 | | E5 | J9 | | | |
| IO | DQ0T4 | | B4 | VREF0B4 | B4 | B3 | D4 | DQ0T4 | DQ0T4 | |
| IO | DQ0T5 | | B4 | VREF0B4 | C4 | C3 | A4 | DQ0T5 | DQ0T5 | |
| IO | | | B4 | VREF0B4 | G8 | C2 | L9 | | | |
| IO | DQ0T6 | | B4 | VREF0B4 | A5 | A5 | B4 | DQ0T6 | DQ0T6 | |
| IO | | | B4 | VREF0B4 | F8 | F8 | G9 | | | |
| IO | DQ0T7 | | B4 | VREF0B4 | C5 | A4 | B3 | DQ0T7 | DQ0T7 | |

*Table 4–1. Pin List for the Stratix EP1S30 Device (Part 32 of 52)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | | | B4 | VREF0B4 | | E7 | F8 | | | |
| IO | | | B4 | VREF0B4 | J9 | L11 | M10 | | | |
| IO | DQ1T0 | | B4 | VREF0B4 | E6 | E6 | D6 | DQ0T8 | DQ0T8 | |
| VREF0B4 | | | B4 | VREF0B4 | E7 | K10 | E6 | | | |
| IO | DQ1T1 | | B4 | VREF0B4 | A6 | C7 | C6 | DQ0T9 | DQ0T9 | |
| IO | DQ1T2 | | B4 | VREF0B4 | B7 | D7 | B5 | DQ0T10 | DQ0T10 | |
| IO | | | B4 | VREF0B4 | | J10 | J11 | | | |
| IO | DQS1T | | B4 | VREF0B4 | B6 | C6 | E7 | DQS0T | | |
| IO | | | B4 | VREF0B4 | H9 | D4 | K11 | | | |
| IO | DQ1T3 | | B4 | VREF0B4 | D6 | A6 | C7 | DQ0T11 | DQ0T11 | |
| IO | DQ1T4 | | B4 | VREF0B4 | A7 | B6 | A5 | DQ0T12 | DQ0T12 | |
| IO | | | B4 | VREF0B4 | | J11 | G10 | | | |
| IO | DQ1T5 | | B4 | VREF0B4 | D7 | D6 | D7 | DQ0T13 | DQ0T13 | |
| IO | | | B4 | VREF0B4 | G9 | G9 | F9 | | | |
| IO | DQ1T6 | | B4 | VREF0B4 | C6 | A7 | A6 | DQ0T14 | DQ0T14 | |
| IO | DQ1T7 | | B4 | VREF0B4 | C7 | B7 | B6 | DQ0T15 | DQ0T15 | |
| IO | | | B4 | VREF0B4 | F9 | G10 | F10 | | | |
| IO | | | B4 | VREF0B4 | | F9 | H11 | | | |
| IO | DQ2T0 | | B4 | VREF0B4 | D8 | B8 | B7 | DQ1T0 | DQ0T16 | |
| IO | DQ2T1 | | B4 | VREF0B4 | C8 | D9 | D8 | DQ1T1 | DQ0T17 | |
| IO | | | B4 | VREF0B4 | H10 | H10 | L11 | | | |

*Table 4–1. Pin List for the Stratix EP1S30 Device (Part 33 of 52)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DQ2T2 | | B4 | VREF0B4 | E8 | E8 | B8 | DQ1T2 | DQ0T18 | |
| IO | DQS2T | | B4 | VREF1B4 | C9 | C8 | A7 | | DQS0T | |
| IO | | | B4 | VREF1B4 | | H11 | F12 | | | |
| IO | DQ2T3 | | B4 | VREF1B4 | D9 | C9 | E9 | DQ1T3 | DQ0T19 | |
| IO | DQ2T4 | | B4 | VREF1B4 | B9 | D8 | A8 | DQ1T4 | DQ0T20 | |
| IO | DQ2T5 | | B4 | VREF1B4 | B8 | A9 | C9 | DQ1T5 | DQ0T21 | |
| IO | DQ2T6 | | B4 | VREF1B4 | A8 | B9 | C8 | DQ1T6 | DQ0T22 | |
| IO | FCLK6 | | B4 | VREF1B4 | G10 | F10 | G12 | | | |
| IO | FCLK7 | | B4 | VREF1B4 | F10 | F11 | A14 | | | |
| IO | DQ2T7 | | B4 | VREF1B4 | A9 | A8 | D9 | DQ1T7 | DQ0T23 | |
| IO | | | B4 | VREF1B4 | | J12 | J12 | | | |
| IO | | | B4 | VREF1B4 | J10 | L12 | K12 | | | |
| IO | DQ3T0 | | B4 | VREF1B4 | E10 | B10 | E11 | DQ1T8 | DQ0T24 | |
| VREF1B4 | | | B4 | VREF1B4 | E9 | K11 | E8 | | | |
| IO | DQ3T1 | | B4 | VREF1B4 | A10 | D10 | B9 | DQ1T9 | DQ0T25 | |
| IO | | | B4 | VREF1B4 | F11 | H12 | H13 | | | |
| IO | DQ3T2 | | B4 | VREF1B4 | C10 | E10 | D10 | DQ1T10 | DQ0T26 | |
| IO | | | B4 | VREF1B4 | K10 | E9 | H12 | | | |
| IO | DQS3T | | B4 | VREF1B4 | D10 | C10 | D11 | DQS1T | | |
| IO | DQ3T3 | | B4 | VREF1B4 | B10 | D11 | C10 | DQ1T11 | DQ0T27 | |
| IO | | | B4 | VREF1B4 | | G11 | F13 | | | |

*Table 4–1. Pin List for the Stratix EP1S30 Device (Part 34 of 52)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **780-Pin FineLine BGA** | **956-Pin BGA** | **1020-Pin FineLine BGA** | **DQS for x16** | **DQS for x32** | **DIFFIO Speed** *Note (1)* |
| IO | DQ3T4 | | B4 | VREF1B4 | A11 | E11 | A9 | DQ1T12 | DQ0T28 | |
| IO | DQ3T5 | | B4 | VREF1B4 | C11 | B11 | B11 | DQ1T13 | DQ0T29 | |
| IO | DEV_OE | | B4 | VREF1B4 | J11 | F12 | L13 | | | |
| IO | DQ3T6 | | B4 | VREF1B4 | D11 | C11 | C11 | DQ1T14 | DQ0T30 | |
| IO | DQ3T7 | | B4 | VREF1B4 | B11 | A10 | B10 | DQ1T15 | DQ0T31 | |
| IO | RUP4 | | B4 | VREF1B4 | H11 | F13 | G13 | | | |
| IO | RDN4 | | B4 | VREF1B4 | G11 | E14 | J13 | | | |
| IO | DQ4T0 | | B4 | VREF1B4 | B12 | D12 | A11 | | | |
| IO | | nWS | B4 | VREF1B4 | K11 | F14 | D14 | | | |
| IO | DQ4T1 | | B4 | VREF1B4 | C12 | E12 | B12 | | | |
| IO | DQ4T2 | | B4 | VREF1B4 | D12 | A12 | C12 | | | |
| IO | | | B4 | VREF2B4 | G12 | G12 | H14 | | | |
| IO | DQS4T | | B4 | VREF2B4 | A13 | C12 | D12 | | | |
| IO | | DATA0 | B4 | VREF2B4 | H12 | E15 | E14 | | | |
| IO | DQ4T3 | | B4 | VREF2B4 | B13 | B12 | C13 | | | |
| IO | DQ4T4 | | B4 | VREF2B4 | E12 | C13 | D13 | | | |
| IO | | | B4 | VREF2B4 | L11 | J13 | K13 | | | |
| IO | DQ4T5 | | B4 | VREF2B4 | C13 | D13 | E13 | | | |
| IO | | DATA1 | B4 | VREF2B4 | F12 | C16 | F14 | | | |
| IO | DQ4T6 | | B4 | VREF2B4 | D13 | E13 | A13 | | | |
| IO | DQ4T7 | | B4 | VREF2B4 | E13 | B13 | B13 | | | |

**Table 4–1. Pin List for the Stratix EP1S30 Device (Part 35 of 52)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | | | B4 | VREF2B4 | M11 | L14 | L12 | | | |
| IO | | DATA2 | B4 | VREF2B4 | J12 | F15 | F15 | | | |
| VREF2B4 | | | B4 | VREF2B4 | E11 | K12 | E10 | | | |
| IO | | | B4 | VREF2B4 | | G13 | C14 | | | |
| IO | | | B4 | VREF2B4 | | | B14 | | | |
| IO | | | B4 | VREF2B4 | | | K14 | | | |
| IO | | | B4 | VREF2B4 | | | J14 | | | |
| IO | | | B4 | VREF2B4 | | | L14 | | | |
| IO | | | B4 | VREF2B4 | | H13 | K15 | | | |
| TMS | | TMS | B4 | VREF2B4 | F13 | D16 | E15 | | | |
| TRST | | TRST | B4 | VREF2B4 | L12 | G15 | G15 | | | |
| TCK | | TCK | B4 | VREF2B4 | K12 | F16 | G14 | | | |
| IO | | DATA3 | B4 | VREF2B4 | M12 | G17 | C16 | | | |
| IO | | | B4 | VREF2B4 | | G14 | J15 | | | |
| IO | | | B4 | VREF2B4 | | L16 | L15 | | | |
| TDI | | TDI | B4 | VREF2B4 | G13 | E16 | D16 | | | |
| TDO | | TDO | B4 | VREF2B4 | H13 | G16 | F16 | | | |
| IO | CLK12n | | B4 | VREF2B4 | J13 | B14 | A15 | | | |
| CLK12p | | | B4 | VREF2B4 | K13 | A14 | B15 | | | |
| IO | CLK13n | | B4 | VREF2B4 | L13 | D14 | C15 | | | |
| CLK13p | | | B4 | VREF2B4 | M13 | C14 | D15 | | | |

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 36 of 52)

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| TEMPDIODEp | | | | | B14 | E17 | E18 | | | |
| TEMPDIODEn | | | | | C14 | F17 | F18 | | | |
| VCCINT | | | | | | | | | | |
| VCCA_PLL5 | | | | | F14 | J17 | G17 | | | |
| GND | | | | | | | | | | |
| GNDA_PLL5 | | | | | G14 | H16 | F17 | | | |
| VCCG_PLL5 | | | | | D14 | K15 | J16 | | | |
| GNDG_PLL5 | | | | | E14 | K17 | L16 | | | |
| VCC_PLL5_OUTA | | | B9 | | F15 | L18 | H17 | | | |
| VCC_PLL5_OUTA | | | B9 | | | | | | | |
| VCC_PLL5_OUTB | | | B10 | | G16 | J18 | L17 | | | |
| VCC_PLL5_OUTB | | | B10 | | | | | | | |
| IO | PLL5_OUT0p | | B9 | VREF0B3 | E15 | B16 | B16 | | | |
| IO | PLL5_OUT0n | | B9 | VREF0B3 | D15 | A16 | A16 | | | |
| IO | PLL5_OUT1p | | B9 | VREF0B3 | K14 | B15 | B17 | | | |
| IO | PLL5_OUT1n | | B9 | VREF0B3 | K15 | A15 | A17 | | | |
| IO | PLL5_FBp | | B9 | VREF0B3 | H14 | D15 | D17 | | | |
| IO | PLL5_FBn | | B9 | VREF0B3 | H15 | C15 | C17 | | | |
| IO | PLL5_OUT2p | | B10 | VREF0B3 | C15 | D17 | B18 | | | |
| IO | PLL5_OUT2n | | B10 | VREF0B3 | B15 | C17 | A18 | | | |
| IO | PLL5_OUT3p | | B10 | VREF0B3 | K16 | B17 | D18 | | | |

*Table 4–1. Pin List for the Stratix EP1S30 Device (Part 37 of 52)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **780-Pin FineLine BGA** | **956-Pin BGA** | **1020-Pin FineLine BGA** | **DQS for x16** | **DQS for x32** | **DIFFIO Speed** *Note (1)* |
| IO | PLL5_OUT3n | | B10 | VREF0B3 | J16 | A17 | C18 | | | |
| nSTATUS | | nSTATUS | B3 | VREF0B3 | M16 | E18 | G16 | | | |
| nCONFIG | | nCONFIG | B3 | VREF0B3 | L16 | F19 | J18 | | | |
| DCLK | | DCLK | B3 | VREF0B3 | F16 | F18 | E19 | | | |
| CONF_DONE | | CONF_DONE | B3 | VREF0B3 | G17 | G18 | G18 | | | |
| CLK14p | | | B3 | VREF0B3 | K17 | A18 | A19 | | | |
| IO | CLK14n | | B3 | VREF0B3 | J17 | B18 | B19 | | | |
| CLK15p | | | B3 | VREF0B3 | M17 | C18 | C19 | | | |
| IO | CLK15n | | B3 | VREF0B3 | L17 | D18 | D19 | | | |
| VREF0B3 | | | B3 | VREF0B3 | E18 | K18 | E21 | | | |
| IO | | | B3 | VREF0B3 | | | K18 | | | |
| IO | | | B3 | VREF0B3 | | | F19 | | | |
| IO | | DATA4 | B3 | VREF0B3 | H17 | G19 | G19 | | | |
| IO | | | B3 | VREF0B3 | L18 | H20 | L18 | | | |
| IO | | | B3 | VREF0B3 | M18 | J19 | L21 | | | |
| IO | | | B3 | VREF0B3 | | | L20 | | | |
| IO | | | B3 | VREF0B3 | | | F20 | | | |
| IO | | | B3 | VREF0B3 | F17 | H19 | H19 | | | |
| IO | DQ5T0 | | B3 | VREF0B3 | D16 | B19 | A20 | | | |
| IO | DQ5T1 | | B3 | VREF0B3 | C16 | C19 | B20 | | | |
| IO | | DATA5 | B3 | VREF0B3 | K18 | F20 | J19 | | | |

*Table 4–1. Pin List for the Stratix EP1S30 Device (Part 38 of 52)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **780-Pin FineLine BGA** | **956-Pin BGA** | **1020-Pin FineLine BGA** | **DQS for x16** | **DQS for x32** | **DIFFIO Speed** *Note (1)* |
| IO | DQ5T2 | | B3 | VREF0B3 | E16 | D19 | C20 | | | |
| IO | DQS5T | | B3 | VREF0B3 | A16 | C20 | D20 | | | |
| IO | | | B3 | VREF0B3 | | G22 | H20 | | | |
| IO | DQ5T3 | | B3 | VREF0B3 | B16 | E19 | E20 | | | |
| IO | | DATA6 | B3 | VREF0B3 | H18 | F21 | K19 | | | |
| IO | DQ5T4 | | B3 | VREF0B3 | E17 | A20 | B21 | | | |
| IO | DQ5T5 | | B3 | VREF0B3 | D17 | B20 | C21 | | | |
| IO | | | B3 | VREF1B3 | F18 | G21 | G20 | | | |
| IO | DQ5T6 | | B3 | VREF1B3 | B17 | D20 | D21 | | | |
| IO | | | B3 | VREF1B3 | | | G21 | | | |
| IO | DQ5T7 | | B3 | VREF1B3 | C17 | E20 | A22 | | | |
| IO | RUP3 | | B3 | VREF1B3 | J18 | F22 | F21 | | | |
| IO | RDN3 | | B3 | VREF1B3 | K19 | F24 | L19 | | | |
| IO | DQ6T0 | | B3 | VREF1B3 | A18 | B21 | B22 | DQ2T0 | DQ1T0 | |
| IO | DQ6T1 | | B3 | VREF1B3 | C18 | C21 | C22 | DQ2T1 | DQ1T1 | |
| IO | | DATA7 | B3 | VREF1B3 | G18 | G20 | J20 | | | |
| IO | DQ6T2 | | B3 | VREF1B3 | D18 | A22 | B23 | DQ2T2 | DQ1T2 | |
| IO | DQS6T | | B3 | VREF1B3 | B18 | C22 | D22 | DQS2T | | |
| IO | | | B3 | VREF1B3 | | L19 | L22 | | | |
| IO | DQ6T3 | | B3 | VREF1B3 | A19 | D21 | C23 | DQ2T3 | DQ1T3 | |
| IO | | CLKUSR | B3 | VREF1B3 | J19 | F23 | H21 | | | |

**Table 4–1. Pin List for the Stratix EP1S30 Device (Part 39 of 52)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DQ6T4 | | B3 | VREF1B3 | B19 | E21 | A24 | DQ2T4 | DQ1T4 | |
| IO | | | B3 | VREF1B3 | | J20 | K20 | | | |
| IO | DQ6T5 | | B3 | VREF1B3 | C19 | B22 | E22 | DQ2T5 | DQ1T5 | |
| IO | DQ6T6 | | B3 | VREF1B3 | E19 | D22 | B24 | DQ2T6 | DQ1T6 | |
| VREF1B3 | | | B3 | VREF1B3 | E20 | K19 | E23 | | | |
| IO | FCLK0 | | B3 | VREF1B3 | F19 | E23 | F22 | | | |
| IO | FCLK1 | | B3 | VREF1B3 | G19 | E25 | G22 | | | |
| IO | DQ6T7 | | B3 | VREF1B3 | D19 | E22 | D23 | DQ2T7 | DQ1T7 | |
| IO | | | B3 | VREF1B3 | H19 | H21 | J21 | | | |
| IO | | | B3 | VREF1B3 | | | K21 | | | |
| IO | DQ7T0 | | B3 | VREF1B3 | B20 | A23 | D24 | DQ2T8 | DQ1T8 | |
| IO | DQ7T1 | | B3 | VREF1B3 | A20 | B23 | A25 | DQ2T9 | DQ1T9 | |
| IO | DQ7T2 | | B3 | VREF1B3 | C20 | A24 | C24 | DQ2T10 | DQ1T10 | |
| IO | | | B3 | VREF1B3 | | | F23 | | | |
| IO | DQS7T | | B3 | VREF1B3 | D20 | C24 | B26 | | DQS1T | |
| IO | DQ7T3 | | B3 | VREF1B3 | A21 | C23 | B25 | DQ2T11 | DQ1T11 | |
| IO | | | B3 | VREF1B3 | J20 | H22 | L23 | | | |
| IO | DQ7T4 | | B3 | VREF1B3 | B21 | D24 | C25 | DQ2T12 | DQ1T12 | |
| IO | DQ7T5 | | B3 | VREF1B3 | C21 | B24 | D25 | DQ2T13 | DQ1T13 | |
| IO | | | B3 | VREF1B3 | | J21 | H22 | | | |
| IO | DQ7T6 | | B3 | VREF1B3 | D21 | D23 | A26 | DQ2T14 | DQ1T14 | |

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 40 of 52)

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DQ7T7 | | B3 | VREF1B3 | E21 | E24 | E24 | DQ2T15 | DQ1T15 | |
| IO | | | B3 | VREF1B3 | H20 | G23 | K22 | | | |
| GND | | | B3 | | | | | | | |
| GND | | | B3 | | | | | | | |
| GND | | | B3 | | G20 | D28 | H24 | | | |
| IO | | | B3 | VREF2B3 | | | G23 | | | |
| IO | DQ8T0 | | B3 | VREF2B3 | B22 | A25 | C26 | DQ3T0 | DQ1T16 | |
| IO | DQ8T1 | | B3 | VREF2B3 | A22 | C25 | A28 | DQ3T1 | DQ1T17 | |
| IO | | | B3 | VREF2B3 | | F25 | J22 | | | |
| IO | DQ8T2 | | B3 | VREF2B3 | C22 | B25 | A27 | DQ3T2 | DQ1T18 | |
| IO | DQS8T | | B3 | VREF2B3 | D23 | C26 | B27 | DQS3T | | |
| IO | | | B3 | VREF2B3 | | | F24 | | | |
| IO | DQ8T3 | | B3 | VREF2B3 | D22 | D25 | D26 | DQ3T3 | DQ1T19 | |
| IO | DQ8T4 | | B3 | VREF2B3 | A23 | A26 | C27 | DQ3T4 | DQ1T20 | |
| IO | | | B3 | VREF2B3 | | E27 | K23 | | | |
| IO | DQ8T5 | | B3 | VREF2B3 | C23 | B26 | B28 | DQ3T5 | DQ1T21 | |
| IO | DQ8T6 | | B3 | VREF2B3 | E23 | E26 | D27 | DQ3T6 | DQ1T22 | |
| VREF2B3 | | | B3 | VREF2B3 | E22 | K20 | E25 | | | |
| IO | DQ8T7 | | B3 | VREF2B3 | B23 | D26 | E26 | DQ3T7 | DQ1T23 | |
| IO | | | B3 | VREF2B3 | F20 | J22 | H23 | | | |
| IO | | | B3 | VREF2B3 | | | J23 | | | |

**Table 4–1. Pin List for the Stratix EP1S30 Device (Part 41 of 52)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DQ9T0 | | B3 | VREF2B3 | A24 | B27 | A29 | DQ3T8 | DQ1T24 | |
| IO | | | B3 | VREF2B3 | | | L24 | | | |
| IO | DQ9T1 | | B3 | VREF2B3 | C25 | C27 | B29 | DQ3T9 | DQ1T25 | |
| IO | | | B3 | VREF2B3 | F21 | H23 | G24 | | | |
| IO | DQ9T2 | | B3 | VREF2B3 | A25 | A27 | B30 | DQ3T10 | DQ1T26 | |
| IO | DQS9T | | B3 | VREF2B3 | C24 | B28 | C28 | | | |
| IO | | | B3 | VREF2B3 | G21 | C30 | F25 | | | |
| IO | DQ9T3 | | B3 | VREF2B3 | D24 | D27 | C29 | DQ3T11 | DQ1T27 | |
| IO | | | B3 | VREF2B3 | G22 | L21 | J24 | | | |
| IO | DQ9T4 | | B3 | VREF2B3 | B24 | A28 | D29 | DQ3T12 | DQ1T28 | |
| IO | DQ9T5 | | B3 | VREF2B3 | B25 | C28 | D28 | DQ3T13 | DQ1T29 | |
| IO | DQ9T6 | | B3 | VREF2B3 | A26 | C29 | C30 | DQ3T14 | DQ1T30 | |
| IO | | | B3 | VREF2B3 | F22 | E28 | F26 | | | |
| IO | DQ9T7 | | B3 | VREF2B3 | B26 | B29 | E28 | DQ3T15 | DQ1T31 | |
| IO | | | B3 | VREF2B3 | | | K24 | | | |
| VCCIO2 | | | | | B28 | C31 | C31 | | | |
| VCCIO2 | | | | | M28 | N31 | C32 | | | |
| VCCIO2 | | | | | P20 | T23 | M32 | | | |
| VCCIO2 | | | | | | | T23 | | | |
| VCCIO1 | | | | | R20 | U20 | AA32 | | | |
| VCCIO1 | | | | | U28 | W31 | AK31 | | | |

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 42 of 52)

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| VCCIO1 | | | | | AG28 | AJ31 | AK32 | | | |
| VCCIO1 | | | | | | | U23 | | | |
| VCCIO8 | | | | | Y15 | AL29 | AC17 | | | |
| VCCIO8 | | | | | AH17 | AL19 | AM21 | | | |
| VCCIO8 | | | | | AH27 | Y17 | AM30 | | | |
| VCCIO7 | | | | | Y14 | AC16 | AC16 | | | |
| VCCIO7 | | | | | AH2 | AL13 | AM12 | | | |
| VCCIO7 | | | | | AH12 | AL3 | AM3 | | | |
| VCCIO6 | | | | | R9 | AJ1 | AA1 | | | |
| VCCIO6 | | | | | U1 | W1 | AK1 | | | |
| VCCIO6 | | | | | AG1 | U12 | AK2 | | | |
| VCCIO6 | | | | | | | U10 | | | |
| VCCIO5 | | | | | B1 | T9 | C1 | | | |
| VCCIO5 | | | | | M1 | N1 | C2 | | | |
| VCCIO5 | | | | | P9 | C1 | M1 | | | |
| VCCIO5 | | | | | | | T10 | | | |
| VCCIO4 | | | | | A2 | A3 | A12 | | | |
| VCCIO4 | | | | | A12 | A13 | A3 | | | |
| VCCIO4 | | | | | J14 | J16 | K16 | | | |
| VCCIO3 | | | | | A17 | M17 | A21 | | | |
| VCCIO3 | | | | | A27 | A19 | A30 | | | |

*Table 4–1. Pin List for the Stratix EP1S30 Device (Part 43 of 52)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| VCCIO3 | | | | | J15 | A29 | K17 | | | |
| VCCINT | | | | | M14 | AA12 | M12 | | | |
| VCCINT | | | | | N11 | AA14 | M14 | | | |
| VCCINT | | | | | N13 | AA20 | M19 | | | |
| VCCINT | | | | | N15 | L13 | M21 | | | |
| VCCINT | | | | | N17 | L20 | N13 | | | |
| VCCINT | | | | | P12 | M11 | N15 | | | |
| VCCINT | | | | | P14 | M13 | N18 | | | |
| VCCINT | | | | | P16 | M15 | N20 | | | |
| VCCINT | | | | | R13 | M19 | P12 | | | |
| VCCINT | | | | | R15 | M21 | P14 | | | |
| VCCINT | | | | | R17 | N12 | P16 | | | |
| VCCINT | | | | | T12 | N14 | P17 | | | |
| VCCINT | | | | | T14 | N16 | P19 | | | |
| VCCINT | | | | | T16 | N18 | P21 | | | |
| VCCINT | | | | | T18 | N20 | R13 | | | |
| VCCINT | | | | | U11 | P11 | R15 | | | |
| VCCINT | | | | | U13 | P13 | R18 | | | |
| VCCINT | | | | | U15 | P14 | R20 | | | |
| VCCINT | | | | | U17 | P15 | T14 | | | |
| VCCINT | | | | | V12 | P17 | T16 | | | |

*Table 4–1. Pin List for the Stratix EP1S30 Device (Part 44 of 52)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **780-Pin FineLine BGA** | **956-Pin BGA** | **1020-Pin FineLine BGA** | **DQS for x16** | **DQS for x32** | **DIFFIO Speed** *Note (1)* |
| VCCINT | | | | | V16 | P19 | T17 | | | |
| VCCINT | | | | | | P21 | T19 | | | |
| VCCINT | | | | | | R12 | U14 | | | |
| VCCINT | | | | | | R13 | U16 | | | |
| VCCINT | | | | | | R14 | U17 | | | |
| VCCINT | | | | | | R18 | U19 | | | |
| VCCINT | | | | | | R19 | V13 | | | |
| VCCINT | | | | | | R20 | V15 | | | |
| VCCINT | | | | | | T11 | V18 | | | |
| VCCINT | | | | | | T13 | V20 | | | |
| VCCINT | | | | | | T19 | W14 | | | |
| VCCINT | | | | | | T21 | W16 | | | |
| VCCINT | | | | | | U10 | W17 | | | |
| VCCINT | | | | | | U14 | W19 | | | |
| VCCINT | | | | | | U18 | Y13 | | | |
| VCCINT | | | | | | U22 | Y15 | | | |
| VCCINT | | | | | | V11 | Y18 | | | |
| VCCINT | | | | | | V13 | Y20 | | | |
| VCCINT | | | | | | V15 | | | | |
| VCCINT | | | | | | V17 | | | | |
| VCCINT | | | | | | V19 | | | | |

**Table 4–1. Pin List for the Stratix EP1S30 Device (Part 45 of 52)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| VCCINT | | | | | | V21 | | | | |
| VCCINT | | | | | | W12 | | | | |
| VCCINT | | | | | | W14 | | | | |
| VCCINT | | | | | | W16 | | | | |
| VCCINT | | | | | | W18 | | | | |
| VCCINT | | | | | | W20 | | | | |
| VCCINT | | | | | | Y11 | | | | |
| VCCINT | | | | | | Y13 | | | | |
| VCCINT | | | | | | Y15 | | | | |
| VCCINT | | | | | | Y19 | | | | |
| VCCINT | | | | | | Y21 | | | | |
| GND | | | | | A14 | A1 | A10 | | | |
| GND | | | | | A15 | A11 | A2 | | | |
| GND | | | | | AA16 | A2 | A23 | | | |
| GND | | | | | AC15 | A21 | A31 | | | |
| GND | | | | | AF26 | A30 | AA16 | | | |
| GND | | | | | AF3 | A31 | AA17 | | | |
| GND | | | | | AG2 | AA17 | AC1 | | | |
| GND | | | | | AG27 | AA18 | AC32 | | | |
| GND | | | | | AH14 | AB16 | AD17 | | | |
| GND | | | | | AH15 | AD18 | AF17 | | | |

**Table 4–1. Pin List for the Stratix EP1S30 Device (Part 46 of 52)**

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | | | |
| GND | | | | | B2 | AK1 | AL1 | | | |
| GND | | | | | B27 | AK2 | AL2 | | | |
| GND | | | | | C26 | AK30 | AL31 | | | |
| GND | | | | | C3 | AK31 | AL32 | | | |
| GND | | | | | G15 | AL1 | AM10 | | | |
| GND | | | | | H16 | AL11 | AM2 | | | |
| GND | | | | | L14 | AL2 | AM23 | | | |
| GND | | | | | L15 | AL21 | AM31 | | | |
| GND | | | | | M15 | AL30 | B1 | | | |
| GND | | | | | N12 | AL31 | B2 | | | |
| GND | | | | | N14 | B1 | B31 | | | |
| GND | | | | | N16 | B2 | B32 | | | |
| GND | | | | | N18 | B30 | H18 | | | |
| GND | | | | | P1 | B31 | J17 | | | |
| GND | | | | | P11 | H17 | K1 | | | |
| GND | | | | | P13 | H18 | K32 | | | |
| GND | | | | | P15 | K16 | M13 | | | |
| GND | | | | | P17 | L15 | M15 | | | |
| GND | | | | | P18 | L17 | M16 | | | |
| GND | | | | | P28 | M1 | M17 | | | |
| GND | | | | | R1 | M12 | M18 | | | |

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 47 of 52)

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| GND | | | | | R11 | M14 | M20 | | | |
| GND | | | | | R12 | M16 | N12 | | | |
| GND | | | | | R14 | M18 | N14 | | | |
| GND | | | | | R16 | M20 | N16 | | | |
| GND | | | | | R18 | M31 | N17 | | | |
| GND | | | | | R28 | N11 | N19 | | | |
| GND | | | | | T11 | N13 | N21 | | | |
| GND | | | | | T13 | N15 | P13 | | | |
| GND | | | | | T15 | N17 | P15 | | | |
| GND | | | | | T17 | N19 | P18 | | | |
| GND | | | | | U12 | N21 | P20 | | | |
| GND | | | | | U14 | P12 | R14 | | | |
| GND | | | | | U16 | P16 | R16 | | | |
| GND | | | | | U18 | P18 | R17 | | | |
| GND | | | | | V13 | P20 | R19 | | | |
| GND | | | | | V14 | R11 | T12 | | | |
| GND | | | | | V15 | R15 | T13 | | | |
| GND | | | | | V17 | R17 | T15 | | | |
| GND | | | | | | R21 | T18 | | | |
| GND | | | | | | T10 | T20 | | | |
| GND | | | | | | T12 | T21 | | | |

**Table 4–1. Pin List for the Stratix EP1S30 Device (Part 48 of 52)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| GND | | | | | | T14 | U12 | | | |
| GND | | | | | | T18 | U13 | | | |
| GND | | | | | | T20 | U15 | | | |
| GND | | | | | | T22 | U18 | | | |
| GND | | | | | | U11 | U20 | | | |
| GND | | | | | | U13 | U21 | | | |
| GND | | | | | | U15 | V14 | | | |
| GND | | | | | | U17 | V16 | | | |
| GND | | | | | | U19 | V17 | | | |
| GND | | | | | | U21 | V19 | | | |
| GND | | | | | | V12 | W13 | | | |
| GND | | | | | | V14 | W15 | | | |
| GND | | | | | | V16 | W18 | | | |
| GND | | | | | | V18 | W20 | | | |
| GND | | | | | | V20 | Y14 | | | |
| GND | | | | | | W11 | Y16 | | | |
| GND | | | | | | W13 | Y17 | | | |
| GND | | | | | | W15 | Y19 | | | |
| GND | | | | | | W17 | | | | |
| GND | | | | | | W19 | | | | |
| GND | | | | | | W21 | | | | |

**Table 4–1. Pin List for the Stratix EP1S30 Device (Part 49 of 52)**

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | | | |
| GND | | | | | | Y1 | | | | |
| GND | | | | | | Y12 | | | | |
| GND | | | | | | Y14 | | | | |
| GND | | | | | | Y16 | | | | |
| GND | | | | | | Y18 | | | | |
| GND | | | | | | Y20 | | | | |
| GND | | | | | | Y31 | | | | |
| No connection | | | | | AC25 | AA22 | AA11 | | | |
| No connection | | | | | AC26 | AB10 | AA13 | | | |
| No connection | | | | | AC3 | AB11 | AB10 | | | |
| No connection | | | | | AC4 | AB15 | AB12 | | | |
| No connection | | | | | AD25 | AB18 | AC11 | | | |
| No connection | | | | | AD26 | AB19 | AD10 | | | |
| No connection | | | | | AD3 | AC14 | AD11 | | | |
| No connection | | | | | AD4 | AC15 | AE10 | | | |
| No connection | | | | | D25 | AD14 | AE16 | | | |
| No connection | | | | | D26 | H14 | AE22 | | | |
| No connection | | | | | D3 | H15 | AF11 | | | |
| No connection | | | | | D4 | J14 | AF16 | | | |
| No connection | | | | | E25 | J15 | AG16 | | | |
| No connection | | | | | E26 | K13 | AG25 | | | |

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 50 of 52)

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **780-Pin FineLine BGA** | **956-Pin BGA** | **1020-Pin FineLine BGA** | **DQS for x16** | **DQS for x32** | **DIFFIO Speed** *Note (1)* |
| No connection | | | | | E3 | K14 | AG26 | | | |
| No connection | | | | | E4 | K21 | AG27 | | | |
| No connection | | | | | | K22 | AG28 | | | |
| No connection | | | | | | L10 | AG5 | | | |
| No connection | | | | | | P22 | AG7 | | | |
| No connection | | | | | | V10 | AG8 | | | |
| No connection | | | | | | | AH1 | | | |
| No connection | | | | | | | AH16 | | | |
| No connection | | | | | | | AH2 | | | |
| No connection | | | | | | | AH21 | | | |
| No connection | | | | | | | AH29 | | | |
| No connection | | | | | | | AH31 | | | |
| No connection | | | | | | | AH32 | | | |
| No connection | | | | | | | AH4 | | | |
| No connection | | | | | | | AH6 | | | |
| No connection | | | | | | | E12 | | | |
| No connection | | | | | | | E16 | | | |
| No connection | | | | | | | E17 | | | |
| No connection | | | | | | | E27 | | | |
| No connection | | | | | | | E29 | | | |
| No connection | | | | | | | E4 | | | |

*Table 4–1. Pin List for the Stratix EP1S30 Device (Part 51 of 52)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **780-Pin FineLine BGA** | **956-Pin BGA** | **1020-Pin FineLine BGA** | **DQS for x16** | **DQS for x32** | **DIFFIO Speed** *Note (1)* |
| No connection | | | | | | | F11 | | | |
| No connection | | | | | | | F28 | | | |
| No connection | | | | | | | F5 | | | |
| No connection | | | | | | | G11 | | | |
| No connection | | | | | | | H10 | | | |
| No connection | | | | | | | H15 | | | |
| No connection | | | | | | | H16 | | | |
| No connection | | | | | | | J10 | | | |
| No connection | | | | | | | K10 | | | |
| No connection | | | | | | | L10 | | | |
| No connection | | | | | | | M11 | | | |
| No connection | | | | | | | N11 | | | |
| No connection | | | | | | | N22 | | | |
| No connection | | | | | | | P11 | | | |
| No connection | | | | | | | P22 | | | |
| No connection | | | | | | | U22 | | | |
| No connection | | | | | | | V12 | | | |
| No connection | | | | | | | V22 | | | |
| No connection | | | | | | | W11 | | | |
| No connection | | | | | | | W12 | | | |
| No connection | | | | | | | W21 | | | |

**Table 4–1. Pin List for the Stratix EP1S30 Device (Part 52 of 52)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FineLine BGA | 956-Pin BGA | 1020-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| No connection | | | | | | | W22 | | | |
| No connection | | | | | | | Y11 | | | |
| No connection | | | | | | | Y12 | | | |
| No connection | | | | | | | Y21 | | | |
| No connection | | | | | | | Y22 | | | |

*Note to Table 4–1:*

(1) The wire bond and flip-chip packages have different data rates for the high speed differential I/O channels. Table 4–2 shows the data rates as supported for each package.

**Table 4–2. High Speed Differential I/O Channel Data Rates**

| Package | Package Type | High Speed Differential I/O Channel Performance (DIFFIO Speed) | | Units |
|---|---|---|---|---|
| | | High | Low | |
| 780-pin FineLine BGA | flip chip | 840 | N/A | Mbps |
| 956-pin BGA | flip chip | 840 | N/A | Mbps |
| 1020-pin FineLine BGA | flip chip | 840 | 462 | Mbps |

## Pin Definitions

Table 4–3 shows pin definitions for the EP1S30 device.

*Table 4–3. Pin Definitions for the EP1S30 Device (Part 1 of 5)*

| Pin Name | Pin Type (1st, 2nd, & 3rd Function) | Pin Description |
|---|---|---|
| **Supply and Reference Pins** | | |
| VREF[1..4]B[1..8] | Input | Input reference voltage for each I/O bank. If a bank is used for a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for that bank. All of the VREF pins within a bank are shorted together. Each VREF pin can support up to 20 inputs on each side. If VREF pins are not used, designers should connect them to either VCC or Gnd. |
| VCCIO[1..8] | Power | These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards. VCCIO also supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5-V, 1.8-V, 2.5-V, 3.3-V PCI, and 3.3-V PCI-X I/O standards. |
| VCCINT | Power | These are internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVDS, LVPECL, 3.3-V PCML, HyperTransport™ technology, differential HSTL, GTL, GTL+, HSTL, SSTL, CTT, and 3.3-V AGP I/O standards. |
| VCC_PLL5_OUTA | Power | External clock output buffer power for PLL5 clock outputs PLL5_OUT[1..0]. The designer must connect this pin to the VCCIO of bank 9. |
| VCC_PLL5_OUTB | Power | External clock output buffer power for PLL5 clock outputs PLL5_OUT[3..2]. The designer must connect this pin to the VCCIO of bank 10. |
| VCC_PLL6_OUTA | Power | External clock output buffer power for PLL6 clock outputs PLL6_OUT[1..0]. The designer must connect this pin to the VCCIO of bank 11. |
| VCC_PLL6_OUTB | Power | External clock output buffer power for PLL6 clock outputs PLL6_OUT[3..2]. The designer must connect this pin to the VCCIO of bank 12. |
| VCCA_PLL[1..12] | Power | Analog power for PLLs[1..12]. The designer must connect this pin to 1.5 V, even if the PLL is not used. |
| GNDA_PLL[1..12] | Ground | Analog ground for PLLs[1..12]. The designer can connect this pin to the GND plane on the board. |
| VCCG_PLL[1..12] | Power | Guard ring power for PLLs[1..12]. The designer must connect this pin to 1.5 V, even if the PLL is not used. |
| GNDG_PLL[1..12] | Ground | Guard ring ground for PLLs[1..12]. The designer can connect this pin to the GND plane on the board. |

*Table 4–3. Pin Definitions for the EP1S30 Device (Part 2 of 5)*

| Pin Name | Pin Type (1st, 2nd, & 3rd Function) | Pin Description |
|---|---|---|
| **Dedicated & Configuration/JTAG Pins** | | |
| CONF_DONE | Bidirectional (open-drain) | This is a dedicated configuration status pin; it is not available as a user I/O pin. |
| nSTATUS | Bidirectional (open-drain) | This is a dedicated configuration status pin; it is not available as a user I/O pin. |
| nCONFIG | Input | Dedicated configuration control input. A low transition resets the target device; a low-to-high transition begins configuration. All I/O pins tri-state when nCONFIG is driven low. |
| DCLK | Input | Clock input used to clock configuration data from an external source into the Stratix device. This is a dedicated pin used for configuration. |
| nIO_PULLUP | Input | IF nIO_PULLUP is driven high during configuration, the weak pull-ups on all user I/O pins are disabled. If driven low, the weak pull-ups are enabled during configuration. nIO_PULLUP can be pulled up to either 1.5, 1.8, 2.5, or 3.3 V. |
| PORSEL | Input | Dedicated input pin used to select POR delay times of 2 ms or 100 ms during powerup. When PORSEL is connected to ground, the POR time is 100 ms. When PORSEL is connected to 3.3 V, the POR time is 2 ms. |
| VCCSEL | Input | VCCSEL is used to select which input buffer is used on all configuration pins. VCCSEL will control whether the 3.3-/2.5-V input buffer or the 1.8-/1.5-V input buffer is used. A "0" means 3.3/2.5 V and a "1" means 1.8-/1.5 V. At powerup, VCCSEL accepts 3.3V and 2.5V TTL Levels. VCCSEL affects the following pins: TDI, TMS, TCK, TRST, MSEL0, MSEL1, MSEL2, nCONFIG, nCE, DCLK, CONF_DONE, nSTATUS, and PLL_ENA. |
| nCE | Input | Active-low chip enables. Dedicated chip enable input used to detect which device is active in a chain of devices. When nCE is low, the device is enabled. When nCE is high, the device is disabled. |
| nCEO | Output | Output that drives low when device configuration is complete. During multi-device configuration, this pin feeds a subsequent device's nCE pin. |
| TMS | Input | This is a dedicated JTAG input pin. |
| TDI | Input | This is a dedicated JTAG input pin. |
| TCK | Input | This is a dedicated JTAG input pin. |

**Table 4–3. Pin Definitions for the EP1S30 Device (Part 3 of 5)**

| Pin Name | Pin Type (1st, 2nd, & 3rd Function) | Pin Description |
|---|---|---|
| TDO | Output | This is a dedicated JTAG input pin. |
| TRST | Input | This is a dedicated JTAG input pin. Active low input, used to asynchronously reset the JTAG boundary scan circuit. |
| MSEL[2..0] | Input | Dedicated mode select control pins that set the configuration mode for the device. |
| TEMPDIODEp | Input | Pin used in conjunction with the temperature sensing diode (bias-high input) inside the Stratix device. If the temperature sensing diode is not used then connect this pin to GND. |
| TEMPDIODEn | Input | Pin used in conjunction with the temperature sensing diode (bias-low input) inside the Stratix device. If the temperature sensing diode is not used then connect this pin to GND. |
| **Clock and PLL Pins** | | |
| PLL_ENA | Input | Dedicated input pin that drives the optional pllena port of all or a set of PLLs. If a PLL uses the pllena port, drive the PLL_ENA pin low to reset all PLLs including the counters to their default state. If VCCSEL = 0, then you must drive the PLL_ENA with a 3.3/2.5 V signal to enable the PLLs. If VCCSEL = 1, connect PLL_ENA to 1.8/1.5 V to enable the PLLs. |
| FCLK[7..0] | Bidirectional | Optional fast regional clock pins. FCLK pins can also be used as type input, output, or as bidirectional pins. |
| FPLL[10..7]CLKp | Input | Dedicated global clock inputs for fast PLLs (PLLs 7 through 10). |
| FPLL[10..7]CLKn | Input | Dedicated negative terminal associated with FPLL[10..7]CLKp pins. |
| CLK[15..0]p | Input | Dedicated global clock inputs 0 to 15. |
| CLK[15..0]n | I/O, Input | Optional negative terminal input for differential global clock input. |
| PLL6_OUT[3..0]p | I/O, Output | Optional external clock outputs [3..0] from enhanced PLL 6. These pins can be differential (four output pin pairs) or single ended (eight clock outputs from PLL6). |
| PLL6_OUT[3..0]n | I/O, Output | Optional negative terminal for external clock outputs [3..0] from PLL6. If the clock outputs are single ended, then each pair of pins (i.e., PLL6_OUT0p and PLL6_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase. |
| PLL5_OUT[3..0]p | I/O, Output | Optional external clock outputs [3..0] from enhanced PLL 5. These pins can be differential (four output pin pairs) or single ended (eight clock outputs from PLL5). |

*Table 4–3. Pin Definitions for the EP1S30 Device (Part 4 of 5)*

| Pin Name | Pin Type (1st, 2nd, & 3rd Function) | Pin Description |
|---|---|---|
| PLL5_OUT[3..0]n | I/O, Output | Optional negative terminal for external clock outputs [3..0] from PLL 5. If the clock outputs are single ended, then each pair of pins (i.e., PLL5_OUT0p and PLL5_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase. |
| **Optional/Dual-Purpose Pins** | | |
| DATA0 | I/O, Input | Dual-purpose configuration data input pin. Can be used as an I/O pin after configuration is complete. |
| DIFFIO_TX[0..151]n | I/O, Output | This pin can be used as the complementary signal of the differential inputs and outputs. If not used for the differential pair, these pins are regular I/O pins. Pins with an n suffix carry the negative signal for the differential channel. Pins with a p suffix carry the positive signal for the differential channel. |
| PLL5_FBp | I/O, Input | External feedback input pin for PLL5. This pin can be used as a user I/O pin if external feedback mode is not used. |
| PLL5_FBn | I/O, Input | Negative terminal input for external feedback input PLL5_FBp. |
| PLL6_FBp | I/O, Input | External feedback input pin for PLL6. |
| PLL6_FBn | I/O, Input | Negative terminal input for external feedback input PLL6_FBp. |
| INIT_DONE | I/O, Output | This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration. |
| DATA[7..1] | I/O, Input | Dual-purpose configuration input data pins. These pins can be used for configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration. |
| nRS | I/O, Input | Read strobe input pin. This pin can be used as a user I/O pin after configuration. |
| DEV_CLRn | I/O, Input | Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as defined in the users design. |
| DEV_OE | I/O, Input | Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design. |
| CLKUSR | I/O, Input | Optional user-supplied clock input. Synchronizes the initialization of one or more devices. This pin can be used as a user I/O pin after configuration. |

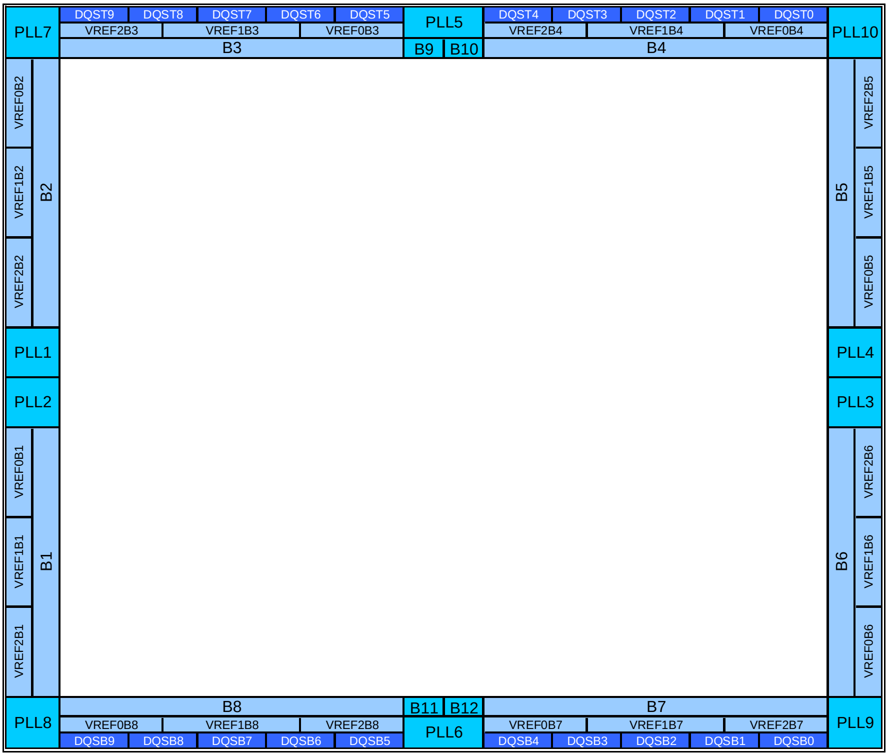
*Table 4–3. Pin Definitions for the EP1S30 Device (Part 5 of 5)*

| Pin Name | Pin Type (1st, 2nd, & 3rd Function) | Pin Description |
|---|---|---|
| RDYnBSY | I/O, Output | Ready not busy output. A high output indicates that the target device is ready to accept another data byte. A low output indicates that the target device is not ready to receive another data byte. This pin can be used as a user I/O pin after configuration |
| nCS,CS | I/O, Input | These are chip-select inputs that enable the Stratix device in the passive parallel asynchronous configuration mode. Drive nCS low and CS high to target a device for configuration. If a design requires an active high enable, use the CS pin and drive the nCS pin low. If a design requires an active low enable, use the nCS pin and drive the CS pin high. Configuration will be paused when either signal is inactive. Hold the nCS and CS pins active during configuration and initialization. The design can use these pins as user I/O pins after configuration. |
| nWS | I/O, Input | Active-low write strobe input to latch a byte of data on the DATA pins. This pin can be used as a user I/O pin after configuration. |
| PGM[2..0] | I/O, Output | These output pins control one of eight pages in the EPC16 configuration device when using remote update or local update configuration modes. When not using remote update or local update configuration modes, these pins are user I/O pins. |
| RUP[8..1] | I/O, Input | Reference pins for banks 8 to 1. The external precision resistors $R_{UP}$ must be connected to the designated RUP pin on that I/O bank. If not required, these pins are regular I/O pins. |
| RDN[8..1] | I/O, Input | Reference pins for banks 8 to 1. The external precision resistors RDN must be connected to the designated RDN pin on that I/O bank. If not required, these pins are regular I/O pins. |
| RUnLU | I/O, Input | Input control pin to select remote update or local update modes. If MSEL2 = 1, this is a input control pin to select remote update (RUnLU =1) or local update (RUnLU =0) modes. If MSEL2 = 0, the RUnLU pin is a user I/O pin. |

## PLL & Bank Diagram

Figure 4–1 shows the PLL and bank locations for the EP1S30 device.

*Figure 4–1. PLL and Bank Diagram* *Notes (1), (2)*



*Notes for Figure 4–1:*

(1) This is a top view of the silicon die. For flip chip packages the die is mounted upside down in the package.

(2) This is a pictoral representation only, to give an idea of placement on the device. Refer to the pinlist and the Quartus II software for exact locations.

## Fast PLL to High-Speed I/O Connections

Table 4–4 shows the number of shows the number of high-speed differential I/O channels that can be driven by each Fast PLL for the EP1S30 device.

*Table 4–4. Fast PLL Connections for the EP1S30 Device*

| Device | Pin Count | FAST PLL Source Location | Number of Rx Channels *(1) (5)* | Number of Tx Channels *(2) (5)* | Number of Overlapped Rx Channels *(3) (5)* | Number of Overlapped Tx Channels *(4) (5)* |
|---|---|---|---|---|---|---|
| EP1S30 | 780 | PLL1 | 16/0 | 18/0 | | |
| | | PLL2 | 16/0 | 17/0 | | |
| | | PLL3 | 16/0 | 17/0 | | |
| | | PLL4 | 16/0 | 18/0 | | |
| | 956 | PLL1 | 20/0 | 19/0 | 19/0 | 19/0 |
| | | PLL2 | 20/0 | 20/0 | 20/0 | 20/0 |
| | | PLL3 | 20/0 | 20/0 | 20/0 | 20/0 |
| | | PLL4 | 20/0 | 19/0 | 19/0 | 19/0 |
| | | PLL7 | 19/0 | 20/0 | 19/0 | 19/0 |
| | | PLL8 | 20/0 | 20/0 | 20/0 | 20/0 |
| | | PLL9 | 20/0 | 20/0 | 20/0 | 20/0 |
| | | PLL10 | 19/0 | 20/0 | 19/0 | 19/0 |
| | 1020 | PLL1 | 20/0 | 19/1 | 19/0 | 19/0 |
| | | PLL2 | 20/0 | 20/0 | 20/0 | 20/0 |
| | | PLL3 | 20/0 | 20/0 | 20/0 | 20/0 |
| | | PLL4 | 20/0 | 19/1 | 19/0 | 19/0 |
| | | PLL7 | 19/1 | 20/0 | 19/0 | 19/0 |
| | | PLL8 | 20/0 | 20/0 | 20/0 | 20/0 |
| | | PLL9 | 20/0 | 20/0 | 20/0 | 20/0 |
| | | PLL10 | 19/1 | 20/0 | 19/0 | 19/0 |

*Notes for Table 4–4:*

(1) This is the total number of Rx channels that the PLL listed in the "FAST PLL Source location" column can drive.

(2) This is the total number of Tx channels that the PLL listed in the "FAST PLL Source location" column can drive.

(3) This is the number of Rx channels that can be driven by the PLL listed in the "FAST PLL Source location" that could alternatively be driven by the other adjacent FAST PLL.

(4) This is the number of Tx channels that can be driven by the PLL listed in the "FAST PLL Source location" that could alternatively be driven by the other adjacent FAST PLL.

(5) The counts are reported in the format of (high speed channels)/(low speed channels).

# 5. Stratix EP1S40 Device Pin Information

S5V3005-1.0

## Introduction

The following tables contain pin information for the Stratix EP1S40 device, organized into the following sections:

# Pin List

Table 5–1 shows the complete pin list for the EP1S40 device:

Table 5–1. Pin List for the Stratix EP1S40 Device (Part 1 of 71)

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed Note (1) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | | | |
| VCCINT | | | | | VCC | VCC | VCC | VCC | | | |
| VCCA_PLL7 | | | | | | L23 | D31 | J31 | | | |
| GND | | | | | GND | GND | GND | GND | | | |
| GNDA_PLL7 | | | | | | M23 | D32 | K31 | | | |
| VCCG_PLL7 | | | | | | J23 | D30 | L30 | | | |
| GNDG_PLL7 | | | | | | K23 | E30 | L31 | | | |
| FPLL7CLKp | | | B2 | VREF0B2 | | E31 | L29 | J38 | | | |
| FPLL7CLKn | | | B2 | VREF0B2 | | D31 | L28 | J39 | | | |
| IO | | | B2 | VREF0B2 | | | | N30 | | | |
| IO | | | B2 | VREF0B2 | | | | N31 | | | |
| IO | DIFFIO_RX44p | | B2 | VREF0B2 | | | E29 | G39 | | | LOW |
| IO | DIFFIO_RX44n | | B2 | VREF0B2 | | | F28 | G38 | | | LOW |
| IO | DIFFIO_TX44p | | B2 | VREF0B2 | D25 | K24 | G25 | M30 | | | HIGH |
| IO | DIFFIO_TX44n | | B2 | VREF0B2 | D26 | J24 | G26 | M31 | | | HIGH |
| IO | DIFFIO_RX43p | | B2 | VREF0B2 | | | E32 | H39 | | | LOW |
| IO | DIFFIO_RX43n | | B2 | VREF0B2 | | | E31 | H38 | | | LOW |
| IO | DIFFIO_TX43p | | B2 | VREF0B2 | E25 | K25 | G28 | J32 | | | HIGH |
| IO | DIFFIO_TX43n | | B2 | VREF0B2 | E26 | J25 | G27 | J33 | | | HIGH |
| IO | DIFFIO_RX42p | | B2 | VREF0B2 | C27 | F28 | F29 | K36 | | | HIGH |
| IO | DIFFIO_RX42n | | B2 | VREF0B2 | C28 | G28 | F30 | K37 | | | HIGH |

*Table 5–1. Pin List for the Stratix EP1S40 Device (Part 2 of 71)*

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_TX42p | | B2 | VREF0B2 | F24 | H24 | H28 | K32 | | | HIGH |
| IO | DIFFIO_TX42n | | B2 | VREF0B2 | F23 | G24 | H27 | K33 | | | HIGH |
| VREF0B2 | | | B2 | VREF0B2 | E24 | L22 | F27 | M29 | | | |
| IO | DIFFIO_RX41p | | B2 | VREF0B2 | | J28 | F31 | J36 | | | HIGH |
| IO | DIFFIO_RX41n | | B2 | VREF0B2 | | H28 | F32 | J37 | | | HIGH |
| IO | DIFFIO_TX41p | | B2 | VREF0B2 | G23 | H25 | J27 | L33 | | | HIGH |
| IO | DIFFIO_TX41n | | B2 | VREF0B2 | G24 | G25 | J28 | L32 | | | HIGH |
| IO | DIFFIO_RX40p | | B2 | VREF0B2 | | D29 | G29 | L37 | | | HIGH |
| IO | DIFFIO_RX40n | | B2 | VREF0B2 | | E29 | G30 | L36 | | | HIGH |
| IO | DIFFIO_TX40p | | B2 | VREF0B2 | H24 | K26 | H25 | M32 | | | HIGH |
| IO | DIFFIO_TX40n | | B2 | VREF0B2 | H23 | L26 | H26 | M33 | | | HIGH |
| IO | DIFFIO_RX39p | | B2 | VREF0B2 | | F29 | H30 | K38 | | | HIGH |
| IO | DIFFIO_RX39n | | B2 | VREF0B2 | | G29 | H29 | K39 | | | HIGH |
| IO | DIFFIO_TX39p | | B2 | VREF0B2 | H22 | J26 | J25 | N32 | | | HIGH |
| IO | DIFFIO_TX39n | | B2 | VREF0B2 | H21 | H26 | J26 | N33 | | | HIGH |
| IO | DIFFIO_RX38p | | B2 | VREF0B2 | D27 | H29 | G31 | M36 | | | HIGH |
| IO | DIFFIO_RX38n | | B2 | VREF0B2 | D28 | J29 | G32 | M37 | | | HIGH |
| IO | DIFFIO_TX38p | | B2 | VREF0B2 | J24 | G26 | K28 | K34 | | | HIGH |
| IO | DIFFIO_TX38n | | B2 | VREF0B2 | J23 | F26 | K27 | K35 | | | HIGH |
| IO | DIFFIO_RX37p | | B2 | VREF1B2 | E27 | D30 | H31 | L38 | | | HIGH |
| IO | DIFFIO_RX37n | | B2 | VREF1B2 | E28 | E30 | H32 | L39 | | | HIGH |
| IO | DIFFIO_TX37p | | B2 | VREF1B2 | K23 | F27 | K26 | L35 | | | HIGH |

**Table 5–1. Pin List for the Stratix EP1S40 Device (Part 3 of 71)**

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_TX37n | | B2 | VREF1B2 | K24 | G27 | K25 | L34 | | | HIGH |
| IO | DIFFIO_RX36p | | B2 | VREF1B2 | F25 | F30 | J29 | M38 | | | HIGH |
| IO | DIFFIO_RX36n | | B2 | VREF1B2 | F26 | G30 | J30 | M39 | | | HIGH |
| IO | DIFFIO_TX36p | | B2 | VREF1B2 | J21 | H27 | L27 | M34 | | | HIGH |
| IO | DIFFIO_TX36n | | B2 | VREF1B2 | J22 | J27 | L26 | M35 | | | HIGH |
| IO | DIFFIO_RX35p | | B2 | VREF1B2 | F27 | H30 | K30 | N36 | | | HIGH |
| IO | DIFFIO_RX35n | | B2 | VREF1B2 | F28 | J30 | K29 | N37 | | | HIGH |
| IO | DIFFIO_TX35p | | B2 | VREF1B2 | K21 | K27 | M26 | N34 | | | HIGH |
| IO | DIFFIO_TX35n | | B2 | VREF1B2 | K22 | L27 | M27 | N35 | | | HIGH |
| IO | DIFFIO_RX34p | | B2 | VREF1B2 | G26 | F31 | J32 | N38 | | | HIGH |
| IO | DIFFIO_RX34n | | B2 | VREF1B2 | G25 | G31 | J31 | P38 | | | HIGH |
| IO | DIFFIO_TX34p | | B2 | VREF1B2 | L22 | L24 | M24 | P32 | | | HIGH |
| IO | DIFFIO_TX34n | | B2 | VREF1B2 | L21 | M24 | M25 | P33 | | | HIGH |
| VREF1B2 | | | B2 | VREF1B2 | K20 | M22 | L25 | N29 | | | |
| IO | DIFFIO_RX33p | | B2 | VREF1B2 | G27 | H31 | K31 | P39 | | | HIGH |
| IO | DIFFIO_RX33n | | B2 | VREF1B2 | G28 | J31 | L32 | R38 | | | HIGH |
| IO | DIFFIO_TX33p | | B2 | VREF1B2 | L23 | L25 | N24 | P34 | | | HIGH |
| IO | DIFFIO_TX33n | | B2 | VREF1B2 | L24 | M25 | N23 | P35 | | | HIGH |
| IO | DIFFIO_RX32p/RUP2 | | B2 | VREF1B2 | H26 | K28 | M28 | P36 | | | HIGH |
| IO | DIFFIO_RX32n/RDN2 | | B2 | VREF1B2 | H25 | K29 | M29 | P37 | | | HIGH |
| IO | DIFFIO_TX32p | | B2 | VREF1B2 | L20 | P24 | N27 | R33 | | | HIGH |
| IO | DIFFIO_TX32n | | B2 | VREF1B2 | L19 | N24 | N28 | R32 | | | HIGH |

**Table 5–1. Pin List for the Stratix EP1S40 Device (Part 4 of 71)**

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_RX31p | | B2 | VREF1B2 | H27 | M28 | L30 | R36 | | | HIGH |
| IO | DIFFIO_RX31n | | B2 | VREF1B2 | H28 | L28 | L31 | R37 | | | HIGH |
| IO | DIFFIO_TX31p | | B2 | VREF1B2 | M22 | N25 | P23 | R34 | | | HIGH |
| IO | DIFFIO_TX31n | | B2 | VREF1B2 | M21 | P25 | P24 | R35 | | | HIGH |
| IO | DIFFIO_RX30p | | B2 | VREF1B2 | J25 | M29 | M31 | T36 | | | HIGH |
| IO | DIFFIO_RX30n | | B2 | VREF1B2 | J26 | L29 | M30 | T37 | | | HIGH |
| IO | DIFFIO_TX30p | | B2 | VREF1B2 | M24 | M26 | N25 | T33 | | | HIGH |
| IO | DIFFIO_TX30n | | B2 | VREF1B2 | M23 | N26 | N26 | T32 | | | HIGH |
| IO | DIFFIO_RX29p | | B2 | VREF2B2 | J27 | P28 | N29 | T39 | | | HIGH |
| IO | DIFFIO_RX29n | | B2 | VREF2B2 | J28 | N28 | N30 | T38 | | | HIGH |
| IO | DIFFIO_TX29p | | B2 | VREF2B2 | M20 | M27 | P28 | T30 | | | HIGH |
| IO | DIFFIO_TX29n | | B2 | VREF2B2 | M19 | N27 | P27 | T31 | | | HIGH |
| IO | DIFFIO_RX28p | | B2 | VREF2B2 | K26 | N29 | N31 | U36 | | | HIGH |
| IO | DIFFIO_RX28n | | B2 | VREF2B2 | K25 | P29 | N32 | U37 | | | HIGH |
| IO | DIFFIO_TX28p | | B2 | VREF2B2 | N26 | P27 | R28 | T34 | | | HIGH |
| IO | DIFFIO_TX28n | | B2 | VREF2B2 | N25 | R27 | R27 | T35 | | | HIGH |
| IO | DIFFIO_RX27p | | B2 | VREF2B2 | K27 | L30 | P29 | U38 | | | HIGH |
| IO | DIFFIO_RX27n | | B2 | VREF2B2 | K28 | K30 | P30 | U39 | | | HIGH |
| IO | DIFFIO_TX27p | | B2 | VREF2B2 | N24 | R26 | P25 | U35 | | | HIGH |
| IO | DIFFIO_TX27n | | B2 | VREF2B2 | N23 | P26 | P26 | U34 | | | HIGH |
| IO | DIFFIO_RX26p | | B2 | VREF2B2 | L25 | N30 | P31 | V36 | | | HIGH |
| IO | DIFFIO_RX26n | | B2 | VREF2B2 | L26 | M30 | P32 | V37 | | | HIGH |

**Table 5–1. Pin List for the Stratix EP1S40 Device (Part 5 of 71)**

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_TX26p | | B2 | VREF2B2 | N22 | N23 | R23 | U33 | | | HIGH |
| IO | DIFFIO_TX26n | | B2 | VREF2B2 | N21 | P23 | R24 | U32 | | | HIGH |
| VREF2B2 | | | B2 | VREF2B2 | P19 | N22 | R21 | P29 | | | |
| IO | DIFFIO_RX25p | | B2 | VREF2B2 | L27 | L31 | R32 | V38 | | | HIGH |
| IO | DIFFIO_RX25n | | B2 | VREF2B2 | L28 | K31 | R31 | V39 | | | HIGH |
| IO | DIFFIO_TX25p | | B2 | VREF2B2 | N20 | T25 | R25 | V35 | | | HIGH |
| IO | DIFFIO_TX25n | | B2 | VREF2B2 | N19 | R25 | R26 | V34 | | | HIGH |
| IO | DIFFIO_RX24p | | B2 | VREF2B2 | M25 | R30 | R30 | W39 | | | HIGH |
| IO | DIFFIO_RX24n | | B2 | VREF2B2 | M26 | P30 | R29 | W38 | | | HIGH |
| IO | DIFFIO_TX24p | | B2 | VREF2B2 | | | M23 | V32 | | | LOW |
| IO | DIFFIO_TX24n | | B2 | VREF2B2 | | | M22 | V31 | | | LOW |
| IO | DIFFIO_RX23p | | B2 | VREF2B2 | M27 | P31 | T32 | W37 | | | HIGH |
| IO | DIFFIO_RX23n | | B2 | VREF2B2 | N28 | R31 | T31 | W36 | | | HIGH |
| IO | DIFFIO_TX23p | | B2 | VREF2B2 | | | N22 | W31 | | | LOW |
| IO | DIFFIO_TX23n | | B2 | VREF2B2 | | | P22 | W32 | | | LOW |
| CLK0n | | | B2 | VREF2B2 | N27 | R28 | T30 | Y39 | | | |
| CLK0p | | | B2 | VREF2B2 | P27 | R29 | T29 | Y38 | | | |
| IO | CLK1n | | B2 | VREF2B2 | P26 | T30 | T28 | Y34 | | | |
| CLK1p | | | B2 | VREF2B2 | P25 | T31 | T27 | Y35 | | | |
| VCCINT | | | | | | | | | | | |
| VCCA_PLL1 | | | | | P23 | R24 | T25 | AA32 | | | |
| GND | | | | | | | | | | | |

*Table 5–1. Pin List for the Stratix EP1S40 Device (Part 6 of 71)*

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| GNDA_PLL1 | | | | | P24 | T24 | T26 | Y31 | | | |
| VCCG_PLL1 | | | | | P21 | R22 | R22 | Y28 | | | |
| GNDG_PLL1 | | | | | P22 | R23 | T22 | Y29 | | | |
| VCCINT | | | | | | | | | | | |
| VCCA_PLL2 | | | | | R23 | U24 | U25 | AA30 | | | |
| GND | | | | | | | | | | | |
| GNDA_PLL2 | | | | | R24 | V24 | U26 | AA31 | | | |
| VCCG_PLL2 | | | | | R21 | U23 | U24 | AA28 | | | |
| GNDG_PLL2 | | | | | R22 | V23 | T24 | AA29 | | | |
| CLK2p | | | B1 | VREF0B1 | R27 | T29 | U31 | Y37 | | | |
| CLK2n | | | B1 | VREF0B1 | T27 | T28 | U32 | Y36 | | | |
| CLK3p | | | B1 | VREF0B1 | R25 | U29 | U29 | AA35 | | | |
| IO | CLK3n | | B1 | VREF0B1 | R26 | U28 | U30 | AA34 | | | |
| IO | DIFFIO_RX22p | | B1 | VREF0B1 | T28 | U31 | U28 | AA39 | | | HIGH |
| IO | DIFFIO_RX22n | | B1 | VREF0B1 | U27 | V31 | U27 | AA38 | | | HIGH |
| IO | DIFFIO_TX22p | | B1 | VREF0B1 | | | U22 | Y33 | | | LOW |
| IO | DIFFIO_TX22n | | B1 | VREF0B1 | | | V22 | AA33 | | | LOW |
| IO | DIFFIO_RX21p | | B1 | VREF0B1 | U26 | AB31 | V32 | AA37 | | | HIGH |
| IO | DIFFIO_RX21n | | B1 | VREF0B1 | U25 | AA31 | V31 | AA36 | | | HIGH |
| IO | DIFFIO_TX21p | | B1 | VREF0B1 | | | W21 | AB33 | | | LOW |
| IO | DIFFIO_TX21n | | B1 | VREF0B1 | | | W22 | AB32 | | | LOW |
| IO | DIFFIO_RX20p | | B1 | VREF0B1 | V27 | V30 | V30 | AB38 | | | HIGH |

**Table 5–1. Pin List for the Stratix EP1S40 Device (Part 7 of 71)**

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed Note (1) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | | | |
| IO | DIFFIO_RX20n | | B1 | VREF0B1 | V28 | U30 | V29 | AB39 | | | HIGH |
| IO | DIFFIO_TX20p | | B1 | VREF0B1 | | | Y21 | AB31 | | | LOW |
| IO | DIFFIO_TX20n | | B1 | VREF0B1 | | | Y22 | AB30 | | | LOW |
| VREF0B1 | | | B1 | VREF0B1 | R19 | V22 | V21 | AE29 | | | |
| IO | DIFFIO_RX19p | | B1 | VREF0B1 | V26 | W30 | W32 | AB37 | | | HIGH |
| IO | DIFFIO_RX19n | | B1 | VREF0B1 | V25 | Y30 | W31 | AB36 | | | HIGH |
| IO | DIFFIO_TX19p | | B1 | VREF0B1 | T21 | V25 | V26 | AB34 | | | HIGH |
| IO | DIFFIO_TX19n | | B1 | VREF0B1 | T22 | U25 | V25 | AB35 | | | HIGH |
| IO | DIFFIO_RX18p | | B1 | VREF0B1 | W28 | AA30 | W30 | AC39 | | | HIGH |
| IO | DIFFIO_RX18n | | B1 | VREF0B1 | W27 | AB30 | W29 | AC38 | | | HIGH |
| IO | DIFFIO_TX18p | | B1 | VREF0B1 | T19 | U26 | V28 | AC32 | | | HIGH |
| IO | DIFFIO_TX18n | | B1 | VREF0B1 | T20 | T26 | V27 | AC33 | | | HIGH |
| IO | DIFFIO_RX17p | | B1 | VREF0B1 | W26 | V29 | Y32 | AC37 | | | HIGH |
| IO | DIFFIO_RX17n | | B1 | VREF0B1 | W25 | W29 | Y31 | AC36 | | | HIGH |
| IO | DIFFIO_TX17p | | B1 | VREF0B1 | T23 | T27 | W25 | AC34 | | | HIGH |
| IO | DIFFIO_TX17n | | B1 | VREF0B1 | T24 | U27 | W26 | AC35 | | | HIGH |
| IO | DIFFIO_RX16p | | B1 | VREF0B1 | Y28 | Y29 | Y30 | AD39 | | | HIGH |
| IO | DIFFIO_RX16n | | B1 | VREF0B1 | Y27 | AA29 | Y29 | AD38 | | | HIGH |
| IO | DIFFIO_TX16p | | B1 | VREF0B1 | T26 | V26 | W27 | AD34 | | | HIGH |
| IO | DIFFIO_TX16n | | B1 | VREF0B1 | T25 | W26 | W28 | AD35 | | | HIGH |
| IO | DIFFIO_RX15p | | B1 | VREF1B1 | Y26 | V28 | AA31 | AD37 | | | HIGH |
| IO | DIFFIO_RX15n | | B1 | VREF1B1 | Y25 | W28 | AA30 | AD36 | | | HIGH |

**Table 5–1. Pin List for the Stratix EP1S40 Device (Part 8 of 71)**

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | | | |
| IO | DIFFIO_TX15p | | B1 | VREF1B1 | U19 | W24 | V24 | AD33 | | | HIGH |
| IO | DIFFIO_TX15n | | B1 | VREF1B1 | U20 | Y24 | V23 | AD32 | | | HIGH |
| IO | DIFFIO_RX14p | | B1 | VREF1B1 | AA28 | Y28 | AB31 | AE37 | | | HIGH |
| IO | DIFFIO_RX14n | | B1 | VREF1B1 | AA27 | AA28 | AB30 | AE36 | | | HIGH |
| IO | DIFFIO_TX14p | | B1 | VREF1B1 | U24 | W25 | Y26 | AD31 | | | HIGH |
| IO | DIFFIO_TX14n | | B1 | VREF1B1 | U23 | Y25 | Y25 | AD30 | | | HIGH |
| IO | DIFFIO_RX13p/RUP1 | | B1 | VREF1B1 | AA25 | AB29 | AA28 | AF37 | | | HIGH |
| IO | DIFFIO_RX13n/RDN1 | | B1 | VREF1B1 | AA26 | AB28 | AA29 | AF36 | | | HIGH |
| IO | DIFFIO_TX13p | | B1 | VREF1B1 | U21 | Y26 | Y28 | AE35 | | | HIGH |
| IO | DIFFIO_TX13n | | B1 | VREF1B1 | U22 | AA26 | Y27 | AE34 | | | HIGH |
| IO | DIFFIO_RX12p | | B1 | VREF1B1 | AB28 | AC31 | AB32 | AE38 | | | HIGH |
| IO | DIFFIO_RX12n | | B1 | VREF1B1 | AB27 | AD31 | AC31 | AF39 | | | HIGH |
| IO | DIFFIO_TX12p | | B1 | VREF1B1 | V19 | W23 | W23 | AE33 | | | HIGH |
| IO | DIFFIO_TX12n | | B1 | VREF1B1 | V20 | Y23 | W24 | AE32 | | | HIGH |
| VREF1B1 | | | B1 | VREF1B1 | W20 | W22 | AA23 | AF29 | | | |
| IO | DIFFIO_RX11p | | B1 | VREF1B1 | AB26 | AE31 | AD32 | AF38 | | | HIGH |
| IO | DIFFIO_RX11n | | B1 | VREF1B1 | AB25 | AF31 | AD31 | AG38 | | | HIGH |
| IO | DIFFIO_TX11p | | B1 | VREF1B1 | V24 | V27 | Y23 | AF35 | | | HIGH |
| IO | DIFFIO_TX11n | | B1 | VREF1B1 | V23 | W27 | Y24 | AF34 | | | HIGH |
| IO | DIFFIO_RX10p | | B1 | VREF1B1 | AC28 | AC30 | AC29 | AG37 | | | HIGH |
| IO | DIFFIO_RX10n | | B1 | VREF1B1 | AC27 | AD30 | AC30 | AG36 | | | HIGH |
| IO | DIFFIO_TX10p | | B1 | VREF1B1 | V22 | Y27 | AA25 | AF33 | | | HIGH |

*Table 5–1. Pin List for the Stratix EP1S40 Device (Part 9 of 71)*

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_TX10n | | B1 | VREF1B1 | V21 | AA27 | AA24 | AF32 | | | HIGH |
| IO | DIFFIO_RX9p | | B1 | VREF1B1 | AD28 | AF30 | AD30 | AH39 | | | HIGH |
| IO | DIFFIO_RX9n | | B1 | VREF1B1 | AD27 | AE30 | AD29 | AH38 | | | HIGH |
| IO | DIFFIO_TX9p | | B1 | VREF1B1 | W23 | AB27 | AA27 | AG35 | | | HIGH |
| IO | DIFFIO_TX9n | | B1 | VREF1B1 | W24 | AC27 | AA26 | AG34 | | | HIGH |
| IO | DIFFIO_RX8p | | B1 | VREF1B1 | AE28 | AG30 | AE32 | AH37 | | | HIGH |
| IO | DIFFIO_RX8n | | B1 | VREF1B1 | AE27 | AH30 | AE31 | AH36 | | | HIGH |
| IO | DIFFIO_TX8p | | B1 | VREF1B1 | W21 | AE27 | AB27 | AG33 | | | HIGH |
| IO | DIFFIO_TX8n | | B1 | VREF1B1 | W22 | AD27 | AB26 | AG32 | | | HIGH |
| IO | DIFFIO_RX7p | | B1 | VREF1B1 | | AC29 | AE30 | AJ39 | | | HIGH |
| IO | DIFFIO_RX7n | | B1 | VREF1B1 | | AD29 | AE29 | AJ38 | | | HIGH |
| IO | DIFFIO_TX7p | | B1 | VREF2B1 | Y21 | AG27 | AC25 | AH34 | | | HIGH |
| IO | DIFFIO_TX7n | | B1 | VREF2B1 | Y22 | AF27 | AC26 | AH35 | | | HIGH |
| IO | DIFFIO_RX6p | | B1 | VREF2B1 | | AE29 | AF32 | AJ37 | | | HIGH |
| IO | DIFFIO_RX6n | | B1 | VREF2B1 | | AF29 | AF31 | AJ36 | | | HIGH |
| IO | DIFFIO_TX6p | | B1 | VREF2B1 | Y24 | AB26 | AC27 | AK35 | | | HIGH |
| IO | DIFFIO_TX6n | | B1 | VREF2B1 | Y23 | AC26 | AC28 | AK34 | | | HIGH |
| IO | DIFFIO_RX5p | | B1 | VREF2B1 | | AH29 | AF30 | AK38 | | | HIGH |
| IO | DIFFIO_RX5n | | B1 | VREF2B1 | | AG29 | AF29 | AK39 | | | HIGH |
| IO | DIFFIO_TX5p | | B1 | VREF2B1 | AA23 | AD26 | AD28 | AH33 | | | HIGH |
| IO | DIFFIO_TX5n | | B1 | VREF2B1 | AA24 | AE26 | AD27 | AH32 | | | HIGH |
| IO | DIFFIO_RX4p | | B1 | VREF2B1 | | AC28 | AG31 | AK37 | | | HIGH |

*Table 5–1. Pin List for the Stratix EP1S40 Device (Part 10 of 71)*

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **780-Pin FBGA** | **956-Pin BGA** | **1020-Pin FBGA** | **1508-Pin FBGA** | **DQS for x16** | **DQS for x32** | **DIFFIO Speed** *Note (1)* |
| IO | DIFFIO_RX4n | | B1 | VREF2B1 | | AD28 | AG32 | AK36 | | | HIGH |
| IO | DIFFIO_TX4p | | B1 | VREF2B1 | | AA25 | AD26 | AJ35 | | | HIGH |
| IO | DIFFIO_TX4n | | B1 | VREF2B1 | U18 | AB25 | AD25 | AJ34 | | | HIGH |
| VREF2B1 | | | B1 | VREF2B1 | AE26 | Y22 | AB25 | AG29 | | | |
| IO | DIFFIO_RX3p | | B1 | VREF2B1 | AF28 | AE28 | AG30 | AL37 | | | HIGH |
| IO | DIFFIO_RX3n | | B1 | VREF2B1 | AF27 | AF28 | AG29 | AL36 | | | HIGH |
| IO | DIFFIO_TX3p | | B1 | VREF2B1 | AB23 | AD25 | AE28 | AJ33 | | | HIGH |
| IO | DIFFIO_TX3n | | B1 | VREF2B1 | AB24 | AC25 | AE27 | AJ32 | | | HIGH |
| IO | DIFFIO_RX2p | | B1 | VREF2B1 | | | AG25 | AM39 | | | LOW |
| IO | DIFFIO_RX2n | | B1 | VREF2B1 | | | AG26 | AM38 | | | LOW |
| IO | DIFFIO_TX2p | | B1 | VREF2B1 | AA21 | AA24 | AE25 | AK32 | | | HIGH |
| IO | DIFFIO_TX2n | | B1 | VREF2B1 | AA22 | AB24 | AE26 | AK33 | | | HIGH |
| IO | DIFFIO_RX1p | | B1 | VREF2B1 | | | AH32 | AN39 | | | LOW |
| IO | DIFFIO_RX1n | | B1 | VREF2B1 | | | AH31 | AN38 | | | LOW |
| IO | DIFFIO_TX1p | | B1 | VREF2B1 | AC25 | AD24 | AF27 | AL33 | | | HIGH |
| IO | DIFFIO_TX1n | | B1 | VREF2B1 | AC26 | AC24 | AF28 | AL32 | | | HIGH |
| IO | DIFFIO_RX0p | | B1 | VREF2B1 | | | AH29 | AP38 | | | LOW |
| IO | DIFFIO_RX0n | | B1 | VREF2B1 | | | AG28 | AP39 | | | LOW |
| IO | DIFFIO_TX0p | | B1 | VREF2B1 | AD25 | AE25 | AF26 | AH31 | | | HIGH |
| IO | DIFFIO_TX0n | | B1 | VREF2B1 | AD26 | AF25 | AF25 | AH30 | | | HIGH |
| FPLL8CLKn | | | B1 | VREF2B1 | | AG31 | AB29 | AL38 | | | |
| FPLL8CLKp | | | B1 | VREF2B1 | | AH31 | AB28 | AL39 | | | |

Table 5–1. Pin List for the Stratix EP1S40 Device (Part 11 of 71)

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | | | B1 | VREF2B1 | | | AA22 | AG30 | | | |
| IO | | | B1 | VREF2B1 | | | AB23 | AG31 | | | |
| VCCINT | | | | | | | | | | | |
| VCCA_PLL8 | | | | | | AB23 | AJ31 | AJ30 | | | |
| GND | | | | | | | | | | | |
| GNDA_PLL8 | | | | | | AA23 | AJ32 | AJ31 | | | |
| VCCG_PLL8 | | | | | | AD23 | AJ30 | AL31 | | | |
| GNDG_PLL8 | | | | | | AC23 | AH30 | AK31 | | | |
| IO | | | B8 | VREF0B8 | AC24 | AG28 | AD24 | AR35 | | | |
| IO | DQ9B7 | | B8 | VREF0B8 | AG26 | AK29 | AH28 | AV34 | DQ3B15 | DQ1B31 | |
| IO | | | B8 | VREF0B8 | AC23 | AJ30 | AE24 | AU36 | | | |
| IO | DQ9B6 | | B8 | VREF0B8 | AH26 | AJ29 | AK30 | AU34 | DQ3B14 | DQ1B30 | |
| IO | | | B8 | VREF0B8 | | | AF24 | AP33 | | | |
| IO | DQ9B5 | | B8 | VREF0B8 | AG25 | AJ28 | AJ28 | AU33 | DQ3B13 | DQ1B29 | |
| IO | | | B8 | VREF0B8 | | | | AN33 | | | |
| IO | DQ9B4 | | B8 | VREF0B8 | AH25 | AL28 | AJ29 | AW33 | DQ3B12 | DQ1B28 | |
| IO | | | B8 | VREF0B8 | AB22 | AH28 | AC24 | AR34 | | | |
| IO | DQ9B3 | | B8 | VREF0B8 | AF25 | AH27 | AK29 | AW34 | DQ3B11 | DQ1B27 | |
| IO | | | B8 | VREF0B8 | | | AG24 | AU35 | | | |
| IO | DQS9B | | B8 | VREF0B8 | AF24 | AK28 | AK28 | AV33 | | | |
| VREF0B8 | | | B8 | VREF0B8 | AD22 | AB22 | AH27 | AJ29 | | | |
| IO | | | B8 | VREF0B8 | | AF26 | AB24 | AT35 | | | |

*Table 5–1. Pin List for the Stratix EP1S40 Device (Part 12 of 71)*

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | | | |
| IO | DQ9B2 | | B8 | VREF0B8 | AG24 | AL27 | AL30 | AV32 | DQ3B10 | DQ1B26 | |
| IO | | | B8 | VREF0B8 | AE25 | AE24 | AC23 | AV36 | | | |
| IO | DQ9B1 | | B8 | VREF0B8 | AE24 | AJ27 | AL29 | AU32 | DQ3B9 | DQ1B25 | |
| IO | | | B8 | VREF0B8 | | | AG23 | AR33 | | | |
| IO | DQ9B0 | | B8 | VREF0B8 | AH24 | AK27 | AM29 | AW32 | DQ3B8 | DQ1B24 | |
| IO | | | B8 | VREF0B8 | AD24 | | | AN32 | | | |
| IO | | | B8 | VREF0B8 | | AC22 | AD23 | AT34 | | | |
| IO | DQ8B7 | | B8 | VREF0B8 | AG23 | AH26 | AH26 | AU31 | DQ3B7 | DQ1B23 | |
| IO | | | B8 | VREF0B8 | | | AB22 | AN31 | | | |
| IO | DQ8B6 | | B8 | VREF0B8 | AD23 | AG26 | AJ27 | AV31 | DQ3B6 | DQ1B22 | |
| IO | | | B8 | VREF0B8 | | AD22 | AF23 | AV35 | | | |
| IO | DQ8B5 | | B8 | VREF0B8 | AF23 | AK26 | AL28 | AW31 | DQ3B5 | DQ1B21 | |
| IO | | | B8 | VREF0B8 | AB21 | | AC22 | AP32 | | | |
| IO | DQ8B4 | | B8 | VREF0B8 | AH23 | AL26 | AK27 | AW30 | DQ3B4 | DQ1B20 | |
| IO | | | B8 | VREF0B8 | | | | AW36 | | | |
| IO | DQ8B3 | | B8 | VREF0B8 | AE22 | AH25 | AJ26 | AU30 | DQ3B3 | DQ1B19 | |
| IO | | | B8 | VREF0B8 | | AC21 | AE23 | AT33 | | | |
| IO | DQS8B | | B8 | VREF1B8 | AE23 | AJ26 | AL27 | AV30 | DQS3B | | |
| IO | DQ8B0 | | B8 | VREF1B8 | AG22 | AL25 | AK26 | AW29 | DQ3B0 | DQ1B16 | |
| IO | DQ8B2 | | B8 | VREF1B8 | AF22 | AK25 | AM27 | AU29 | DQ3B2 | DQ1B18 | |
| IO | | | B8 | VREF1B8 | AB20 | AE22 | AE22 | AT32 | | | |
| IO | DQ8B1 | | B8 | VREF1B8 | AH22 | AJ25 | AM28 | AV29 | DQ3B1 | DQ1B17 | |

Table 5–1. Pin List for the Stratix EP1S40 Device (Part 13 of 71)

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed Note (1) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **780-Pin FBGA** | **956-Pin BGA** | **1020-Pin FBGA** | **1508-Pin FBGA** | | | |
| IO | | | B8 | VREF1B8 | | | AF22 | AT31 | | | |
| IO | | | B8 | VREF1B8 | | AA21 | AD22 | AR32 | | | |
| IO | | | B8 | VREF1B8 | | | | AN30 | | | |
| IO | | | B8 | VREF1B8 | Y20 | AD21 | AA21 | AW35 | | | |
| IO | DQ7B7 | | B8 | VREF1B8 | AD21 | AG24 | AH24 | AR28 | DQ2B15 | DQ1B15 | |
| IO | | | B8 | VREF1B8 | | | AG22 | AN29 | | | |
| IO | DQ7B6 | | B8 | VREF1B8 | AE21 | AH23 | AJ24 | AT28 | DQ2B14 | DQ1B14 | |
| VREF1B8 | | | B8 | VREF1B8 | AD20 | AB21 | AH25 | AJ28 | | | |
| IO | | | B8 | VREF1B8 | | | | AP31 | | | |
| IO | DQ7B5 | | B8 | VREF1B8 | AG21 | AK24 | AJ25 | AU28 | DQ2B13 | DQ1B13 | |
| IO | | | B8 | VREF1B8 | AC22 | AC20 | AB21 | AP30 | | | |
| IO | DQ7B4 | | B8 | VREF1B8 | AF21 | AH24 | AK25 | AV28 | DQ2B12 | DQ1B12 | |
| IO | | | B8 | VREF1B8 | | | AG21 | AT30 | | | |
| IO | DQ7B3 | | B8 | VREF1B8 | AE20 | AJ23 | AL25 | AR27 | DQ2B11 | DQ1B11 | |
| IO | | | B8 | VREF1B8 | | AA19 | AC21 | AR31 | | | |
| IO | DQS7B | | B8 | VREF1B8 | AG20 | AJ24 | AL26 | AT27 | | DQS1B | |
| IO | | | B8 | VREF1B8 | | | | AP29 | | | |
| IO | DQ7B2 | | B8 | VREF1B8 | AF20 | AL24 | AK24 | AW28 | DQ2B10 | DQ1B10 | |
| IO | | | B8 | VREF1B8 | | | AD21 | AR29 | | | |
| IO | DQ7B1 | | B8 | VREF1B8 | AH21 | AK23 | AM25 | AU27 | DQ2B9 | DQ1B9 | |
| IO | | | B8 | VREF1B8 | | | | AR30 | | | |
| IO | DQ7B0 | | B8 | VREF1B8 | AH20 | AL23 | AM26 | AV27 | DQ2B8 | DQ1B8 | |

**Table 5–1. Pin List for the Stratix EP1S40 Device (Part 14 of 71)**

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | | | |
| IO | | | B8 | VREF1B8 | | | | AN28 | | | |
| IO | | | B8 | VREF1B8 | AC20 | AD20 | AG20 | AM27 | | | |
| IO | FCLK3 | | B8 | VREF1B8 | AC21 | AF23 | AE21 | AT29 | | | |
| IO | FCLK2 | | B8 | VREF1B8 | AC19 | AF22 | AF21 | AN26 | | | |
| IO | DQ6B7 | | B8 | VREF2B8 | AE19 | AG22 | AJ23 | AR26 | DQ2B7 | DQ1B7 | |
| IO | DQ6B6 | | B8 | VREF2B8 | AD19 | AH22 | AL24 | AT26 | DQ2B6 | DQ1B6 | |
| IO | DQ6B5 | | B8 | VREF2B8 | AF19 | AK22 | AH22 | AU26 | DQ2B5 | DQ1B5 | |
| IO | | | B8 | VREF2B8 | | AE20 | AB20 | AP28 | | | |
| IO | DQ6B4 | | B8 | VREF2B8 | AG19 | AG21 | AM24 | AV26 | DQ2B4 | DQ1B4 | |
| IO | | PGM2 | B8 | VREF2B8 | AB19 | AF24 | AA20 | AL25 | | | |
| IO | DQ6B3 | | B8 | VREF2B8 | AH19 | AH21 | AK23 | AW26 | DQ2B3 | DQ1B3 | |
| IO | | | B8 | VREF2B8 | | | AD20 | AN27 | | | |
| IO | DQS6B | | B8 | VREF2B8 | AF18 | AJ22 | AJ22 | AU25 | DQS2B | | |
| IO | | | B8 | VREF2B8 | | | AE20 | AM26 | | | |
| IO | DQ6B2 | | B8 | VREF2B8 | AD18 | AL22 | AL23 | AT25 | DQ2B2 | DQ1B2 | |
| IO | | | B8 | VREF2B8 | AA20 | AE21 | AF20 | AN25 | | | |
| VREF2B8 | | | B8 | VREF2B8 | AH18 | AB20 | AH23 | AJ27 | | | |
| IO | RDN8 | | B8 | VREF2B8 | Y19 | AE23 | AC20 | AH24 | | | |
| IO | RUP8 | | B8 | VREF2B8 | W19 | AG25 | AH19 | AF23 | | | |
| IO | DQ6B0 | | B8 | VREF2B8 | AG18 | AK21 | AL22 | AV25 | DQ2B0 | DQ1B0 | |
| IO | | | B8 | VREF2B8 | | | | AP27 | | | |
| IO | DQ6B1 | | B8 | VREF2B8 | AE18 | AJ21 | AK22 | AR25 | DQ2B1 | DQ1B1 | |

*Table 5–1. Pin List for the Stratix EP1S40 Device (Part 15 of 71)*

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | | | |
| IO | DQ5B7 | | B8 | VREF2B8 | AF17 | AG20 | AM22 | AT24 | | | |
| IO | | | B8 | VREF2B8 | | | | AP26 | | | |
| IO | DQ5B6 | | B8 | VREF2B8 | AG17 | AH20 | AJ21 | AU24 | | | |
| IO | | | B8 | VREF2B8 | | | AB19 | AM25 | | | |
| IO | DQ5B5 | | B8 | VREF2B8 | AE17 | AK20 | AK21 | AV24 | | | |
| IO | | | B8 | VREF2B8 | | AC19 | AK18 | AP25 | | | |
| IO | DQ5B4 | | B8 | VREF2B8 | AD17 | AL20 | AL21 | AW24 | | | |
| IO | | RDYnBSY | B8 | VREF2B8 | AA19 | AG23 | AA19 | AH23 | | | |
| IO | DQ5B3 | | B8 | VREF2B8 | AG16 | AG19 | AH20 | AW23 | | | |
| IO | | | B8 | VREF2B8 | AB18 | AD19 | AD19 | AM24 | | | |
| IO | DQS5B | | B8 | VREF2B8 | AH16 | AJ20 | AJ20 | AU23 | | | |
| IO | | | B8 | VREF2B8 | | AE19 | AJ18 | AN24 | | | |
| IO | DQ5B2 | | B8 | VREF2B8 | AD16 | AH19 | AK20 | AR23 | | | |
| IO | | nCS | B8 | VREF3B8 | Y18 | AF20 | AC19 | AL23 | | | |
| IO | DQ5B1 | | B8 | VREF3B8 | AF16 | AJ19 | AL20 | AV23 | | | |
| IO | | | B8 | VREF3B8 | | | | AP24 | | | |
| IO | DQ5B0 | | B8 | VREF3B8 | AE16 | AK19 | AM20 | AT23 | | | |
| IO | | | B8 | VREF3B8 | W18 | AE18 | AH18 | AR24 | | | |
| IO | | | B8 | VREF3B8 | V18 | | | AM23 | | | |
| IO | | | B8 | VREF3B8 | | | | AN23 | | | |
| IO | | | B8 | VREF3B8 | | | | AN22 | | | |
| IO | | | B8 | VREF3B8 | | | | AP23 | | | |

**Table 5–1. Pin List for the Stratix EP1S40 Device (Part 16 of 71)**

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | | CS | B8 | VREF3B8 | AA18 | AF21 | AG19 | AJ23 | | | |
| IO | | | B8 | VREF3B8 | | | | AR22 | | | |
| IO | | | B8 | VREF3B8 | | | | AP22 | | | |
| VREF3B8 | | | B8 | VREF3B8 | | AB19 | AH21 | AJ26 | | | |
| IO | CLK5n | | B8 | VREF3B8 | Y17 | AH18 | AJ19 | AU22 | | | |
| CLK5p | | | B8 | VREF3B8 | AA17 | AJ18 | AK19 | AT22 | | | |
| IO | CLK4n | | B8 | VREF3B8 | AB17 | AK18 | AL19 | AW22 | | | |
| CLK4p | | | B8 | VREF3B8 | AC17 | AL18 | AM19 | AV22 | | | |
| PLL_ENA | | PLL_ENA | B8 | VREF3B8 | AC18 | AF19 | AF19 | AM22 | | | |
| MSEL0 | | MSEL0 | B8 | VREF3B8 | AC16 | AF18 | AG18 | AP21 | | | |
| MSEL1 | | MSEL1 | B8 | VREF3B8 | W17 | AG18 | AE18 | AG21 | | | |
| MSEL2 | | MSEL2 | B8 | VREF3B8 | AB15 | AG17 | AE19 | AM21 | | | |
| IO | PLL6_OUT3n | | B12 | VREF3B8 | Y16 | AL17 | AM18 | AV20 | | | |
| IO | PLL6_OUT3p | | B12 | VREF3B8 | W16 | AK17 | AL18 | AW20 | | | |
| IO | PLL6_OUT2n | | B12 | VREF3B8 | AG15 | AJ17 | AK17 | AW21 | | | |
| IO | PLL6_OUT2p | | B12 | VREF3B8 | AF15 | AH17 | AJ17 | AV21 | | | |
| IO | PLL6_FBn | | B11 | VREF3B8 | AA15 | AJ15 | AM17 | AU20 | | | |
| IO | PLL6_FBp | | B11 | VREF3B8 | AA14 | AH15 | AL17 | AT20 | | | |
| IO | PLL6_OUT1n | | B11 | VREF3B8 | W15 | AL15 | AK16 | AU21 | | | |
| IO | PLL6_OUT1p | | B11 | VREF3B8 | W14 | AK15 | AJ16 | AT21 | | | |
| IO | PLL6_OUT0n | | B11 | VREF3B8 | AE15 | AL16 | AM16 | AU19 | | | |
| IO | PLL6_OUT0p | | B11 | VREF3B8 | AD15 | AK16 | AL16 | AT19 | | | |

**Table 5–1. Pin List for the Stratix EP1S40 Device (Part 17 of 71)**

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| VCC_PLL6_OUTB | | | B12 | | AB16 | AC18 | AB17 | AH21 | | | |
| VCC_PLL6_OUTB | | | B12 | | | | | | | | |
| VCC_PLL6_OUTA | | | B11 | | AC14 | AD17 | AE17 | AJ21 | | | |
| VCC_PLL6_OUTA | | | B11 | | | | | | | | |
| VCCINT | | | | | | | | | | | |
| VCCA_PLL6 | | | | | AG14 | AB17 | AG17 | AK21 | | | |
| GND | | | | | | | | | | | |
| GNDA_PLL6 | | | | | AF14 | AC17 | AH17 | AL20 | | | |
| VCCG_PLL6 | | | | | AA13 | AD15 | AD16 | AJ20 | | | |
| GNDG_PLL6 | | | | | AB14 | AD16 | AB16 | AH20 | | | |
| VCCINT | | | | | | | | | | | |
| VCCA_PLL12 | | | | | | AC14 | AG16 | AK19 | | | |
| GND | | | | | | | | | | | |
| GNDA_PLL12 | | | | | | AD14 | AH16 | AL19 | | | |
| VCCG_PLL12 | | | | | | AC15 | AF16 | AJ19 | | | |
| GNDG_PLL12 | | | | | | AB15 | AE16 | AH19 | | | |
| CLK7p | | | B7 | VREF0B7 | W13 | AJ14 | AM15 | AW18 | | | |
| IO | CLK7n | | B7 | VREF0B7 | Y13 | AH14 | AL15 | AV18 | | | |
| CLK6p | | | B7 | VREF0B7 | AD14 | AL14 | AK15 | AW19 | | | |
| IO | CLK6n/PLL12_OUT | | B7 | VREF0B7 | AE14 | AK14 | AJ15 | AV19 | | | |
| nCE | | nCE | B7 | VREF0B7 | AB13 | AF17 | AF18 | AN20 | | | |
| nCEO | | nCEO | B7 | VREF0B7 | AC13 | AF16 | AH15 | AP20 | | | |

Table 5–1. Pin List for the Stratix EP1S40 Device (Part 18 of 71)

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | | | |
| IO | | | B7 | VREF0B7 | | | | AP19 | | | |
| IO | | | B7 | VREF0B7 | | | | AR19 | | | |
| IO | | PGM0 | B7 | VREF0B7 | W12 | AE17 | AD18 | AG20 | | | |
| nIO_PULLUP | | nIO_PULLUP | B7 | VREF0B7 | Y12 | AE16 | AF15 | AR20 | | | |
| VCCSEL | | VCCSEL | B7 | VREF0B7 | AA12 | AE15 | AJ14 | AM19 | | | |
| PORSEL | | PORSEL | B7 | VREF0B7 | AC12 | AG16 | AG15 | AN19 | | | |
| VREF0B7 | | | B7 | VREF0B7 | AD11 | AB14 | AH12 | AJ15 | | | |
| IO | | INIT_DONE | B7 | VREF0B7 | W11 | AF15 | AE15 | AL18 | | | |
| IO | | | B7 | VREF0B7 | | | AC18 | AN18 | | | |
| IO | DQ4B7 | | B7 | VREF0B7 | AD13 | AK13 | AL13 | AU17 | | | |
| IO | | | B7 | VREF0B7 | V11 | AA16 | AD15 | AP18 | | | |
| IO | DQ4B6 | | B7 | VREF0B7 | AE13 | AG13 | AM13 | AR17 | | | |
| IO | | nRS | B7 | VREF0B7 | AC11 | AE14 | AB18 | AL17 | | | |
| IO | DQ4B5 | | B7 | VREF0B7 | AF13 | AH13 | AH13 | AT17 | | | |
| IO | | | B7 | VREF0B7 | Y11 | AA15 | AC15 | AR18 | | | |
| IO | DQ4B4 | | B7 | VREF0B7 | AD12 | AJ13 | AJ13 | AV17 | | | |
| IO | | | B7 | VREF0B7 | | AH16 | AD14 | AT18 | | | |
| IO | DQ4B3 | | B7 | VREF0B7 | AG13 | AK12 | AK13 | AV16 | | | |
| IO | | RUnLU | B7 | VREF0B7 | W10 | AJ16 | AF14 | AK17 | | | |
| IO | DQS4B | | B7 | VREF1B7 | AH13 | AJ12 | AJ12 | AU16 | | | |
| IO | | | B7 | VREF1B7 | | | AA18 | AP16 | | | |
| IO | DQ4B2 | | B7 | VREF1B7 | AE12 | AL12 | AK12 | AW17 | | | |

Table 5–1. Pin List for the Stratix EP1S40 Device (Part 19 of 71)

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed Note (1) |
| IO | | | B7 | VREF1B7 | AB12 | AE13 | AE14 | AU18 | | | |
| IO | DQ4B1 | | B7 | VREF1B7 | AF12 | AG12 | AL12 | AT16 | | | |
| IO | | PGM1 | B7 | VREF1B7 | AA11 | AG15 | AG14 | AF16 | | | |
| IO | DQ4B0 | | B7 | VREF1B7 | AG12 | AH12 | AM11 | AW16 | | | |
| IO | DQ3B6 | | B7 | VREF1B7 | AH11 | AJ11 | AK11 | AR15 | DQ1B14 | DQ0B30 | |
| IO | | | B7 | VREF1B7 | | | AK14 | AR16 | | | |
| IO | DQ3B7 | | B7 | VREF1B7 | AG11 | AL10 | AL10 | AT15 | DQ1B15 | DQ0B31 | |
| IO | RDN7 | | B7 | VREF1B7 | AC10 | AG14 | AC14 | AP17 | | | |
| IO | RUP7 | | B7 | VREF1B7 | AB11 | AF13 | AF13 | AN16 | | | |
| IO | | | B7 | VREF1B7 | | AC13 | AB15 | AP13 | | | |
| IO | DQ3B5 | | B7 | VREF1B7 | AE11 | AK11 | AL11 | AV15 | DQ1B13 | DQ0B29 | |
| IO | DEV_CLRn | | B7 | VREF1B7 | AC9 | AF14 | AH14 | AN17 | | | |
| IO | DQ3B4 | | B7 | VREF1B7 | AF11 | AG11 | AK10 | AV14 | DQ1B12 | DQ0B28 | |
| IO | | | B7 | VREF1B7 | | AD13 | AL14 | AP15 | | | |
| IO | DQ3B3 | | B7 | VREF1B7 | AE10 | AH11 | AM9 | AW14 | DQ1B11 | DQ0B27 | |
| VREF1B7 | | | B7 | VREF1B7 | | AB13 | AH10 | AJ14 | | | |
| IO | | | B7 | VREF1B7 | Y10 | AA13 | AA15 | AR11 | | | |
| IO | DQS3B | | B7 | VREF1B7 | AG10 | AJ10 | AJ11 | AU15 | DQS1B | | |
| IO | | | B7 | VREF1B7 | AA10 | AE12 | AD13 | AN13 | | | |
| IO | DQ3B2 | | B7 | VREF1B7 | AH10 | AG10 | AL9 | AR14 | DQ1B10 | DQ0B26 | |
| IO | | | B7 | VREF1B7 | | | AG13 | AP14 | | | |
| IO | DQ3B1 | | B7 | VREF1B7 | AF10 | AH10 | AJ10 | AT14 | DQ1B9 | DQ0B25 | |

**Table 5–1. Pin List for the Stratix EP1S40 Device (Part 20 of 71)**

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | | | |
| IO | | | B7 | VREF1B7 | | | AA14 | AN12 | | | |
| IO | DQ3B0 | | B7 | VREF1B7 | AD10 | AK10 | AH11 | AU14 | DQ1B8 | DQ0B24 | |
| IO | | | B7 | VREF1B7 | Y9 | AD12 | AB14 | AP12 | | | |
| IO | | | B7 | VREF1B7 | | | | AT10 | | | |
| IO | FCLK5 | | B7 | VREF1B7 | AC8 | AF12 | AM14 | AN14 | | | |
| IO | FCLK4 | | B7 | VREF1B7 | AB10 | AF11 | AF12 | AT11 | | | |
| IO | DQ2B7 | | B7 | VREF2B7 | AG9 | AL8 | AL8 | AT13 | DQ1B7 | DQ0B23 | |
| IO | DQ2B6 | | B7 | VREF2B7 | AF9 | AK9 | AJ9 | AU13 | DQ1B6 | DQ0B22 | |
| IO | DQ2B5 | | B7 | VREF2B7 | AE9 | AL9 | AK9 | AV13 | DQ1B5 | DQ0B21 | |
| IO | | | B7 | VREF2B7 | | AC12 | AC13 | AN11 | | | |
| IO | DQ2B4 | | B7 | VREF2B7 | AH8 | AH8 | AM8 | AV12 | DQ1B4 | DQ0B20 | |
| IO | | | B7 | VREF2B7 | | AE11 | AE13 | AP11 | | | |
| IO | DQ2B3 | | B7 | VREF2B7 | AH9 | AK8 | AH9 | AR13 | DQ1B3 | DQ0B19 | |
| IO | | | B7 | VREF2B7 | | AA11 | AB13 | AW5 | | | |
| IO | DQS2B | | B7 | VREF2B7 | AE8 | AJ8 | AK8 | AU12 | | DQS0B | |
| IO | | | B7 | VREF2B7 | | AG9 | AD12 | AP10 | | | |
| IO | DQ2B2 | | B7 | VREF2B7 | AD8 | AG8 | AM7 | AR12 | DQ1B2 | DQ0B18 | |
| IO | | | B7 | VREF2B7 | AA9 | AD11 | AE12 | AT9 | | | |
| IO | DQ2B1 | | B7 | VREF2B7 | AF8 | AH9 | AJ8 | AT12 | DQ1B1 | DQ0B17 | |
| IO | | | B7 | VREF2B7 | | | AC12 | AP9 | | | |
| IO | DQ2B0 | | B7 | VREF2B7 | AG8 | AJ9 | AL7 | AW12 | DQ1B0 | DQ0B16 | |
| IO | | | B7 | VREF2B7 | | | | AT8 | | | |

*Table 5–1. Pin List for the Stratix EP1S40 Device (Part 21 of 71)*

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | | | B7 | VREF2B7 | AB9 | AF10 | AG12 | AR10 | | | |
| IO | | | B7 | VREF2B7 | | AE10 | AG11 | AR9 | | | |
| VREF2B7 | | | B7 | VREF2B7 | AD9 | AB12 | AH8 | AJ13 | | | |
| IO | | | B7 | VREF2B7 | | | AA13 | AT7 | | | |
| IO | DQ1B6 | | B7 | VREF2B7 | AG7 | AL7 | AM6 | AW11 | DQ0B14 | DQ0B14 | |
| IO | | | B7 | VREF2B7 | AB8 | AC11 | AD11 | AN10 | | | |
| IO | DQ1B5 | | B7 | VREF2B7 | AH7 | AH6 | AJ7 | AU10 | DQ0B13 | DQ0B13 | |
| IO | DQ1B7 | | B7 | VREF2B7 | AF6 | AK7 | AL6 | AV11 | DQ0B15 | DQ0B15 | |
| IO | DQ1B4 | | B7 | VREF2B7 | AF7 | AK6 | AM5 | AW10 | DQ0B12 | DQ0B12 | |
| IO | | | B7 | VREF2B7 | | AD10 | AB12 | AR7 | | | |
| IO | DQ1B3 | | B7 | VREF2B7 | AD6 | AL6 | AK7 | AU11 | DQ0B11 | DQ0B11 | |
| IO | | | B7 | VREF2B7 | | | AE11 | AW4 | | | |
| IO | DQS1B | | B7 | VREF2B7 | AE7 | AJ6 | AH7 | AV10 | DQS0B | | |
| IO | | | B7 | VREF2B7 | AD5 | AF9 | AF11 | AR8 | | | |
| IO | DQ1B2 | | B7 | VREF2B7 | AH6 | AH7 | AL5 | AW9 | DQ0B10 | DQ0B10 | |
| IO | | | B7 | VREF3B7 | | AC10 | AC11 | AU5 | | | |
| IO | DQ1B1 | | B7 | VREF3B7 | AG6 | AJ7 | AK6 | AV9 | DQ0B9 | DQ0B9 | |
| IO | | | B7 | VREF3B7 | | | AF10 | AP8 | | | |
| IO | DQ1B0 | | B7 | VREF3B7 | AE6 | AG6 | AJ6 | AU9 | DQ0B8 | DQ0B8 | |
| IO | | | B7 | VREF3B7 | AC7 | | | AV5 | | | |
| IO | | | B7 | VREF3B7 | | AE9 | AG10 | AN9 | | | |
| IO | DQ0B7 | | B7 | VREF3B7 | AF5 | AL4 | AL3 | AV8 | DQ0B7 | DQ0B7 | |

*Table 5–1. Pin List for the Stratix EP1S40 Device (Part 22 of 71)*

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **780-Pin FBGA** | **956-Pin BGA** | **1020-Pin FBGA** | **1508-Pin FBGA** | **DQS for x16** | **DQS for x32** | **DIFFIO Speed** *Note (1)* |
| IO | | | B7 | VREF3B7 | AE4 | | AA12 | AT5 | | | |
| IO | DQ0B6 | | B7 | VREF3B7 | AH5 | AL5 | AL4 | AW8 | DQ0B6 | DQ0B6 | |
| IO | | | B7 | VREF3B7 | AB7 | AE8 | AD10 | AN8 | | | |
| IO | DQ0B5 | | B7 | VREF3B7 | AF4 | AJ4 | AM4 | AW6 | DQ0B5 | DQ0B5 | |
| IO | | | B7 | VREF3B7 | | AF8 | AE10 | AT6 | | | |
| VREF3B7 | | | B7 | VREF3B7 | AD7 | AB11 | AH6 | AJ12 | | | |
| IO | DQ0B4 | | B7 | VREF3B7 | AG4 | AK3 | AJ4 | AU8 | DQ0B4 | DQ0B4 | |
| IO | | | B7 | VREF3B7 | | AG4 | AB11 | AN7 | | | |
| IO | DQ0B3 | | B7 | VREF3B7 | AG5 | AK5 | AJ5 | AW7 | DQ0B3 | DQ0B3 | |
| IO | | | B7 | VREF3B7 | | AF6 | AE9 | AR6 | | | |
| IO | DQS0B | | B7 | VREF3B7 | AH3 | AK4 | AK5 | AV7 | | | |
| IO | | | B7 | VREF3B7 | AC6 | AG7 | AG9 | AV4 | | | |
| IO | DQ0B2 | | B7 | VREF3B7 | AG3 | AH5 | AH5 | AU7 | DQ0B2 | DQ0B2 | |
| IO | | | B7 | VREF3B7 | | | AC9 | AR5 | | | |
| IO | DQ0B1 | | B7 | VREF3B7 | AE5 | AJ5 | AK3 | AV6 | DQ0B1 | DQ0B1 | |
| IO | | | B7 | VREF3B7 | AC5 | AJ2 | AD9 | AU4 | | | |
| IO | DQ0B0 | | B7 | VREF3B7 | AH4 | AJ3 | AK4 | AU6 | DQ0B0 | DQ0B0 | |
| IO | | | B7 | VREF3B7 | | AH4 | AF9 | AP7 | | | |
| GNDG_PLL9 | | | | | | AC9 | AH3 | AK9 | | | |
| VCCG_PLL9 | | | | | | AD9 | AJ3 | AL9 | | | |
| GNDA_PLL9 | | | | | | AA9 | AJ1 | AJ9 | | | |
| GND | | | | | | | | | | | |

*Table 5–1. Pin List for the Stratix EP1S40 Device (Part 23 of 71)*

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| VCCA_PLL9 | | | | | | AB9 | AJ2 | AJ10 | | | |
| VCCINT | | | | | | | | | | | |
| IO | | | B6 | VREF0B6 | | | AB9 | AG10 | | | |
| IO | | | B6 | VREF0B6 | | | AC10 | AG9 | | | |
| FPLL9CLKp | | | B6 | VREF0B6 | | AH1 | AB5 | AL1 | | | |
| FPLL9CLKn | | | B6 | VREF0B6 | | AG1 | AB4 | AL2 | | | |
| IO | DIFFIO_TX89n | | B6 | VREF0B6 | AC3 | AC8 | AF8 | AH10 | | | HIGH |
| IO | DIFFIO_TX89p | | B6 | VREF0B6 | AC4 | AD8 | AF7 | AH9 | | | HIGH |
| IO | DIFFIO_RX89n | | B6 | VREF0B6 | | | AG5 | AP1 | | | LOW |
| IO | DIFFIO_RX89p | | B6 | VREF0B6 | | | AH4 | AP2 | | | LOW |
| IO | DIFFIO_TX88n | | B6 | VREF0B6 | AD3 | AF7 | AF5 | AL8 | | | HIGH |
| IO | DIFFIO_TX88p | | B6 | VREF0B6 | AD4 | AE7 | AF6 | AL7 | | | HIGH |
| IO | DIFFIO_RX88n | | B6 | VREF0B6 | | | AH2 | AN2 | | | LOW |
| IO | DIFFIO_RX88p | | B6 | VREF0B6 | | | AH1 | AN1 | | | LOW |
| IO | DIFFIO_TX87n | | B6 | VREF0B6 | AA7 | AB8 | AE7 | AK7 | | | HIGH |
| IO | DIFFIO_TX87p | | B6 | VREF0B6 | AA8 | AA8 | AE8 | AK8 | | | HIGH |
| IO | DIFFIO_RX87n | | B6 | VREF0B6 | | | AG7 | AM2 | | | LOW |
| IO | DIFFIO_RX87p | | B6 | VREF0B6 | | | AG8 | AM1 | | | LOW |
| IO | DIFFIO_TX86n | | B6 | VREF0B6 | AB5 | AC7 | AD6 | AJ7 | | | HIGH |
| IO | DIFFIO_TX86p | | B6 | VREF0B6 | AB6 | AD7 | AD5 | AJ8 | | | HIGH |
| IO | DIFFIO_RX86n | | B6 | VREF0B6 | AF2 | AF4 | AG4 | AL4 | | | HIGH |
| IO | DIFFIO_RX86p | | B6 | VREF0B6 | AF1 | AE4 | AG3 | AL3 | | | HIGH |

*Table 5–1. Pin List for the Stratix EP1S40 Device (Part 24 of 71)*

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| VREF0B6 | | | B6 | VREF0B6 | AE3 | AA10 | AG6 | AH11 | | | |
| IO | DIFFIO_TX85n | | B6 | VREF0B6 | U12 | AB7 | AE6 | AH8 | | | HIGH |
| IO | DIFFIO_TX85p | | B6 | VREF0B6 | | AA7 | AE5 | AH7 | | | HIGH |
| IO | DIFFIO_RX85n | | B6 | VREF0B6 | | AD4 | AG1 | AK4 | | | HIGH |
| IO | DIFFIO_RX85p | | B6 | VREF0B6 | | AC4 | AG2 | AK3 | | | HIGH |
| IO | DIFFIO_TX84n | | B6 | VREF0B6 | AA5 | AE6 | AD8 | AG8 | | | HIGH |
| IO | DIFFIO_TX84p | | B6 | VREF0B6 | AA6 | AD6 | AD7 | AG7 | | | HIGH |
| IO | DIFFIO_RX84n | | B6 | VREF0B6 | | AG3 | AF4 | AK1 | | | HIGH |
| IO | DIFFIO_RX84p | | B6 | VREF0B6 | | AH3 | AF3 | AK2 | | | HIGH |
| IO | DIFFIO_TX83n | | B6 | VREF0B6 | Y6 | AC6 | AC5 | AK6 | | | HIGH |
| IO | DIFFIO_TX83p | | B6 | VREF0B6 | Y5 | AB6 | AC6 | AK5 | | | HIGH |
| IO | DIFFIO_RX83n | | B6 | VREF0B6 | | AF3 | AF2 | AJ4 | | | HIGH |
| IO | DIFFIO_RX83p | | B6 | VREF0B6 | | AE3 | AF1 | AJ3 | | | HIGH |
| IO | DIFFIO_TX82n | | B6 | VREF0B6 | Y7 | AF5 | AC7 | AJ5 | | | HIGH |
| IO | DIFFIO_TX82p | | B6 | VREF0B6 | Y8 | AG5 | AC8 | AJ6 | | | HIGH |
| IO | DIFFIO_RX82n | | B6 | VREF1B6 | | AD3 | AE4 | AJ2 | | | HIGH |
| IO | DIFFIO_RX82p | | B6 | VREF1B6 | | AC3 | AE3 | AJ1 | | | HIGH |
| IO | DIFFIO_TX81n | | B6 | VREF1B6 | W7 | AD5 | AB7 | AH5 | | | HIGH |
| IO | DIFFIO_TX81p | | B6 | VREF1B6 | W8 | AE5 | AB6 | AH6 | | | HIGH |
| IO | DIFFIO_RX81n | | B6 | VREF1B6 | AE2 | AH2 | AE2 | AH4 | | | HIGH |
| IO | DIFFIO_RX81p | | B6 | VREF1B6 | AE1 | AG2 | AE1 | AH3 | | | HIGH |
| IO | DIFFIO_TX80n | | B6 | VREF1B6 | W5 | AC5 | AA6 | AG6 | | | HIGH |

**Table 5–1. Pin List for the Stratix EP1S40 Device (Part 25 of 71)**

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_TX80p | | B6 | VREF1B6 | W6 | AB5 | AA7 | AG5 | | | HIGH |
| IO | DIFFIO_RX80n | | B6 | VREF1B6 | AD2 | AE2 | AC3 | AH1 | | | HIGH |
| IO | DIFFIO_RX80p | | B6 | VREF1B6 | AD1 | AF2 | AC4 | AH2 | | | HIGH |
| IO | DIFFIO_TX79n | | B6 | VREF1B6 | V8 | AA6 | AA9 | AF8 | | | HIGH |
| IO | DIFFIO_TX79p | | B6 | VREF1B6 | V7 | Y6 | AA8 | AF7 | | | HIGH |
| IO | DIFFIO_RX79n | | B6 | VREF1B6 | AC2 | AD2 | AD3 | AG4 | | | HIGH |
| IO | DIFFIO_RX79p | | B6 | VREF1B6 | AC1 | AC2 | AD4 | AG3 | | | HIGH |
| IO | DIFFIO_TX78n | | B6 | VREF1B6 | V6 | Y9 | Y5 | AF6 | | | HIGH |
| IO | DIFFIO_TX78p | | B6 | VREF1B6 | V5 | W9 | Y6 | AF5 | | | HIGH |
| IO | DIFFIO_RX78n | | B6 | VREF1B6 | AB4 | AF1 | AD2 | AG2 | | | HIGH |
| IO | DIFFIO_RX78p | | B6 | VREF1B6 | AB3 | AE1 | AD1 | AF2 | | | HIGH |
| VREF1B6 | | | B6 | VREF1B6 | W9 | Y10 | AB8 | AG11 | | | |
| IO | DIFFIO_TX77n | | B6 | VREF1B6 | V9 | Y8 | Y7 | AE8 | | | HIGH |
| IO | DIFFIO_TX77p | | B6 | VREF1B6 | V10 | W8 | Y8 | AE7 | | | HIGH |
| IO | DIFFIO_RX77n | | B6 | VREF1B6 | AB2 | AD1 | AC2 | AF1 | | | HIGH |
| IO | DIFFIO_RX77p | | B6 | VREF1B6 | AB1 | AC1 | AB1 | AE2 | | | HIGH |
| IO | DIFFIO_TX76n | | B6 | VREF1B6 | U7 | AA5 | W5 | AE6 | | | HIGH |
| IO | DIFFIO_TX76p | | B6 | VREF1B6 | U8 | Y5 | W6 | AE5 | | | HIGH |
| IO | DIFFIO_RX76n/RDN6 | | B6 | VREF1B6 | AA3 | AB4 | AA4 | AF4 | | | HIGH |
| IO | DIFFIO_RX76p/RUP6 | | B6 | VREF1B6 | AA4 | AB3 | AA5 | AF3 | | | HIGH |
| IO | DIFFIO_TX75n | | B6 | VREF1B6 | U6 | Y7 | Y10 | AD10 | | | HIGH |
| IO | DIFFIO_TX75p | | B6 | VREF1B6 | U5 | W7 | Y9 | AD9 | | | HIGH |

**Table 5–1. Pin List for the Stratix EP1S40 Device (Part 26 of 71)**

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | | | |
| IO | DIFFIO_RX75n | | B6 | VREF1B6 | AA2 | Y4 | AB3 | AE4 | | | HIGH |
| IO | DIFFIO_RX75p | | B6 | VREF1B6 | AA1 | AA4 | AB2 | AE3 | | | HIGH |
| IO | DIFFIO_TX74n | | B6 | VREF1B6 | U9 | U7 | W10 | AD8 | | | HIGH |
| IO | DIFFIO_TX74p | | B6 | VREF1B6 | U10 | V7 | W9 | AD7 | | | HIGH |
| IO | DIFFIO_RX74n | | B6 | VREF1B6 | Y4 | W4 | AA3 | AD4 | | | HIGH |
| IO | DIFFIO_RX74p | | B6 | VREF1B6 | Y3 | V4 | AA2 | AD3 | | | HIGH |
| IO | DIFFIO_TX73n | | B6 | VREF2B6 | T6 | W6 | V9 | AD5 | | | HIGH |
| IO | DIFFIO_TX73p | | B6 | VREF2B6 | T5 | V6 | V10 | AD6 | | | HIGH |
| IO | DIFFIO_RX73n | | B6 | VREF2B6 | Y2 | AA3 | Y4 | AD2 | | | HIGH |
| IO | DIFFIO_RX73p | | B6 | VREF2B6 | Y1 | Y3 | Y3 | AD1 | | | HIGH |
| IO | DIFFIO_TX72n | | B6 | VREF2B6 | T10 | U6 | V5 | AC5 | | | HIGH |
| IO | DIFFIO_TX72p | | B6 | VREF2B6 | T9 | T6 | V6 | AC6 | | | HIGH |
| IO | DIFFIO_RX72n | | B6 | VREF2B6 | W4 | W3 | Y2 | AC4 | | | HIGH |
| IO | DIFFIO_RX72p | | B6 | VREF2B6 | W3 | V3 | Y1 | AC3 | | | HIGH |
| IO | DIFFIO_TX71n | | B6 | VREF2B6 | T7 | W5 | V8 | AC7 | | | HIGH |
| IO | DIFFIO_TX71p | | B6 | VREF2B6 | T8 | V5 | V7 | AC8 | | | HIGH |
| IO | DIFFIO_RX71n | | B6 | VREF2B6 | W2 | AB2 | W4 | AC2 | | | HIGH |
| IO | DIFFIO_RX71p | | B6 | VREF2B6 | W1 | AA2 | W3 | AC1 | | | HIGH |
| IO | DIFFIO_TX70n | | B6 | VREF2B6 | T4 | T5 | W8 | AB5 | | | HIGH |
| IO | DIFFIO_TX70p | | B6 | VREF2B6 | T3 | U5 | W7 | AB6 | | | HIGH |
| IO | DIFFIO_RX70n | | B6 | VREF2B6 | V4 | Y2 | W2 | AB4 | | | HIGH |
| IO | DIFFIO_RX70p | | B6 | VREF2B6 | V3 | W2 | W1 | AB3 | | | HIGH |

**Table 5–1. Pin List for the Stratix EP1S40 Device (Part 27 of 71)**

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| VREF2B6 | | | B6 | VREF2B6 | R10 | W10 | AA10 | AF11 | | | |
| IO | DIFFIO_TX69n | | B6 | VREF2B6 | | | AB10 | AB8 | | | LOW |
| IO | DIFFIO_TX69p | | B6 | VREF2B6 | | | AA11 | AB9 | | | LOW |
| IO | DIFFIO_RX69n | | B6 | VREF2B6 | V1 | AA1 | V4 | AB1 | | | HIGH |
| IO | DIFFIO_RX69p | | B6 | VREF2B6 | V2 | AB1 | V3 | AB2 | | | HIGH |
| IO | DIFFIO_TX68n | | B6 | VREF2B6 | | | Y11 | AA11 | | | LOW |
| IO | DIFFIO_TX68p | | B6 | VREF2B6 | | | Y12 | AA10 | | | LOW |
| IO | DIFFIO_RX68n | | B6 | VREF2B6 | U4 | V2 | V2 | AA4 | | | HIGH |
| IO | DIFFIO_RX68p | | B6 | VREF2B6 | U3 | U2 | V1 | AA3 | | | HIGH |
| IO | DIFFIO_TX67n | | B6 | VREF2B6 | | | W11 | AA9 | | | LOW |
| IO | DIFFIO_TX67p | | B6 | VREF2B6 | | | W12 | AA8 | | | LOW |
| IO | DIFFIO_RX67n | | B6 | VREF2B6 | U2 | V1 | U5 | AA2 | | | HIGH |
| IO | DIFFIO_RX67p | | B6 | VREF2B6 | T1 | U1 | U6 | AA1 | | | HIGH |
| IO | CLK8n | | B6 | VREF2B6 | R3 | U4 | U3 | Y5 | | | |
| CLK8p | | | B6 | VREF2B6 | R4 | U3 | U4 | Y6 | | | |
| CLK9n | | | B6 | VREF2B6 | T2 | T3 | U1 | Y2 | | | |
| CLK9p | | | B6 | VREF2B6 | R2 | T4 | U2 | Y1 | | | |
| GNDG_PLL3 | | | | | R7 | V9 | U11 | Y11 | | | |
| VCCG_PLL3 | | | | | R8 | U9 | V11 | Y12 | | | |
| GNDA_PLL3 | | | | | R5 | V8 | U7 | Y9 | | | |
| GND | | | | | | | | | | | |
| VCCA_PLL3 | | | | | R6 | U8 | U8 | W8 | | | |

**Table 5–1. Pin List for the Stratix EP1S40 Device (Part 28 of 71)**

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | | | |
| VCCINT | | | | | | | | | | | |
| GNDG_PLL4 | | | | | P7 | R9 | U9 | W11 | | | |
| VCCG_PLL4 | | | | | P8 | R10 | T9 | W12 | | | |
| GNDA_PLL4 | | | | | P5 | R8 | T7 | W9 | | | |
| GND | | | | | | | | | | | |
| VCCA_PLL4 | | | | | P6 | T8 | T8 | W10 | | | |
| VCCINT | | | | | | | | | | | |
| CLK10p | | | B5 | VREF0B5 | P4 | T1 | T6 | Y3 | | | |
| IO | CLK10n | | B5 | VREF0B5 | P3 | T2 | T5 | Y4 | | | |
| CLK11p | | | B5 | VREF0B5 | P2 | R3 | T4 | W5 | | | |
| CLK11n | | | B5 | VREF0B5 | N2 | R4 | T3 | W6 | | | |
| IO | DIFFIO_TX66n | | B5 | VREF0B5 | | | T11 | Y7 | | | LOW |
| IO | DIFFIO_TX66p | | B5 | VREF0B5 | | | R11 | W7 | | | LOW |
| IO | DIFFIO_RX66n | | B5 | VREF0B5 | M2 | R1 | T2 | W1 | | | HIGH |
| IO | DIFFIO_RX66p | | B5 | VREF0B5 | N1 | P1 | T1 | W2 | | | HIGH |
| IO | DIFFIO_TX65n | | B5 | VREF0B5 | | | P11 | V7 | | | LOW |
| IO | DIFFIO_TX65p | | B5 | VREF0B5 | | | N11 | V8 | | | LOW |
| IO | DIFFIO_RX65n | | B5 | VREF0B5 | M3 | P2 | R1 | W4 | | | HIGH |
| IO | DIFFIO_RX65p | | B5 | VREF0B5 | M4 | R2 | R2 | W3 | | | HIGH |
| IO | DIFFIO_TX64n | | B5 | VREF0B5 | N10 | R7 | R7 | V6 | | | HIGH |
| IO | DIFFIO_TX64p | | B5 | VREF0B5 | N9 | T7 | R8 | V5 | | | HIGH |
| IO | DIFFIO_RX64n | | B5 | VREF0B5 | L1 | K1 | R3 | V1 | | | HIGH |

**Table 5–1. Pin List for the Stratix EP1S40 Device (Part 29 of 71)**

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_RX64p | | B5 | VREF0B5 | L2 | L1 | R4 | V2 | | | HIGH |
| VREF0B5 | | | B5 | VREF0B5 | P10 | P10 | R12 | R11 | | | |
| IO | DIFFIO_TX63n | | B5 | VREF0B5 | N5 | P8 | P7 | U8 | | | HIGH |
| IO | DIFFIO_TX63p | | B5 | VREF0B5 | N6 | N8 | P8 | U7 | | | HIGH |
| IO | DIFFIO_RX63n | | B5 | VREF0B5 | L3 | N2 | P1 | V3 | | | HIGH |
| IO | DIFFIO_RX63p | | B5 | VREF0B5 | L4 | M2 | P2 | V4 | | | HIGH |
| IO | DIFFIO_TX62n | | B5 | VREF0B5 | N7 | R6 | R5 | U6 | | | HIGH |
| IO | DIFFIO_TX62p | | B5 | VREF0B5 | N8 | P6 | R6 | U5 | | | HIGH |
| IO | DIFFIO_RX62n | | B5 | VREF0B5 | K1 | L2 | P3 | U1 | | | HIGH |
| IO | DIFFIO_RX62p | | B5 | VREF0B5 | K2 | K2 | P4 | U2 | | | HIGH |
| IO | DIFFIO_TX61n | | B5 | VREF0B5 | N4 | P9 | R10 | T5 | | | HIGH |
| IO | DIFFIO_TX61p | | B5 | VREF0B5 | N3 | N9 | R9 | T6 | | | HIGH |
| IO | DIFFIO_RX61n | | B5 | VREF0B5 | K4 | P3 | N1 | U3 | | | HIGH |
| IO | DIFFIO_RX61p | | B5 | VREF0B5 | K3 | N3 | N2 | U4 | | | HIGH |
| IO | DIFFIO_TX60n | | B5 | VREF0B5 | M10 | P7 | P6 | T7 | | | HIGH |
| IO | DIFFIO_TX60p | | B5 | VREF0B5 | M9 | N7 | P5 | T8 | | | HIGH |
| IO | DIFFIO_RX60n | | B5 | VREF0B5 | J1 | L3 | N3 | T2 | | | HIGH |
| IO | DIFFIO_RX60p | | B5 | VREF0B5 | J2 | M3 | N4 | T1 | | | HIGH |
| IO | DIFFIO_TX59n | | B5 | VREF1B5 | M6 | N6 | N7 | T9 | | | HIGH |
| IO | DIFFIO_TX59p | | B5 | VREF1B5 | M5 | M6 | N8 | T10 | | | HIGH |
| IO | DIFFIO_RX59n | | B5 | VREF1B5 | J3 | P4 | M2 | T3 | | | HIGH |
| IO | DIFFIO_RX59p | | B5 | VREF1B5 | J4 | N4 | M3 | T4 | | | HIGH |

*Table 5–1. Pin List for the Stratix EP1S40 Device (Part 30 of 71)*

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | | | |
| IO | DIFFIO_TX58n | | B5 | VREF1B5 | M8 | R5 | P9 | R5 | | | HIGH |
| IO | DIFFIO_TX58p | | B5 | VREF1B5 | M7 | P5 | P10 | R6 | | | HIGH |
| IO | DIFFIO_RX58n | | B5 | VREF1B5 | H1 | M4 | L2 | R3 | | | HIGH |
| IO | DIFFIO_RX58p | | B5 | VREF1B5 | H2 | L4 | L3 | R4 | | | HIGH |
| IO | DIFFIO_TX57n | | B5 | VREF1B5 | L10 | M5 | N5 | R8 | | | HIGH |
| IO | DIFFIO_TX57p | | B5 | VREF1B5 | L9 | N5 | N6 | R7 | | | HIGH |
| IO | DIFFIO_RX57n/RDN5 | | B5 | VREF1B5 | H3 | K3 | M4 | P3 | | | HIGH |
| IO | DIFFIO_RX57p/RUP5 | | B5 | VREF1B5 | H4 | K4 | M5 | P4 | | | HIGH |
| IO | DIFFIO_TX56n | | B5 | VREF1B5 | L5 | M8 | N10 | P5 | | | HIGH |
| IO | DIFFIO_TX56p | | B5 | VREF1B5 | L6 | L8 | N9 | P6 | | | HIGH |
| IO | DIFFIO_RX56n | | B5 | VREF1B5 | G1 | J1 | L1 | R2 | | | HIGH |
| IO | DIFFIO_RX56p | | B5 | VREF1B5 | G2 | H1 | K2 | P1 | | | HIGH |
| VREF1B5 | | | B5 | VREF1B5 | K9 | N10 | L8 | P11 | | | |
| IO | DIFFIO_TX55n | | B5 | VREF1B5 | L8 | M7 | M8 | P7 | | | HIGH |
| IO | DIFFIO_TX55p | | B5 | VREF1B5 | L7 | L7 | M9 | P8 | | | HIGH |
| IO | DIFFIO_RX55n | | B5 | VREF1B5 | G4 | G1 | J2 | P2 | | | HIGH |
| IO | DIFFIO_RX55p | | B5 | VREF1B5 | G3 | F1 | J1 | N2 | | | HIGH |
| IO | DIFFIO_TX54n | | B5 | VREF1B5 | K7 | L5 | M6 | N5 | | | HIGH |
| IO | DIFFIO_TX54p | | B5 | VREF1B5 | K8 | K5 | M7 | N6 | | | HIGH |
| IO | DIFFIO_RX54n | | B5 | VREF1B5 | F1 | H2 | K4 | N4 | | | HIGH |
| IO | DIFFIO_RX54p | | B5 | VREF1B5 | F2 | J2 | K3 | N3 | | | HIGH |
| IO | DIFFIO_TX53n | | B5 | VREF1B5 | J7 | H5 | L6 | N8 | | | HIGH |

**Table 5–1. Pin List for the Stratix EP1S40 Device (Part 31 of 71)**

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_TX53p | | B5 | VREF1B5 | J8 | J5 | L7 | N7 | | | HIGH |
| IO | DIFFIO_RX53n | | B5 | VREF1B5 | F3 | G2 | J3 | M1 | | | HIGH |
| IO | DIFFIO_RX53p | | B5 | VREF1B5 | F4 | F2 | J4 | M2 | | | HIGH |
| IO | DIFFIO_TX52n | | B5 | VREF1B5 | K5 | F5 | K5 | M6 | | | HIGH |
| IO | DIFFIO_TX52p | | B5 | VREF1B5 | K6 | G5 | K6 | M5 | | | HIGH |
| IO | DIFFIO_RX52n | | B5 | VREF1B5 | E1 | J3 | H1 | M3 | | | HIGH |
| IO | DIFFIO_RX52p | | B5 | VREF1B5 | E2 | H3 | H2 | M4 | | | HIGH |
| IO | DIFFIO_TX51n | | B5 | VREF2B5 | J6 | L6 | K8 | L5 | | | HIGH |
| IO | DIFFIO_TX51p | | B5 | VREF2B5 | J5 | K6 | K7 | L6 | | | HIGH |
| IO | DIFFIO_RX51n | | B5 | VREF2B5 | D1 | G3 | G1 | L1 | | | HIGH |
| IO | DIFFIO_RX51p | | B5 | VREF2B5 | D2 | F3 | G2 | L2 | | | HIGH |
| IO | DIFFIO_TX50n | | B5 | VREF2B5 | H8 | J6 | J5 | M7 | | | HIGH |
| IO | DIFFIO_TX50p | | B5 | VREF2B5 | H7 | H6 | J6 | M8 | | | HIGH |
| IO | DIFFIO_RX50n | | B5 | VREF2B5 | | J4 | H3 | L3 | | | HIGH |
| IO | DIFFIO_RX50p | | B5 | VREF2B5 | | H4 | H4 | L4 | | | HIGH |
| IO | DIFFIO_TX49n | | B5 | VREF2B5 | H6 | G6 | J7 | K5 | | | HIGH |
| IO | DIFFIO_TX49p | | B5 | VREF2B5 | H5 | F6 | J8 | K6 | | | HIGH |
| IO | DIFFIO_RX49n | | B5 | VREF2B5 | | G4 | F1 | K2 | | | HIGH |
| IO | DIFFIO_RX49p | | B5 | VREF2B5 | | F4 | F2 | K1 | | | HIGH |
| IO | DIFFIO_TX48n | | B5 | VREF2B5 | G5 | K8 | H5 | L8 | | | HIGH |
| IO | DIFFIO_TX48p | | B5 | VREF2B5 | G6 | J8 | H6 | L7 | | | HIGH |
| IO | DIFFIO_RX48n | | B5 | VREF2B5 | | E2 | G3 | K3 | | | HIGH |

Table 5–1. Pin List for the Stratix EP1S40 Device (Part 32 of 71)

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed Note (1) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | | | |
| IO | DIFFIO_RX48p | | B5 | VREF2B5 | | D2 | G4 | K4 | | | HIGH |
| VREF2B5 | | | B5 | VREF2B5 | E5 | M10 | F6 | N11 | | | |
| IO | DIFFIO_TX47n | | B5 | VREF2B5 | F6 | K7 | H8 | K7 | | | HIGH |
| IO | DIFFIO_TX47p | | B5 | VREF2B5 | F5 | J7 | H7 | K8 | | | HIGH |
| IO | DIFFIO_RX47n | | B5 | VREF2B5 | C1 | E3 | F3 | J3 | | | HIGH |
| IO | DIFFIO_RX47p | | B5 | VREF2B5 | C2 | D3 | F4 | J4 | | | HIGH |
| IO | DIFFIO_TX46n | | B5 | VREF2B5 | D3 | H7 | G6 | J7 | | | HIGH |
| IO | DIFFIO_TX46p | | B5 | VREF2B5 | D4 | G7 | G5 | J8 | | | HIGH |
| IO | DIFFIO_RX46n | | B5 | VREF2B5 | | | E2 | H2 | | | LOW |
| IO | DIFFIO_RX46p | | B5 | VREF2B5 | | | E1 | H1 | | | LOW |
| IO | DIFFIO_TX45n | | B5 | VREF2B5 | E3 | G8 | G7 | M9 | | | HIGH |
| IO | DIFFIO_TX45p | | B5 | VREF2B5 | E4 | H8 | G8 | M10 | | | HIGH |
| IO | DIFFIO_RX45n | | B5 | VREF2B5 | | | F5 | G2 | | | LOW |
| IO | DIFFIO_RX45p | | B5 | VREF2B5 | | | E4 | G1 | | | LOW |
| IO | | | B5 | VREF2B5 | | | | N9 | | | |
| IO | | | B5 | VREF2B5 | | | | N10 | | | |
| FPLL10CLKn | | | B5 | VREF2B5 | | D1 | L5 | J1 | | | |
| FPLL10CLKp | | | B5 | VREF2B5 | | E1 | L4 | J2 | | | |
| GNDG_PLL10 | | | | | | K9 | E3 | L9 | | | |
| VCCG_PLL10 | | | | | | J9 | D3 | L10 | | | |
| GNDA_PLL10 | | | | | | M9 | D1 | K9 | | | |
| GND | | | | | | | | | | | |

**Table 5–1. Pin List for the Stratix EP1S40 Device (Part 33 of 71)**

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| VCCA_PLL10 | | | | | | L9 | D2 | J9 | | | |
| VCCINT | | | | | | | | | | | |
| IO | | | B4 | VREF0B4 | | D4 | F8 | F7 | | | |
| IO | DQ0T0 | | B4 | VREF0B4 | A4 | C4 | D5 | C6 | DQ0T0 | DQ0T0 | |
| IO | | | B4 | VREF0B4 | G7 | | F7 | C4 | | | |
| IO | DQ0T1 | | B4 | VREF0B4 | A3 | C5 | C3 | B6 | DQ0T1 | DQ0T1 | |
| IO | | | B4 | VREF0B4 | | E4 | J9 | E5 | | | |
| IO | DQ0T2 | | B4 | VREF0B4 | B3 | D5 | E5 | C7 | DQ0T2 | DQ0T2 | |
| IO | | | B4 | VREF0B4 | | H9 | G9 | B4 | | | |
| IO | DQS0T | | B4 | VREF0B4 | D5 | B4 | C5 | B7 | | | |
| IO | | | B4 | VREF0B4 | F7 | E5 | H9 | E6 | | | |
| IO | DQ0T3 | | B4 | VREF0B4 | B5 | B5 | C4 | A7 | DQ0T3 | DQ0T3 | |
| IO | | | B4 | VREF0B4 | | C2 | K9 | G7 | | | |
| IO | DQ0T4 | | B4 | VREF0B4 | B4 | B3 | D4 | C8 | DQ0T4 | DQ0T4 | |
| VREF0B4 | | | B4 | VREF0B4 | E7 | K10 | E6 | L11 | | | |
| IO | | | B4 | VREF0B4 | | J10 | F9 | D6 | | | |
| IO | DQ0T5 | | B4 | VREF0B4 | C4 | C3 | A4 | A6 | DQ0T5 | DQ0T5 | |
| IO | | | B4 | VREF0B4 | G8 | F7 | L9 | G8 | | | |
| IO | DQ0T6 | | B4 | VREF0B4 | A5 | A5 | B4 | A8 | DQ0T6 | DQ0T6 | |
| IO | | | B4 | VREF0B4 | J9 | | K10 | D5 | | | |
| IO | DQ0T7 | | B4 | VREF0B4 | C5 | A4 | B3 | B8 | DQ0T7 | DQ0T7 | |
| IO | | | B4 | VREF0B4 | | F8 | H10 | G9 | | | |

**Table 5–1. Pin List for the Stratix EP1S40 Device (Part 34 of 71)**

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed Note (1) |
| IO | | | B4 | VREF0B4 | F8 | | | B5 | | | |
| IO | DQ1T0 | | B4 | VREF0B4 | E6 | E6 | D6 | C9 | DQ0T8 | DQ0T8 | |
| IO | | | B4 | VREF0B4 | | E7 | J10 | F8 | | | |
| IO | DQ1T1 | | B4 | VREF0B4 | A6 | C7 | C6 | B9 | DQ0T9 | DQ0T9 | |
| IO | | | B4 | VREF0B4 | | | L10 | C5 | | | |
| IO | DQ1T2 | | B4 | VREF1B4 | B7 | D7 | B5 | A9 | DQ0T10 | DQ0T10 | |
| IO | | | B4 | VREF1B4 | | H10 | F10 | E8 | | | |
| IO | DQS1T | | B4 | VREF1B4 | B6 | C6 | E7 | B10 | DQS0T | | |
| IO | | | B4 | VREF1B4 | H9 | G9 | G10 | A4 | | | |
| IO | DQ1T3 | | B4 | VREF1B4 | D6 | A6 | C7 | C11 | DQ0T11 | DQ0T11 | |
| IO | | | B4 | VREF1B4 | | L11 | M10 | E7 | | | |
| IO | DQ1T4 | | B4 | VREF1B4 | A7 | B6 | A5 | A10 | DQ0T12 | DQ0T12 | |
| IO | DQ1T7 | | B4 | VREF1B4 | C7 | B7 | B6 | B11 | DQ0T15 | DQ0T15 | |
| IO | DQ1T5 | | B4 | VREF1B4 | D7 | D6 | D7 | C10 | DQ0T13 | DQ0T13 | |
| IO | | | B4 | VREF1B4 | G9 | J11 | K11 | G10 | | | |
| IO | DQ1T6 | | B4 | VREF1B4 | C6 | A7 | A6 | A11 | DQ0T14 | DQ0T14 | |
| IO | | | B4 | VREF1B4 | | | L11 | D7 | | | |
| VREF1B4 | | | B4 | VREF1B4 | E9 | K11 | E8 | L12 | | | |
| IO | | | B4 | VREF1B4 | | F9 | J11 | E9 | | | |
| IO | | | B4 | VREF1B4 | | E9 | H11 | E10 | | | |
| IO | | | B4 | VREF1B4 | | | | D8 | | | |
| IO | DQ2T0 | | B4 | VREF1B4 | D8 | B8 | B7 | A12 | DQ1T0 | DQ0T16 | |

**Table 5–1. Pin List for the Stratix EP1S40 Device (Part 35 of 71)**

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | | | B4 | VREF1B4 | | | M11 | F9 | | | |
| IO | DQ2T1 | | B4 | VREF1B4 | C8 | D9 | D8 | D12 | DQ1T1 | DQ0T17 | |
| IO | | | B4 | VREF1B4 | F9 | H11 | G11 | D9 | | | |
| IO | DQ2T2 | | B4 | VREF1B4 | E8 | E8 | B8 | E12 | DQ1T2 | DQ0T18 | |
| IO | | | B4 | VREF1B4 | | G10 | K12 | F10 | | | |
| IO | DQS2T | | B4 | VREF1B4 | C9 | C8 | A7 | C12 | | DQS0T | |
| IO | | | B4 | VREF1B4 | | | L12 | A5 | | | |
| IO | DQ2T3 | | B4 | VREF1B4 | D9 | C9 | E9 | E13 | DQ1T3 | DQ0T19 | |
| IO | | | B4 | VREF1B4 | | | F11 | F11 | | | |
| IO | DQ2T4 | | B4 | VREF1B4 | B9 | D8 | A8 | B12 | DQ1T4 | DQ0T20 | |
| IO | | | B4 | VREF1B4 | H10 | J12 | J12 | G11 | | | |
| IO | DQ2T5 | | B4 | VREF1B4 | B8 | A9 | C9 | B13 | DQ1T5 | DQ0T21 | |
| IO | DQ2T6 | | B4 | VREF1B4 | A8 | B9 | C8 | C13 | DQ1T6 | DQ0T22 | |
| IO | DQ2T7 | | B4 | VREF1B4 | A9 | A8 | D9 | D13 | DQ1T7 | DQ0T23 | |
| IO | FCLK6 | | B4 | VREF2B4 | G10 | F10 | G12 | D11 | | | |
| IO | FCLK7 | | B4 | VREF2B4 | F10 | F11 | A14 | G14 | | | |
| IO | | | B4 | VREF2B4 | J10 | G11 | H12 | D10 | | | |
| IO | | | B4 | VREF2B4 | | | | F12 | | | |
| IO | DQ3T0 | | B4 | VREF2B4 | E10 | B10 | E11 | C14 | DQ1T8 | DQ0T24 | |
| IO | | | B4 | VREF2B4 | | | K13 | G12 | | | |
| IO | DQ3T1 | | B4 | VREF2B4 | A10 | D10 | B9 | D14 | DQ1T9 | DQ0T25 | |
| IO | | | B4 | VREF2B4 | F11 | G12 | F13 | F13 | | | |

**Table 5–1. Pin List for the Stratix EP1S40 Device (Part 36 of 71)**

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | | | |
| IO | DQ3T2 | | B4 | VREF2B4 | C10 | E10 | D10 | E14 | DQ1T10 | DQ0T26 | |
| IO | | | B4 | VREF2B4 | K10 | H12 | F12 | G13 | | | |
| IO | DQS3T | | B4 | VREF2B4 | D10 | C10 | D11 | C15 | DQS1T | | |
| IO | | | B4 | VREF2B4 | G12 | L12 | L14 | E11 | | | |
| VREF2B4 | | | B4 | VREF2B4 | E11 | K12 | E10 | L13 | | | |
| IO | DQ3T3 | | B4 | VREF2B4 | B10 | D11 | C10 | A14 | DQ1T11 | DQ0T27 | |
| IO | | | B4 | VREF2B4 | | H13 | B14 | G15 | | | |
| IO | DQ3T4 | | B4 | VREF2B4 | A11 | E11 | A9 | B14 | DQ1T12 | DQ0T28 | |
| IO | | | B4 | VREF2B4 | | J13 | H13 | F14 | | | |
| IO | DQ3T5 | | B4 | VREF2B4 | C11 | B11 | B11 | B15 | DQ1T13 | DQ0T29 | |
| IO | DEV_OE | | B4 | VREF2B4 | J11 | F12 | L13 | P16 | | | |
| IO | RUP4 | | B4 | VREF2B4 | H11 | F13 | G13 | F15 | | | |
| IO | RDN4 | | B4 | VREF2B4 | G11 | E14 | J13 | E16 | | | |
| IO | DQ3T7 | | B4 | VREF2B4 | B11 | A10 | B10 | D15 | DQ1T15 | DQ0T31 | |
| IO | | | B4 | VREF2B4 | | | C14 | G16 | | | |
| IO | DQ3T6 | | B4 | VREF2B4 | D11 | C11 | C11 | E15 | DQ1T14 | DQ0T30 | |
| IO | DQ4T0 | | B4 | VREF2B4 | B12 | D12 | A11 | A16 | | | |
| IO | | nWS | B4 | VREF2B4 | K11 | F14 | D14 | F16 | | | |
| IO | DQ4T1 | | B4 | VREF2B4 | C12 | E12 | B12 | D16 | | | |
| IO | | | B4 | VREF2B4 | | | H14 | F17 | | | |
| IO | DQ4T2 | | B4 | VREF2B4 | D12 | A12 | C12 | A17 | | | |
| IO | | | B4 | VREF2B4 | | G13 | K14 | G17 | | | |

*Table 5–1. Pin List for the Stratix EP1S40 Device (Part 37 of 71)*

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **780-Pin FBGA** | **956-Pin BGA** | **1020-Pin FBGA** | **1508-Pin FBGA** | | | |
| IO | DQS4T | | B4 | VREF2B4 | A13 | C12 | D12 | C16 | | | |
| IO | | DATA0 | B4 | VREF3B4 | H12 | E15 | E14 | M17 | | | |
| IO | DQ4T3 | | B4 | VREF3B4 | B13 | B12 | C13 | B16 | | | |
| IO | | | B4 | VREF3B4 | | G14 | J14 | C18 | | | |
| IO | DQ4T4 | | B4 | VREF3B4 | E12 | C13 | D13 | B17 | | | |
| IO | | | B4 | VREF3B4 | L11 | L14 | L15 | D18 | | | |
| IO | DQ4T5 | | B4 | VREF3B4 | C13 | D13 | E13 | D17 | | | |
| IO | | DATA1 | B4 | VREF3B4 | F12 | C16 | F14 | J17 | | | |
| IO | DQ4T6 | | B4 | VREF3B4 | D13 | E13 | A13 | E17 | | | |
| IO | | | B4 | VREF3B4 | | | J15 | E18 | | | |
| IO | DQ4T7 | | B4 | VREF3B4 | E13 | B13 | B13 | C17 | | | |
| IO | | | B4 | VREF3B4 | M11 | L16 | K15 | F18 | | | |
| IO | | DATA2 | B4 | VREF3B4 | J12 | F15 | F15 | K18 | | | |
| VREF3B4 | | | B4 | VREF3B4 | | K13 | E12 | L14 | | | |
| TMS | | TMS | B4 | VREF3B4 | F13 | D16 | E15 | F19 | | | |
| TRST | | TRST | B4 | VREF3B4 | L12 | G15 | G15 | H19 | | | |
| TCK | | TCK | B4 | VREF3B4 | K12 | F16 | G14 | E20 | | | |
| IO | | DATA3 | B4 | VREF3B4 | M12 | G17 | C16 | P21 | | | |
| IO | | | B4 | VREF3B4 | | | | H18 | | | |
| IO | | | B4 | VREF3B4 | | | | G18 | | | |
| TDI | | TDI | B4 | VREF3B4 | G13 | E16 | D16 | F20 | | | |
| TDO | | TDO | B4 | VREF3B4 | H13 | G16 | F16 | G20 | | | |

**Table 5–1. Pin List for the Stratix EP1S40 Device (Part 38 of 71)**

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | CLK12n | | B4 | VREF3B4 | J13 | B14 | A15 | A18 | | | |
| CLK12p | | | B4 | VREF3B4 | K13 | A14 | B15 | B18 | | | |
| IO | CLK13n/PLL11_OUT | | B4 | VREF3B4 | L13 | D14 | C15 | C19 | | | |
| CLK13p | | | B4 | VREF3B4 | M13 | C14 | D15 | D19 | | | |
| VCCINT | | | | | | | | | | | |
| VCCA_PLL11 | | | | | | J14 | E16 | K19 | | | |
| GND | | | | | | | | | | | |
| GNDA_PLL11 | | | | | | H14 | E17 | J19 | | | |
| VCCG_PLL11 | | | | | | H15 | H16 | L19 | | | |
| GNDG_PLL11 | | | | | | J15 | H15 | M19 | | | |
| TEMPDIODEp | | | | | B14 | E17 | E18 | F21 | | | |
| TEMPDIODEn | | | | | C14 | F17 | F18 | H21 | | | |
| VCCINT | | | | | | | | | | | |
| VCCA_PLL5 | | | | | F14 | J17 | G17 | L21 | | | |
| GND | | | | | | | | | | | |
| GNDA_PLL5 | | | | | G14 | H16 | F17 | M21 | | | |
| VCCG_PLL5 | | | | | D14 | K15 | J16 | L20 | | | |
| GNDG_PLL5 | | | | | E14 | K17 | L16 | M20 | | | |
| VCC_PLL5_OUTA | | | B9 | | F15 | L18 | H17 | J20 | | | |
| VCC_PLL5_OUTA | | | B9 | | | | | | | | |
| VCC_PLL5_OUTB | | | B10 | | G16 | J18 | L17 | K21 | | | |
| VCC_PLL5_OUTB | | | B10 | | | | | | | | |

*Table 5–1. Pin List for the Stratix EP1S40 Device (Part 39 of 71)*

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | PLL5_OUT0p | | B9 | VREF0B3 | E15 | B16 | B16 | C21 | | | |
| IO | PLL5_OUT0n | | B9 | VREF0B3 | D15 | A16 | A16 | D21 | | | |
| IO | PLL5_OUT1p | | B9 | VREF0B3 | K14 | B15 | B17 | C20 | | | |
| IO | PLL5_OUT1n | | B9 | VREF0B3 | K15 | A15 | A17 | D20 | | | |
| IO | PLL5_FBp | | B9 | VREF0B3 | H14 | D15 | D17 | B19 | | | |
| IO | PLL5_FBn | | B9 | VREF0B3 | H15 | C15 | C17 | A19 | | | |
| IO | PLL5_OUT2p | | B10 | VREF0B3 | C15 | D17 | B18 | B21 | | | |
| IO | PLL5_OUT2n | | B10 | VREF0B3 | B15 | C17 | A18 | A21 | | | |
| IO | PLL5_OUT3p | | B10 | VREF0B3 | K16 | B17 | D18 | A20 | | | |
| IO | PLL5_OUT3n | | B10 | VREF0B3 | J16 | A17 | C18 | B20 | | | |
| nSTATUS | | nSTATUS | B3 | VREF0B3 | M16 | E18 | G16 | N21 | | | |
| nCONFIG | | nCONFIG | B3 | VREF0B3 | L16 | F19 | J18 | L22 | | | |
| DCLK | | DCLK | B3 | VREF0B3 | F16 | F18 | E19 | G21 | | | |
| CONF_DONE | | CONF_DONE | B3 | VREF0B3 | G17 | G18 | G18 | H22 | | | |
| CLK14p | | | B3 | VREF0B3 | K17 | A18 | A19 | B22 | | | |
| IO | CLK14n | | B3 | VREF0B3 | J17 | B18 | B19 | A22 | | | |
| CLK15p | | | B3 | VREF0B3 | M17 | C18 | C19 | D22 | | | |
| IO | CLK15n | | B3 | VREF0B3 | L17 | D18 | D19 | C22 | | | |
| VREF0B3 | | | B3 | VREF0B3 | E18 | K18 | E21 | L25 | | | |
| IO | | | B3 | VREF0B3 | | | | G22 | | | |
| IO | | | B3 | VREF0B3 | | | | E22 | | | |
| IO | | DATA4 | B3 | VREF0B3 | H17 | G19 | G19 | L23 | | | |

**Table 5–1. Pin List for the Stratix EP1S40 Device (Part 40 of 71)**

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | | | |
| IO | | | B3 | VREF0B3 | | | | F22 | | | |
| IO | | | B3 | VREF0B3 | | | | E21 | | | |
| IO | | | B3 | VREF0B3 | | | | F23 | | | |
| IO | | | B3 | VREF0B3 | | | | G23 | | | |
| IO | | | B3 | VREF0B3 | L18 | H19 | H19 | H23 | | | |
| IO | DQ5T0 | | B3 | VREF0B3 | D16 | B19 | A20 | B23 | | | |
| IO | | | B3 | VREF0B3 | | | K18 | F24 | | | |
| IO | DQ5T1 | | B3 | VREF0B3 | C16 | C19 | B20 | E23 | | | |
| IO | | DATA5 | B3 | VREF0B3 | K18 | F20 | J19 | J23 | | | |
| IO | DQ5T2 | | B3 | VREF1B3 | E16 | D19 | C20 | D23 | | | |
| IO | | | B3 | VREF1B3 | | | F19 | G24 | | | |
| IO | DQS5T | | B3 | VREF1B3 | A16 | C20 | D20 | C23 | | | |
| IO | | | B3 | VREF1B3 | | | | H24 | | | |
| IO | DQ5T3 | | B3 | VREF1B3 | B16 | E19 | E20 | A23 | | | |
| IO | | DATA6 | B3 | VREF1B3 | H18 | F21 | K19 | E24 | | | |
| IO | DQ5T4 | | B3 | VREF1B3 | E17 | A20 | B21 | A24 | | | |
| IO | | | B3 | VREF1B3 | | J19 | F20 | F25 | | | |
| IO | DQ5T5 | | B3 | VREF1B3 | D17 | B20 | C21 | B24 | | | |
| IO | | | B3 | VREF1B3 | M18 | H20 | L18 | G25 | | | |
| IO | DQ5T6 | | B3 | VREF1B3 | B17 | D20 | D21 | C24 | | | |
| IO | | | B3 | VREF1B3 | | | L20 | H25 | | | |
| IO | DQ5T7 | | B3 | VREF1B3 | C17 | E20 | A22 | D24 | | | |

Table 5–1. Pin List for the Stratix EP1S40 Device (Part 41 of 71)

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | | | |
| IO | DQ6T1 | | B3 | VREF1B3 | C18 | C21 | C22 | E25 | DQ2T1 | DQ1T1 | |
| IO | | | B3 | VREF1B3 | F17 | L19 | K20 | H26 | | | |
| IO | DQ6T0 | | B3 | VREF1B3 | A18 | B21 | B22 | B25 | DQ2T0 | DQ1T0 | |
| IO | RUP3 | | B3 | VREF1B3 | J18 | F22 | F21 | P23 | | | |
| IO | RDN3 | | B3 | VREF1B3 | K19 | F24 | L19 | M24 | | | |
| VREF1B3 | | | B3 | VREF1B3 | | K19 | E23 | L26 | | | |
| IO | | DATA7 | B3 | VREF1B3 | G18 | G20 | J20 | P25 | | | |
| IO | DQ6T2 | | B3 | VREF1B3 | D18 | A22 | B23 | D25 | DQ2T2 | DQ1T2 | |
| IO | | | B3 | VREF1B3 | | | H20 | F27 | | | |
| IO | DQS6T | | B3 | VREF1B3 | B18 | C22 | D22 | C25 | DQS2T | | |
| IO | | | B3 | VREF1B3 | | | | F26 | | | |
| IO | DQ6T3 | | B3 | VREF1B3 | A19 | D21 | C23 | A26 | DQ2T3 | DQ1T3 | |
| IO | | CLKUSR | B3 | VREF1B3 | J19 | F23 | H21 | J25 | | | |
| IO | DQ6T4 | | B3 | VREF1B3 | B19 | E21 | A24 | B26 | DQ2T4 | DQ1T4 | |
| IO | | | B3 | VREF1B3 | | | G20 | G27 | | | |
| IO | DQ6T5 | | B3 | VREF1B3 | C19 | B22 | E22 | C26 | DQ2T5 | DQ1T5 | |
| IO | DQ6T6 | | B3 | VREF1B3 | E19 | D22 | B24 | D26 | DQ2T6 | DQ1T6 | |
| IO | DQ6T7 | | B3 | VREF1B3 | D19 | E22 | D23 | E26 | DQ2T7 | DQ1T7 | |
| IO | FCLK0 | | B3 | VREF2B3 | F19 | E23 | F22 | G26 | | | |
| IO | FCLK1 | | B3 | VREF2B3 | G19 | E25 | G22 | D29 | | | |
| IO | | | B3 | VREF2B3 | | | | F28 | | | |
| IO | | | B3 | VREF2B3 | H19 | J20 | K21 | H27 | | | |

*Table 5–1. Pin List for the Stratix EP1S40 Device (Part 42 of 71)*

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | | | |
| IO | DQ7T0 | | B3 | VREF2B3 | B20 | A23 | D24 | B27 | DQ2T8 | DQ1T8 | |
| IO | | | B3 | VREF2B3 | | | | F29 | | | |
| IO | DQ7T1 | | B3 | VREF2B3 | A20 | B23 | A25 | C27 | DQ2T9 | DQ1T9 | |
| IO | | | B3 | VREF2B3 | | | | E29 | | | |
| IO | DQ7T2 | | B3 | VREF2B3 | C20 | A24 | C24 | D27 | DQ2T10 | DQ1T10 | |
| IO | | | B3 | VREF2B3 | | G21 | J21 | G28 | | | |
| IO | DQS7T | | B3 | VREF2B3 | D20 | C24 | B26 | C28 | | DQS1T | |
| IO | | | B3 | VREF2B3 | | | L21 | F30 | | | |
| IO | DQ7T3 | | B3 | VREF2B3 | A21 | C23 | B25 | E27 | DQ2T11 | DQ1T11 | |
| IO | | | B3 | VREF2B3 | | H21 | G21 | D30 | | | |
| IO | DQ7T4 | | B3 | VREF2B3 | B21 | D24 | C25 | B28 | DQ2T12 | DQ1T12 | |
| IO | | | B3 | VREF2B3 | | | H22 | G29 | | | |
| IO | DQ7T5 | | B3 | VREF2B3 | C21 | B24 | D25 | A28 | DQ2T13 | DQ1T13 | |
| IO | | | B3 | VREF2B3 | J20 | L21 | L22 | G30 | | | |
| VREF2B3 | | | B3 | VREF2B3 | E20 | K20 | E25 | L27 | | | |
| IO | DQ7T6 | | B3 | VREF2B3 | D21 | D23 | A26 | D28 | DQ2T14 | DQ1T14 | |
| IO | | | B3 | VREF2B3 | | | | D31 | | | |
| IO | DQ7T7 | | B3 | VREF2B3 | E21 | E24 | E24 | E28 | DQ2T15 | DQ1T15 | |
| IO | | | B3 | VREF2B3 | H20 | J21 | J22 | D32 | | | |
| IO | | | B3 | VREF2B3 | | | | A35 | | | |
| IO | | | B3 | VREF2B3 | | | K22 | F31 | | | |
| IO | | | B3 | VREF2B3 | | | | E30 | | | |

**Table 5–1. Pin List for the Stratix EP1S40 Device  (Part 43 of 71)**

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DQ8T1 | | B3 | VREF2B3 | A22 | C25 | A28 | B29 | DQ3T1 | DQ1T17 | |
| IO | | | B3 | VREF2B3 | F18 | G22 | F23 | E31 | | | |
| IO | DQ8T2 | | B3 | VREF2B3 | C22 | B25 | A27 | C29 | DQ3T2 | DQ1T18 | |
| IO | DQ8T0 | | B3 | VREF2B3 | B22 | A25 | C26 | A29 | DQ3T0 | DQ1T16 | |
| IO | DQS8T | | B3 | VREF2B3 | D23 | C26 | B27 | B30 | DQS3T | | |
| GND | | | | | | | | | | | |
| GND | | | | | | | | | | | |
| GND | | | | | G20 | D28 | H24 | E32 | | | |
| IO | | | B3 | VREF3B3 | | | G23 | D33 | | | |
| IO | DQ8T3 | | B3 | VREF3B3 | D22 | D25 | D26 | C30 | DQ3T3 | DQ1T19 | |
| IO | | | B3 | VREF3B3 | F20 | H22 | J23 | A36 | | | |
| IO | DQ8T4 | | B3 | VREF3B3 | A23 | A26 | C27 | A30 | DQ3T4 | DQ1T20 | |
| IO | | | B3 | VREF3B3 | | | L23 | F32 | | | |
| IO | DQ8T5 | | B3 | VREF3B3 | C23 | B26 | B28 | A31 | DQ3T5 | DQ1T21 | |
| IO | | | B3 | VREF3B3 | | | | B35 | | | |
| IO | DQ8T6 | | B3 | VREF3B3 | E23 | E26 | D27 | B31 | DQ3T6 | DQ1T22 | |
| IO | | | B3 | VREF3B3 | G21 | G23 | H23 | G31 | | | |
| IO | DQ8T7 | | B3 | VREF3B3 | B23 | D26 | E26 | C31 | DQ3T7 | DQ1T23 | |
| IO | | | B3 | VREF3B3 | | | | D34 | | | |
| IO | | | B3 | VREF3B3 | G22 | H23 | K23 | G32 | | | |
| IO | DQ9T0 | | B3 | VREF3B3 | A24 | B27 | A29 | A32 | DQ3T8 | DQ1T24 | |
| IO | | | B3 | VREF3B3 | | | | E33 | | | |

**Table 5–1. Pin List for the Stratix EP1S40 Device (Part 44 of 71)**

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DQ9T1 | | B3 | VREF3B3 | C25 | C27 | B29 | C32 | DQ3T9 | DQ1T25 | |
| IO | | | B3 | VREF3B3 | | J22 | F24 | B36 | | | |
| IO | DQ9T2 | | B3 | VREF3B3 | A25 | A27 | B30 | B32 | DQ3T10 | DQ1T26 | |
| IO | | | B3 | VREF3B3 | | E27 | L24 | D35 | | | |
| VREF3B3 | | | B3 | VREF3B3 | E22 | K21 | E27 | L28 | | | |
| IO | DQS9T | | B3 | VREF3B3 | C24 | B28 | C28 | B33 | | | |
| IO | | | B3 | VREF3B3 | | | G24 | C35 | | | |
| IO | DQ9T3 | | B3 | VREF3B3 | D24 | D27 | C29 | A34 | DQ3T11 | DQ1T27 | |
| IO | | | B3 | VREF3B3 | F21 | F25 | F25 | E34 | | | |
| IO | DQ9T4 | | B3 | VREF3B3 | B24 | A28 | D29 | A33 | DQ3T12 | DQ1T28 | |
| IO | | | B3 | VREF3B3 | | | K24 | G33 | | | |
| IO | DQ9T5 | | B3 | VREF3B3 | B25 | C28 | D28 | C33 | DQ3T13 | DQ1T29 | |
| IO | | | B3 | VREF3B3 | | | | F33 | | | |
| IO | DQ9T6 | | B3 | VREF3B3 | A26 | C29 | C30 | C34 | DQ3T14 | DQ1T30 | |
| IO | | | B3 | VREF3B3 | F22 | C30 | F26 | C36 | | | |
| IO | DQ9T7 | | B3 | VREF3B3 | B26 | B29 | E28 | B34 | DQ3T15 | DQ1T31 | |
| IO | | | B3 | VREF3B3 | | E28 | J24 | E35 | | | |
| VCCIO2 | | | | | B28 | C31 | C31 | C39 | | | |
| VCCIO2 | | | | | M28 | N31 | C32 | R39 | | | |
| VCCIO2 | | | | | P20 | T23 | M32 | W35 | | | |
| VCCIO2 | | | | | | | T23 | V25 | | | |
| VCCIO2 | | | | | | | | H33 | | | |

**Table 5–1. Pin List for the Stratix EP1S40 Device (Part 45 of 71)**

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | | | |
| VCCIO1 | | | | | R20 | U20 | AA32 | AA25 | | | |
| VCCIO1 | | | | | U28 | W31 | AK31 | Y32 | | | |
| VCCIO1 | | | | | AG28 | AJ31 | AK32 | AE39 | | | |
| VCCIO1 | | | | | | | U23 | AU39 | | | |
| VCCIO1 | | | | | | | | AM33 | | | |
| VCCIO8 | | | | | Y15 | AL29 | AC17 | AW37 | | | |
| VCCIO8 | | | | | AH17 | AL19 | AM21 | AW25 | | | |
| VCCIO8 | | | | | AH27 | Y17 | AM30 | AR21 | | | |
| VCCIO8 | | | | | | | | AE22 | | | |
| VCCIO8 | | | | | | | | AM30 | | | |
| VCCIO7 | | | | | Y14 | AC16 | AC16 | AE19 | | | |
| VCCIO7 | | | | | AH2 | AL13 | AM12 | AM20 | | | |
| VCCIO7 | | | | | AH12 | AL3 | AM3 | AW15 | | | |
| VCCIO7 | | | | | | | | AW3 | | | |
| VCCIO7 | | | | | | | | AM10 | | | |
| VCCIO6 | | | | | R9 | AJ1 | AA1 | AU1 | | | |
| VCCIO6 | | | | | U1 | W1 | AK1 | AM7 | | | |
| VCCIO6 | | | | | AG1 | U12 | AK2 | AE1 | | | |
| VCCIO6 | | | | | | | U10 | AA5 | | | |
| VCCIO6 | | | | | | | | AB15 | | | |
| VCCIO5 | | | | | B1 | T9 | C1 | W15 | | | |
| VCCIO5 | | | | | M1 | N1 | C2 | Y8 | | | |

**Table 5–1. Pin List for the Stratix EP1S40 Device (Part 46 of 71)**

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| VCCIO5 | | | | | P9 | C1 | M1 | R1 | | | |
| VCCIO5 | | | | | | | T10 | H7 | | | |
| VCCIO5 | | | | | | | | C1 | | | |
| VCCIO4 | | | | | A2 | A3 | A12 | A3 | | | |
| VCCIO4 | | | | | A12 | A13 | A3 | A15 | | | |
| VCCIO4 | | | | | J14 | J16 | K16 | E19 | | | |
| VCCIO4 | | | | | | | | R18 | | | |
| VCCIO4 | | | | | | | | H10 | | | |
| VCCIO3 | | | | | A17 | M17 | A21 | H20 | | | |
| VCCIO3 | | | | | A27 | A19 | A30 | R21 | | | |
| VCCIO3 | | | | | J15 | A29 | K17 | A25 | | | |
| VCCIO3 | | | | | | | | A37 | | | |
| VCCIO3 | | | | | | | | H30 | | | |
| VCCINT | | | | | M14 | AA12 | M12 | AA16 | | | |
| VCCINT | | | | | N11 | AA14 | M14 | AA18 | | | |
| VCCINT | | | | | N13 | AA20 | M19 | AA22 | | | |
| VCCINT | | | | | N15 | L13 | M21 | AA24 | | | |
| VCCINT | | | | | N17 | L20 | N13 | AB17 | | | |
| VCCINT | | | | | P12 | M11 | N15 | AB19 | | | |
| VCCINT | | | | | P14 | M13 | N18 | AB21 | | | |
| VCCINT | | | | | P16 | M15 | N20 | AB23 | | | |
| VCCINT | | | | | R13 | M19 | P12 | AB25 | | | |

Table 5–1. Pin List for the Stratix EP1S40 Device (Part 47 of 71)

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | | | |
| VCCINT | | | | | R15 | M21 | P14 | AC16 | | | |
| VCCINT | | | | | R17 | N12 | P16 | AC18 | | | |
| VCCINT | | | | | T12 | N14 | P17 | AC20 | | | |
| VCCINT | | | | | T14 | N16 | P19 | AC22 | | | |
| VCCINT | | | | | T16 | N18 | P21 | AC24 | | | |
| VCCINT | | | | | T18 | N20 | R13 | AD15 | | | |
| VCCINT | | | | | U11 | P11 | R15 | AD17 | | | |
| VCCINT | | | | | U13 | P13 | R18 | AD19 | | | |
| VCCINT | | | | | U15 | P14 | R20 | AD21 | | | |
| VCCINT | | | | | U17 | P15 | T14 | AD23 | | | |
| VCCINT | | | | | V12 | P17 | T16 | AD25 | | | |
| VCCINT | | | | | V16 | P19 | T17 | AE16 | | | |
| VCCINT | | | | | | P21 | T19 | AE18 | | | |
| VCCINT | | | | | | R12 | U14 | AE20 | | | |
| VCCINT | | | | | | R13 | U16 | AE24 | | | |
| VCCINT | | | | | | R14 | U17 | R16 | | | |
| VCCINT | | | | | | R18 | U19 | R20 | | | |
| VCCINT | | | | | | R19 | V13 | R22 | | | |
| VCCINT | | | | | | R20 | V15 | R24 | | | |
| VCCINT | | | | | | T11 | V18 | T15 | | | |
| VCCINT | | | | | | T13 | V20 | T17 | | | |
| VCCINT | | | | | | T19 | W14 | T19 | | | |

**Table 5–1. Pin List for the Stratix EP1S40 Device (Part 48 of 71)**

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| VCCINT | | | | | | T21 | W16 | T21 | | | |
| VCCINT | | | | | | U10 | W17 | T23 | | | |
| VCCINT | | | | | | U14 | W19 | T25 | | | |
| VCCINT | | | | | | U18 | Y13 | U16 | | | |
| VCCINT | | | | | | U22 | Y15 | U18 | | | |
| VCCINT | | | | | | V11 | Y18 | U20 | | | |
| VCCINT | | | | | | V13 | Y20 | U22 | | | |
| VCCINT | | | | | | V15 | | U24 | | | |
| VCCINT | | | | | | V17 | | V15 | | | |
| VCCINT | | | | | | V19 | | V17 | | | |
| VCCINT | | | | | | V21 | | V19 | | | |
| VCCINT | | | | | | W12 | | V21 | | | |
| VCCINT | | | | | | W14 | | V23 | | | |
| VCCINT | | | | | | W16 | | W16 | | | |
| VCCINT | | | | | | W18 | | W18 | | | |
| VCCINT | | | | | | W20 | | W22 | | | |
| VCCINT | | | | | | Y11 | | W24 | | | |
| VCCINT | | | | | | Y13 | | Y15 | | | |
| VCCINT | | | | | | Y15 | | Y17 | | | |
| VCCINT | | | | | | Y19 | | Y23 | | | |
| VCCINT | | | | | | Y21 | | Y25 | | | |
| GND | | | | | A14 | A1 | A10 | A13 | | | |

Table 5–1. Pin List for the Stratix EP1S40 Device (Part 49 of 71)

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| GND | | | | | A15 | A11 | A2 | A2 | | | |
| GND | | | | | AA16 | A2 | A23 | A27 | | | |
| GND | | | | | AC15 | A21 | A31 | A38 | | | |
| GND | | | | | AF26 | A30 | AA16 | AA15 | | | |
| GND | | | | | AF3 | A31 | AA17 | AA17 | | | |
| GND | | | | | AG2 | AA17 | AC1 | AA23 | | | |
| GND | | | | | AG27 | AA18 | AC32 | AA7 | | | |
| GND | | | | | AH14 | AB16 | AD17 | AB16 | | | |
| GND | | | | | AH15 | AD18 | AF17 | AB18 | | | |
| GND | | | | | B2 | AK1 | AL1 | AB20 | | | |
| GND | | | | | B27 | AK2 | AL2 | AB22 | | | |
| GND | | | | | C26 | AK30 | AL31 | AB24 | | | |
| GND | | | | | C3 | AK31 | AL32 | AC15 | | | |
| GND | | | | | G15 | AL1 | AM10 | AC17 | | | |
| GND | | | | | H16 | AL11 | AM2 | AC19 | | | |
| GND | | | | | L14 | AL2 | AM23 | AC21 | | | |
| GND | | | | | L15 | AL21 | AM31 | AC23 | | | |
| GND | | | | | M15 | AL30 | B1 | AC25 | | | |
| GND | | | | | N12 | AL31 | B2 | AD16 | | | |
| GND | | | | | N14 | B1 | B31 | AD18 | | | |
| GND | | | | | N16 | B2 | B32 | AD20 | | | |
| GND | | | | | N18 | B30 | H18 | AD22 | | | |

Table 5–1. Pin List for the Stratix EP1S40 Device (Part 50 of 71)

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| GND | | | | | P1 | B31 | J17 | AD24 | | | |
| GND | | | | | P11 | H17 | K1 | AE15 | | | |
| GND | | | | | P13 | H18 | K32 | AE17 | | | |
| GND | | | | | P15 | K16 | M13 | AE21 | | | |
| GND | | | | | P17 | L15 | M15 | AE23 | | | |
| GND | | | | | P18 | L17 | M16 | AE25 | | | |
| GND | | | | | P28 | M1 | M17 | AG1 | | | |
| GND | | | | | R1 | M12 | M18 | AG39 | | | |
| GND | | | | | R11 | M14 | M20 | AK10 | | | |
| GND | | | | | R12 | M16 | N12 | AK20 | | | |
| GND | | | | | R14 | M18 | N14 | AK22 | | | |
| GND | | | | | R16 | M20 | N16 | AK30 | | | |
| GND | | | | | R18 | M31 | N17 | AL21 | | | |
| GND | | | | | R28 | N11 | N19 | AM32 | | | |
| GND | | | | | T11 | N13 | N21 | AM8 | | | |
| GND | | | | | T13 | N15 | P13 | AN21 | | | |
| GND | | | | | T15 | N17 | P15 | AU3 | | | |
| GND | | | | | T17 | N19 | P18 | AU37 | | | |
| GND | | | | | | N21 | P20 | AV1 | | | |
| GND | | | | | U14 | P12 | R14 | AV2 | | | |
| GND | | | | | U16 | P16 | R16 | AV38 | | | |
| GND | | | | | | P18 | R17 | AV39 | | | |

**Table 5–1. Pin List for the Stratix EP1S40 Device (Part 51 of 71)**

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| GND | | | | | V13 | P20 | R19 | AW13 | | | |
| GND | | | | | V14 | R11 | T12 | AW2 | | | |
| GND | | | | | V15 | R15 | T13 | AW27 | | | |
| GND | | | | | V17 | R17 | T15 | AW38 | | | |
| GND | | | | | | R21 | T18 | B1 | | | |
| GND | | | | | | T10 | T20 | B2 | | | |
| GND | | | | | | T12 | T21 | B38 | | | |
| GND | | | | | | T14 | U12 | B39 | | | |
| GND | | | | | | T18 | U13 | C3 | | | |
| GND | | | | | | T20 | U15 | C37 | | | |
| GND | | | | | | T22 | U18 | G19 | | | |
| GND | | | | | | U11 | U20 | H32 | | | |
| GND | | | | | | U13 | U21 | H8 | | | |
| GND | | | | | | U15 | V14 | J21 | | | |
| GND | | | | | | U17 | V16 | K10 | | | |
| GND | | | | | | U19 | V17 | K20 | | | |
| GND | | | | | | U21 | V19 | K22 | | | |
| GND | | | | | | V12 | W13 | K30 | | | |
| GND | | | | | | V14 | W15 | N1 | | | |
| GND | | | | | | V16 | W18 | N39 | | | |
| GND | | | | | | V18 | W20 | R15 | | | |
| GND | | | | | | V20 | Y14 | R17 | | | |

*Table 5–1. Pin List for the Stratix EP1S40 Device (Part 52 of 71)*

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| GND | | | | | | W11 | Y16 | R19 | | | |
| GND | | | | | | W13 | Y17 | R23 | | | |
| GND | | | | | | W15 | Y19 | R25 | | | |
| GND | | | | | | W17 | | T16 | | | |
| GND | | | | | | W19 | | T18 | | | |
| GND | | | | | | W21 | | T20 | | | |
| GND | | | | | | Y1 | | T22 | | | |
| GND | | | | | | Y12 | | T24 | | | |
| GND | | | | | | Y14 | | U15 | | | |
| GND | | | | | | Y16 | | U17 | | | |
| GND | | | | | | Y18 | | U19 | | | |
| GND | | | | | | Y20 | | U21 | | | |
| GND | | | | | | Y31 | | U23 | | | |
| GND | | | | | | | | U25 | | | |
| GND | | | | | | | | V16 | | | |
| GND | | | | | | | | V18 | | | |
| GND | | | | | | | | V20 | | | |
| GND | | | | | | | | V22 | | | |
| GND | | | | | | | | V24 | | | |
| GND | | | | | | | | W17 | | | |
| GND | | | | | | | | W23 | | | |
| GND | | | | | | | | W25 | | | |

**Table 5–1. Pin List for the Stratix EP1S40 Device (Part 53 of 71)**

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| GND | | | | | | | | W33 | | | |
| GND | | | | | | | | Y10 | | | |
| GND | | | | | | | | Y16 | | | |
| GND | | | | | | | | Y18 | | | |
| GND | | | | | | | | Y22 | | | |
| GND | | | | | | | | Y24 | | | |
| GND | | | | | | | | Y30 | | | |
| No connection | | | | | | AA22 | AG27 | AA12 | | | |
| No connection | | | | | | AB10 | V12 | AA13 | | | |
| No connection | | | | | | AB18 | | AA14 | | | |
| No connection | | | | | | K14 | | AA26 | | | |
| No connection | | | | | | K22 | | AA27 | | | |
| No connection | | | | | | L10 | | AA6 | | | |
| No connection | | | | | | P22 | | AB10 | | | |
| No connection | | | | | | V10 | | AB11 | | | |
| No connection | | | | | | | | AB12 | | | |
| No connection | | | | | | | | AB13 | | | |
| No connection | | | | | | | | AB14 | | | |
| No connection | | | | | | | | AB26 | | | |
| No connection | | | | | | | | AB27 | | | |
| No connection | | | | | | | | AB28 | | | |
| No connection | | | | | | | | AB29 | | | |

*Table 5–1. Pin List for the Stratix EP1S40 Device (Part 54 of 71)*

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **780-Pin FBGA** | **956-Pin BGA** | **1020-Pin FBGA** | **1508-Pin FBGA** | | | |
| No connection | | | | | | | | AB7 | | | |
| No connection | | | | | | | | AC10 | | | |
| No connection | | | | | | | | AC11 | | | |
| No connection | | | | | | | | AC12 | | | |
| No connection | | | | | | | | AC13 | | | |
| No connection | | | | | | | | AC14 | | | |
| No connection | | | | | | | | AC26 | | | |
| No connection | | | | | | | | AC27 | | | |
| No connection | | | | | | | | AC28 | | | |
| No connection | | | | | | | | AC29 | | | |
| No connection | | | | | | | | AC30 | | | |
| No connection | | | | | | | | AC31 | | | |
| No connection | | | | | | | | AC9 | | | |
| No connection | | | | | | | | AD11 | | | |
| No connection | | | | | | | | AD12 | | | |
| No connection | | | | | | | | AD13 | | | |
| No connection | | | | | | | | AD14 | | | |
| No connection | | | | | | | | AD26 | | | |
| No connection | | | | | | | | AD27 | | | |
| No connection | | | | | | | | AD28 | | | |
| No connection | | | | | | | | AD29 | | | |
| No connection | | | | | | | | AE10 | | | |

Table 5–1. Pin List for the Stratix EP1S40 Device (Part 55 of 71)

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | | | |
| No connection | | | | | | | | AE11 | | | |
| No connection | | | | | | | | AE12 | | | |
| No connection | | | | | | | | AE13 | | | |
| No connection | | | | | | | | AE14 | | | |
| No connection | | | | | | | | AE26 | | | |
| No connection | | | | | | | | AE27 | | | |
| No connection | | | | | | | | AE28 | | | |
| No connection | | | | | | | | AE30 | | | |
| No connection | | | | | | | | AE31 | | | |
| No connection | | | | | | | | AE9 | | | |
| No connection | | | | | | | | AF10 | | | |
| No connection | | | | | | | | AF12 | | | |
| No connection | | | | | | | | AF13 | | | |
| No connection | | | | | | | | AF14 | | | |
| No connection | | | | | | | | AF15 | | | |
| No connection | | | | | | | | AF17 | | | |
| No connection | | | | | | | | AF18 | | | |
| No connection | | | | | | | | AF19 | | | |
| No connection | | | | | | | | AF20 | | | |
| No connection | | | | | | | | AF21 | | | |
| No connection | | | | | | | | AF22 | | | |
| No connection | | | | | | | | AF24 | | | |

*Table 5–1. Pin List for the Stratix EP1S40 Device (Part 56 of 71)*

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | | | |
| No connection | | | | | | | | AF25 | | | |
| No connection | | | | | | | | AF26 | | | |
| No connection | | | | | | | | AF27 | | | |
| No connection | | | | | | | | AF28 | | | |
| No connection | | | | | | | | AF30 | | | |
| No connection | | | | | | | | AF31 | | | |
| No connection | | | | | | | | AF9 | | | |
| No connection | | | | | | | | AG12 | | | |
| No connection | | | | | | | | AG13 | | | |
| No connection | | | | | | | | AG14 | | | |
| No connection | | | | | | | | AG15 | | | |
| No connection | | | | | | | | AG16 | | | |
| No connection | | | | | | | | AG17 | | | |
| No connection | | | | | | | | AG18 | | | |
| No connection | | | | | | | | AG19 | | | |
| No connection | | | | | | | | AG22 | | | |
| No connection | | | | | | | | AG23 | | | |
| No connection | | | | | | | | AG24 | | | |
| No connection | | | | | | | | AG25 | | | |
| No connection | | | | | | | | AG26 | | | |
| No connection | | | | | | | | AG27 | | | |
| No connection | | | | | | | | AG28 | | | |

*Table 5–1. Pin List for the Stratix EP1S40 Device (Part 57 of 71)*

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| No connection | | | | | | | | AH12 | | | |
| No connection | | | | | | | | AH13 | | | |
| No connection | | | | | | | | AH14 | | | |
| No connection | | | | | | | | AH15 | | | |
| No connection | | | | | | | | AH16 | | | |
| No connection | | | | | | | | AH17 | | | |
| No connection | | | | | | | | AH18 | | | |
| No connection | | | | | | | | AH22 | | | |
| No connection | | | | | | | | AH25 | | | |
| No connection | | | | | | | | AH26 | | | |
| No connection | | | | | | | | AH27 | | | |
| No connection | | | | | | | | AH28 | | | |
| No connection | | | | | | | | AH29 | | | |
| No connection | | | | | | | | AJ11 | | | |
| No connection | | | | | | | | AJ16 | | | |
| No connection | | | | | | | | AJ17 | | | |
| No connection | | | | | | | | AJ18 | | | |
| No connection | | | | | | | | AJ22 | | | |
| No connection | | | | | | | | AJ24 | | | |
| No connection | | | | | | | | AJ25 | | | |
| No connection | | | | | | | | AK11 | | | |
| No connection | | | | | | | | AK12 | | | |

Table 5–1. Pin List for the Stratix EP1S40 Device (Part 58 of 71)

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **780-Pin FBGA** | **956-Pin BGA** | **1020-Pin FBGA** | **1508-Pin FBGA** | **DQS for x16** | **DQS for x32** | **DIFFIO Speed** *Note (1)* |
| No connection | | | | | | | | AK13 | | | |
| No connection | | | | | | | | AK14 | | | |
| No connection | | | | | | | | AK15 | | | |
| No connection | | | | | | | | AK16 | | | |
| No connection | | | | | | | | AK18 | | | |
| No connection | | | | | | | | AK23 | | | |
| No connection | | | | | | | | AK24 | | | |
| No connection | | | | | | | | AK25 | | | |
| No connection | | | | | | | | AK26 | | | |
| No connection | | | | | | | | AK27 | | | |
| No connection | | | | | | | | AK28 | | | |
| No connection | | | | | | | | AK29 | | | |
| No connection | | | | | | | | AL10 | | | |
| No connection | | | | | | | | AL11 | | | |
| No connection | | | | | | | | AL12 | | | |
| No connection | | | | | | | | AL13 | | | |
| No connection | | | | | | | | AL14 | | | |
| No connection | | | | | | | | AL15 | | | |
| No connection | | | | | | | | AL16 | | | |
| No connection | | | | | | | | AL22 | | | |
| No connection | | | | | | | | AL24 | | | |
| No connection | | | | | | | | AL26 | | | |

**Table 5–1. Pin List for the Stratix EP1S40 Device (Part 59 of 71)**

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| No connection | | | | | | | | AL27 | | | |
| No connection | | | | | | | | AL28 | | | |
| No connection | | | | | | | | AL29 | | | |
| No connection | | | | | | | | AL30 | | | |
| No connection | | | | | | | | AL34 | | | |
| No connection | | | | | | | | AL35 | | | |
| No connection | | | | | | | | AL5 | | | |
| No connection | | | | | | | | AL6 | | | |
| No connection | | | | | | | | AM11 | | | |
| No connection | | | | | | | | AM12 | | | |
| No connection | | | | | | | | AM13 | | | |
| No connection | | | | | | | | AM14 | | | |
| No connection | | | | | | | | AM15 | | | |
| No connection | | | | | | | | AM16 | | | |
| No connection | | | | | | | | AM17 | | | |
| No connection | | | | | | | | AM18 | | | |
| No connection | | | | | | | | AM28 | | | |
| No connection | | | | | | | | AM29 | | | |
| No connection | | | | | | | | AM3 | | | |
| No connection | | | | | | | | AM31 | | | |
| No connection | | | | | | | | AM34 | | | |
| No connection | | | | | | | | AM35 | | | |

**Table 5–1. Pin List for the Stratix EP1S40 Device (Part 60 of 71)**

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | | | |
| No connection | | | | | | | | AM36 | | | |
| No connection | | | | | | | | AM37 | | | |
| No connection | | | | | | | | AM4 | | | |
| No connection | | | | | | | | AM5 | | | |
| No connection | | | | | | | | AM6 | | | |
| No connection | | | | | | | | AM9 | | | |
| No connection | | | | | | | | AN15 | | | |
| No connection | | | | | | | | AN3 | | | |
| No connection | | | | | | | | AN34 | | | |
| No connection | | | | | | | | AN35 | | | |
| No connection | | | | | | | | AN36 | | | |
| No connection | | | | | | | | AN37 | | | |
| No connection | | | | | | | | AN4 | | | |
| No connection | | | | | | | | AN5 | | | |
| No connection | | | | | | | | AN6 | | | |
| No connection | | | | | | | | AP3 | | | |
| No connection | | | | | | | | AP34 | | | |
| No connection | | | | | | | | AP35 | | | |
| No connection | | | | | | | | AP36 | | | |
| No connection | | | | | | | | AP37 | | | |
| No connection | | | | | | | | AP4 | | | |
| No connection | | | | | | | | AP5 | | | |

**Table 5–1. Pin List for the Stratix EP1S40 Device (Part 61 of 71)**

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| No connection | | | | | | | | AP6 | | | |
| No connection | | | | | | | | AR1 | | | |
| No connection | | | | | | | | AR2 | | | |
| No connection | | | | | | | | AR3 | | | |
| No connection | | | | | | | | AR36 | | | |
| No connection | | | | | | | | AR37 | | | |
| No connection | | | | | | | | AR38 | | | |
| No connection | | | | | | | | AR39 | | | |
| No connection | | | | | | | | AR4 | | | |
| No connection | | | | | | | | AT1 | | | |
| No connection | | | | | | | | AT2 | | | |
| No connection | | | | | | | | AT3 | | | |
| No connection | | | | | | | | AT36 | | | |
| No connection | | | | | | | | AT37 | | | |
| No connection | | | | | | | | AT38 | | | |
| No connection | | | | | | | | AT39 | | | |
| No connection | | | | | | | | AT4 | | | |
| No connection | | | | | | | | AU2 | | | |
| No connection | | | | | | | | AU38 | | | |
| No connection | | | | | | | | AV3 | | | |
| No connection | | | | | | | | AV37 | | | |
| No connection | | | | | | | | B3 | | | |

Table 5–1. Pin List for the Stratix EP1S40 Device (Part 62 of 71)

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | | | |
| No connection | | | | | | | | B37 | | | |
| No connection | | | | | | | | C2 | | | |
| No connection | | | | | | | | C38 | | | |
| No connection | | | | | | | | D1 | | | |
| No connection | | | | | | | | D2 | | | |
| No connection | | | | | | | | D3 | | | |
| No connection | | | | | | | | D36 | | | |
| No connection | | | | | | | | D37 | | | |
| No connection | | | | | | | | D38 | | | |
| No connection | | | | | | | | D39 | | | |
| No connection | | | | | | | | D4 | | | |
| No connection | | | | | | | | E1 | | | |
| No connection | | | | | | | | E2 | | | |
| No connection | | | | | | | | E3 | | | |
| No connection | | | | | | | | E36 | | | |
| No connection | | | | | | | | E37 | | | |
| No connection | | | | | | | | E38 | | | |
| No connection | | | | | | | | E39 | | | |
| No connection | | | | | | | | E4 | | | |
| No connection | | | | | | | | F1 | | | |
| No connection | | | | | | | | F2 | | | |
| No connection | | | | | | | | F3 | | | |

**Table 5–1. Pin List for the Stratix EP1S40 Device (Part 63 of 71)**

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| No connection | | | | | | | | F34 | | | |
| No connection | | | | | | | | F35 | | | |
| No connection | | | | | | | | F36 | | | |
| No connection | | | | | | | | F37 | | | |
| No connection | | | | | | | | F38 | | | |
| No connection | | | | | | | | F39 | | | |
| No connection | | | | | | | | F4 | | | |
| No connection | | | | | | | | F5 | | | |
| No connection | | | | | | | | F6 | | | |
| No connection | | | | | | | | G3 | | | |
| No connection | | | | | | | | G34 | | | |
| No connection | | | | | | | | G35 | | | |
| No connection | | | | | | | | G36 | | | |
| No connection | | | | | | | | G37 | | | |
| No connection | | | | | | | | G4 | | | |
| No connection | | | | | | | | G5 | | | |
| No connection | | | | | | | | G6 | | | |
| No connection | | | | | | | | H11 | | | |
| No connection | | | | | | | | H12 | | | |
| No connection | | | | | | | | H13 | | | |
| No connection | | | | | | | | H14 | | | |
| No connection | | | | | | | | H15 | | | |

*Table 5–1. Pin List for the Stratix EP1S40 Device (Part 64 of 71)*

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | | | |
| No connection | | | | | | | | H16 | | | |
| No connection | | | | | | | | H17 | | | |
| No connection | | | | | | | | H28 | | | |
| No connection | | | | | | | | H29 | | | |
| No connection | | | | | | | | H3 | | | |
| No connection | | | | | | | | H31 | | | |
| No connection | | | | | | | | H34 | | | |
| No connection | | | | | | | | H35 | | | |
| No connection | | | | | | | | H36 | | | |
| No connection | | | | | | | | H37 | | | |
| No connection | | | | | | | | H4 | | | |
| No connection | | | | | | | | H5 | | | |
| No connection | | | | | | | | H6 | | | |
| No connection | | | | | | | | H9 | | | |
| No connection | | | | | | | | J10 | | | |
| No connection | | | | | | | | J11 | | | |
| No connection | | | | | | | | J12 | | | |
| No connection | | | | | | | | J13 | | | |
| No connection | | | | | | | | J14 | | | |
| No connection | | | | | | | | J15 | | | |
| No connection | | | | | | | | J16 | | | |
| No connection | | | | | | | | J18 | | | |

**Table 5–1. Pin List for the Stratix EP1S40 Device (Part 65 of 71)**

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| No connection | | | | | | | | J22 | | | |
| No connection | | | | | | | | J24 | | | |
| No connection | | | | | | | | J26 | | | |
| No connection | | | | | | | | J27 | | | |
| No connection | | | | | | | | J28 | | | |
| No connection | | | | | | | | J29 | | | |
| No connection | | | | | | | | J30 | | | |
| No connection | | | | | | | | J34 | | | |
| No connection | | | | | | | | J35 | | | |
| No connection | | | | | | | | J5 | | | |
| No connection | | | | | | | | J6 | | | |
| No connection | | | | | | | | K11 | | | |
| No connection | | | | | | | | K12 | | | |
| No connection | | | | | | | | K13 | | | |
| No connection | | | | | | | | K14 | | | |
| No connection | | | | | | | | K15 | | | |
| No connection | | | | | | | | K16 | | | |
| No connection | | | | | | | | K17 | | | |
| No connection | | | | | | | | K23 | | | |
| No connection | | | | | | | | K24 | | | |
| No connection | | | | | | | | K25 | | | |
| No connection | | | | | | | | K26 | | | |

Table 5–1. Pin List for the Stratix EP1S40 Device (Part 66 of 71)

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | | | |
| No connection | | | | | | | | K27 | | | |
| No connection | | | | | | | | K28 | | | |
| No connection | | | | | | | | K29 | | | |
| No connection | | | | | | | | L15 | | | |
| No connection | | | | | | | | L16 | | | |
| No connection | | | | | | | | L17 | | | |
| No connection | | | | | | | | L18 | | | |
| No connection | | | | | | | | L24 | | | |
| No connection | | | | | | | | L29 | | | |
| No connection | | | | | | | | M11 | | | |
| No connection | | | | | | | | M12 | | | |
| No connection | | | | | | | | M13 | | | |
| No connection | | | | | | | | M14 | | | |
| No connection | | | | | | | | M15 | | | |
| No connection | | | | | | | | M16 | | | |
| No connection | | | | | | | | M18 | | | |
| No connection | | | | | | | | M22 | | | |
| No connection | | | | | | | | M23 | | | |
| No connection | | | | | | | | M25 | | | |
| No connection | | | | | | | | M26 | | | |
| No connection | | | | | | | | M27 | | | |
| No connection | | | | | | | | M28 | | | |

*Table 5–1. Pin List for the Stratix EP1S40 Device (Part 67 of 71)*

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **780-Pin FBGA** | **956-Pin BGA** | **1020-Pin FBGA** | **1508-Pin FBGA** | **DQS for x16** | **DQS for x32** | **DIFFIO Speed** *Note (1)* |
| No connection | | | | | | | | N12 | | | |
| No connection | | | | | | | | N13 | | | |
| No connection | | | | | | | | N14 | | | |
| No connection | | | | | | | | N15 | | | |
| No connection | | | | | | | | N16 | | | |
| No connection | | | | | | | | N17 | | | |
| No connection | | | | | | | | N18 | | | |
| No connection | | | | | | | | N19 | | | |
| No connection | | | | | | | | N20 | | | |
| No connection | | | | | | | | N22 | | | |
| No connection | | | | | | | | N23 | | | |
| No connection | | | | | | | | N24 | | | |
| No connection | | | | | | | | N25 | | | |
| No connection | | | | | | | | N26 | | | |
| No connection | | | | | | | | N27 | | | |
| No connection | | | | | | | | N28 | | | |
| No connection | | | | | | | | P10 | | | |
| No connection | | | | | | | | P12 | | | |
| No connection | | | | | | | | P13 | | | |
| No connection | | | | | | | | P14 | | | |
| No connection | | | | | | | | P15 | | | |
| No connection | | | | | | | | P17 | | | |

**Table 5–1. Pin List for the Stratix EP1S40 Device (Part 68 of 71)**

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | | | |
| No connection | | | | | | | | P18 | | | |
| No connection | | | | | | | | P19 | | | |
| No connection | | | | | | | | P20 | | | |
| No connection | | | | | | | | P22 | | | |
| No connection | | | | | | | | P24 | | | |
| No connection | | | | | | | | P26 | | | |
| No connection | | | | | | | | P27 | | | |
| No connection | | | | | | | | P28 | | | |
| No connection | | | | | | | | P30 | | | |
| No connection | | | | | | | | P31 | | | |
| No connection | | | | | | | | P9 | | | |
| No connection | | | | | | | | R10 | | | |
| No connection | | | | | | | | R12 | | | |
| No connection | | | | | | | | R13 | | | |
| No connection | | | | | | | | R14 | | | |
| No connection | | | | | | | | R26 | | | |
| No connection | | | | | | | | R27 | | | |
| No connection | | | | | | | | R28 | | | |
| No connection | | | | | | | | R29 | | | |
| No connection | | | | | | | | R30 | | | |
| No connection | | | | | | | | R31 | | | |
| No connection | | | | | | | | R9 | | | |

*Table 5–1. Pin List for the Stratix EP1S40 Device (Part 69 of 71)*

| Device | | | | | Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| No connection | | | | | | | | T11 | | | |
| No connection | | | | | | | | T12 | | | |
| No connection | | | | | | | | T13 | | | |
| No connection | | | | | | | | T14 | | | |
| No connection | | | | | | | | T26 | | | |
| No connection | | | | | | | | T27 | | | |
| No connection | | | | | | | | T28 | | | |
| No connection | | | | | | | | T29 | | | |
| No connection | | | | | | | | U10 | | | |
| No connection | | | | | | | | U11 | | | |
| No connection | | | | | | | | U12 | | | |
| No connection | | | | | | | | U13 | | | |
| No connection | | | | | | | | U14 | | | |
| No connection | | | | | | | | U26 | | | |
| No connection | | | | | | | | U27 | | | |
| No connection | | | | | | | | U28 | | | |
| No connection | | | | | | | | U29 | | | |
| No connection | | | | | | | | U30 | | | |
| No connection | | | | | | | | U31 | | | |
| No connection | | | | | | | | U9 | | | |
| No connection | | | | | | | | V10 | | | |
| No connection | | | | | | | | V11 | | | |

*Table 5–1. Pin List for the Stratix EP1S40 Device (Part 70 of 71)*

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **780-Pin FBGA** | **956-Pin BGA** | **1020-Pin FBGA** | **1508-Pin FBGA** | | | |
| No connection | | | | | | | | V12 | | | |
| No connection | | | | | | | | V13 | | | |
| No connection | | | | | | | | V14 | | | |
| No connection | | | | | | | | V26 | | | |
| No connection | | | | | | | | V27 | | | |
| No connection | | | | | | | | V28 | | | |
| No connection | | | | | | | | V29 | | | |
| No connection | | | | | | | | V30 | | | |
| No connection | | | | | | | | V33 | | | |
| No connection | | | | | | | | V9 | | | |
| No connection | | | | | | | | W13 | | | |
| No connection | | | | | | | | W14 | | | |
| No connection | | | | | | | | W26 | | | |
| No connection | | | | | | | | W27 | | | |
| No connection | | | | | | | | W28 | | | |
| No connection | | | | | | | | W29 | | | |
| No connection | | | | | | | | W30 | | | |
| No connection | | | | | | | | W34 | | | |
| No connection | | | | | | | | Y13 | | | |
| No connection | | | | | | | | Y14 | | | |
| No connection | | | | | | | | Y26 | | | |

**Table 5–1. Pin List for the Stratix EP1S40 Device (Part 71 of 71)**

| Device | | | | | Package | | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 780-Pin FBGA | 956-Pin BGA | 1020-Pin FBGA | 1508-Pin FBGA | | | |
| No connection | | | | | | | | Y27 | | | |

*Note to Table 5–1:*

(1) The wire bond and flip-chip packages have different data rates for the high speed differential I/O channels. Table 5–2 shows the data rates as supported for each package.

**Table 5–2. High Speed Differential I/O Channel Data Rates**

| Package | Package Type | High Speed Differential I/O Channel Performance (DIFFIO Speed) | | Units |
|---|---|---|---|---|
| | | High | Low | |
| 780-pin FineLine BGA | flip chip | 840 | N/A | Mbps |
| 956-pin BGA | flip chip | 840 | N/A | Mbps |
| 1020-pin FineLine BGA | flip chip | 840 | 462 | Mbps |
| 1508-pin FineLine BGA | flip chip | 840 | 462 | Mbps |

## Pin Definitions

Table 5–3 shows pin definitions for the EP1S40 device.

*Table 5–3. Pin Definitions for the EP1S40 Device (Part 1 of 5)*

| Pin Name | Pin Type (1st, 2nd, & 3rd Function) | Pin Description |
|---|---|---|
| **Supply and Reference Pins** | | |
| VREF[1..4]B[1..8] | Input | Input reference voltage for each I/O bank. If a bank is used for a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for that bank. All of the VREF pins within a bank are shorted together. Each VREF pin can support up to 20 inputs on each side. If VREF pins are not used, designers should connect them to either VCC or Gnd. |
| VCCIO[1..8] | Power | These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards. VCCIO also supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5-V, 1.8-V, 2.5-V, 3.3-V PCI, and 3.3-V PCI-X I/O standards. |
| VCCINT | Power | These are internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVDS, LVPECL, 3.3-V PCML, HyperTransportô technology, differential HSTL, GTL, GTL+, HSTL, SSTL, CTT, and 3.3-V AGP I/O standards. |
| VCC_PLL5_OUTA | Power | External clock output buffer power for PLL5 clock outputs PLL5_OUT[1..0]. The designer must connect this pin to the VCCIO of bank 9. |
| VCC_PLL5_OUTB | Power | External clock output buffer power for PLL5 clock outputs PLL5_OUT[3..2]. The designer must connect this pin to the VCCIO of bank 10. |
| VCC_PLL6_OUTA | Power | External clock output buffer power for PLL6 clock outputs PLL6_OUT[1..0]. The designer must connect this pin to the VCCIO of bank 11. |
| VCC_PLL6_OUTB | Power | External clock output buffer power for PLL6 clock outputs PLL6_OUT[3..2]. The designer must connect this pin to the VCCIO of bank 12. |
| VCCA_PLL[1..12] | Power | Analog power for PLLs[1..12]. The designer must connect this pin to 1.5 V, even if the PLL is not used. |
| GNDA_PLL[1..12] | Ground | Analog ground for PLLs[1..12]. The designer can connect this pin to the GND plane on the board. |
| VCCG_PLL[1..12] | Power | Guard ring power for PLLs[1..12]. The designer must connect this pin to 1.5 V, even if the PLL is not used. |
| GNDG_PLL[1..12] | Ground | Guard ring ground for PLLs[1..12]. The designer can connect this pin to the GND plane on the board. |

*Table 5–3. Pin Definitions for the EP1S40 Device (Part 2 of 5)*

| Pin Name | Pin Type (1st, 2nd, & 3rd Function) | Pin Description |
|---|---|---|
| **Dedicated & Configuration/JTAG Pins** | | |
| CONF_DONE | Bidirectional (open-drain) | This is a dedicated configuration status pin; it is not available as a user I/O pin. |
| nSTATUS | Bidirectional (open-drain) | This is a dedicated configuration status pin; it is not available as a user I/O pin. |
| nCONFIG | Input | Dedicated configuration control input. A low transition resets the target device; a low-to-high transition begins configuration. All I/O pins tri-state when nCONFIG is driven low. |
| DCLK | Input | Clock input used to clock configuration data from an external source into the Stratix device. This is a dedicated pin used for configuration. |
| nIO_PULLUP | Input | IF nIO_PULLUP is driven high during configuration, the weak pull-ups on all user I/O pins are disabled. If driven low, the weak pull-ups are enabled during configuration. nIO_PULLUP can be pulled up to either 1.5, 1.8, 2.5, or 3.3 V. |
| PORSEL | Input | Dedicated input pin used to select POR delay times of 2 ms or 100 ms during powerup. When PORSEL is connected to ground, the POR time is 100 ms. When PORSEL is connected to 3.3 V, the POR time is 2 ms. |
| VCCSEL | Input | VCCSEL is used to select which input buffer is used on all configuration pins. VCCSEL will control whether the 3.3-/2.5-V input buffer or the 1.8-/1.5-V input buffer is used. A "0" means 3.3/2.5 V and a "1" means 1.8-/1.5 V. At powerup, VCCSEL accepts 3.3V and 2.5V TTL Levels. VCCSEL affects the following pins: TDI, TMS, TCK, TRST, MSEL0, MSEL1, MSEL2, nCONFIG, nCE, DCLK, CONF_DONE, nSTATUS, and PLL_ENA. |
| nCE | Input | Active-low chip enables. Dedicated chip enable input used to detect which device is active in a chain of devices. When nCE is low, the device is enabled. When nCE is high, the device is disabled. |
| nCEO | Output | Output that drives low when device configuration is complete. During multi-device configuration, this pin feeds a subsequent deviceís nCE pin. |
| TMS | Input | This is a dedicated JTAG input pin. |
| TDI | Input | This is a dedicated JTAG input pin. |
| TCK | Input | This is a dedicated JTAG input pin. |

*Table 5–3. Pin Definitions for the EP1S40 Device (Part 3 of 5)*

| Pin Name | Pin Type (1st, 2nd, & 3rd Function) | Pin Description |
|---|---|---|
| TDO | Output | This is a dedicated JTAG input pin. |
| TRST | Input | This is a dedicated JTAG input pin. Active low input, used to asynchronously reset the JTAG boundary scan circuit. |
| MSEL[2..0] | Input | Dedicated mode select control pins that set the configuration mode for the device. |
| TEMPDIODEp | Input | Pin used in conjunction with the temperature sensing diode (bias-high input) inside the Stratix device. If the temperature sensing diode is not used then connect this pin to GND. |
| TEMPDIODEn | Input | Pin used in conjunction with the temperature sensing diode (bias-low input) inside the Stratix device. If the temperature sensing diode is not used then connect this pin to GND. |
| **Clock and PLL Pins** | | |
| PLL_ENA | Input | Dedicated input pin that drives the optional pllena port of all or a set of PLLs. If a PLL uses the pllena port, drive the PLL_ENA pin low to reset all PLLs including the counters to their default state. If VCCSEL = 0, then you must drive the PLL_ENA with a 3.3/2.5 V signal to enable the PLLs. If VCCSEL = 1, connect PLL_ENA to 1.8/1.5 V to enable the PLLs. |
| FCLK[7..0] | Bidirectional | Dedicated fast regional clock pins. FCLK pins can also be used as type input, output, or as bidirectional pins. |
| FPLL[10..7]CLKp | Input | Dedicated global clock inputs for fast PLLs (PLLs 7 through 10). |
| FPLL[10..7]CLKn | Input | Dedicated negative terminal associated with FPLL[10..7]CLKp pins. |
| CLK[15..0]p | Input | Dedicated global clock inputs 0 to 15. |
| CLK[15..0]n | I/O, Input | Optional negative terminal input for differential global clock input. |
| PLL6_OUT[3..0]p | I/O, Output | Optional external clock outputs [3..0] from enhanced PLL 6. These pins can be differential (four output pin pairs) or single ended (eight clock outputs from PLL6). |
| PLL6_OUT[3..0]n | I/O, Output | Optional negative terminal for external clock outputs [3..0] from PLL6. If the clock outputs are single ended, then each pair of pins (i.e., PLL6_OUT0p and PLL6_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase. |
| PLL5_OUT[3..0]p | I/O, Output | Optional external clock outputs [3..0] from enhanced PLL 5. These pins can be differential (four output pin pairs) or single ended (eight clock outputs from PLL5). |

*Table 5–3. Pin Definitions for the EP1S40 Device (Part 4 of 5)*

| Pin Name | Pin Type (1st, 2nd, & 3rd Function) | Pin Description |
|---|---|---|
| PLL5_OUT[3..0]n | I/O, Output | Optional negative terminal for external clock outputs [3..0] from PLL 5. If the clock outputs are single ended, then each pair of pins (i.e., PLL5_OUT0p and PLL5_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase. |
| **Optional/Dual-Purpose Pins** | | |
| DATA0 | I/O, Input | Dual-purpose configuration data input pin. Can be used as an I/O pin after configuration is complete. |
| DIFFIO_TX[0..151]n | I/O, Output | This pin can be used as the complementary signal of the differential inputs and outputs. If not used for the differential pair, these pins are regular I/O pins. Pins with an n suffix carry the negative signal for the differential channel. Pins with a p suffix carry the positive signal for the differential channel. |
| CLK6n, PLL12_OUT | I/O, Input (CLK6n), Output (PLL12_OUT) | This pin can be used as an I/O pin, CLK6n, as the PLL12_OUT pin. Only the EP1S40 and larger devices have this pin. |
| CLK13n, PLL11_OUT | I/O, Input (CLK13n), Output (PLL11_OUT) | This pin can be used as an I/O pin, CLK13n, or used as the PLL11_OUT pin. Only the EP1S40 and larger devices have this pin. |
| PLL5_FBp | I/O, Input | External feedback input pin for PLL5. This pin can be used as a user I/O pin if external feedback mode is not used. |
| PLL5_FBn | I/O, Input | Negative terminal input for external feedback input PLL5_FBp |
| PLL6_FBp | I/O, Input | External feedback input pin for PLL6 |
| PLL6_FBn | I/O, Input | Negative terminal input for external feedback input PLL6_FBp |
| INIT_DONE | I/O, Output | This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration. |
| DATA[7..1] | I/O, Input | Dual-purpose configuration input data pins. These pins can be used for configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration. |
| nRS | I/O, Input | Read strobe input pin. This pin can be used as a user I/O pin after configuration. |
| DEV_CLRn | I/O, Input | Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as defined in the users design. |

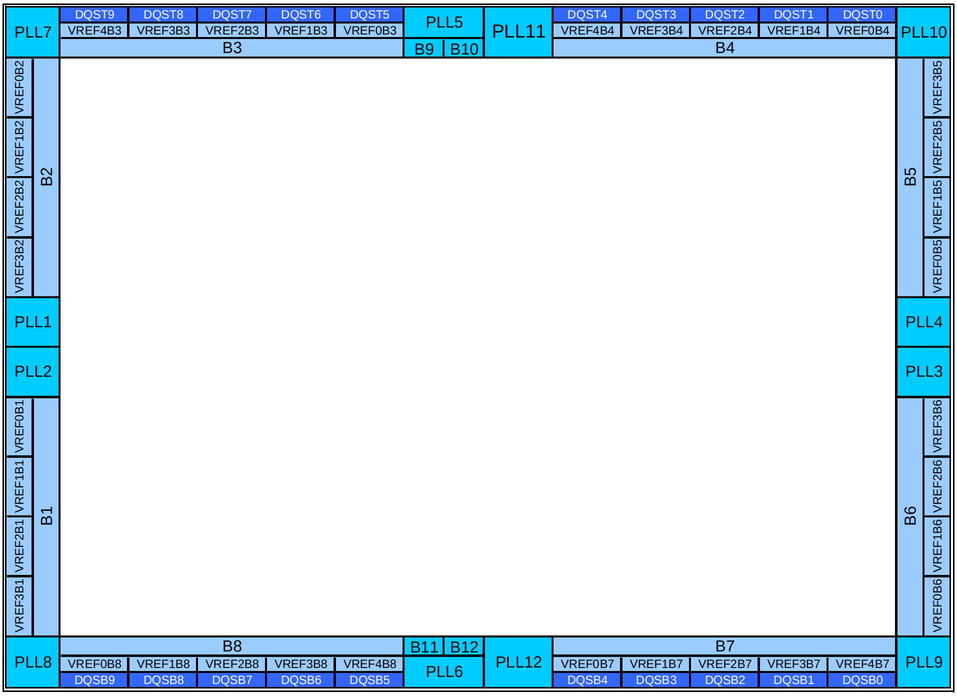
*Table 5–3. Pin Definitions for the EP1S40 Device (Part 5 of 5)*

| Pin Name | Pin Type (1st, 2nd, & 3rd Function) | Pin Description |
|---|---|---|
| DEV_OE | I/O, Input | Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design. |
| CLKUSR | I/O, Input | Optional user-supplied clock input. Synchronizes the initialization of one or more devices. This pin can be used as a user I/O pin after configuration. |
| RDYnBSY | I/O, Output | Ready not busy output. A high output indicates that the target device is ready to accept another data byte. A low output indicates that the target device is not ready to receive another data byte. This pin can be used as a user I/O pin after configuration. |
| nCS,CS | I/O, Input | These are chip-select inputs that enable the Stratix device in the passive parallel asynchronous configuration mode. Drive nCS low and CS high to target a device for configuration. If a design requires an active high enable, use the CS pin and drive the nCS pin low. If a design requires an active low enable, use the nCS pin and drive the CS pin high. Configuration will be paused when either signal is inactive. Hold the nCS and CS pins active during configuration and initialization. The design can use these pins as user I/O pins after configuration. |
| nWS | I/O, Input | Active-low write strobe input to latch a byte of data on the DATA pins. This pin can be used as a user I/O pin after configuration. |
| PGM[2..0] | I/O, Output | These output pins control one of eight pages in the EPC16 configuration device when using remote update or local update configuration modes. When not using remote update or local update configuration modes, these pins are user I/O pins. |
| RUP[8..1] | I/O, Input | Reference pins for banks 8 to 1. The external precision resistors $R_{UP}$ must be connected to the designated RUP pin on that I/O bank. If not required, these pins are regular I/O pins. |
| RDN[8..1] | I/O, Input | Reference pins for banks 8 to 1. The external precision resistors RDN must be connected to the designated RDN pin on that I/O bank. If not required, these pins are regular I/O pins. |
| RUnLU | I/O, Input | Input control pin to select remote update or local update modes. If MSEL2 = 1, this is a input control pin to select remote update (RUnLU =1) or local update (RUnLU =0) modes. If MSEL2 = 0, the RUnLU pin is a user I/O pin. |

## PLL & Bank Diagram

Figure 5–1 shows the PLL and bank locations for the EP1S40 device.

*Figure 5–1. PLL and Bank Diagram* Notes (1), (2)



*Notes for Figure 5–1:*

(1) This is a top view of the silicon die. For flip chip packages the die is mounted upside down in the package.

(2) This is a pictoral representation only, to give an idea of placement on the device. Refer to the pinlist and the Quartus II software software for exact locations.

## Fast PLL to High-Speed I/O Connections

Table 5–4 shows the number of shows the number of high-speed differential I/O channels that can be driven by each Fast PLL for the EP1S40 device.

*Table 5–4. Fast PLL Connections for the EP1S40 Device (Part 1 of 2)*

| Device | Pin Count | FAST PLL Source Location | Number of Rx Channels *(1) (5)* | Number of Tx Channels *(2) (5)* | Number of Overlapped Rx Channels *(3) (5)* | Number of Overlapped Tx Channels *(4) (5)* |
|---|---|---|---|---|---|---|
| EP1S40 | 780 | PLL1 | 17/0 | 18/0 | | |
| | | PLL2 | 16/0 | 16/0 | | |
| | | PLL3 | 16/0 | 16/0 | | |
| | | PLL4 | 17/0 | 18/0 | | |
| | 956 | PLL1 | 20/0 | 18/0 | 18/0 | 18/0 |
| | | PLL2 | 20/0 | 17/0 | 17/0 | 17/0 |
| | | PLL3 | 20/0 | 17/0 | 17/0 | 17/0 |
| | | PLL4 | 20/0 | 18/0 | 18/0 | 18/0 |
| | | PLL7 | 18/0 | 20/0 | 18/0 | 18/0 |
| | | PLL8 | 17/0 | 20/0 | 17/0 | 17/0 |
| | | PLL9 | 17/0 | 20/0 | 17/0 | 17/0 |
| | | PLL10 | 18/0 | 20/0 | 18/0 | 18/0 |
| | 1020 | PLL1 | 20/0 | 18/2 | 18/0 | 18/0 |
| | | PLL2 | 20/0 | 17/3 | 17/0 | 17/0 |
| | | PLL3 | 20/0 | 17/3 | 17/0 | 17/0 |
| | | PLL4 | 20/0 | 18/2 | 18/0 | 18/0 |
| | | PLL7 | 18/2 | 20/0 | 18/0 | 18/0 |
| | | PLL8 | 17/3 | 20/0 | 17/0 | 17/0 |
| | | PLL9 | 17/3 | 20/0 | 17/0 | 17/0 |
| | | PLL10 | 18/2 | 20/0 | 18/0 | 18/0 |

*Table 5–4. Fast PLL Connections for the EP1S40 Device (Part 2 of 2)*

| Device | Pin Count | FAST PLL Source Location | Number of Rx Channels *(1) (5)* | Number of Tx Channels *(2) (5)* | Number of Overlapped Rx Channels *(3) (5)* | Number of Overlapped Tx Channels *(4) (5)* |
|---|---|---|---|---|---|---|
| EP1S40 | 1508 | PLL1 | 20/0 | 20 | 18/0 | 18/0 |
| | | PLL2 | 20/0 | 20 | 17/0 | 17/0 |
| | | PLL3 | 20/0 | 20 | 17/0 | 17/0 |
| | | PLL4 | 20/0 | 20 | 18/0 | 18/0 |
| | | PLL7 | 18/2 | 20/0 | 18/0 | 18/0 |
| | | PLL8 | 17/3 | 20/0 | 17/0 | 17/0 |
| | | PLL9 | 17/3 | 20/0 | 17/0 | 17/0 |
| | | PLL10 | 18/2 | 20/0 | 18/0 | 18/0 |

*Notes for Table 5–4:*

(1) This is the total number of Rx channels that the PLL listed in the "FAST PLL Source location" column can drive.

(2) This is the total number of Tx channels that the PLL listed in the "FAST PLL Source location" column can drive.

(3) This is the number of Rx channels that can be driven by the PLL listed in the "FAST PLL Source location" that could alternatively be driven by the other adjacent FAST PLL.

(4) This is the number of Tx channels that can be driven by the PLL listed in the "FAST PLL Source location" that could alternatively be driven by the other adjacent FAST PLL.

(5) The counts are reported in the format of (high speed channels)/(low speed channels).

# 6. Stratix EP1S60 Device Pin Information

S5V3006-1.0

## Introduction

The following tables contain pin information for the Stratix EP1S60 device, organized into the following sections:

# Pin List

Table 6–1 shows the complete pin list for the EP1S60 device:

*Table 6–1. Pin List for the Stratix EP1S60 Device (Part 1 of 78)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **956-Pin BGA** | **1020-Pin FineLine BGA** | **1508-Pin FineLine BGA** | **DQS for x16** | **DQS for x32** | **DIFFIO Speed** *Note (1)* |
| VCCINT | | | | | VCC | VCC | VCC | | | |
| VCCA_PLL7 | | | | | L23 | D31 | J31 | | | |
| GND | | | | | GND | GND | GND | | | |
| GNDA_PLL7 | | | | | M23 | D32 | K31 | | | |
| VCCG_PLL7 | | | | | J23 | D30 | L30 | | | |
| GNDG_PLL7 | | | | | K23 | E30 | L31 | | | |
| FPLL7CLKp | | | B2 | VREF0B2 | E31 | L29 | J38 | | | |
| FPLL7CLKn | | | B2 | VREF0B2 | D31 | L28 | J39 | | | |
| IO | | | B2 | VREF0B2 | | | N30 | | | |
| IO | | | B2 | VREF0B2 | | | N31 | | | |
| IO | DIFFIO_RX57p | | B2 | VREF0B2 | | | F36 | | | LOW |
| IO | DIFFIO_RX57n | | B2 | VREF0B2 | | | F37 | | | LOW |
| IO | DIFFIO_TX57p | | B2 | VREF0B2 | K24 | G25 | M30 | | | HIGH |
| IO | DIFFIO_TX57n | | B2 | VREF0B2 | J24 | G26 | M31 | | | HIGH |
| IO | DIFFIO_RX56p | | B2 | VREF0B2 | | | D39 | | | LOW |
| IO | DIFFIO_RX56n | | B2 | VREF0B2 | | | D38 | | | LOW |
| IO | DIFFIO_TX56p | | B2 | VREF0B2 | K25 | G28 | J32 | | | HIGH |
| IO | DIFFIO_TX56n | | B2 | VREF0B2 | J25 | G27 | J33 | | | HIGH |
| IO | DIFFIO_RX55p | | B2 | VREF0B2 | | | G36 | | | LOW |
| IO | DIFFIO_RX55n | | B2 | VREF0B2 | | | G37 | | | LOW |

**Table 6–1. Pin List for the Stratix EP1S60 Device (Part 2 of 78)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_TX55p | | B2 | VREF0B2 | H24 | H28 | K32 | | | HIGH |
| IO | DIFFIO_TX55n | | B2 | VREF0B2 | G24 | H27 | K33 | | | HIGH |
| IO | DIFFIO_RX54p | | B2 | VREF0B2 | | | E38 | | | LOW |
| IO | DIFFIO_RX54n | | B2 | VREF0B2 | | | E39 | | | LOW |
| IO | DIFFIO_TX54p | | B2 | VREF0B2 | H25 | J27 | L33 | | | HIGH |
| IO | DIFFIO_TX54n | | B2 | VREF0B2 | G25 | J28 | L32 | | | HIGH |
| VREF0B2 | | | B2 | VREF0B2 | L22 | F27 | M29 | | | |
| IO | DIFFIO_RX53p | | B2 | VREF0B2 | | | F38 | | | LOW |
| IO | DIFFIO_RX53n | | B2 | VREF0B2 | | | F39 | | | LOW |
| IO | DIFFIO_TX53p | | B2 | VREF0B2 | K26 | H25 | M32 | | | HIGH |
| IO | DIFFIO_TX53n | | B2 | VREF0B2 | L26 | H26 | M33 | | | HIGH |
| IO | DIFFIO_RX52p | | B2 | VREF0B2 | | | H37 | | | LOW |
| IO | DIFFIO_RX52n | | B2 | VREF0B2 | | | H36 | | | LOW |
| IO | DIFFIO_TX52p | | B2 | VREF0B2 | J26 | J25 | N32 | | | HIGH |
| IO | DIFFIO_TX52n | | B2 | VREF0B2 | H26 | J26 | N33 | | | HIGH |
| IO | DIFFIO_RX51p | | B2 | VREF0B2 | | E29 | G39 | | | LOW |
| IO | DIFFIO_RX51n | | B2 | VREF0B2 | | F28 | G38 | | | LOW |
| IO | DIFFIO_TX51p | | B2 | VREF0B2 | G26 | K28 | K34 | | | HIGH |
| IO | DIFFIO_TX51n | | B2 | VREF0B2 | F26 | K27 | K35 | | | HIGH |
| IO | DIFFIO_RX50p | | B2 | VREF0B2 | | E32 | H39 | | | LOW |
| IO | DIFFIO_RX50n | | B2 | VREF0B2 | | E31 | H38 | | | LOW |
| IO | DIFFIO_TX50p | | B2 | VREF0B2 | F27 | K26 | L35 | | | HIGH |

*Table 6–1. Pin List for the Stratix EP1S60 Device (Part 3 of 78)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **956-Pin BGA** | **1020-Pin FineLine BGA** | **1508-Pin FineLine BGA** | **DQS for x16** | **DQS for x32** | **DIFFIO Speed** *Note (1)* |
| IO | DIFFIO_TX50n | | B2 | VREF0B2 | G27 | K25 | L34 | | | HIGH |
| IO | DIFFIO_RX49p | | B2 | VREF0B2 | F28 | F29 | K36 | | | HIGH |
| IO | DIFFIO_RX49n | | B2 | VREF0B2 | G28 | F30 | K37 | | | HIGH |
| IO | DIFFIO_TX49p | | B2 | VREF0B2 | H27 | L27 | M34 | | | HIGH |
| IO | DIFFIO_TX49n | | B2 | VREF0B2 | J27 | L26 | M35 | | | HIGH |
| IO | DIFFIO_RX48p | | B2 | VREF1B2 | J28 | F31 | J36 | | | HIGH |
| IO | DIFFIO_RX48n | | B2 | VREF1B2 | H28 | F32 | J37 | | | HIGH |
| IO | DIFFIO_TX48p | | B2 | VREF1B2 | K27 | M26 | N34 | | | HIGH |
| IO | DIFFIO_TX48n | | B2 | VREF1B2 | L27 | M27 | N35 | | | HIGH |
| IO | DIFFIO_RX47p | | B2 | VREF1B2 | D29 | G29 | L37 | | | HIGH |
| IO | DIFFIO_RX47n | | B2 | VREF1B2 | E29 | G30 | L36 | | | HIGH |
| IO | DIFFIO_TX47p | | B2 | VREF1B2 | L24 | M24 | P32 | | | HIGH |
| IO | DIFFIO_TX47n | | B2 | VREF1B2 | M24 | M25 | P33 | | | HIGH |
| IO | DIFFIO_RX46p | | B2 | VREF1B2 | F29 | H30 | K38 | | | HIGH |
| IO | DIFFIO_RX46n | | B2 | VREF1B2 | G29 | H29 | K39 | | | HIGH |
| IO | DIFFIO_TX46p | | B2 | VREF1B2 | L25 | N24 | P34 | | | HIGH |
| IO | DIFFIO_TX46n | | B2 | VREF1B2 | M25 | N23 | P35 | | | HIGH |
| IO | DIFFIO_RX45p | | B2 | VREF1B2 | H29 | G31 | M36 | | | HIGH |
| IO | DIFFIO_RX45n | | B2 | VREF1B2 | J29 | G32 | M37 | | | HIGH |
| IO | DIFFIO_TX45p | | B2 | VREF1B2 | P24 | N27 | R33 | | | HIGH |
| IO | DIFFIO_TX45n | | B2 | VREF1B2 | N24 | N28 | R32 | | | HIGH |
| IO | DIFFIO_RX44p | | B2 | VREF1B2 | D30 | H31 | L38 | | | HIGH |

**Table 6–1. Pin List for the Stratix EP1S60 Device (Part 4 of 78)**

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | | | |
| IO | DIFFIO_RX44n | | B2 | VREF1B2 | E30 | H32 | L39 | | | HIGH |
| IO | DIFFIO_TX44p | | B2 | VREF1B2 | N25 | P23 | R34 | | | HIGH |
| IO | DIFFIO_TX44n | | B2 | VREF1B2 | P25 | P24 | R35 | | | HIGH |
| VREF1B2 | | | B2 | VREF1B2 | M22 | L25 | N29 | | | |
| IO | DIFFIO_RX43p | | B2 | VREF1B2 | F30 | J29 | M38 | | | HIGH |
| IO | DIFFIO_RX43n | | B2 | VREF1B2 | G30 | J30 | M39 | | | HIGH |
| IO | DIFFIO_TX43p | | B2 | VREF1B2 | M26 | N25 | T33 | | | HIGH |
| IO | DIFFIO_TX43n | | B2 | VREF1B2 | N26 | N26 | T32 | | | HIGH |
| IO | DIFFIO_RX42p | | B2 | VREF1B2 | H30 | K30 | N36 | | | HIGH |
| IO | DIFFIO_RX42n | | B2 | VREF1B2 | J30 | K29 | N37 | | | HIGH |
| IO | DIFFIO_TX42p | | B2 | VREF1B2 | M27 | P28 | T30 | | | HIGH |
| IO | DIFFIO_TX42n | | B2 | VREF1B2 | N27 | P27 | T31 | | | HIGH |
| IO | DIFFIO_RX41p | | B2 | VREF1B2 | F31 | J32 | N38 | | | HIGH |
| IO | DIFFIO_RX41n | | B2 | VREF1B2 | G31 | J31 | P38 | | | HIGH |
| IO | DIFFIO_TX41p | | B2 | VREF1B2 | P27 | R28 | T34 | | | HIGH |
| IO | DIFFIO_TX41n | | B2 | VREF1B2 | R27 | R27 | T35 | | | HIGH |
| IO | DIFFIO_RX40p | | B2 | VREF1B2 | H31 | K31 | P39 | | | HIGH |
| IO | DIFFIO_RX40n | | B2 | VREF1B2 | J31 | L32 | R38 | | | HIGH |
| IO | DIFFIO_TX40p | | B2 | VREF1B2 | R26 | P25 | U35 | | | HIGH |
| IO | DIFFIO_TX40n | | B2 | VREF1B2 | P26 | P26 | U34 | | | HIGH |
| IO | DIFFIO_RX39p/RUP2 | | B2 | VREF1B2 | K28 | M28 | P36 | | | HIGH |
| IO | DIFFIO_RX39n/RDN2 | | B2 | VREF1B2 | K29 | M29 | P37 | | | HIGH |

*Table 6–1. Pin List for the Stratix EP1S60 Device (Part 5 of 78)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_TX39p | | B2 | VREF1B2 | N23 | R23 | U33 | | | HIGH |
| IO | DIFFIO_TX39n | | B2 | VREF1B2 | P23 | R24 | U32 | | | HIGH |
| IO | DIFFIO_RX38p | | B2 | VREF2B2 | M28 | L30 | R36 | | | HIGH |
| IO | DIFFIO_RX38n | | B2 | VREF2B2 | L28 | L31 | R37 | | | HIGH |
| IO | DIFFIO_TX38p | | B2 | VREF2B2 | T25 | R25 | V35 | | | HIGH |
| IO | DIFFIO_TX38n | | B2 | VREF2B2 | R25 | R26 | V34 | | | HIGH |
| IO | DIFFIO_RX37p | | B2 | VREF2B2 | M29 | M31 | T36 | | | HIGH |
| IO | DIFFIO_RX37n | | B2 | VREF2B2 | L29 | M30 | T37 | | | HIGH |
| IO | DIFFIO_TX37p | | B2 | VREF2B2 | | M23 | U31 | | | LOW |
| IO | DIFFIO_TX37n | | B2 | VREF2B2 | | M22 | U30 | | | LOW |
| IO | DIFFIO_RX36p | | B2 | VREF2B2 | P28 | N29 | T39 | | | HIGH |
| IO | DIFFIO_RX36n | | B2 | VREF2B2 | N28 | N30 | T38 | | | HIGH |
| IO | DIFFIO_TX36p | | B2 | VREF2B2 | | N22 | U29 | | | LOW |
| IO | DIFFIO_TX36n | | B2 | VREF2B2 | | P22 | U28 | | | LOW |
| IO | DIFFIO_RX35p | | B2 | VREF2B2 | N29 | N31 | U36 | | | HIGH |
| IO | DIFFIO_RX35n | | B2 | VREF2B2 | P29 | N32 | U37 | | | HIGH |
| IO | DIFFIO_TX35p | | B2 | VREF2B2 | | | V32 | | | LOW |
| IO | DIFFIO_TX35n | | B2 | VREF2B2 | | | V31 | | | LOW |
| IO | DIFFIO_RX34p | | B2 | VREF2B2 | L30 | P29 | U38 | | | HIGH |
| IO | DIFFIO_RX34n | | B2 | VREF2B2 | K30 | P30 | U39 | | | HIGH |
| IO | DIFFIO_TX34p | | B2 | VREF2B2 | | | V29 | | | LOW |
| IO | DIFFIO_TX34n | | B2 | VREF2B2 | | | V30 | | | LOW |

**Table 6–1. Pin List for the Stratix EP1S60 Device (Part 6 of 78)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| VREF2B2 | | | B2 | VREF2B2 | N22 | R21 | P29 | | | |
| IO | DIFFIO_RX33p | | B2 | VREF2B2 | N30 | P31 | V36 | | | HIGH |
| IO | DIFFIO_RX33n | | B2 | VREF2B2 | M30 | P32 | V37 | | | HIGH |
| IO | DIFFIO_TX33p | | B2 | VREF2B2 | | | V33 | | | LOW |
| IO | DIFFIO_TX33n | | B2 | VREF2B2 | | | W34 | | | LOW |
| IO | DIFFIO_RX32p | | B2 | VREF2B2 | L31 | R32 | V38 | | | HIGH |
| IO | DIFFIO_RX32n | | B2 | VREF2B2 | K31 | R31 | V39 | | | HIGH |
| IO | DIFFIO_TX32p | | B2 | VREF2B2 | | | W31 | | | LOW |
| IO | DIFFIO_TX32n | | B2 | VREF2B2 | | | W32 | | | LOW |
| IO | DIFFIO_RX31p | | B2 | VREF2B2 | R30 | R30 | W39 | | | HIGH |
| IO | DIFFIO_RX31n | | B2 | VREF2B2 | P30 | R29 | W38 | | | HIGH |
| IO | DIFFIO_TX31p | | B2 | VREF2B2 | | | W28 | | | LOW |
| IO | DIFFIO_TX31n | | B2 | VREF2B2 | | | W27 | | | LOW |
| IO | DIFFIO_RX30p | | B2 | VREF2B2 | P31 | T32 | W37 | | | HIGH |
| IO | DIFFIO_RX30n | | B2 | VREF2B2 | R31 | T31 | W36 | | | HIGH |
| IO | DIFFIO_TX30p | | B2 | VREF2B2 | | | W29 | | | LOW |
| IO | DIFFIO_TX30n | | B2 | VREF2B2 | | | W30 | | | LOW |
| CLK0n | | | B2 | VREF2B2 | R28 | T30 | Y39 | | | |
| CLK0p | | | B2 | VREF2B2 | R29 | T29 | Y38 | | | |
| IO | CLK1n | | B2 | VREF2B2 | T30 | T28 | Y34 | | | |
| CLK1p | | | B2 | VREF2B2 | T31 | T27 | Y35 | | | |
| VCCINT | | | | | | | | | | |

Table 6–1. Pin List for the Stratix EP1S60 Device (Part 7 of 78)

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| VCCA_PLL1 | | | | | R24 | T25 | AA32 | | | |
| GND | | | | | | | | | | |
| GNDA_PLL1 | | | | | T24 | T26 | Y31 | | | |
| VCCG_PLL1 | | | | | R22 | R22 | Y28 | | | |
| GNDG_PLL1 | | | | | R23 | T22 | Y29 | | | |
| VCCINT | | | | | | | | | | |
| VCCA_PLL2 | | | | | U24 | U25 | AA30 | | | |
| GND | | | | | | | | | | |
| GNDA_PLL2 | | | | | V24 | U26 | AA31 | | | |
| VCCG_PLL2 | | | | | U23 | U24 | AA28 | | | |
| GNDG_PLL2 | | | | | V23 | T24 | AA29 | | | |
| CLK2p | | | B1 | VREF0B1 | T29 | U31 | Y37 | | | |
| CLK2n | | | B1 | VREF0B1 | T28 | U32 | Y36 | | | |
| CLK3p | | | B1 | VREF0B1 | U29 | U29 | AA35 | | | |
| IO | CLK3n | | B1 | VREF0B1 | U28 | U30 | AA34 | | | |
| IO | DIFFIO_RX29p | | B1 | VREF0B1 | U31 | U28 | AA39 | | | HIGH |
| IO | DIFFIO_RX29n | | B1 | VREF0B1 | V31 | U27 | AA38 | | | HIGH |
| IO | DIFFIO_TX29p | | B1 | VREF0B1 | | | AA27 | | | LOW |
| IO | DIFFIO_TX29n | | B1 | VREF0B1 | | | AA26 | | | LOW |
| IO | DIFFIO_RX28p | | B1 | VREF0B1 | AB31 | V32 | AA37 | | | HIGH |
| IO | DIFFIO_RX28n | | B1 | VREF0B1 | AA31 | V31 | AA36 | | | HIGH |
| IO | DIFFIO_TX28p | | B1 | VREF0B1 | | | AB27 | | | LOW |

**Table 6–1. Pin List for the Stratix EP1S60 Device (Part 8 of 78)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_TX28n | | B1 | VREF0B1 | | | AB26 | | | LOW |
| IO | DIFFIO_RX27p | | B1 | VREF0B1 | V30 | V30 | AB38 | | | HIGH |
| IO | DIFFIO_RX27n | | B1 | VREF0B1 | U30 | V29 | AB39 | | | HIGH |
| IO | DIFFIO_TX27p | | B1 | VREF0B1 | | | Y33 | | | LOW |
| IO | DIFFIO_TX27n | | B1 | VREF0B1 | | | AA33 | | | LOW |
| VREF0B1 | | | B1 | VREF0B1 | V22 | V21 | AE29 | | | |
| IO | DIFFIO_RX26p | | B1 | VREF0B1 | W30 | W32 | AB37 | | | HIGH |
| IO | DIFFIO_RX26n | | B1 | VREF0B1 | Y30 | W31 | AB36 | | | HIGH |
| IO | DIFFIO_TX26p | | B1 | VREF0B1 | | | AB33 | | | LOW |
| IO | DIFFIO_TX26n | | B1 | VREF0B1 | | | AB32 | | | LOW |
| IO | DIFFIO_RX25p | | B1 | VREF0B1 | AA30 | W30 | AC39 | | | HIGH |
| IO | DIFFIO_RX25n | | B1 | VREF0B1 | AB30 | W29 | AC38 | | | HIGH |
| IO | DIFFIO_TX25p | | B1 | VREF0B1 | | | AB28 | | | LOW |
| IO | DIFFIO_TX25n | | B1 | VREF0B1 | | | AB29 | | | LOW |
| IO | DIFFIO_RX24p | | B1 | VREF0B1 | V29 | Y32 | AC37 | | | HIGH |
| IO | DIFFIO_RX24n | | B1 | VREF0B1 | W29 | Y31 | AC36 | | | HIGH |
| IO | DIFFIO_TX24p | | B1 | VREF0B1 | | | AB31 | | | LOW |
| IO | DIFFIO_TX24n | | B1 | VREF0B1 | | | AB30 | | | LOW |
| IO | DIFFIO_RX23p | | B1 | VREF0B1 | Y29 | Y30 | AD39 | | | HIGH |
| IO | DIFFIO_RX23n | | B1 | VREF0B1 | AA29 | Y29 | AD38 | | | HIGH |
| IO | DIFFIO_TX23p | | B1 | VREF0B1 | | U22 | AC26 | | | LOW |
| IO | DIFFIO_TX23n | | B1 | VREF0B1 | | V22 | AC27 | | | LOW |

*Table 6–1. Pin List for the Stratix EP1S60 Device (Part 9 of 78)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **956-Pin BGA** | **1020-Pin FineLine BGA** | **1508-Pin FineLine BGA** | **DQS for x16** | **DQS for x32** | **DIFFIO Speed** *Note (1)* |
| IO | DIFFIO_RX22p | | B1 | VREF1B1 | V28 | AA31 | AD37 | | | HIGH |
| IO | DIFFIO_RX22n | | B1 | VREF1B1 | W28 | AA30 | AD36 | | | HIGH |
| IO | DIFFIO_TX22p | | B1 | VREF1B1 | | W21 | AC31 | | | LOW |
| IO | DIFFIO_TX22n | | B1 | VREF1B1 | | W22 | AC30 | | | LOW |
| IO | DIFFIO_RX21p | | B1 | VREF1B1 | Y28 | AB31 | AE37 | | | HIGH |
| IO | DIFFIO_RX21n | | B1 | VREF1B1 | AA28 | AB30 | AE36 | | | HIGH |
| IO | DIFFIO_TX21p | | B1 | VREF1B1 | | Y21 | AC28 | | | LOW |
| IO | DIFFIO_TX21n | | B1 | VREF1B1 | | Y22 | AC29 | | | LOW |
| IO | DIFFIO_RX20p/RUP1 | | B1 | VREF1B1 | AB29 | AA28 | AF37 | | | HIGH |
| IO | DIFFIO_RX20n/RDN1 | | B1 | VREF1B1 | AB28 | AA29 | AF36 | | | HIGH |
| IO | DIFFIO_TX20p | | B1 | VREF1B1 | | AA22 | AD29 | | | LOW |
| IO | DIFFIO_TX20n | | B1 | VREF1B1 | | AB23 | AD28 | | | LOW |
| IO | DIFFIO_RX19p | | B1 | VREF1B1 | AC31 | AB32 | AE38 | | | HIGH |
| IO | DIFFIO_RX19n | | B1 | VREF1B1 | AD31 | AC31 | AF39 | | | HIGH |
| IO | DIFFIO_TX19p | | B1 | VREF1B1 | V25 | V26 | AB34 | | | HIGH |
| IO | DIFFIO_TX19n | | B1 | VREF1B1 | U25 | V25 | AB35 | | | HIGH |
| VREF1B1 | | | B1 | VREF1B1 | W22 | AA23 | AF29 | | | |
| IO | DIFFIO_RX18p | | B1 | VREF1B1 | AE31 | AD32 | AF38 | | | HIGH |
| IO | DIFFIO_RX18n | | B1 | VREF1B1 | AF31 | AD31 | AG38 | | | HIGH |
| IO | DIFFIO_TX18p | | B1 | VREF1B1 | U26 | V28 | AC32 | | | HIGH |
| IO | DIFFIO_TX18n | | B1 | VREF1B1 | T26 | V27 | AC33 | | | HIGH |
| IO | DIFFIO_RX17p | | B1 | VREF1B1 | AC30 | AC29 | AG37 | | | HIGH |

**Table 6–1. Pin List for the Stratix EP1S60 Device (Part 10 of 78)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_RX17n | | B1 | VREF1B1 | AD30 | AC30 | AG36 | | | HIGH |
| IO | DIFFIO_TX17p | | B1 | VREF1B1 | T27 | W25 | AC34 | | | HIGH |
| IO | DIFFIO_TX17n | | B1 | VREF1B1 | U27 | W26 | AC35 | | | HIGH |
| IO | DIFFIO_RX16p | | B1 | VREF1B1 | AF30 | AD30 | AH39 | | | HIGH |
| IO | DIFFIO_RX16n | | B1 | VREF1B1 | AE30 | AD29 | AH38 | | | HIGH |
| IO | DIFFIO_TX16p | | B1 | VREF1B1 | V26 | W27 | AD34 | | | HIGH |
| IO | DIFFIO_TX16n | | B1 | VREF1B1 | W26 | W28 | AD35 | | | HIGH |
| IO | DIFFIO_RX15p | | B1 | VREF1B1 | AG30 | AE32 | AH37 | | | HIGH |
| IO | DIFFIO_RX15n | | B1 | VREF1B1 | AH30 | AE31 | AH36 | | | HIGH |
| IO | DIFFIO_TX15p | | B1 | VREF1B1 | W24 | V24 | AD33 | | | HIGH |
| IO | DIFFIO_TX15n | | B1 | VREF1B1 | Y24 | V23 | AD32 | | | HIGH |
| IO | DIFFIO_RX14p | | B1 | VREF2B1 | AC29 | AE30 | AJ39 | | | HIGH |
| IO | DIFFIO_RX14n | | B1 | VREF2B1 | AD29 | AE29 | AJ38 | | | HIGH |
| IO | DIFFIO_TX14p | | B1 | VREF2B1 | W25 | Y26 | AD31 | | | HIGH |
| IO | DIFFIO_TX14n | | B1 | VREF2B1 | Y25 | Y25 | AD30 | | | HIGH |
| IO | DIFFIO_RX13p | | B1 | VREF2B1 | AE29 | AF32 | AJ37 | | | HIGH |
| IO | DIFFIO_RX13n | | B1 | VREF2B1 | AF29 | AF31 | AJ36 | | | HIGH |
| IO | DIFFIO_TX13p | | B1 | VREF2B1 | Y26 | Y28 | AE35 | | | HIGH |
| IO | DIFFIO_TX13n | | B1 | VREF2B1 | AA26 | Y27 | AE34 | | | HIGH |
| IO | DIFFIO_RX12p | | B1 | VREF2B1 | AH29 | AF30 | AK38 | | | HIGH |
| IO | DIFFIO_RX12n | | B1 | VREF2B1 | AG29 | AF29 | AK39 | | | HIGH |
| IO | DIFFIO_TX12p | | B1 | VREF2B1 | W23 | W23 | AE33 | | | HIGH |

Table 6–1. Pin List for the Stratix EP1S60 Device (Part 11 of 78)

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed Note (1) |
| IO | DIFFIO_TX12n | | B1 | VREF2B1 | Y23 | W24 | AE32 | | | HIGH |
| IO | DIFFIO_RX11p | | B1 | VREF2B1 | AC28 | AG31 | AK37 | | | HIGH |
| IO | DIFFIO_RX11n | | B1 | VREF2B1 | AD28 | AG32 | AK36 | | | HIGH |
| IO | DIFFIO_TX11p | | B1 | VREF2B1 | V27 | Y23 | AF35 | | | HIGH |
| IO | DIFFIO_TX11n | | B1 | VREF2B1 | W27 | Y24 | AF34 | | | HIGH |
| VREF2B1 | | | B1 | VREF2B1 | Y22 | AB25 | AG29 | | | |
| IO | DIFFIO_RX10p | | B1 | VREF2B1 | AE28 | AG30 | AL37 | | | HIGH |
| IO | DIFFIO_RX10n | | B1 | VREF2B1 | AF28 | AG29 | AL36 | | | HIGH |
| IO | DIFFIO_TX10p | | B1 | VREF2B1 | Y27 | AA25 | AF33 | | | HIGH |
| IO | DIFFIO_TX10n | | B1 | VREF2B1 | AA27 | AA24 | AF32 | | | HIGH |
| IO | DIFFIO_RX9p | | B1 | VREF2B1 | | AH32 | AM39 | | | LOW |
| IO | DIFFIO_RX9n | | B1 | VREF2B1 | | AH31 | AM38 | | | LOW |
| IO | DIFFIO_TX9p | | B1 | VREF2B1 | AB27 | AA27 | AG35 | | | HIGH |
| IO | DIFFIO_TX9n | | B1 | VREF2B1 | AC27 | AA26 | AG34 | | | HIGH |
| IO | DIFFIO_RX8p | | B1 | VREF2B1 | | AH29 | AN39 | | | LOW |
| IO | DIFFIO_RX8n | | B1 | VREF2B1 | | AG28 | AN38 | | | LOW |
| IO | DIFFIO_TX8p | | B1 | VREF2B1 | AE27 | AB27 | AG33 | | | HIGH |
| IO | DIFFIO_TX8n | | B1 | VREF2B1 | AD27 | AB26 | AG32 | | | HIGH |
| IO | DIFFIO_RX7p | | B1 | VREF2B1 | | AG25 | AM37 | | | LOW |
| IO | DIFFIO_RX7n | | B1 | VREF2B1 | | AG26 | AM36 | | | LOW |
| IO | DIFFIO_TX7p | | B1 | VREF2B1 | AG27 | AC25 | AH34 | | | HIGH |
| IO | DIFFIO_TX7n | | B1 | VREF2B1 | AF27 | AC26 | AH35 | | | HIGH |

**Table 6–1. Pin List for the Stratix EP1S60 Device (Part 12 of 78)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_RX6p | | B1 | VREF3B1 | | | AP38 | | | LOW |
| IO | DIFFIO_RX6n | | B1 | VREF3B1 | | | AP39 | | | LOW |
| IO | DIFFIO_TX6p | | B1 | VREF3B1 | AB26 | AC27 | AK35 | | | HIGH |
| IO | DIFFIO_TX6n | | B1 | VREF3B1 | AC26 | AC28 | AK34 | | | HIGH |
| IO | DIFFIO_RX5p | | B1 | VREF3B1 | | | AN37 | | | LOW |
| IO | DIFFIO_RX5n | | B1 | VREF3B1 | | | AN36 | | | LOW |
| IO | DIFFIO_TX5p | | B1 | VREF3B1 | AD26 | AD28 | AH33 | | | HIGH |
| IO | DIFFIO_TX5n | | B1 | VREF3B1 | AE26 | AD27 | AH32 | | | HIGH |
| IO | DIFFIO_RX4p | | B1 | VREF3B1 | | | AR38 | | | LOW |
| IO | DIFFIO_RX4n | | B1 | VREF3B1 | | | AR39 | | | LOW |
| IO | DIFFIO_TX4p | | B1 | VREF3B1 | AA25 | AD26 | AJ35 | | | HIGH |
| IO | DIFFIO_TX4n | | B1 | VREF3B1 | AB25 | AD25 | AJ34 | | | HIGH |
| IO | DIFFIO_RX3p | | B1 | VREF3B1 | | | AT39 | | | LOW |
| IO | DIFFIO_RX3n | | B1 | VREF3B1 | | | AT38 | | | LOW |
| IO | DIFFIO_TX3p | | B1 | VREF3B1 | AD25 | AE28 | AJ33 | | | HIGH |
| IO | DIFFIO_TX3n | | B1 | VREF3B1 | AC25 | AE27 | AJ32 | | | HIGH |
| VREF3B1 | | | B1 | VREF3B1 | AA22 | AG27 | AH29 | | | |
| IO | DIFFIO_RX2p | | B1 | VREF3B1 | | | AM35 | | | LOW |
| IO | DIFFIO_RX2n | | B1 | VREF3B1 | | | AM34 | | | LOW |
| IO | DIFFIO_TX2p | | B1 | VREF3B1 | AA24 | AE25 | AK32 | | | HIGH |
| IO | DIFFIO_TX2n | | B1 | VREF3B1 | AB24 | AE26 | AK33 | | | HIGH |
| IO | DIFFIO_RX1p | | B1 | VREF3B1 | | | AP36 | | | LOW |

*Table 6–1. Pin List for the Stratix EP1S60 Device (Part 13 of 78)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_RX1n | | B1 | VREF3B1 | | | AP37 | | | LOW |
| IO | DIFFIO_TX1p | | B1 | VREF3B1 | AD24 | AF27 | AL33 | | | HIGH |
| IO | DIFFIO_TX1n | | B1 | VREF3B1 | AC24 | AF28 | AL32 | | | HIGH |
| IO | DIFFIO_RX0p | | B1 | VREF3B1 | | | AR37 | | | LOW |
| IO | DIFFIO_RX0n | | B1 | VREF3B1 | | | AR36 | | | LOW |
| IO | DIFFIO_TX0p | | B1 | VREF3B1 | AE25 | AF26 | AH31 | | | HIGH |
| IO | DIFFIO_TX0n | | B1 | VREF3B1 | AF25 | AF25 | AH30 | | | HIGH |
| FPLL8CLKn | | | B1 | VREF3B1 | AG31 | AB29 | AL38 | | | |
| FPLL8CLKp | | | B1 | VREF3B1 | AH31 | AB28 | AL39 | | | |
| IO | | | B1 | VREF3B1 | | | AG30 | | | |
| IO | | | B1 | VREF3B1 | | | AG31 | | | |
| VCCINT | | | | | | | | | | |
| VCCA_PLL8 | | | | | AB23 | AJ31 | AJ30 | | | |
| GND | | | | | | | | | | |
| GNDA_PLL8 | | | | | AA23 | AJ32 | AJ31 | | | |
| VCCG_PLL8 | | | | | AD23 | AJ30 | AL31 | | | |
| GNDG_PLL8 | | | | | AC23 | AH30 | AK31 | | | |
| IO | | | B8 | VREF0B8 | AG28 | AB24 | AR35 | | | |
| IO | | | B8 | VREF0B8 | | | AU36 | | | |
| IO | | | B8 | VREF0B8 | | | AT35 | | | |
| IO | | | B8 | VREF0B8 | | | AN32 | | | |
| IO | | | B8 | VREF0B8 | | | AV36 | | | |

**Table 6–1. Pin List for the Stratix EP1S60 Device (Part 14 of 78)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | | | B8 | VREF0B8 | | | AT34 | | | |
| IO | | | B8 | VREF0B8 | AJ30 | AC24 | AN33 | | | |
| IO | DQ9B7 | | B8 | VREF0B8 | AK29 | AH28 | AV34 | DQ3B15 | DQ1B31 | |
| IO | | | B8 | VREF0B8 | | | AP33 | | | |
| IO | DQ9B6 | | B8 | VREF0B8 | AJ29 | AK30 | AU34 | DQ3B14 | DQ1B30 | |
| IO | | | B8 | VREF0B8 | AE24 | AG24 | AL30 | | | |
| IO | DQ9B5 | | B8 | VREF0B8 | AJ28 | AJ28 | AU33 | DQ3B13 | DQ1B29 | |
| IO | | | B8 | VREF0B8 | AF26 | AC23 | AR34 | | | |
| IO | DQ9B4 | | B8 | VREF0B8 | AL28 | AJ29 | AW33 | DQ3B12 | DQ1B28 | |
| IO | | | B8 | VREF0B8 | | AE24 | AU35 | | | |
| IO | DQ9B3 | | B8 | VREF0B8 | AH27 | AK29 | AW34 | DQ3B11 | DQ1B27 | |
| IO | | | B8 | VREF0B8 | | AG23 | AW36 | | | |
| IO | DQS9B | | B8 | VREF0B8 | AK28 | AK28 | AV33 | | | |
| VREF0B8 | | | B8 | VREF0B8 | AB22 | AH27 | AJ29 | | | |
| IO | | | B8 | VREF0B8 | AH28 | AD24 | AM31 | | | |
| IO | DQ9B2 | | B8 | VREF0B8 | AL27 | AL30 | AV32 | DQ3B10 | DQ1B26 | |
| IO | | | B8 | VREF0B8 | | AF24 | AK29 | | | |
| IO | DQ9B1 | | B8 | VREF0B8 | AJ27 | AL29 | AU32 | DQ3B9 | DQ1B25 | |
| IO | | | B8 | VREF0B8 | | | AN31 | | | |
| IO | DQ9B0 | | B8 | VREF0B8 | AK27 | AM29 | AW32 | DQ3B8 | DQ1B24 | |
| IO | | | B8 | VREF0B8 | AC22 | AD23 | AR33 | | | |
| IO | | | B8 | VREF0B8 | | | AP32 | | | |

*Table 6–1. Pin List for the Stratix EP1S60 Device (Part 15 of 78)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | | | B8 | VREF0B8 | | | AV35 | | | |
| IO | | | B8 | VREF0B8 | | | AR32 | | | |
| IO | | | B8 | VREF0B8 | | | AL29 | | | |
| IO | DQ8B7 | | B8 | VREF0B8 | AH26 | AH26 | AU31 | DQ3B7 | DQ1B23 | |
| IO | | | B8 | VREF0B8 | | | AT33 | | | |
| IO | DQ8B6 | | B8 | VREF0B8 | AG26 | AJ27 | AV31 | DQ3B6 | DQ1B22 | |
| IO | | | B8 | VREF0B8 | AD22 | AE23 | AK28 | | | |
| IO | DQ8B5 | | B8 | VREF0B8 | AK26 | AL28 | AW31 | DQ3B5 | DQ1B21 | |
| IO | | | B8 | VREF0B8 | | AF23 | AP31 | | | |
| IO | DQ8B4 | | B8 | VREF0B8 | AL26 | AK27 | AW30 | DQ3B4 | DQ1B20 | |
| IO | | | B8 | VREF1B8 | | AB22 | AW35 | | | |
| IO | DQ8B3 | | B8 | VREF1B8 | AH25 | AJ26 | AU30 | DQ3B3 | DQ1B19 | |
| IO | | | B8 | VREF1B8 | AC21 | AC22 | AM29 | | | |
| IO | DQS8B | | B8 | VREF1B8 | AJ26 | AL27 | AV30 | DQS3B | | |
| IO | | | B8 | VREF1B8 | | AG22 | AK27 | | | |
| IO | DQ8B2 | | B8 | VREF1B8 | AK25 | AM27 | AU29 | DQ3B2 | DQ1B18 | |
| IO | | | B8 | VREF1B8 | | | AN30 | | | |
| IO | DQ8B1 | | B8 | VREF1B8 | AJ25 | AM28 | AV29 | DQ3B1 | DQ1B17 | |
| IO | | | B8 | VREF1B8 | AA21 | AD22 | AT32 | | | |
| IO | DQ8B0 | | B8 | VREF1B8 | AL25 | AK26 | AW29 | DQ3B0 | DQ1B16 | |
| IO | | | B8 | VREF1B8 | AE22 | AF22 | AT31 | | | |
| IO | | | B8 | VREF1B8 | | | AP29 | | | |

**Table 6–1. Pin List for the Stratix EP1S60 Device (Part 16 of 78)**

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | | | |
| IO | | | B8 | VREF1B8 | | | AL28 | | | |
| IO | | | B8 | VREF1B8 | | | AP30 | | | |
| IO | | | B8 | VREF1B8 | | | AN29 | | | |
| IO | DQ7B7 | | B8 | VREF1B8 | AG24 | AH24 | AR28 | DQ2B15 | DQ1B15 | |
| IO | | | B8 | VREF1B8 | | | AL27 | | | |
| IO | DQ7B6 | | B8 | VREF1B8 | AH23 | AJ24 | AT28 | DQ2B14 | DQ1B14 | |
| VREF1B8 | | | B8 | VREF1B8 | AB21 | AH25 | AJ28 | | | |
| IO | | | B8 | VREF1B8 | AA19 | AE22 | AR31 | | | |
| IO | DQ7B5 | | B8 | VREF1B8 | AK24 | AJ25 | AU28 | DQ2B13 | DQ1B13 | |
| IO | | | B8 | VREF1B8 | | AA21 | AR30 | | | |
| IO | DQ7B4 | | B8 | VREF1B8 | AH24 | AK25 | AV28 | DQ2B12 | DQ1B12 | |
| IO | | | B8 | VREF1B8 | AD21 | AB21 | AK26 | | | |
| IO | DQ7B3 | | B8 | VREF1B8 | AJ23 | AL25 | AR27 | DQ2B11 | DQ1B11 | |
| IO | | | B8 | VREF1B8 | | | AM28 | | | |
| IO | DQS7B | | B8 | VREF1B8 | AJ24 | AL26 | AT27 | | DQS1B | |
| IO | | | B8 | VREF1B8 | | AC21 | AN28 | | | |
| IO | DQ7B2 | | B8 | VREF1B8 | AL24 | AK24 | AW28 | DQ2B10 | DQ1B10 | |
| IO | | | B8 | VREF1B8 | AC20 | AG21 | AP28 | | | |
| IO | DQ7B1 | | B8 | VREF1B8 | AK23 | AM25 | AU27 | DQ2B9 | DQ1B9 | |
| IO | | | B8 | VREF1B8 | | | AT30 | | | |
| IO | DQ7B0 | | B8 | VREF1B8 | AL23 | AM26 | AV27 | DQ2B8 | DQ1B8 | |
| IO | | | B8 | VREF1B8 | | | AM27 | | | |

*Table 6–1. Pin List for the Stratix EP1S60 Device (Part 17 of 78)*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **956-Pin BGA** | **1020-Pin FineLine BGA** | **1508-Pin FineLine BGA** | | | |
| IO | | | B8 | VREF1B8 | | | AL26 | | | |
| IO | FCLK3 | | B8 | VREF1B8 | AF23 | AE21 | AT29 | | | |
| IO | FCLK2 | | B8 | VREF1B8 | AF22 | AF21 | AN26 | | | |
| IO | | | B8 | VREF2B8 | | | AR29 | | | |
| IO | DQ6B7 | | B8 | VREF2B8 | AG22 | AJ23 | AR26 | DQ2B7 | DQ1B7 | |
| IO | | | B8 | VREF2B8 | | | AN27 | | | |
| IO | DQ6B6 | | B8 | VREF2B8 | AH22 | AL24 | AT26 | DQ2B6 | DQ1B6 | |
| IO | | | B8 | VREF2B8 | | | AK25 | | | |
| IO | DQ6B5 | | B8 | VREF2B8 | AK22 | AH22 | AU26 | DQ2B5 | DQ1B5 | |
| IO | | | B8 | VREF2B8 | | AD21 | AP27 | | | |
| IO | DQ6B4 | | B8 | VREF2B8 | AG21 | AM24 | AV26 | DQ2B4 | DQ1B4 | |
| IO | | PGM2 | B8 | VREF2B8 | AF24 | AA20 | AL25 | | | |
| IO | DQ6B3 | | B8 | VREF2B8 | AH21 | AK23 | AW26 | DQ2B3 | DQ1B3 | |
| IO | | | B8 | VREF2B8 | AD20 | AG20 | AP26 | | | |
| IO | DQS6B | | B8 | VREF2B8 | AJ22 | AJ22 | AU25 | DQS2B | | |
| IO | | | B8 | VREF2B8 | | AB20 | AM26 | | | |
| IO | DQ6B2 | | B8 | VREF2B8 | AL22 | AL23 | AT25 | DQ2B2 | DQ1B2 | |
| IO | | | B8 | VREF2B8 | AE21 | AF20 | AN25 | | | |
| IO | DQ6B1 | | B8 | VREF2B8 | AJ21 | AK22 | AR25 | DQ2B1 | DQ1B1 | |
| IO | | | B8 | VREF2B8 | | | AM25 | | | |
| IO | DQ6B0 | | B8 | VREF2B8 | AK21 | AL22 | AV25 | DQ2B0 | DQ1B0 | |
| VREF2B8 | | | B8 | VREF2B8 | AB20 | AH23 | AJ27 | | | |

**Table 6–1. Pin List for the Stratix EP1S60 Device (Part 18 of 78)**

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | | | |
| IO | RDN8 | | B8 | VREF2B8 | AE23 | AC20 | AH24 | | | |
| IO | | | B8 | VREF2B8 | AC19 | AD20 | AK24 | | | |
| IO | | | B8 | VREF2B8 | | | AJ24 | | | |
| IO | | | B8 | VREF2B8 | | | AL24 | | | |
| IO | RUP8 | | B8 | VREF2B8 | AG25 | AH19 | AF23 | | | |
| IO | DQ5B7 | | B8 | VREF2B8 | AG20 | AM22 | AT24 | | | |
| IO | | | B8 | VREF2B8 | | | AP25 | | | |
| IO | DQ5B6 | | B8 | VREF2B8 | AH20 | AJ21 | AU24 | | | |
| IO | | | B8 | VREF2B8 | AE20 | AE20 | AM24 | | | |
| IO | DQ5B5 | | B8 | VREF2B8 | AK20 | AK21 | AV24 | | | |
| IO | | | B8 | VREF2B8 | AD19 | AK18 | AN24 | | | |
| IO | DQ5B4 | | B8 | VREF2B8 | AL20 | AL21 | AW24 | | | |
| IO | | RDYnBSY | B8 | VREF2B8 | AG23 | AA19 | AH23 | | | |
| IO | DQ5B3 | | B8 | VREF2B8 | AG19 | AH20 | AW23 | | | |
| IO | | | B8 | VREF2B8 | AE19 | AB19 | AP24 | | | |
| IO | DQS5B | | B8 | VREF2B8 | AJ20 | AJ20 | AU23 | | | |
| IO | | | B8 | VREF2B8 | | AJ18 | AR24 | | | |
| IO | DQ5B2 | | B8 | VREF2B8 | AH19 | AK20 | AR23 | | | |
| IO | | nCS | B8 | VREF3B8 | AF20 | AC19 | AL23 | | | |
| IO | DQ5B1 | | B8 | VREF3B8 | AJ19 | AL20 | AV23 | | | |
| IO | | | B8 | VREF3B8 | | AD19 | AK23 | | | |
| IO | DQ5B0 | | B8 | VREF3B8 | AK19 | AM20 | AT23 | | | |

*Table 6–1. Pin List for the Stratix EP1S60 Device (Part 19 of 78)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **956-Pin BGA** | **1020-Pin FineLine BGA** | **1508-Pin FineLine BGA** | **DQS for x16** | **DQS for x32** | **DIFFIO Speed** *Note (1)* |
| IO | | | B8 | VREF3B8 | | | AM23 | | | |
| IO | | CS | B8 | VREF3B8 | AF21 | AG19 | AJ23 | | | |
| IO | | | B8 | VREF3B8 | | | AR22 | | | |
| IO | | | B8 | VREF3B8 | | | AL22 | | | |
| IO | | | B8 | VREF3B8 | | | AN23 | | | |
| IO | | | B8 | VREF3B8 | | | AN22 | | | |
| IO | | | B8 | VREF3B8 | | | AP23 | | | |
| IO | | | B8 | VREF3B8 | AE18 | AH18 | AP22 | | | |
| VREF3B8 | | | B8 | VREF3B8 | AB19 | AH21 | AJ26 | | | |
| IO | CLK5n | | B8 | VREF3B8 | AH18 | AJ19 | AU22 | | | |
| CLK5p | | | B8 | VREF3B8 | AJ18 | AK19 | AT22 | | | |
| IO | CLK4n | | B8 | VREF3B8 | AK18 | AL19 | AW22 | | | |
| CLK4p | | | B8 | VREF3B8 | AL18 | AM19 | AV22 | | | |
| PLL_ENA | | PLL_ENA | B8 | VREF3B8 | AF19 | AF19 | AM22 | | | |
| MSEL0 | | MSEL0 | B8 | VREF3B8 | AF18 | AG18 | AP21 | | | |
| MSEL1 | | MSEL1 | B8 | VREF3B8 | AG18 | AE18 | AG21 | | | |
| MSEL2 | | MSEL2 | B8 | VREF3B8 | AG17 | AE19 | AM21 | | | |
| IO | PLL6_OUT3n | | B12 | VREF3B8 | AL17 | AM18 | AV20 | | | |
| IO | PLL6_OUT3p | | B12 | VREF3B8 | AK17 | AL18 | AW20 | | | |
| IO | PLL6_OUT2n | | B12 | VREF3B8 | AJ17 | AK17 | AW21 | | | |
| IO | PLL6_OUT2p | | B12 | VREF3B8 | AH17 | AJ17 | AV21 | | | |
| IO | PLL6_FBn | | B11 | VREF3B8 | AJ15 | AM17 | AU20 | | | |

*Table 6–1. Pin List for the Stratix EP1S60 Device (Part 20 of 78)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | PLL6_FBp | | B11 | VREF3B8 | AH15 | AL17 | AT20 | | | |
| IO | PLL6_OUT1n | | B11 | VREF3B8 | AL15 | AK16 | AU21 | | | |
| IO | PLL6_OUT1p | | B11 | VREF3B8 | AK15 | AJ16 | AT21 | | | |
| IO | PLL6_OUT0n | | B11 | VREF3B8 | AL16 | AM16 | AU19 | | | |
| IO | PLL6_OUT0p | | B11 | VREF3B8 | AK16 | AL16 | AT19 | | | |
| VCC_PLL6_OUTB | | | B12 | | AC18 | AB17 | AH21 | | | |
| VCC_PLL6_OUTB | | | B12 | | | | | | | |
| VCC_PLL6_OUTA | | | B11 | | AD17 | AE17 | AJ21 | | | |
| VCC_PLL6_OUTA | | | B11 | | | | | | | |
| VCCINT | | | | | | | | | | |
| VCCA_PLL6 | | | | | AB17 | AG17 | AK21 | | | |
| GND | | | | | | | | | | |
| GNDA_PLL6 | | | | | AC17 | AH17 | AL20 | | | |
| VCCG_PLL6 | | | | | AD15 | AD16 | AJ20 | | | |
| GNDG_PLL6 | | | | | AD16 | AB16 | AH20 | | | |
| VCCINT | | | | | | | | | | |
| VCCA_PLL12 | | | | | AC14 | AG16 | AK19 | | | |
| GND | | | | | | | | | | |
| GNDA_PLL12 | | | | | AD14 | AH16 | AL19 | | | |
| VCCG_PLL12 | | | | | AC15 | AF16 | AJ19 | | | |
| GNDG_PLL12 | | | | | AB15 | AE16 | AH19 | | | |
| CLK7p | | | B7 | VREF0B7 | AJ14 | AM15 | AW18 | | | |

**Table 6–1. Pin List for the Stratix EP1S60 Device (Part 21 of 78)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | CLK7n | | B7 | VREF0B7 | AH14 | AL15 | AV18 | | | |
| CLK6p | | | B7 | VREF0B7 | AL14 | AK15 | AW19 | | | |
| IO | CLK6n/PLL12_OUT | | B7 | VREF0B7 | AK14 | AJ15 | AV19 | | | |
| nCE | | nCE | B7 | VREF0B7 | AF17 | AF18 | AN20 | | | |
| nCEO | | nCEO | B7 | VREF0B7 | AF16 | AH15 | AP20 | | | |
| IO | | | B7 | VREF0B7 | | | AP19 | | | |
| IO | | | B7 | VREF0B7 | | | AR19 | | | |
| IO | | PGM0 | B7 | VREF0B7 | AE17 | AD18 | AG20 | | | |
| nIO_PULLUP | | nIO_PULLUP | B7 | VREF0B7 | AE16 | AF15 | AR20 | | | |
| VCCSEL | | VCCSEL | B7 | VREF0B7 | AE15 | AJ14 | AM19 | | | |
| PORSEL | | PORSEL | B7 | VREF0B7 | AG16 | AG15 | AN19 | | | |
| IO | | | B7 | VREF0B7 | | | AH18 | | | |
| IO | | | B7 | VREF0B7 | | | AJ18 | | | |
| IO | | INIT_DONE | B7 | VREF0B7 | AF15 | AE15 | AL18 | | | |
| IO | | | B7 | VREF0B7 | | | AM18 | | | |
| IO | | | B7 | VREF0B7 | | | AK18 | | | |
| IO | | | B7 | VREF0B7 | | | AN18 | | | |
| VREF0B7 | | | B7 | VREF0B7 | AB14 | AH12 | AJ15 | | | |
| IO | | | B7 | VREF0B7 | AA16 | AC18 | AP18 | | | |
| IO | | | B7 | VREF0B7 | | | AR16 | | | |
| IO | | | B7 | VREF0B7 | | | AR18 | | | |
| IO | | | B7 | VREF0B7 | | | AM17 | | | |

Table 6–1. Pin List for the Stratix EP1S60 Device (Part 22 of 78)

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | | | |
| IO | | | B7 | VREF0B7 | | | AT18 | | | |
| IO | | | B7 | VREF0B7 | | | AU18 | | | |
| IO | | nRS | B7 | VREF0B7 | AE14 | AB18 | AL17 | | | |
| IO | | | B7 | VREF0B7 | | AA18 | AH17 | | | |
| IO | DQ4B7 | | B7 | VREF0B7 | AK13 | AL13 | AU17 | | | |
| IO | | | B7 | VREF0B7 | AH16 | AE14 | AJ17 | | | |
| IO | DQ4B6 | | B7 | VREF0B7 | AG13 | AM13 | AR17 | | | |
| IO | | RUnLU | B7 | VREF0B7 | AJ16 | AF14 | AK17 | | | |
| IO | DQ4B5 | | B7 | VREF0B7 | AH13 | AH13 | AT17 | | | |
| IO | | | B7 | VREF0B7 | AA15 | AD14 | AM16 | | | |
| IO | DQ4B4 | | B7 | VREF0B7 | AJ13 | AJ13 | AV17 | | | |
| IO | | | B7 | VREF0B7 | | AD15 | AP16 | | | |
| IO | DQ4B3 | | B7 | VREF0B7 | AK12 | AK13 | AV16 | | | |
| IO | | PGM1 | B7 | VREF0B7 | AG15 | AG14 | AF16 | | | |
| IO | DQS4B | | B7 | VREF1B7 | AJ12 | AJ12 | AU16 | | | |
| IO | | | B7 | VREF1B7 | AA13 | AB15 | AH16 | | | |
| IO | DQ4B2 | | B7 | VREF1B7 | AL12 | AK12 | AW17 | | | |
| IO | | | B7 | VREF1B7 | | AC15 | AP15 | | | |
| IO | DQ4B1 | | B7 | VREF1B7 | AG12 | AL12 | AT16 | | | |
| IO | DEV_CLRn | | B7 | VREF1B7 | AF14 | AH14 | AN17 | | | |
| IO | DQ4B0 | | B7 | VREF1B7 | AH12 | AM11 | AW16 | | | |
| IO | RDN7 | | B7 | VREF1B7 | AG14 | AC14 | AP17 | | | |

**Table 6–1. Pin List for the Stratix EP1S60 Device (Part 23 of 78)**

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **956-Pin BGA** | **1020-Pin FineLine BGA** | **1508-Pin FineLine BGA** | | | |
| IO | | | B7 | VREF1B7 | | | AK16 | | | |
| IO | | | B7 | VREF1B7 | | | AJ16 | | | |
| IO | | | B7 | VREF1B7 | AD13 | AK14 | AL16 | | | |
| IO | RUP7 | | B7 | VREF1B7 | AF13 | AF13 | AN16 | | | |
| IO | DQ3B7 | | B7 | VREF1B7 | AL10 | AL10 | AT15 | DQ1B15 | DQ0B31 | |
| IO | | | B7 | VREF1B7 | | AA15 | AL15 | | | |
| IO | DQ3B6 | | B7 | VREF1B7 | AJ11 | AK11 | AR15 | DQ1B14 | DQ0B30 | |
| IO | | | B7 | VREF1B7 | AC13 | AE13 | AM15 | | | |
| IO | DQ3B5 | | B7 | VREF1B7 | AK11 | AL11 | AV15 | DQ1B13 | DQ0B29 | |
| IO | | | B7 | VREF1B7 | AE13 | AG13 | AN15 | | | |
| VREF1B7 | | | B7 | VREF1B7 | AB13 | AH10 | AJ14 | | | |
| IO | DQ3B4 | | B7 | VREF1B7 | AG11 | AK10 | AV14 | DQ1B12 | DQ0B28 | |
| IO | | | B7 | VREF1B7 | | | AP13 | | | |
| IO | DQ3B3 | | B7 | VREF1B7 | AH11 | AM9 | AW14 | DQ1B11 | DQ0B27 | |
| IO | | | B7 | VREF1B7 | AD12 | AD13 | AM14 | | | |
| IO | DQS3B | | B7 | VREF1B7 | AJ10 | AJ11 | AU15 | DQS1B | | |
| IO | | | B7 | VREF1B7 | AE12 | AL14 | AP14 | | | |
| IO | DQ3B2 | | B7 | VREF1B7 | AG10 | AL9 | AR14 | DQ1B10 | DQ0B26 | |
| IO | | | B7 | VREF1B7 | AC12 | AE12 | AR11 | | | |
| IO | DQ3B1 | | B7 | VREF1B7 | AH10 | AJ10 | AT14 | DQ1B9 | DQ0B25 | |
| IO | | | B7 | VREF1B7 | | AB14 | AN13 | | | |
| IO | DQ3B0 | | B7 | VREF1B7 | AK10 | AH11 | AU14 | DQ1B8 | DQ0B24 | |

*Table 6–1. Pin List for the Stratix EP1S60 Device (Part 24 of 78)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | | | B7 | VREF1B7 | | | AK15 | | | |
| IO | | | B7 | VREF1B7 | | | AM13 | | | |
| IO | | | B7 | VREF1B7 | | | AP11 | | | |
| IO | | | B7 | VREF1B7 | | | AL14 | | | |
| IO | DQ2B7 | | B7 | VREF1B7 | AL8 | AL8 | AT13 | DQ1B7 | DQ0B23 | |
| IO | FCLK5 | | B7 | VREF1B7 | AF12 | AM14 | AN14 | | | |
| IO | FCLK4 | | B7 | VREF1B7 | AF11 | AF12 | AT11 | | | |
| IO | DQ2B6 | | B7 | VREF2B7 | AK9 | AJ9 | AU13 | DQ1B6 | DQ0B22 | |
| IO | | | B7 | VREF2B7 | | AB13 | AM12 | | | |
| IO | DQ2B5 | | B7 | VREF2B7 | AL9 | AK9 | AV13 | DQ1B5 | DQ0B21 | |
| IO | | | B7 | VREF2B7 | AG9 | AA14 | AT10 | | | |
| IO | DQ2B4 | | B7 | VREF2B7 | AH8 | AM8 | AV12 | DQ1B4 | DQ0B20 | |
| IO | | | B7 | VREF2B7 | AE11 | AC13 | AP12 | | | |
| IO | DQ2B3 | | B7 | VREF2B7 | AK8 | AH9 | AR13 | DQ1B3 | DQ0B19 | |
| IO | | | B7 | VREF2B7 | | | AP10 | | | |
| IO | DQS2B | | B7 | VREF2B7 | AJ8 | AK8 | AU12 | | DQS0B | |
| IO | | | B7 | VREF2B7 | AE10 | AE11 | AR10 | | | |
| IO | DQ2B2 | | B7 | VREF2B7 | AG8 | AM7 | AR12 | DQ1B2 | DQ0B18 | |
| IO | | | B7 | VREF2B7 | AF10 | AD12 | AK14 | | | |
| IO | DQ2B1 | | B7 | VREF2B7 | AH9 | AJ8 | AT12 | DQ1B1 | DQ0B17 | |
| IO | | | B7 | VREF2B7 | | AC12 | AL12 | | | |
| IO | DQ2B0 | | B7 | VREF2B7 | AJ9 | AL7 | AW12 | DQ1B0 | DQ0B16 | |

*Table 6–1. Pin List for the Stratix EP1S60 Device (Part 25 of 78)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **956-Pin BGA** | **1020-Pin FineLine BGA** | **1508-Pin FineLine BGA** | **DQS for x16** | **DQS for x32** | **DIFFIO Speed** *Note (1)* |
| IO | | | B7 | VREF2B7 | | | AN11 | | | |
| IO | | | B7 | VREF2B7 | | | AN12 | | | |
| IO | | | B7 | VREF2B7 | AD11 | AG12 | AL13 | | | |
| VREF2B7 | | | B7 | VREF2B7 | AB12 | AH8 | AJ13 | | | |
| IO | | | B7 | VREF2B7 | | | AT8 | | | |
| IO | | | B7 | VREF2B7 | AA11 | AD11 | AN10 | | | |
| IO | DQ1B7 | | B7 | VREF2B7 | AK7 | AL6 | AV11 | DQ0B15 | DQ0B15 | |
| IO | | | B7 | VREF2B7 | | AA13 | AK13 | | | |
| IO | DQ1B6 | | B7 | VREF2B7 | AL7 | AM6 | AW11 | DQ0B14 | DQ0B14 | |
| IO | | | B7 | VREF2B7 | AF9 | AF11 | AT9 | | | |
| IO | DQ1B5 | | B7 | VREF2B7 | AH6 | AJ7 | AU10 | DQ0B13 | DQ0B13 | |
| IO | | | B7 | VREF2B7 | AD10 | AB12 | AW5 | | | |
| IO | DQ1B4 | | B7 | VREF2B7 | AK6 | AM5 | AW10 | DQ0B12 | DQ0B12 | |
| IO | | | B7 | VREF2B7 | AC11 | AE10 | AM11 | | | |
| IO | DQ1B3 | | B7 | VREF2B7 | AL6 | AK7 | AU11 | DQ0B11 | DQ0B11 | |
| IO | | | B7 | VREF2B7 | | | AR9 | | | |
| IO | DQS1B | | B7 | VREF2B7 | AJ6 | AH7 | AV10 | DQS0B | | |
| IO | | | B7 | VREF2B7 | AC10 | AD10 | AV5 | | | |
| IO | DQ1B2 | | B7 | VREF2B7 | AH7 | AL5 | AW9 | DQ0B10 | DQ0B10 | |
| IO | | | B7 | VREF2B7 | AE9 | AC11 | AR8 | | | |
| IO | DQ1B1 | | B7 | VREF2B7 | AJ7 | AK6 | AV9 | DQ0B9 | DQ0B9 | |
| IO | | | B7 | VREF2B7 | | AF10 | AP9 | | | |

**Table 6–1. Pin List for the Stratix EP1S60 Device (Part 26 of 78)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DQ1B0 | | B7 | VREF3B7 | AG6 | AJ6 | AU9 | DQ0B8 | DQ0B8 | |
| IO | | | B7 | VREF3B7 | | | AR7 | | | |
| IO | | | B7 | VREF3B7 | | | AT7 | | | |
| IO | | | B7 | VREF3B7 | | | AW4 | | | |
| IO | | | B7 | VREF3B7 | | | AK12 | | | |
| IO | | | B7 | VREF3B7 | AF8 | AG11 | AL11 | | | |
| IO | DQ0B7 | | B7 | VREF3B7 | AL4 | AL3 | AV8 | DQ0B7 | DQ0B7 | |
| IO | | | B7 | VREF3B7 | | AB11 | AM9 | | | |
| IO | DQ0B6 | | B7 | VREF3B7 | AL5 | AL4 | AW8 | DQ0B6 | DQ0B6 | |
| IO | | | B7 | VREF3B7 | AH4 | AE9 | AK11 | | | |
| IO | DQ0B5 | | B7 | VREF3B7 | AJ4 | AM4 | AW6 | DQ0B5 | DQ0B5 | |
| IO | | | B7 | VREF3B7 | AG7 | AF9 | AN9 | | | |
| VREF3B7 | | | B7 | VREF3B7 | AB11 | AH6 | AJ12 | | | |
| IO | DQ0B4 | | B7 | VREF3B7 | AK3 | AJ4 | AU8 | DQ0B4 | DQ0B4 | |
| IO | | | B7 | VREF3B7 | | | AR6 | | | |
| IO | DQ0B3 | | B7 | VREF3B7 | AK5 | AJ5 | AW7 | DQ0B3 | DQ0B3 | |
| IO | | | B7 | VREF3B7 | AF6 | AA12 | AU5 | | | |
| IO | DQS0B | | B7 | VREF3B7 | AK4 | AK5 | AV7 | | | |
| IO | | | B7 | VREF3B7 | AE8 | AG10 | AP8 | | | |
| IO | DQ0B2 | | B7 | VREF3B7 | AH5 | AH5 | AU7 | DQ0B2 | DQ0B2 | |
| IO | | | B7 | VREF3B7 | AG4 | AC9 | AN7 | | | |
| IO | DQ0B1 | | B7 | VREF3B7 | AJ5 | AK3 | AV6 | DQ0B1 | DQ0B1 | |

*Table 6–1. Pin List for the Stratix EP1S60 Device (Part 27 of 78)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **956-Pin BGA** | **1020-Pin FineLine BGA** | **1508-Pin FineLine BGA** | **DQS for x16** | **DQS for x32** | **DIFFIO Speed** *Note (1)* |
| IO | | | B7 | VREF3B7 | | AD9 | AP7 | | | |
| IO | DQ0B0 | | B7 | VREF3B7 | AJ3 | AK4 | AU6 | DQ0B0 | DQ0B0 | |
| IO | | | B7 | VREF3B7 | | | AL10 | | | |
| IO | | | B7 | VREF3B7 | | | AU4 | | | |
| IO | | | B7 | VREF3B7 | | | AR5 | | | |
| IO | | | B7 | VREF3B7 | | | AN8 | | | |
| IO | | | B7 | VREF3B7 | | | AT5 | | | |
| IO | | | B7 | VREF3B7 | | | AT6 | | | |
| IO | | | B7 | VREF3B7 | AJ2 | AG9 | AV4 | | | |
| GNDG_PLL9 | | | | | AC9 | AH3 | AK9 | | | |
| VCCG_PLL9 | | | | | AD9 | AJ3 | AL9 | | | |
| GNDA_PLL9 | | | | | AA9 | AJ1 | AJ9 | | | |
| GND | | | | | | | | | | |
| VCCA_PLL9 | | | | | AB9 | AJ2 | AJ10 | | | |
| VCCINT | | | | | | | | | | |
| IO | | | B6 | VREF0B6 | | | AG10 | | | |
| IO | | | B6 | VREF0B6 | | | AG9 | | | |
| FPLL9CLKp | | | B6 | VREF0B6 | AH1 | AB5 | AL1 | | | |
| FPLL9CLKn | | | B6 | VREF0B6 | AG1 | AB4 | AL2 | | | |
| IO | DIFFIO_TX115n | | B6 | VREF0B6 | AC8 | AF8 | AH10 | | | HIGH |
| IO | DIFFIO_TX115p | | B6 | VREF0B6 | AD8 | AF7 | AH9 | | | HIGH |
| IO | DIFFIO_RX115n | | B6 | VREF0B6 | | | AR4 | | | LOW |

**Table 6–1. Pin List for the Stratix EP1S60 Device (Part 28 of 78)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_RX115p | | B6 | VREF0B6 | | | AR3 | | | LOW |
| IO | DIFFIO_TX114n | | B6 | VREF0B6 | AF7 | AF5 | AL8 | | | HIGH |
| IO | DIFFIO_TX114p | | B6 | VREF0B6 | AE7 | AF6 | AL7 | | | HIGH |
| IO | DIFFIO_RX114n | | B6 | VREF0B6 | | | AP3 | | | LOW |
| IO | DIFFIO_RX114p | | B6 | VREF0B6 | | | AP4 | | | LOW |
| IO | DIFFIO_TX113n | | B6 | VREF0B6 | AB8 | AE7 | AK7 | | | HIGH |
| IO | DIFFIO_TX113p | | B6 | VREF0B6 | AA8 | AE8 | AK8 | | | HIGH |
| IO | DIFFIO_RX113n | | B6 | VREF0B6 | | | AM6 | | | LOW |
| IO | DIFFIO_RX113p | | B6 | VREF0B6 | | | AM5 | | | LOW |
| VREF0B6 | | | B6 | VREF0B6 | AA10 | AG6 | AH11 | | | |
| IO | DIFFIO_TX112n | | B6 | VREF0B6 | AC7 | AD6 | AJ7 | | | HIGH |
| IO | DIFFIO_TX112p | | B6 | VREF0B6 | AD7 | AD5 | AJ8 | | | HIGH |
| IO | DIFFIO_RX112n | | B6 | VREF0B6 | | | AT2 | | | LOW |
| IO | DIFFIO_RX112p | | B6 | VREF0B6 | | | AT1 | | | LOW |
| IO | DIFFIO_TX111n | | B6 | VREF0B6 | AB7 | AE6 | AH8 | | | HIGH |
| IO | DIFFIO_TX111p | | B6 | VREF0B6 | AA7 | AE5 | AH7 | | | HIGH |
| IO | DIFFIO_RX111n | | B6 | VREF0B6 | | | AR2 | | | LOW |
| IO | DIFFIO_RX111p | | B6 | VREF0B6 | | | AR1 | | | LOW |
| IO | DIFFIO_TX110n | | B6 | VREF0B6 | AE6 | AD8 | AG8 | | | HIGH |
| IO | DIFFIO_TX110p | | B6 | VREF0B6 | AD6 | AD7 | AG7 | | | HIGH |
| IO | DIFFIO_RX110n | | B6 | VREF0B6 | | | AN4 | | | LOW |
| IO | DIFFIO_RX110p | | B6 | VREF0B6 | | | AN3 | | | LOW |

**Table 6–1. Pin List for the Stratix EP1S60 Device (Part 29 of 78)**

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | | | |
| IO | DIFFIO_TX109n | | B6 | VREF0B6 | AC6 | AC5 | AK6 | | | HIGH |
| IO | DIFFIO_TX109p | | B6 | VREF0B6 | AB6 | AC6 | AK5 | | | HIGH |
| IO | DIFFIO_RX109n | | B6 | VREF0B6 | | | AP1 | | | LOW |
| IO | DIFFIO_RX109p | | B6 | VREF0B6 | | | AP2 | | | LOW |
| IO | DIFFIO_TX108n | | B6 | VREF1B6 | AF5 | AC7 | AJ5 | | | HIGH |
| IO | DIFFIO_TX108p | | B6 | VREF1B6 | AG5 | AC8 | AJ6 | | | HIGH |
| IO | DIFFIO_RX108n | | B6 | VREF1B6 | | AG7 | AM4 | | | LOW |
| IO | DIFFIO_RX108p | | B6 | VREF1B6 | | AG8 | AM3 | | | LOW |
| IO | DIFFIO_TX107n | | B6 | VREF1B6 | AD5 | AB7 | AH5 | | | HIGH |
| IO | DIFFIO_TX107p | | B6 | VREF1B6 | AE5 | AB6 | AH6 | | | HIGH |
| IO | DIFFIO_RX107n | | B6 | VREF1B6 | | AG5 | AN2 | | | LOW |
| IO | DIFFIO_RX107p | | B6 | VREF1B6 | | AH4 | AN1 | | | LOW |
| IO | DIFFIO_TX106n | | B6 | VREF1B6 | AC5 | AA6 | AG6 | | | HIGH |
| IO | DIFFIO_TX106p | | B6 | VREF1B6 | AB5 | AA7 | AG5 | | | HIGH |
| IO | DIFFIO_RX106n | | B6 | VREF1B6 | | AH2 | AM2 | | | LOW |
| IO | DIFFIO_RX106p | | B6 | VREF1B6 | | AH1 | AM1 | | | LOW |
| IO | DIFFIO_TX105n | | B6 | VREF1B6 | AA6 | AA9 | AF8 | | | HIGH |
| IO | DIFFIO_TX105p | | B6 | VREF1B6 | Y6 | AA8 | AF7 | | | HIGH |
| IO | DIFFIO_RX105n | | B6 | VREF1B6 | AF4 | AG4 | AL4 | | | HIGH |
| IO | DIFFIO_RX105p | | B6 | VREF1B6 | AE4 | AG3 | AL3 | | | HIGH |
| VREF1B6 | | | B6 | VREF1B6 | Y10 | AB8 | AG11 | | | |
| IO | DIFFIO_TX104n | | B6 | VREF1B6 | Y9 | Y5 | AF6 | | | HIGH |

**Table 6–1. Pin List for the Stratix EP1S60 Device (Part 30 of 78)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_TX104p | | B6 | VREF1B6 | W9 | Y6 | AF5 | | | HIGH |
| IO | DIFFIO_RX104n | | B6 | VREF1B6 | AD4 | AG1 | AK4 | | | HIGH |
| IO | DIFFIO_RX104p | | B6 | VREF1B6 | AC4 | AG2 | AK3 | | | HIGH |
| IO | DIFFIO_TX103n | | B6 | VREF1B6 | Y8 | Y7 | AE8 | | | HIGH |
| IO | DIFFIO_TX103p | | B6 | VREF1B6 | W8 | Y8 | AE7 | | | HIGH |
| IO | DIFFIO_RX103n | | B6 | VREF1B6 | AG3 | AF4 | AK1 | | | HIGH |
| IO | DIFFIO_RX103p | | B6 | VREF1B6 | AH3 | AF3 | AK2 | | | HIGH |
| IO | DIFFIO_TX102n | | B6 | VREF1B6 | AA5 | W5 | AE6 | | | HIGH |
| IO | DIFFIO_TX102p | | B6 | VREF1B6 | Y5 | W6 | AE5 | | | HIGH |
| IO | DIFFIO_RX102n | | B6 | VREF1B6 | AF3 | AF2 | AJ4 | | | HIGH |
| IO | DIFFIO_RX102p | | B6 | VREF1B6 | AE3 | AF1 | AJ3 | | | HIGH |
| IO | DIFFIO_TX101n | | B6 | VREF1B6 | Y7 | Y10 | AD10 | | | HIGH |
| IO | DIFFIO_TX101p | | B6 | VREF1B6 | W7 | Y9 | AD9 | | | HIGH |
| IO | DIFFIO_RX101n | | B6 | VREF1B6 | AD3 | AE4 | AJ2 | | | HIGH |
| IO | DIFFIO_RX101p | | B6 | VREF1B6 | AC3 | AE3 | AJ1 | | | HIGH |
| IO | DIFFIO_TX100n | | B6 | VREF2B6 | U7 | W10 | AD8 | | | HIGH |
| IO | DIFFIO_TX100p | | B6 | VREF2B6 | V7 | W9 | AD7 | | | HIGH |
| IO | DIFFIO_RX100n | | B6 | VREF2B6 | AH2 | AE2 | AH4 | | | HIGH |
| IO | DIFFIO_RX100p | | B6 | VREF2B6 | AG2 | AE1 | AH3 | | | HIGH |
| IO | DIFFIO_TX99n | | B6 | VREF2B6 | W6 | V9 | AD5 | | | HIGH |
| IO | DIFFIO_TX99p | | B6 | VREF2B6 | V6 | V10 | AD6 | | | HIGH |
| IO | DIFFIO_RX99n | | B6 | VREF2B6 | AE2 | AC3 | AH1 | | | HIGH |

**Table 6–1. Pin List for the Stratix EP1S60 Device (Part 31 of 78)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_RX99p | | B6 | VREF2B6 | AF2 | AC4 | AH2 | | | HIGH |
| IO | DIFFIO_TX98n | | B6 | VREF2B6 | U6 | V5 | AC5 | | | HIGH |
| IO | DIFFIO_TX98p | | B6 | VREF2B6 | T6 | V6 | AC6 | | | HIGH |
| IO | DIFFIO_RX98n | | B6 | VREF2B6 | AD2 | AD3 | AG4 | | | HIGH |
| IO | DIFFIO_RX98p | | B6 | VREF2B6 | AC2 | AD4 | AG3 | | | HIGH |
| IO | DIFFIO_TX97n | | B6 | VREF2B6 | W5 | V8 | AC7 | | | HIGH |
| IO | DIFFIO_TX97p | | B6 | VREF2B6 | V5 | V7 | AC8 | | | HIGH |
| IO | DIFFIO_RX97n | | B6 | VREF2B6 | AF1 | AD2 | AG2 | | | HIGH |
| IO | DIFFIO_RX97p | | B6 | VREF2B6 | AE1 | AD1 | AF2 | | | HIGH |
| VREF2B6 | | | B6 | VREF2B6 | W10 | AA10 | AF11 | | | |
| IO | DIFFIO_TX96n | | B6 | VREF2B6 | T5 | W8 | AB5 | | | HIGH |
| IO | DIFFIO_TX96p | | B6 | VREF2B6 | U5 | W7 | AB6 | | | HIGH |
| IO | DIFFIO_RX96n | | B6 | VREF2B6 | AD1 | AC2 | AF1 | | | HIGH |
| IO | DIFFIO_RX96p | | B6 | VREF2B6 | AC1 | AB1 | AE2 | | | HIGH |
| IO | DIFFIO_TX95n | | B6 | VREF2B6 | | AB9 | AD12 | | | LOW |
| IO | DIFFIO_TX95p | | B6 | VREF2B6 | | AC10 | AD11 | | | LOW |
| IO | DIFFIO_RX95n/RDN6 | | B6 | VREF2B6 | AB4 | AA4 | AF4 | | | HIGH |
| IO | DIFFIO_RX95p/RUP6 | | B6 | VREF2B6 | AB3 | AA5 | AF3 | | | HIGH |
| IO | DIFFIO_TX94n | | B6 | VREF2B6 | | AB10 | AC11 | | | LOW |
| IO | DIFFIO_TX94p | | B6 | VREF2B6 | | AA11 | AC12 | | | LOW |
| IO | DIFFIO_RX94n | | B6 | VREF2B6 | Y4 | AB3 | AE4 | | | HIGH |
| IO | DIFFIO_RX94p | | B6 | VREF2B6 | AA4 | AB2 | AE3 | | | HIGH |

**Table 6–1. Pin List for the Stratix EP1S60 Device (Part 32 of 78)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_TX93n | | B6 | VREF2B6 | | Y11 | AC9 | | | LOW |
| IO | DIFFIO_TX93p | | B6 | VREF2B6 | | Y12 | AC10 | | | LOW |
| IO | DIFFIO_RX93n | | B6 | VREF2B6 | W4 | AA3 | AD4 | | | HIGH |
| IO | DIFFIO_RX93p | | B6 | VREF2B6 | V4 | AA2 | AD3 | | | HIGH |
| IO | DIFFIO_TX92n | | B6 | VREF3B6 | | W11 | AB10 | | | LOW |
| IO | DIFFIO_TX92p | | B6 | VREF3B6 | | W12 | AB11 | | | LOW |
| IO | DIFFIO_RX92n | | B6 | VREF3B6 | AA3 | Y4 | AD2 | | | HIGH |
| IO | DIFFIO_RX92p | | B6 | VREF3B6 | Y3 | Y3 | AD1 | | | HIGH |
| IO | DIFFIO_TX91n | | B6 | VREF3B6 | | | AB13 | | | LOW |
| IO | DIFFIO_TX91p | | B6 | VREF3B6 | | | AB12 | | | LOW |
| IO | DIFFIO_RX91n | | B6 | VREF3B6 | W3 | Y2 | AC4 | | | HIGH |
| IO | DIFFIO_RX91p | | B6 | VREF3B6 | V3 | Y1 | AC3 | | | HIGH |
| IO | DIFFIO_TX90n | | B6 | VREF3B6 | | | AB8 | | | LOW |
| IO | DIFFIO_TX90p | | B6 | VREF3B6 | | | AB9 | | | LOW |
| IO | DIFFIO_RX90n | | B6 | VREF3B6 | AB2 | W4 | AC2 | | | HIGH |
| IO | DIFFIO_RX90p | | B6 | VREF3B6 | AA2 | W3 | AC1 | | | HIGH |
| IO | DIFFIO_TX89n | | B6 | VREF3B6 | | | AB7 | | | LOW |
| IO | DIFFIO_TX89p | | B6 | VREF3B6 | | | AA6 | | | LOW |
| IO | DIFFIO_RX89n | | B6 | VREF3B6 | Y2 | W2 | AB4 | | | HIGH |
| IO | DIFFIO_RX89p | | B6 | VREF3B6 | W2 | W1 | AB3 | | | HIGH |
| VREF3B6 | | | B6 | VREF3B6 | V10 | V12 | AE11 | | | |
| IO | DIFFIO_TX88n | | B6 | VREF3B6 | | | AA12 | | | LOW |

*Table 6–1. Pin List for the Stratix EP1S60 Device (Part 33 of 78)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **956-Pin BGA** | **1020-Pin FineLine BGA** | **1508-Pin FineLine BGA** | **DQS for x16** | **DQS for x32** | **DIFFIO Speed** *Note (1)* |
| IO | DIFFIO_TX88p | | B6 | VREF3B6 | | | AA13 | | | LOW |
| IO | DIFFIO_RX88n | | B6 | VREF3B6 | AA1 | V4 | AB1 | | | HIGH |
| IO | DIFFIO_RX88p | | B6 | VREF3B6 | AB1 | V3 | AB2 | | | HIGH |
| IO | DIFFIO_TX87n | | B6 | VREF3B6 | | | AA11 | | | LOW |
| IO | DIFFIO_TX87p | | B6 | VREF3B6 | | | AA10 | | | LOW |
| IO | DIFFIO_RX87n | | B6 | VREF3B6 | V2 | V2 | AA4 | | | HIGH |
| IO | DIFFIO_RX87p | | B6 | VREF3B6 | U2 | V1 | AA3 | | | HIGH |
| IO | DIFFIO_TX86n | | B6 | VREF3B6 | | | AA9 | | | LOW |
| IO | DIFFIO_TX86p | | B6 | VREF3B6 | | | AA8 | | | LOW |
| IO | DIFFIO_RX86n | | B6 | VREF3B6 | V1 | U5 | AA2 | | | HIGH |
| IO | DIFFIO_RX86p | | B6 | VREF3B6 | U1 | U6 | AA1 | | | HIGH |
| IO | CLK8n | | B6 | VREF3B6 | U4 | U3 | Y5 | | | |
| CLK8p | | | B6 | VREF3B6 | U3 | U4 | Y6 | | | |
| CLK9n | | | B6 | VREF3B6 | T3 | U1 | Y2 | | | |
| CLK9p | | | B6 | VREF3B6 | T4 | U2 | Y1 | | | |
| GNDG_PLL3 | | | | | V9 | U11 | Y11 | | | |
| VCCG_PLL3 | | | | | U9 | V11 | Y12 | | | |
| GNDA_PLL3 | | | | | V8 | U7 | Y9 | | | |
| GND | | | | | | | | | | |
| VCCA_PLL3 | | | | | U8 | U8 | W8 | | | |
| VCCINT | | | | | | | | | | |
| GNDG_PLL4 | | | | | R9 | U9 | W11 | | | |

*Table 6–1. Pin List for the Stratix EP1S60 Device (Part 34 of 78)*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | | | |
| VCCG_PLL4 | | | | | R10 | T9 | W12 | | | |
| GNDA_PLL4 | | | | | R8 | T7 | W9 | | | |
| GND | | | | | | | | | | |
| VCCA_PLL4 | | | | | T8 | T8 | W10 | | | |
| VCCINT | | | | | | | | | | |
| CLK10p | | | B5 | VREF0B5 | T1 | T6 | Y3 | | | |
| IO | CLK10n | | B5 | VREF0B5 | T2 | T5 | Y4 | | | |
| CLK11p | | | B5 | VREF0B5 | R3 | T4 | W5 | | | |
| CLK11n | | | B5 | VREF0B5 | R4 | T3 | W6 | | | |
| IO | DIFFIO_TX85n | | B5 | VREF0B5 | | | Y7 | | | LOW |
| IO | DIFFIO_TX85p | | B5 | VREF0B5 | | | W7 | | | LOW |
| IO | DIFFIO_RX85n | | B5 | VREF0B5 | R1 | T2 | W1 | | | HIGH |
| IO | DIFFIO_RX85p | | B5 | VREF0B5 | P1 | T1 | W2 | | | HIGH |
| IO | DIFFIO_TX84n | | B5 | VREF0B5 | | | V7 | | | LOW |
| IO | DIFFIO_TX84p | | B5 | VREF0B5 | | | V8 | | | LOW |
| IO | DIFFIO_RX84n | | B5 | VREF0B5 | P2 | R1 | W4 | | | HIGH |
| IO | DIFFIO_RX84p | | B5 | VREF0B5 | R2 | R2 | W3 | | | HIGH |
| IO | DIFFIO_TX83n | | B5 | VREF0B5 | | | V9 | | | LOW |
| IO | DIFFIO_TX83p | | B5 | VREF0B5 | | | V10 | | | LOW |
| IO | DIFFIO_RX83n | | B5 | VREF0B5 | K1 | R3 | V1 | | | HIGH |
| IO | DIFFIO_RX83p | | B5 | VREF0B5 | L1 | R4 | V2 | | | HIGH |
| IO | DIFFIO_TX82n | | B5 | VREF0B5 | | | W14 | | | LOW |

**Table 6–1. Pin List for the Stratix EP1S60 Device (Part 35 of 78)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_TX82p | | B5 | VREF0B5 | | | V14 | | | LOW |
| IO | DIFFIO_RX82n | | B5 | VREF0B5 | N2 | P1 | V3 | | | HIGH |
| IO | DIFFIO_RX82p | | B5 | VREF0B5 | M2 | P2 | V4 | | | HIGH |
| VREF0B5 | | | B5 | VREF0B5 | P10 | R12 | R11 | | | |
| IO | DIFFIO_TX81n | | B5 | VREF0B5 | | | V11 | | | LOW |
| IO | DIFFIO_TX81p | | B5 | VREF0B5 | | | V12 | | | LOW |
| IO | DIFFIO_RX81n | | B5 | VREF0B5 | L2 | P3 | U1 | | | HIGH |
| IO | DIFFIO_RX81p | | B5 | VREF0B5 | K2 | P4 | U2 | | | HIGH |
| IO | DIFFIO_TX80n | | B5 | VREF0B5 | | | U13 | | | LOW |
| IO | DIFFIO_TX80p | | B5 | VREF0B5 | | | V13 | | | LOW |
| IO | DIFFIO_RX80n | | B5 | VREF0B5 | P3 | N1 | U3 | | | HIGH |
| IO | DIFFIO_RX80p | | B5 | VREF0B5 | N3 | N2 | U4 | | | HIGH |
| IO | DIFFIO_TX79n | | B5 | VREF0B5 | | T11 | U12 | | | LOW |
| IO | DIFFIO_TX79p | | B5 | VREF0B5 | | R11 | U11 | | | LOW |
| IO | DIFFIO_RX79n | | B5 | VREF0B5 | L3 | N3 | T2 | | | HIGH |
| IO | DIFFIO_RX79p | | B5 | VREF0B5 | M3 | N4 | T1 | | | HIGH |
| IO | DIFFIO_TX78n | | B5 | VREF0B5 | | P11 | U9 | | | LOW |
| IO | DIFFIO_TX78p | | B5 | VREF0B5 | | N11 | U10 | | | LOW |
| IO | DIFFIO_RX78n | | B5 | VREF0B5 | P4 | M2 | T3 | | | HIGH |
| IO | DIFFIO_RX78p | | B5 | VREF0B5 | N4 | M3 | T4 | | | HIGH |
| IO | DIFFIO_TX77n | | B5 | VREF0B5 | R7 | R7 | V6 | | | HIGH |
| IO | DIFFIO_TX77p | | B5 | VREF0B5 | T7 | R8 | V5 | | | HIGH |

**Table 6–1. Pin List for the Stratix EP1S60 Device (Part 36 of 78)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_RX77n | | B5 | VREF0B5 | M4 | L2 | R3 | | | HIGH |
| IO | DIFFIO_RX77p | | B5 | VREF0B5 | L4 | L3 | R4 | | | HIGH |
| IO | DIFFIO_TX76n | | B5 | VREF1B5 | P8 | P7 | U8 | | | HIGH |
| IO | DIFFIO_TX76p | | B5 | VREF1B5 | N8 | P8 | U7 | | | HIGH |
| IO | DIFFIO_RX76n/RDN5 | | B5 | VREF1B5 | K3 | M4 | P3 | | | HIGH |
| IO | DIFFIO_RX76p/RUP5 | | B5 | VREF1B5 | K4 | M5 | P4 | | | HIGH |
| IO | DIFFIO_TX75n | | B5 | VREF1B5 | R6 | R5 | U6 | | | HIGH |
| IO | DIFFIO_TX75p | | B5 | VREF1B5 | P6 | R6 | U5 | | | HIGH |
| IO | DIFFIO_RX75n | | B5 | VREF1B5 | J1 | L1 | R2 | | | HIGH |
| IO | DIFFIO_RX75p | | B5 | VREF1B5 | H1 | K2 | P1 | | | HIGH |
| IO | DIFFIO_TX74n | | B5 | VREF1B5 | P9 | R10 | T5 | | | HIGH |
| IO | DIFFIO_TX74p | | B5 | VREF1B5 | N9 | R9 | T6 | | | HIGH |
| IO | DIFFIO_RX74n | | B5 | VREF1B5 | G1 | J2 | P2 | | | HIGH |
| IO | DIFFIO_RX74p | | B5 | VREF1B5 | F1 | J1 | N2 | | | HIGH |
| IO | DIFFIO_TX73n | | B5 | VREF1B5 | P7 | P6 | T7 | | | HIGH |
| IO | DIFFIO_TX73p | | B5 | VREF1B5 | N7 | P5 | T8 | | | HIGH |
| IO | DIFFIO_RX73n | | B5 | VREF1B5 | H2 | K4 | N4 | | | HIGH |
| IO | DIFFIO_RX73p | | B5 | VREF1B5 | J2 | K3 | N3 | | | HIGH |
| IO | DIFFIO_TX72n | | B5 | VREF1B5 | N6 | N7 | T9 | | | HIGH |
| IO | DIFFIO_TX72p | | B5 | VREF1B5 | M6 | N8 | T10 | | | HIGH |
| IO | DIFFIO_RX72n | | B5 | VREF1B5 | G2 | J3 | M1 | | | HIGH |
| IO | DIFFIO_RX72p | | B5 | VREF1B5 | F2 | J4 | M2 | | | HIGH |

*Table 6–1. Pin List for the Stratix EP1S60 Device (Part 37 of 78)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| VREF1B5 | | | B5 | VREF1B5 | N10 | L8 | P11 | | | |
| IO | DIFFIO_TX71n | | B5 | VREF1B5 | R5 | P9 | R5 | | | HIGH |
| IO | DIFFIO_TX71p | | B5 | VREF1B5 | P5 | P10 | R6 | | | HIGH |
| IO | DIFFIO_RX71n | | B5 | VREF1B5 | J3 | H1 | M3 | | | HIGH |
| IO | DIFFIO_RX71p | | B5 | VREF1B5 | H3 | H2 | M4 | | | HIGH |
| IO | DIFFIO_TX70n | | B5 | VREF1B5 | M5 | N5 | R8 | | | HIGH |
| IO | DIFFIO_TX70p | | B5 | VREF1B5 | N5 | N6 | R7 | | | HIGH |
| IO | DIFFIO_RX70n | | B5 | VREF1B5 | G3 | G1 | L1 | | | HIGH |
| IO | DIFFIO_RX70p | | B5 | VREF1B5 | F3 | G2 | L2 | | | HIGH |
| IO | DIFFIO_TX69n | | B5 | VREF1B5 | M8 | N10 | P5 | | | HIGH |
| IO | DIFFIO_TX69p | | B5 | VREF1B5 | L8 | N9 | P6 | | | HIGH |
| IO | DIFFIO_RX69n | | B5 | VREF1B5 | J4 | H3 | L3 | | | HIGH |
| IO | DIFFIO_RX69p | | B5 | VREF1B5 | H4 | H4 | L4 | | | HIGH |
| IO | DIFFIO_TX68n | | B5 | VREF1B5 | M7 | M8 | P7 | | | HIGH |
| IO | DIFFIO_TX68p | | B5 | VREF1B5 | L7 | M9 | P8 | | | HIGH |
| IO | DIFFIO_RX68n | | B5 | VREF1B5 | G4 | F1 | K2 | | | HIGH |
| IO | DIFFIO_RX68p | | B5 | VREF1B5 | F4 | F2 | K1 | | | HIGH |
| IO | DIFFIO_TX67n | | B5 | VREF1B5 | L5 | M6 | N5 | | | HIGH |
| IO | DIFFIO_TX67p | | B5 | VREF1B5 | K5 | M7 | N6 | | | HIGH |
| IO | DIFFIO_RX67n | | B5 | VREF1B5 | E2 | G3 | K3 | | | HIGH |
| IO | DIFFIO_RX67p | | B5 | VREF1B5 | D2 | G4 | K4 | | | HIGH |
| IO | DIFFIO_TX66n | | B5 | VREF2B5 | H5 | L6 | N8 | | | HIGH |

**Table 6–1. Pin List for the Stratix EP1S60 Device (Part 38 of 78)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_TX66p | | B5 | VREF2B5 | J5 | L7 | N7 | | | HIGH |
| IO | DIFFIO_RX66n | | B5 | VREF2B5 | E3 | F3 | J3 | | | HIGH |
| IO | DIFFIO_RX66p | | B5 | VREF2B5 | D3 | F4 | J4 | | | HIGH |
| IO | DIFFIO_TX65n | | B5 | VREF2B5 | F5 | K5 | M6 | | | HIGH |
| IO | DIFFIO_TX65p | | B5 | VREF2B5 | G5 | K6 | M5 | | | HIGH |
| IO | DIFFIO_RX65n | | B5 | VREF2B5 | | E2 | H2 | | | LOW |
| IO | DIFFIO_RX65p | | B5 | VREF2B5 | | E1 | H1 | | | LOW |
| IO | DIFFIO_TX64n | | B5 | VREF2B5 | L6 | K8 | L5 | | | HIGH |
| IO | DIFFIO_TX64p | | B5 | VREF2B5 | K6 | K7 | L6 | | | HIGH |
| IO | DIFFIO_RX64n | | B5 | VREF2B5 | | F5 | G2 | | | LOW |
| IO | DIFFIO_RX64p | | B5 | VREF2B5 | | E4 | G1 | | | LOW |
| IO | DIFFIO_TX63n | | B5 | VREF2B5 | J6 | J5 | M7 | | | HIGH |
| IO | DIFFIO_TX63p | | B5 | VREF2B5 | H6 | J6 | M8 | | | HIGH |
| IO | DIFFIO_RX63n | | B5 | VREF2B5 | | | H3 | | | LOW |
| IO | DIFFIO_RX63p | | B5 | VREF2B5 | | | H4 | | | LOW |
| IO | DIFFIO_TX62n | | B5 | VREF2B5 | G6 | J7 | K5 | | | HIGH |
| IO | DIFFIO_TX62p | | B5 | VREF2B5 | F6 | J8 | K6 | | | HIGH |
| IO | DIFFIO_RX62n | | B5 | VREF2B5 | | | F1 | | | LOW |
| IO | DIFFIO_RX62p | | B5 | VREF2B5 | | | F2 | | | LOW |
| VREF2B5 | | | B5 | VREF2B5 | M10 | F6 | N11 | | | |
| IO | DIFFIO_TX61n | | B5 | VREF2B5 | K8 | H5 | L8 | | | HIGH |
| IO | DIFFIO_TX61p | | B5 | VREF2B5 | J8 | H6 | L7 | | | HIGH |

Table 6–1. Pin List for the Stratix EP1S60 Device (Part 39 of 78)

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DIFFIO_RX61n | | B5 | VREF2B5 | | | E1 | | | LOW |
| IO | DIFFIO_RX61p | | B5 | VREF2B5 | | | E2 | | | LOW |
| IO | DIFFIO_TX60n | | B5 | VREF2B5 | K7 | H8 | K7 | | | HIGH |
| IO | DIFFIO_TX60p | | B5 | VREF2B5 | J7 | H7 | K8 | | | HIGH |
| IO | DIFFIO_RX60n | | B5 | VREF2B5 | | | G4 | | | LOW |
| IO | DIFFIO_RX60p | | B5 | VREF2B5 | | | G3 | | | LOW |
| IO | DIFFIO_TX59n | | B5 | VREF2B5 | H7 | G6 | J7 | | | HIGH |
| IO | DIFFIO_TX59p | | B5 | VREF2B5 | G7 | G5 | J8 | | | HIGH |
| IO | DIFFIO_RX59n | | B5 | VREF2B5 | | | D1 | | | LOW |
| IO | DIFFIO_RX59p | | B5 | VREF2B5 | | | D2 | | | LOW |
| IO | DIFFIO_TX58n | | B5 | VREF2B5 | G8 | G7 | M9 | | | HIGH |
| IO | DIFFIO_TX58p | | B5 | VREF2B5 | H8 | G8 | M10 | | | HIGH |
| IO | DIFFIO_RX58n | | B5 | VREF2B5 | | | F3 | | | LOW |
| IO | DIFFIO_RX58p | | B5 | VREF2B5 | | | F4 | | | LOW |
| IO | | | B5 | VREF2B5 | | | N9 | | | |
| IO | | | B5 | VREF2B5 | | | N10 | | | |
| FPLL10CLKn | | | B5 | VREF2B5 | D1 | L5 | J1 | | | |
| FPLL10CLKp | | | B5 | VREF2B5 | E1 | L4 | J2 | | | |
| GNDG_PLL10 | | | | | K9 | E3 | L9 | | | |
| VCCG_PLL10 | | | | | J9 | D3 | L10 | | | |
| GNDA_PLL10 | | | | | M9 | D1 | K9 | | | |
| GND | | | | | | | | | | |

**Table 6–1. Pin List for the Stratix EP1S60 Device (Part 40 of 78)**

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed Note (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | | | |
| VCCA_PLL10 | | | | | L9 | D2 | J9 | | | |
| VCCINT | | | | | | | | | | |
| IO | | | B4 | VREF0B4 | C2 | F7 | B4 | | | |
| IO | | | B4 | VREF0B4 | | | D6 | | | |
| IO | | | B4 | VREF0B4 | | | D5 | | | |
| IO | | | B4 | VREF0B4 | | | G8 | | | |
| IO | | | B4 | VREF0B4 | | | E5 | | | |
| IO | | | B4 | VREF0B4 | | | C4 | | | |
| IO | | | B4 | VREF0B4 | D4 | F8 | J10 | | | |
| IO | DQ0T0 | | B4 | VREF0B4 | C4 | D5 | C6 | DQ0T0 | DQ0T0 | |
| IO | | | B4 | VREF0B4 | | K9 | F7 | | | |
| IO | DQ0T1 | | B4 | VREF0B4 | C5 | C3 | B6 | DQ0T1 | DQ0T1 | |
| IO | | | B4 | VREF0B4 | E4 | L9 | G7 | | | |
| IO | DQ0T2 | | B4 | VREF0B4 | D5 | E5 | C7 | DQ0T2 | DQ0T2 | |
| IO | | | B4 | VREF0B4 | H9 | F9 | F8 | | | |
| IO | DQS0T | | B4 | VREF0B4 | B4 | C5 | B7 | | | |
| IO | | | B4 | VREF0B4 | E5 | M10 | C5 | | | |
| IO | DQ0T3 | | B4 | VREF0B4 | B5 | C4 | A7 | DQ0T3 | DQ0T3 | |
| IO | | | B4 | VREF0B4 | | | E6 | | | |
| IO | DQ0T4 | | B4 | VREF0B4 | B3 | D4 | C8 | DQ0T4 | DQ0T4 | |
| VREF0B4 | | | B4 | VREF0B4 | K10 | E6 | L11 | | | |
| IO | | | B4 | VREF0B4 | E7 | G9 | G9 | | | |

Table 6–1. Pin List for the Stratix EP1S60 Device (Part 41 of 78)

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DQ0T5 | | B4 | VREF0B4 | C3 | A4 | A6 | DQ0T5 | DQ0T5 | |
| IO | | | B4 | VREF0B4 | F7 | H9 | E7 | | | |
| IO | DQ0T6 | | B4 | VREF0B4 | A5 | B4 | A8 | DQ0T6 | DQ0T6 | |
| IO | | | B4 | VREF0B4 | | J9 | H9 | | | |
| IO | DQ0T7 | | B4 | VREF0B4 | A4 | B3 | B8 | DQ0T7 | DQ0T7 | |
| IO | | | B4 | VREF0B4 | F8 | F10 | J11 | | | |
| IO | | | B4 | VREF0B4 | | | K12 | | | |
| IO | | | B4 | VREF0B4 | | | A4 | | | |
| IO | | | B4 | VREF0B4 | | | D7 | | | |
| IO | | | B4 | VREF0B4 | | | K11 | | | |
| IO | DQ1T0 | | B4 | VREF0B4 | E6 | D6 | C9 | DQ0T8 | DQ0T8 | |
| IO | | | B4 | VREF1B4 | | G10 | F9 | | | |
| IO | DQ1T1 | | B4 | VREF1B4 | C7 | C6 | B9 | DQ0T9 | DQ0T9 | |
| IO | | | B4 | VREF1B4 | J10 | L10 | E8 | | | |
| IO | DQ1T2 | | B4 | VREF1B4 | D7 | B5 | A9 | DQ0T10 | DQ0T10 | |
| IO | | | B4 | VREF1B4 | | | B5 | | | |
| IO | DQS1T | | B4 | VREF1B4 | C6 | E7 | B10 | DQS0T | | |
| IO | | | B4 | VREF1B4 | G10 | F11 | D8 | | | |
| IO | DQ1T3 | | B4 | VREF1B4 | A6 | C7 | C11 | DQ0T11 | DQ0T11 | |
| IO | | | B4 | VREF1B4 | J11 | H10 | H11 | | | |
| IO | DQ1T4 | | B4 | VREF1B4 | B6 | A5 | A10 | DQ0T12 | DQ0T12 | |
| IO | | | B4 | VREF1B4 | G9 | J10 | A5 | | | |

*Table 6–1. Pin List for the Stratix EP1S60 Device (Part 42 of 78)*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **956-Pin BGA** | **1020-Pin FineLine BGA** | **1508-Pin FineLine BGA** | | | |
| IO | DQ1T5 | | B4 | VREF1B4 | D6 | D7 | C10 | DQ0T13 | DQ0T13 | |
| IO | | | B4 | VREF1B4 | | G11 | G11 | | | |
| IO | DQ1T6 | | B4 | VREF1B4 | A7 | A6 | A11 | DQ0T14 | DQ0T14 | |
| IO | | | B4 | VREF1B4 | F9 | K10 | K13 | | | |
| IO | DQ1T7 | | B4 | VREF1B4 | B7 | B6 | B11 | DQ0T15 | DQ0T15 | |
| IO | | | B4 | VREF1B4 | H10 | M11 | G10 | | | |
| IO | | | B4 | VREF1B4 | | | J12 | | | |
| VREF1B4 | | | B4 | VREF1B4 | K11 | E8 | L12 | | | |
| IO | | | B4 | VREF1B4 | | | E10 | | | |
| IO | | | B4 | VREF1B4 | | | G12 | | | |
| IO | | | B4 | VREF1B4 | | | F10 | | | |
| IO | DQ2T0 | | B4 | VREF1B4 | B8 | B7 | A12 | DQ1T0 | DQ0T16 | |
| IO | | | B4 | VREF1B4 | | L11 | M14 | | | |
| IO | DQ2T1 | | B4 | VREF1B4 | D9 | D8 | D12 | DQ1T1 | DQ0T17 | |
| IO | | | B4 | VREF1B4 | E9 | F12 | K14 | | | |
| IO | DQ2T2 | | B4 | VREF1B4 | E8 | B8 | E12 | DQ1T2 | DQ0T18 | |
| IO | | | B4 | VREF1B4 | H11 | H11 | D9 | | | |
| IO | DQS2T | | B4 | VREF1B4 | C8 | A7 | C12 | | DQS0T | |
| IO | | | B4 | VREF1B4 | L11 | K11 | E9 | | | |
| IO | DQ2T3 | | B4 | VREF1B4 | C9 | E9 | E13 | DQ1T3 | DQ0T19 | |
| IO | | | B4 | VREF1B4 | | | H13 | | | |
| IO | DQ2T4 | | B4 | VREF1B4 | D8 | A8 | B12 | DQ1T4 | DQ0T20 | |

**Table 6–1. Pin List for the Stratix EP1S60 Device (Part 43 of 78)**

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | | | |
| IO | | | B4 | VREF1B4 | J12 | L12 | F11 | | | |
| IO | DQ2T5 | | B4 | VREF1B4 | A9 | C9 | B13 | DQ1T5 | DQ0T21 | |
| IO | | | B4 | VREF1B4 | | J11 | H12 | | | |
| IO | DQ2T6 | | B4 | VREF1B4 | B9 | C8 | C13 | DQ1T6 | DQ0T22 | |
| IO | FCLK6 | | B4 | VREF2B4 | F10 | G12 | D11 | | | |
| IO | FCLK7 | | B4 | VREF2B4 | F11 | A14 | G14 | | | |
| IO | DQ2T7 | | B4 | VREF2B4 | A8 | D9 | D13 | DQ1T7 | DQ0T23 | |
| IO | | | B4 | VREF2B4 | | | J14 | | | |
| IO | | | B4 | VREF2B4 | | | J13 | | | |
| IO | | | B4 | VREF2B4 | | | D10 | | | |
| IO | | | B4 | VREF2B4 | | | G13 | | | |
| IO | DQ3T0 | | B4 | VREF2B4 | B10 | E11 | C14 | DQ1T8 | DQ0T24 | |
| IO | | | B4 | VREF2B4 | | H12 | F12 | | | |
| IO | DQ3T1 | | B4 | VREF2B4 | D10 | B9 | D14 | DQ1T9 | DQ0T25 | |
| IO | | | B4 | VREF2B4 | L12 | K12 | M15 | | | |
| IO | DQ3T2 | | B4 | VREF2B4 | E10 | D10 | E14 | DQ1T10 | DQ0T26 | |
| IO | | | B4 | VREF2B4 | H12 | B14 | H14 | | | |
| IO | DQS3T | | B4 | VREF2B4 | C10 | D11 | C15 | DQS1T | | |
| IO | | | B4 | VREF2B4 | G11 | J12 | K15 | | | |
| IO | DQ3T3 | | B4 | VREF2B4 | D11 | C10 | A14 | DQ1T11 | DQ0T27 | |
| IO | | | B4 | VREF2B4 | | | E11 | | | |
| IO | DQ3T4 | | B4 | VREF2B4 | E11 | A9 | B14 | DQ1T12 | DQ0T28 | |

*Table 6–1. Pin List for the Stratix EP1S60 Device (Part 44 of 78)*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | | | |
| VREF2B4 | | | B4 | VREF2B4 | K12 | E10 | L13 | | | |
| IO | | | B4 | VREF2B4 | G12 | C14 | J15 | | | |
| IO | DQ3T5 | | B4 | VREF2B4 | B11 | B11 | B15 | DQ1T13 | DQ0T29 | |
| IO | | | B4 | VREF2B4 | | K13 | F13 | | | |
| IO | DQ3T6 | | B4 | VREF2B4 | C11 | C11 | E15 | DQ1T14 | DQ0T30 | |
| IO | DEV_OE | | B4 | VREF2B4 | F12 | L13 | P16 | | | |
| IO | DQ3T7 | | B4 | VREF2B4 | A10 | B10 | D15 | DQ1T15 | DQ0T31 | |
| IO | RUP4 | | B4 | VREF2B4 | F13 | G13 | F15 | | | |
| IO | | | B4 | VREF2B4 | H13 | F13 | G15 | | | |
| IO | | | B4 | VREF2B4 | | | L16 | | | |
| IO | | | B4 | VREF2B4 | | | F14 | | | |
| IO | RDN4 | | B4 | VREF2B4 | E14 | J13 | E16 | | | |
| IO | DQ4T0 | | B4 | VREF2B4 | D12 | A11 | A16 | | | |
| IO | | nWS | B4 | VREF2B4 | F14 | D14 | F16 | | | |
| IO | DQ4T1 | | B4 | VREF2B4 | E12 | B12 | D16 | | | |
| IO | | | B4 | VREF2B4 | | | H15 | | | |
| IO | DQ4T2 | | B4 | VREF2B4 | A12 | C12 | A17 | | | |
| IO | | | B4 | VREF2B4 | J13 | H13 | M16 | | | |
| IO | DQS4T | | B4 | VREF2B4 | C12 | D12 | C16 | | | |
| IO | | DATA0 | B4 | VREF3B4 | E15 | E14 | M17 | | | |
| IO | DQ4T3 | | B4 | VREF3B4 | B12 | C13 | B16 | | | |
| IO | | | B4 | VREF3B4 | G13 | K14 | J16 | | | |

**Table 6–1. Pin List for the Stratix EP1S60 Device (Part 45 of 78)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| IO | DQ4T4 | | B4 | VREF3B4 | C13 | D13 | B17 | | | |
| IO | | | B4 | VREF3B4 | L14 | L14 | K16 | | | |
| IO | DQ4T5 | | B4 | VREF3B4 | D13 | E13 | D17 | | | |
| IO | | DATA1 | B4 | VREF3B4 | C16 | F14 | J17 | | | |
| IO | DQ4T6 | | B4 | VREF3B4 | E13 | A13 | E17 | | | |
| IO | | | B4 | VREF3B4 | | H14 | L17 | | | |
| IO | DQ4T7 | | B4 | VREF3B4 | B13 | B13 | C17 | | | |
| IO | | | B4 | VREF3B4 | L16 | J14 | H16 | | | |
| IO | | | B4 | VREF3B4 | | | G16 | | | |
| IO | | | B4 | VREF3B4 | | | G17 | | | |
| IO | | | B4 | VREF3B4 | | | E18 | | | |
| IO | | | B4 | VREF3B4 | | | H17 | | | |
| IO | | | B4 | VREF3B4 | G14 | L15 | F18 | | | |
| IO | | | B4 | VREF3B4 | | | K17 | | | |
| IO | | | B4 | VREF3B4 | | | F17 | | | |
| VREF3B4 | | | B4 | VREF3B4 | K13 | E12 | L14 | | | |
| IO | | | B4 | VREF3B4 | | | G18 | | | |
| IO | | | B4 | VREF3B4 | | | J18 | | | |
| IO | | | B4 | VREF3B4 | | | H18 | | | |
| IO | | DATA2 | B4 | VREF3B4 | F15 | F15 | K18 | | | |
| IO | | | B4 | VREF3B4 | | | L18 | | | |
| IO | | | B4 | VREF3B4 | | | M18 | | | |

**Table 6–1. Pin List for the Stratix EP1S60 Device (Part 46 of 78)**

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | | | |
| TMS | | TMS | B4 | VREF3B4 | D16 | E15 | F19 | | | |
| TRST | | TRST | B4 | VREF3B4 | G15 | G15 | H19 | | | |
| TCK | | TCK | B4 | VREF3B4 | F16 | G14 | E20 | | | |
| IO | | DATA3 | B4 | VREF3B4 | G17 | C16 | P21 | | | |
| IO | | | B4 | VREF3B4 | | J15 | D18 | | | |
| IO | | | B4 | VREF3B4 | | K15 | C18 | | | |
| TDI | | TDI | B4 | VREF3B4 | E16 | D16 | F20 | | | |
| TDO | | TDO | B4 | VREF3B4 | G16 | F16 | G20 | | | |
| IO | CLK12n | | B4 | VREF3B4 | B14 | A15 | A18 | | | |
| CLK12p | | | B4 | VREF3B4 | A14 | B15 | B18 | | | |
| IO | CLK13n/PLL11_OUT | | B4 | VREF3B4 | D14 | C15 | C19 | | | |
| CLK13p | | | B4 | VREF3B4 | C14 | D15 | D19 | | | |
| VCCINT | | | | | | | | | | |
| VCCA_PLL11 | | | | | J14 | E16 | K19 | | | |
| GND | | | | | | | | | | |
| GNDA_PLL11 | | | | | H14 | E17 | J19 | | | |
| VCCG_PLL11 | | | | | H15 | H16 | L19 | | | |
| GNDG_PLL11 | | | | | J15 | H15 | M19 | | | |
| TEMPDIODEp | | | | | E17 | E18 | F21 | | | |
| TEMPDIODEn | | | | | F17 | F18 | H21 | | | |
| VCCINT | | | | | | | | | | |
| VCCA_PLL5 | | | | | J17 | G17 | L21 | | | |

*Table 6–1. Pin List for the Stratix EP1S60 Device (Part 47 of 78)*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | | | |
| GND | | | | | | | | | | |
| GNDA_PLL5 | | | | | H16 | F17 | M21 | | | |
| VCCG_PLL5 | | | | | K15 | J16 | L20 | | | |
| GNDG_PLL5 | | | | | K17 | L16 | M20 | | | |
| VCC_PLL5_OUTA | | | B9 | | L18 | H17 | J20 | | | |
| VCC_PLL5_OUTA | | | B9 | | | | | | | |
| VCC_PLL5_OUTB | | | B10 | | J18 | L17 | K21 | | | |
| VCC_PLL5_OUTB | | | B10 | | | | | | | |
| IO | PLL5_OUT0p | | B9 | VREF0B3 | B16 | B16 | C21 | | | |
| IO | PLL5_OUT0n | | B9 | VREF0B3 | A16 | A16 | D21 | | | |
| IO | PLL5_OUT1p | | B9 | VREF0B3 | B15 | B17 | C20 | | | |
| IO | PLL5_OUT1n | | B9 | VREF0B3 | A15 | A17 | D20 | | | |
| IO | PLL5_FBp | | B9 | VREF0B3 | D15 | D17 | B19 | | | |
| IO | PLL5_FBn | | B9 | VREF0B3 | C15 | C17 | A19 | | | |
| IO | PLL5_OUT2p | | B10 | VREF0B3 | D17 | B18 | B21 | | | |
| IO | PLL5_OUT2n | | B10 | VREF0B3 | C17 | A18 | A21 | | | |
| IO | PLL5_OUT3p | | B10 | VREF0B3 | B17 | D18 | A20 | | | |
| IO | PLL5_OUT3n | | B10 | VREF0B3 | A17 | C18 | B20 | | | |
| nSTATUS | | nSTATUS | B3 | VREF0B3 | E18 | G16 | N21 | | | |
| nCONFIG | | nCONFIG | B3 | VREF0B3 | F19 | J18 | L22 | | | |
| DCLK | | DCLK | B3 | VREF0B3 | F18 | E19 | G21 | | | |
| CONF_DONE | | CONF_DONE | B3 | VREF0B3 | G18 | G18 | H22 | | | |

*Table 6–1. Pin List for the Stratix EP1S60 Device (Part 48 of 78)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **956-Pin BGA** | **1020-Pin FineLine BGA** | **1508-Pin FineLine BGA** | **DQS for x16** | **DQS for x32** | **DIFFIO Speed** *Note (1)* |
| CLK14p | | | B3 | VREF0B3 | A18 | A19 | B22 | | | |
| IO | CLK14n | | B3 | VREF0B3 | B18 | B19 | A22 | | | |
| CLK15p | | | B3 | VREF0B3 | C18 | C19 | D22 | | | |
| IO | CLK15n | | B3 | VREF0B3 | D18 | D19 | C22 | | | |
| VREF0B3 | | | B3 | VREF0B3 | K18 | E21 | L25 | | | |
| IO | | | B3 | VREF0B3 | | | G22 | | | |
| IO | | | B3 | VREF0B3 | | | E22 | | | |
| IO | | | B3 | VREF0B3 | | | E21 | | | |
| IO | | | B3 | VREF0B3 | | | F22 | | | |
| IO | | | B3 | VREF0B3 | | | J22 | | | |
| IO | | | B3 | VREF0B3 | L19 | K18 | N22 | | | |
| IO | | DATA4 | B3 | VREF0B3 | G19 | G19 | L23 | | | |
| IO | | | B3 | VREF0B3 | | | H23 | | | |
| IO | DQ5T0 | | B3 | VREF0B3 | B19 | A20 | B23 | | | |
| IO | | | B3 | VREF0B3 | H19 | H19 | K23 | | | |
| IO | DQ5T1 | | B3 | VREF0B3 | C19 | B20 | E23 | | | |
| IO | | DATA5 | B3 | VREF0B3 | F20 | J19 | J23 | | | |
| IO | DQ5T2 | | B3 | VREF1B3 | D19 | C20 | D23 | | | |
| IO | | | B3 | VREF1B3 | | F19 | F23 | | | |
| IO | DQS5T | | B3 | VREF1B3 | C20 | D20 | C23 | | | |
| IO | | | B3 | VREF1B3 | G21 | L18 | G23 | | | |
| IO | DQ5T3 | | B3 | VREF1B3 | E19 | E20 | A23 | | | |

**Table 6–1. Pin List for the Stratix EP1S60 Device (Part 49 of 78)**

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | | | |
| IO | | DATA6 | B3 | VREF1B3 | F21 | K19 | E24 | | | |
| IO | DQ5T4 | | B3 | VREF1B3 | A20 | B21 | A24 | | | |
| IO | | | B3 | VREF1B3 | | F20 | F24 | | | |
| IO | DQ5T5 | | B3 | VREF1B3 | B20 | C21 | B24 | | | |
| IO | | | B3 | VREF1B3 | J19 | G20 | G24 | | | |
| IO | DQ5T6 | | B3 | VREF1B3 | D20 | D21 | C24 | | | |
| IO | | | B3 | VREF1B3 | | | N23 | | | |
| IO | DQ5T7 | | B3 | VREF1B3 | E20 | A22 | D24 | | | |
| IO | RUP3 | | B3 | VREF1B3 | F22 | F21 | P23 | | | |
| IO | | | B3 | VREF1B3 | | | H24 | | | |
| IO | | | B3 | VREF1B3 | | | K24 | | | |
| IO | | | B3 | VREF1B3 | H21 | H20 | J24 | | | |
| IO | RDN3 | | B3 | VREF1B3 | F24 | L19 | M24 | | | |
| VREF1B3 | | | B3 | VREF1B3 | K19 | E23 | L26 | | | |
| IO | DQ6T0 | | B3 | VREF1B3 | B21 | B22 | B25 | DQ2T0 | DQ1T0 | |
| IO | | | B3 | VREF1B3 | | | F25 | | | |
| IO | DQ6T1 | | B3 | VREF1B3 | C21 | C22 | E25 | DQ2T1 | DQ1T1 | |
| IO | | DATA7 | B3 | VREF1B3 | G20 | J20 | P25 | | | |
| IO | DQ6T2 | | B3 | VREF1B3 | A22 | B23 | D25 | DQ2T2 | DQ1T2 | |
| IO | | | B3 | VREF1B3 | | K20 | L24 | | | |
| IO | DQS6T | | B3 | VREF1B3 | C22 | D22 | C25 | DQS2T | | |
| IO | | | B3 | VREF1B3 | H20 | G21 | G25 | | | |

Table 6–1. Pin List for the Stratix EP1S60 Device (Part 50 of 78)

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed Note (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | | | |
| IO | DQ6T3 | | B3 | VREF1B3 | D21 | C23 | A26 | DQ2T3 | DQ1T3 | |
| IO | | CLKUSR | B3 | VREF1B3 | F23 | H21 | J25 | | | |
| IO | DQ6T4 | | B3 | VREF1B3 | E21 | A24 | B26 | DQ2T4 | DQ1T4 | |
| IO | | | B3 | VREF1B3 | | L20 | H25 | | | |
| IO | DQ6T5 | | B3 | VREF1B3 | B22 | E22 | C26 | DQ2T5 | DQ1T5 | |
| IO | | | B3 | VREF1B3 | | | F26 | | | |
| IO | DQ6T6 | | B3 | VREF1B3 | D22 | B24 | D26 | DQ2T6 | DQ1T6 | |
| IO | | | B3 | VREF1B3 | J20 | J21 | K25 | | | |
| IO | DQ6T7 | | B3 | VREF1B3 | E22 | D23 | E26 | DQ2T7 | DQ1T7 | |
| IO | | | B3 | VREF1B3 | | | F27 | | | |
| IO | FCLK0 | | B3 | VREF2B3 | E23 | F22 | G26 | | | |
| IO | FCLK1 | | B3 | VREF2B3 | E25 | G22 | D29 | | | |
| IO | | | B3 | VREF2B3 | | | H26 | | | |
| IO | | | B3 | VREF2B3 | | | J26 | | | |
| IO | DQ7T0 | | B3 | VREF2B3 | A23 | D24 | B27 | DQ2T8 | DQ1T8 | |
| IO | | | B3 | VREF2B3 | L21 | K21 | F28 | | | |
| IO | DQ7T1 | | B3 | VREF2B3 | B23 | A25 | C27 | DQ2T9 | DQ1T9 | |
| IO | | | B3 | VREF2B3 | | | G27 | | | |
| IO | DQ7T2 | | B3 | VREF2B3 | A24 | C24 | D27 | DQ2T10 | DQ1T10 | |
| IO | | | B3 | VREF2B3 | | L21 | H27 | | | |
| IO | DQS7T | | B3 | VREF2B3 | C24 | B26 | C28 | | DQS1T | |
| IO | | | B3 | VREF2B3 | | | J27 | | | |

Table 6–1. Pin List for the Stratix EP1S60 Device (Part 51 of 78)

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed Note (1) |
| IO | DQ7T3 | | B3 | VREF2B3 | C23 | B25 | E27 | DQ2T11 | DQ1T11 | |
| IO | | | B3 | VREF2B3 | | H22 | K26 | | | |
| IO | DQ7T4 | | B3 | VREF2B3 | D24 | C25 | B28 | DQ2T12 | DQ1T12 | |
| IO | | | B3 | VREF2B3 | | | E29 | | | |
| IO | DQ7T5 | | B3 | VREF2B3 | B24 | D25 | A28 | DQ2T13 | DQ1T13 | |
| IO | | | B3 | VREF2B3 | | J22 | D31 | | | |
| VREF2B3 | | | B3 | VREF2B3 | K20 | E25 | L27 | | | |
| IO | DQ7T6 | | B3 | VREF2B3 | D23 | A26 | D28 | DQ2T14 | DQ1T14 | |
| IO | | | B3 | VREF2B3 | | | D30 | | | |
| IO | DQ7T7 | | B3 | VREF2B3 | E24 | E24 | E28 | DQ2T15 | DQ1T15 | |
| IO | | | B3 | VREF2B3 | | | E30 | | | |
| IO | | | B3 | VREF2B3 | | | H28 | | | |
| IO | | | B3 | VREF2B3 | | | K27 | | | |
| IO | | | B3 | VREF2B3 | | | G28 | | | |
| IO | | | B3 | VREF2B3 | G22 | F23 | F29 | | | |
| IO | DQ8T0 | | B3 | VREF2B3 | A25 | C26 | A29 | DQ3T0 | DQ1T16 | |
| IO | | | B3 | VREF2B3 | J21 | K22 | F30 | | | |
| IO | DQ8T1 | | B3 | VREF2B3 | C25 | A28 | B29 | DQ3T1 | DQ1T17 | |
| IO | | | B3 | VREF2B3 | | | E31 | | | |
| IO | DQ8T2 | | B3 | VREF2B3 | B25 | A27 | C29 | DQ3T2 | DQ1T18 | |
| IO | | | B3 | VREF2B3 | H22 | G23 | G29 | | | |
| IO | DQS8T | | B3 | VREF2B3 | C26 | B27 | B30 | DQS3T | | |

*Table 6–1. Pin List for the Stratix EP1S60 Device (Part 52 of 78)*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | | | |
| IO | | | B3 | VREF2B3 | | L22 | J28 | | | |
| IO | DQ8T3 | | B3 | VREF2B3 | D25 | D26 | C30 | DQ3T3 | DQ1T19 | |
| IO | | | B3 | VREF2B3 | | | H29 | | | |
| GND | | | B3 | | | | | | | |
| GND | | | B3 | | | | | | | |
| GND | | | B3 | | D28 | H24 | E32 | | | |
| IO | DQ8T4 | | B3 | VREF3B3 | A26 | C27 | A30 | DQ3T4 | DQ1T20 | |
| IO | | | B3 | VREF3B3 | G23 | F24 | D32 | | | |
| IO | DQ8T5 | | B3 | VREF3B3 | B26 | B28 | A31 | DQ3T5 | DQ1T21 | |
| IO | | | B3 | VREF3B3 | | H23 | K28 | | | |
| IO | DQ8T6 | | B3 | VREF3B3 | E26 | D27 | B31 | DQ3T6 | DQ1T22 | |
| IO | | | B3 | VREF3B3 | | | J29 | | | |
| IO | DQ8T7 | | B3 | VREF3B3 | D26 | E26 | C31 | DQ3T7 | DQ1T23 | |
| IO | | | B3 | VREF3B3 | | | G30 | | | |
| IO | | | B3 | VREF3B3 | | | F31 | | | |
| IO | | | B3 | VREF3B3 | | | D33 | | | |
| IO | | | B3 | VREF3B3 | | | G31 | | | |
| IO | | | B3 | VREF3B3 | J22 | K23 | K29 | | | |
| IO | DQ9T0 | | B3 | VREF3B3 | B27 | A29 | A32 | DQ3T8 | DQ1T24 | |
| IO | | | B3 | VREF3B3 | | | A35 | | | |
| IO | DQ9T1 | | B3 | VREF3B3 | C27 | B29 | C32 | DQ3T9 | DQ1T25 | |
| IO | | | B3 | VREF3B3 | H23 | J23 | F32 | | | |

*Table 6–1. Pin List for the Stratix EP1S60 Device (Part 53 of 78)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **956-Pin BGA** | **1020-Pin FineLine BGA** | **1508-Pin FineLine BGA** | **DQS for x16** | **DQS for x32** | **DIFFIO Speed** *Note (1)* |
| IO | DQ9T2 | | B3 | VREF3B3 | A27 | B30 | B32 | DQ3T10 | DQ1T26 | |
| IO | | | B3 | VREF3B3 | F25 | J24 | C35 | | | |
| VREF3B3 | | | B3 | VREF3B3 | K21 | E27 | L28 | | | |
| IO | DQS9T | | B3 | VREF3B3 | B28 | C28 | B33 | | | |
| IO | | | B3 | VREF3B3 | | F25 | B35 | | | |
| IO | DQ9T3 | | B3 | VREF3B3 | D27 | C29 | A34 | DQ3T11 | DQ1T27 | |
| IO | | | B3 | VREF3B3 | | G24 | D34 | | | |
| IO | DQ9T4 | | B3 | VREF3B3 | A28 | D29 | A33 | DQ3T12 | DQ1T28 | |
| IO | | | B3 | VREF3B3 | E27 | L23 | E34 | | | |
| IO | DQ9T5 | | B3 | VREF3B3 | C28 | D28 | C33 | DQ3T13 | DQ1T29 | |
| IO | | | B3 | VREF3B3 | | F26 | E33 | | | |
| IO | DQ9T6 | | B3 | VREF3B3 | C29 | C30 | C34 | DQ3T14 | DQ1T30 | |
| IO | | | B3 | VREF3B3 | | | F33 | | | |
| IO | DQ9T7 | | B3 | VREF3B3 | B29 | E28 | B34 | DQ3T15 | DQ1T31 | |
| IO | | | B3 | VREF3B3 | C30 | K24 | G33 | | | |
| IO | | | B3 | VREF3B3 | | | A36 | | | |
| IO | | | B3 | VREF3B3 | | | B36 | | | |
| IO | | | B3 | VREF3B3 | | | G32 | | | |
| IO | | | B3 | VREF3B3 | | | D35 | | | |
| IO | | | B3 | VREF3B3 | | | C36 | | | |
| IO | | | B3 | VREF3B3 | E28 | L24 | E35 | | | |
| VCCIO2 | | | | | C31 | C31 | C39 | | | |

**Table 6–1. Pin List for the Stratix EP1S60 Device (Part 54 of 78)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| VCCIO2 | | | | | N31 | C32 | R39 | | | |
| VCCIO2 | | | | | T23 | M32 | W35 | | | |
| VCCIO2 | | | | | | T23 | V25 | | | |
| VCCIO2 | | | | | | | H33 | | | |
| VCCIO2 | | | | | | | | | | |
| VCCIO2 | | | | | | | | | | |
| VCCIO2 | | | | | | | | | | |
| VCCIO2 | | | | | | | | | | |
| VCCIO2 | | | | | | | | | | |
| VCCIO2 | | | | | | | | | | |
| VCCIO2 | | | | | | | | | | |
| VCCIO2 | | | | | | | | | | |
| VCCIO2 | | | | | | | | | | |
| VCCIO2 | | | | | | | | | | |
| VCCIO2 | | | | | | | | | | |
| VCCIO1 | | | | | U20 | AA32 | AA25 | | | |
| VCCIO1 | | | | | W31 | AK31 | Y32 | | | |
| VCCIO1 | | | | | AJ31 | AK32 | AE39 | | | |
| VCCIO1 | | | | | | U23 | AU39 | | | |
| VCCIO1 | | | | | | | AM33 | | | |
| VCCIO1 | | | | | | | | | | |
| VCCIO1 | | | | | | | | | | |

**Table 6–1. Pin List for the Stratix EP1S60 Device (Part 55 of 78)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| VCCIO1 | | | | | | | | | | |
| VCCIO1 | | | | | | | | | | |
| VCCIO1 | | | | | | | | | | |
| VCCIO1 | | | | | | | | | | |
| VCCIO1 | | | | | | | | | | |
| VCCIO1 | | | | | | | | | | |
| VCCIO1 | | | | | | | | | | |
| VCCIO1 | | | | | | | | | | |
| VCCIO1 | | | | | | | | | | |
| VCCIO8 | | | | | AL29 | AC17 | AW37 | | | |
| VCCIO8 | | | | | AL19 | AM21 | AW25 | | | |
| VCCIO8 | | | | | Y17 | AM30 | AR21 | | | |
| VCCIO8 | | | | | | | AE22 | | | |
| VCCIO8 | | | | | | | AM30 | | | |
| VCCIO8 | | | | | | | | | | |
| VCCIO8 | | | | | | | | | | |
| VCCIO8 | | | | | | | | | | |
| VCCIO8 | | | | | | | | | | |
| VCCIO8 | | | | | | | | | | |
| VCCIO8 | | | | | | | | | | |
| VCCIO8 | | | | | | | | | | |
| VCCIO8 | | | | | | | | | | |

Table 6–1. Pin List for the Stratix EP1S60 Device (Part 56 of 78)

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| VCCIO8 | | | | | | | | | | |
| VCCIO7 | | | | | AC16 | AC16 | AE19 | | | |
| VCCIO7 | | | | | AL13 | AM12 | AM20 | | | |
| VCCIO7 | | | | | AL3 | AM3 | AW15 | | | |
| VCCIO7 | | | | | | | AW3 | | | |
| VCCIO7 | | | | | | | AM10 | | | |
| VCCIO7 | | | | | | | | | | |
| VCCIO7 | | | | | | | | | | |
| VCCIO7 | | | | | | | | | | |
| VCCIO7 | | | | | | | | | | |
| VCCIO7 | | | | | | | | | | |
| VCCIO7 | | | | | | | | | | |
| VCCIO7 | | | | | | | | | | |
| VCCIO7 | | | | | | | | | | |
| VCCIO6 | | | | | AJ1 | AA1 | AU1 | | | |
| VCCIO6 | | | | | W1 | AK1 | AM7 | | | |
| VCCIO6 | | | | | U12 | AK2 | AE1 | | | |
| VCCIO6 | | | | | | U10 | AA5 | | | |
| VCCIO6 | | | | | | | AB15 | | | |
| VCCIO6 | | | | | | | | | | |
| VCCIO6 | | | | | | | | | | |
| VCCIO6 | | | | | | | | | | |

***Table 6–1. Pin List for the Stratix EP1S60 Device  (Part 57 of 78)***

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| VCCIO6 | | | | | | | | | | |
| VCCIO6 | | | | | | | | | | |
| VCCIO6 | | | | | | | | | | |
| VCCIO6 | | | | | | | | | | |
| VCCIO6 | | | | | | | | | | |
| VCCIO6 | | | | | | | | | | |
| VCCIO6 | | | | | | | | | | |
| VCCIO6 | | | | | | | | | | |
| VCCIO5 | | | | | T9 | C1 | W15 | | | |
| VCCIO5 | | | | | N1 | C2 | Y8 | | | |
| VCCIO5 | | | | | C1 | M1 | R1 | | | |
| VCCIO5 | | | | | | T10 | H7 | | | |
| VCCIO5 | | | | | | | C1 | | | |
| VCCIO5 | | | | | | | | | | |
| VCCIO5 | | | | | | | | | | |
| VCCIO5 | | | | | | | | | | |
| VCCIO5 | | | | | | | | | | |
| VCCIO5 | | | | | | | | | | |
| VCCIO5 | | | | | | | | | | |
| VCCIO5 | | | | | | | | | | |
| VCCIO5 | | | | | | | | | | |
| VCCIO5 | | | | | | | | | | |

**Table 6–1. Pin List for the Stratix EP1S60 Device (Part 58 of 78)**

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | | | |
| VCCIO5 | | | | | | | | | | |
| VCCIO5 | | | | | | | | | | |
| VCCIO4 | | | | | A3 | A12 | A3 | | | |
| VCCIO4 | | | | | A13 | A3 | A15 | | | |
| VCCIO4 | | | | | J16 | K16 | E19 | | | |
| VCCIO4 | | | | | | | R18 | | | |
| VCCIO4 | | | | | | | H10 | | | |
| VCCIO4 | | | | | | | | | | |
| VCCIO4 | | | | | | | | | | |
| VCCIO4 | | | | | | | | | | |
| VCCIO4 | | | | | | | | | | |
| VCCIO4 | | | | | | | | | | |
| VCCIO4 | | | | | | | | | | |
| VCCIO4 | | | | | | | | | | |
| VCCIO4 | | | | | | | | | | |
| VCCIO3 | | | | | M17 | A21 | H20 | | | |
| VCCIO3 | | | | | A19 | A30 | R21 | | | |
| VCCIO3 | | | | | A29 | K17 | A25 | | | |
| VCCIO3 | | | | | | | A37 | | | |
| VCCIO3 | | | | | | | H30 | | | |
| VCCIO3 | | | | | | | | | | |
| VCCIO3 | | | | | | | | | | |

**Table 6–1. Pin List for the Stratix EP1S60 Device (Part 59 of 78)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| VCCIO3 | | | | | | | | | | |
| VCCIO3 | | | | | | | | | | |
| VCCIO3 | | | | | | | | | | |
| VCCIO3 | | | | | | | | | | |
| VCCIO3 | | | | | | | | | | |
| VCCIO3 | | | | | | | | | | |
| VCCIO3 | | | | | | | | | | |
| VCCINT | | | | | M11 | M12 | R16 | | | |
| VCCINT | | | | | M13 | M14 | R20 | | | |
| VCCINT | | | | | M15 | M19 | R22 | | | |
| VCCINT | | | | | M19 | M21 | R24 | | | |
| VCCINT | | | | | M21 | N13 | T15 | | | |
| VCCINT | | | | | N12 | N15 | T17 | | | |
| VCCINT | | | | | N14 | N18 | T19 | | | |
| VCCINT | | | | | N16 | N20 | T21 | | | |
| VCCINT | | | | | N18 | P12 | T23 | | | |
| VCCINT | | | | | N20 | P14 | T25 | | | |
| VCCINT | | | | | Y11 | P16 | U16 | | | |
| VCCINT | | | | | Y13 | P17 | U18 | | | |
| VCCINT | | | | | Y15 | P19 | U20 | | | |
| VCCINT | | | | | Y19 | P21 | U22 | | | |
| VCCINT | | | | | Y21 | R13 | U24 | | | |

Table 6–1. Pin List for the Stratix EP1S60 Device (Part 60 of 78)

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| VCCINT | | | | | W12 | R15 | V15 | | | |
| VCCINT | | | | | W14 | R18 | V17 | | | |
| VCCINT | | | | | W16 | R20 | V19 | | | |
| VCCINT | | | | | W18 | T14 | V21 | | | |
| VCCINT | | | | | W20 | T16 | V23 | | | |
| VCCINT | | | | | V11 | T17 | W16 | | | |
| VCCINT | | | | | V13 | T19 | W18 | | | |
| VCCINT | | | | | V15 | U14 | W22 | | | |
| VCCINT | | | | | V17 | U16 | W24 | | | |
| VCCINT | | | | | V19 | U17 | Y15 | | | |
| VCCINT | | | | | V21 | U19 | Y17 | | | |
| VCCINT | | | | | U10 | V13 | Y23 | | | |
| VCCINT | | | | | U14 | V15 | Y25 | | | |
| VCCINT | | | | | U18 | V18 | AA16 | | | |
| VCCINT | | | | | U22 | V20 | AA18 | | | |
| VCCINT | | | | | T11 | W14 | AA22 | | | |
| VCCINT | | | | | T13 | W16 | AA24 | | | |
| VCCINT | | | | | T19 | W17 | AB17 | | | |
| VCCINT | | | | | T21 | W19 | AB19 | | | |
| VCCINT | | | | | P11 | Y13 | AB21 | | | |
| VCCINT | | | | | P13 | Y15 | AB23 | | | |
| VCCINT | | | | | P14 | Y18 | AB25 | | | |

**Table 6–1. Pin List for the Stratix EP1S60 Device (Part 61 of 78)**

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | | | |
| VCCINT | | | | | P15 | Y20 | AC16 | | | |
| VCCINT | | | | | P17 | | AC18 | | | |
| VCCINT | | | | | P19 | | AC20 | | | |
| VCCINT | | | | | P21 | | AC22 | | | |
| VCCINT | | | | | R12 | | AC24 | | | |
| VCCINT | | | | | R13 | | AD15 | | | |
| VCCINT | | | | | R14 | | AD17 | | | |
| VCCINT | | | | | R18 | | AD19 | | | |
| VCCINT | | | | | R19 | | AD21 | | | |
| VCCINT | | | | | R20 | | AD23 | | | |
| VCCINT | | | | | L20 | | AD25 | | | |
| VCCINT | | | | | L13 | | AE16 | | | |
| VCCINT | | | | | AA20 | | AE18 | | | |
| VCCINT | | | | | AA12 | | AE20 | | | |
| VCCINT | | | | | AA14 | | AE24 | | | |
| GND | | | | | AD18 | AD17 | | | | |
| GND | | | | | AA18 | AF17 | AK22 | | | |
| GND | | | | | H17 | J17 | | | | |
| GND | | | | | H18 | H18 | AL21 | | | |
| GND | | | | | AL30 | A10 | J21 | | | |
| GND | | | | | AK30 | A2 | | | | |
| GND | | | | | AK31 | A23 | K22 | | | |

**Table 6–1. Pin List for the Stratix EP1S60 Device (Part 62 of 78)**

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | | | |
| GND | | | | | AL31 | A31 | | | | |
| GND | | | | | A30 | AA16 | A2 | | | |
| GND | | | | | A31 | AA17 | B2 | | | |
| GND | | | | | B31 | AC1 | B1 | | | |
| GND | | | | | B30 | AC32 | A38 | | | |
| GND | | | | | A1 | AL1 | B38 | | | |
| GND | | | | | B1 | AL2 | B39 | | | |
| GND | | | | | B2 | AL31 | AV39 | | | |
| GND | | | | | A2 | AL32 | AV38 | | | |
| GND | | | | | AL1 | AM10 | AW38 | | | |
| GND | | | | | AK1 | AM2 | AV1 | | | |
| GND | | | | | AK2 | AM23 | AV2 | | | |
| GND | | | | | AL2 | AM31 | AW2 | | | |
| GND | | | | | AL11 | B1 | AW13 | | | |
| GND | | | | | AL21 | B2 | A13 | | | |
| GND | | | | | A21 | B31 | A27 | | | |
| GND | | | | | A11 | B32 | AW27 | | | |
| GND | | | | | Y31 | K1 | N1 | | | |
| GND | | | | | M31 | K32 | N39 | | | |
| GND | | | | | M1 | M13 | AG39 | | | |
| GND | | | | | Y1 | M15 | AG1 | | | |
| GND | | | | | | M16 | Y10 | | | |

*Table 6–1. Pin List for the Stratix EP1S60 Device (Part 63 of 78)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| GND | | | | | | M17 | AA7 | | | |
| GND | | | | | | M18 | Y30 | | | |
| GND | | | | | | M20 | W33 | | | |
| GND | | | | | | N12 | G19 | | | |
| GND | | | | | | N14 | K20 | | | |
| GND | | | | | | N16 | AK20 | | | |
| GND | | | | | | N17 | AN21 | | | |
| GND | | | | | | N19 | AU37 | | | |
| GND | | | | | | N21 | C37 | | | |
| GND | | | | | | P13 | C3 | | | |
| GND | | | | | | P15 | AU3 | | | |
| GND | | | | | | P18 | AK30 | | | |
| GND | | | | | | P20 | K30 | | | |
| GND | | | | | | R14 | K10 | | | |
| GND | | | | | | R16 | AK10 | | | |
| GND | | | | | | R17 | AM32 | | | |
| GND | | | | | | R19 | H32 | | | |
| GND | | | | | | T12 | H8 | | | |
| GND | | | | | | T13 | AM8 | | | |
| GND | | | | | | T15 | | | | |
| GND | | | | | | T18 | | | | |
| GND | | | | | | T20 | | | | |

Table 6–1. Pin List for the Stratix EP1S60 Device (Part 64 of 78)

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| GND | | | | | | T21 | | | | |
| GND | | | | | | U12 | | | | |
| GND | | | | | | U13 | | | | |
| GND | | | | | | U15 | | | | |
| GND | | | | | | U18 | | | | |
| GND | | | | | | U20 | | | | |
| GND | | | | | | U21 | | | | |
| GND | | | | | | V14 | | | | |
| GND | | | | | | V16 | | | | |
| GND | | | | | | V17 | | | | |
| GND | | | | | | V19 | | | | |
| GND | | | | | | W13 | | | | |
| GND | | | | | | W15 | | | | |
| GND | | | | | | W18 | | | | |
| GND | | | | | | W20 | | | | |
| GND | | | | | | Y14 | | | | |
| GND | | | | | | Y16 | | | | |
| GND | | | | | | Y17 | | | | |
| GND | | | | | | Y19 | | | | |
| GND | | | | | AB16 | | | | | |
| GND | | | | | Y16 | | | | | |
| GND | | | | | V16 | | | | | |

*Table 6–1. Pin List for the Stratix EP1S60 Device (Part 65 of 78)*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | | | |
| GND | | | | | AA17 | | | | | |
| GND | | | | | W17 | | | | | |
| GND | | | | | U17 | | | | | |
| GND | | | | | K16 | | | | | |
| GND | | | | | M16 | | | | | |
| GND | | | | | P16 | | | | | |
| GND | | | | | L17 | | | | | |
| GND | | | | | N17 | | | | | |
| GND | | | | | R17 | | | | | |
| GND | | | | | T10 | | | | | |
| GND | | | | | T12 | | | | | |
| GND | | | | | T14 | | | | | |
| GND | | | | | U11 | | | | | |
| GND | | | | | U13 | | | | | |
| GND | | | | | U15 | | | | | |
| GND | | | | | T22 | | | | | |
| GND | | | | | T20 | | | | | |
| GND | | | | | T18 | | | | | |
| GND | | | | | U21 | | | | | |
| GND | | | | | U19 | | | | | |
| GND | | | | | V12 | | | | | |
| GND | | | | | V14 | | | | | |

**Table 6–1. Pin List for the Stratix EP1S60 Device (Part 66 of 78)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| GND | | | | | V18 | | | | | |
| GND | | | | | V20 | | | | | |
| GND | | | | | M18 | | | | | |
| GND | | | | | P18 | | | | | |
| GND | | | | | L15 | | | | | |
| GND | | | | | N15 | | | | | |
| GND | | | | | R15 | | | | | |
| GND | | | | | W11 | | | | | |
| GND | | | | | W13 | | | | | |
| GND | | | | | W15 | | | | | |
| GND | | | | | Y12 | | | | | |
| GND | | | | | Y14 | | | | | |
| GND | | | | | W21 | | | | | |
| GND | | | | | W19 | | | | | |
| GND | | | | | Y18 | | | | | |
| GND | | | | | Y20 | | | | | |
| GND | | | | | M20 | | | | | |
| GND | | | | | M14 | | | | | |
| GND | | | | | M12 | | | | | |
| GND | | | | | N11 | | | | | |
| GND | | | | | N13 | | | | | |
| GND | | | | | N19 | | | | | |

*Table 6–1. Pin List for the Stratix EP1S60 Device (Part 67 of 78)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| GND | | | | | N21 | | | | | |
| GND | | | | | P12 | | | | | |
| GND | | | | | R11 | | | | | |
| GND | | | | | R21 | | | | | |
| GND | | | | | P20 | | | | | |
| GND | | | | | | | R15 | | | |
| GND | | | | | | | R17 | | | |
| GND | | | | | | | R19 | | | |
| GND | | | | | | | R23 | | | |
| GND | | | | | | | R25 | | | |
| GND | | | | | | | T16 | | | |
| GND | | | | | | | T18 | | | |
| GND | | | | | | | T20 | | | |
| GND | | | | | | | T22 | | | |
| GND | | | | | | | T24 | | | |
| GND | | | | | | | U15 | | | |
| GND | | | | | | | U17 | | | |
| GND | | | | | | | U19 | | | |
| GND | | | | | | | U21 | | | |
| GND | | | | | | | U23 | | | |
| GND | | | | | | | U25 | | | |
| GND | | | | | | | V16 | | | |

**Table 6–1. Pin List for the Stratix EP1S60 Device (Part 68 of 78)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| GND | | | | | | | V18 | | | |
| GND | | | | | | | V20 | | | |
| GND | | | | | | | V22 | | | |
| GND | | | | | | | V24 | | | |
| GND | | | | | | | W17 | | | |
| GND | | | | | | | W23 | | | |
| GND | | | | | | | W25 | | | |
| GND | | | | | | | Y16 | | | |
| GND | | | | | | | Y18 | | | |
| GND | | | | | | | Y22 | | | |
| GND | | | | | | | Y24 | | | |
| GND | | | | | | | AA15 | | | |
| GND | | | | | | | AA17 | | | |
| GND | | | | | | | AA23 | | | |
| GND | | | | | | | AB16 | | | |
| GND | | | | | | | AB18 | | | |
| GND | | | | | | | AB20 | | | |
| GND | | | | | | | AB22 | | | |
| GND | | | | | | | AB24 | | | |
| GND | | | | | | | AC15 | | | |
| GND | | | | | | | AC17 | | | |
| GND | | | | | | | AC19 | | | |

**Table 6–1. Pin List for the Stratix EP1S60 Device (Part 69 of 78)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| GND | | | | | | | AC21 | | | |
| GND | | | | | | | AC23 | | | |
| GND | | | | | | | AC25 | | | |
| GND | | | | | | | AD16 | | | |
| GND | | | | | | | AD18 | | | |
| GND | | | | | | | AD20 | | | |
| GND | | | | | | | AD22 | | | |
| GND | | | | | | | AD24 | | | |
| GND | | | | | | | AE15 | | | |
| GND | | | | | | | AE17 | | | |
| GND | | | | | | | AE21 | | | |
| GND | | | | | | | AE23 | | | |
| GND | | | | | | | AE25 | | | |
| No connection | | | | | AB18 | | AA14 | | | |
| No connection | | | | | AB10 | | AE10 | | | |
| No connection | | | | | K14 | | AE31 | | | |
| No connection | | | | | K22 | | AF18 | | | |
| No connection | | | | | L10 | | AF27 | | | |
| No connection | | | | | P22 | | AG16 | | | |
| No connection | | | | | | | AG26 | | | |
| No connection | | | | | | | AH25 | | | |
| No connection | | | | | | | AL6 | | | |

*Table 6–1. Pin List for the Stratix EP1S60 Device (Part 70 of 78)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| No connection | | | | | | | AP34 | | | |
| No connection | | | | | | | AV37 | | | |
| No connection | | | | | | | E4 | | | |
| No connection | | | | | | | G35 | | | |
| No connection | | | | | | | J35 | | | |
| No connection | | | | | | | M26 | | | |
| No connection | | | | | | | N17 | | | |
| No connection | | | | | | | N27 | | | |
| No connection | | | | | | | P18 | | | |
| No connection | | | | | | | P31 | | | |
| No connection | | | | | | | R30 | | | |
| No connection | | | | | | | T29 | | | |
| No connection | | | | | | | Y13 | | | |
| No connection | | | | | | | AB14 | | | |
| No connection | | | | | | | AE12 | | | |
| No connection | | | | | | | AF9 | | | |
| No connection | | | | | | | AF19 | | | |
| No connection | | | | | | | AF28 | | | |
| No connection | | | | | | | AG17 | | | |
| No connection | | | | | | | AG27 | | | |
| No connection | | | | | | | AH26 | | | |
| No connection | | | | | | | AL34 | | | |

**Table 6–1. Pin List for the Stratix EP1S60 Device (Part 71 of 78)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| No connection | | | | | | | AP35 | | | |
| No connection | | | | | | | B3 | | | |
| No connection | | | | | | | E36 | | | |
| No connection | | | | | | | H5 | | | |
| No connection | | | | | | | L15 | | | |
| No connection | | | | | | | M27 | | | |
| No connection | | | | | | | N18 | | | |
| No connection | | | | | | | N28 | | | |
| No connection | | | | | | | P19 | | | |
| No connection | | | | | | | R9 | | | |
| No connection | | | | | | | R31 | | | |
| No connection | | | | | | | U26 | | | |
| No connection | | | | | | | Y14 | | | |
| No connection | | | | | | | AC13 | | | |
| No connection | | | | | | | AE13 | | | |
| No connection | | | | | | | AF10 | | | |
| No connection | | | | | | | AF20 | | | |
| No connection | | | | | | | AF30 | | | |
| No connection | | | | | | | AG18 | | | |
| No connection | | | | | | | AG28 | | | |
| No connection | | | | | | | AH27 | | | |
| No connection | | | | | | | AL35 | | | |

*Table 6–1. Pin List for the Stratix EP1S60 Device (Part 72 of 78)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **956-Pin BGA** | **1020-Pin FineLine BGA** | **1508-Pin FineLine BGA** | **DQS for x16** | **DQS for x32** | **DIFFIO Speed** *Note (1)* |
| No connection | | | | | | | AT3 | | | |
| No connection | | | | | | | B37 | | | |
| No connection | | | | | | | E37 | | | |
| No connection | | | | | | | H6 | | | |
| No connection | | | | | | | L29 | | | |
| No connection | | | | | | | M28 | | | |
| No connection | | | | | | | N19 | | | |
| No connection | | | | | | | P9 | | | |
| No connection | | | | | | | P20 | | | |
| No connection | | | | | | | R10 | | | |
| No connection | | | | | | | T11 | | | |
| No connection | | | | | | | U27 | | | |
| No connection | | | | | | | Y26 | | | |
| No connection | | | | | | | AC14 | | | |
| No connection | | | | | | | AE14 | | | |
| No connection | | | | | | | AF12 | | | |
| No connection | | | | | | | AF21 | | | |
| No connection | | | | | | | AF31 | | | |
| No connection | | | | | | | AG19 | | | |
| No connection | | | | | | | AH12 | | | |
| No connection | | | | | | | AH28 | | | |
| No connection | | | | | | | AN5 | | | |

Table 6–1. Pin List for the Stratix EP1S60 Device (Part 73 of 78)

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pad Name / Function** | **Optional Function(s)** | **Configuration Function** | **Bank Number** | **VREF Bank** | **956-Pin BGA** | **1020-Pin FineLine BGA** | **1508-Pin FineLine BGA** | | | |
| No connection | | | | | | | AT4 | | | |
| No connection | | | | | | | C2 | | | |
| No connection | | | | | | | F5 | | | |
| No connection | | | | | | | H31 | | | |
| No connection | | | | | | | M11 | | | |
| No connection | | | | | | | R29 | | | |
| No connection | | | | | | | N20 | | | |
| No connection | | | | | | | P10 | | | |
| No connection | | | | | | | P22 | | | |
| No connection | | | | | | | R12 | | | |
| No connection | | | | | | | T12 | | | |
| No connection | | | | | | | V26 | | | |
| No connection | | | | | | | Y27 | | | |
| No connection | | | | | | | AD13 | | | |
| No connection | | | | | | | AE26 | | | |
| No connection | | | | | | | AF13 | | | |
| No connection | | | | | | | AF22 | | | |
| No connection | | | | | | | AG12 | | | |
| No connection | | | | | | | AG22 | | | |
| No connection | | | | | | | AH13 | | | |
| No connection | | | | | | | AJ11 | | | |
| No connection | | | | | | | AN6 | | | |

*Table 6–1. Pin List for the Stratix EP1S60 Device (Part 74 of 78)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| No connection | | | | | | | AT36 | | | |
| No connection | | | | | | | C38 | | | |
| No connection | | | | | | | F6 | | | |
| No connection | | | | | | | H34 | | | |
| No connection | | | | | | | M12 | | | |
| No connection | | | | | | | N12 | | | |
| No connection | | | | | | | P12 | | | |
| No connection | | | | | | | P24 | | | |
| No connection | | | | | | | R13 | | | |
| No connection | | | | | | | T13 | | | |
| No connection | | | | | | | V27 | | | |
| No connection | | | | | | | AD14 | | | |
| No connection | | | | | | | AE27 | | | |
| No connection | | | | | | | AF14 | | | |
| No connection | | | | | | | AF24 | | | |
| No connection | | | | | | | AG13 | | | |
| No connection | | | | | | | AG23 | | | |
| No connection | | | | | | | AH14 | | | |
| No connection | | | | | | | AJ22 | | | |
| No connection | | | | | | | AN34 | | | |
| No connection | | | | | | | AT37 | | | |
| No connection | | | | | | | D3 | | | |

**Table 6–1. Pin List for the Stratix EP1S60 Device (Part 75 of 78)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| No connection | | | | | | | F34 | | | |
| No connection | | | | | | | H35 | | | |
| No connection | | | | | | | M13 | | | |
| No connection | | | | | | | N13 | | | |
| No connection | | | | | | | P13 | | | |
| No connection | | | | | | | P26 | | | |
| No connection | | | | | | | R14 | | | |
| No connection | | | | | | | T14 | | | |
| No connection | | | | | | | W13 | | | |
| No connection | | | | | | | AD26 | | | |
| No connection | | | | | | | AE28 | | | |
| No connection | | | | | | | AF15 | | | |
| No connection | | | | | | | AF25 | | | |
| No connection | | | | | | | AG14 | | | |
| No connection | | | | | | | AG24 | | | |
| No connection | | | | | | | AH15 | | | |
| No connection | | | | | | | AJ25 | | | |
| No connection | | | | | | | AN35 | | | |
| No connection | | | | | | | AU2 | | | |
| No connection | | | | | | | D4 | | | |
| No connection | | | | | | | F35 | | | |
| No connection | | | | | | | J5 | | | |

**Table 6–1. Pin List for the Stratix EP1S60 Device (Part 76 of 78)**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| No connection | | | | | | | M22 | | | |
| No connection | | | | | | | N14 | | | |
| No connection | | | | | | | N24 | | | |
| No connection | | | | | | | P14 | | | |
| No connection | | | | | | | P27 | | | |
| No connection | | | | | | | R26 | | | |
| No connection | | | | | | | T26 | | | |
| No connection | | | | | | | U14 | | | |
| No connection | | | | | | | AD27 | | | |
| No connection | | | | | | | AE30 | | | |
| No connection | | | | | | | AF17 | | | |
| No connection | | | | | | | AF26 | | | |
| No connection | | | | | | | AG15 | | | |
| No connection | | | | | | | AG25 | | | |
| No connection | | | | | | | AH22 | | | |
| No connection | | | | | | | AL5 | | | |
| No connection | | | | | | | AP5 | | | |
| No connection | | | | | | | AU38 | | | |
| No connection | | | | | | | D36 | | | |
| No connection | | | | | | | G5 | | | |
| No connection | | | | | | | J6 | | | |
| No connection | | | | | | | M23 | | | |

*Table 6–1. Pin List for the Stratix EP1S60 Device (Part 77 of 78)*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| No connection | | | | | | | N15 | | | |
| No connection | | | | | | | N25 | | | |
| No connection | | | | | | | P15 | | | |
| No connection | | | | | | | P28 | | | |
| No connection | | | | | | | R27 | | | |
| No connection | | | | | | | T27 | | | |
| No connection | | | | | | | W26 | | | |
| No connection | | | | | | | AE9 | | | |
| No connection | | | | | | | AP6 | | | |
| No connection | | | | | | | AV3 | | | |
| No connection | | | | | | | D37 | | | |
| No connection | | | | | | | G6 | | | |
| No connection | | | | | | | J30 | | | |
| No connection | | | | | | | M25 | | | |
| No connection | | | | | | | N16 | | | |
| No connection | | | | | | | N26 | | | |
| No connection | | | | | | | P17 | | | |
| No connection | | | | | | | P30 | | | |
| No connection | | | | | | | R28 | | | |
| No connection | | | | | | | T28 | | | |
| No connection | | | | | | | V28 | | | |

### Table 6–1. Pin List for the Stratix EP1S60 Device (Part 78 of 78)

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pad Name / Function | Optional Function(s) | Configuration Function | Bank Number | VREF Bank | 956-Pin BGA | 1020-Pin FineLine BGA | 1508-Pin FineLine BGA | DQS for x16 | DQS for x32 | DIFFIO Speed *Note (1)* |
| No connection | | | | | | | E3 | | | |
| No connection | | | | | | | G34 | | | |
| No connection | | | | | | | J34 | | | |

*Note to Table 6–1:*

(1) The wire bond and flip-chip packages have different data rates for the high speed differential I/O channels. Table 6–2 shows the data rates as supported for each package.

### Table 6–2. High Speed Differential I/O Channel Data Rates

| Package | Package Type | High Speed Differential I/O Channel Performance (DIFFIO Speed) | | Units |
|---|---|---|---|---|
| | | High | Low | |
| 956-pin BGA | flip chip | 840 | N/A | Mbps |
| 1020-pin FineLine BGA | flip chip | 840 | 462 | Mbps |
| 1508-pin FineLine BGA | flip chip | 840 | 462 | Mbps |

## Pin Definitions

Table 6–3 shows pin definitions for the EP1S60 device.

*Table 6–3. Pin Definitions for the EP1S60 Device (Part 1 of 5)*

| Pin Name | Pin Type (1st, 2nd, & 3rd Function) | Pin Description |
|---|---|---|
| **Supply and Reference Pins** | | |
| VREF[1..4]B[1..8] | Input | Input reference voltage for each I/O bank. If a bank is used for a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for that bank. All of the VREF pins within a bank are shorted together. Each VREF pin can support up to 20 inputs on each side. If VREF pins are not used, designers should connect them to either VCC or Gnd. |
| VCCIO[1..8] | Power | These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards. VCCIO also supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5-V, 1.8-V, 2.5-V, 3.3-V PCI, and 3.3-V PCI-X I/O standards. |
| VCCINT | Power | These are internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVDS, LVPECL, 3.3-V PCML, HyperTransportô technology, differential HSTL, GTL, GTL+, HSTL, SSTL, CTT, and 3.3-V AGP I/O standards. |
| VCC_PLL5_OUTA | Power | External clock output buffer power for PLL5 clock outputs PLL5_OUT[1..0]. The designer must connect this pin to the VCCIO of bank 9. |
| VCC_PLL5_OUTB | Power | External clock output buffer power for PLL5 clock outputs PLL5_OUT[3..2]. The designer must connect this pin to the VCCIO of bank 10. |
| VCC_PLL6_OUTA | Power | External clock output buffer power for PLL6 clock outputs PLL6_OUT[1..0]. The designer must connect this pin to the VCCIO of bank 11. |
| VCC_PLL6_OUTB | Power | External clock output buffer power for PLL6 clock outputs PLL6_OUT[3..2]. The designer must connect this pin to the VCCIO of bank 12. |
| VCCA_PLL[1..12] | Power | Analog power for PLLs[1..12]. The designer must connect this pin to 1.5 V, even if the PLL is not used. |
| GNDA_PLL[1..12] | Ground | Analog ground for PLLs[1..12]. The designer can connect this pin to the GND plane on the board. |
| VCCG_PLL[1..12] | Power | Guard ring power for PLLs[1..12]. The designer must connect this pin to 1.5 V, even if the PLL is not used. |
| GNDG_PLL[1..12] | Ground | Guard ring ground for PLLs[1..12]. The designer can connect this pin to the GND plane on the board. |

*Table 6–3. Pin Definitions for the EP1S60 Device (Part 2 of 5)*

| Pin Name | Pin Type (1st, 2nd, & 3rd Function) | Pin Description |
|---|---|---|
| **Dedicated & Configuration/JTAG Pins** | | |
| CONF_DONE | Bidirectional (open-drain) | This is a dedicated configuration status pin; it is not available as a user I/O pin. |
| nSTATUS | Bidirectional (open-drain) | This is a dedicated configuration status pin; it is not available as a user I/O pin. |
| nCONFIG | Input | Dedicated configuration control input. A low transition resets the target device; a low-to-high transition begins configuration. All I/O pins tri-state when nCONFIG is driven low. |
| DCLK | Input | Clock input used to clock configuration data from an external source into the Stratix device. This is a dedicated pin used for configuration. |
| nIO_PULLUP | Input | IF nIO_PULLUP is driven high during configuration, the weak pull-ups on all user I/O pins are disabled. If driven low, the weak pull-ups are enabled during configuration. nIO_PULLUP can be pulled up to either 1.5, 1.8, 2.5, or 3.3 V. |
| PORSEL | Input | Dedicated input pin used to select POR delay times of 2 ms or 100 ms during powerup. When PORSEL is connected to ground, the POR time is 100 ms. When PORSEL is connected to 3.3 V, the POR time is 2 ms. |
| VCCSEL | Input | VCCSEL is used to select which input buffer is used on all configuration pins. VCCSEL will control whether the 3.3-/2.5-V input buffer or the 1.8-/1.5-V input buffer is used. A "0" means 3.3/2.5 V and a "1" means 1.8-/1.5 V. At powerup, VCCSEL accepts 3.3V and 2.5V TTL Levels. VCCSEL affects the following pins: TDI, TMS, TCK, TRST, MSEL0, MSEL1, MSEL2, nCONFIG, nCE, DCLK, CONF_DONE, nSTATUS, and PLL_ENA. |
| nCE | Input | Active-low chip enables. Dedicated chip enable input used to detect which device is active in a chain of devices. When nCE is low, the device is enabled. When nCE is high, the device is disabled. |
| nCEO | Output | Output that drives low when device configuration is complete. During multi-device configuration, this pin feeds a subsequent deviceís nCE pin. |
| TMS | Input | This is a dedicated JTAG input pin. |
| TDI | Input | This is a dedicated JTAG input pin. |
| TCK | Input | This is a dedicated JTAG input pin. |

**Table 6–3. Pin Definitions for the EP1S60 Device (Part 3 of 5)**

| Pin Name | Pin Type (1st, 2nd, & 3rd Function) | Pin Description |
|---|---|---|
| TDO | Output | This is a dedicated JTAG input pin. |
| TRST | Input | This is a dedicated JTAG input pin. Active low input, used to asynchronously reset the JTAG boundary scan circuit. |
| MSEL[2..0] | Input | Dedicated mode select control pins that set the configuration mode for the device. |
| TEMPDIODEp | Input | Pin used in conjunction with the temperature sensing diode (bias-high input) inside the Stratix device. If the temperature sensing diode is not used then connect this pin to GND. |
| TEMPDIODEn | Input | Pin used in conjunction with the temperature sensing diode (bias-low input) inside the Stratix device. If the temperature sensing diode is not used then connect this pin to GND. |
| **Clock and PLL Pins** | | |
| PLL_ENA | Input | Dedicated input pin that drives the optional pllena port of all or a set of PLLs. If a PLL uses the pllena port, drive the PLL_ENA pin low to reset all PLLs including the counters to their default state. If VCCSEL = 0, then you must drive the PLL_ENA with a 3.3/2.5 V signal to enable the PLLs. If VCCSEL = 1, connect PLL_ENA to 1.8/1.5 V to enable the PLLs. |
| FCLK[7..0] | Bidirectional | Dedicated fast regional clock pins. FCLK pins can also be used as type input, output, or as bidirectional pins. |
| FPLL[10..7]CLKp | Input | Dedicated global clock inputs for fast PLLs (PLLs 7 through 10). |
| FPLL[10..7]CLKn | Input | Dedicated negative terminal associated with FPLL[10..7]CLKp pins. |
| CLK[15..0]p | Input | Dedicated global clock inputs 0 to 15. |
| CLK[15..0]n | I/O, Input | Optional negative terminal input for differential global clock input. |
| PLL6_OUT[3..0]p | I/O, Output | Optional external clock outputs [3..0] from enhanced PLL 6. These pins can be differential (four output pin pairs) or single ended (eight clock outputs from PLL6). |
| PLL6_OUT[3..0]n | I/O, Output | Optional negative terminal for external clock outputs [3..0] from PLL6. If the clock outputs are single ended, then each pair of pins (i.e., PLL6_OUT0p and PLL6_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase. |
| PLL5_OUT[3..0]p | I/O, Output | Optional external clock outputs [3..0] from enhanced PLL 5. These pins can be differential (four output pin pairs) or single ended (eight clock outputs from PLL5). |

*Table 6–3. Pin Definitions for the EP1S60 Device (Part 4 of 5)*

| Pin Name | Pin Type (1st, 2nd, & 3rd Function) | Pin Description |
|---|---|---|
| PLL5_OUT[3..0]n | I/O, Output | Optional negative terminal for external clock outputs [3..0] from PLL 5. If the clock outputs are single ended, then each pair of pins (i.e., PLL5_OUT0p and PLL5_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase. |
| **Optional/Dual-Purpose Pins** | | |
| DATA0 | I/O, Input | Dual-purpose configuration data input pin. Can be used as an I/O pin after configuration is complete. |
| DIFFIO_TX[0..151]n | I/O, Output | This pin can be used as the complementary signal of the differential inputs and outputs. If not used for the differential pair, these pins are regular I/O pins. Pins with an n suffix carry the negative signal for the differential channel. Pins with a p suffix carry the positive signal for the differential channel. |
| CLK6n, PLL12_OUT | I/O, Input (CLK6n), Output (PLL12_OUT) | This pin can be used as an I/O pin, CLK6n, as the PLL12_OUT pin. Only the EP1S40 and larger devices have this pin. |
| CLK13n, PLL11_OUT | I/O, Input (CLK13n), Output (PLL11_OUT) | This pin can be used as an I/O pin, CLK13n, or used as the PLL11_OUT pin. Only the EP1S40 and larger devices have this pin. |
| PLL5_FBp | I/O, Input | External feedback input pin for PLL5. This pin can be used as a user I/O pin if external feedback mode is not used. |
| PLL5_FBn | I/O, Input | Negative terminal input for external feedback input PLL5_FBp |
| PLL6_FBp | I/O, Input | External feedback input pin for PLL6 |
| PLL6_FBn | I/O, Input | Negative terminal input for external feedback input PLL6_FBp |
| INIT_DONE | I/O, Output | This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration. |
| DATA[7..1] | I/O, Input | Dual-purpose configuration input data pins. These pins can be used for configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration. |
| nRS | I/O, Input | Read strobe input pin. This pin can be used as a user I/O pin after configuration. |
| DEV_CLRn | I/O, Input | Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as defined in the users design. |

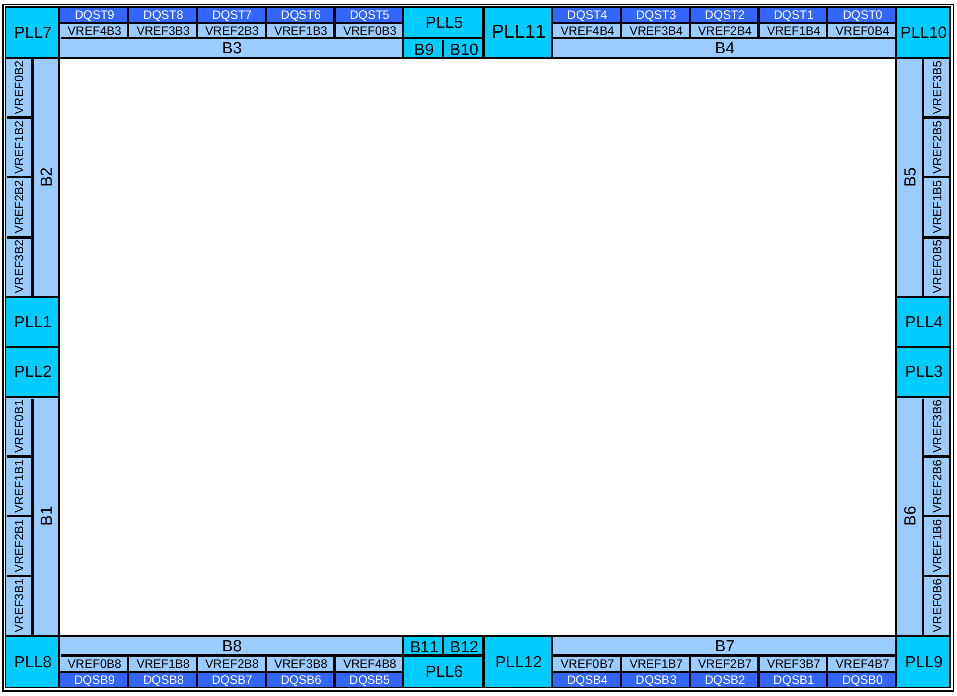
*Table 6–3. Pin Definitions for the EP1S60 Device (Part 5 of 5)*

| Pin Name | Pin Type (1st, 2nd, & 3rd Function) | Pin Description |
|---|---|---|
| DEV_OE | I/O, Input | Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design. |
| CLKUSR | I/O, Input | Optional user-supplied clock input. Synchronizes the initialization of one or more devices. This pin can be used as a user I/O pin after configuration. |
| RDYnBSY | I/O, Output | Ready not busy output. A high output indicates that the target device is ready to accept another data byte. A low output indicates that the target device is not ready to receive another data byte. This pin can be used as a user I/O pin after configuration. |
| nCS,CS | I/O, Input | These are chip-select inputs that enable the Stratix device in the passive parallel asynchronous configuration mode. Drive nCS low and CS high to target a device for configuration. If a design requires an active high enable, use the CS pin and drive the nCS pin low. If a design requires an active low enable, use the nCS pin and drive the CS pin high. Configuration will be paused when either signal is inactive. Hold the nCS and CS pins active during configuration and initialization. The design can use these pins as user I/O pins after configuration. |
| nWS | I/O, Input | Active-low write strobe input to latch a byte of data on the DATA pins. This pin can be used as a user I/O pin after configuration. |
| PGM[2..0] | I/O, Output | These output pins control one of eight pages in the EPC16 configuration device when using remote update or local update configuration modes. When not using remote update or local update configuration modes, these pins are user I/O pins. |
| RUP[8..1] | I/O, Input | Reference pins for banks 8 to 1. The external precision resistors $R_{UP}$ must be connected to the designated RUP pin on that I/O bank. If not required, these pins are regular I/O pins. |
| RDN[8..1] | I/O, Input | Reference pins for banks 8 to 1. The external precision resistors RDN must be connected to the designated RDN pin on that I/O bank. If not required, these pins are regular I/O pins. |
| RUnLU | I/O, Input | Input control pin to select remote update or local update modes. If MSEL2 = 1, this is a input control pin to select remote update (RUnLU =1) or local update (RUnLU =0) modes. If MSEL2 = 0, the RUnLU pin is a user I/O pin. |

## PLL & Bank Diagram

Figure 6–1 shows the PLL and bank locations for the EP1S60 device.

*Figure 6–1. PLL and Bank Diagram* Notes (1), (2)



*Notes for Figure 6–1:*

(1) This is a top view of the silicon die. For flip chip packages the die is mounted upside down in the package.

(2) This is a pictoral representation only, to give an idea of placement on the device. Refer to the pinlist and the Quartus II software for exact locations.

## Fast PLL to High-Speed I/O Connections

Table 6–4 shows the number of shows the number of high-speed differential I/O channels that can be driven by each Fast PLL for the EP1S60 device.

*Table 6–4. Fast PLL Connections for the EP1S60 Device*

| Device | Pin Count | FAST PLL Source Location | Number of Rx Channels (1) (5) | Number of Tx Channels (2) (5) | Number of Overlapped Rx Channels (3) (5) | Number of Overlapped Tx Channels (4) (5) |
|---|---|---|---|---|---|---|
| EP1S60 | 956 | PLL1 | 20/0 | 12/0 | 12/0 | 12/0 |
| | | PLL2 | 20/0 | 10/0 | 10/0 | 10/0 |
| | | PLL3 | 20/0 | 10/0 | 10/0 | 10/0 |
| | | PLL4 | 20/0 | 12/0 | 12/0 | 12/0 |
| | | PLL7 | 12/0 | 20/0 | 12/0 | 12/0 |
| | | PLL8 | 10/0 | 20/0 | 10/0 | 10/0 |
| | | PLL9 | 10/0 | 20/0 | 10/0 | 10/0 |
| | | PLL10 | 12/0 | 20/0 | 12/0 | 12/0 |
| | 1020 | PLL1 | 20/0 | 12/2 | 12/0 | 12/0 |
| | | PLL2 | 20/0 | 10/3 | 10/0 | 10/0 |
| | | PLL3 | 20/0 | 10/3 | 10/0 | 10/0 |
| | | PLL4 | 20/0 | 12/2 | 12/0 | 12/0 |
| | | PLL7 | 12/2 | 20/0 | 12/0 | 12/0 |
| | | PLL8 | 10/3 | 20/0 | 10/0 | 10/0 |
| | | PLL9 | 10/3 | 20/0 | 10/0 | 10/0 |
| | | PLL10 | 12/2 | 20/0 | 12/0 | 12/0 |
| | 1508 | PLL1 | 20/0 | 12/8 | 12/0 | 12/0 |
| | | PLL2 | 20/0 | 10/10 | 10/0 | 10/0 |
| | | PLL3 | 20/0 | 10/10 | 10/0 | 10/0 |
| | | PLL4 | 20/0 | 12/8 | 12/0 | 12/0 |
| | | PLL7 | 12/8 | 20/0 | 12/0 | 12/0 |
| | | PLL8 | 10/10 | 20/0 | 10/0 | 10/0 |
| | | PLL9 | 10/10 | 20/0 | 10/0 | 10/0 |
| | | PLL10 | 12/8 | 20/0 | 12/0 | 12/0 |

*Notes for Table 6–4:*

(1) This is the total number of Rx channels that the PLL listed in the "FAST PLL Source location" column can drive.

(2) This is the total number of Tx channels that the PLL listed in the "FAST PLL Source location" column can drive.

(3) This is the number of Rx channels that can be driven by the PLL listed in the "FAST PLL Source location" that could alternatively be driven by the other adjacent FAST PLL.

(4) This is the number of Tx channels that can be driven by the PLL listed in the "FAST PLL Source location" that could alternatively be driven by the other adjacent FAST PLL.

(5) The counts are reported in the format of (high speed channels)/(low speed channels).

# 7. Stratix EP1S80 Device Pin Information

S5V3007-1.0

## Introduction

The following tables contain pin information for the Straix EP1S80 device, organized into the following sections:

# Pin List

Table 7–1 shows the complete pin list for the EP1S80 device.

**Table 7–1. Pin List for the Stratix EP1S80 Device**

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| VCCINT | | | | | VCC | VCC | VCC | | | |
| VCCA_PLL7 | | | | | L23 | D31 | J31 | | | |
| GND | | | | | GND | GND | GND | | | |
| GNDA_PLL7 | | | | | M23 | D32 | K31 | | | |
| VCCG_PLL7 | | | | | J23 | D30 | L30 | | | |
| GNDG_PLL7 | | | | | K23 | E30 | L31 | | | |
| FPLL7CLKp | | | B2 | VREF0B2 | E31 | L29 | J38 | | | |
| FPLL7CLKn | | | B2 | VREF0B2 | D31 | L28 | J39 | | | |
| IO | | | B2 | VREF0B2 | | | P26 | | | |
| IO | | | B2 | VREF0B2 | | | R26 | | | |
| IO | DIFFIO_RX75p | | B2 | VREF0B2 | | | F34 | | | LOW |
| IO | DIFFIO_RX75n | | B2 | VREF0B2 | | | F35 | | | LOW |
| IO | DIFFIO_TX75p | | B2 | VREF0B2 | | | T26 | | | LOW |
| IO | DIFFIO_TX75n | | B2 | VREF0B2 | | | U26 | | | LOW |
| IO | DIFFIO_RX74p | | B2 | VREF0B2 | | | H35 | | | LOW |
| IO | DIFFIO_RX74n | | B2 | VREF0B2 | | | H34 | | | LOW |
| IO | DIFFIO_TX74p | | B2 | VREF0B2 | | | U27 | | | LOW |
| IO | DIFFIO_TX74n | | B2 | VREF0B2 | | | T27 | | | LOW |
| IO | DIFFIO_RX73p | | B2 | VREF0B2 | | | G35 | | | LOW |
| IO | DIFFIO_RX73n | | B2 | VREF0B2 | | | G34 | | | LOW |
| IO | DIFFIO_TX73p | | B2 | VREF0B2 | | | P27 | | | LOW |

**Table 7–1. Pin List for the Stratix EP1S80 Device**

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| IO | DIFFIO_TX73n | | B2 | VREF0B2 | | | R27 | | | LOW |
| IO | DIFFIO_RX72p | | B2 | VREF0B2 | | | J34 | | | LOW |
| IO | DIFFIO_RX72n | | B2 | VREF0B2 | | | J35 | | | LOW |
| IO | DIFFIO_TX72p | | B2 | VREF0B2 | | | T28 | | | LOW |
| IO | DIFFIO_TX72n | | B2 | VREF0B2 | | | T29 | | | LOW |
| VREF0B2 | | | B2 | VREF0B2 | L22 | F27 | M29 | | | |
| IO | DIFFIO_RX71p | | B2 | VREF0B2 | | | D37 | | | LOW |
| IO | DIFFIO_RX71n | | B2 | VREF0B2 | | | C38 | | | LOW |
| IO | DIFFIO_TX71p | | B2 | VREF0B2 | | | P28 | | | LOW |
| IO | DIFFIO_TX71n | | B2 | VREF0B2 | | | R28 | | | LOW |
| IO | DIFFIO_RX70p | | B2 | VREF0B2 | | | F36 | | | LOW |
| IO | DIFFIO_RX70n | | B2 | VREF0B2 | | | F37 | | | LOW |
| IO | DIFFIO_TX70p | | B2 | VREF0B2 | | | N30 | | | LOW |
| IO | DIFFIO_TX70n | | B2 | VREF0B2 | | | N31 | | | LOW |
| IO | DIFFIO_RX69p | | B2 | VREF0B2 | | | G36 | | | LOW |
| IO | DIFFIO_RX69n | | B2 | VREF0B2 | | | G37 | | | LOW |
| IO | DIFFIO_TX69p | | B2 | VREF0B2 | | | P31 | | | LOW |
| IO | DIFFIO_TX69n | | B2 | VREF0B2 | | | P30 | | | LOW |
| IO | DIFFIO_RX68p | | B2 | VREF0B2 | | | H37 | | | LOW |
| IO | DIFFIO_RX68n | | B2 | VREF0B2 | | | H36 | | | LOW |
| IO | DIFFIO_TX68p | | B2 | VREF0B2 | | | R31 | | | LOW |
| IO | DIFFIO_TX68n | | B2 | VREF0B2 | | | R30 | | | LOW |
| IO | DIFFIO_RX67p | | B2 | VREF0B2 | | | D39 | | | LOW |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pin Name/Function** | **Optional Function(s)** | **Configura-tion Function** | **Bank Number** | **VREF Bank** | **B956** | **F1020** | **F1508** | | | |
| IO | DIFFIO_RX67n | | B2 | VREF0B2 | | | D38 | | | LOW |
| IO | DIFFIO_TX67p | | B2 | VREF0B2 | K24 | G25 | M30 | | | HIGH |
| IO | DIFFIO_TX67n | | B2 | VREF0B2 | J24 | G26 | M31 | | | HIGH |
| IO | DIFFIO_RX66p | | B2 | VREF1B2 | | | E36 | | | LOW |
| IO | DIFFIO_RX66n | | B2 | VREF1B2 | | | E37 | | | LOW |
| IO | DIFFIO_TX66p | | B2 | VREF1B2 | K25 | G28 | J32 | | | HIGH |
| IO | DIFFIO_TX66n | | B2 | VREF1B2 | J25 | G27 | J33 | | | HIGH |
| IO | DIFFIO_RX65p | | B2 | VREF1B2 | | | E38 | | | LOW |
| IO | DIFFIO_RX65n | | B2 | VREF1B2 | | | E39 | | | LOW |
| IO | DIFFIO_TX65p | | B2 | VREF1B2 | H24 | H28 | K32 | | | HIGH |
| IO | DIFFIO_TX65n | | B2 | VREF1B2 | G24 | H27 | K33 | | | HIGH |
| IO | DIFFIO_RX64p | | B2 | VREF1B2 | | | F38 | | | LOW |
| IO | DIFFIO_RX64n | | B2 | VREF1B2 | | | F39 | | | LOW |
| IO | DIFFIO_TX64p | | B2 | VREF1B2 | H25 | J27 | L33 | | | HIGH |
| IO | DIFFIO_TX64n | | B2 | VREF1B2 | G25 | J28 | L32 | | | HIGH |
| IO | DIFFIO_RX63p | | B2 | VREF1B2 | | | G39 | | | LOW |
| IO | DIFFIO_RX63n | | B2 | VREF1B2 | | | G38 | | | LOW |
| IO | DIFFIO_TX63p | | B2 | VREF1B2 | K26 | H25 | M32 | | | HIGH |
| IO | DIFFIO_TX63n | | B2 | VREF1B2 | L26 | H26 | M33 | | | HIGH |
| IO | DIFFIO_RX62p | | B2 | VREF1B2 | | | H39 | | | LOW |
| IO | DIFFIO_RX62n | | B2 | VREF1B2 | | | H38 | | | LOW |
| IO | DIFFIO_TX62p | | B2 | VREF1B2 | J26 | J25 | N32 | | | HIGH |
| IO | DIFFIO_TX62n | | B2 | VREF1B2 | H26 | J26 | N33 | | | HIGH |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pin Name/Function** | **Optional Function(s)** | **Configura-tion Function** | **Bank Number** | **VREF Bank** | **B956** | **F1020** | **F1508** | | | |
| VREF1B2 | | | B2 | VREF1B2 | M22 | | N29 | | | |
| IO | | | B2 | VREF1B2 | | | | | | |
| IO | | | B2 | VREF1B2 | | | | | | |
| IO | DIFFIO_TX61p | | B2 | VREF1B2 | G26 | K28 | K34 | | | HIGH |
| IO | DIFFIO_TX61n | | B2 | VREF1B2 | F26 | K27 | K35 | | | HIGH |
| IO | | | B2 | VREF1B2 | | | | | | |
| IO | | | B2 | VREF1B2 | | | | | | |
| IO | DIFFIO_TX60p | | B2 | VREF1B2 | F27 | K26 | L35 | | | HIGH |
| IO | DIFFIO_TX60n | | B2 | VREF1B2 | G27 | K25 | L34 | | | HIGH |
| IO | DIFFIO_RX59p | | B2 | VREF1B2 | | E32 | | | | LOW |
| IO | DIFFIO_RX59n | | B2 | VREF1B2 | | E31 | | | | LOW |
| IO | DIFFIO_TX59p | | B2 | VREF1B2 | H27 | L27 | M34 | | | HIGH |
| IO | DIFFIO_TX59n | | B2 | VREF1B2 | J27 | L26 | M35 | | | HIGH |
| IO | DIFFIO_RX58p | | B2 | VREF1B2 | | E29 | | | | LOW |
| IO | DIFFIO_RX58n | | B2 | VREF1B2 | | F28 | | | | LOW |
| IO | DIFFIO_TX58p | | B2 | VREF1B2 | K27 | M26 | N34 | | | HIGH |
| IO | DIFFIO_TX58n | | B2 | VREF1B2 | L27 | M27 | N35 | | | HIGH |
| IO | DIFFIO_RX57p | | B2 | VREF1B2 | F28 | F29 | K36 | | | HIGH |
| IO | DIFFIO_RX57n | | B2 | VREF1B2 | G28 | F30 | K37 | | | HIGH |
| IO | DIFFIO_TX57p | | B2 | VREF1B2 | L24 | M24 | P32 | | | HIGH |
| IO | DIFFIO_TX57n | | B2 | VREF1B2 | M24 | M25 | P33 | | | HIGH |
| IO | DIFFIO_RX56p | | B2 | VREF2B2 | J28 | F31 | J36 | | | HIGH |
| IO | DIFFIO_RX56n | | B2 | VREF2B2 | H28 | F32 | J37 | | | HIGH |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pin Name/Function** | **Optional Function(s)** | **Configura-tion Function** | **Bank Number** | **VREF Bank** | **B956** | **F1020** | **F1508** | | | |
| IO | DIFFIO_TX56p | | B2 | VREF2B2 | L25 | N24 | P34 | | | HIGH |
| IO | DIFFIO_TX56n | | B2 | VREF2B2 | M25 | N23 | P35 | | | HIGH |
| IO | DIFFIO_RX55p | | B2 | VREF2B2 | D29 | G29 | L37 | | | HIGH |
| IO | DIFFIO_RX55n | | B2 | VREF2B2 | E29 | G30 | L36 | | | HIGH |
| IO | DIFFIO_TX55p | | B2 | VREF2B2 | P24 | N27 | R33 | | | HIGH |
| IO | DIFFIO_TX55n | | B2 | VREF2B2 | N24 | N28 | R32 | | | HIGH |
| IO | DIFFIO_RX54p | | B2 | VREF2B2 | F29 | H30 | K38 | | | HIGH |
| IO | DIFFIO_RX54n | | B2 | VREF2B2 | G29 | H29 | K39 | | | HIGH |
| IO | DIFFIO_TX54p | | B2 | VREF2B2 | N25 | P23 | R34 | | | HIGH |
| IO | DIFFIO_TX54n | | B2 | VREF2B2 | P25 | P24 | R35 | | | HIGH |
| IO | DIFFIO_RX53p | | B2 | VREF2B2 | H29 | G31 | M36 | | | HIGH |
| IO | DIFFIO_RX53n | | B2 | VREF2B2 | J29 | G32 | M37 | | | HIGH |
| IO | DIFFIO_TX53p | | B2 | VREF2B2 | M26 | N25 | T33 | | | HIGH |
| IO | DIFFIO_TX53n | | B2 | VREF2B2 | N26 | N26 | T32 | | | HIGH |
| IO | DIFFIO_RX52p | | B2 | VREF2B2 | D30 | H31 | L38 | | | HIGH |
| IO | DIFFIO_RX52n | | B2 | VREF2B2 | E30 | H32 | L39 | | | HIGH |
| IO | DIFFIO_TX52p | | B2 | VREF2B2 | M27 | P28 | T30 | | | HIGH |
| IO | DIFFIO_TX52n | | B2 | VREF2B2 | N27 | P27 | T31 | | | HIGH |
| VREF2B2 | | | B2 | VREF2B2 | N22 | L25 | P29 | | | |
| IO | DIFFIO_RX51p | | B2 | VREF2B2 | F30 | J29 | M38 | | | HIGH |
| IO | DIFFIO_RX51n | | B2 | VREF2B2 | G30 | J30 | M39 | | | HIGH |
| IO | DIFFIO_TX51p | | B2 | VREF2B2 | P27 | R28 | T34 | | | HIGH |
| IO | DIFFIO_TX51n | | B2 | VREF2B2 | R27 | R27 | T35 | | | HIGH |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pin Name/Function** | **Optional Function(s)** | **Configura-tion Function** | **Bank Number** | **VREF Bank** | **B956** | **F1020** | **F1508** | **DQS for x16** | **DQS for x32** | **DIFFIO Speed (1)** |
| IO | DIFFIO_RX50p | | B2 | VREF2B2 | H30 | K30 | N36 | | | HIGH |
| IO | DIFFIO_RX50n | | B2 | VREF2B2 | J30 | K29 | N37 | | | HIGH |
| IO | DIFFIO_TX50p | | B2 | VREF2B2 | R26 | P25 | U35 | | | HIGH |
| IO | DIFFIO_TX50n | | B2 | VREF2B2 | P26 | P26 | U34 | | | HIGH |
| IO | DIFFIO_RX49p | | B2 | VREF2B2 | F31 | J32 | N38 | | | HIGH |
| IO | DIFFIO_RX49n | | B2 | VREF2B2 | G31 | J31 | P38 | | | HIGH |
| IO | DIFFIO_TX49p | | B2 | VREF2B2 | N23 | R23 | U33 | | | HIGH |
| IO | DIFFIO_TX49n | | B2 | VREF2B2 | P23 | R24 | U32 | | | HIGH |
| IO | DIFFIO_RX48p | | B2 | VREF2B2 | H31 | K31 | P39 | | | HIGH |
| IO | DIFFIO_RX48n | | B2 | VREF2B2 | J31 | L32 | R38 | | | HIGH |
| IO | DIFFIO_TX48p | | B2 | VREF2B2 | T25 | R25 | V35 | | | HIGH |
| IO | DIFFIO_TX48n | | B2 | VREF2B2 | R25 | R26 | V34 | | | HIGH |
| IO | DIFFIO_RX47p/RUP2 | | B2 | VREF2B2 | K28 | M28 | P36 | | | HIGH |
| IO | DIFFIO_RX47n/RDN2 | | B2 | VREF2B2 | K29 | M29 | P37 | | | HIGH |
| IO | DIFFIO_TX47p | | B2 | VREF2B2 | | M23 | U31 | | | LOW |
| IO | DIFFIO_TX47n | | B2 | VREF2B2 | | M22 | U30 | | | LOW |
| IO | DIFFIO_RX46p | | B2 | VREF3B2 | M28 | L30 | R36 | | | HIGH |
| IO | DIFFIO_RX46n | | B2 | VREF3B2 | L28 | L31 | R37 | | | HIGH |
| IO | DIFFIO_TX46p | | B2 | VREF3B2 | | N22 | U29 | | | LOW |
| IO | DIFFIO_TX46n | | B2 | VREF3B2 | | P22 | U28 | | | LOW |
| IO | DIFFIO_RX45p | | B2 | VREF3B2 | M29 | M31 | T36 | | | HIGH |
| IO | DIFFIO_RX45n | | B2 | VREF3B2 | L29 | M30 | T37 | | | HIGH |
| IO | DIFFIO_TX45p | | B2 | VREF3B2 | | | V28 | | | LOW |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pin Name/Function** | **Optional Function(s)** | **Configura-tion Function** | **Bank Number** | **VREF Bank** | **B956** | **F1020** | **F1508** | | | |
| IO | DIFFIO_TX45n | | B2 | VREF3B2 | | | V27 | | | LOW |
| IO | DIFFIO_RX44p | | B2 | VREF3B2 | P28 | N29 | T39 | | | HIGH |
| IO | DIFFIO_RX44n | | B2 | VREF3B2 | N28 | N30 | T38 | | | HIGH |
| IO | DIFFIO_TX44p | | B2 | VREF3B2 | | | V29 | | | LOW |
| IO | DIFFIO_TX44n | | B2 | VREF3B2 | | | V30 | | | LOW |
| IO | DIFFIO_RX43p | | B2 | VREF3B2 | N29 | N31 | U36 | | | HIGH |
| IO | DIFFIO_RX43n | | B2 | VREF3B2 | P29 | N32 | U37 | | | HIGH |
| IO | DIFFIO_TX43p | | B2 | VREF3B2 | | | V32 | | | LOW |
| IO | DIFFIO_TX43n | | B2 | VREF3B2 | | | V31 | | | LOW |
| IO | DIFFIO_RX42p | | B2 | VREF3B2 | L30 | P29 | U38 | | | HIGH |
| IO | DIFFIO_RX42n | | B2 | VREF3B2 | K30 | P30 | U39 | | | HIGH |
| IO | DIFFIO_TX42p | | B2 | VREF3B2 | | | V33 | | | LOW |
| IO | DIFFIO_TX42n | | B2 | VREF3B2 | | | W34 | | | LOW |
| VREF3B2 | | | B2 | VREF3B2 | P22 | R21 | R29 | | | |
| IO | DIFFIO_RX41p | | B2 | VREF3B2 | N30 | P31 | V36 | | | HIGH |
| IO | DIFFIO_RX41n | | B2 | VREF3B2 | M30 | P32 | V37 | | | HIGH |
| IO | DIFFIO_TX41p | | B2 | VREF3B2 | | | V26 | | | LOW |
| IO | DIFFIO_TX41n | | B2 | VREF3B2 | | | W26 | | | LOW |
| IO | DIFFIO_RX40p | | B2 | VREF3B2 | L31 | R32 | V38 | | | HIGH |
| IO | DIFFIO_RX40n | | B2 | VREF3B2 | K31 | R31 | V39 | | | HIGH |
| IO | DIFFIO_TX40p | | B2 | VREF3B2 | | | W28 | | | LOW |
| IO | DIFFIO_TX40n | | B2 | VREF3B2 | | | W27 | | | LOW |
| IO | DIFFIO_RX39p | | B2 | VREF3B2 | R30 | R30 | W39 | | | HIGH |

**Table 7–1. Pin List for the Stratix EP1S80 Device**

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| IO | DIFFIO_RX39n | | B2 | VREF3B2 | P30 | R29 | W38 | | | HIGH |
| IO | DIFFIO_TX39p | | B2 | VREF3B2 | | | W29 | | | LOW |
| IO | DIFFIO_TX39n | | B2 | VREF3B2 | | | W30 | | | LOW |
| IO | DIFFIO_RX38p | | B2 | VREF3B2 | P31 | T32 | W37 | | | HIGH |
| IO | DIFFIO_RX38n | | B2 | VREF3B2 | R31 | T31 | W36 | | | HIGH |
| IO | DIFFIO_TX38p | | B2 | VREF3B2 | | | W31 | | | LOW |
| IO | DIFFIO_TX38n | | B2 | VREF3B2 | | | W32 | | | LOW |
| CLK0n | | | B2 | VREF3B2 | R28 | T30 | Y39 | | | |
| CLK0p | | | B2 | VREF3B2 | R29 | T29 | Y38 | | | |
| IO | CLK1n | | B2 | VREF3B2 | T30 | T28 | Y34 | | | |
| CLK1p | | | B2 | VREF3B2 | T31 | T27 | Y35 | | | |
| VCCINT | | | | | | | | | | |
| VCCA_PLL1 | | | | | R24 | T25 | AA32 | | | |
| GND | | | | | | | | | | |
| GNDA_PLL1 | | | | | T24 | T26 | Y31 | | | |
| VCCG_PLL1 | | | | | R22 | R22 | Y28 | | | |
| GNDG_PLL1 | | | | | R23 | T22 | Y29 | | | |
| VCCINT | | | | | | | | | | |
| VCCA_PLL2 | | | | | U24 | U25 | AA30 | | | |
| GND | | | | | | | | | | |
| GNDA_PLL2 | | | | | V24 | U26 | AA31 | | | |
| VCCG_PLL2 | | | | | U23 | U24 | AA28 | | | |
| GNDG_PLL2 | | | | | V23 | T24 | AA29 | | | |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pin Name/Function** | **Optional Function(s)** | **Configura-tion Function** | **Bank Number** | **VREF Bank** | **B956** | **F1020** | **F1508** | | | |
| CLK2p | | | B1 | VREF0B1 | T29 | U31 | Y37 | | | |
| CLK2n | | | B1 | VREF0B1 | T28 | U32 | Y36 | | | |
| CLK3p | | | B1 | VREF0B1 | U29 | U29 | AA35 | | | |
| IO | CLK3n | | B1 | VREF0B1 | U28 | U30 | AA34 | | | |
| IO | DIFFIO_RX37p | | B1 | VREF0B1 | U31 | U28 | AA39 | | | HIGH |
| IO | DIFFIO_RX37n | | B1 | VREF0B1 | V31 | U27 | AA38 | | | HIGH |
| IO | DIFFIO_TX37p | | B1 | VREF0B1 | | | Y27 | | | LOW |
| IO | DIFFIO_TX37n | | B1 | VREF0B1 | | | Y26 | | | LOW |
| IO | DIFFIO_RX36p | | B1 | VREF0B1 | AB31 | V32 | AA37 | | | HIGH |
| IO | DIFFIO_RX36n | | B1 | VREF0B1 | AA31 | V31 | AA36 | | | HIGH |
| IO | DIFFIO_TX36p | | B1 | VREF0B1 | | | Y33 | | | LOW |
| IO | DIFFIO_TX36n | | B1 | VREF0B1 | | | AA33 | | | LOW |
| IO | DIFFIO_RX35p | | B1 | VREF0B1 | V30 | V30 | AB38 | | | HIGH |
| IO | DIFFIO_RX35n | | B1 | VREF0B1 | U30 | V29 | AB39 | | | HIGH |
| IO | DIFFIO_TX35p | | B1 | VREF0B1 | | | AA27 | | | LOW |
| IO | DIFFIO_TX35n | | B1 | VREF0B1 | | | AA26 | | | LOW |
| IO | DIFFIO_RX34p | | B1 | VREF0B1 | W30 | W32 | AB37 | | | HIGH |
| IO | DIFFIO_RX34n | | B1 | VREF0B1 | Y30 | W31 | AB36 | | | HIGH |
| IO | DIFFIO_TX34p | | B1 | VREF0B1 | | | AB33 | | | LOW |
| IO | DIFFIO_TX34n | | B1 | VREF0B1 | | | AB32 | | | LOW |
| VREF0B1 | | | B1 | VREF0B1 | V22 | V21 | AE29 | | | |
| IO | DIFFIO_RX33p | | B1 | VREF0B1 | AA30 | W30 | AC39 | | | HIGH |
| IO | DIFFIO_RX33n | | B1 | VREF0B1 | AB30 | W29 | AC38 | | | HIGH |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| IO | DIFFIO_TX33p | | B1 | VREF0B1 | | | AB31 | | | LOW |
| IO | DIFFIO_TX33n | | B1 | VREF0B1 | | | AB30 | | | LOW |
| IO | DIFFIO_RX32p | | B1 | VREF0B1 | V29 | Y32 | AC37 | | | HIGH |
| IO | DIFFIO_RX32n | | B1 | VREF0B1 | W29 | Y31 | AC36 | | | HIGH |
| IO | DIFFIO_TX32p | | B1 | VREF0B1 | | | AB28 | | | LOW |
| IO | DIFFIO_TX32n | | B1 | VREF0B1 | | | AB29 | | | LOW |
| IO | DIFFIO_RX31p | | B1 | VREF0B1 | Y29 | Y30 | AD39 | | | HIGH |
| IO | DIFFIO_RX31n | | B1 | VREF0B1 | AA29 | Y29 | AD38 | | | HIGH |
| IO | DIFFIO_TX31p | | B1 | VREF0B1 | | U22 | AB27 | | | LOW |
| IO | DIFFIO_TX31n | | B1 | VREF0B1 | | V22 | AB26 | | | LOW |
| IO | DIFFIO_RX30p | | B1 | VREF0B1 | V28 | AA31 | AD37 | | | HIGH |
| IO | DIFFIO_RX30n | | B1 | VREF0B1 | W28 | AA30 | AD36 | | | HIGH |
| IO | DIFFIO_TX30p | | B1 | VREF0B1 | | W21 | AC26 | | | LOW |
| IO | DIFFIO_TX30n | | B1 | VREF0B1 | | W22 | AC27 | | | LOW |
| IO | DIFFIO_RX29p | | B1 | VREF0B1 | Y28 | AB31 | AE37 | | | HIGH |
| IO | DIFFIO_RX29n | | B1 | VREF0B1 | AA28 | AB30 | AE36 | | | HIGH |
| IO | DIFFIO_TX29p | | B1 | VREF0B1 | | Y21 | AC28 | | | LOW |
| IO | DIFFIO_TX29n | | B1 | VREF0B1 | | Y22 | AC29 | | | LOW |
| IO | DIFFIO_RX28p/RUP1 | | B1 | VREF1B1 | AB29 | AA28 | AF37 | | | HIGH |
| IO | DIFFIO_RX28n/RDN1 | | B1 | VREF1B1 | AB28 | AA29 | AF36 | | | HIGH |
| IO | DIFFIO_TX28p | | B1 | VREF1B1 | | AA22 | AC31 | | | LOW |
| IO | DIFFIO_TX28n | | B1 | VREF1B1 | | AB23 | AC30 | | | LOW |
| IO | DIFFIO_RX27p | | B1 | VREF1B1 | AC31 | AB32 | AE38 | | | HIGH |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| IO | DIFFIO_RX27n | | B1 | VREF1B1 | AD31 | AC31 | AF39 | | | HIGH |
| IO | DIFFIO_TX27p | | B1 | VREF1B1 | V25 | V26 | AB34 | | | HIGH |
| IO | DIFFIO_TX27n | | B1 | VREF1B1 | U25 | V25 | AB35 | | | HIGH |
| IO | DIFFIO_RX26p | | B1 | VREF1B1 | AE31 | AD32 | AF38 | | | HIGH |
| IO | DIFFIO_RX26n | | B1 | VREF1B1 | AF31 | AD31 | AG38 | | | HIGH |
| IO | DIFFIO_TX26p | | B1 | VREF1B1 | U26 | V28 | AC32 | | | HIGH |
| IO | DIFFIO_TX26n | | B1 | VREF1B1 | T26 | V27 | AC33 | | | HIGH |
| IO | DIFFIO_RX25p | | B1 | VREF1B1 | AC30 | AC29 | AG37 | | | HIGH |
| IO | DIFFIO_RX25n | | B1 | VREF1B1 | AD30 | AC30 | AG36 | | | HIGH |
| IO | DIFFIO_TX25p | | B1 | VREF1B1 | T27 | W25 | AC34 | | | HIGH |
| IO | DIFFIO_TX25n | | B1 | VREF1B1 | U27 | W26 | AC35 | | | HIGH |
| IO | DIFFIO_RX24p | | B1 | VREF1B1 | AF30 | AD30 | AH39 | | | HIGH |
| IO | DIFFIO_RX24n | | B1 | VREF1B1 | AE30 | AD29 | AH38 | | | HIGH |
| IO | DIFFIO_TX24p | | B1 | VREF1B1 | V26 | W27 | AD34 | | | HIGH |
| IO | DIFFIO_TX24n | | B1 | VREF1B1 | W26 | W28 | AD35 | | | HIGH |
| VREF1B1 | | | B1 | VREF1B1 | W22 | AA23 | AF29 | | | |
| IO | DIFFIO_RX23p | | B1 | VREF1B1 | AG30 | AE32 | AH37 | | | HIGH |
| IO | DIFFIO_RX23n | | B1 | VREF1B1 | AH30 | AE31 | AH36 | | | HIGH |
| IO | DIFFIO_TX23p | | B1 | VREF1B1 | W24 | V24 | AD33 | | | HIGH |
| IO | DIFFIO_TX23n | | B1 | VREF1B1 | Y24 | V23 | AD32 | | | HIGH |
| IO | DIFFIO_RX22p | | B1 | VREF1B1 | AC29 | AE30 | AJ39 | | | HIGH |
| IO | DIFFIO_RX22n | | B1 | VREF1B1 | AD29 | AE29 | AJ38 | | | HIGH |
| IO | DIFFIO_TX22p | | B1 | VREF1B1 | W25 | Y26 | AD31 | | | HIGH |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pin Name/Function** | **Optional Function(s)** | **Configura-tion Function** | **Bank Number** | **VREF Bank** | **B956** | **F1020** | **F1508** | | | |
| IO | DIFFIO_TX22n | | B1 | VREF1B1 | Y25 | Y25 | AD30 | | | HIGH |
| IO | DIFFIO_RX21p | | B1 | VREF1B1 | AE29 | AF32 | AJ37 | | | HIGH |
| IO | DIFFIO_RX21n | | B1 | VREF1B1 | AF29 | AF31 | AJ36 | | | HIGH |
| IO | DIFFIO_TX21p | | B1 | VREF1B1 | Y26 | Y28 | AE35 | | | HIGH |
| IO | DIFFIO_TX21n | | B1 | VREF1B1 | AA26 | Y27 | AE34 | | | HIGH |
| IO | DIFFIO_RX20p | | B1 | VREF1B1 | AH29 | AF30 | AK38 | | | HIGH |
| IO | DIFFIO_RX20n | | B1 | VREF1B1 | AG29 | AF29 | AK39 | | | HIGH |
| IO | DIFFIO_TX20p | | B1 | VREF1B1 | W23 | W23 | AE33 | | | HIGH |
| IO | DIFFIO_TX20n | | B1 | VREF1B1 | Y23 | W24 | AE32 | | | HIGH |
| IO | DIFFIO_RX19p | | B1 | VREF1B1 | AC28 | AG31 | AK37 | | | HIGH |
| IO | DIFFIO_RX19n | | B1 | VREF1B1 | AD28 | AG32 | AK36 | | | HIGH |
| IO | DIFFIO_TX19p | | B1 | VREF1B1 | V27 | Y23 | AF35 | | | HIGH |
| IO | DIFFIO_TX19n | | B1 | VREF1B1 | W27 | Y24 | AF34 | | | HIGH |
| IO | DIFFIO_RX18p | | B1 | VREF2B1 | AE28 | AG30 | AL37 | | | HIGH |
| IO | DIFFIO_RX18n | | B1 | VREF2B1 | AF28 | AG29 | AL36 | | | HIGH |
| IO | DIFFIO_TX18p | | B1 | VREF2B1 | Y27 | AA25 | AF33 | | | HIGH |
| IO | DIFFIO_TX18n | | B1 | VREF2B1 | AA27 | AA24 | AF32 | | | HIGH |
| IO | DIFFIO_RX17p | | B1 | VREF2B1 | | AH32 | | | | LOW |
| IO | DIFFIO_RX17n | | B1 | VREF2B1 | | AH31 | | | | LOW |
| IO | DIFFIO_TX17p | | B1 | VREF2B1 | AB27 | AA27 | AG35 | | | HIGH |
| IO | DIFFIO_TX17n | | B1 | VREF2B1 | AC27 | AA26 | AG34 | | | HIGH |
| IO | DIFFIO_RX16p | | B1 | VREF2B1 | | AG25 | | | | LOW |
| IO | DIFFIO_RX16n | | B1 | VREF2B1 | | AG26 | | | | LOW |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| IO | DIFFIO_TX16p | | B1 | VREF2B1 | AE27 | AB27 | AG33 | | | HIGH |
| IO | DIFFIO_TX16n | | B1 | VREF2B1 | AD27 | AB26 | AG32 | | | HIGH |
| IO | DIFFIO_RX15p | | B1 | VREF2B1 | | AH29 | | | | LOW |
| IO | DIFFIO_RX15n | | B1 | VREF2B1 | | AG28 | | | | LOW |
| IO | DIFFIO_TX15p | | B1 | VREF2B1 | AG27 | AC25 | AH34 | | | HIGH |
| IO | DIFFIO_TX15n | | B1 | VREF2B1 | AF27 | AC26 | AH35 | | | HIGH |
| IO | | | B1 | VREF2B1 | | | | | | |
| IO | | | B1 | VREF2B1 | | | | | | |
| IO | DIFFIO_TX14p | | B1 | VREF2B1 | AB26 | AC27 | AK35 | | | HIGH |
| IO | DIFFIO_TX14n | | B1 | VREF2B1 | AC26 | AC28 | AK34 | | | HIGH |
| VREF2B1 | | | B1 | VREF2B1 | Y22 | AB25 | AG29 | | | |
| IO | DIFFIO_RX13p | | B1 | VREF2B1 | | | AM39 | | | LOW |
| IO | DIFFIO_RX13n | | B1 | VREF2B1 | | | AM38 | | | LOW |
| IO | DIFFIO_TX13p | | B1 | VREF2B1 | AD26 | AD28 | AH33 | | | HIGH |
| IO | DIFFIO_TX13n | | B1 | VREF2B1 | AE26 | AD27 | AH32 | | | HIGH |
| IO | DIFFIO_RX12p | | B1 | VREF2B1 | | | AN39 | | | LOW |
| IO | DIFFIO_RX12n | | B1 | VREF2B1 | | | AN38 | | | LOW |
| IO | DIFFIO_TX12p | | B1 | VREF2B1 | AA25 | AD26 | AJ35 | | | HIGH |
| IO | DIFFIO_TX12n | | B1 | VREF2B1 | AB25 | AD25 | AJ34 | | | HIGH |
| IO | DIFFIO_RX11p | | B1 | VREF2B1 | | | AP38 | | | LOW |
| IO | DIFFIO_RX11n | | B1 | VREF2B1 | | | AP39 | | | LOW |
| IO | DIFFIO_TX11p | | B1 | VREF2B1 | AD25 | AE28 | AJ33 | | | HIGH |
| IO | DIFFIO_TX11n | | B1 | VREF2B1 | AC25 | AE27 | AJ32 | | | HIGH |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pin Name/Function** | **Optional Function(s)** | **Configura-tion Function** | **Bank Number** | **VREF Bank** | **B956** | **F1020** | **F1508** | | | |
| IO | DIFFIO_RX10p | | B1 | VREF2B1 | | | AR38 | | | LOW |
| IO | DIFFIO_RX10n | | B1 | VREF2B1 | | | AR39 | | | LOW |
| IO | DIFFIO_TX10p | | B1 | VREF2B1 | AA24 | AE25 | AK32 | | | HIGH |
| IO | DIFFIO_TX10n | | B1 | VREF2B1 | AB24 | AE26 | AK33 | | | HIGH |
| IO | DIFFIO_RX9p | | B1 | VREF2B1 | | | AT39 | | | LOW |
| IO | DIFFIO_RX9n | | B1 | VREF2B1 | | | AT38 | | | LOW |
| IO | DIFFIO_TX9p | | B1 | VREF2B1 | AD24 | AF27 | AL33 | | | HIGH |
| IO | DIFFIO_TX9n | | B1 | VREF2B1 | AC24 | AF28 | AL32 | | | HIGH |
| IO | DIFFIO_RX8p | | B1 | VREF3B1 | | | AM37 | | | LOW |
| IO | DIFFIO_RX8n | | B1 | VREF3B1 | | | AM36 | | | LOW |
| IO | DIFFIO_TX8p | | B1 | VREF3B1 | AE25 | AF26 | AH31 | | | HIGH |
| IO | DIFFIO_TX8n | | B1 | VREF3B1 | AF25 | AF25 | AH30 | | | HIGH |
| IO | DIFFIO_RX7p | | B1 | VREF3B1 | | | AN37 | | | LOW |
| IO | DIFFIO_RX7n | | B1 | VREF3B1 | | | AN36 | | | LOW |
| IO | DIFFIO_TX7p | | B1 | VREF3B1 | | | AE31 | | | LOW |
| IO | DIFFIO_TX7n | | B1 | VREF3B1 | | | AE30 | | | LOW |
| IO | DIFFIO_RX6p | | B1 | VREF3B1 | | | AP36 | | | LOW |
| IO | DIFFIO_RX6n | | B1 | VREF3B1 | | | AP37 | | | LOW |
| IO | DIFFIO_TX6p | | B1 | VREF3B1 | | | AF30 | | | LOW |
| IO | DIFFIO_TX6n | | B1 | VREF3B1 | | | AF31 | | | LOW |
| IO | DIFFIO_RX5p | | B1 | VREF3B1 | | | AR37 | | | LOW |
| IO | DIFFIO_RX5n | | B1 | VREF3B1 | | | AR36 | | | LOW |
| IO | DIFFIO_TX5p | | B1 | VREF3B1 | | | AG30 | | | LOW |

Table 7–1. Pin List for the Stratix EP1S80 Device

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pin Name/Function** | **Optional Function(s)** | **Configura-tion Function** | **Bank Number** | **VREF Bank** | **B956** | **F1020** | **F1508** | | | |
| IO | DIFFIO_TX5n | | B1 | VREF3B1 | | | AG31 | | | LOW |
| IO | DIFFIO_RX4p | | B1 | VREF3B1 | | | AU38 | | | LOW |
| IO | DIFFIO_RX4n | | B1 | VREF3B1 | | | AT37 | | | LOW |
| IO | DIFFIO_TX4p | | B1 | VREF3B1 | | | AD29 | | | LOW |
| IO | DIFFIO_TX4n | | B1 | VREF3B1 | | | AD28 | | | LOW |
| VREF3B1 | | | B1 | VREF3B1 | AA22 | AG27 | AH29 | | | |
| IO | DIFFIO_RX3p | | B1 | VREF3B1 | | | AL35 | | | LOW |
| IO | DIFFIO_RX3n | | B1 | VREF3B1 | | | AL34 | | | LOW |
| IO | DIFFIO_TX3p | | B1 | VREF3B1 | | | AD27 | | | LOW |
| IO | DIFFIO_TX3n | | B1 | VREF3B1 | | | AD26 | | | LOW |
| IO | DIFFIO_RX2p | | B1 | VREF3B1 | | | AM35 | | | LOW |
| IO | DIFFIO_RX2n | | B1 | VREF3B1 | | | AM34 | | | LOW |
| IO | DIFFIO_TX2p | | B1 | VREF3B1 | | | AE28 | | | LOW |
| IO | DIFFIO_TX2n | | B1 | VREF3B1 | | | AE27 | | | LOW |
| IO | DIFFIO_RX1p | | B1 | VREF3B1 | | | AN34 | | | LOW |
| IO | DIFFIO_RX1n | | B1 | VREF3B1 | | | AN35 | | | LOW |
| IO | DIFFIO_TX1p | | B1 | VREF3B1 | | | AF28 | | | LOW |
| IO | DIFFIO_TX1n | | B1 | VREF3B1 | | | AF27 | | | LOW |
| IO | DIFFIO_RX0p | | B1 | VREF3B1 | | | AP35 | | | LOW |
| IO | DIFFIO_RX0n | | B1 | VREF3B1 | | | AP34 | | | LOW |
| IO | DIFFIO_TX0p | | B1 | VREF3B1 | | | AF26 | | | LOW |
| IO | DIFFIO_TX0n | | B1 | VREF3B1 | | | AE26 | | | LOW |
| FPLL8CLKn | | | B1 | VREF3B1 | AG31 | AB29 | AL38 | | | |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| FPLL8CLKp | | | B1 | VREF3B1 | AH31 | AB28 | AL39 | | | |
| IO | | | B1 | VREF3B1 | | | AG28 | | | |
| IO | | | B1 | VREF3B1 | | | AH28 | | | |
| VCCINT | | | | | | | | | | |
| VCCA_PLL8 | | | | | AB23 | AJ31 | AJ30 | | | |
| GND | | | | | | | | | | |
| GNDA_PLL8 | | | | | AA23 | AJ32 | AJ31 | | | |
| VCCG_PLL8 | | | | | AD23 | AJ30 | AL31 | | | |
| GNDG_PLL8 | | | | | AC23 | AH30 | AK31 | | | |
| IO | | | B8 | VREF0B8 | | | | | | |
| IO | | | B8 | VREF0B8 | | | AR35 | | | |
| IO | | | B8 | VREF0B8 | | | AT36 | | | |
| IO | | | B8 | VREF0B8 | AG28 | AB24 | AN32 | | | |
| IO | | | B8 | VREF0B8 | | | AR34 | | | |
| IO | | | B8 | VREF0B8 | | | AU36 | | | |
| IO | | | B8 | VREF0B8 | | | AN33 | | | |
| IO | | | B8 | VREF0B8 | | | AL30 | | | |
| IO | | | B8 | VREF0B8 | | | AM31 | | | |
| IO | | | B8 | VREF0B8 | AF26 | AC24 | AT35 | | | |
| IO | DQ9B7 | | B8 | VREF0B8 | AK29 | AH28 | AV34 | DQ3B15 | DQ1B31 | |
| IO | | | B8 | VREF0B8 | | | AN31 | | | |
| IO | DQ9B6 | | B8 | VREF0B8 | AJ29 | AK30 | AU34 | DQ3B14 | DQ1B30 | |
| IO | | | B8 | VREF0B8 | | AD24 | AP33 | | | |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| IO | DQ9B5 | | B8 | VREF0B8 | AJ28 | AJ28 | AU33 | DQ3B13 | DQ1B29 | |
| IO | | | B8 | VREF0B8 | AE24 | AC23 | AV37 | | | |
| IO | DQ9B4 | | B8 | VREF0B8 | AL28 | AJ29 | AW33 | DQ3B12 | DQ1B28 | |
| IO | | | B8 | VREF0B8 | | AA21 | AR33 | | | |
| VREF0B8 | | | B8 | VREF0B8 | AB22 | AH27 | AJ29 | | | |
| IO | DQ9B3 | | B8 | VREF0B8 | AH27 | AK29 | AW34 | DQ3B11 | DQ1B27 | |
| IO | | | B8 | VREF0B8 | | AB22 | AK29 | | | |
| IO | DQS9B | | B8 | VREF0B8 | AK28 | AK28 | AV33 | | | |
| IO | | | B8 | VREF0B8 | AJ30 | AE24 | AP32 | | | |
| IO | DQ9B2 | | B8 | VREF0B8 | AL27 | AL30 | AV32 | DQ3B10 | DQ1B26 | |
| IO | | | B8 | VREF0B8 | | AD23 | AV35 | | | |
| IO | DQ9B1 | | B8 | VREF0B8 | AJ27 | AL29 | AU32 | DQ3B9 | DQ1B25 | |
| IO | | | B8 | VREF0B8 | | | AL29 | | | |
| IO | DQ9B0 | | B8 | VREF0B8 | AK27 | AM29 | AW32 | DQ3B8 | DQ1B24 | |
| IO | | | B8 | VREF0B8 | AH28 | AF24 | AT34 | | | |
| IO | | | B8 | VREF0B8 | | | AV36 | | | |
| IO | | | B8 | VREF0B8 | | | AP31 | | | |
| IO | | | B8 | VREF1B8 | | | AK28 | | | |
| IO | | | B8 | VREF1B8 | | | AU35 | | | |
| IO | | | B8 | VREF1B8 | | | AT33 | | | |
| IO | | | B8 | VREF1B8 | | | AL28 | | | |
| IO | | | B8 | VREF1B8 | | | AN30 | | | |
| IO | DQ8B7 | | B8 | VREF1B8 | AH26 | AH26 | AU31 | DQ3B7 | DQ1B23 | |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| IO | | | B8 | VREF1B8 | | | AM29 | | | |
| IO | DQ8B6 | | B8 | VREF1B8 | AG26 | AJ27 | AV31 | DQ3B6 | DQ1B22 | |
| IO | | | B8 | VREF1B8 | AD22 | AG24 | AR32 | | | |
| IO | DQ8B5 | | B8 | VREF1B8 | AK26 | AL28 | AW31 | DQ3B5 | DQ1B21 | |
| IO | | | B8 | VREF1B8 | | AC22 | AP30 | | | |
| IO | DQ8B4 | | B8 | VREF1B8 | AL26 | AK27 | AW30 | DQ3B4 | DQ1B20 | |
| IO | | | B8 | VREF1B8 | | AE23 | AK27 | | | |
| IO | DQ8B3 | | B8 | VREF1B8 | AH25 | AJ26 | AU30 | DQ3B3 | DQ1B19 | |
| IO | | | B8 | VREF1B8 | AC22 | AB21 | AW36 | | | |
| IO | DQS8B | | B8 | VREF1B8 | AJ26 | AL27 | AV30 | DQS3B | | |
| IO | | | B8 | VREF1B8 | | AF23 | AM28 | | | |
| IO | DQ8B2 | | B8 | VREF1B8 | AK25 | AM27 | AU29 | DQ3B2 | DQ1B18 | |
| VREF1B8 | | | B8 | VREF1B8 | AB21 | AH25 | AJ28 | | | |
| IO | | | B8 | VREF1B8 | | | AH27 | | | |
| IO | DQ8B1 | | B8 | VREF1B8 | AJ25 | AM28 | AV29 | DQ3B1 | DQ1B17 | |
| IO | | | B8 | VREF1B8 | AD21 | AD22 | AL27 | | | |
| IO | DQ8B0 | | B8 | VREF1B8 | AL25 | AK26 | AW29 | DQ3B0 | DQ1B16 | |
| IO | | | B8 | VREF1B8 | AE22 | AG23 | AT32 | | | |
| IO | | | B8 | VREF1B8 | | | AN28 | | | |
| IO | | | B8 | VREF1B8 | | | AG27 | | | |
| IO | | | B8 | VREF1B8 | | | AN29 | | | |
| IO | | | B8 | VREF1B8 | | | AR31 | | | |
| IO | | | B8 | VREF1B8 | | | AW35 | | | |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| IO | | | B8 | VREF1B8 | | | AR30 | | | |
| IO | | | B8 | VREF1B8 | | | AM27 | | | |
| IO | DQ7B7 | | B8 | VREF2B8 | AG24 | AH24 | AR28 | DQ2B15 | DQ1B15 | |
| IO | | | B8 | VREF2B8 | | | AK26 | | | |
| IO | DQ7B6 | | B8 | VREF2B8 | AH23 | AJ24 | AT28 | DQ2B14 | DQ1B14 | |
| IO | | | B8 | VREF2B8 | AC21 | AE22 | AL26 | | | |
| IO | DQ7B5 | | B8 | VREF2B8 | AK24 | AJ25 | AU28 | DQ2B13 | DQ1B13 | |
| IO | | | B8 | VREF2B8 | | AF22 | AT31 | | | |
| IO | DQ7B4 | | B8 | VREF2B8 | AH24 | AK25 | AV28 | DQ2B12 | DQ1B12 | |
| IO | | | B8 | VREF2B8 | AA21 | AC21 | AH26 | | | |
| IO | DQ7B3 | | B8 | VREF2B8 | AJ23 | AL25 | AR27 | DQ2B11 | DQ1B11 | |
| IO | | | B8 | VREF2B8 | | | AP29 | | | |
| IO | DQS7B | | B8 | VREF2B8 | AJ24 | AL26 | AT27 | | DQS1B | |
| IO | | | B8 | VREF2B8 | | AG22 | AP28 | | | |
| IO | DQ7B2 | | B8 | VREF2B8 | AL24 | AK24 | AW28 | DQ2B10 | DQ1B10 | |
| IO | | | B8 | VREF2B8 | AD20 | AG21 | AG26 | | | |
| IO | DQ7B1 | | B8 | VREF2B8 | AK23 | AM25 | AU27 | DQ2B9 | DQ1B9 | |
| IO | | | B8 | VREF2B8 | | | AR29 | | | |
| IO | DQ7B0 | | B8 | VREF2B8 | AL23 | AM26 | AV27 | DQ2B8 | DQ1B8 | |
| IO | | | B8 | VREF2B8 | | | AP27 | | | |
| VREF2B8 | | | B8 | VREF2B8 | AB20 | AH23 | AJ27 | | | |
| IO | | | B8 | VREF2B8 | | | AG25 | | | |
| IO | | | B8 | VREF2B8 | | | AH25 | | | |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
| IO | | | B8 | VREF2B8 | | | AT30 | | | |
| IO | | | B8 | VREF2B8 | | | AM26 | | | |
| IO | FCLK3 | | B8 | VREF2B8 | AF23 | AE21 | AT29 | | | |
| IO | FCLK2 | | B8 | VREF2B8 | AF22 | AF21 | AN26 | | | |
| IO | | | B8 | VREF2B8 | | | AK25 | | | |
| IO | DQ6B7 | | B8 | VREF2B8 | AG22 | AJ23 | AR26 | DQ2B7 | DQ1B7 | |
| IO | | | B8 | VREF2B8 | | | AN27 | | | |
| IO | DQ6B6 | | B8 | VREF2B8 | AH22 | AL24 | AT26 | DQ2B6 | DQ1B6 | |
| IO | | | B8 | VREF2B8 | | | AP26 | | | |
| IO | DQ6B5 | | B8 | VREF2B8 | AK22 | AH22 | AU26 | DQ2B5 | DQ1B5 | |
| IO | | | B8 | VREF3B8 | | AB20 | AF25 | | | |
| IO | DQ6B4 | | B8 | VREF3B8 | AG21 | AM24 | AV26 | DQ2B4 | DQ1B4 | |
| IO | | PGM2 | B8 | VREF3B8 | AF24 | AA20 | AL25 | | | |
| IO | DQ6B3 | | B8 | VREF3B8 | AH21 | AK23 | AW26 | DQ2B3 | DQ1B3 | |
| IO | | | B8 | VREF3B8 | | AD21 | AM25 | | | |
| IO | DQS6B | | B8 | VREF3B8 | AJ22 | AJ22 | AU25 | DQS2B | | |
| IO | | | B8 | VREF3B8 | | AD20 | AF24 | | | |
| IO | DQ6B2 | | B8 | VREF3B8 | AL22 | AL23 | AT25 | DQ2B2 | DQ1B2 | |
| IO | | | B8 | VREF3B8 | AE21 | AF20 | AN25 | | | |
| IO | DQ6B1 | | B8 | VREF3B8 | AJ21 | AK22 | AR25 | DQ2B1 | DQ1B1 | |
| IO | | | B8 | VREF3B8 | | | AP25 | | | |
| IO | DQ6B0 | | B8 | VREF3B8 | AK21 | AL22 | AV25 | DQ2B0 | DQ1B0 | |
| IO | RDN8 | | B8 | VREF3B8 | AE23 | AC20 | AH24 | | | |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pin Name/Function** | **Optional Function(s)** | **Configura-tion Function** | **Bank Number** | **VREF Bank** | **B956** | **F1020** | **F1508** | | | |
| IO | RUP8 | | B8 | VREF3B8 | AG25 | AH19 | AF23 | | | |
| IO | | | B8 | VREF3B8 | | | AJ24 | | | |
| IO | | | B8 | VREF3B8 | | | AL24 | | | |
| IO | | | B8 | VREF3B8 | | | AN24 | | | |
| IO | | | B8 | VREF3B8 | | | AM24 | | | |
| VREF3B8 | | | B8 | VREF3B8 | AB19 | AH21 | AJ26 | | | |
| IO | | | B8 | VREF3B8 | | | AG24 | | | |
| IO | | | B8 | VREF3B8 | AC20 | AE20 | AK24 | | | |
| IO | DQ5B7 | | B8 | VREF3B8 | AG20 | AM22 | AT24 | | | |
| IO | | | B8 | VREF3B8 | | | AP24 | | | |
| IO | DQ5B6 | | B8 | VREF3B8 | AH20 | AJ21 | AU24 | | | |
| IO | | | B8 | VREF3B8 | AE20 | AG20 | AR24 | | | |
| IO | DQ5B5 | | B8 | VREF3B8 | AK20 | AK21 | AV24 | | | |
| IO | | | B8 | VREF3B8 | AD19 | AB19 | AG23 | | | |
| IO | DQ5B4 | | B8 | VREF3B8 | AL20 | AL21 | AW24 | | | |
| IO | | RDYnBSY | B8 | VREF3B8 | AG23 | AA19 | AH23 | | | |
| IO | DQ5B3 | | B8 | VREF3B8 | AG19 | AH20 | AW23 | | | |
| IO | | | B8 | VREF3B8 | | AK18 | AP23 | | | |
| IO | DQS5B | | B8 | VREF4B8 | AJ20 | AJ20 | AU23 | | | |
| IO | | | B8 | VREF4B8 | AC19 | AD19 | AK23 | | | |
| IO | DQ5B2 | | B8 | VREF4B8 | AH19 | AK20 | AR23 | | | |
| IO | | nCS | B8 | VREF4B8 | AF20 | AC19 | AL23 | | | |
| IO | DQ5B1 | | B8 | VREF4B8 | AJ19 | AL20 | AV23 | | | |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pin Name/Function** | **Optional Function(s)** | **Configura-tion Function** | **Bank Number** | **VREF Bank** | **B956** | **F1020** | **F1508** | | | |
| IO | | | B8 | VREF4B8 | AE18 | AJ18 | AM23 | | | |
| IO | DQ5B0 | | B8 | VREF4B8 | AK19 | AM20 | AT23 | | | |
| IO | | | B8 | VREF4B8 | | | AF22 | | | |
| IO | | CS | B8 | VREF4B8 | AF21 | AG19 | AJ23 | | | |
| IO | | | B8 | VREF4B8 | AE19 | | AG22 | | | |
| IO | | | B8 | VREF4B8 | | | AN23 | | | |
| IO | | | B8 | VREF4B8 | | | AR22 | | | |
| IO | | | B8 | VREF4B8 | | | AH22 | | | |
| IO | | | B8 | VREF4B8 | | | AF21 | | | |
| IO | | | B8 | VREF4B8 | AA19 | AH18 | AJ22 | | | |
| IO | | | B8 | VREF4B8 | | | AL22 | | | |
| IO | | | B8 | VREF4B8 | | | AP22 | | | |
| IO | | | B8 | VREF4B8 | | | AN22 | | | |
| VREF4B8 | | | B8 | VREF4B8 | AB18 | | AJ25 | | | |
| IO | CLK5n | | B8 | VREF4B8 | AH18 | AJ19 | AU22 | | | |
| CLK5p | | | B8 | VREF4B8 | AJ18 | AK19 | AT22 | | | |
| IO | CLK4n | | B8 | VREF4B8 | AK18 | AL19 | AW22 | | | |
| CLK4p | | | B8 | VREF4B8 | AL18 | AM19 | AV22 | | | |
| PLL_ENA | | PLL_ENA | B8 | VREF4B8 | AF19 | AF19 | AM22 | | | |
| MSEL0 | | MSEL0 | B8 | VREF4B8 | AF18 | AG18 | AP21 | | | |
| MSEL1 | | MSEL1 | B8 | VREF4B8 | AG18 | AE18 | AG21 | | | |
| MSEL2 | | MSEL2 | B8 | VREF4B8 | AG17 | AE19 | AM21 | | | |
| IO | PLL6_OUT3n | | B12 | VREF4B8 | AL17 | AM18 | AV20 | | | |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| IO | PLL6_OUT3p | | B12 | VREF4B8 | AK17 | AL18 | AW20 | | | |
| IO | PLL6_OUT2n | | B12 | VREF4B8 | AJ17 | AK17 | AW21 | | | |
| IO | PLL6_OUT2p | | B12 | VREF4B8 | AH17 | AJ17 | AV21 | | | |
| IO | PLL6_FBn | | B11 | VREF4B8 | AJ15 | AM17 | AU20 | | | |
| IO | PLL6_FBp | | B11 | VREF4B8 | AH15 | AL17 | AT20 | | | |
| IO | PLL6_OUT1n | | B11 | VREF4B8 | AL15 | AK16 | AU21 | | | |
| IO | PLL6_OUT1p | | B11 | VREF4B8 | AK15 | AJ16 | AT21 | | | |
| IO | PLL6_OUT0n | | B11 | VREF4B8 | AL16 | AM16 | AU19 | | | |
| IO | PLL6_OUT0p | | B11 | VREF4B8 | AK16 | AL16 | AT19 | | | |
| VCC_PLL6_OUTB | | | B12 | | AC18 | AB17 | AH21 | | | |
| VCC_PLL6_OUTB | | | B12 | | | | | | | |
| VCC_PLL6_OUTA | | | B11 | | AD17 | AE17 | AJ21 | | | |
| VCC_PLL6_OUTA | | | B11 | | | | | | | |
| VCCINT | | | | | | | | | | |
| VCCA_PLL6 | | | | | AB17 | AG17 | AK21 | | | |
| GND | | | | | | | | | | |
| GNDA_PLL6 | | | | | AC17 | AH17 | AL20 | | | |
| VCCG_PLL6 | | | | | AD15 | AD16 | AJ20 | | | |
| GNDG_PLL6 | | | | | AD16 | AB16 | AH20 | | | |
| VCCINT | | | | | | | | | | |
| VCCA_PLL12 | | | | | AC14 | AG16 | AK19 | | | |
| GND | | | | | | | | | | |
| GNDA_PLL12 | | | | | AD14 | AH16 | AL19 | | | |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pin Name/Function** | **Optional Function(s)** | **Configura-tion Function** | **Bank Number** | **VREF Bank** | **B956** | **F1020** | **F1508** | | | |
| VCCG_PLL12 | | | | | AC15 | AF16 | AJ19 | | | |
| GNDG_PLL12 | | | | | AB15 | AE16 | AH19 | | | |
| CLK7p | | | B7 | VREF0B7 | AJ14 | AM15 | AW18 | | | |
| IO | CLK7n | | B7 | VREF0B7 | AH14 | AL15 | AV18 | | | |
| CLK6p | | | B7 | VREF0B7 | AL14 | AK15 | AW19 | | | |
| IO | CLK6n/PLL12_OUT | | B7 | VREF0B7 | AK14 | AJ15 | AV19 | | | |
| nCE | | nCE | B7 | VREF0B7 | AF17 | AF18 | AN20 | | | |
| nCEO | | nCEO | B7 | VREF0B7 | AF16 | AH15 | AP20 | | | |
| IO | | | B7 | VREF0B7 | | | AF20 | | | |
| IO | | | B7 | VREF0B7 | | | AG19 | | | |
| IO | | PGM0 | B7 | VREF0B7 | AE17 | AD18 | AG20 | | | |
| nIO_PULLUP | | nIO_PULLUP | B7 | VREF0B7 | AE16 | AF15 | AR20 | | | |
| VCCSEL | | VCCSEL | B7 | VREF0B7 | AE15 | AJ14 | AM19 | | | |
| PORSEL | | PORSEL | B7 | VREF0B7 | AG16 | AG15 | AN19 | | | |
| IO | | | B7 | VREF0B7 | | | AK18 | | | |
| IO | | | B7 | VREF0B7 | | | AF19 | | | |
| IO | | INIT_DONE | B7 | VREF0B7 | AF15 | AE15 | AL18 | | | |
| IO | | | B7 | VREF0B7 | | | AM18 | | | |
| IO | | | B7 | VREF0B7 | | | AP19 | | | |
| IO | | | B7 | VREF0B7 | | | AR19 | | | |
| VREF0B7 | | | B7 | VREF0B7 | AB14 | AH12 | AJ15 | | | |
| IO | | | B7 | VREF0B7 | | | AH18 | | | |
| IO | | | B7 | VREF0B7 | | | AG18 | | | |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| IO | | | B7 | VREF0B7 | | | AJ18 | | | |
| IO | | | B7 | VREF0B7 | AH16 | AC18 | AP18 | | | |
| IO | | | B7 | VREF0B7 | | | AN18 | | | |
| IO | | | B7 | VREF0B7 | | | AR18 | | | |
| IO | | | B7 | VREF0B7 | | | AG17 | | | |
| IO | | | B7 | VREF0B7 | | | AH17 | | | |
| IO | | | B7 | VREF0B7 | AA16 | AA18 | AF18 | | | |
| IO | | nRS | B7 | VREF0B7 | AE14 | AB18 | AL17 | | | |
| IO | | | B7 | VREF0B7 | | | AT18 | | | |
| IO | DQ4B7 | | B7 | VREF0B7 | AK13 | AL13 | AU17 | | | |
| IO | | | B7 | VREF0B7 | AA15 | AC15 | AJ17 | | | |
| IO | DQ4B6 | | B7 | VREF0B7 | AG13 | AM13 | AR17 | | | |
| IO | | RUnLU | B7 | VREF0B7 | AJ16 | AF14 | AK17 | | | |
| IO | DQ4B5 | | B7 | VREF0B7 | AH13 | AH13 | AT17 | | | |
| IO | | | B7 | VREF0B7 | | AD15 | AU18 | | | |
| IO | DQ4B4 | | B7 | VREF0B7 | AJ13 | AJ13 | AV17 | | | |
| IO | | | B7 | VREF1B7 | AC13 | AE14 | AF17 | | | |
| IO | DQ4B3 | | B7 | VREF1B7 | AK12 | AK13 | AV16 | | | |
| IO | | PGM1 | B7 | VREF1B7 | AG15 | AG14 | AF16 | | | |
| IO | DQS4B | | B7 | VREF1B7 | AJ12 | AJ12 | AU16 | | | |
| IO | | | B7 | VREF1B7 | AD13 | AK14 | AM17 | | | |
| IO | DQ4B2 | | B7 | VREF1B7 | AL12 | AK12 | AW17 | | | |
| IO | | | B7 | VREF1B7 | | AB15 | AG16 | | | |

**Table 7–1. Pin List for the Stratix EP1S80 Device**

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| IO | DQ4B1 | | B7 | VREF1B7 | AG12 | AL12 | AT16 | | | |
| IO | DEV_CLRn | | B7 | VREF1B7 | AF14 | AH14 | AN17 | | | |
| IO | DQ4B0 | | B7 | VREF1B7 | AH12 | AM11 | AW16 | | | |
| IO | | | B7 | VREF1B7 | AE13 | AL14 | AM16 | | | |
| IO | | | B7 | VREF1B7 | | | AP16 | | | |
| VREF1B7 | | | B7 | VREF1B7 | AB13 | | AJ14 | | | |
| IO | | | B7 | VREF1B7 | | | AK16 | | | |
| IO | | | B7 | VREF1B7 | | | AH16 | | | |
| IO | | | B7 | VREF1B7 | | | AL16 | | | |
| IO | | | B7 | VREF1B7 | | | AJ16 | | | |
| IO | RDN7 | | B7 | VREF1B7 | AG14 | AC14 | AP17 | | | |
| IO | RUP7 | | B7 | VREF1B7 | AF13 | AF13 | AN16 | | | |
| IO | DQ3B7 | | B7 | VREF1B7 | AL10 | AL10 | AT15 | DQ1B15 | DQ0B31 | |
| IO | | | B7 | VREF1B7 | | AE13 | AF15 | | | |
| IO | DQ3B6 | | B7 | VREF1B7 | AJ11 | AK11 | AR15 | DQ1B14 | DQ0B30 | |
| IO | | | B7 | VREF1B7 | | AD14 | AP15 | | | |
| IO | DQ3B5 | | B7 | VREF1B7 | AK11 | AL11 | AV15 | DQ1B13 | DQ0B29 | |
| IO | | | B7 | VREF1B7 | AA13 | AG13 | AR16 | | | |
| IO | DQ3B4 | | B7 | VREF1B7 | AG11 | AK10 | AV14 | DQ1B12 | DQ0B28 | |
| IO | | | B7 | VREF1B7 | AC12 | | AG15 | | | |
| IO | DQ3B3 | | B7 | VREF1B7 | AH11 | AM9 | AW14 | DQ1B11 | DQ0B27 | |
| IO | | | B7 | VREF1B7 | | AA15 | AM15 | | | |
| IO | DQS3B | | B7 | VREF1B7 | AJ10 | AJ11 | AU15 | DQS1B | | |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| IO | | | B7 | VREF1B7 | AA11 | AG12 | AN15 | | | |
| IO | DQ3B2 | | B7 | VREF2B7 | AG10 | AL9 | AR14 | DQ1B10 | DQ0B26 | |
| IO | | | B7 | VREF2B7 | | AB14 | AK15 | | | |
| IO | DQ3B1 | | B7 | VREF2B7 | AH10 | AJ10 | AT14 | DQ1B9 | DQ0B25 | |
| IO | | | B7 | VREF2B7 | | AD13 | AL15 | | | |
| IO | DQ3B0 | | B7 | VREF2B7 | AK10 | AH11 | AU14 | DQ1B8 | DQ0B24 | |
| IO | | | B7 | VREF2B7 | | | AP14 | | | |
| IO | | | B7 | VREF2B7 | | | AH15 | | | |
| IO | | | B7 | VREF2B7 | | | AG14 | | | |
| IO | | | B7 | VREF2B7 | | | AM14 | | | |
| IO | | | B7 | VREF2B7 | | | AR11 | | | |
| IO | FCLK5 | | B7 | VREF2B7 | AF12 | AM14 | AN14 | | | |
| IO | FCLK4 | | B7 | VREF2B7 | AF11 | AF12 | AT11 | | | |
| VREF2B7 | | | B7 | VREF2B7 | AB12 | AH10 | AJ13 | | | |
| IO | | | B7 | VREF2B7 | | | AH14 | | | |
| IO | DQ2B7 | | B7 | VREF2B7 | AL8 | AL8 | AT13 | DQ1B7 | DQ0B23 | |
| IO | | | B7 | VREF2B7 | AD12 | AC13 | AP12 | | | |
| IO | DQ2B6 | | B7 | VREF2B7 | AK9 | AJ9 | AU13 | DQ1B6 | DQ0B22 | |
| IO | | | B7 | VREF2B7 | | | AP13 | | | |
| IO | DQ2B5 | | B7 | VREF2B7 | AL9 | AK9 | AV13 | DQ1B5 | DQ0B21 | |
| IO | | | B7 | VREF2B7 | AC11 | AA14 | AG13 | | | |
| IO | DQ2B4 | | B7 | VREF2B7 | AH8 | AM8 | AV12 | DQ1B4 | DQ0B20 | |
| IO | | | B7 | VREF2B7 | AE12 | AE12 | AN12 | | | |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| IO | DQ2B3 | | B7 | VREF2B7 | AK8 | AH9 | AR13 | DQ1B3 | DQ0B19 | |
| IO | | | B7 | VREF2B7 | | | AN13 | | | |
| IO | DQS2B | | B7 | VREF2B7 | AJ8 | AK8 | AU12 | | DQS0B | |
| IO | | | B7 | VREF2B7 | AD11 | AD12 | AK14 | | | |
| IO | DQ2B2 | | B7 | VREF2B7 | AG8 | AM7 | AR12 | DQ1B2 | DQ0B18 | |
| IO | | | B7 | VREF2B7 | AE11 | AF11 | AL14 | | | |
| IO | DQ2B1 | | B7 | VREF2B7 | AH9 | AJ8 | AT12 | DQ1B1 | DQ0B17 | |
| IO | | | B7 | VREF2B7 | | AG11 | AT10 | | | |
| IO | DQ2B0 | | B7 | VREF2B7 | AJ9 | AL7 | AW12 | DQ1B0 | DQ0B16 | |
| IO | | | B7 | VREF3B7 | | | AR9 | | | |
| IO | | | B7 | VREF3B7 | | | AH13 | | | |
| IO | | | B7 | VREF3B7 | AF10 | AB13 | AR10 | | | |
| IO | | | B7 | VREF3B7 | | | AT8 | | | |
| IO | | | B7 | VREF3B7 | | | AM13 | | | |
| IO | | | B7 | VREF3B7 | | | AP11 | | | |
| IO | | | B7 | VREF3B7 | | | AM12 | | | |
| IO | | | B7 | VREF3B7 | AC10 | AC12 | AH12 | | | |
| IO | DQ1B7 | | B7 | VREF3B7 | AK7 | AL6 | AV11 | DQ0B15 | DQ0B15 | |
| IO | | | B7 | VREF3B7 | | AE11 | AL13 | | | |
| IO | DQ1B6 | | B7 | VREF3B7 | AL7 | AM6 | AW11 | DQ0B14 | DQ0B14 | |
| IO | | | B7 | VREF3B7 | AG9 | AG10 | AT9 | | | |
| VREF3B7 | | | B7 | VREF3B7 | AB11 | AH8 | AJ12 | | | |
| IO | DQ1B5 | | B7 | VREF3B7 | AH6 | AJ7 | AU10 | DQ0B13 | DQ0B13 | |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| IO | | | B7 | VREF3B7 | AG7 | AD11 | AK13 | | | |
| IO | DQ1B4 | | B7 | VREF3B7 | AK6 | AM5 | AW10 | DQ0B12 | DQ0B12 | |
| IO | | | B7 | VREF3B7 | AE10 | AF10 | AW5 | | | |
| IO | DQ1B3 | | B7 | VREF3B7 | AL6 | AK7 | AU11 | DQ0B11 | DQ0B11 | |
| IO | | | B7 | VREF3B7 | | | AN11 | | | |
| IO | DQS1B | | B7 | VREF3B7 | AJ6 | AH7 | AV10 | DQS0B | | |
| IO | | | B7 | VREF3B7 | AD10 | AE10 | AM11 | | | |
| IO | DQ1B2 | | B7 | VREF3B7 | AH7 | AL5 | AW9 | DQ0B10 | DQ0B10 | |
| IO | | | B7 | VREF3B7 | AF9 | AG9 | AR8 | | | |
| IO | DQ1B1 | | B7 | VREF3B7 | AJ7 | AK6 | AV9 | DQ0B9 | DQ0B9 | |
| IO | | | B7 | VREF3B7 | | AA13 | AP10 | | | |
| IO | DQ1B0 | | B7 | VREF3B7 | AG6 | AJ6 | AU9 | DQ0B8 | DQ0B8 | |
| IO | | | B7 | VREF3B7 | | | AK12 | | | |
| IO | | | B7 | VREF3B7 | | | AL12 | | | |
| IO | | | B7 | VREF3B7 | | | AT7 | | | |
| IO | | | B7 | VREF3B7 | | | AW4 | | | |
| IO | | | B7 | VREF3B7 | | | AN10 | | | |
| IO | | | B7 | VREF4B7 | | | AL11 | | | |
| IO | | | B7 | VREF4B7 | | | AK11 | | | |
| IO | | | B7 | VREF4B7 | AE9 | AB12 | AV4 | | | |
| IO | DQ0B7 | | B7 | VREF4B7 | AL4 | AL3 | AV8 | DQ0B7 | DQ0B7 | |
| IO | | | B7 | VREF4B7 | | AF9 | AP9 | | | |
| IO | DQ0B6 | | B7 | VREF4B7 | AL5 | AL4 | AW8 | DQ0B6 | DQ0B6 | |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pin Name/Function** | **Optional Function(s)** | **Configura-tion Function** | **Bank Number** | **VREF Bank** | **B956** | **F1020** | **F1508** | | | |
| IO | | | B7 | VREF4B7 | AJ2 | AE9 | AU4 | | | |
| IO | DQ0B5 | | B7 | VREF4B7 | AJ4 | AM4 | AW6 | DQ0B5 | DQ0B5 | |
| IO | | | B7 | VREF4B7 | AH4 | AD10 | AR7 | | | |
| IO | DQ0B4 | | B7 | VREF4B7 | AK3 | AJ4 | AU8 | DQ0B4 | DQ0B4 | |
| IO | | | B7 | VREF4B7 | | | AV5 | | | |
| IO | DQ0B3 | | B7 | VREF4B7 | AK5 | AJ5 | AW7 | DQ0B3 | DQ0B3 | |
| VREF4B7 | | | B7 | VREF4B7 | AB10 | AH6 | AJ11 | | | |
| IO | | | B7 | VREF4B7 | AG4 | AB11 | AR6 | | | |
| IO | DQS0B | | B7 | VREF4B7 | AK4 | AK5 | AV7 | | | |
| IO | | | B7 | VREF4B7 | | AA12 | AP8 | | | |
| IO | DQ0B2 | | B7 | VREF4B7 | AH5 | AH5 | AU7 | DQ0B2 | DQ0B2 | |
| IO | | | B7 | VREF4B7 | AF8 | AC11 | AU5 | | | |
| IO | DQ0B1 | | B7 | VREF4B7 | AJ5 | AK3 | AV6 | DQ0B1 | DQ0B1 | |
| IO | | | B7 | VREF4B7 | | AD9 | AL10 | | | |
| IO | DQ0B0 | | B7 | VREF4B7 | AJ3 | AK4 | AU6 | DQ0B0 | DQ0B0 | |
| IO | | | B7 | VREF4B7 | AE8 | | AT5 | | | |
| IO | | | B7 | VREF4B7 | | | AM9 | | | |
| IO | | | B7 | VREF4B7 | | | AN9 | | | |
| IO | | | B7 | VREF4B7 | | | AV3 | | | |
| IO | | | B7 | VREF4B7 | | | AR5 | | | |
| IO | | | B7 | VREF4B7 | | | AN7 | | | |
| IO | | | B7 | VREF4B7 | AF6 | AC9 | AN8 | | | |
| IO | | | B7 | VREF4B7 | | | AT4 | | | |

**Table 7–1. Pin List for the Stratix EP1S80 Device**

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| IO | | | B7 | VREF4B7 | | | AT6 | | | |
| IO | | | B7 | VREF4B7 | | | AP7 | | | |
| GNDG_PLL9 | | | | | AC9 | AH3 | AK9 | | | |
| VCCG_PLL9 | | | | | AD9 | AJ3 | AL9 | | | |
| GNDA_PLL9 | | | | | AA9 | AJ1 | AJ9 | | | |
| GND | | | | | | | | | | |
| VCCA_PLL9 | | | | | AB9 | AJ2 | AJ10 | | | |
| VCCINT | | | | | | | | | | |
| IO | | | B6 | VREF0B6 | | | AF13 | | | |
| IO | | | B6 | VREF0B6 | | | AF14 | | | |
| FPLL9CLKp | | | B6 | VREF0B6 | AH1 | AB5 | AL1 | | | |
| FPLL9CLKn | | | B6 | VREF0B6 | AG1 | AB4 | AL2 | | | |
| IO | DIFFIO_TX151n | | B6 | VREF0B6 | | | AF12 | | | LOW |
| IO | DIFFIO_TX151p | | B6 | VREF0B6 | | | AG12 | | | LOW |
| IO | DIFFIO_RX151n | | B6 | VREF0B6 | | | AP6 | | | LOW |
| IO | DIFFIO_RX151p | | B6 | VREF0B6 | | | AP5 | | | LOW |
| IO | DIFFIO_TX150n | | B6 | VREF0B6 | | | AE12 | | | LOW |
| IO | DIFFIO_TX150p | | B6 | VREF0B6 | | | AE13 | | | LOW |
| IO | DIFFIO_RX150n | | B6 | VREF0B6 | | | AN5 | | | LOW |
| IO | DIFFIO_RX150p | | B6 | VREF0B6 | | | AN6 | | | LOW |
| IO | DIFFIO_TX149n | | B6 | VREF0B6 | | | AG10 | | | LOW |
| IO | DIFFIO_TX149p | | B6 | VREF0B6 | | | AG9 | | | LOW |
| IO | DIFFIO_RX149n | | B6 | VREF0B6 | | | AM6 | | | LOW |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| IO | DIFFIO_RX149p | | B6 | VREF0B6 | | | AM5 | | | LOW |
| IO | DIFFIO_TX148n | | B6 | VREF0B6 | | | AF10 | | | LOW |
| IO | DIFFIO_TX148p | | B6 | VREF0B6 | | | AF9 | | | LOW |
| IO | DIFFIO_RX148n | | B6 | VREF0B6 | | | AL6 | | | LOW |
| IO | DIFFIO_RX148p | | B6 | VREF0B6 | | | AL5 | | | LOW |
| VREF0B6 | | | B6 | VREF0B6 | V10 | AG6 | AE11 | | | |
| IO | DIFFIO_TX147n | | B6 | VREF0B6 | | | AE14 | | | LOW |
| IO | DIFFIO_TX147p | | B6 | VREF0B6 | | | AD14 | | | LOW |
| IO | DIFFIO_RX147n | | B6 | VREF0B6 | | | AR4 | | | LOW |
| IO | DIFFIO_RX147p | | B6 | VREF0B6 | | | AR3 | | | LOW |
| IO | DIFFIO_TX146n | | B6 | VREF0B6 | | | AE9 | | | LOW |
| IO | DIFFIO_TX146p | | B6 | VREF0B6 | | | AE10 | | | LOW |
| IO | DIFFIO_RX146n | | B6 | VREF0B6 | | | AT3 | | | LOW |
| IO | DIFFIO_RX146p | | B6 | VREF0B6 | | | AU2 | | | LOW |
| IO | DIFFIO_TX145n | | B6 | VREF0B6 | | | AC13 | | | LOW |
| IO | DIFFIO_TX145p | | B6 | VREF0B6 | | | AD13 | | | LOW |
| IO | DIFFIO_RX145n | | B6 | VREF0B6 | | | AP3 | | | LOW |
| IO | DIFFIO_RX145p | | B6 | VREF0B6 | | | AP4 | | | LOW |
| IO | DIFFIO_TX144n | | B6 | VREF0B6 | | | AD12 | | | LOW |
| IO | DIFFIO_TX144p | | B6 | VREF0B6 | | | AD11 | | | LOW |
| IO | DIFFIO_RX144n | | B6 | VREF0B6 | | | AN4 | | | LOW |
| IO | DIFFIO_RX144p | | B6 | VREF0B6 | | | AN3 | | | LOW |
| IO | DIFFIO_TX143n | | B6 | VREF0B6 | AC8 | AF8 | AH10 | | | HIGH |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pin Name/Function** | **Optional Function(s)** | **Configura-tion Function** | **Bank Number** | **VREF Bank** | **B956** | **F1020** | **F1508** | | | |
| IO | DIFFIO_TX143p | | B6 | VREF0B6 | AD8 | AF7 | AH9 | | | HIGH |
| IO | DIFFIO_RX143n | | B6 | VREF0B6 | | | AM4 | | | LOW |
| IO | DIFFIO_RX143p | | B6 | VREF0B6 | | | AM3 | | | LOW |
| IO | DIFFIO_TX142n | | B6 | VREF1B6 | AF7 | AF5 | AL8 | | | HIGH |
| IO | DIFFIO_TX142p | | B6 | VREF1B6 | AE7 | AF6 | AL7 | | | HIGH |
| IO | DIFFIO_RX142n | | B6 | VREF1B6 | | | AT2 | | | LOW |
| IO | DIFFIO_RX142p | | B6 | VREF1B6 | | | AT1 | | | LOW |
| IO | DIFFIO_TX141n | | B6 | VREF1B6 | AB8 | AE7 | AK7 | | | HIGH |
| IO | DIFFIO_TX141p | | B6 | VREF1B6 | AA8 | AE8 | AK8 | | | HIGH |
| IO | DIFFIO_RX141n | | B6 | VREF1B6 | | | AR2 | | | LOW |
| IO | DIFFIO_RX141p | | B6 | VREF1B6 | | | AR1 | | | LOW |
| IO | DIFFIO_TX140n | | B6 | VREF1B6 | AC7 | AD6 | AJ7 | | | HIGH |
| IO | DIFFIO_TX140p | | B6 | VREF1B6 | AD7 | AD5 | AJ8 | | | HIGH |
| IO | DIFFIO_RX140n | | B6 | VREF1B6 | | | AP1 | | | LOW |
| IO | DIFFIO_RX140p | | B6 | VREF1B6 | | | AP2 | | | LOW |
| IO | DIFFIO_TX139n | | B6 | VREF1B6 | AB7 | AE6 | AH8 | | | HIGH |
| IO | DIFFIO_TX139p | | B6 | VREF1B6 | AA7 | AE5 | AH7 | | | HIGH |
| IO | DIFFIO_RX139n | | B6 | VREF1B6 | | | AN2 | | | LOW |
| IO | DIFFIO_RX139p | | B6 | VREF1B6 | | | AN1 | | | LOW |
| IO | DIFFIO_TX138n | | B6 | VREF1B6 | AE6 | AD8 | AG8 | | | HIGH |
| IO | DIFFIO_TX138p | | B6 | VREF1B6 | AD6 | AD7 | AG7 | | | HIGH |
| IO | DIFFIO_RX138n | | B6 | VREF1B6 | | | AM2 | | | LOW |
| IO | DIFFIO_RX138p | | B6 | VREF1B6 | | | AM1 | | | LOW |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pin Name/Function** | **Optional Function(s)** | **Configura-tion Function** | **Bank Number** | **VREF Bank** | **B956** | **F1020** | **F1508** | | | |
| VREF1B6 | | | B6 | VREF1B6 | W10 | AB8 | AF11 | | | |
| IO | DIFFIO_TX137n | | B6 | VREF1B6 | AC6 | AC5 | AK6 | | | HIGH |
| IO | DIFFIO_TX137p | | B6 | VREF1B6 | AB6 | AC6 | AK5 | | | HIGH |
| IO | | | B6 | VREF1B6 | | | | | | |
| IO | | | B6 | VREF1B6 | | | | | | |
| IO | DIFFIO_TX136n | | B6 | VREF1B6 | AF5 | AC7 | AJ5 | | | HIGH |
| IO | DIFFIO_TX136p | | B6 | VREF1B6 | AG5 | AC8 | AJ6 | | | HIGH |
| IO | DIFFIO_RX135n | | B6 | VREF1B6 | | AH2 | | | | LOW |
| IO | DIFFIO_RX135p | | B6 | VREF1B6 | | AH1 | | | | LOW |
| IO | DIFFIO_TX135n | | B6 | VREF1B6 | AD5 | AB7 | AH5 | | | HIGH |
| IO | DIFFIO_TX135p | | B6 | VREF1B6 | AE5 | AB6 | AH6 | | | HIGH |
| IO | DIFFIO_RX136n | | B6 | VREF1B6 | | AG5 | | | | LOW |
| IO | DIFFIO_RX136p | | B6 | VREF1B6 | | AH4 | | | | LOW |
| IO | DIFFIO_TX134n | | B6 | VREF1B6 | AC5 | AA6 | AG6 | | | HIGH |
| IO | DIFFIO_TX134p | | B6 | VREF1B6 | AB5 | AA7 | AG5 | | | HIGH |
| IO | DIFFIO_RX137n | | B6 | VREF1B6 | | AG7 | | | | LOW |
| IO | DIFFIO_RX137p | | B6 | VREF1B6 | | AG8 | | | | LOW |
| IO | DIFFIO_TX133n | | B6 | VREF1B6 | AA6 | AA9 | AF8 | | | HIGH |
| IO | DIFFIO_TX133p | | B6 | VREF1B6 | Y6 | AA8 | AF7 | | | HIGH |
| IO | DIFFIO_RX133n | | B6 | VREF1B6 | AF4 | AG4 | AL4 | | | HIGH |
| IO | DIFFIO_RX133p | | B6 | VREF1B6 | AE4 | AG3 | AL3 | | | HIGH |
| IO | DIFFIO_TX132n | | B6 | VREF2B6 | Y9 | Y5 | AF6 | | | HIGH |
| IO | DIFFIO_TX132p | | B6 | VREF2B6 | W9 | Y6 | AF5 | | | HIGH |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| IO | DIFFIO_RX132n | | B6 | VREF2B6 | AD4 | AG1 | AK4 | | | HIGH |
| IO | DIFFIO_RX132p | | B6 | VREF2B6 | AC4 | AG2 | AK3 | | | HIGH |
| IO | DIFFIO_TX131n | | B6 | VREF2B6 | Y8 | Y7 | AE8 | | | HIGH |
| IO | DIFFIO_TX131p | | B6 | VREF2B6 | W8 | Y8 | AE7 | | | HIGH |
| IO | DIFFIO_RX131n | | B6 | VREF2B6 | AG3 | AF4 | AK1 | | | HIGH |
| IO | DIFFIO_RX131p | | B6 | VREF2B6 | AH3 | AF3 | AK2 | | | HIGH |
| IO | DIFFIO_TX130n | | B6 | VREF2B6 | AA5 | W5 | AE6 | | | HIGH |
| IO | DIFFIO_TX130p | | B6 | VREF2B6 | Y5 | W6 | AE5 | | | HIGH |
| IO | DIFFIO_RX130n | | B6 | VREF2B6 | AF3 | AF2 | AJ4 | | | HIGH |
| IO | DIFFIO_RX130p | | B6 | VREF2B6 | AE3 | AF1 | AJ3 | | | HIGH |
| IO | DIFFIO_TX129n | | B6 | VREF2B6 | Y7 | Y10 | AD10 | | | HIGH |
| IO | DIFFIO_TX129p | | B6 | VREF2B6 | W7 | Y9 | AD9 | | | HIGH |
| IO | DIFFIO_RX129n | | B6 | VREF2B6 | AD3 | AE4 | AJ2 | | | HIGH |
| IO | DIFFIO_RX129p | | B6 | VREF2B6 | AC3 | AE3 | AJ1 | | | HIGH |
| IO | DIFFIO_TX128n | | B6 | VREF2B6 | U7 | W10 | AD8 | | | HIGH |
| IO | DIFFIO_TX128p | | B6 | VREF2B6 | V7 | W9 | AD7 | | | HIGH |
| IO | DIFFIO_RX128n | | B6 | VREF2B6 | AH2 | AE2 | AH4 | | | HIGH |
| IO | DIFFIO_RX128p | | B6 | VREF2B6 | AG2 | AE1 | AH3 | | | HIGH |
| VREF2B6 | | | B6 | VREF2B6 | Y10 | AA10 | AG11 | | | |
| IO | DIFFIO_TX127n | | B6 | VREF2B6 | W6 | V9 | AD5 | | | HIGH |
| IO | DIFFIO_TX127p | | B6 | VREF2B6 | V6 | V10 | AD6 | | | HIGH |
| IO | DIFFIO_RX127n | | B6 | VREF2B6 | AE2 | AC3 | AH1 | | | HIGH |
| IO | DIFFIO_RX127p | | B6 | VREF2B6 | AF2 | AC4 | AH2 | | | HIGH |

**Table 7–1. Pin List for the Stratix EP1S80 Device**

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| IO | DIFFIO_TX126n | | B6 | VREF2B6 | U6 | V5 | AC5 | | | HIGH |
| IO | DIFFIO_TX126p | | B6 | VREF2B6 | T6 | V6 | AC6 | | | HIGH |
| IO | DIFFIO_RX126n | | B6 | VREF2B6 | AD2 | AD3 | AG4 | | | HIGH |
| IO | DIFFIO_RX126p | | B6 | VREF2B6 | AC2 | AD4 | AG3 | | | HIGH |
| IO | DIFFIO_TX125n | | B6 | VREF2B6 | W5 | V8 | AC7 | | | HIGH |
| IO | DIFFIO_TX125p | | B6 | VREF2B6 | V5 | V7 | AC8 | | | HIGH |
| IO | DIFFIO_RX125n | | B6 | VREF2B6 | AF1 | AD2 | AG2 | | | HIGH |
| IO | DIFFIO_RX125p | | B6 | VREF2B6 | AE1 | AD1 | AF2 | | | HIGH |
| IO | DIFFIO_TX124n | | B6 | VREF2B6 | T5 | W8 | AB5 | | | HIGH |
| IO | DIFFIO_TX124p | | B6 | VREF2B6 | U5 | W7 | AB6 | | | HIGH |
| IO | DIFFIO_RX124n | | B6 | VREF2B6 | AD1 | AC2 | AF1 | | | HIGH |
| IO | DIFFIO_RX124p | | B6 | VREF2B6 | AC1 | AB1 | AE2 | | | HIGH |
| IO | DIFFIO_TX123n | | B6 | VREF2B6 | | AB9 | AC11 | | | LOW |
| IO | DIFFIO_TX123p | | B6 | VREF2B6 | | AC10 | AC12 | | | LOW |
| IO | DIFFIO_RX123n/RDN6 | | B6 | VREF2B6 | AB4 | AA4 | AF4 | | | HIGH |
| IO | DIFFIO_RX123p/RUP6 | | B6 | VREF2B6 | AB3 | AA5 | AF3 | | | HIGH |
| IO | DIFFIO_TX122n | | B6 | VREF3B6 | | AB10 | AC9 | | | LOW |
| IO | DIFFIO_TX122p | | B6 | VREF3B6 | | AA11 | AC10 | | | LOW |
| IO | DIFFIO_RX122n | | B6 | VREF3B6 | Y4 | AB3 | AE4 | | | HIGH |
| IO | DIFFIO_RX122p | | B6 | VREF3B6 | AA4 | AB2 | AE3 | | | HIGH |
| IO | DIFFIO_TX121n | | B6 | VREF3B6 | | Y11 | AC14 | | | LOW |
| IO | DIFFIO_TX121p | | B6 | VREF3B6 | | Y12 | AB14 | | | LOW |
| IO | DIFFIO_RX121n | | B6 | VREF3B6 | W4 | AA3 | AD4 | | | HIGH |

**Table 7–1. Pin List for the Stratix EP1S80 Device**

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| IO | DIFFIO_RX121p | | B6 | VREF3B6 | V4 | AA2 | AD3 | | | HIGH |
| IO | DIFFIO_TX120n | | B6 | VREF3B6 | | W11 | AB13 | | | LOW |
| IO | DIFFIO_TX120p | | B6 | VREF3B6 | | W12 | AB12 | | | LOW |
| IO | DIFFIO_RX120n | | B6 | VREF3B6 | AA3 | Y4 | AD2 | | | HIGH |
| IO | DIFFIO_RX120p | | B6 | VREF3B6 | Y3 | Y3 | AD1 | | | HIGH |
| IO | DIFFIO_TX119n | | B6 | VREF3B6 | | | AB10 | | | LOW |
| IO | DIFFIO_TX119p | | B6 | VREF3B6 | | | AB11 | | | LOW |
| IO | DIFFIO_RX119n | | B6 | VREF3B6 | W3 | Y2 | AC4 | | | HIGH |
| IO | DIFFIO_RX119p | | B6 | VREF3B6 | V3 | Y1 | AC3 | | | HIGH |
| IO | DIFFIO_TX118n | | B6 | VREF3B6 | | | AB8 | | | LOW |
| IO | DIFFIO_TX118p | | B6 | VREF3B6 | | | AB9 | | | LOW |
| IO | DIFFIO_RX118n | | B6 | VREF3B6 | AB2 | W4 | AC2 | | | HIGH |
| IO | DIFFIO_RX118p | | B6 | VREF3B6 | AA2 | W3 | AC1 | | | HIGH |
| VREF3B6 | | | B6 | VREF3B6 | AA10 | V12 | AH11 | | | |
| IO | DIFFIO_TX117n | | B6 | VREF3B6 | | | AA12 | | | LOW |
| IO | DIFFIO_TX117p | | B6 | VREF3B6 | | | AA13 | | | LOW |
| IO | DIFFIO_RX117n | | B6 | VREF3B6 | Y2 | W2 | AB4 | | | HIGH |
| IO | DIFFIO_RX117p | | B6 | VREF3B6 | W2 | W1 | AB3 | | | HIGH |
| IO | DIFFIO_TX116n | | B6 | VREF3B6 | | | AA11 | | | LOW |
| IO | DIFFIO_TX116p | | B6 | VREF3B6 | | | AA10 | | | LOW |
| IO | DIFFIO_RX116n | | B6 | VREF3B6 | AA1 | V4 | AB1 | | | HIGH |
| IO | DIFFIO_RX116p | | B6 | VREF3B6 | AB1 | V3 | AB2 | | | HIGH |
| IO | DIFFIO_TX115n | | B6 | VREF3B6 | | | AA9 | | | LOW |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pin Name/Function** | **Optional Function(s)** | **Configura-tion Function** | **Bank Number** | **VREF Bank** | **B956** | **F1020** | **F1508** | | | |
| IO | DIFFIO_TX115p | | B6 | VREF3B6 | | | AA8 | | | LOW |
| IO | DIFFIO_RX115n | | B6 | VREF3B6 | V2 | V2 | AA4 | | | HIGH |
| IO | DIFFIO_RX115p | | B6 | VREF3B6 | U2 | V1 | AA3 | | | HIGH |
| IO | DIFFIO_TX114n | | B6 | VREF3B6 | | | AB7 | | | LOW |
| IO | DIFFIO_TX114p | | B6 | VREF3B6 | | | AA6 | | | LOW |
| IO | DIFFIO_RX114n | | B6 | VREF3B6 | V1 | U5 | AA2 | | | HIGH |
| IO | DIFFIO_RX114p | | B6 | VREF3B6 | U1 | U6 | AA1 | | | HIGH |
| IO | CLK8n | | B6 | VREF3B6 | U4 | U3 | Y5 | | | |
| CLK8p | | | B6 | VREF3B6 | U3 | U4 | Y6 | | | |
| CLK9n | | | B6 | VREF3B6 | T3 | U1 | Y2 | | | |
| CLK9p | | | B6 | VREF3B6 | T4 | U2 | Y1 | | | |
| GNDG_PLL3 | | | | | V9 | U11 | Y11 | | | |
| VCCG_PLL3 | | | | | U9 | V11 | Y12 | | | |
| GNDA_PLL3 | | | | | V8 | U7 | Y9 | | | |
| GND | | | | | | | | | | |
| VCCA_PLL3 | | | | | U8 | U8 | W8 | | | |
| VCCINT | | | | | | | | | | |
| GNDG_PLL4 | | | | | R9 | U9 | W11 | | | |
| VCCG_PLL4 | | | | | R10 | T9 | W12 | | | |
| GNDA_PLL4 | | | | | R8 | T7 | W9 | | | |
| GND | | | | | | | | | | |
| VCCA_PLL4 | | | | | T8 | T8 | W10 | | | |
| VCCINT | | | | | | | | | | |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| CLK10p | | | B5 | VREF0B5 | T1 | T6 | Y3 | | | |
| IO | CLK10n | | B5 | VREF0B5 | T2 | T5 | Y4 | | | |
| CLK11p | | | B5 | VREF0B5 | R3 | T4 | W5 | | | |
| CLK11n | | | B5 | VREF0B5 | R4 | T3 | W6 | | | |
| IO | DIFFIO_TX113n | | B5 | VREF0B5 | | | Y7 | | | LOW |
| IO | DIFFIO_TX113p | | B5 | VREF0B5 | | | W7 | | | LOW |
| IO | DIFFIO_RX113n | | B5 | VREF0B5 | R1 | T2 | W1 | | | HIGH |
| IO | DIFFIO_RX113p | | B5 | VREF0B5 | P1 | T1 | W2 | | | HIGH |
| IO | DIFFIO_TX112n | | B5 | VREF0B5 | | | AA14 | | | LOW |
| IO | DIFFIO_TX112p | | B5 | VREF0B5 | | | Y14 | | | LOW |
| IO | DIFFIO_RX112n | | B5 | VREF0B5 | P2 | R1 | W4 | | | HIGH |
| IO | DIFFIO_RX112p | | B5 | VREF0B5 | R2 | R2 | W3 | | | HIGH |
| IO | DIFFIO_TX111n | | B5 | VREF0B5 | | | W13 | | | LOW |
| IO | DIFFIO_TX111p | | B5 | VREF0B5 | | | Y13 | | | LOW |
| IO | DIFFIO_RX111n | | B5 | VREF0B5 | K1 | R3 | V1 | | | HIGH |
| IO | DIFFIO_RX111p | | B5 | VREF0B5 | L1 | R4 | V2 | | | HIGH |
| IO | DIFFIO_TX110n | | B5 | VREF0B5 | | | W14 | | | LOW |
| IO | DIFFIO_TX110p | | B5 | VREF0B5 | | | V14 | | | LOW |
| IO | DIFFIO_RX110n | | B5 | VREF0B5 | N2 | P1 | V3 | | | HIGH |
| IO | DIFFIO_RX110p | | B5 | VREF0B5 | M2 | P2 | V4 | | | HIGH |
| VREF0B5 | | | B5 | VREF0B5 | L10 | R12 | M11 | | | |
| IO | DIFFIO_TX109n | | B5 | VREF0B5 | | | V7 | | | LOW |
| IO | DIFFIO_TX109p | | B5 | VREF0B5 | | | V8 | | | LOW |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| IO | DIFFIO_RX109n | | B5 | VREF0B5 | L2 | P3 | U1 | | | HIGH |
| IO | DIFFIO_RX109p | | B5 | VREF0B5 | K2 | P4 | U2 | | | HIGH |
| IO | DIFFIO_TX108n | | B5 | VREF0B5 | | | V9 | | | LOW |
| IO | DIFFIO_TX108p | | B5 | VREF0B5 | | | V10 | | | LOW |
| IO | DIFFIO_RX108n | | B5 | VREF0B5 | P3 | N1 | U3 | | | HIGH |
| IO | DIFFIO_RX108p | | B5 | VREF0B5 | N3 | N2 | U4 | | | HIGH |
| IO | DIFFIO_TX107n | | B5 | VREF0B5 | | | V11 | | | LOW |
| IO | DIFFIO_TX107p | | B5 | VREF0B5 | | | V12 | | | LOW |
| IO | DIFFIO_RX107n | | B5 | VREF0B5 | L3 | N3 | T2 | | | HIGH |
| IO | DIFFIO_RX107p | | B5 | VREF0B5 | M3 | N4 | T1 | | | HIGH |
| IO | DIFFIO_TX106n | | B5 | VREF0B5 | | | U13 | | | LOW |
| IO | DIFFIO_TX106p | | B5 | VREF0B5 | | | V13 | | | LOW |
| IO | DIFFIO_RX106n | | B5 | VREF0B5 | P4 | M2 | T3 | | | HIGH |
| IO | DIFFIO_RX106p | | B5 | VREF0B5 | N4 | M3 | T4 | | | HIGH |
| IO | DIFFIO_TX105n | | B5 | VREF0B5 | | T11 | U9 | | | LOW |
| IO | DIFFIO_TX105p | | B5 | VREF0B5 | | R11 | U10 | | | LOW |
| IO | DIFFIO_RX105n | | B5 | VREF0B5 | M4 | L2 | R3 | | | HIGH |
| IO | DIFFIO_RX105p | | B5 | VREF0B5 | L4 | L3 | R4 | | | HIGH |
| IO | DIFFIO_TX104n | | B5 | VREF1B5 | | P11 | U12 | | | LOW |
| IO | DIFFIO_TX104p | | B5 | VREF1B5 | | N11 | U11 | | | LOW |
| IO | DIFFIO_RX104n/RDN5 | | B5 | VREF1B5 | K3 | M4 | P3 | | | HIGH |
| IO | DIFFIO_RX104p/RUP5 | | B5 | VREF1B5 | K4 | M5 | P4 | | | HIGH |
| IO | DIFFIO_TX103n | | B5 | VREF1B5 | R7 | R7 | V6 | | | HIGH |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pin Name/Function** | **Optional Function(s)** | **Configura-tion Function** | **Bank Number** | **VREF Bank** | **B956** | **F1020** | **F1508** | | | |
| IO | DIFFIO_TX103p | | B5 | VREF1B5 | T7 | R8 | V5 | | | HIGH |
| IO | DIFFIO_RX103n | | B5 | VREF1B5 | J1 | L1 | R2 | | | HIGH |
| IO | DIFFIO_RX103p | | B5 | VREF1B5 | H1 | K2 | P1 | | | HIGH |
| IO | DIFFIO_TX102n | | B5 | VREF1B5 | P8 | P7 | U8 | | | HIGH |
| IO | DIFFIO_TX102p | | B5 | VREF1B5 | N8 | P8 | U7 | | | HIGH |
| IO | DIFFIO_RX102n | | B5 | VREF1B5 | G1 | J2 | P2 | | | HIGH |
| IO | DIFFIO_RX102p | | B5 | VREF1B5 | F1 | J1 | N2 | | | HIGH |
| IO | DIFFIO_TX101n | | B5 | VREF1B5 | R6 | R5 | U6 | | | HIGH |
| IO | DIFFIO_TX101p | | B5 | VREF1B5 | P6 | R6 | U5 | | | HIGH |
| IO | DIFFIO_RX101n | | B5 | VREF1B5 | H2 | K4 | N4 | | | HIGH |
| IO | DIFFIO_RX101p | | B5 | VREF1B5 | J2 | K3 | N3 | | | HIGH |
| IO | DIFFIO_TX100n | | B5 | VREF1B5 | P9 | R10 | T5 | | | HIGH |
| IO | DIFFIO_TX100p | | B5 | VREF1B5 | N9 | R9 | T6 | | | HIGH |
| IO | DIFFIO_RX100n | | B5 | VREF1B5 | G2 | J3 | M1 | | | HIGH |
| IO | DIFFIO_RX100p | | B5 | VREF1B5 | F2 | J4 | M2 | | | HIGH |
| VREF1B5 | | | B5 | VREF1B5 | M10 | L8 | N11 | | | |
| IO | DIFFIO_TX99n | | B5 | VREF1B5 | P7 | P6 | T7 | | | HIGH |
| IO | DIFFIO_TX99p | | B5 | VREF1B5 | N7 | P5 | T8 | | | HIGH |
| IO | DIFFIO_RX99n | | B5 | VREF1B5 | J3 | H1 | M3 | | | HIGH |
| IO | DIFFIO_RX99p | | B5 | VREF1B5 | H3 | H2 | M4 | | | HIGH |
| IO | DIFFIO_TX98n | | B5 | VREF1B5 | N6 | N7 | T9 | | | HIGH |
| IO | DIFFIO_TX98p | | B5 | VREF1B5 | M6 | N8 | T10 | | | HIGH |
| IO | DIFFIO_RX98n | | B5 | VREF1B5 | G3 | G1 | L1 | | | HIGH |

**Table 7–1. Pin List for the Stratix EP1S80 Device**

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| IO | DIFFIO_RX98p | | B5 | VREF1B5 | F3 | G2 | L2 | | | HIGH |
| IO | DIFFIO_TX97n | | B5 | VREF1B5 | R5 | P9 | R5 | | | HIGH |
| IO | DIFFIO_TX97p | | B5 | VREF1B5 | P5 | P10 | R6 | | | HIGH |
| IO | DIFFIO_RX97n | | B5 | VREF1B5 | J4 | H3 | L3 | | | HIGH |
| IO | DIFFIO_RX97p | | B5 | VREF1B5 | H4 | H4 | L4 | | | HIGH |
| IO | DIFFIO_TX96n | | B5 | VREF1B5 | M5 | N5 | R8 | | | HIGH |
| IO | DIFFIO_TX96p | | B5 | VREF1B5 | N5 | N6 | R7 | | | HIGH |
| IO | DIFFIO_RX96n | | B5 | VREF1B5 | G4 | F1 | K2 | | | HIGH |
| IO | DIFFIO_RX96p | | B5 | VREF1B5 | F4 | F2 | K1 | | | HIGH |
| IO | DIFFIO_TX95n | | B5 | VREF1B5 | M8 | N10 | P5 | | | HIGH |
| IO | DIFFIO_TX95p | | B5 | VREF1B5 | L8 | N9 | P6 | | | HIGH |
| IO | DIFFIO_RX95n | | B5 | VREF1B5 | E2 | G3 | K3 | | | HIGH |
| IO | DIFFIO_RX95p | | B5 | VREF1B5 | D2 | G4 | K4 | | | HIGH |
| IO | DIFFIO_TX94n | | B5 | VREF2B5 | M7 | M8 | P7 | | | HIGH |
| IO | DIFFIO_TX94p | | B5 | VREF2B5 | L7 | M9 | P8 | | | HIGH |
| IO | DIFFIO_RX94n | | B5 | VREF2B5 | E3 | F3 | J3 | | | HIGH |
| IO | DIFFIO_RX94p | | B5 | VREF2B5 | D3 | F4 | J4 | | | HIGH |
| IO | DIFFIO_TX93n | | B5 | VREF2B5 | L5 | M6 | N5 | | | HIGH |
| IO | DIFFIO_TX93p | | B5 | VREF2B5 | K5 | M7 | N6 | | | HIGH |
| IO | DIFFIO_RX90n | | B5 | VREF2B5 | | E2 | | | | LOW |
| IO | DIFFIO_RX90p | | B5 | VREF2B5 | | E1 | | | | LOW |
| IO | DIFFIO_TX92n | | B5 | VREF2B5 | H5 | L6 | N8 | | | HIGH |
| IO | DIFFIO_TX92p | | B5 | VREF2B5 | J5 | L7 | N7 | | | HIGH |

**Table 7–1. Pin List for the Stratix EP1S80 Device**

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| IO | DIFFIO_RX91n | | B5 | VREF2B5 | | F5 | | | | LOW |
| IO | DIFFIO_RX91p | | B5 | VREF2B5 | | E4 | | | | LOW |
| IO | DIFFIO_TX91n | | B5 | VREF2B5 | F5 | K5 | M6 | | | HIGH |
| IO | DIFFIO_TX91p | | B5 | VREF2B5 | G5 | K6 | M5 | | | HIGH |
| IO | | | B5 | VREF2B5 | | | | | | |
| IO | | | B5 | VREF2B5 | | | | | | |
| IO | DIFFIO_TX90n | | B5 | VREF2B5 | L6 | K8 | L5 | | | HIGH |
| IO | DIFFIO_TX90p | | B5 | VREF2B5 | K6 | K7 | L6 | | | HIGH |
| IO | | | B5 | VREF2B5 | | | | | | |
| IO | | | B5 | VREF2B5 | | | | | | |
| VREF2B5 | | | B5 | VREF2B5 | N10 | F6 | P11 | | | |
| IO | DIFFIO_TX89n | | B5 | VREF2B5 | J6 | J5 | M7 | | | HIGH |
| IO | DIFFIO_TX89p | | B5 | VREF2B5 | H6 | J6 | M8 | | | HIGH |
| IO | DIFFIO_RX89n | | B5 | VREF2B5 | | | H2 | | | LOW |
| IO | DIFFIO_RX89p | | B5 | VREF2B5 | | | H1 | | | LOW |
| IO | DIFFIO_TX88n | | B5 | VREF2B5 | G6 | J7 | K5 | | | HIGH |
| IO | DIFFIO_TX88p | | B5 | VREF2B5 | F6 | J8 | K6 | | | HIGH |
| IO | DIFFIO_RX88n | | B5 | VREF2B5 | | | G2 | | | LOW |
| IO | DIFFIO_RX88p | | B5 | VREF2B5 | | | G1 | | | LOW |
| IO | DIFFIO_TX87n | | B5 | VREF2B5 | K8 | H5 | L8 | | | HIGH |
| IO | DIFFIO_TX87p | | B5 | VREF2B5 | J8 | H6 | L7 | | | HIGH |
| IO | DIFFIO_RX87n | | B5 | VREF2B5 | | | F1 | | | LOW |
| IO | DIFFIO_RX87p | | B5 | VREF2B5 | | | F2 | | | LOW |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pin Name/Function** | **Optional Function(s)** | **Configura-tion Function** | **Bank Number** | **VREF Bank** | **B956** | **F1020** | **F1508** | | | |
| IO | DIFFIO_TX86n | | B5 | VREF2B5 | K7 | H8 | K7 | | | HIGH |
| IO | DIFFIO_TX86p | | B5 | VREF2B5 | J7 | H7 | K8 | | | HIGH |
| IO | DIFFIO_RX86n | | B5 | VREF2B5 | | | E1 | | | LOW |
| IO | DIFFIO_RX86p | | B5 | VREF2B5 | | | E2 | | | LOW |
| IO | DIFFIO_TX85n | | B5 | VREF2B5 | H7 | G6 | J7 | | | HIGH |
| IO | DIFFIO_TX85p | | B5 | VREF2B5 | G7 | G5 | J8 | | | HIGH |
| IO | DIFFIO_RX85n | | B5 | VREF2B5 | | | D1 | | | LOW |
| IO | DIFFIO_RX85p | | B5 | VREF2B5 | | | D2 | | | LOW |
| IO | DIFFIO_TX84n | | B5 | VREF3B5 | G8 | G7 | M9 | | | HIGH |
| IO | DIFFIO_TX84p | | B5 | VREF3B5 | H8 | G8 | M10 | | | HIGH |
| IO | DIFFIO_RX84n | | B5 | VREF3B5 | | | H3 | | | LOW |
| IO | DIFFIO_RX84p | | B5 | VREF3B5 | | | H4 | | | LOW |
| IO | DIFFIO_TX83n | | B5 | VREF3B5 | | | R10 | | | LOW |
| IO | DIFFIO_TX83p | | B5 | VREF3B5 | | | R9 | | | LOW |
| IO | DIFFIO_RX83n | | B5 | VREF3B5 | | | G4 | | | LOW |
| IO | DIFFIO_RX83p | | B5 | VREF3B5 | | | G3 | | | LOW |
| IO | DIFFIO_TX82n | | B5 | VREF3B5 | | | P10 | | | LOW |
| IO | DIFFIO_TX82p | | B5 | VREF3B5 | | | P9 | | | LOW |
| IO | DIFFIO_RX82n | | B5 | VREF3B5 | | | F3 | | | LOW |
| IO | DIFFIO_RX82p | | B5 | VREF3B5 | | | F4 | | | LOW |
| IO | DIFFIO_TX81n | | B5 | VREF3B5 | | | N9 | | | LOW |
| IO | DIFFIO_TX81p | | B5 | VREF3B5 | | | N10 | | | LOW |
| IO | DIFFIO_RX81n | | B5 | VREF3B5 | | | E3 | | | LOW |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pin Name/Function** | **Optional Function(s)** | **Configura-tion Function** | **Bank Number** | **VREF Bank** | **B956** | **F1020** | **F1508** | | | |
| IO | DIFFIO_RX81p | | B5 | VREF3B5 | | | E4 | | | LOW |
| IO | DIFFIO_TX80n | | B5 | VREF3B5 | | | T13 | | | LOW |
| IO | DIFFIO_TX80p | | B5 | VREF3B5 | | | U14 | | | LOW |
| IO | DIFFIO_RX80n | | B5 | VREF3B5 | | | C2 | | | LOW |
| IO | DIFFIO_RX80p | | B5 | VREF3B5 | | | D3 | | | LOW |
| VREF3B5 | | | B5 | VREF3B5 | P10 | | R11 | | | |
| IO | DIFFIO_TX79n | | B5 | VREF3B5 | | | T11 | | | LOW |
| IO | DIFFIO_TX79p | | B5 | VREF3B5 | | | T12 | | | LOW |
| IO | DIFFIO_RX79n | | B5 | VREF3B5 | | | J5 | | | LOW |
| IO | DIFFIO_RX79p | | B5 | VREF3B5 | | | J6 | | | LOW |
| IO | DIFFIO_TX78n | | B5 | VREF3B5 | | | R13 | | | LOW |
| IO | DIFFIO_TX78p | | B5 | VREF3B5 | | | R12 | | | LOW |
| IO | DIFFIO_RX78n | | B5 | VREF3B5 | | | H6 | | | LOW |
| IO | DIFFIO_RX78p | | B5 | VREF3B5 | | | H5 | | | LOW |
| IO | DIFFIO_TX77n | | B5 | VREF3B5 | | | R14 | | | LOW |
| IO | DIFFIO_TX77p | | B5 | VREF3B5 | | | T14 | | | LOW |
| IO | DIFFIO_RX77n | | B5 | VREF3B5 | | | G5 | | | LOW |
| IO | DIFFIO_RX77p | | B5 | VREF3B5 | | | G6 | | | LOW |
| IO | DIFFIO_TX76n | | B5 | VREF3B5 | | | N12 | | | LOW |
| IO | DIFFIO_TX76p | | B5 | VREF3B5 | | | P12 | | | LOW |
| IO | DIFFIO_RX76n | | B5 | VREF3B5 | | | F5 | | | LOW |
| IO | DIFFIO_RX76p | | B5 | VREF3B5 | | | F6 | | | LOW |
| IO | | | B5 | VREF3B5 | | | P13 | | | |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| IO | | | B5 | VREF3B5 | | | P14 | | | |
| FPLL10CLKn | | | B5 | VREF3B5 | D1 | L5 | J1 | | | |
| FPLL10CLKp | | | B5 | VREF3B5 | E1 | L4 | J2 | | | |
| GNDG_PLL10 | | | | | K9 | E3 | L9 | | | |
| VCCG_PLL10 | | | | | J9 | D3 | L10 | | | |
| GNDA_PLL10 | | | | | M9 | D1 | K9 | | | |
| GND | | | | | | | | | | |
| VCCA_PLL10 | | | | | L9 | D2 | J9 | | | |
| VCCINT | | | | | | | | | | |
| IO | | | B4 | VREF0B4 | | | | | | |
| IO | | | B4 | VREF0B4 | | | B3 | | | |
| IO | | | B4 | VREF0B4 | | | D4 | | | |
| IO | | | B4 | VREF0B4 | C2 | M10 | G8 | | | |
| IO | | | B4 | VREF0B4 | | | G7 | | | |
| IO | | | B4 | VREF0B4 | | | E5 | | | |
| IO | | | B4 | VREF0B4 | | | C4 | | | |
| IO | | | B4 | VREF0B4 | | | G9 | | | |
| IO | | | B4 | VREF0B4 | | | H9 | | | |
| IO | | | B4 | VREF0B4 | E5 | K9 | E6 | | | |
| IO | DQ0T0 | | B4 | VREF0B4 | C4 | D5 | C6 | DQ0T0 | DQ0T0 | |
| IO | | | B4 | VREF0B4 | | L9 | J10 | | | |
| IO | DQ0T1 | | B4 | VREF0B4 | C5 | C3 | B6 | DQ0T1 | DQ0T1 | |
| IO | | | B4 | VREF0B4 | F8 | M11 | D6 | | | |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| IO | DQ0T2 | | B4 | VREF0B4 | D5 | E5 | C7 | DQ0T2 | DQ0T2 | |
| IO | | | B4 | VREF0B4 | D4 | F7 | F8 | | | |
| IO | DQS0T | | B4 | VREF0B4 | B4 | C5 | B7 | | | |
| IO | | | B4 | VREF0B4 | E4 | L10 | F7 | | | |
| VREF0B4 | | | B4 | VREF0B4 | K10 | E6 | L11 | | | |
| IO | DQ0T3 | | B4 | VREF0B4 | B5 | C4 | A7 | DQ0T3 | DQ0T3 | |
| IO | | | B4 | VREF0B4 | | | D7 | | | |
| IO | DQ0T4 | | B4 | VREF0B4 | B3 | D4 | C8 | DQ0T4 | DQ0T4 | |
| IO | | | B4 | VREF0B4 | F7 | K10 | E7 | | | |
| IO | DQ0T5 | | B4 | VREF0B4 | C3 | A4 | A6 | DQ0T5 | DQ0T5 | |
| IO | | | B4 | VREF0B4 | H9 | J9 | D5 | | | |
| IO | DQ0T6 | | B4 | VREF0B4 | A5 | B4 | A8 | DQ0T6 | DQ0T6 | |
| IO | | | B4 | VREF0B4 | | F8 | F9 | | | |
| IO | DQ0T7 | | B4 | VREF0B4 | A4 | B3 | B8 | DQ0T7 | DQ0T7 | |
| IO | | | B4 | VREF0B4 | G9 | H9 | C5 | | | |
| IO | | | B4 | VREF0B4 | | | K11 | | | |
| IO | | | B4 | VREF0B4 | | | J11 | | | |
| IO | | | B4 | VREF1B4 | | | G10 | | | |
| IO | | | B4 | VREF1B4 | | | B5 | | | |
| IO | | | B4 | VREF1B4 | | | B4 | | | |
| IO | | | B4 | VREF1B4 | | | J12 | | | |
| IO | | | B4 | VREF1B4 | | | K12 | | | |
| IO | DQ1T0 | | B4 | VREF1B4 | E6 | D6 | C9 | DQ0T8 | DQ0T8 | |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| IO | | | B4 | VREF1B4 | | F9 | F10 | | | |
| IO | DQ1T1 | | B4 | VREF1B4 | C7 | C6 | B9 | DQ0T9 | DQ0T9 | |
| IO | | | B4 | VREF1B4 | E7 | G9 | E8 | | | |
| IO | DQ1T2 | | B4 | VREF1B4 | D7 | B5 | A9 | DQ0T10 | DQ0T10 | |
| IO | | | B4 | VREF1B4 | | | H11 | | | |
| IO | DQS1T | | B4 | VREF1B4 | C6 | E7 | B10 | DQS0T | | |
| IO | | | B4 | VREF1B4 | F9 | L11 | G11 | | | |
| IO | DQ1T3 | | B4 | VREF1B4 | A6 | C7 | C11 | DQ0T11 | DQ0T11 | |
| IO | | | B4 | VREF1B4 | H10 | H10 | A4 | | | |
| IO | DQ1T4 | | B4 | VREF1B4 | B6 | A5 | A10 | DQ0T12 | DQ0T12 | |
| IO | | | B4 | VREF1B4 | | J10 | K13 | | | |
| IO | DQ1T5 | | B4 | VREF1B4 | D6 | D7 | C10 | DQ0T13 | DQ0T13 | |
| VREF1B4 | | | B4 | VREF1B4 | K11 | E8 | L12 | | | |
| IO | | | B4 | VREF1B4 | E9 | F10 | A5 | | | |
| IO | DQ1T6 | | B4 | VREF1B4 | A7 | A6 | A11 | DQ0T14 | DQ0T14 | |
| IO | | | B4 | VREF1B4 | G10 | G10 | J13 | | | |
| IO | DQ1T7 | | B4 | VREF1B4 | B7 | B6 | B11 | DQ0T15 | DQ0T15 | |
| IO | | | B4 | VREF1B4 | J10 | K11 | M12 | | | |
| IO | | | B4 | VREF1B4 | | | H12 | | | |
| IO | | | B4 | VREF1B4 | | | F11 | | | |
| IO | | | B4 | VREF1B4 | | | H13 | | | |
| IO | | | B4 | VREF1B4 | | | D8 | | | |
| IO | | | B4 | VREF1B4 | | | E10 | | | |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| IO | | | B4 | VREF1B4 | | | M13 | | | |
| IO | | | B4 | VREF1B4 | | | E9 | | | |
| IO | DQ2T0 | | B4 | VREF2B4 | B8 | B7 | A12 | DQ1T0 | DQ0T16 | |
| IO | | | B4 | VREF2B4 | | L12 | D10 | | | |
| IO | DQ2T1 | | B4 | VREF2B4 | D9 | D8 | D12 | DQ1T1 | DQ0T17 | |
| IO | | | B4 | VREF2B4 | G11 | H11 | J14 | | | |
| IO | DQ2T2 | | B4 | VREF2B4 | E8 | B8 | E12 | DQ1T2 | DQ0T18 | |
| IO | | | B4 | VREF2B4 | | J11 | D9 | | | |
| IO | DQS2T | | B4 | VREF2B4 | C8 | A7 | C12 | | DQS0T | |
| IO | | | B4 | VREF2B4 | G12 | | G13 | | | |
| IO | DQ2T3 | | B4 | VREF2B4 | C9 | E9 | E13 | DQ1T3 | DQ0T19 | |
| IO | | | B4 | VREF2B4 | H11 | F11 | G12 | | | |
| IO | DQ2T4 | | B4 | VREF2B4 | D8 | A8 | B12 | DQ1T4 | DQ0T20 | |
| IO | | | B4 | VREF2B4 | | G11 | K14 | | | |
| IO | DQ2T5 | | B4 | VREF2B4 | A9 | C9 | B13 | DQ1T5 | DQ0T21 | |
| IO | | | B4 | VREF2B4 | | | F13 | | | |
| IO | DQ2T6 | | B4 | VREF2B4 | B9 | C8 | C13 | DQ1T6 | DQ0T22 | |
| IO | | | B4 | VREF2B4 | J11 | K12 | F12 | | | |
| IO | DQ2T7 | | B4 | VREF2B4 | A8 | D9 | D13 | DQ1T7 | DQ0T23 | |
| IO | | | B4 | VREF2B4 | | | N13 | | | |
| VREF2B4 | | | B4 | VREF2B4 | K12 | E10 | L13 | | | |
| IO | FCLK6 | | B4 | VREF2B4 | F10 | G12 | D11 | | | |
| IO | FCLK7 | | B4 | VREF2B4 | F11 | A14 | G14 | | | |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| IO | | | B4 | VREF2B4 | | | E11 | | | |
| IO | | | B4 | VREF2B4 | | | H14 | | | |
| IO | | | B4 | VREF2B4 | | | M14 | | | |
| IO | | | B4 | VREF2B4 | | | N14 | | | |
| IO | | | B4 | VREF2B4 | | | F14 | | | |
| IO | DQ3T0 | | B4 | VREF2B4 | B10 | E11 | C14 | DQ1T8 | DQ0T24 | |
| IO | | | B4 | VREF2B4 | | H12 | J15 | | | |
| IO | DQ3T1 | | B4 | VREF2B4 | D10 | B9 | D14 | DQ1T9 | DQ0T25 | |
| IO | | | B4 | VREF2B4 | L11 | J12 | K15 | | | |
| IO | DQ3T2 | | B4 | VREF2B4 | E10 | D10 | E14 | DQ1T10 | DQ0T26 | |
| IO | | | B4 | VREF3B4 | H12 | F12 | H15 | | | |
| IO | DQS3T | | B4 | VREF3B4 | C10 | D11 | C15 | DQS1T | | |
| IO | | | B4 | VREF3B4 | | K13 | M15 | | | |
| IO | DQ3T3 | | B4 | VREF3B4 | D11 | C10 | A14 | DQ1T11 | DQ0T27 | |
| IO | | | B4 | VREF3B4 | J12 | | N15 | | | |
| IO | DQ3T4 | | B4 | VREF3B4 | E11 | A9 | B14 | DQ1T12 | DQ0T28 | |
| IO | | | B4 | VREF3B4 | G13 | H13 | G15 | | | |
| IO | DQ3T5 | | B4 | VREF3B4 | B11 | B11 | B15 | DQ1T13 | DQ0T29 | |
| IO | | | B4 | VREF3B4 | | L14 | P15 | | | |
| IO | DQ3T6 | | B4 | VREF3B4 | C11 | C11 | E15 | DQ1T14 | DQ0T30 | |
| IO | DEV_OE | | B4 | VREF3B4 | F12 | L13 | P16 | | | |
| IO | DQ3T7 | | B4 | VREF3B4 | A10 | B10 | D15 | DQ1T15 | DQ0T31 | |
| IO | RUP4 | | B4 | VREF3B4 | F13 | G13 | F15 | | | |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pin Name/Function** | **Optional Function(s)** | **Configura-tion Function** | **Bank Number** | **VREF Bank** | **B956** | **F1020** | **F1508** | | | |
| IO | RDN4 | | B4 | VREF3B4 | E14 | J13 | E16 | | | |
| IO | | | B4 | VREF3B4 | | | L16 | | | |
| IO | | | B4 | VREF3B4 | | | J16 | | | |
| IO | | | B4 | VREF3B4 | | | M16 | | | |
| IO | | | B4 | VREF3B4 | | | K16 | | | |
| VREF3B4 | | | B4 | VREF3B4 | K13 | E12 | L14 | | | |
| IO | | | B4 | VREF3B4 | | | G16 | | | |
| IO | | | B4 | VREF3B4 | L12 | B14 | H16 | | | |
| IO | DQ4T0 | | B4 | VREF3B4 | D12 | A11 | A16 | | | |
| IO | | nWS | B4 | VREF3B4 | F14 | D14 | F16 | | | |
| IO | DQ4T1 | | B4 | VREF3B4 | E12 | B12 | D16 | | | |
| IO | | | B4 | VREF3B4 | | | N16 | | | |
| IO | DQ4T2 | | B4 | VREF3B4 | A12 | C12 | A17 | | | |
| IO | | | B4 | VREF3B4 | H13 | F13 | F17 | | | |
| IO | DQS4T | | B4 | VREF3B4 | C12 | D12 | C16 | | | |
| IO | | DATA0 | B4 | VREF3B4 | E15 | E14 | M17 | | | |
| IO | DQ4T3 | | B4 | VREF3B4 | B12 | C13 | B16 | | | |
| IO | | | B4 | VREF3B4 | | K14 | P17 | | | |
| IO | DQ4T4 | | B4 | VREF4B4 | C13 | D13 | B17 | | | |
| IO | | | B4 | VREF4B4 | G14 | H14 | H17 | | | |
| IO | DQ4T5 | | B4 | VREF4B4 | D13 | E13 | D17 | | | |
| IO | | DATA1 | B4 | VREF4B4 | C16 | F14 | J17 | | | |
| IO | DQ4T6 | | B4 | VREF4B4 | E13 | A13 | E17 | | | |

***Table 7–1. Pin List for the Stratix EP1S80 Device***

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pin Name/Function** | **Optional Function(s)** | **Configura-tion Function** | **Bank Number** | **VREF Bank** | **B956** | **F1020** | **F1508** | | | |
| IO | | | B4 | VREF4B4 | | J14 | K17 | | | |
| IO | DQ4T7 | | B4 | VREF4B4 | B13 | B13 | C17 | | | |
| IO | | | B4 | VREF4B4 | J13 | C14 | C18 | | | |
| IO | | | B4 | VREF4B4 | | | G17 | | | |
| IO | | | B4 | VREF4B4 | | | P18 | | | |
| IO | | | B4 | VREF4B4 | | | L17 | | | |
| IO | | | B4 | VREF4B4 | | | N17 | | | |
| IO | | | B4 | VREF4B4 | | | D18 | | | |
| IO | | | B4 | VREF4B4 | | | F18 | | | |
| IO | | | B4 | VREF4B4 | L14 | L15 | E18 | | | |
| IO | | | B4 | VREF4B4 | | | L18 | | | |
| IO | | | B4 | VREF4B4 | | | N18 | | | |
| IO | | | B4 | VREF4B4 | | | M18 | | | |
| VREF4B4 | | | B4 | VREF4B4 | K14 | | L15 | | | |
| IO | | | B4 | VREF4B4 | | | G18 | | | |
| IO | | | B4 | VREF4B4 | | | H18 | | | |
| IO | | | B4 | VREF4B4 | L16 | K15 | J18 | | | |
| IO | | DATA2 | B4 | VREF4B4 | F15 | F15 | K18 | | | |
| IO | | | B4 | VREF4B4 | | | P19 | | | |
| IO | | | B4 | VREF4B4 | | | N19 | | | |
| TMS | | TMS | B4 | VREF4B4 | D16 | E15 | F19 | | | |
| TRST | | TRST | B4 | VREF4B4 | G15 | G15 | H19 | | | |
| TCK | | TCK | B4 | VREF4B4 | F16 | G14 | E20 | | | |

**Table 7–1. Pin List for the Stratix EP1S80 Device**

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| IO | | DATA3 | B4 | VREF4B4 | G17 | C16 | P21 | | | |
| IO | | | B4 | VREF4B4 | | | P20 | | | |
| IO | | | B4 | VREF4B4 | | J15 | N20 | | | |
| TDI | | TDI | B4 | VREF4B4 | E16 | D16 | F20 | | | |
| TDO | | TDO | B4 | VREF4B4 | G16 | F16 | G20 | | | |
| IO | CLK12n | | B4 | VREF4B4 | B14 | A15 | A18 | | | |
| CLK12p | | | B4 | VREF4B4 | A14 | B15 | B18 | | | |
| IO | CLK13n/PLL11_OUT | | B4 | VREF4B4 | D14 | C15 | C19 | | | |
| CLK13p | | | B4 | VREF4B4 | C14 | D15 | D19 | | | |
| VCCINT | | | | | | | | | | |
| VCCA_PLL11 | | | | | J14 | E16 | K19 | | | |
| GND | | | | | | | | | | |
| GNDA_PLL11 | | | | | H14 | E17 | J19 | | | |
| VCCG_PLL11 | | | | | H15 | H16 | L19 | | | |
| GNDG_PLL11 | | | | | J15 | H15 | M19 | | | |
| TEMPDIODEp | | | | | E17 | E18 | F21 | | | |
| TEMPDIODEn | | | | | F17 | F18 | H21 | | | |
| VCCINT | | | | | | | | | | |
| VCCA_PLL5 | | | | | J17 | G17 | L21 | | | |
| GND | | | | | | | | | | |
| GNDA_PLL5 | | | | | H16 | F17 | M21 | | | |
| VCCG_PLL5 | | | | | K15 | J16 | L20 | | | |
| GNDG_PLL5 | | | | | K17 | L16 | M20 | | | |

**Table 7–1. Pin List for the Stratix EP1S80 Device**

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| VCC_PLL5_OUTA | | | B9 | | L18 | H17 | J20 | | | |
| VCC_PLL5_OUTA | | | B9 | | | | | | | |
| VCC_PLL5_OUTB | | | B10 | | J18 | L17 | K21 | | | |
| VCC_PLL5_OUTB | | | B10 | | | | | | | |
| IO | PLL5_OUT0p | | B9 | VREF0B3 | B16 | B16 | C21 | | | |
| IO | PLL5_OUT0n | | B9 | VREF0B3 | A16 | A16 | D21 | | | |
| IO | PLL5_OUT1p | | B9 | VREF0B3 | B15 | B17 | C20 | | | |
| IO | PLL5_OUT1n | | B9 | VREF0B3 | A15 | A17 | D20 | | | |
| IO | PLL5_FBp | | B9 | VREF0B3 | D15 | D17 | B19 | | | |
| IO | PLL5_FBn | | B9 | VREF0B3 | C15 | C17 | A19 | | | |
| IO | PLL5_OUT2p | | B10 | VREF0B3 | D17 | B18 | B21 | | | |
| IO | PLL5_OUT2n | | B10 | VREF0B3 | C17 | A18 | A21 | | | |
| IO | PLL5_OUT3p | | B10 | VREF0B3 | B17 | D18 | A20 | | | |
| IO | PLL5_OUT3n | | B10 | VREF0B3 | A17 | C18 | B20 | | | |
| nSTATUS | | nSTATUS | B3 | VREF0B3 | E18 | G16 | N21 | | | |
| nCONFIG | | nCONFIG | B3 | VREF0B3 | F19 | J18 | L22 | | | |
| DCLK | | DCLK | B3 | VREF0B3 | F18 | E19 | G21 | | | |
| CONF_DONE | | CONF_DONE | B3 | VREF0B3 | G18 | G18 | H22 | | | |
| CLK14p | | | B3 | VREF0B3 | A18 | A19 | B22 | | | |
| IO | CLK14n | | B3 | VREF0B3 | B18 | B19 | A22 | | | |
| CLK15p | | | B3 | VREF0B3 | C18 | C19 | D22 | | | |
| IO | CLK15n | | B3 | VREF0B3 | D18 | D19 | C22 | | | |
| VREF0B3 | | | B3 | VREF0B3 | K18 | E21 | L25 | | | |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| IO | | | B3 | VREF0B3 | | | E21 | | | |
| IO | | | B3 | VREF0B3 | | | G22 | | | |
| IO | | | B3 | VREF0B3 | | | J22 | | | |
| IO | | | B3 | VREF0B3 | | | N22 | | | |
| IO | | | B3 | VREF0B3 | | | M22 | | | |
| IO | | | B3 | VREF0B3 | | | P22 | | | |
| IO | | | B3 | VREF0B3 | | | E22 | | | |
| IO | | | B3 | VREF0B3 | | | G23 | | | |
| IO | | | B3 | VREF0B3 | L19 | F19 | F22 | | | |
| IO | | DATA4 | B3 | VREF0B3 | G19 | G19 | L23 | | | |
| IO | | | B3 | VREF0B3 | | | N23 | | | |
| IO | DQ5T0 | | B3 | VREF0B3 | B19 | A20 | B23 | | | |
| IO | | | B3 | VREF0B3 | J19 | K18 | H23 | | | |
| IO | DQ5T1 | | B3 | VREF0B3 | C19 | B20 | E23 | | | |
| IO | | DATA5 | B3 | VREF0B3 | F20 | J19 | J23 | | | |
| IO | DQ5T2 | | B3 | VREF0B3 | D19 | C20 | D23 | | | |
| IO | | | B3 | VREF0B3 | | L18 | K23 | | | |
| IO | DQS5T | | B3 | VREF0B3 | C20 | D20 | C23 | | | |
| IO | | | B3 | VREF1B3 | H19 | H19 | F23 | | | |
| IO | DQ5T3 | | B3 | VREF1B3 | E19 | E20 | A23 | | | |
| IO | | DATA6 | B3 | VREF1B3 | F21 | K19 | E24 | | | |
| IO | DQ5T4 | | B3 | VREF1B3 | A20 | B21 | A24 | | | |
| IO | | | B3 | VREF1B3 | | H20 | M23 | | | |

Table 7–1. Pin List for the Stratix EP1S80 Device

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| IO | DQ5T5 | | B3 | VREF1B3 | B20 | C21 | B24 | | | |
| IO | | | B3 | VREF1B3 | H20 | F20 | F24 | | | |
| IO | DQ5T6 | | B3 | VREF1B3 | D20 | D21 | C24 | | | |
| IO | | | B3 | VREF1B3 | | | G24 | | | |
| IO | DQ5T7 | | B3 | VREF1B3 | E20 | A22 | D24 | | | |
| IO | | | B3 | VREF1B3 | J20 | G20 | K24 | | | |
| IO | | | B3 | VREF1B3 | | | N24 | | | |
| VREF1B3 | | | B3 | VREF1B3 | K19 | | L26 | | | |
| IO | | | B3 | VREF1B3 | | | H24 | | | |
| IO | | | B3 | VREF1B3 | | | F25 | | | |
| IO | | | B3 | VREF1B3 | | | J24 | | | |
| IO | | | B3 | VREF1B3 | | | L24 | | | |
| IO | RUP3 | | B3 | VREF1B3 | F22 | F21 | P23 | | | |
| IO | RDN3 | | B3 | VREF1B3 | F24 | L19 | M24 | | | |
| IO | DQ6T0 | | B3 | VREF1B3 | B21 | B22 | B25 | DQ2T0 | DQ1T0 | |
| IO | | | B3 | VREF1B3 | | | G25 | | | |
| IO | DQ6T1 | | B3 | VREF1B3 | C21 | C22 | E25 | DQ2T1 | DQ1T1 | |
| IO | | DATA7 | B3 | VREF1B3 | G20 | J20 | P25 | | | |
| IO | DQ6T2 | | B3 | VREF1B3 | A22 | B23 | D25 | DQ2T2 | DQ1T2 | |
| IO | | | B3 | VREF1B3 | | K20 | P24 | | | |
| IO | DQS6T | | B3 | VREF1B3 | C22 | D22 | C25 | DQS2T | | |
| IO | | | B3 | VREF1B3 | | G21 | H25 | | | |
| IO | DQ6T3 | | B3 | VREF1B3 | D21 | C23 | A26 | DQ2T3 | DQ1T3 | |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pin Name/Function** | **Optional Function(s)** | **Configura-tion Function** | **Bank Number** | **VREF Bank** | **B956** | **F1020** | **F1508** | | | |
| IO | | CLKUSR | B3 | VREF1B3 | F23 | H21 | J25 | | | |
| IO | DQ6T4 | | B3 | VREF1B3 | E21 | A24 | B26 | DQ2T4 | DQ1T4 | |
| IO | | | B3 | VREF1B3 | | L20 | N25 | | | |
| IO | DQ6T5 | | B3 | VREF2B3 | B22 | E22 | C26 | DQ2T5 | DQ1T5 | |
| IO | | | B3 | VREF2B3 | | | F26 | | | |
| IO | DQ6T6 | | B3 | VREF2B3 | D22 | B24 | D26 | DQ2T6 | DQ1T6 | |
| IO | | | B3 | VREF2B3 | | J21 | G27 | | | |
| IO | DQ6T7 | | B3 | VREF2B3 | E22 | D23 | E26 | DQ2T7 | DQ1T7 | |
| IO | | | B3 | VREF2B3 | | | K25 | | | |
| IO | FCLK0 | | B3 | VREF2B3 | E23 | F22 | G26 | | | |
| IO | FCLK1 | | B3 | VREF2B3 | E25 | G22 | D29 | | | |
| IO | | | B3 | VREF2B3 | | | H26 | | | |
| IO | | | B3 | VREF2B3 | | | D30 | | | |
| IO | | | B3 | VREF2B3 | | | M25 | | | |
| IO | | | B3 | VREF2B3 | | | N26 | | | |
| VREF2B3 | | | B3 | VREF2B3 | K20 | E23 | L27 | | | |
| IO | | | B3 | VREF2B3 | | | F27 | | | |
| IO | DQ7T0 | | B3 | VREF2B3 | A23 | D24 | B27 | DQ2T8 | DQ1T8 | |
| IO | | | B3 | VREF2B3 | | K21 | E29 | | | |
| IO | DQ7T1 | | B3 | VREF2B3 | B23 | A25 | C27 | DQ2T9 | DQ1T9 | |
| IO | | | B3 | VREF2B3 | L21 | | M26 | | | |
| IO | DQ7T2 | | B3 | VREF2B3 | A24 | C24 | D27 | DQ2T10 | DQ1T10 | |
| IO | | | B3 | VREF2B3 | | L21 | F28 | | | |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| IO | DQS7T | | B3 | VREF2B3 | C24 | B26 | C28 | | DQS1T | |
| IO | | | B3 | VREF2B3 | H21 | | F29 | | | |
| IO | DQ7T3 | | B3 | VREF2B3 | C23 | B25 | E27 | DQ2T11 | DQ1T11 | |
| IO | | | B3 | VREF2B3 | J21 | H22 | N27 | | | |
| IO | DQ7T4 | | B3 | VREF2B3 | D24 | C25 | B28 | DQ2T12 | DQ1T12 | |
| IO | | | B3 | VREF2B3 | | | D31 | | | |
| IO | DQ7T5 | | B3 | VREF2B3 | B24 | D25 | A28 | DQ2T13 | DQ1T13 | |
| IO | | | B3 | VREF2B3 | | J22 | J26 | | | |
| IO | DQ7T6 | | B3 | VREF2B3 | D23 | A26 | D28 | DQ2T14 | DQ1T14 | |
| IO | | | B3 | VREF2B3 | | | K26 | | | |
| IO | DQ7T7 | | B3 | VREF2B3 | E24 | E24 | E28 | DQ2T15 | DQ1T15 | |
| IO | | | B3 | VREF3B3 | | | H27 | | | |
| IO | | | B3 | VREF3B3 | | | E30 | | | |
| IO | | | B3 | VREF3B3 | | | A35 | | | |
| IO | | | B3 | VREF3B3 | | | F30 | | | |
| IO | | | B3 | VREF3B3 | | | M27 | | | |
| IO | | | B3 | VREF3B3 | | | N28 | | | |
| IO | | | B3 | VREF3B3 | | | G28 | | | |
| IO | | | B3 | VREF3B3 | G21 | F23 | D32 | | | |
| IO | DQ8T0 | | B3 | VREF3B3 | A25 | C26 | A29 | DQ3T0 | DQ1T16 | |
| IO | | | B3 | VREF3B3 | J22 | G23 | J27 | | | |
| IO | DQ8T1 | | B3 | VREF3B3 | C25 | A28 | B29 | DQ3T1 | DQ1T17 | |
| IO | | | B3 | VREF3B3 | | | M28 | | | |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| VREF3B3 | | | B3 | VREF3B3 | K21 | E25 | L28 | | | |
| IO | DQ8T2 | | B3 | VREF3B3 | B25 | A27 | C29 | DQ3T2 | DQ1T18 | |
| IO | | | B3 | VREF3B3 | H22 | K22 | H28 | | | |
| IO | DQS8T | | B3 | VREF3B3 | C26 | B27 | B30 | DQS3T | | |
| IO | | | B3 | VREF3B3 | | H23 | E31 | | | |
| IO | DQ8T3 | | B3 | VREF3B3 | D25 | D26 | C30 | DQ3T3 | DQ1T19 | |
| IO | | | B3 | VREF3B3 | | | K27 | | | |
| IO | DQ8T4 | | B3 | VREF3B3 | A26 | C27 | A30 | DQ3T4 | DQ1T20 | |
| IO | | | B3 | VREF3B3 | | J23 | G29 | | | |
| IO | DQ8T5 | | B3 | VREF3B3 | B26 | B28 | A31 | DQ3T5 | DQ1T21 | |
| IO | | | B3 | VREF3B3 | G22 | F24 | D33 | | | |
| IO | DQ8T6 | | B3 | VREF3B3 | E26 | D27 | B31 | DQ3T6 | DQ1T22 | |
| IO | | | B3 | VREF3B3 | | | H29 | | | |
| GND | | | | | | | | | | |
| GND | | | | | | | | | | |
| GND | | | | | D28 | H24 | E32 | | | |
| IO | DQ8T7 | | B3 | VREF3B3 | D26 | E26 | C31 | DQ3T7 | DQ1T23 | |
| IO | | | B3 | VREF3B3 | | | G30 | | | |
| IO | | | B3 | VREF3B3 | | | J28 | | | |
| IO | | | B3 | VREF3B3 | | | B35 | | | |
| IO | | | B3 | VREF3B3 | | | C35 | | | |
| IO | | | B3 | VREF3B3 | | | K28 | | | |
| IO | | | B3 | VREF4B3 | | | F31 | | | |

**Table 7–1. Pin List for the Stratix EP1S80 Device**

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| IO | | | B3 | VREF4B3 | | | B36 | | | |
| IO | | | B3 | VREF4B3 | F25 | F25 | D34 | | | |
| IO | DQ9T0 | | B3 | VREF4B3 | B27 | A29 | A32 | DQ3T8 | DQ1T24 | |
| IO | | | B3 | VREF4B3 | | | J29 | | | |
| IO | DQ9T1 | | B3 | VREF4B3 | C27 | B29 | C32 | DQ3T9 | DQ1T25 | |
| IO | | | B3 | VREF4B3 | G23 | G24 | A36 | | | |
| IO | DQ9T2 | | B3 | VREF4B3 | A27 | B30 | B32 | DQ3T10 | DQ1T26 | |
| IO | | | B3 | VREF4B3 | C30 | L22 | F32 | | | |
| IO | DQS9T | | B3 | VREF4B3 | B28 | C28 | B33 | | | |
| IO | | | B3 | VREF4B3 | | J24 | K29 | | | |
| IO | DQ9T3 | | B3 | VREF4B3 | D27 | C29 | A34 | DQ3T11 | DQ1T27 | |
| VREF4B3 | | | B3 | VREF4B3 | K22 | E27 | L29 | | | |
| IO | | | B3 | VREF4B3 | | K23 | E33 | | | |
| IO | DQ9T4 | | B3 | VREF4B3 | A28 | D29 | A33 | DQ3T12 | DQ1T28 | |
| IO | | | B3 | VREF4B3 | E27 | F26 | B37 | | | |
| IO | DQ9T5 | | B3 | VREF4B3 | C28 | D28 | C33 | DQ3T13 | DQ1T29 | |
| IO | | | B3 | VREF4B3 | | L23 | F33 | | | |
| IO | DQ9T6 | | B3 | VREF4B3 | C29 | C30 | C34 | DQ3T14 | DQ1T30 | |
| IO | | | B3 | VREF4B3 | | | G31 | | | |
| IO | DQ9T7 | | B3 | VREF4B3 | B29 | E28 | B34 | DQ3T15 | DQ1T31 | |
| IO | | | B3 | VREF4B3 | H23 | K24 | D35 | | | |
| IO | | | B3 | VREF4B3 | | | H31 | | | |
| IO | | | B3 | VREF4B3 | | | J30 | | | |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| IO | | | B3 | VREF4B3 | | | G33 | | | |
| IO | | | B3 | VREF4B3 | | | C36 | | | |
| IO | | | B3 | VREF4B3 | | | E34 | | | |
| IO | | | B3 | VREF4B3 | E28 | L24 | G32 | | | |
| IO | | | B3 | VREF4B3 | | | D36 | | | |
| IO | | | B3 | VREF4B3 | | | E35 | | | |
| IO | | | B3 | VREF4B3 | | | | | | |
| VCCIO2 | | | | | C31 | C31 | C39 | | | |
| VCCIO2 | | | | | N31 | C32 | R39 | | | |
| VCCIO2 | | | | | T23 | M32 | W35 | | | |
| VCCIO2 | | | | | | T23 | V25 | | | |
| VCCIO2 | | | | | | | H33 | | | |
| VCCIO1 | | | | | U20 | AA32 | AA25 | | | |
| VCCIO1 | | | | | W31 | AK31 | Y32 | | | |
| VCCIO1 | | | | | AJ31 | AK32 | AE39 | | | |
| VCCIO1 | | | | | | U23 | AU39 | | | |
| VCCIO1 | | | | | | | AM33 | | | |
| VCCIO8 | | | | | AL29 | AC17 | AW37 | | | |
| VCCIO8 | | | | | AL19 | AM21 | AW25 | | | |
| VCCIO8 | | | | | Y17 | AM30 | AR21 | | | |
| VCCIO8 | | | | | | | AE22 | | | |
| VCCIO8 | | | | | | | AM30 | | | |
| VCCIO7 | | | | | AC16 | AC16 | AE19 | | | |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| **Pin Name/Function** | **Optional Function(s)** | **Configura-tion Function** | **Bank Number** | **VREF Bank** | **B956** | **F1020** | **F1508** | | | |
| VCCIO7 | | | | | AL13 | AM12 | AM20 | | | |
| VCCIO7 | | | | | AL3 | AM3 | AW15 | | | |
| VCCIO7 | | | | | | | AW3 | | | |
| VCCIO7 | | | | | | | AM10 | | | |
| VCCIO6 | | | | | AJ1 | AA1 | AU1 | | | |
| VCCIO6 | | | | | W1 | AK1 | AM7 | | | |
| VCCIO6 | | | | | U12 | AK2 | AE1 | | | |
| VCCIO6 | | | | | | U10 | AA5 | | | |
| VCCIO6 | | | | | | | AB15 | | | |
| VCCIO5 | | | | | T9 | C1 | W15 | | | |
| VCCIO5 | | | | | N1 | C2 | Y8 | | | |
| VCCIO5 | | | | | C1 | M1 | R1 | | | |
| VCCIO5 | | | | | | T10 | H7 | | | |
| VCCIO5 | | | | | | | C1 | | | |
| VCCIO4 | | | | | A3 | A12 | A3 | | | |
| VCCIO4 | | | | | A13 | A3 | A15 | | | |
| VCCIO4 | | | | | J16 | K16 | E19 | | | |
| VCCIO4 | | | | | | | R18 | | | |
| VCCIO4 | | | | | | | H10 | | | |
| VCCIO3 | | | | | M17 | A21 | H20 | | | |
| VCCIO3 | | | | | A19 | A30 | R21 | | | |
| VCCIO3 | | | | | A29 | K17 | A25 | | | |
| VCCIO3 | | | | | | | A37 | | | |

Table 7–1. Pin List for the Stratix EP1S80 Device

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| VCCIO3 | | | | | | | H30 | | | |
| VCCINT | | | | | AA12 | M12 | AA16 | | | |
| VCCINT | | | | | AA14 | M14 | AA18 | | | |
| VCCINT | | | | | AA20 | M19 | AA22 | | | |
| VCCINT | | | | | L13 | M21 | AA24 | | | |
| VCCINT | | | | | L20 | N13 | AB17 | | | |
| VCCINT | | | | | M11 | N15 | AB19 | | | |
| VCCINT | | | | | M13 | N18 | AB21 | | | |
| VCCINT | | | | | M15 | N20 | AB23 | | | |
| VCCINT | | | | | M19 | P12 | AB25 | | | |
| VCCINT | | | | | M21 | P14 | AC16 | | | |
| VCCINT | | | | | N12 | P16 | AC18 | | | |
| VCCINT | | | | | N14 | P17 | AC20 | | | |
| VCCINT | | | | | N16 | P19 | AC22 | | | |
| VCCINT | | | | | N18 | P21 | AC24 | | | |
| VCCINT | | | | | N20 | R13 | AD15 | | | |
| VCCINT | | | | | P11 | R15 | AD17 | | | |
| VCCINT | | | | | P13 | R18 | AD19 | | | |
| VCCINT | | | | | P14 | R20 | AD21 | | | |
| VCCINT | | | | | P15 | T14 | AD23 | | | |
| VCCINT | | | | | P17 | T16 | AD25 | | | |
| VCCINT | | | | | P19 | T17 | AE16 | | | |
| VCCINT | | | | | P21 | T19 | AE18 | | | |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
| VCCINT | | | | | R12 | U14 | AE20 | | | |
| VCCINT | | | | | R13 | U16 | AE24 | | | |
| VCCINT | | | | | R14 | U17 | R16 | | | |
| VCCINT | | | | | R18 | U19 | R20 | | | |
| VCCINT | | | | | R19 | V13 | R22 | | | |
| VCCINT | | | | | R20 | V15 | R24 | | | |
| VCCINT | | | | | T11 | V18 | T15 | | | |
| VCCINT | | | | | T13 | V20 | T17 | | | |
| VCCINT | | | | | T19 | W14 | T19 | | | |
| VCCINT | | | | | T21 | W16 | T21 | | | |
| VCCINT | | | | | U10 | W17 | T23 | | | |
| VCCINT | | | | | U14 | W19 | T25 | | | |
| VCCINT | | | | | U18 | Y13 | U16 | | | |
| VCCINT | | | | | U22 | Y15 | U18 | | | |
| VCCINT | | | | | V11 | Y18 | U20 | | | |
| VCCINT | | | | | V13 | Y20 | U22 | | | |
| VCCINT | | | | | V15 | | U24 | | | |
| VCCINT | | | | | V17 | | V15 | | | |
| VCCINT | | | | | V19 | | V17 | | | |
| VCCINT | | | | | V21 | | V19 | | | |
| VCCINT | | | | | W12 | | V21 | | | |
| VCCINT | | | | | W14 | | V23 | | | |
| VCCINT | | | | | W16 | | W16 | | | |

**Table 7–1. Pin List for the Stratix EP1S80 Device**

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| VCCINT | | | | | W18 | | W18 | | | |
| VCCINT | | | | | W20 | | W22 | | | |
| VCCINT | | | | | Y11 | | W24 | | | |
| VCCINT | | | | | Y13 | | Y15 | | | |
| VCCINT | | | | | Y15 | | Y17 | | | |
| VCCINT | | | | | Y19 | | Y23 | | | |
| VCCINT | | | | | Y21 | | Y25 | | | |
| GND | | | | | A1 | A10 | A13 | | | |
| GND | | | | | A11 | A2 | A2 | | | |
| GND | | | | | A2 | A23 | A27 | | | |
| GND | | | | | A21 | A31 | A38 | | | |
| GND | | | | | A30 | AA16 | AA15 | | | |
| GND | | | | | A31 | AA17 | AA17 | | | |
| GND | | | | | AA17 | AC1 | AA23 | | | |
| GND | | | | | AA18 | AC32 | AA7 | | | |
| GND | | | | | AB16 | AD17 | AB16 | | | |
| GND | | | | | AD18 | AF17 | AB18 | | | |
| GND | | | | | AK1 | AL1 | AB20 | | | |
| GND | | | | | AK2 | AL2 | AB22 | | | |
| GND | | | | | AK30 | AL31 | AB24 | | | |
| GND | | | | | AK31 | AL32 | AC15 | | | |
| GND | | | | | AL1 | AM10 | AC17 | | | |
| GND | | | | | AL11 | AM2 | AC19 | | | |

**Table 7–1. Pin List for the Stratix EP1S80 Device**

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| GND | | | | | AL2 | AM23 | AC21 | | | |
| GND | | | | | AL21 | AM31 | AC23 | | | |
| GND | | | | | AL30 | B1 | AC25 | | | |
| GND | | | | | AL31 | B2 | AD16 | | | |
| GND | | | | | B1 | B31 | AD18 | | | |
| GND | | | | | B2 | B32 | AD20 | | | |
| GND | | | | | B30 | H18 | AD22 | | | |
| GND | | | | | B31 | J17 | AD24 | | | |
| GND | | | | | H17 | K1 | AE15 | | | |
| GND | | | | | H18 | K32 | AE17 | | | |
| GND | | | | | K16 | M13 | AE21 | | | |
| GND | | | | | L15 | M15 | AE23 | | | |
| GND | | | | | L17 | M16 | AE25 | | | |
| GND | | | | | M1 | M17 | AG1 | | | |
| GND | | | | | M12 | M18 | AG39 | | | |
| GND | | | | | M14 | M20 | AK10 | | | |
| GND | | | | | M16 | N12 | AK20 | | | |
| GND | | | | | M18 | N14 | AK22 | | | |
| GND | | | | | M20 | N16 | AK30 | | | |
| GND | | | | | M31 | N17 | AL21 | | | |
| GND | | | | | N11 | N19 | AM32 | | | |
| GND | | | | | N13 | N21 | AM8 | | | |
| GND | | | | | N15 | P13 | AN21 | | | |

*Table 7–1. Pin List for the Stratix EP1S80 Device*

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| GND | | | | | N17 | P15 | AU3 | | | |
| GND | | | | | N19 | P18 | AU37 | | | |
| GND | | | | | N21 | P20 | AV1 | | | |
| GND | | | | | P12 | R14 | AV2 | | | |
| GND | | | | | P16 | R16 | AV38 | | | |
| GND | | | | | P18 | R17 | AV39 | | | |
| GND | | | | | P20 | R19 | AW13 | | | |
| GND | | | | | R11 | T12 | AW2 | | | |
| GND | | | | | R15 | T13 | AW27 | | | |
| GND | | | | | R17 | T15 | AW38 | | | |
| GND | | | | | R21 | T18 | B1 | | | |
| GND | | | | | T10 | T20 | B2 | | | |
| GND | | | | | T12 | T21 | B38 | | | |
| GND | | | | | T14 | U12 | B39 | | | |
| GND | | | | | T18 | U13 | C3 | | | |
| GND | | | | | T20 | U15 | C37 | | | |
| GND | | | | | T22 | U18 | G19 | | | |
| GND | | | | | U11 | U20 | H32 | | | |
| GND | | | | | U13 | U21 | H8 | | | |
| GND | | | | | U15 | V14 | J21 | | | |
| GND | | | | | U17 | V16 | K10 | | | |
| GND | | | | | U19 | V17 | K20 | | | |
| GND | | | | | U21 | V19 | K22 | | | |

**Table 7–1. Pin List for the Stratix EP1S80 Device**

| Device | | | | | Package | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
| GND | | | | | V12 | W13 | K30 | | | |
| GND | | | | | V14 | W15 | N1 | | | |
| GND | | | | | V16 | W18 | N39 | | | |
| GND | | | | | V18 | W20 | R15 | | | |
| GND | | | | | V20 | Y14 | R17 | | | |
| GND | | | | | W11 | Y16 | R19 | | | |
| GND | | | | | W13 | Y17 | R23 | | | |
| GND | | | | | W15 | Y19 | R25 | | | |
| GND | | | | | W17 | | T16 | | | |
| GND | | | | | W19 | | T18 | | | |
| GND | | | | | W21 | | T20 | | | |
| GND | | | | | Y1 | | T22 | | | |
| GND | | | | | Y12 | | T24 | | | |
| GND | | | | | Y14 | | U15 | | | |
| GND | | | | | Y16 | | U17 | | | |
| GND | | | | | Y18 | | U19 | | | |
| GND | | | | | Y20 | | U21 | | | |
| GND | | | | | Y31 | | U23 | | | |
| GND | | | | | | | U25 | | | |
| GND | | | | | | | V16 | | | |
| GND | | | | | | | V18 | | | |
| GND | | | | | | | V20 | | | |
| GND | | | | | | | V22 | | | |

**Table 7–1. Pin List for the Stratix EP1S80 Device**

| Device | | | | | Package | | | DQS for x16 | DQS for x32 | DIFFIO Speed (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name/Function | Optional Function(s) | Configura-tion Function | Bank Number | VREF Bank | B956 | F1020 | F1508 | | | |
| GND | | | | | | | V24 | | | |
| GND | | | | | | | W17 | | | |
| GND | | | | | | | W23 | | | |
| GND | | | | | | | W25 | | | |
| GND | | | | | | | W33 | | | |
| GND | | | | | | | Y10 | | | |
| GND | | | | | | | Y16 | | | |
| GND | | | | | | | Y18 | | | |
| GND | | | | | | | Y22 | | | |
| GND | | | | | | | Y24 | | | |
| GND | | | | | | | Y30 | | | |

*Note to Table 7–1:*

(1) The wire bond and flip-chip packages will have different data rates for the high speed differential I/O channels. Table 7–2 shows the data rates as supported for each package.

**Table 7–2. High Speed Differential I/O Channel Data Rates**

| Package | Package Type | High Speed Differential I/O Channel Performance (DIFFIO Speed) | | Units |
|---|---|---|---|---|
| | | High | Low | |
| B956 | flip chip | 840 | 462 | Mbps |
| F1020 | flip chip | 840 | 462 | Mbps |
| F1508 | flip chip | 840 | 462 | Mbps |

## Pin Definitions

Table 7–3 show pin definitions for the EP1S80 device.

*Table 7–3. Pin Definitions for the EP1S80 Device (Part 1 of 6)*

| Pin Name | Pin Type (1st, 2nd, & 3rd Function) | Pin Description |
|---|---|---|
| **Supply and Reference Pins** | | |
| VREF[1..4]B[1..8] | Input | Input reference voltage for each I/O bank. If a bank is used for a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for that bank. All of the VREF pins within a bank are shorted together. Each VREF pin can support up to 20 inputs on each side. If VREF pins are not used, designers should connect them to either VCC or Gnd. |
| VCCIO[1..8] | Power | These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards. VCCIO also supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5-V, 1.8-V, 2.5-V, 3.3-V PCI, and 3.3-V PCI-X I/O standards. |
| VCCINT | Power | These are internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVDS, LVPECL, 3.3-V PCML, HyperTransport™ technology, differential HSTL, GTL, GTL+, HSTL, SSTL, CTT, and 3.3-V AGP I/O standards. |
| VCC_PLL5_OUTA | Power | External clock output buffer power for PLL5 clock outputs PLL5_OUT[1..0]. The designer must connect this pin to the VCCIO of bank 9. |
| VCC_PLL5_OUTB | Power | External clock output buffer power for PLL5 clock outputs PLL5_OUT[3..2]. The designer must connect this pin to the VCCIO of bank 10. |
| VCC_PLL6_OUTA | Power | External clock output buffer power for PLL6 clock outputs PLL6_OUT[1..0]. The designer must connect this pin to the VCCIO of bank 11. |
| VCC_PLL6_OUTB | Power | External clock output buffer power for PLL6 clock outputs PLL6_OUT[3..2]. The designer must connect this pin to the VCCIO of bank 12. |
| VCCA_PLL[1..12] | Power | Analog power for PLLs[1..12]. The designer must connect this pin to 1.5 V, even if the PLL is not used. |
| GNDA_PLL[1..12] | Ground | Analog ground for PLLs[1..12]. The designer can connect this pin to the GND plane on the board. |

**Table 7–3. Pin Definitions for the EP1S80 Device (Part 2 of 6)**

| | | |
|---|---|---|
| VCCG_PLL[1..12] | Power | Guard ring power for PLLs[1..12]. The designer must connect this pin to 1.5 V, even if the PLL is not used. |
| GNDG_PLL[1..12] | Ground | Guard ring ground for PLLs[1..12]. The designer can connect this pin to the GND plane on the board. |
| **Dedicated & Configuration/JTAG Pins** | | |
| CONF_DONE | Bidirectional (open-drain) | This is a dedicated configuration status pin; it is not available as a user I/O pin. |
| nSTATUS | Bidirectional (open-drain) | This is a dedicated configuration status pin; it is not available as a user I/O pin. |
| nCONFIG | Input | Dedicated configuration control input. A low transition resets the target device; a low-to-high transition begins configuration. All I/O pins tri-state when nCONFIG is driven low. |
| DCLK | Input | Clock input used to clock configuration data from an external source into the Stratix device. This is a dedicated pin used for configuration. |
| nIO_PULLUP | Input | IF nIO_PULLUP is driven high during configuration, the weak pull-ups on all user I/O pins are disabled. If driven low, the weak pull-ups are enabled during configuration. nIO_PULLUP can be pulled up to either 1.5, 1.8, 2.5, or 3.3 V. |
| PORSEL | Input | Dedicated input pin used to select POR delay times of 2 ms or 100 ms during powerup. When PORSEL is connected to ground, the POR time is 100 ms. When PORSEL is connected to 3.3 V, the POR time is 2 ms. |
| VCCSEL | Input | VCCSEL is used to select which input buffer is used on all configuration pins. VCCSEL will control whether the 3.3-/2.5-V input buffer or the 1.8-/1.5-V input buffer is used. A "0" means 3.3/2.5 V and a "1" means 1.8-/1.5 V. At powerup, VCCSEL accepts 3.3V and 2.5V TTL Levels. VCCSEL affects the following pins: TDI, TMS, TCK, TRST, MSEL0, MSEL1, MSEL2, nCONFIG, nCE, DCLK, CONF_DONE, nSTATUS, and PLL_ENA. |
| nCE | Input | Active-low chip enables. Dedicated chip enable input used to detect which device is active in a chain of devices. When nCE is low, the device is enabled. When nCE is high, the device is disabled. |
| nCEO | Output | Output that drives low when device configuration is complete. During multi-device configuration, this pin feeds a subsequent device's nCE pin. |
| TMS | Input | This is a dedicated JTAG input pin. |
| TDI | Input | This is a dedicated JTAG input pin. |

***Table 7–3. Pin Definitions for the EP1S80 Device (Part 3 of 6)***

| | | |
|---|---|---|
| TCK | Input | This is a dedicated JTAG input pin. |
| TDO | Output | This is a dedicated JTAG input pin. |
| TRST | Input | This is a dedicated JTAG input pin. Active low input, used to asynchronously reset the JTAG boundary scan circuit. |
| MSEL[2..0] | Input | Dedicated mode select control pins that set the configuration mode for the device. |
| TEMPDIODEp | Input | Pin used in conjunction with the temperature sensing diode (bias-high input) inside the Stratix device. If the temperature sensing diode is not used then connect this pin to GND. |
| TEMPDIODEn | Input | Pin used in conjunction with the temperature sensing diode (bias-low input) inside the Stratix device. If the temperature sensing diode is not used then connect this pin to GND. |
| **Clock and PLL Pins** | | |
| PLL_ENA | Input | Dedicated input pin that drives the optional pllena port of all or a set of PLLs. If a PLL uses the pllena port, drive the PLL_ENA pin low to reset all PLLs including the counters to their default state. If VCCSEL = 0, then you must drive the PLL_ENA with a 3.3/2.5 V signal to enable the PLLs. If VCCSEL = 1, connect PLL_ENA to 1.8/1.5 V to enable the PLLs. |
| FCLK[7..0] | Bidirectional | Dedicated fast regional clock pins. FCLK pins can also be used as type input, output, or as bidirectional pins. |
| FPLL[10..7]CLKp | Input | Dedicated global clock inputs for fast PLLs (PLLs 7 through 10). |
| FPLL[10..7]CLKn | Input | Dedicated negative terminal associated with FPLL[10..7]CLKp pins. |
| CLK[15..0]p | Input | Dedicated global clock inputs 0 to 15. |
| CLK[15..0]n | I/O, Input | Optional negative terminal input for differential global clock input. |
| PLL6_OUT[3..0]p | I/O, Output | Optional external clock outputs [3..0] from enhanced PLL 6. These pins can be differential (four output pin pairs) or single ended (eight clock outputs from PLL6). |
| PLL6_OUT[3..0]n | I/O, Output | Optional negative terminal for external clock outputs [3..0] from PLL6. If the clock outputs are single ended, then each pair of pins (i.e., PLL6_OUT0p and PLL6_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase. |

**Table 7–3. Pin Definitions for the EP1S80 Device (Part 4 of 6)**

| | | |
|---|---|---|
| PLL5_OUT[3..0]p | I/O, Output | Optional external clock outputs [3..0] from enhanced PLL 5. These pins can be differential (four output pin pairs) or single ended (eight clock outputs from PLL5). |
| PLL5_OUT[3..0]n | I/O, Output | Optional negative terminal for external clock outputs [3..0] from PLL 5. If the clock outputs are single ended, then each pair of pins (i.e., PLL5_OUT0p and PLL5_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase. |
| **Optional/Dual-Purpose Pins** | | |
| DATA0 | I/O, Input | Dual-purpose configuration data input pin. Can be used as an I/O pin after configuration is complete. |
| DIFFIO_TX[0..151]n | I/O, Output | This pin can be used as the complementary signal of the differential inputs and outputs. If not used for the differential pair, these pins are regular I/O pins. Pins with an n suffix carry the negative signal for the differential channel. Pins with a p suffix carry the positive signal for the differential channel. |
| CLK6n, PLL12_OUT | I/O, Input (CLK6n), Output (PLL12_OUT) | This pin can be used as an I/O pin, CLK6n, as the PLL12_OUT pin. Only the EP1S40 and larger devices have this pin. |
| CLK13n, PLL11_OUT | I/O, Input (CLK13n), Output (PLL11_OUT) | This pin can be used as an I/O pin, CLK13n, or used as the PLL11_OUT pin. Only the EP1S40 and larger devices have this pin. |
| PLL5_FBp | I/O, Input | External feedback input pin for PLL5. This pin can be used as a user I/O pin if external feedback mode is not used. |
| PLL5_FBn | I/O, Input | Negative terminal input for external feedback input PLL5_FBp |
| PLL6_FBp | I/O, Input | External feedback input pin for PLL6 |
| PLL6_FBn | I/O, Input | Negative terminal input for external feedback input PLL6_FBp |
| INIT_DONE | I/O, Output | This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration. |
| DATA[7..1] | I/O, Input | Dual-purpose configuration input data pins. These pins can be used for configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration. |

***Table 7–3. Pin Definitions for the EP1S80 Device (Part 5 of 6)***

| | | |
|---|---|---|
| nRS | I/O, Input | Read strobe input pin. This pin can be used as a user I/O pin after configuration. |
| DEV_CLRn | I/O, Input | Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as defined in the users design. |
| DEV_OE | I/O, Input | Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design. |
| CLKUSR | I/O, Input | Optional user-supplied clock input. Synchronizes the initialization of one or more devices. This pin can be used as a user I/O pin after configuration. |
| RDYnBSY | I/O, Output | Ready not busy output. A high output indicates that the target device is ready to accept another data byte. A low output indicates that the target device is not ready to receive another data byte. This pin can be used as a user I/O pin after configuration. |
| nCS,CS | I/O, Input | These are chip-select inputs that enable the Stratix device in the passive parallel asynchronous configuration mode. Drive nCS low and CS high to target a device for configuration. If a design requires an active high enable, use the CS pin and drive the nCS pin low. If a design requires an active low enable, use the nCS pin and drive the CS pin high. Configuration will be paused when either signal is inactive. Hold the nCS and CS pins active during configuration and initialization. The design can use these pins as user I/O pins after configuration. |
| nWS | I/O, Input | Active-low write strobe input to latch a byte of data on the DATA pins. This pin can be used as a user I/O pin after configuration. |
| PGM[2..0] | I/O, Output | These output pins control one of eight pages in the EPC16 configuration device when using remote update or local update configuration modes. When not using remote update or local update configuration modes, these pins are user I/O pins. |
| RUP[8..1] | I/O, Input | Reference pins for banks 8 to 1. The external precision resistors RUP must be connected to the designated RUP pin on that I/O bank. If not required, these pins are regular I/O pins. |

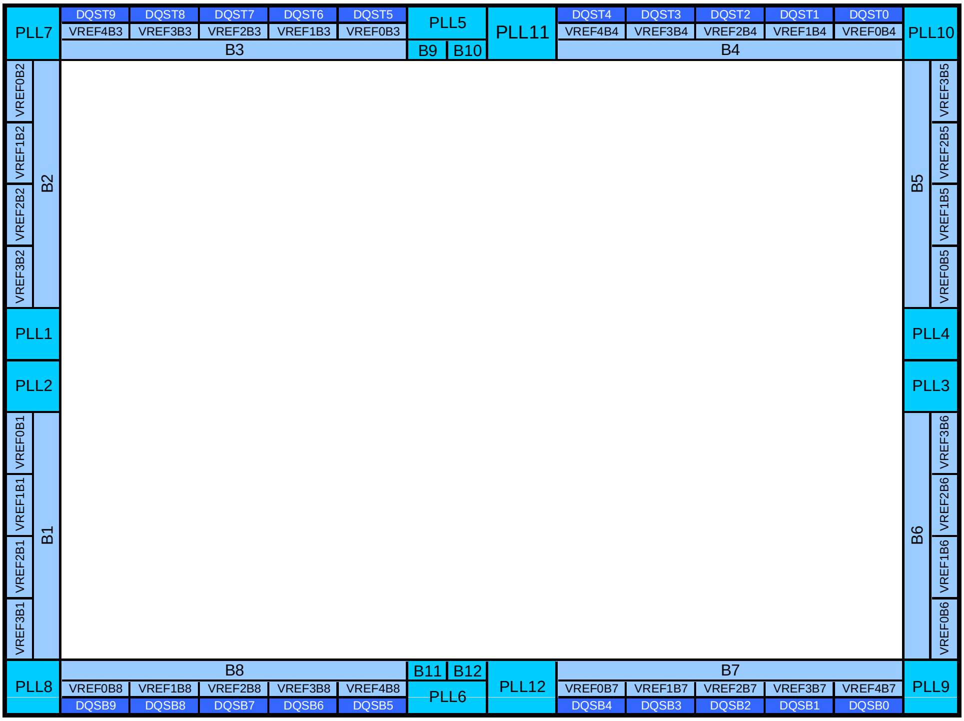
Table 7–3. Pin Definitions for the EP1S80 Device (Part 6 of 6)

| | | |
|---|---|---|
| RDN[8..1] | I/O, Input | Reference pins for banks 8 to 1. The external precision resistors RDN must be connected to the designated RDN pin on that I/O bank. If not required, these pins are regular I/O pins. |
| RUnLU | I/O, Input | Input control pin to select remote update or local update modes. If MSEL2 = 1, this is a input control pin to select remote update (RUnLU =1) or local update (RUnLU =0) modes. If MSEL2=0, the RUnLU pin is a user I/O pin. |

# PLL and Bank Diagram

Figure 7–1 shows the PLL and bank locations for the EP1S80 device.

*Figure 7–1. PLL and Bank Diagram* *Notes (1), (2)*



*Notes for Figure 7–1:*

(1) This is a top view of the silicon die. For flip chip packages the die is mounted up-side down in the package.

(2) This is a pictoral representation only to get an idea of placement on the device. Refer to the pin-list and the Quartus II for exact locations.

## Fast PLL to High-Speed I/O Connections

Table 7–4 displays the clock resources for high-speed differential I/O (DIFFIO) Receiver and Transmitter channels.

*Table 7–4. EP1S80 Clock Resources for High-Speed Differential I/O (DIFFIO) Receiver & Transmitter Channels (Part 1 of 2)*

| Pin Count | Fast PLL Source | Receiver Channels *(1)*, *(5)* | | Transmitter Channels *(2)*, *(5)* | | Overlapped Receiver Channels *(3)*, *(5)* | | Overlapped Transmitter Channels *(4)*, *(5)* | |
|---|---|---|---|---|---|---|---|---|---|
| | | High | Low | High | Low | High | Low | High | Low |
| 956 | PLL1 | [38-57] | - | [48-57] | - | [48-57] | - | [48-57] | - |
| | PLL2 | [18-37] | - | [18-27] | - | [18-27] | - | [18-27] | - |
| | PLL3 | [114-133] | - | [124-133] | - | [124-133] | - | [124-133] | - |
| | PLL4 | [94-113] | - | [94-103] | - | [94-103] | - | [94-103] | - |
| | PLL7 | [48-57] | - | [48-67] | - | [48-57] | - | [48-57] | - |
| | PLL8 | [18-27] | - | [8-27] | - | [18-27] | - | [18-27] | - |
| | PLL9 | [124-133] | - | [124-143] | - | [124-133] | - | [124-133] | - |
| | PLL10 | [94-103] | - | [84-103] | - | [94-103] | - | [94-103] | - |
| 1,020 | PLL1 | [38-57] | - | [48-57] | [46-47] | [48-57] | - | [48-57] | - |
| | PLL2 | [18-37] | - | [18-27] | [28-31] | [18-27] | - | [18-27] | - |
| | PLL3 | [114-133] | - | [124-133] | [120-123] | [124-133] | - | [124-133] | - |
| | PLL4 | [94-113] | - | [94-103] | [104-105] | [94-103] | - | [94-103] | - |
| | PLL7 | [48-57] | [58-59] | [48-67] | - | [48-57] | - | [48-67] | - |
| | PLL8 | [18-27] | [15-17] | [8-27] | - | [18-27] | - | [8-27] | - |
| | PLL9 | [124-133] | [135-137] | [124-143] | - | [124-133] | - | [124-143] | - |
| | PLL10 | [94-103] | [90-91] | [84-103] | - | [94-103] | - | [84-103] | - |

***Table 7–4. EP1S80 Clock Resources for High-Speed Differential I/O (DIFFIO) Receiver & Transmitter Channels (Part 2 of 2)***

| Pin Count | Fast PLL Source | Receiver Channels *(1)*, *(5)* | | Transmitter Channels *(2)*, *(5)* | | Overlapped Receiver Channels *(3)*, *(5)* | | Overlapped Transmitter Channels *(4)*, *(5)* | |
|---|---|---|---|---|---|---|---|---|---|
| | | High | Low | High | Low | High | Low | High | Low |
| 1,508 | PLL1 | [38-57] | - | [48-57] | [38-47] | [48-57] | - | [48-57] | - |
| | PLL2 | [18-37] | - | [18-27 | [28-37] | [18-27] | - | [18-27] | - |
| | PLL3 | [114-113] | - | [124-133] | [114-123] | [124-133] | - | [124-133] | - |
| | PLL4 | [94-113] | - | [94-103] | [104-113] | [94-103] | - | [94-103] | - |
| | PLL7 | [48-57] | [62-75] | [48-67] | [68-75] | [48-57] | - | [48-67] | - |
| | PLL8 | [18-27] | [0-13] | [8-27] | [0-7] | [18-27] | - | [8-27] | - |
| | PLL9 | [124-133] | [138-151] | [124-143] | [144-151] | [124-133] | - | [124-143] | - |
| | PLL10 | [94-103] | [76-89] | [84-103] | [76-83] | [94-103] | - | [84-103] | - |

*Notes for Table 7–4:*

(1) These receiver channels can be clocked by the PLL listed in the "Fast PLL Source" column.

(2) These transmitter channels can be clocked by the PLL listed in the "Fast PLL Source" column.

(3) These receiver channels can be driven by the PLL listed in the "Fast PLL Source" or alternatively be driven by the other adjacent fast PLL. See the PLL & Bank Diagram for PLL locations.

(4) These transmitter channels can be driven by the PLL listed in the "Fast PLL Source" or alternatively be driven by the other adjacent fast PLL. See the PLL & Bank Diagram for PLL locations.

(5) Each range of channel numbers are shown in [ ] brackets. For example PLL1, can clock `DIFFIO_RX38` to `DIFFIO_RX57`, therefore the range is shown as [38-57].

# Section II. PCB Layout Guidelines

This section provides information for board layout designers to successfully layout their boards for Stratix devices. They contain the required PCB layout guidelines, device pin tables, and package specifications.

This section contains the following chapters:

- Chapter 8. Package Information for Stratix Devices
- Chapter 9. Designing with FineLine BGA Packages

## Revision History

The table below shows the revision history for Chapter 8 and 9.

| Chapter(s) | Date / Version | Changes Made |
|---|---|---|
| 7 | August 2001<br>v1.1 | Updated Table 9–6. |
| | v1.03 | Updated the "PCB Layout for FineLine BGA Packages" section and Table 9–6. |
| | v1.02 | Minor updates. |
| | v1.01 | Updated Table 9–6. |
| 6 through12 | April 2003<br>v1.0 | Removed from Volume 1 and created Volume 3 for with pin table information. |
| 13 & 14 | April 2003<br>v1.0 | Moved to Volume 3 and are now Chapters 8 and 9. |

# 8. Package Information for Stratix Devices

S5V3008-1.0

## Introduction

This data sheet provides package information for Altera® devices. It includes these sections:

In this data sheet, packages are listed in order of ascending pin count.

In this data sheet, packages are listed in order of ascending pin count.

## Device & Package Cross Reference

Table 8–1 shows which Altera Stratix devices are available in BGA, FineLine BGA and Ultra FineLine BGA packages.

*Table 8–1. Stratix Devices in BGA, FineLine BGA & Ultra FineLine BGA Packages (Part 1 of 2)*

| Device | Package | Pins |
|---|---|---|
| EP1S10 | Thermally Enhanced FineLine BGA | 484 |
| | Non-Thermally Enhanced BGA Cavity Up | 672 |
| | Non-Thermally Enhanced FineLine BGA | 672 |
| | Thermally Enhanced FineLine BGA | 780 |
| EP1S20 | Thermally Enhanced FineLine BGA | 484 |
| | Non-Thermally Enhanced BGA Cavity Up | 672 |
| | Non-Thermally Enhanced FineLine BGA | 672 |
| | Thermally Enhanced FineLine BGA | 780 |
| EP1S25 | Non-Thermally Enhanced BGA Cavity Up | 672 |
| | Non-Thermally Enhanced FineLine BGA | 672 |
| | Thermally Enhanced FineLine BGA | 780 |
| | Thermally Enhanced FineLine BGA | 1,020 |
| EP1S30 | Thermally Enhanced FineLine BGA | 780 |
| | Thermally Enhanced BGA Cavity Up | 956 |
| | Thermally Enhanced FineLine BGA | 1,020 |

*Table 8–1. Stratix Devices in BGA, FineLine BGA & Ultra FineLine BGA Packages (Part 2 of 2)*

| Device | Package | Pins |
|---|---|---|
| EP1S40 | Thermally Enhanced BGA Cavity up | 956 |
| | Thermally Enhanced FineLine BGA | 1,020 |
| | Thermally Enhanced FineLine BGA | 1,508 |
| EP1S60 | Thermally Enhanced BGA Cavity Up | 956 |
| | Thermally Enhanced FineLine BGA | 1,020 |
| | Thermally Enhanced FineLine BGA | 1,508 |
| EP1S80 | Thermally Enhanced BGA Cavity Up | 956 |
| | Thermally Enhanced FineLine BGA | 1,020 |
| | Thermally Enhanced FineLine BGA | 1,508 |

## Thermal Resistance

Table 8–2 provides $\theta_{JA}$ (junction-to-ambient thermal resistance) and $\theta_{JC}$ (junction-to-case thermal resistance) values for Altera Stratix devices.

*Table 8–2. Thermal Resistance of Stratix Devices (Part 1 of 2)*

| Device | Pin Count | Package | $\theta_{JC}$ (° C/W) | $\theta_{JA}$ (° C/W) Still Air | $\theta_{JA}$ (° C/W) 100 ft./min. | $\theta_{JA}$ (° C/W) 200 ft./min. | $\theta_{JA}$ (° C/W) 400 ft./min. |
|---|---|---|---|---|---|---|---|
| EP1S10 | 484 | FBGA | 0.38 | 11.9 | 9.8 | 8.4 | 7.2 |
| | 672 | BGA | 3.2 | 16.8 | 13.7 | 11.9 | 10.5 |
| | 672 | FBGA | 3.4 | 17.2 | 14 | 12.2 | 10.8 |
| | 780 | FBGA | 0.43 | 10.9 | 8.8 | 7.4 | 6.3 |
| EP1S20 | 484 | FBGA | 0.30 | 11.8 | 9.7 | 8.3 | 7.1 |
| | 672 | BGA | 2.5 | 15.5 | 12.4 | 10.7 | 9.3 |
| | 672 | FBGA | 2.7 | 16 | 12.8 | 11 | 9.6 |
| | 780 | FBGA | 0.31 | 10.7 | 8.6 | 7.2 | 6.1 |
| EP1S25 | 672 | BGA | 2.2 | 14.8 | 11.7 | 10.0 | 8.7 |
| | 672 | FBGA | 2.3 | 15.3 | 12 | 10.4 | 9 |
| | 780 | FBGA | 0.25 | 10.5 | 8.5 | 7.1 | 6.0 |
| | 1020 | FBGA | 0.25 | 10.0 | 8.0 | 6.6 | 5.5 |

*Table 8–2. Thermal Resistance of Stratix Devices (Part 2 of 2)*

| Device | Pin Count | Package | $\theta_{JC}$ (° C/W) | $\theta_{JA}$ (° C/W) Still Air | $\theta_{JA}$ (° C/W) 100 ft./min. | $\theta_{JA}$ (° C/W) 200 ft./min. | $\theta_{JA}$ (° C/W) 400 ft./min. |
|---|---|---|---|---|---|---|---|
| EP1S30 | 780 | FBGA | 0.2 | 10.4 | 8.4 | 7.0 | 5.9 |
| | 956 | BGA | 0.2 | 9.1 | 7.1 | 5.8 | 4.8 |
| | 1020 | FBGA | 0.2 | 9.9 | 7.9 | 6.5 | 5.4 |
| EP1S40 | 780 | FBGA | 0.17 | 10.4 | 8.3 | 6.9 | 5.8 |
| | 956 | BGA | 0.18 | 9.0 | 7.0 | 5.7 | 4.7 |
| | 1020 | FBGA | 0.17 | 9.8 | 7.8 | 6.4 | 5.3 |
| | 1508 | FBGA | 0.18 | 9.1 | 7.1 | 5.8 | 4.7 |
| EP1S60 | 956 | BGA | 0.13 | 8.9 | 6.9 | 5.6 | 4.6 |
| | 1020 | FBGA | 0.13 | 9.7 | 7.7 | 6.3 | 5.2 |
| | 1508 | FBGA | 0.13 | 8.9 | 7.0 | 5.6 | 4.6 |
| EP1S80 | 956 | BGA | 0.1 | 8.8 | 6.8 | 5.5 | 4.5 |
| | 1020 | FBGA | 0.1 | 9.6 | 7.6 | 6.2 | 5.1 |
| | 1508 | FBGA | 0.1 | 8.8 | 6.9 | 5.5 | 4.5 |

## Package Outlines

The package outlines on the folowing pages are listed in order of ascending pin count. Altera package outlines meet the requirements of *JEDEC Publication No. 95.*

## 484-Pin Thermally Enhanced FineLine Ball-Grid Array (FBGA)

- All dimensions and tolerances conform to ANSI Y14.5M – 1994.
- Controlling dimension is in millimeters.
- Some devices have a chamfered corner at the A-1 ball location.
- M is the maximum solder ball matrix size.

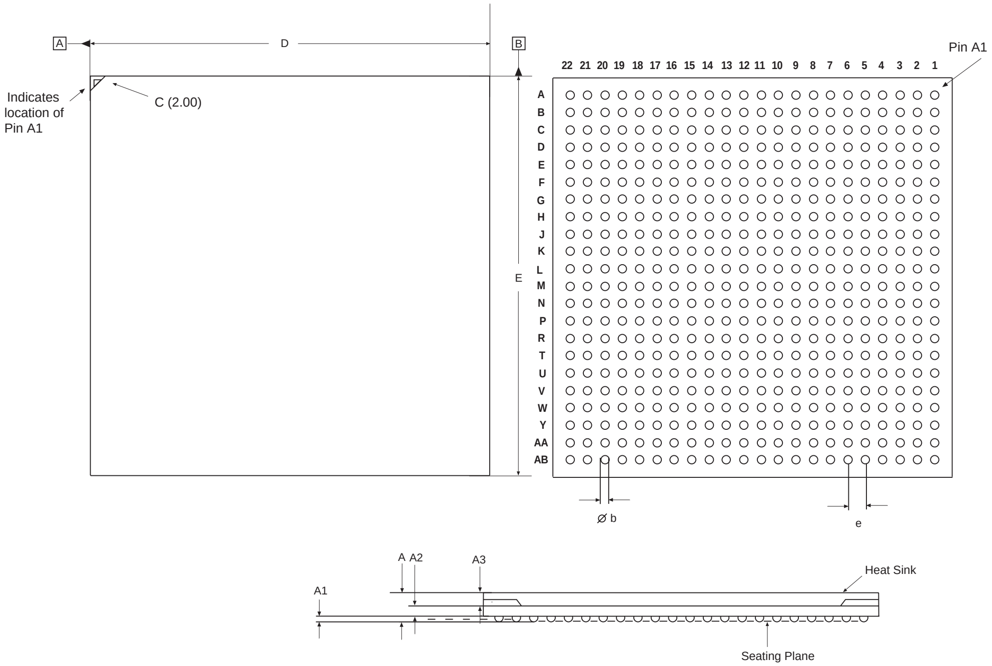
***Package Information***

| Description | Specification |
|---|---|
| Ordering Code Reference | F |
| Package Acronym | FBGA |
| Lead Material | Tin-lead alloy (63/37) |
| Lead Finish | N/A |
| JEDEC Outline | MS-034 |
| JEDEC Option | AAJ-1 |
| Maximum Lead Coplanarity | 0.008 inches (0.20 mm) |
| Weight | 3.6 g |
| Moisture Sensitivity Level | Printed on moisture barrier bag |

***Package Outline Figure Reference***

| Symbol | Millimeters | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | – | – | 3.50 |
| A1 | 0.30 | – | – |
| A2 | 0.25 | – | 3.00 |
| A3 | – | – | 2.50 |
| D/E | 23.00 BSC | | |
| b | 0.50 | 0.60 | 0.70 |
| e | 1.00 BSC | | |
| M | 22 | | |

## Package Outline



## 672-Pin Non-Thermally Enhanced FineLine Ball-Grid Array (FBGA)

- All dimensions and tolerances conform to ANSI Y14.5M – 1994.
- Controlling dimension is in millimeters.
- Some devices have a chamfered corner at the A-1 ball location.
- M is the maximum solder ball matrix size.

***Package Information***

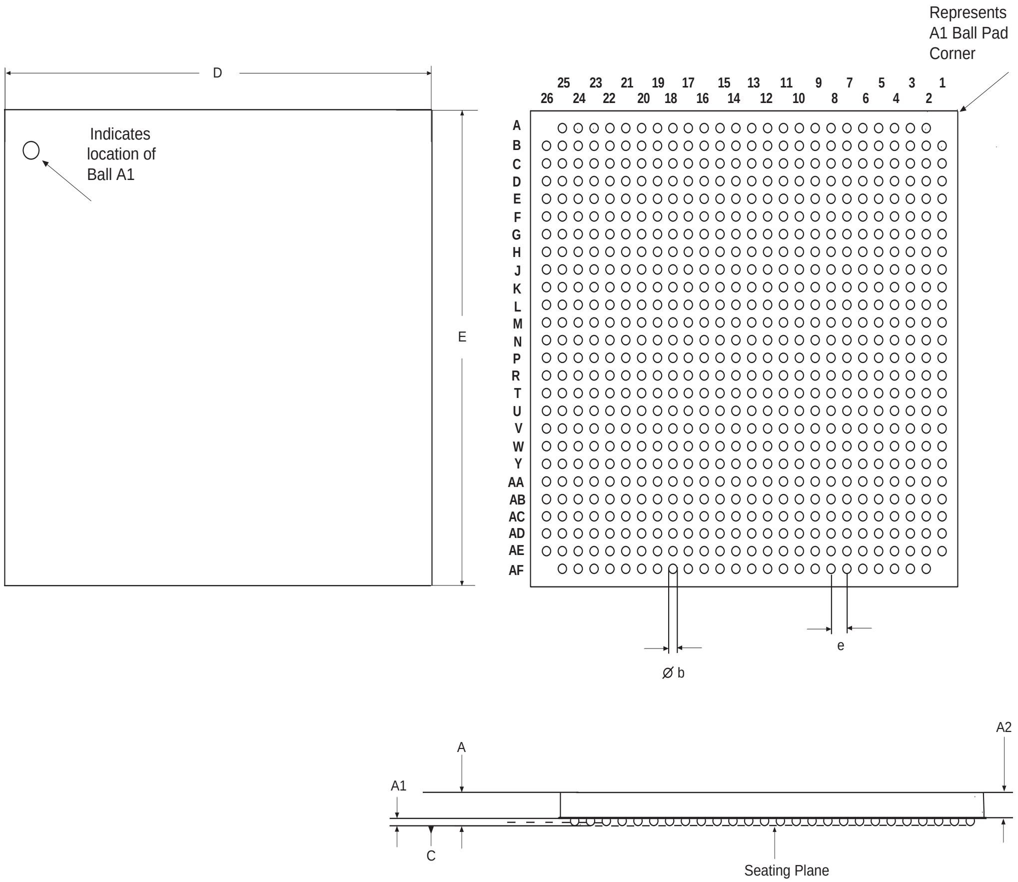
| Description | Specification |
|---|---|
| Ordering Code Reference | F |
| Package Acronym | FBGA |
| Lead Material | Tin-lead alloy (63/37) |
| Lead Finish | N/A |
| JEDEC Outline | MS-034 |
| JEDEC Option | AAL-1 |
| Maximum Lead Coplanarity | 0.008 inches (0.20 mm) |
| Weight | 3.0 g |
| Moisture Sensitivity Level | Printed on moisture barrier bag |

***Package Outline Figure Reference***

| Symbol | Millimeters | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A *(1)* | – | – | 3.50 |
| A1 | 0.30 | – | – |
| A2 | 0.25 | – | 3.00 |
| D/E | 27.00 BSC | | |
| b | 0.50 | 0.60 | 0.70 |
| e | 1.00 BSC | | |
| M | 26 | | |

(1) Altera's thickness specification for A is 2.6 mm maximum. The Max item for A in the table reflects the JEDEC specification.

## Package Outline



## 672-Pin Thermally Enhanced FineLine Ball-Grid Array (FBGA)

- All dimensions and tolerances conform to ANSI Y14.5M – 1994.
- Controlling dimension is in millimeters.
- Orientation of the package is shown by a chamfer and/or a pin 1 mark.

***Package Information***

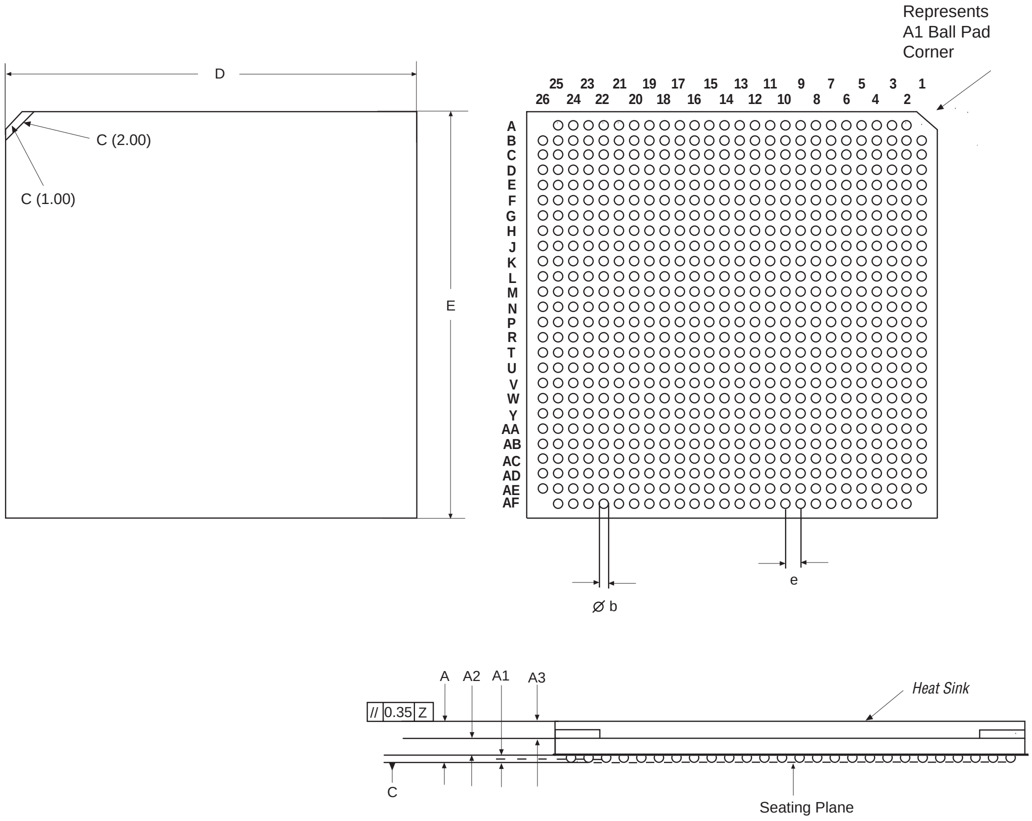
| Description | Specification |
|---|---|
| Ordering Code Reference | F |
| Package Acronym | FBGA |
| Lead Material | Tin-lead alloy (63/37) |
| Lead Finish | N/A |
| JEDEC Outline | MS-034 |
| JEDEC Option | AAL-1 |
| Maximum Lead Coplanarity | 0.008 inches (0.20 mm) |
| Weight | 4.9 g<br>7.66 g *(2)* |
| Moisture Sensitivity Level | Printed on moisture barrier bag |

(1) Heavier weight refers to new packages mentioned in PCN 0214.

***Package Outline Figure Reference***

| Symbol | Millimeters | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | – | – | 3.50 |
| A1 | 0.30 | – | – |
| A2 | 0.25 | – | 3.00 |
| A3 | – | – | 2.50 |
| b | 0.50 | 0.60 | 0.70 |
| e | 1.00 BSC | | |
| D/E | 27.00 BSC | | |
| M | 26 | | |

## *Package Outline*



## 672-Pin Non-Thermally Enhanced Ball-Grid Array (BGA) Cavity Up

- All dimensions and tolerances conform to ANSI Y14.5M – 1994.
- Controlling dimension is in millimeters.
- M is the maximum solder ball matrix size.

*Package Information*

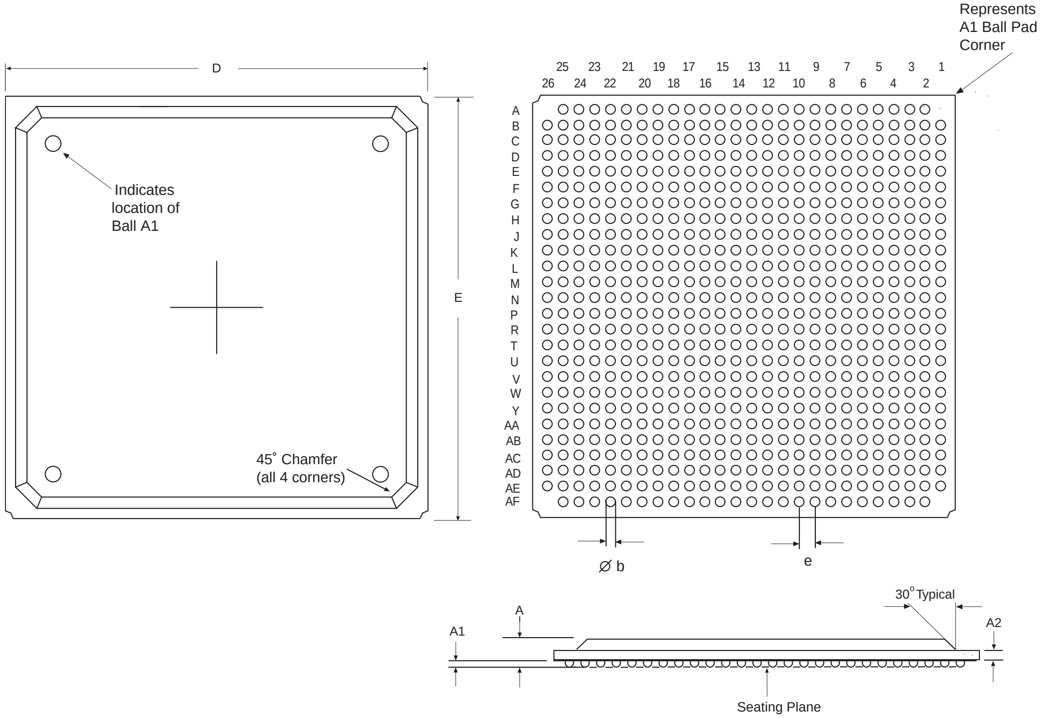
| Description | Specification |
|---|---|
| Ordering Code Reference | B |
| Package Acronym | BGA |
| Lead Material | Tin-lead alloy (63/37) |
| Lead Finish | N/A |
| JEDEC Outline | MS-034 |
| JEDEC Option | BAR-2, depopulated |
| Maximum Lead Coplanarity | 0.008 inches (0.20 mm) |
| Weight | 5.2 g |
| Moisture Sensitivity Level | Printed on moisture barrier bag |

*Figure Reference*

| Symbol | Millimeters | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A *(3)* | – | – | 3.50 |
| A1 | 0.35 | – | – |
| A2 | 0.25 | – | 3.00 |
| b | 0.60 | 0.75 | 0.90 |
| D/E | 35.00 BSC | | |
| e | 1.27 BSC | | |
| M | 26 | | |

(1) Altera's thickness specification for A is 2.6 mm maximum. The Max item for A in the table reflects the JEDEC specification.

## Package Outline



## 780-Pin Thermally Enhanced FineLine Ball-Grid Array (FBGA)

- All dimensions and tolerances conform to ANSI Y14.5M – 1994.
- Controlling dimension is in millimeters.
- Orientation of the package is shown by a chamfer and/or a pin 1 mark.

*Package Information*

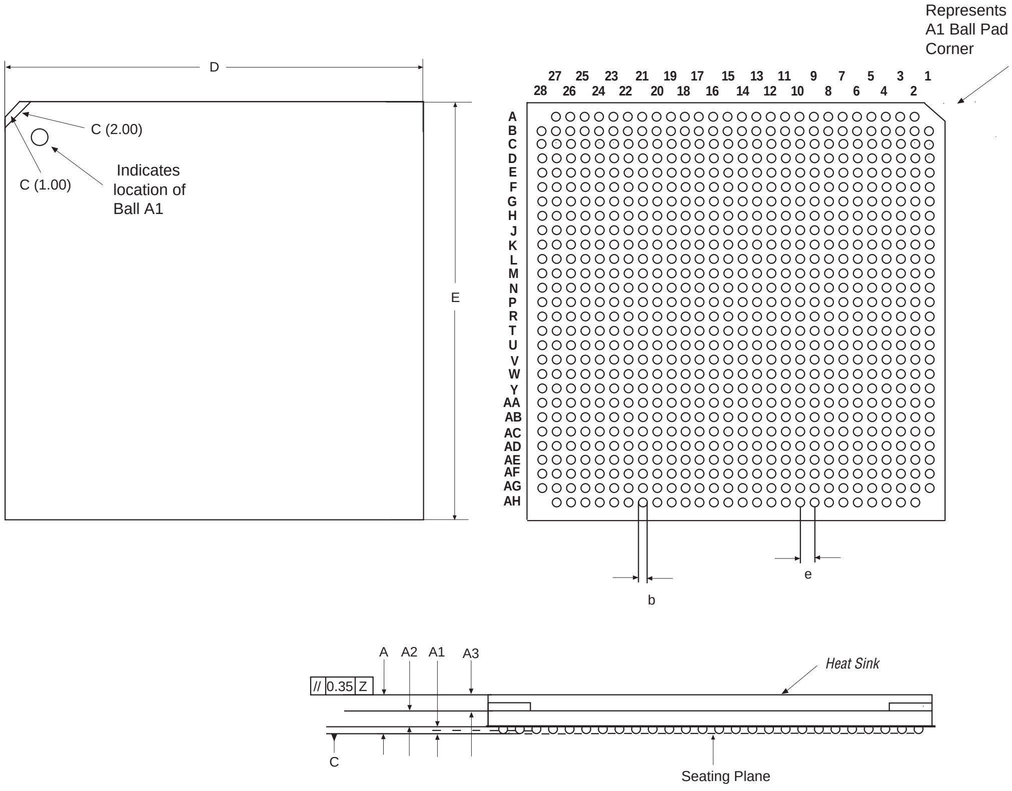
| Description | Specification |
|---|---|
| Ordering Code Reference | F |
| Package Acronym | FBGA |
| Lead Material | Tin-lead alloy (63/37) |
| Lead Finish | N/A |
| JEDEC Outline | MS-034 |
| JEDEC Option | AAM-1 |
| Maximum Lead Coplanarity | 0.008 inches (0.20 mm) |
| Weight | 5.8 g<br>8.9 g *(4)* |
| Moisture Sensitivity Level | Printed on moisture barrier bag |

(1) Note: Heavier weight refers to new packages mentioned in PCN 0214.

*Package Outline Figure Reference*

| Symbol | Millimeters | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | – | – | 3.50 |
| A1 | 0.35 | – | – |
| A2 | 0.25 | – | 3.00 |
| A3 | – | – | 2.50 |
| b | 0.50 | 0.60 | 0.70 |
| e | 1.00 BSC | | |
| D/E | 29.00 BSC | | |
| M | 28 | | |

## Package Outline



## 956-Pin Thermally Enhanced Ball Grid Array (BGA) Cavity Up

- All dimensions and tolerances conform to ANSI Y14.5M – 1994.
- Controlling dimension is in millimeters.
- Orientation of the package is shown by a chamfer and/or a pin 1 mark.
- M is the maximum solder ball matrix size.

***Package Information***

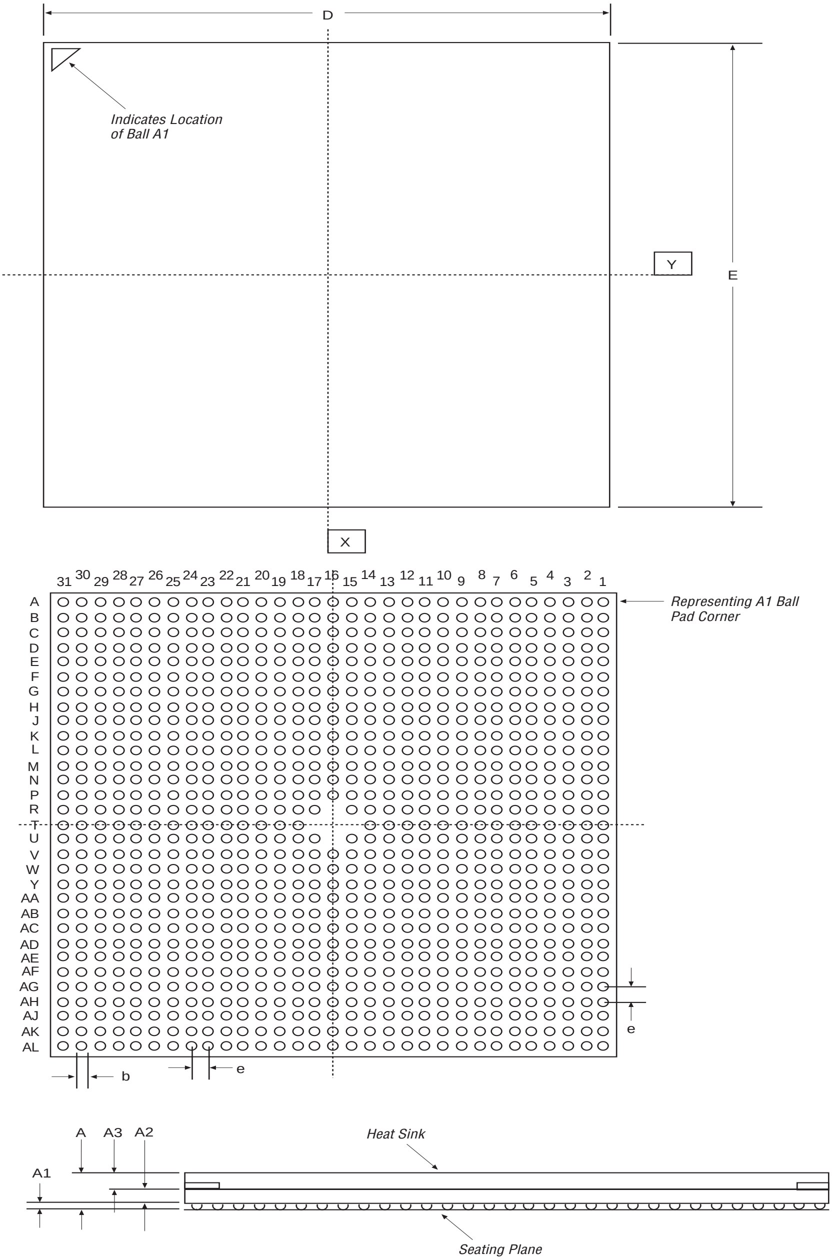
| Description | Specification |
|---|---|
| Ordering Code Reference | B |
| Package Acronym | BGA |
| Lead Material | Tin-lead alloy (63/37) |
| Lead Finish | N/A |
| JEDEC Outline | MS-034 |
| JEDEC Option | BAU-1 |
| Maximum Lead Co-planarity | 0.008 inches (0.20 mm) |
| Weight | 8.7 g<br>15.30 g *(5)* |
| Moisture Sensitivity Level | Printed on moisture barrier bag |

(1) Note: Heavier weight refers to new packages mentioned in PCN 0214.

***Table 8–1. Figure Reference***

| Symbol | Millimeters | | |
|---|---|---|---|
| | **Min.** | **Nom.** | **Max.** |
| A | – | – | 3.5 |
| A1 | 0.35 | – | – |
| A2 | 0.25 | – | 3.00 |
| A3 | – | – | 2.5 |
| b | 0.60 | 0.75 | 0.90 |
| D/E | 40.00 BSC | | |
| e | 1.27 BSC | | |
| M | 31 | | |

## Package Outline



## 1020-Pin Thermally Enhanced FineLine Ball-Grid Array (FBGA)

- All dimensions and tolerances conform to ANSI Y14.5M – 1994.
- Controlling dimension is in millimeters.
- Orientation of the package is shown by a chamfer and/or a pin 1 mark.
- M is the maximum solder ball matrix size.

***Package Information***

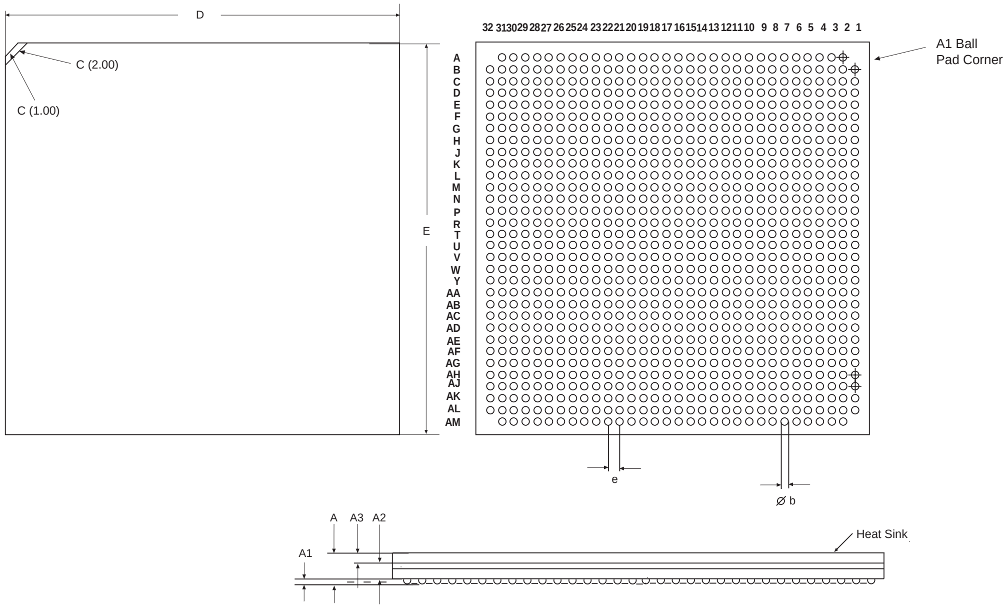
| Description | Specification |
|---|---|
| Ordering Code Reference | F |
| Package Acronym | FBGA |
| Lead Material | Tin-lead alloy (63/37) |
| Lead Finish | N/A |
| JEDEC Outline | MS-034 |
| JEDEC Option | AAP-1, depopulated |
| Maximum Lead Coplanarity | 0.008 inches (0.20 mm) |
| Weight | 7.7 g<br>11.54 g *(6)* |
| Moisture Sensitivity Level | Printed on moisture barrier bag |

(1) Note: Heavier weight refers to new packages mentioned in PCN 0214.

***Package Outline Figure Reference***

| Symbol | Millimeters | | |
|---|---|---|---|
| | **Min.** | **Nom.** | **Max.** |
| A | – | – | 3.50 |
| A1 | 0.35 | – | – |
| A2 | 0.25 | – | 3.00 |
| A3 | – | – | 2.50 |
| b | 0.50 | 0.60 | 0.70 |
| e | 1.00 BSC | | |
| D/E | 33.00 BSC | | |
| M | 32 | | |

## Package Outline



## 1508-Pin Thermally Enhanced FineLine Ball-Grid Array (FBGA)

- All dimensions and tolerances conform to ANSI Y14.5M – 1994.
- Controlling dimension is in millimeters.
- Orientation of the package is shown by a chamfer and/or a pin 1 mark.
- M is the maximum solder ball matrix size.

*Package Information*

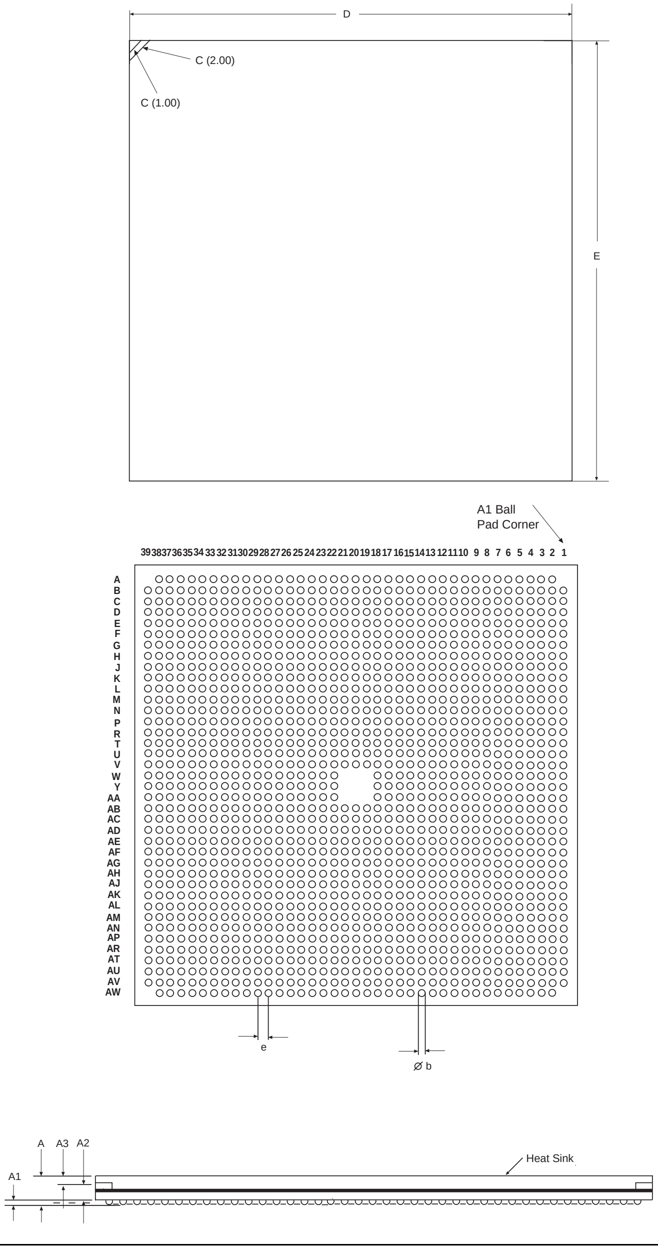
| Description | Specification |
|---|---|
| Ordering Code Reference | F |
| Package Acronym | FBGA |
| Lead Material | Tin-lead alloy (63/37) |
| Lead Finish | N/A |
| JEDEC Outline | MS-034 |
| JEDEC Option | AAU-1 |
| Maximum Lead Coplanarity | 0.008 inches (0.20 mm) |
| Weight | 9.3 g<br>15.30 g *(7)* |
| Moisture Sensitivity Level | Printed on moisture barrier bag |

(1) Heavier weight refers to new packages mentioned in PCN 0214.

*Package Outline Figure Reference*

| Symbol | Millimeters | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | – | – | 3.50 |
| A1 | 0.35 | – | – |
| A2 | 0.25 | – | 3.00 |
| A3 | – | – | 2.50 |
| b | 0.50 | 0.60 | 0.70 |
| e | 1.00 BSC | | |
| D/E | 40.00 BSC | | |
| M | 39 | | |

## Package Outline



# 9. Designing with FineLine BGA Packages

S5V3009-1.0

Chapter 9, Designing with FineLine BGA Packages, replaces *AN 114: Designing with FineLine BGA Packages.*

## Introduction

As programmable logic devices (PLDs) increase in density and I/O pins, the demand for small packages and diverse packaging options continues to grow. Ball-grid array (BGA) packages are an ideal solution because the I/O connections are on the interior of the device, improving the ratio between pin count and board area. Typical BGA packages contain up to twice as many connections as quad flat pack (QFP) packages for the same area. Further, BGA solder balls are considerably stronger than QFP leads, resulting in robust packages that can tolerate rough handling.

Altera has developed a new BGA solution for users of high-density PLDs called the FineLine BGA™ package. The new format requires less than half the board space of standard BGA packages. This application note provides guidelines for designing your printed circuit board (PCB) for Altera's FineLine BGA packages and discusses the following topics:

- Overview of BGA packages
- PCB layout terminology
- PCB layout for FineLine BGA packages

## Overview of BGA Packages

As PLDs grow to 1 million gates and beyond, designers require more advanced, flexible packages. BGA packages empower designers by offering the technological benefits and flexibility to meet future system requirements.

In BGA packages, the I/O connections are located on the interior of the device. Leads normally placed along the periphery of the package are replaced with solder balls arranged in a matrix across the bottom of the substrate. The final device is soldered directly to the PCB using assembly processes virtually identical to the standard surface mount technology preferred by system designers.

In addition, BGA packages provide the following advantages:

- *Fewer damaged leads*—BGA leads consist of solid solder balls, which are less likely to suffer damage during handling.

- *More leads per unit area*—Lead counts are increased by moving the solder balls closer to the edges of the package and by decreasing the pitch to 1.0 mm.
- *Less expensive surface mount equipment*—BGA packages can tolerate slightly imperfect placement during mounting, requiring less expensive surface mount equipment. The placement can be imperfect because the BGA packages self-align during solder reflow.
- *Smaller footprints*—BGA packages are usually 20% to 50% smaller than QFP packages, making BGA packages more attractive for applications that require high performance and a smaller footprint.
- *Integrated circuit speed advantages*—BGA packages can operate well into the microwave frequency spectrum and can achieve high electrical performance by using ground planes, ground rings, and power rings in the package construction.
- *Improved heat dissipation*—Because the die is located at the center of the FineLine BGA package and most `VCC` and `GND` pins are located at the center of the package, the `GND` and `VCC` pins are located under the die. As a result, the heat generated in the device can be transferred out through the `GND` and `VCC` pins (i.e., the `GND` and `VCC` pins act as a heat sink).

## PCB Layout Terminology

This section defines common terms used in PCB layout.

### Escape Routing

Escape routing is the method used to route each signal from a package to another element on the PCB.

### Multi-Layer PCBs

The increased I/O count associated with BGA packages has made multi-layer PCBs the industry-standard method for performing escape routing. Signals can be routed to other elements on the PCB through various numbers of PCB layers.

### Vias

Vias, or plated through holes, are used in multi-layer PCBs to transfer signals from one layer to another. Vias are actual holes drilled through a multi-layer PCB and provide electrical connections between various PCB layers. All vias provide layer-to-layer connections only; device leads or other reinforcing material are not inserted into vias.

Table 9–1 describes the terms used to define via dimensions.

*Table 9–1. Via Dimension Terms*

| Term | Definition |
|---|---|
| Aspect ratio | The aspect ratio is the ratio of a via's length or depth to its pre-plated diameter. |
| Drilled hole diameter | The drilled hole diameter is the diameter of the actual via hole drilled in the board. |
| Finished via diameter | The finished via diameter is the diameter of a via hole that has been finished. |

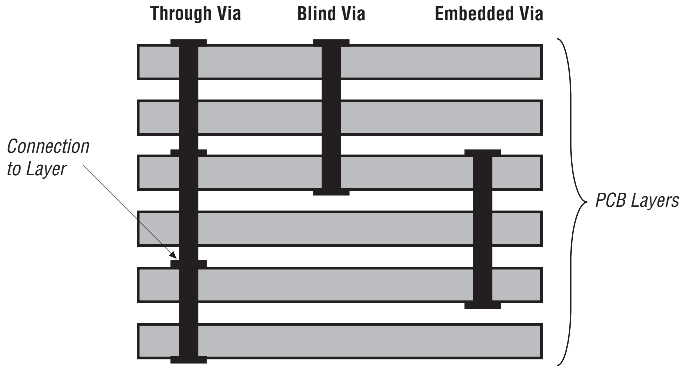
Table 9–2 shows the three via types typically used on PCBs.

*Table 9–2. Via Types*

| Type | Description |
|---|---|
| Through via | An interconnection between the top and the bottom layer of a PCB. Through vias can also provide interconnections to inner PCB layers. |
| Blind via | An interconnection from the top or bottom layer to an inner PCB layer. |
| Embedded via | An interconnection between any number of inner PCB layers. |

Figure 9–1 shows all three via types.

*Figure 9–1. Types of Vias*



Blind vias and through vias are used more frequently than embedded vias. Blind vias can be more expensive than through vias, but overall costs can be reduced because signal traces can be routed under a blind via, requiring fewer PCB layers. Through vias, on the other hand, do not permit signals to be routed through lower layers, which can increase the required number of PCB layers and overall costs.

## Via Capture Pad

Vias are connected electrically to PCB layers through via capture pads, which surround each via.

## Surface Land Pad

Surface land pads are the areas on the PCB to which the BGA solder balls adhere. The size of these pads affects the space available for vias and escape routing. In general, surface land pads are available in the following two basic designs:

- Non solder mask defined (NSMD), also known as copper defined
- Solder mask defined (SMD)

The main differences between the two surface land pad types are the size of the trace and space, the type of vias you can use, and the shape of the solder balls after solder reflow.

### *Non Solder Mask Defined Pad*

In the non solder mask defined (NSMD) pad, the solder mask opening is larger than the copper pad. Thus, the surface land pad's copper surface is completely exposed, providing greater area to which the BGA solder ball can adhere (see Figure 9–2). Altera recommends that you use a NSMD pad for most applications because it provides more flexibility, fewer stress points, and more line-routing space between pads.

### *Solder Mask Defined Pad*

In the solder mask defined (SMD) pad, the solder mask overlaps the surface land pad's copper surface (see Figure 9–2). This overlapping provides greater adhesion strength between the copper pad and the PCB's epoxy/glass laminate, which can be important under extreme bending and during accelerated thermal cycling tests. However, the solder mask overlap shrinks the amount of copper surface available for the BGA solder ball.

Figure 9–2. Side View of NSMD & SMD Land Pads

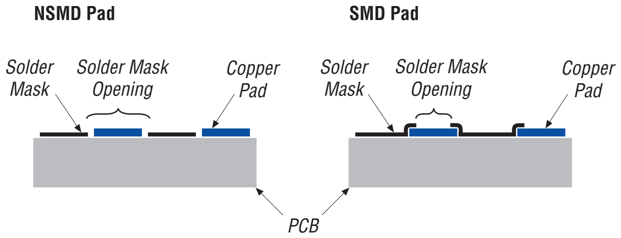
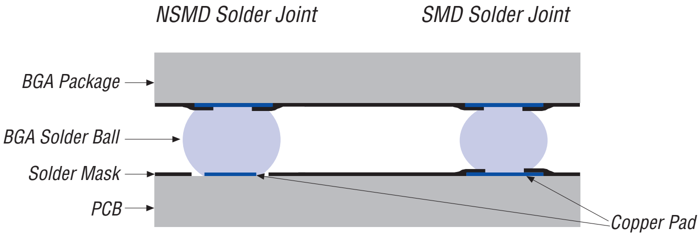


Figure 9–3 shows the side view for an NSMD and SMD solder joint.

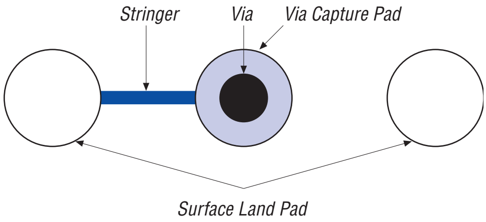
Figure 9–3. Side View of NSMD & SMD Solder Joints



## Stringer

Stringers are rectangular or square interconnect segments that electrically connect via capture pads and surface land pads. Figure 9–4 shows the connection between vias, via capture pads, surface land pads, and stringers.

Figure 9–4. Via, Land Pad, Stringer & Via Capture Pad



## PCB Layout for FineLine BGA Packages

When designing a PCB for FineLine BGA packages, consider the following factors:

- Surface land pad dimension
- Via capture pad layout and dimension
- Signal line space and trace width
- Number of PCB layers

☞ For all FineLine BGA figures, the controlling dimension is millimeters.

### Surface Land Pad Dimension

Surface land pads should be the same size as the BGA pad to provide a balanced stress on solder joints. For this reason, Altera recommends using a 15.75-mil surface land pad, because it is the same size as the BGA pad. Figure 9–5 shows a 15.75-mil BGA pad.

*Figure 9–5. 15.75-Mil BGA Pad*

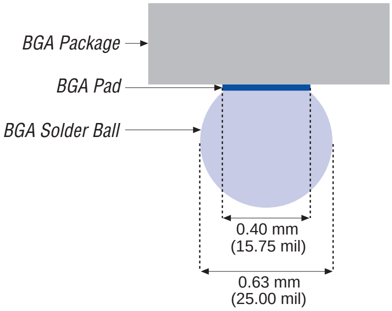
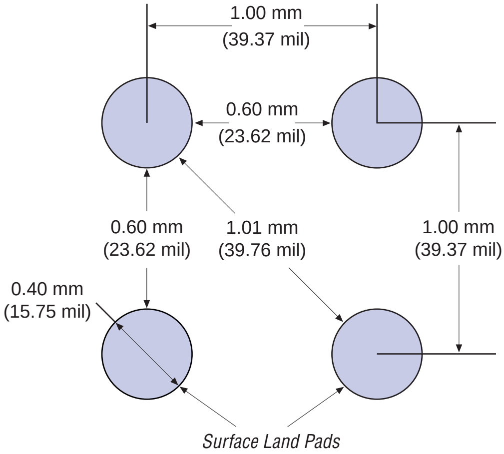


Figure 9–6 shows how much space is available for vias and escape routing when you use 15.75-mil surface land pads.

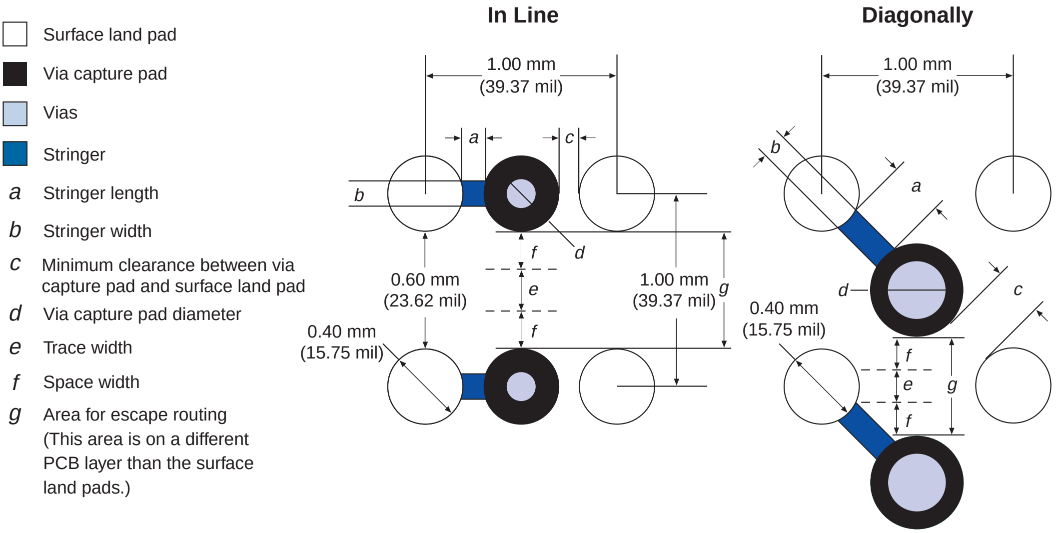
*Figure 9–6. Space Available for 15.75-Mil Surface Land Pads*



## Via Capture Pad Layout & Dimension

The size and layout of via capture pads affect the amount of space available for escape routing. In general, you can layout via capture pads in the following two ways: in-line with the surface land pads or in the diagonal of surface land pads. Figure 9–7 shows both layouts.

*Figure 9–7. Placement of Via Capture Pad*



The decision to place the via capture pads diagonally or in-line with the surface lands pads is based on the following factors:

- Diameter of the via capture pad
- Stringer length
- Clearance between via capture pad and surface land pad

To decide how to lay out your PCB, use the information shown in Figure 9–7 and Table 9–3. If your PCB design guidelines do not conform to either equation in Table 9–3, contact Altera Applications for further assistance.

*Table 9–3. Formula for Via Layouts*

| Layout | Formula |
|---|---|
| In-line | $a + c + d$ ð 23.62 mil |
| Diagonally | $a + c + d$ ð 39.76 mil |

Table 9–3 shows that you can place a larger via capture pad diagonally than in-line with the surface land pads.

Via capture pad size also affects how many traces can be routed on a PCB. Figure 9–8 shows sample layouts of typical and premium via capture pads. The typical layout shows a via capture pad size of 27 mil, a via size of 8 mil, and an inner space/trace of 4 mil. With this layout, only one trace can be routed between the vias. If more traces are required, you must reduce the via capture pad size or the space/trace size.

The premium layout shows a via capture pad size of 20 mil, a via size of 5 mil, and an inner space/trace of 3 mil. This layout provides enough space to route two traces between the vias.

*Figure 9–8. Typical & Premium Via Capture Pad Sizes*

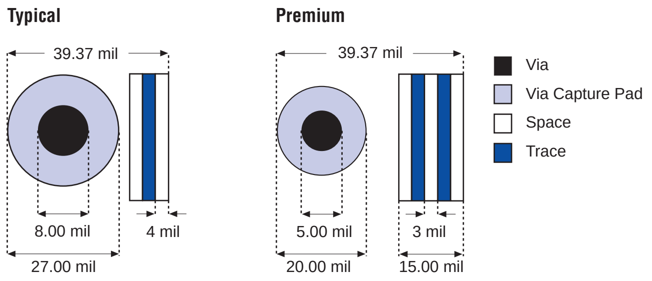


Table 9–4 shows the typical and premium layout specifications used by most PCB vendors.

*Table 9–4. Vendor Specifications*

| Specification | Typical (Mil) | Premium (Mil) |
|---|---|---|
| Trace/space width | 5/5 | 3/3 |
| Drilled hole diameter | 12 | 10 |
| Finished via diameter | 8 | ð 5 |
| Via capture pad | 25.5 | 20 |
| Aspect ratio | 7:1 | 10:1 |

For detailed information on drill sizes, via sizes, space/trace sizes, or via capture pad sizes, contact your PCB vendor directly.

## Signal Line Space & Trace Width

The ability to perform escape routing is defined by the width of the trace and the minimum space required between traces. The minimum area for signal routing is the smallest area that the signal must be routed through (i.e., the distance between two vias, or $g$ in Figure 9–7). This area is calculated by the following formula:

$$g = 39.37 - d$$

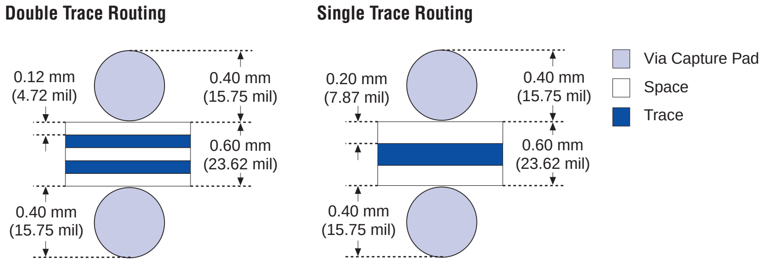
The number of traces that can be routed through this area is based on the permitted line trace and space widths. You can use Table 9–5 to determine the total number of traces that can be routed through $g$.

*Table 9–5. Number of Traces*

| Number of Traces | Formula |
|---|---|
| 1 | *g* Š [2 × (space width)] + trace width |
| 2 | *g* Š [3 × (space width)] + [2 × (trace width)] |
| 3 | *g* Š [5 × (space width)] + [3 × (trace width)] |

Figure 9–9 shows that by reducing the trace and space size, you can route more traces through $g$. Increasing the number of traces reduces the required number of PCB layers and decreases the overall cost.

*Figure 9–9. Escape Routing for Double & Single Traces*



## Number of PCB Layers

In general, the number of PCB layers required to route signals is inversely proportional to the number of traces between vias (i.e., the greater the number of traces, the fewer the number of PCB layers required). You can estimate the number of layers your PCB requires by first determining:

- Trace and space size
- Number of traces routed between the via capture pads
- Type of vias used

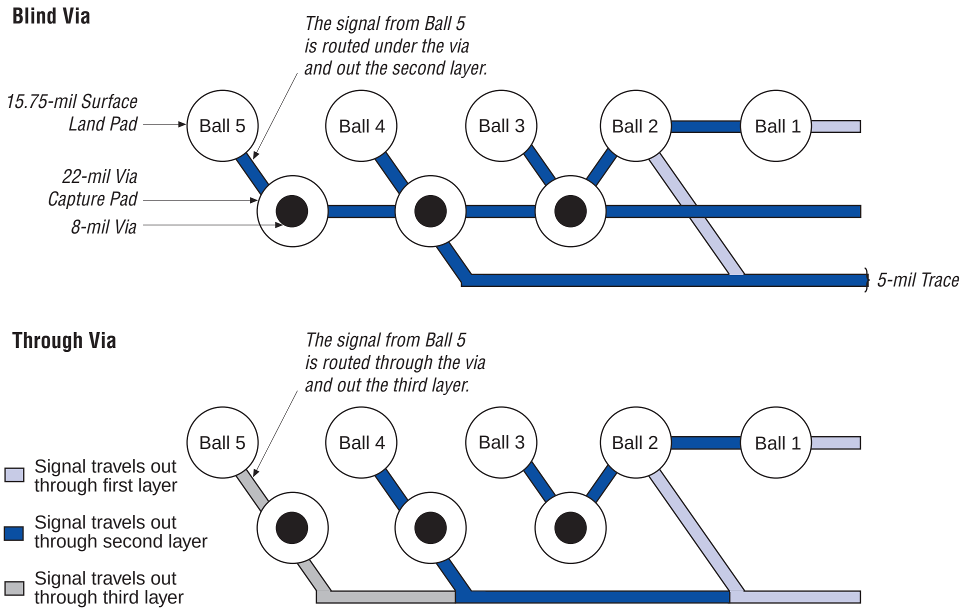
Table 9–6 shows the number of PCB layers required to route signals for various FineLine BGA packages in EPF10K50E devices, assuming the use of a power plane, ground plane, and all I/O pins. This table shows that using double traces and blind vias reduces the required number of layers.

*Table 9–6. Minimum Required PCB Layers*

| FineLine BGA Package (Balls) | Single Trace | | Double Trace | |
|---|---|---|---|---|
| | Blind Vias (Layers) | Through Vias (Layers) | Blind Vias (Layers) | Through Vias (Layers) |
| 100 | 2 | 2 | 1 | 1 |
| 256 | 2 | 2 | 2 | 2 |
| 484 | 2 | 3 | 2 | 2 |
| 672 | 3 | 4 | 2 | 3 |

Using fewer I/O pins than the maximum can reduce the required number of layers. Via type can also reduce the number of layers required. To see how the via type can affect the required number of PCB layers, consider the sample layouts shown in Figure 9–10.

*Figure 9–10. Sample PCB Layout*



The blind via layout in Figure 9–10 requires only two PCB layers. The signals from the first two balls can be routed directly through the first layer. The signals from the third and fourth balls can be routed through a via and out the second layer, and the signal from the fifth ball can be routed under the vias for Ball 4 and Ball 3 and out the second layer. Together, only two PCB layers are required.

In contrast, the through via layout in Figure 9–10 requires three PCB layers, because signals cannot be routed under through vias. The signals from the third and fourth balls can still be routed through a via and out the second layer, but the signal from the fifth ball must be routed through a via and out the third layer. Using blind vias rather than through vias in this example saves one PCB layer.

## Conclusion

Altera has taken a leadership position in PLD packaging with the recent introduction of 1.00-mm FineLine BGA packages. These packages use a reduced PCB area while maintaining a very high pin count. By using the information in this application note, you can easily design PCBs to use FineLine BGA packages, and take advantage of the package's reduced size.