

Features :

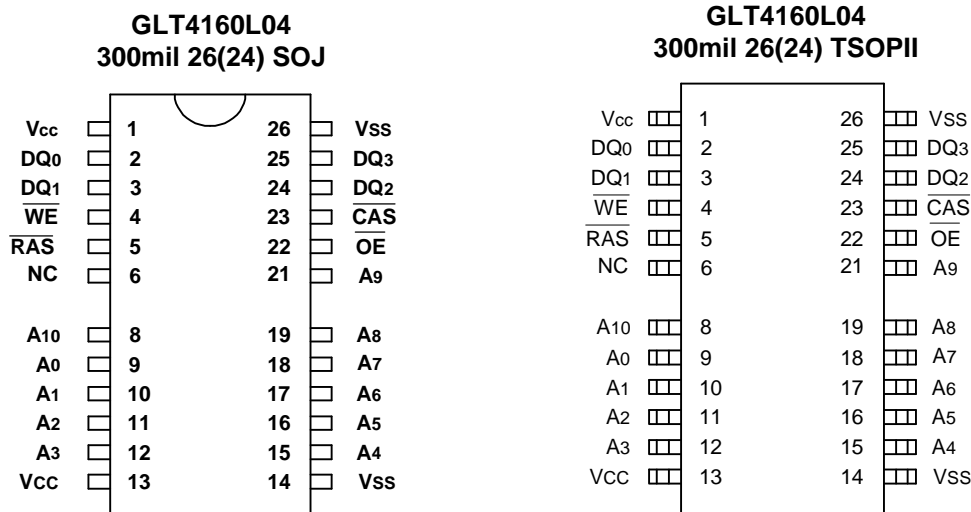
- * 4,194,304 words by 4 bits organization.
- * Fast access time and cycle time
- * Low power dissipation.
- * Read-Modify-Write, $\overline{\text{RAS}}$ -Only Refresh, $\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh, Hidden Refresh.
- * 2,048 refresh cycles per 32ms.
- * Available in 300 mil 26(24) SOJ and TSOPII.
- * 3.3V±0.3V Vcc Power Supply voltage.
- * All inputs and Outputs are LVTTTL compatible.
- * Extended Data-Out (EDO) Page access cycle.
- * Self-refresh Capability. (S-Version).

Description :

The GLT4160L04 is a high-performance CMOS dynamic random access memory containing 16,777,216 bits organized in a x4 configuration. The GLT4160L04 offers page cycle access with Extended Data Output. The GLT4160L04 has 11 row- and 11 column-addresses, and accepts 2048-cycle refresh in 32 ms.

The GLT4160L04 provides EDO PAGE MODE operation which allows for fast data access within a row-address defined boundary, up to 2048 x 4 bits with cycle times as short as 18ns.

| HIGH PERFORMANCE | 40 | 45 | 50 | 60 | 70 |
|---|-----------|-----------|-----------|-----------|-----------|
| Max. $\overline{\text{RAS}}$ Access Time, (t _{RAC}) | 40 ns | 45 ns | 50 ns | 60 ns | 70 ns |
| Max. Column Address Access Time, (t _{AA}) | 20 ns | 22 ns | 25 ns | 30 ns | 35 ns |
| Min. Extended Data Out Page Mode Cycle Time, (t _{PC}) | 18 ns | 18 ns | 20 ns | 25 ns | 30 ns |
| Min. Read/Write Cycle Time, (t _{RC}) | 70 ns | 80 ns | 84 ns | 104 ns | 124 ns |
| Max. $\overline{\text{CAS}}$ Access Time (t _{CAC}) | 12 ns | 12 ns | 13 ns | 15 ns | 20 ns |

Pin Configuration :

Pin Descriptions:

| Name | Function |
|------------------|-----------------------|
| $A_0 - A_{10}$ | Address Inputs |
| \overline{RAS} | Row Address Strobe |
| \overline{CAS} | Column Address Strobe |
| \overline{WE} | Write Enable |
| \overline{OE} | Output Enable |
| $DQ_0 - DQ_3$ | Data Inputs / Outputs |
| V_{CC} | +3.3V Power Supply |
| V_{SS} | Ground |
| NC | No Connection |

Truth Table:

| Function | | RAS | CAS | WE | OE | ADDRESS | | DATA-IN/OUT |
|------------------------------|-----------|-------|-----|-----|-----|----------------|----------------|------------------|
| | | | | | | t _R | t _C | DQ1-DQ4 |
| Standby | | H | H→X | X | X | X | X | High-Z |
| READ | | L | L | H | L | ROW | COL | Data-Out |
| EARLY WRITE | | L | L | L | X | ROW | COL | Data-In |
| READ WRITE | | L | L | H→L | L→H | ROW | COL | Data-Out,Data-In |
| EDO-PAGE-MODE READ | 1st Cycle | L | H→L | H | L | ROW | COL | Data-Out |
| | 2nd cycle | L | H→L | H | L | n/a | COL | Data-Out |
| EDO-PAGE-MODE EARLY-WRITE | 1st Cycle | L | H→L | L | X | ROW | COL | Data-In |
| | 2nd cycle | L | H→L | L | X | n/a | COL | Data-In |
| EDO-PAGE-MODE READ-WRITE | 1st Cycle | L | H→L | H→L | L→H | ROW | COL | Data-Out,Data-In |
| | 2nd cycle | L | H→L | H→L | L→H | n/a | COL | Data-Out,Data-In |
| RAS -ONLY REFRESH | | L | H | X | X | ROW | n/a | High-Z |
| HIDDEN REFRESH | READ | L→H→L | L | H | L | ROW | COL | Data-Out |
| | WRITE | L→H→L | L | L | X | ROW | COL | Data-In |
| CBR REFRESH | | H→L | L | H | X | X | X | High-Z |
| SELF REFRESH | | H→L | L | H | X | X | X | High-Z |

DC and Operating Characteristics (1-2)
 $T_A = 0^{\circ}\text{C to } 70^{\circ}\text{C, } -20^{\circ}\text{C to } 85^{\circ}\text{C } V_{CC}=3.3\text{V}\pm 0.3\text{V, } V_{SS}=0\text{V, unless otherwise specified.}$

| Sym. | Parameter | Test Conditions | Access Time | Min. | Typ | Max. | Unit | Notes |
|-----------|---|---|---|------|-----|------------------------|---------------|-------|
| I_{LI} | Input Leakage Current (any input pin) | $0\text{V} \leq V_{IN} \leq V_{CC}+0.3\text{V}$ (All other pins not under test=0V) | | -5 | | +5 | μA | |
| I_{LO} | Output Leakage Current (for High-Z State) | $0\text{V} \leq V_{out} \leq V_{CC}$ Output is disabled (Hiz) | | -5 | | +5 | μA | |
| I_{CC1} | Operating Current, Random READ/WRITE | $t_{RC} = t_{RC}(\text{min.})$ | $t_{RAC} = 40\text{ns}$ $t_{RAC} = 45\text{ns}$ $t_{RAC} = 50\text{ns}$ $t_{RAC} = 60\text{ns}$ $t_{RAC} = 70\text{ns}$ | | | 130 120 80 70 | mA | 1,2 |
| I_{CC2} | Standby Current (TTL) | $\overline{\text{RAS}}, \overline{\text{CAS}}$ at V_{IH} other inputs $\geq V_{SS}$ | | | | 1 | mA | |
| I_{CC3} | Refresh Current, RAS -Only | $\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ at V_{IH} $t_{RC} = t_{RC}(\text{min.})$ | $t_{RAC} = 40\text{ns}$ $t_{RAC} = 45\text{ns}$ $t_{RAC} = 50\text{ns}$ $t_{RAC} = 60\text{ns}$ $t_{RAC} = 70\text{ns}$ | | | 130 120 80 70 | mA | 2 |
| I_{CC4} | Operating Current, EDO Page Mode | $\overline{\text{RAS}}$ at V_{IL} , $\overline{\text{CAS}}$ address cycling: $t_{PC}=t_{PC}(\text{min.})$ | $t_{RAC} = 40\text{ns}$ $t_{RAC} = 45\text{ns}$ $t_{RAC} = 50\text{ns}$ $t_{RAC} = 60\text{ns}$ $t_{RAC} = 70\text{ns}$ | | | 130 120 80 70 | mA | 1,2 |
| I_{CC5} | Refresh Current, CAS Before RAS | $\overline{\text{RAS}}, \overline{\text{CAS}}$ address cycling: $t_{RC}=t_{RC}(\text{min.})$ | $t_{RAC} = 40\text{ns}$ $t_{RAC} = 45\text{ns}$ $t_{RAC} = 50\text{ns}$ $t_{RAC} = 60\text{ns}$ $t_{RAC} = 70\text{ns}$ | | | 130 120 80 70 | mA | 2 |
| I_{CC6} | Standby Current, (CMOS) | $\overline{\text{RAS}} \geq V_{CC}-0.2\text{V,}$ $\overline{\text{CAS}} \geq V_{CC}-0.2\text{V,}$ All other inputs V_{SS} | | | | 300 | μA | 1,5 |
| I_{CC7} | Self refresh Current | $\overline{\text{RAS}} = \overline{\text{CAS}} = 0.2\text{V,}$ $\overline{\text{WE}} = \overline{\text{OE}} = A_0 \sim A_{10} = V_{CC}-0.2\text{V or } 0.2\text{V}$ $DQ_0 \sim DQ_3 = V_{CC}-0.2\text{V, } 0.2\text{V or Open}$ | | | | 300 | μA | |
| V_{IL} | Input Low Voltage | | | -0.3 | | +0.8 | V | 3 |
| V_{IH} | Input High Voltage | | | 2.0 | | $V_{CC}+0.3$ | V | 4 |
| V_{OL} | Output Low Voltage | $I_{OL} = 2\text{mA}$ | | | | 0.4 | V | |
| V_{OH} | Output High Voltage | $I_{OH} = -2\text{mA}$ | | 2.4 | | | V | |

Notes:

- I_{CC} is dependent on output loading when the device output is selected. Specified $I_{CC}(\text{max.})$ is measured with the output open.
- I_{CC} is dependent upon the number of address transitions specified $I_{CC}(\text{max.})$ is measured with a maximum of one transition per address cycle in random Read/Write and EDO Fast Page Mode.
- Specified $V_{IL}(\text{min.})$ is steady state operation. During transitions $V_{IL}(\text{min.})$ may undershoot to -1V for a period not to exceed 15ns. All AC parameters are measured with $V_{IL}(\text{min.}) \geq V_{SS}$ and $V_{IH}(\text{max.}) \leq V_{CC}$.
- Specified $V_{IH}(\text{max.})$ is steady state operation. During transitions $V_{IH}(\text{max.})$ may overshoot to $V_{CC}+1\text{V}$ for a period not to exceed 15ns. All AC parameters are measured with $V_{IL}(\text{min.}) \geq V_{SS}$ and $V_{IH}(\text{max.}) \leq V_{CC}$.
- S-Version.

AC Characteristics
 $T_A = 0^{\circ}\text{C to } 70^{\circ}\text{C}, -20^{\circ}\text{C to } 85^{\circ}\text{C}$ $V_{CC} = 3.3\text{ V} \pm 0.3\text{V}$, $V_{IH}/V_{IL} = 3/0\text{ V}$, $V_{OH}/V_{OL} = 2/0.8\text{V}$

 An initial pause of 200 μs and 8 CAS-before-RAS or RAS-only refresh cycles are required after power-up.

| Parameter | Symbol | 40 | | 45 | | 50 | | 60 | | 70 | | Unit | Notes |
|--|-----------|------|------|------|------|------|------|------|------|------|------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Read or Write Cycle Time | t_{RC} | 70 | | 84 | | 84 | | 104 | | 124 | | ns | |
| Read Modify Write Cycle Time | t_{RWC} | 91 | | 116 | | 116 | | 140 | | 170 | | ns | |
| RAS Precharge Time | t_{RP} | 25 | | 30 | | 30 | | 40 | | 50 | | ns | |
| RAS Pulse Width | t_{RAS} | 40 | 10K | 50 | 10k | 50 | 10k | 60 | 10k | 70 | 10k | ns | |
| Access Time from RAS | t_{RAC} | | 40 | | 50 | | 50 | | 60 | | 70 | ns | 1,2,3 |
| Access Time from CAS | t_{CAC} | | 12 | | 13 | | 13 | | 15 | | 20 | ns | 1,5,7 |
| Access Time from Column Address | t_{AA} | | 20 | | 25 | | 25 | | 30 | | 35 | ns | 1,5,6 |
| CAS to Output Low-Z | t_{CLZ} | 3 | | 3 | | 3 | | 3 | | 3 | | ns | |
| CAS to Output High-Z | t_{CEZ} | 3 | 8 | 3 | 13 | 3 | 13 | 3 | 15 | 3 | 20 | ns | |
| RAS Hold Time | t_{RSH} | 12 | | 13 | | 13 | | 15 | | 20 | | ns | |
| CAS Hold Time | t_{CSH} | 34 | | 38 | | 38 | | 45 | | 50 | | ns | |
| CAS Pulse Width | t_{CAS} | 7 | 10k | 8 | 10k | 8 | 10k | 10 | 10k | 15 | 10k | ns | |
| RAS to CAS Delay Time | t_{RCD} | 18 | 28 | 20 | 37 | 20 | 37 | 20 | 45 | 20 | 50 | ns | |
| RAS to Column Address Delay Time | t_{RAD} | 13 | 20 | 15 | 25 | 15 | 25 | 15 | 30 | 15 | 35 | ns | 7 |
| CAS to RAS Precharge Time | t_{CRP} | 5 | | 5 | | 5 | | 5 | | 5 | | ns | |
| Row Address Set-Up Time | t_{ASR} | 0 | | 0 | | 0 | | 0 | | 0 | | ns | |
| Row Address Hold Time | t_{RAH} | 8 | | 10 | | 10 | | 10 | | 10 | | ns | |
| Column Address Set-Up Time | t_{ASC} | 0 | | 0 | | 0 | | 0 | | 0 | | ns | |
| Column Address Hold Time | t_{CAH} | 6 | | 8 | | 8 | | 10 | | 15 | | ns | |
| Column Address to RAS Lead Time | t_{RAL} | 20 | | 25 | | 25 | | 30 | | 35 | | ns | |
| Column Address Hold Time Referenced to RAS | t_{AR} | 34 | | 40 | | 40 | | 45 | | 50 | | ns | |
| Read Command Set-Up Time | t_{RCS} | 0 | | 0 | | 0 | | 0 | | 0 | | ns | |
| Read Command Hold Time Referenced to CAS | t_{RCH} | 0 | | 0 | | 0 | | 0 | | 0 | | ns | 4 |
| Read Command Hold Time Referenced to RAS | t_{RRH} | 0 | | 0 | | 0 | | 0 | | 0 | | ns | 4 |
| Write Command Set-Up Time | t_{WCS} | 0 | | 0 | | 0 | | 0 | | 0 | | ns | 8,9 |
| Write Command Hold Time | t_{WCH} | 6 | | 10 | | 10 | | 10 | | 15 | | ns | |
| Write Command Pulse Width | t_{WCP} | 6 | | 10 | | 10 | | 10 | | 15 | | ns | |
| Write Command to RAS Lead Time | t_{RWL} | 12 | | 13 | | 13 | | 15 | | 30 | | ns | |
| Write Command to CAS Lead Time | t_{CWL} | 8 | | 8 | | 8 | | 10 | | 15 | | ns | |

AC Characteristics

| Parameter | Symbol | 40 | | 45 | | 50 | | 60 | | 70 | | Unit | Notes |
|--|------------|------|------|------|------|------|------|------|------|------|------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Data Set-Up Time | t_{DS} | 0 | | | | 0 | | 0 | | 0 | | ns | 10 |
| Data Hold Time | t_{DH} | 7 | | | | 8 | | 10 | | 15 | | ns | 10 |
| Data Hold Time Referenced to \overline{RAS} | t_{DHR} | 36 | | | | 40 | | 45 | | 50 | | ns | |
| \overline{RAS} to \overline{WE} Delay Time | t_{RWD} | 54 | | | | 67 | | 79 | | 94 | | ns | |
| \overline{CAS} to \overline{WE} Delay Time | t_{CWD} | 24 | | | | 30 | | 34 | | 44 | | ns | |
| Column Address to \overline{WE} Delay Time | t_{AWD} | 32 | | | | 42 | | 49 | | 59 | | ns | |
| \overline{CAS} Precharge to \overline{WE} Delay | t_{CPWD} | 47 | | | | 47 | | 54 | | 64 | | ns | |
| \overline{RAS} to \overline{CAS} Precharge Time | t_{RPC} | 5 | | | | 5 | | 5 | | 5 | | ns | |
| \overline{CAS} precharge time (\overline{CAS} Before \overline{RAS} counter test cycle) | t_{CPT} | 20 | | | | 20 | | 20 | | 25 | | ns | |
| Access Time from \overline{CAS} Precharge | t_{CPA} | | 22 | | | | 28 | | 35 | | 40 | ns | |
| EDO Page Mode Cycle Time | t_{PC} | 18 | | | | 20 | | 25 | | 30 | | ns | |
| EDO Page Mode Read-Modify-Write Cycle Time | t_{PRWC} | 50 | | | | 47 | | 56 | | 71 | | ns | |
| \overline{CAS} Precharge Time (EDO Page Mode) | t_{CP} | 6 | | | | 8 | | 10 | | 10 | | ns | |
| \overline{RAS} Pulse Width (EDO Page Mode Only) | t_{RASP} | 40 | 100k | | | 50 | 100k | 60 | 100k | 70 | 100k | ns | |
| \overline{RAS} Hold Time from \overline{CAS} precharge | t_{RHCP} | 30 | | | | 30 | | 35 | | 40 | | ns | |
| Access Time from \overline{OE} | t_{OEA} | | 12 | | | | 13 | | 15 | | 20 | ns | |
| \overline{OE} to Data Delay Time | t_{OED} | 8 | | | | 13 | | 15 | | 20 | | ns | |
| \overline{OE} to Output Low-Z | t_{OLZ} | 3 | | | | 3 | | 3 | | 3 | | ns | |
| \overline{OE} to Output High-Z | t_{OEZ} | 3 | 8 | | | 3 | 13 | 3 | 15 | 3 | 20 | ns | |
| \overline{WE} to Data Delay | t_{WED} | 15 | | | | 15 | | 15 | | 20 | | ns | |
| \overline{OE} Command Hold Time | t_{OEH} | 7 | | | | 13 | | 15 | | 20 | | ns | |
| Data Output Hold after \overline{CAS} low | t_{DOH} | 3 | | | | 5 | | 5 | | 5 | | ns | |
| \overline{RAS} to Output High-Z | t_{REZ} | 3 | 8 | | | 3 | 13 | 3 | 15 | 3 | 20 | ns | |
| \overline{WE} to Output High-Z | t_{WEZ} | 3 | 10 | | | 3 | 13 | 3 | 15 | 3 | 20 | ns | |
| \overline{OE} to \overline{CAS} Hold Time | t_{OCH} | 5 | | | | 5 | | 5 | | 5 | | ns | |
| \overline{CAS} Hold Time to \overline{OE} | t_{CHO} | 5 | | | | 5 | | 5 | | 5 | | ns | |
| \overline{OE} Precharge Time | t_{OEP} | 5 | | | | 5 | | 5 | | 5 | | ns | |
| \overline{WE} Puts width (EDO mixed read write cycle) | t_{WPE} | 5 | | | | 5 | | 5 | | 5 | | ns | |
| \overline{CAS} Set-Up Time for \overline{CAS} -before- \overline{RAS} Cycle | t_{CSR} | 5 | | | | 5 | | 5 | | 5 | | ns | |

| Parameter | Symbol | 40 | | 45 | | 50 | | 60 | | 70 | | Unit | Notes |
|---|------------|------|------|------|------|------|------|------|------|------|------|---------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | | |
| CAS Hold Time for CAS-before-RAS Cycle | t_{CHR} | 8 | | | | 10 | | 10 | | 15 | | ns | |
| WE to RAS precharge time (CAS Before RAS refresh) | t_{WRP} | 10 | | | | 10 | | 10 | | 10 | | ns | |
| WE to RAS hold time (CAS Before RAS refresh) | t_{WRH} | 10 | | | | 10 | | 10 | | 10 | | ns | |
| Transition Time | t_T | 2 | 50 | | | 2 | 50 | 2 | 50 | 2 | 50 | ns | 11 |
| Refresh Period (2,048 cycles) | t_{REF} | | 32 | | | | 32 | | 32 | | 32 | ms | |
| Refresh Period (S-Version) | t_{REF} | | 128 | | | | 128 | | 128 | | 128 | ms | |
| RAS Pulse Width (CAS Before RAS Self refresh) | t_{RASS} | 100 | | | | 100 | | 100 | | 100 | | μ s | |
| RAS precharge Time (CAS Before RAS Self refresh) | t_{RPS} | 70 | | | | 90 | | 110 | | 130 | | ns | |
| CAS Hold Time (CAS Before RAS Self refresh) | t_{CHS} | -50 | | | | -50 | | -50 | | -50 | | ns | |

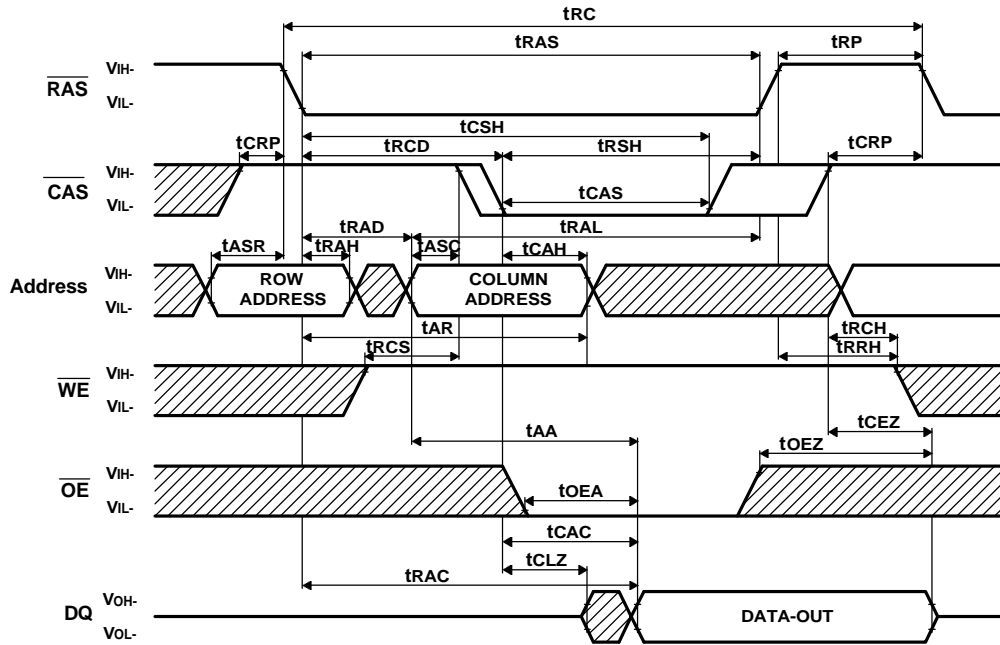
TEST MODE CYCLE

| Parameter | Symbol | 40 | | 50 | | 60 | | 70 | | Unit | Notes |
|--|------------|------|------|------|------|------|------|------|------|------|---------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Random read or write cycle time | t_{RC} | 89 | | 89 | | 109 | | 129 | | ns | |
| Read-modify-write cycle time | t_{RWC} | 121 | | 121 | | 145 | | 175 | | ns | |
| Access time from \overline{RAS} | t_{RAC} | | 55 | | 55 | | 65 | | 75 | ns | 1,2,3,7 |
| Access time from \overline{CAS} | t_{CAC} | | 18 | | 18 | | 20 | | 25 | ns | 1,3,7 |
| Access time from column address | t_{AA} | | 30 | | 30 | | 35 | | 40 | ns | 1,2,7 |
| \overline{RAS} pulse width | t_{RAS} | 55 | 10k | 55 | 10k | 65 | 10k | 75 | 10k | ns | |
| \overline{CAS} pulse width | t_{CAS} | 13 | 10k | 13 | 10k | 15 | 10k | 20 | 10k | ns | |
| \overline{RAS} hold time | t_{RSH} | 18 | | 18 | | 20 | | 25 | | ns | |
| \overline{CAS} hold time | t_{CSH} | 43 | | 43 | | 50 | | 55 | | ns | |
| Column address to \overline{RAS} lead time | t_{RAL} | 30 | | 30 | | 35 | | 40 | | ns | |
| \overline{CAS} to \overline{WE} delay time | t_{CWD} | 35 | | 35 | | 39 | | 49 | | ns | 8 |
| \overline{RAS} to \overline{WE} delay time | t_{RWD} | 72 | | 72 | | 84 | | 99 | | ns | 8 |
| Column address to \overline{WE} delay time | t_{AWD} | 47 | | 47 | | 54 | | 64 | | ns | 8 |
| \overline{CAS} Precharge to \overline{WE} delay time | t_{CPWD} | 52 | | 52 | | 59 | | 69 | | ns | 8 |
| EDO Page Mode cycle time | t_{PC} | 25 | | 25 | | 30 | | 35 | | ns | |
| EDO page mode read-modify-write cycle time | t_{PRWC} | 53 | | 53 | | 61 | | 76 | | ns | |
| \overline{RAS} Pulse width (EDO page cycle) | t_{RASP} | 55 | 100k | 55 | 100k | 65 | 100k | 75 | 100k | ns | |
| Access time form \overline{CAS} precharge | t_{CPA} | | 33 | | 33 | | 40 | | 45 | ns | 1 |
| \overline{OE} access time | t_{OEA} | | 18 | | 18 | | 20 | | 25 | ns | |
| \overline{OE} to data delay | t_{OED} | 18 | | 18 | | 20 | | 25 | | ns | |
| \overline{OE} command hold time | t_{OEHL} | 18 | | 18 | | 20 | | 25 | | ns | |
| Write command set-up time (Test mode in) | t_{WTS} | 10 | | 10 | | 10 | | 10 | | ns | |
| Write command hold time (Test mode in) | t_{WTH} | 10 | | 10 | | 10 | | 10 | | ns | |

Notes:

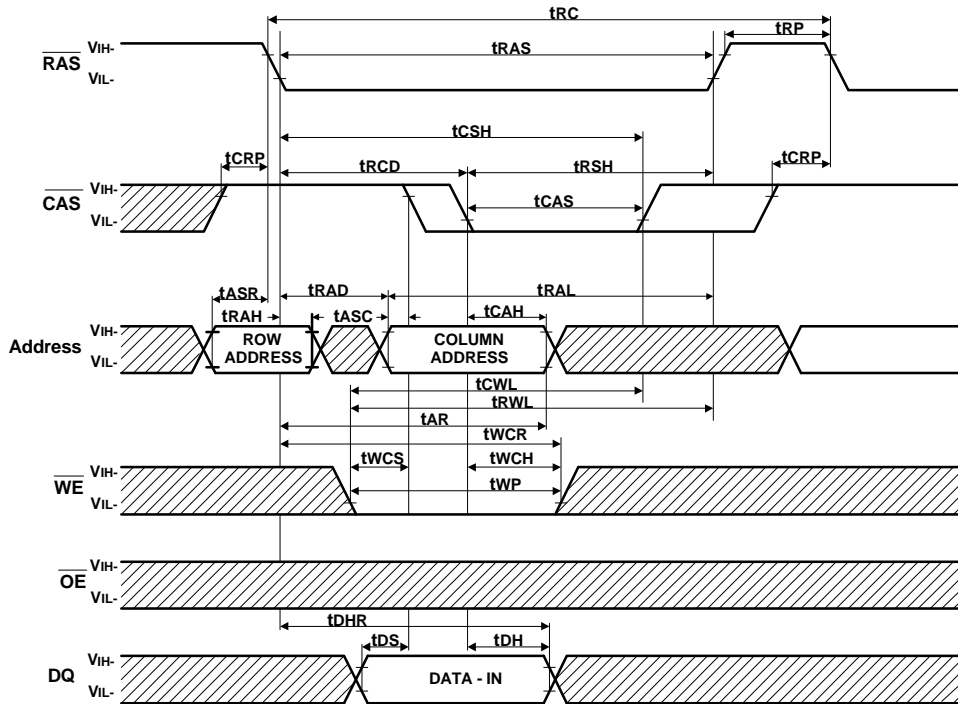
1. Measure with a load equivalent to one TTL input and 100 pF.
2. Assumes that $t_{RCD} \leq t_{RCD}(\text{max.})$. If t_{RCD} is greater than $t_{RCD}(\text{max.})$, access time will be t_{CAC} dominant.
3. Assumes that $t_{RAD} \leq t_{RAD}(\text{max.})$. If t_{RAD} is greater than $t_{RAD}(\text{max.})$, access time will be controlled by t_{AA} .
4. Either t_{RRH} or t_{RCH} must be satisfied for a Read Cycle.
5. Access time is determined by the longest of t_{AA} , t_{CAC} and t_{CPA} .
6. Assumes that $t_{RAD} \geq t_{RAD}(\text{max.})$.
7. Assumes that $t_{RCD} \geq t_{RCD}(\text{max.})$.
8. t_{WCS} , t_{RWD} , t_{AWD} and t_{CWD} are not restrictive operating parameters.
9. $t_{WCS}(\text{min.})$ must be satisfied in an Early Write Cycle.
10. t_{DS} and t_{DH} are referenced to the latter occurrence of \overline{CAS} or \overline{WE} .
11. t_T is measured between $V_{IH}(\text{min.})$ and $V_{IL}(\text{max.})$. AC-measurements assume $t_T = 2 \text{ ns}$.

Read CYCLE



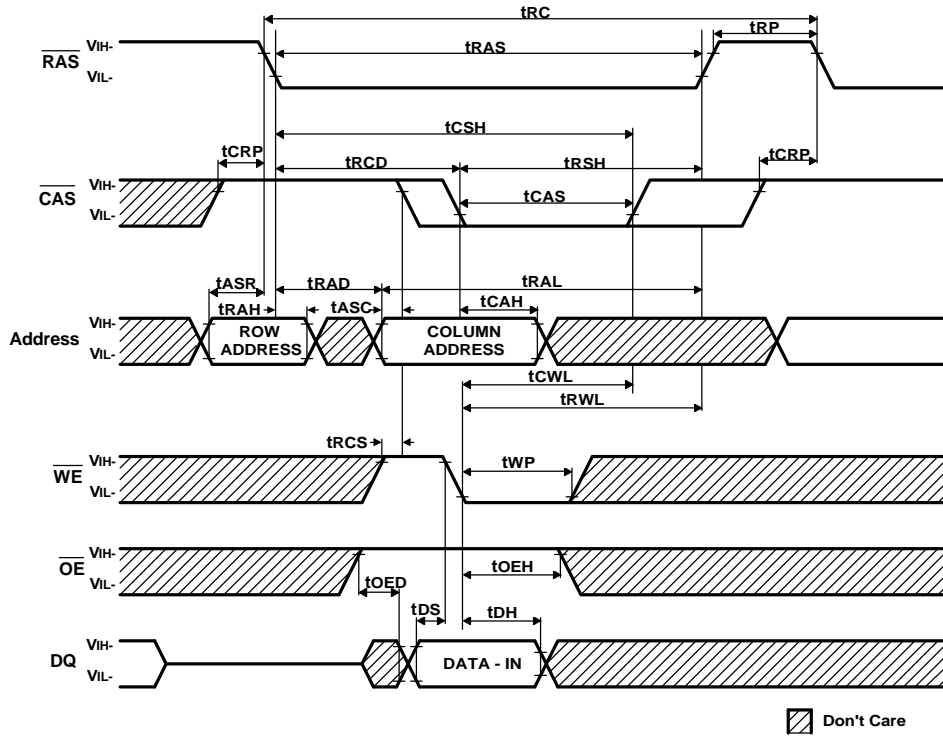
Don't Care

Early Write Cycle NOTE : D_{OUT} = OPEN

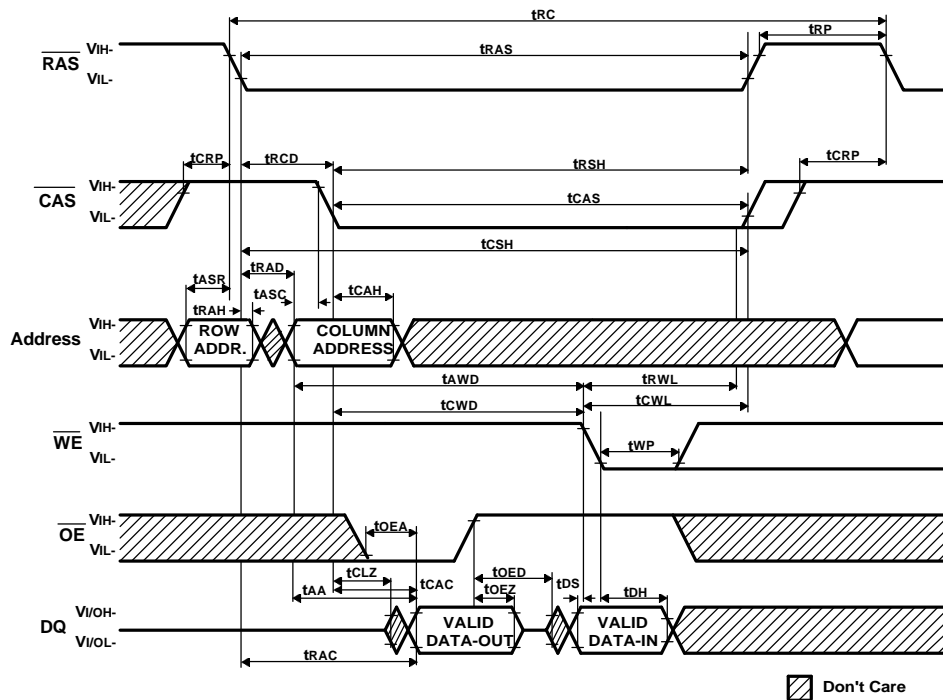


Don't Care

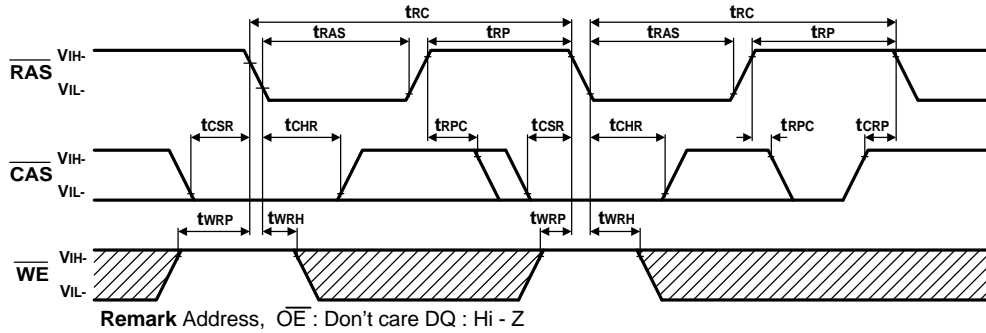
OE Controlled Write Cycle NOTE : D_{OUT} = OPEN



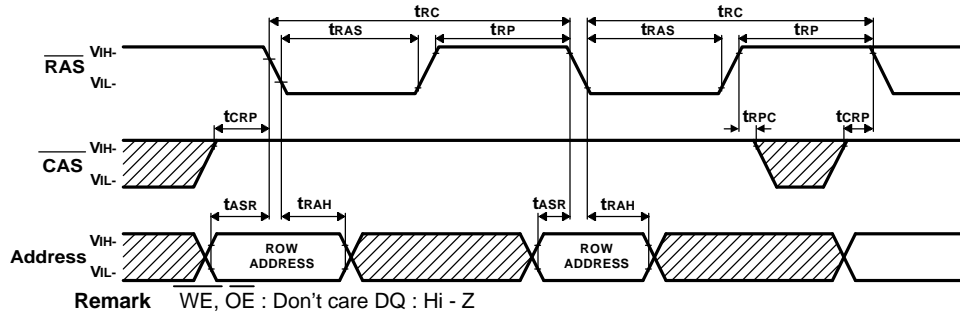
Read - Modify - Write Cycle



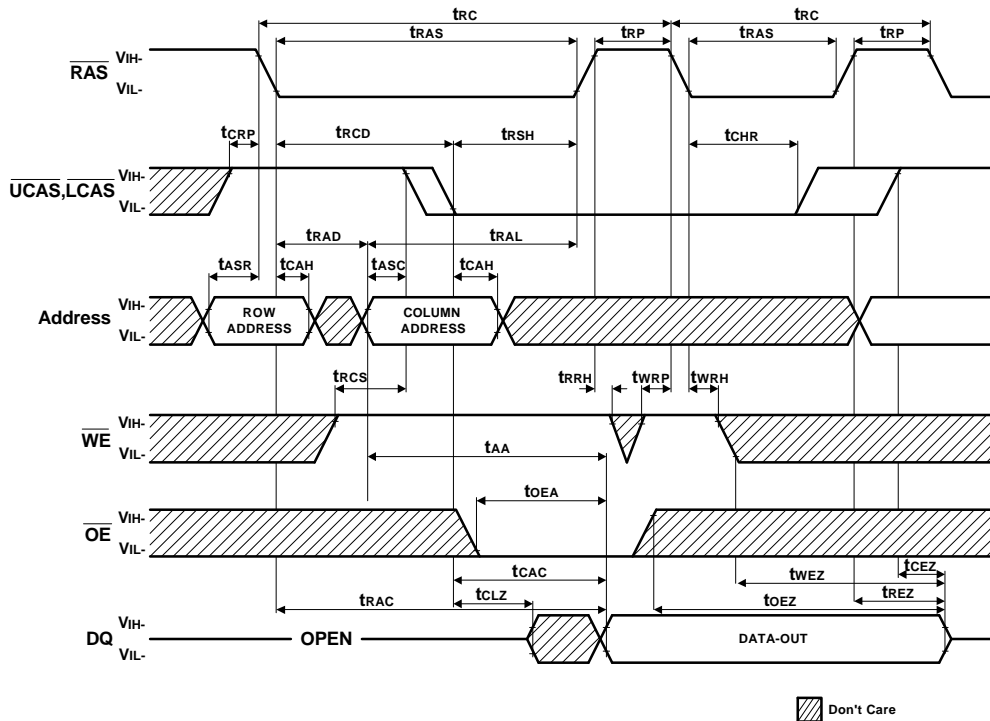
CAS - Before - RAS Refresh Cycle



RAS-Only Refresh Cycle

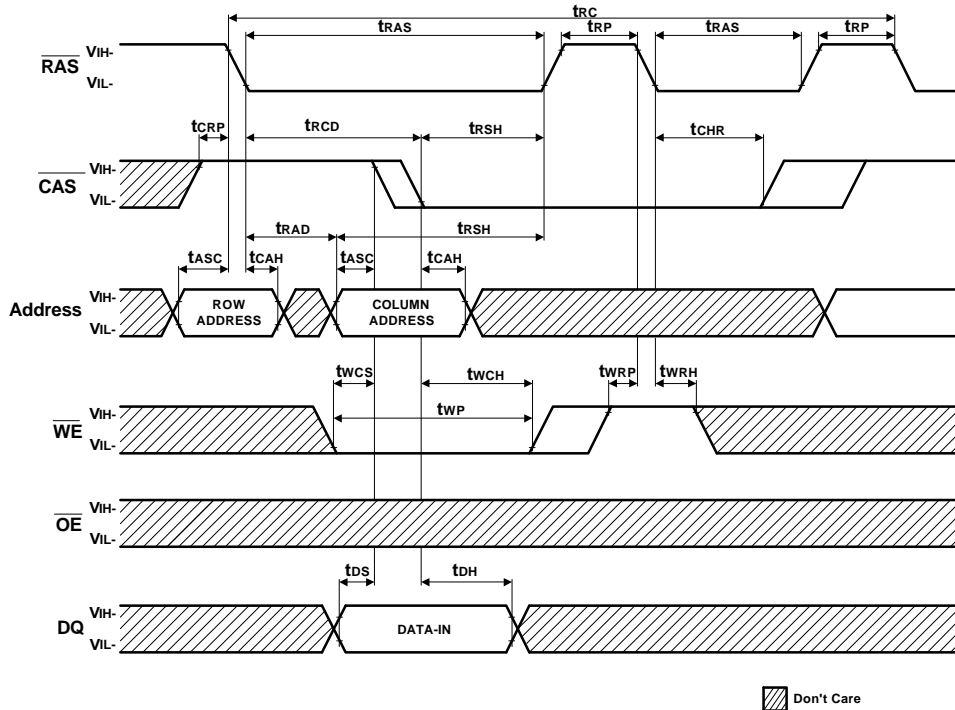


Hidden Refresh Cycle (Read)

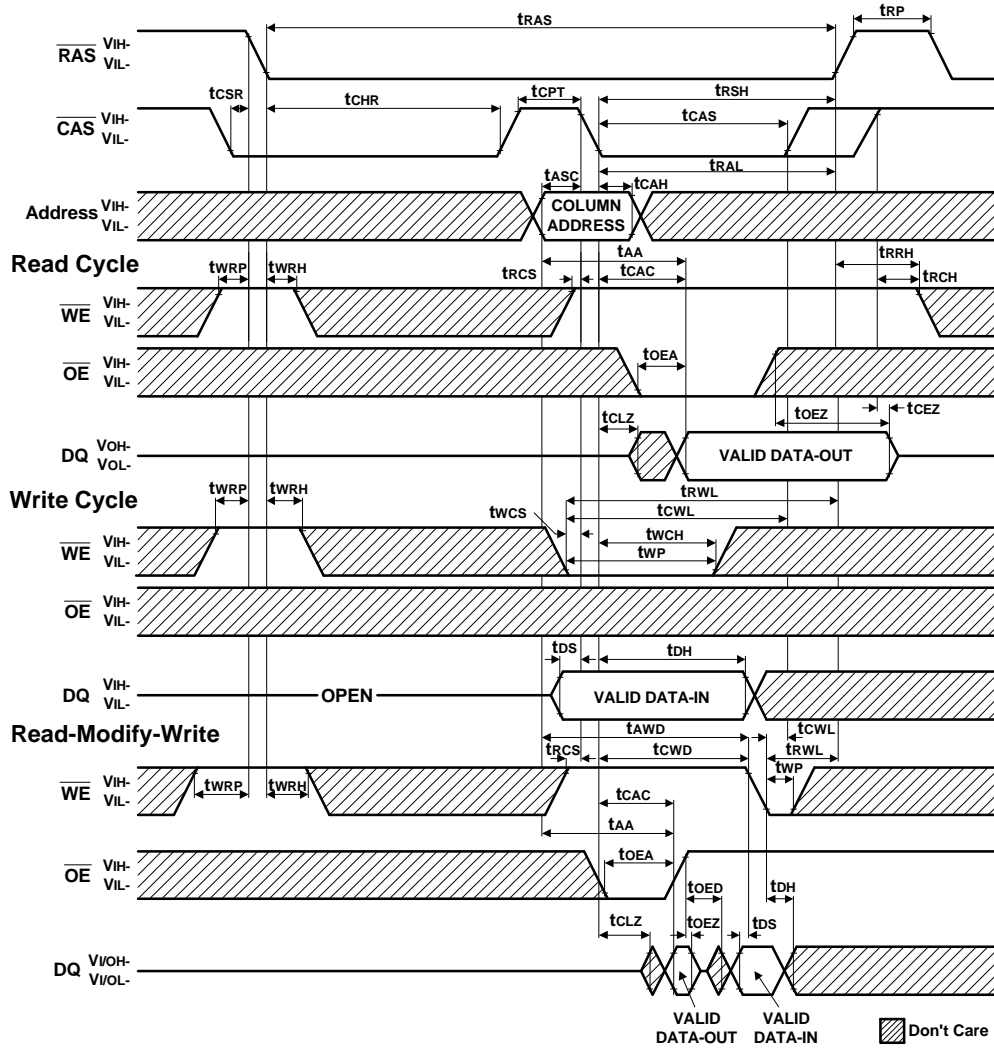


Don't Care

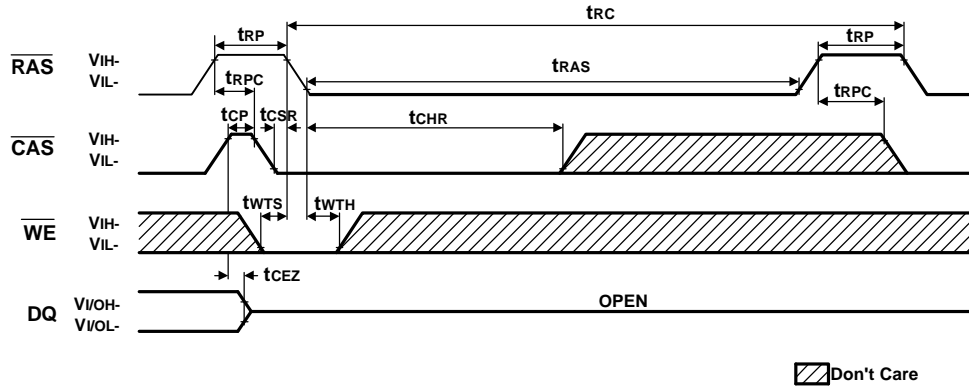
Hidden Refresh Cycle (Write) NOTE : D_{OUT} = OPEN



CAS-Before RAS Refresh Counter Test Cycle



TEST MODE IN CYCLE



Test Mode

By using the test mode, the test time can be reduced. The reason for this is that, the memory emulates the x 16-bit organization during test mode. Don't care about the input levels of the $\overline{\text{CAS}}$ input A0, A1 .

(1) Setting the mode

Executing the test mode cycle ($\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle) sets the test mode.

(2) Write / read operation

When either a "0" or a "1" is written to the input pin in test mode, this data is written to 16 bits of memory cell.

Next, when the data is read from the output pin at the same address, the cell be checked.

Output = "1" Normal write (all memory cells)
Output = "0" Abnormal write

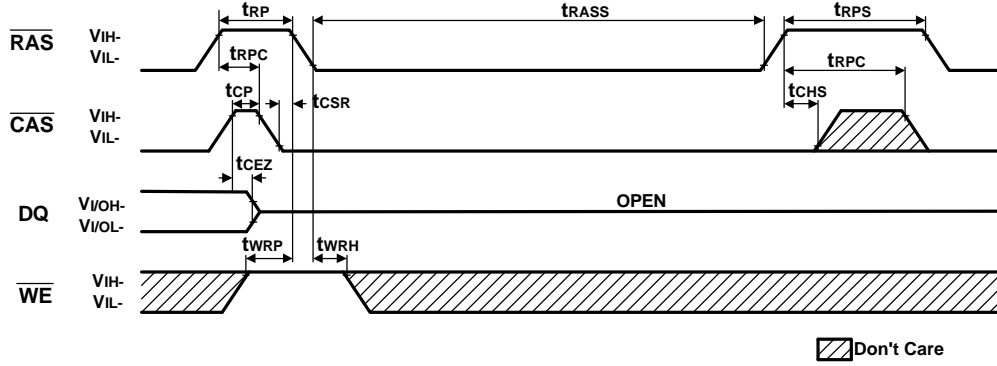
(3) Refresh

Refresh in the test mode must be performed with the $\overline{\text{RAS}}$ / $\overline{\text{CAS}}$ cycle or with the $\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle. The $\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle use the same counter as the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh's internal counter.

(4) Mode Cancellation

The test mode is cancelled by executing one cycle of $\overline{\text{RAS}}$ only refresh cycle or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle.

CAS-BEFORE-RAS SELF REFRESH CYCLE



NOTE : \overline{OE} , Address = Don't Care

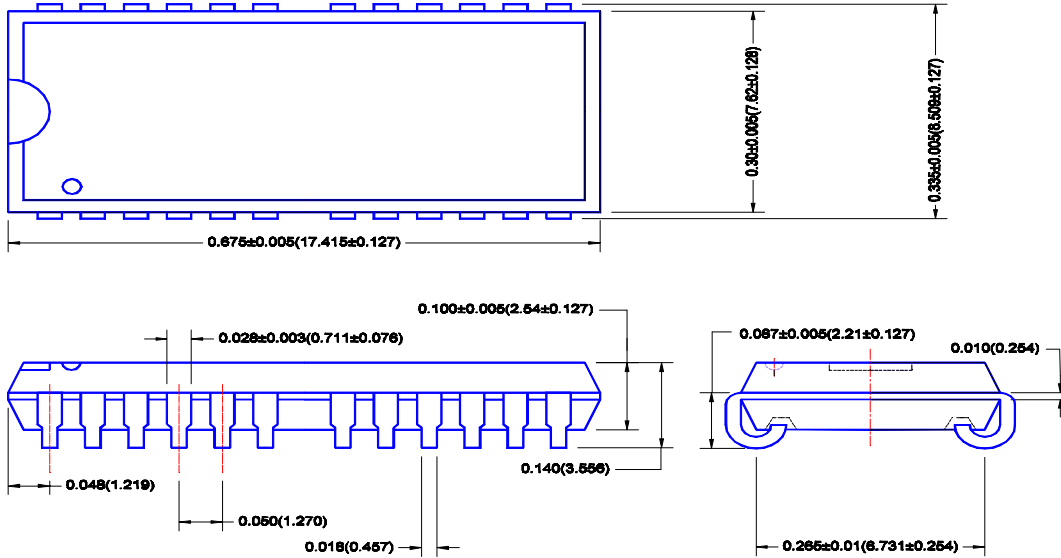
Ordering Information

| <i>Part Number</i> | <i>SPEED</i> | <i>POWER</i> | <i>FEATURE</i> | <i>TEMPERATURE</i> | <i>PACKAGE</i> |
|--------------------|--------------|--------------|----------------|--------------------|-----------------------|
| GLT4160L04-40J3 | 40ns | Normal | EDO | Commercial | SOJ 300mil 26(24)L |
| GLT4160L04-50J3 | 50ns | Normal | EDO | Commercial | SOJ 300mil 26(24)L |
| GLT4160L04-60J3 | 60ns | Normal | EDO | Commercial | SOJ 300mil 26(24)L |
| GLT4160L04-70J3 | 70ns | Normal | EDO | Commercial | SOJ 300mil 26(24)L |
| GLT4160L04E-40J3 | 40ns | Normal | EDO | Extended | SOJ 300mil 26(24)L |
| GLT4160L04E-50J3 | 50ns | Normal | EDO | Extended | SOJ 300mil 26(24)L |
| GLT4160L04E-60J3 | 60ns | Normal | EDO | Extended | SOJ 300mil 26(24)L |
| GLT4160L04E-70J3 | 70ns | Normal | EDO | Extended | SOJ 300mil 26(24)L |
| GLT4160L04S-40J3 | 40ns | Self Refresh | EDO | Commercial | SOJ 300mil 26(24)L |
| GLT4160L04S-50J3 | 50ns | Self Refresh | EDO | Commercial | SOJ 300mil 26(24)L |
| GLT4160L04S-60J3 | 60ns | Self Refresh | EDO | Commercial | SOJ 300mil 26(24)L |
| GLT4160L04S-70J3 | 70ns | Self Refresh | EDO | Commercial | SOJ 300mil 26(24)L |
| GLT4160L04SE-40J3 | 40ns | Self Refresh | EDO | Extended | SOJ 300mil 26(24)L |
| GLT4160L04SE-50J3 | 50ns | Self Refresh | EDO | Extended | SOJ 300mil 26(24)L |
| GLT4160L04SE-60J3 | 60ns | Self Refresh | EDO | Extended | SOJ 300mil 26(24)L |
| GLT4160L04SE-70J3 | 70ns | Self Refresh | EDO | Extended | SOJ 300mil 26(24)L |
| GLT4160L04P-40J3 | 40ns | Normal | EDO | Commercial | SOJ 300mil 26(24)L |
| GLT4160L04P-50J3 | 50ns | Normal | EDO | Commercial | SOJ 300mil 26(24)L |
| GLT4160L04P-60J3 | 60ns | Normal | EDO | Commercial | SOJ 300mil 26(24)L |
| GLT4160L04P-70J3 | 70ns | Normal | EDO | Commercial | SOJ 300mil 26(24)L |
| GLT4160L04-40TC | 40ns | Normal | EDO | Commercial | TSOPII 300mil 26(24)L |
| GLT4160L04-50TC | 50ns | Normal | EDO | Commercial | TSOPII 300mil 26(24)L |
| GLT4160L04-60TC | 60ns | Normal | EDO | Commercial | TSOPII 300mil 26(24)L |
| GLT4160L04-70TC | 70ns | Normal | EDO | Commercial | TSOPII 300mil 26(24)L |
| GLT4160L04E-40TC | 40ns | Normal | EDO | Extended | TSOPII 300mil 26(24)L |
| GLT4160L04E-50TC | 50ns | Normal | EDO | Extended | TSOPII 300mil 26(24)L |
| GLT4160L04E-60TC | 60ns | Normal | EDO | Extended | TSOPII 300mil 26(24)L |
| GLT4160L04E-70TC | 70ns | Normal | EDO | Extended | TSOPII 300mil 26(24)L |
| GLT4160L04S-40TC | 40ns | Self Refresh | EDO | Commercial | TSOPII 300mil 26(24)L |
| GLT4160L04S-50TC | 50ns | Self Refresh | EDO | Commercial | TSOPII 300mil 26(24)L |
| GLT4160L04S-60TC | 60ns | Self Refresh | EDO | Commercial | TSOPII 300mil 26(24)L |
| GLT4160L04S-70TC | 70ns | Self Refresh | EDO | Commercial | TSOPII 300mil 26(24)L |
| GLT4160L04SE-40TC | 40ns | Self Refresh | EDO | Extended | TSOPII 300mil 26(24)L |
| GLT4160L04SE-50TC | 50ns | Self Refresh | EDO | Extended | TSOPII 300mil 26(24)L |
| GLT4160L04SE-60TC | 60ns | Self Refresh | EDO | Extended | TSOPII 300mil 26(24)L |
| GLT4160L04SE-70TC | 70ns | Self Refresh | EDO | Extended | TSOPII 300mil 26(24)L |
| GLT4160L04P-40TC | 40ns | Normal | EDO | Commercial | TSOPII 300mil 26(24)L |
| GLT4160L04P-50TC | 50ns | Normal | EDO | Commercial | TSOPII 300mil 26(24)L |
| GLT4160L04P-60TC | 60ns | Normal | EDO | Commercial | TSOPII 300mil 26(24)L |
| GLT4160L04P-70TC | 70ns | Normal | EDO | Commercial | TSOPII 300mil 26(24)L |

Package Information

300mil 24/26 Lead Thin Small Outline Package SOJ

Unit : Inch(mm)



300mil 24/26 Lead Thin Small Outline Package (TSOP) TYPE II

Unit : Inch(mm)

