MicroConverter, Dual 10-channel 24-Bit ADCs with Embedded 62kB FLASH MCU

Preliminary Technical Data ADuC845

FEATURES

High Resolution Sigma-Delta ADCs

- Two Independent ADCs (24-Bit Resolution)
- Up to 10 ADC input channels
- 24-Bit No Missing Codes, Primary ADC
- 20-Bit rms (17.4 Bit p-p) Effective Resolution @ 60 Hz
- Offset Drift 10 nV/°C, Gain Drift 0.5 ppm/°C (Chop enabled)

Memory

- 62 Kbytes On-Chip Flash/EE Program Memory
- 4 Kbytes On-Chip Flash/EE Data Memory
- Flash/EE, 100 Year Retention, 100 Kcycles Endurance
- 3 Levels of Flash/EE Program Memory Security
- In-Circuit Serial Download (No External Hardware)
- High Speed User Download (5 Seconds)
- 2304 Bytes On-Chip Data RAM

8051-Based Core

- 8051 Compatible Instruction Set
- High Performance Single Cycle Core
- 32 kHz External Crystal
- On-Chip Programmable PLL (12.58 MHz Max)
- 3 □ 16-Bit Timer/Counter
- 26 Programmable I/O Lines
- 11 Interrupt Sources, Two Priority Levels
- Dual Data Pointer, Extended 11-Bit Stack Pointer

On-Chip Peripherals

- Internal Power on Reset Circuit
- 12-Bit Voltage Output DAC
- Dual 16-Bit S-D DACs/PWMs
- On-Chip Temperature Sensor
- Dual Excitation Current Sources
- Time Interval Counter (Wakeup/RTC Timer)
- UART, SPI®, and I²C® Serial I/O
- High Speed Baud Rate Generator (incl 115,200)
- Watchdog Timer (WDT)
- Power Supply Monitor (PSM)

Power

- Normal: 2.3mA Max @ 3.6 V (Core CLK = 1.57 MHz)
- Power-Down: 20uA Max with Wakeup Timer Running
- Specified for 3 V and 5 V Operation

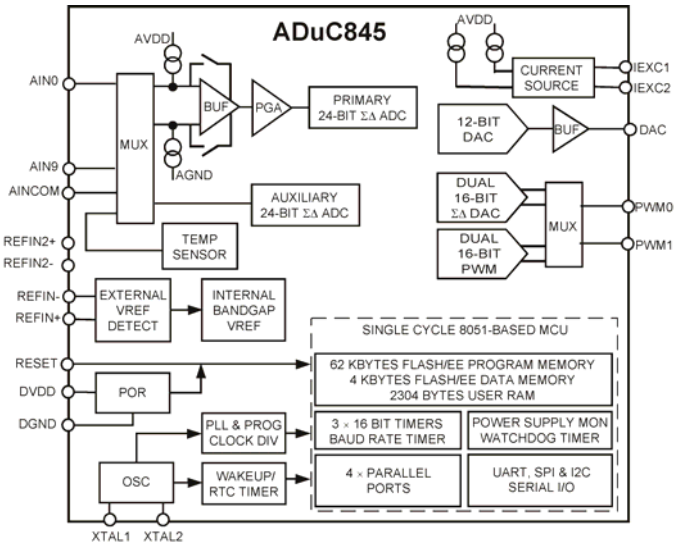
Package and Temperature Range

- 52-Lead MQFP (14 mm x 14 mm), –40°C to +125°C
- 56-Lead CSP (8 mm x 8 mm), –40°C to +85°C

APPLICATIONS

- Multi channel Sensor monitoring
- Industrial/Environmental Instrumentation
- WeighScales
- Portable Instrumentation, Battery Powered Systems
- 4-20mA Transmitters
- Data Logging
- Precision System Monitoring

FUNCTIONAL BLOCK DIAGRAM



REV. PrC

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SPECIFICATIONS[1]

(AVDD = 2.7 V to 3.6 V or 4.75 V to 5.25 V, DVDD = 2.85 V to 3.6 V or 4.75 V to 5.25 V, REFIN(+) = 2.5 V, REFIN(–) = AGND; AGND = DGND = 0 V; XTAL1/XTAL2 = 32.768 kHz Crystal; all specifications T_{MIN} to T_{MAX} unless otherwise noted.). Input Buffer On for Primary ADC unless otherwise noted.

PARAMETER	MIN	TYP	MAX	UNITS	CONDITION
PRIMARY ADC[1]					
Conversion Rate	5.4	19.79	105	Hz	Chop On (ADCMODE.3 = 0)
	16.06	59.36	1365	Hz	Chop Off (ADCMODE.3 = 1)
No Missing Codes[2]	24			Bits	19.79Hz Update Rate
	24			Bits	59.36Hz Update Rate
Resolution					
		13.5		Bits Pk-Pk	Range = ± 20mV, 20Hz Update Rate, Chop On
		13		Bits Pk-Pk	Range = ± 20mV, 59Hz Update Rate, Chop Off
		18.5		Bits Pk-Pk	Range = ± 2.56V, 20Hz Update Rate, Chop On
		17.4		Bits Pk-Pk	Range = ± 2.56V, 59.4Hz Update Rate, Chop Off
Output Noise	See Tables V, VI VII & VIII in ADC Description				Output Noise varies with selected Update Rates, Gain Range and Chop status.
Integral Non Linearity		±2	± 15	ppm of FSR	1 LSB_{16}
Offset Error[3]		± 3		µV	Chop On (ADCMODE.3=0)
		See tables VII & VIII			Chop Off (ADCMODE.3=1). Offset Error is in the order of the noise for the programmed gain and update rate following a calibration.
Offset Error Drift vs. Temp		± 10		nV/°C	Chop On (ADCMODE.3=0)
		±200		nV/°C	Chop Off (ADCMODE.3=1)
Full-Scale Error[4]		± 10		µV	
Gain Error Drift vs. Temp[5]		± 0.5		ppm/°C	
PRIMARY ADC ANALOG INPUTS					
Differential Input Voltage Ranges[9, 10]					GAIN = 1 to 128
Bipolar Mode (ADC0CON1.5 = 0)		± 1.024 x V_{REF}/GAIN		V	V_{REF} = REFIN(+) - REFIN(-) or REFIN2(+) – REFIN2(-) (or Int 1.25V Ref)
Unipolar Mode (ADC0CON1.5 = 1)		0 → 1.024 x Vref/GAIN		V	V_{REF} = REFIN(+) - REFIN(-) or REFIN2(+) – REFIN2(-) (or Int 1.25V Ref)
ADC Range Matching		± 2		µV	AIN=18mV, Chop=On, Buffer=On.
Common Mode DC Rejection					
On AIN	95	100		dBs	@DC, AIN=7.8mV, Range=± 20mV
On AIN		113		dBs	@DC, AIN=1V, Range=± 2.56V
Common Mode 50/60Hz Rejection					20Hz Update Rate
On AIN	95			dBs	50/60Hz ± 1Hz, AIN=7.8mV, Range=± 20mV
On AIN	90			dBs	50/60Hz ± 1Hz, AIN=1V, Range=± 2.56V
					59Hz Update Rate
On AIN	95			dBs	50/60Hz ± 1Hz, AIN=7.8mV, Range=± 20mV
On AIN	90			dBs	50/60Hz ± 1Hz, AIN=1V, Range=± 2.56V
Normal Mode 50/60 Hz Rejection					50/60Hz ± 1Hz
On AIN	60			dBs	20Hz Update Rate, Chop On
On AIN	60			dBs	59Hz Update Rate, Chop Off
Analog Input Current[2]			± 1	nA	T_{MAX} = 85°C, Buffer On
			± 5	nA	T_{MAX} = 125°C, Buffer On
Analog Input Current Drift		± 5		pA/°C	T_{MAX} = 85°C, Buffer On
		± 15		pA/°C	T_{MAX} = 125°C, Buffer On
Analog Input Current		± 125		nA/V	± 2.56V Range, Buffer Bypassed
Analog Input Current Drift		± 2		pA/V/°C	Buffer bypassed
Absolute AIN Voltage Limits[2]	A_{GND} + 0.1		AV_{DD} – 0.1	V	Ain1-Ain10 and AINCON with Buffer ON (ADC0CON1.6 = 0 & ADC0CON1.7 = 0)
Absolute AIN Voltage Limits	A_{GND} - 0.03		AV_{DD} + 0.03	V	Ain1-Ain10 and AINCON with Buffer Bypassed (ADC0CON1.6=0, ADC0CON1.7=1)

EXTERNAL REFERENCE INPUTS					
REFIN(+) to REFIN(-) Voltage		2.5		V	REFIN refers to both REFIN and REFIN2.
REFIN(+) to REFIN(–) Range[2]	1		AV_{DD}	V	REFIN refers to both REFIN and REFIN2.
Average Reference Input Current		+/-1		μA/V	Both ADCs Enabled
Average Reference Input Current Drift		+/- 0.1		nA/V/°C	
'NOXREF' Trigger Voltage	0.3		0.65	V	NOXREF (ADCSTAT.4) bit active if Vref<0.3V, and Inactive if Vref>0.65V
Common Mode Rejection					
DC Rejection		125		dB	@DC, AIN=1V, Range=± 2.56V
50/60Hz Rejection[2]	90			dB	50/60Hz ± 1Hz, AIN=1V, Range=± 2.56V, SF=82 REJ60 = 1 (ADCMODE.6 = 1)
Normal Mode Rejection					
50/60 Hz Rejection[2]	60			dB	50/60Hz ± 1Hz, AIN=1V, Range=± 2.56V, SF=82 REJ60 = 1 (ADCMODE.6 = 1)
AUXILIARY ADC					
Conversion Rate	5.4	19.79	105	Hz	Chop On
	16.06	59.36	1365	Hz	Chop Off
No Missing Codes[2]	24			Bits	19.79Hz Update Rate, Chop On
	24			Bits	59.36Hz Update Rate, Chop Off
Resolution					
		16		Bits Pk-Pk	Range = ± 2.56V, 19.79Hz Update Rate, Chop On
		16		Bits Pk-Pk	Range = ± 2.56V, 59.36Hz Update Rate, Chop Off
Output Noise		See Table IX Auxiliary ADC			Output Noise varies with selected Update Rates Output Noise will typically degrade from Chop Enabled figures by 1LSB if CHOP is disabled.
Integral Non Linearity			± 15	ppm of FSR	1 LSB_{16}
Offset Error[3]		-2		LSB	Chop on
		See tables **XXXXXXXXXXXXXXX**			Offset error is in the order of the noise and dependent on the 16-bit calibration for the update rate chosen.
Offset Error Drift		1		μV /°C	Chop On
		20		μV /°C	Chop Off
Fullscale Error[4]		-2.5		LSBs	
Gain Error Drift[5]		± 0.5		ppm/°C	
Normal Mode 50/60 Hz Rejection					50/60Hz ± 1Hz
On AIN	60			dB	19.79Hz Update Rate, Chop On
	60			dB	59.36Hz Update Rate, Chop Off
On REFIN	60			dB	19.79Hz Update Rate, Chop On
	60			dB	59.36Hz Update Rate, Chop Off
AUXILIARY ADC ANALOG INPUTS					
Differential Input Voltage Ranges[9, 10]					REFIN (REFIN2 is not available to Aux ADC)
Bipolar Mode (ADC1CON.5)		± Vref		V	REFIN=REFIN(+)-REFIN(-) (or Int 1.25V Ref)
Unipolar Mode (ADC1CON.5)		0 → Vref		V	REFIN=REFIN(+)-REFIN(-) (or Int 1.25V Ref)
Average Analog Input Current		125		nA/V	
Analog Input Current Drift		± 2		pA/V/°C	
Analog Input Current		± 125		nA/V	± 2.56V Range
Analog Input Current Drift		± 2		pA/V/°C	
Absolute AIN/AINCOM Voltage Limits[2,11]	A_{GND}-0.03		V_{DD}+0.03	V	

PARAMETER	MIN	TYP	MAX	UNITS	CONDITION
ADC SYSTEM CALIBRATION					
Full Scale Calibration Limit			+1.05 x FS	V	
Zero Scale Calibration Limit	-1.05 x FS			V	
Input Span	0.8 x FS		2.1 x FS	V	
DAC					
Voltage Range		0 → V_{REF}		V	DACCON.2 = 0
		0 → AV_{DD}		V	DACCON.2 = 1
Resistive Load		10		kΩ	From DAC Output to AGND
Capacitive Load		100		pF	From DAC Output to AGND
Output Impedance		0.5		Ω	
I_{SINK}		50		µA	
DC Specifications[7]					
Resolution	12				
Relative Accuracy		± 3		LSBs	
Differential NonLinearity			-1	Bit	Guaranteed 12-Bit Monotonic
Offset Error			± 50	mV	
Gain Error[8]			± 1	%	AV_{DD} Range
		± 1		%	V_{REF} Range
AC Specifications[2,7]					
Voltage Output Settling Time		15		us	Setling time to 1LSB of final value
Digital to Analog Glitch Energy		10		nVs	1 LSB change at major carry
INT REFERENCE					CHOP ENABLED
ADC Reference					
Reference Voltage	1.237	1.25	1.2625	V	initial tolerance @ 25°C, VDD=5V
Power Supply Rejection		45		dBs	
Reference Tempco		100		ppm/°C	
DAC Reference					
Reference Voltage	2.475	2.5	1.525	V	initial tolerance @ 25°C, VDD=5V
Power Supply Rejection		50		dBs	
Reference Tempco		± 100		ppm/°C	
TEMPERATURE SENSOR					(ADC RATE TBD)
Accuracy		+/- 2		°C	
Thermal Impedance		90		°C/W	MQFP Package
		52		°C/W	CSP Package
TRANSDUCER BURNOUT CURRENT SOURCES					
AIN+ Current		-100		nA	AIN+ is the selected positive input (Ain4 or Ain6 only) to the primary ADC
AIN- Current		100		nA	AIN- is the selected negative input (Ain5 or Ain7 only) to the primary ADC
Initial Tolerance at 25°C		+/- 10		%	
Drift		0.03		%/°C	
EXCITATION CURRENT SOURCES					
Output Current		-200		µA	Available from each Current Source
Initial Tolerance at 25°C		+/-10		%	
Drift		200		ppm/°C	
Initial Current Matching at 25°C		+/-1		%	Matching between both Current Sources
Drift Matching		20		ppm/°C	
Line Regulation (AV_{DD})		1		µA/V	AV_{DD}=5V +/- 5%
Load Regulation			0.1	V	
Output Compliance	A_{GND}		AV_{DD}-0.6	V	

PARAMETER	MIN	TYP	MAX	UNITS	CONDITION
POWER SUPPLY MONITOR (PSM)					
AV_{DD} Trip Point Selection Range	2.63		4.63	V	Four Trip Points selectable in this range
AV_{DD} Trip Point Accuracy			+/- 3.0	%	T_{MAX} = 85°C
AV_{DD} Trip Point Accuracy			+/- 3.0	%	T_{MAX} = 125°C
DV_{DD} Trip Point Selection Range	2.63		4.63	V	Four Trip Points selectable in this range
DV_{DD} Trip Point Accuracy			+/- 3.0	%	T_{MAX} = 85°C
DV_{DD} Trip Point Accuracy			+/- 3.0	%	T_{MAX} = 125°C
CRYSTAL OSCILLATOR (XTAL 1AND XTAL2)					
Logic Inputs, XTAL1 Only[2]					
V_{INL}, Input Low Voltage			0.8	V	DV_{DD} = 5V
			0.4	V	DV_{DD} = 3V
V_{INH}, Input Low Voltage	3.5			V	DV_{DD} = 5V
	2.5			V	DV_{DD} = 3V
XTAL1 Input Capacitance		18		pF	
XTAL2 Output Capacitance		18		pF	
LOGIC INPUTS					
All Inputs except SCLOCK, RESET and XTAL1[2]					
V_{INL}, Input Low Voltage			0.8	V	DV_{DD} = 5V
			0.4	V	DV_{DD} = 3V
V_{INH}, Input Low Voltage	2.0			V	
SCLOCK and RESET Only (Schmidt Triggered Inputs)[2]					
V_{T+}	1.3		3.0	V	DV_{DD} = 5V
	0.95		2.5	V	DV_{DD} = 3V
V_{T-}	0.8		1.4	V	DV_{DD} = 5V
	0.4		1.1	V	DV_{DD} = 3V
V_{T+} - V_{T-}	0.3		0.85	V	DV_{DD} = 5V or 3V
Input Currents	2.0			V	
Port 0, P1.0→P1.7, EA			+/- 10	µA	V_{IN} = 0V or V_{DD}
SCLOCK, MOSI,MISO SS[13]	-10		-40	µA	V_{IN} = 0V, DV_{DD}=5V, Internal Pullup
			+/-10	µA	V_{IN} = DV_{DD}, DV_{DD}=5V
RESET			+/-10	µA	V_{IN} = 0V, DV_{DD}=5V
	35		105	µA	V_{IN} = DV_{DD}, DV_{DD}=5V, Internal Pull-Down
Port 2, Port 3			+/-10	µA	V_{IN} = DV_{DD}, DV_{DD}=5V
	-180		-660	µA	V_{IN} = 2V, DV_{DD}=5V
	-20		-75	µA	V_{IN} = 0.45V, DV_{DD}=5V
Input Capacitance		10		pF	All Digital Inputs
LOGIC OUTPUTS					
All Digital Outputs except XTAL2[2]					
V_{OH}, Output High Voltage	2.4			V	DV_{DD} = 5V, I_{SOURCE} = 80 µA
	2.4			V	DV_{DD} = 3V, I_{SOURCE} = 20 µA
V_{OL}, Output Low Voltage[14]			0.8	V	I_{SINK} = 8mA, SCLOCK, MOSI/SDATA
			0.8	V	I_{SINK} = 10mA, P1.0, P1.1
			0.8	V	I_{SINK} = 1.6mA, All Other Outputs
Floating State Leakage Current			+/-10	µA	
Floating State Output Capacitance		10		pF	

PARAMETER	MIN	TYP	MAX	UNITS	CONDITION
START UP TIME					
At Power On		300		ms	
After External RESET in Normal Mode		3		ms	
After WDT RESET in Normal Mode		3		ms	Controlled via WDCON SFR

From Idle Mode		10	us	
From Power-Down Mode				
Oscillator Running				PLLCON.7 = 0
Wakeup with INT0 Interrupt		20	us	
Wakeup with SPI Interrupt		20	us	
Wakeup with TIC Interrupt		20	us	
Wakeup with External RESET		3	us	
Oscillator Powered Down				PLLCON.7 = 1
Wakeup with INT0 Interrupt		20	us	
Wakeup with SPI Interrupt		20	us	
Wakeup with External RESET		5	ms	
FLAH/EE MEMORY RELIABILITY CHARACTERISTICS				
Endurance[16]	100,000	700,000	Cycles	
Data Retention[17]	100		Years	
POWER REQUIREMENTS				
Power Supply Voltages				
AV_{DD} 3V Nominal	2.85	3.6	V	
AV_{DD} 5V Nominal	4.75	5.25	V	
DV_{DD} 3V Nominal	2.85	3.6	V	
DV_{DD} 5V Nominal	4.75	5.25	V	
Power Supply Rejection				AIN=1V, Range=± 2.56V, Primary & Auxiliary
Chop Disabled	70 95		dB	ADC.
Chop Enabled	113		dB	
5V POWER CONSUMPTION				4.75V < DVDD <5.25V, AVDD= 5.25V
Normal Mode[18, 19]				
DV_{DD} Current		4	mA	core clock = 1.57MHz
	13	16	mA	core clock = 12.58MHz
AV_{DD} Current		180	µA	
Power-Down Mode[18, 19]				
DV_{DD} Current		53	µA	T_{MAX} = 85°C; Osc ON;TIC ON
		100	µA	T_{MAX} = 125°C; Osc ON; TIC ON
DV_{DD} Current		30	µA	T_{MAX} = 85°C; Osc OFF
		80	µA	T_{MAX} = 125°C; Osc OFF
AV_{DD} Current		1	µA	T_{MAX} = 85°C; Osc ON or OFF
		3	µA	T_{MAX} = 125°C; Osc ON or OFF
Typical Additional Peripheral Currents (AI_{DD} and D I_{DD})				
Primary ADC	1		mA	
Auxiliary ADC	0.5		mA	
Power Supply Monitor	50		µA	
DAC	150		µA	
Dual Excitation Current Sources	400		µA	
3V POWER CONSUMPTION				4.75V < DVDD <5.25V, AVDD= 5.25V
Normal Mode[18, 19]				
DV_{DD} Current		2.3	mA	core clock = 1.57MHz
	8	10	mA	core clock = 12.58MHz
AV_{DD} Current		180	µA	
Power-Down Mode[18, 19]				
DV_{DD} Current		20	µA	T_{MAX} = 85°C; Osc ON;TIC ON
		40	µA	T_{MAX} = 125°C; Osc ON; TIC ON
DV_{DD} Current	10		µA	Osc OFF
		80	µA	T_{MAX} = 125°C; Osc OFF
AV_{DD} Current		1	µA	T_{MAX} = 85°C; Osc ON or OFF
		3	µA	T_{MAX} = 125°C; Osc ON or OFF

NOTES

1 Temperature Range for ADuC845BS (MQFP package) is –40°C to +125°C.
Temperature Range for ADuC845BCP (CSP package) is –40°C to +85°C.

2 These numbers are not production tested but are guaranteed by design and/or characterization data on production release.

3 System Zero-Scale Calibration can remove this error.

4 The primary ADC is factory calibrated at 25°C with AVDD = DVDD = 5 V yielding this full-scale error of 10 μV. If user power supply or temperature conditions are significantly different from these, an Internal Full-Scale Calibration will restore this error to 10 μV. A system zero-scale and full-scale calibration will remove this error altogether.

5 Gain Error Drift is a span drift. To calculate Full-Scale Error Drift, add the Offset Error Drift to the Gain Error Drift times the full-scale input.

6 The auxiliary ADC is factory calibrated at 25°C with AVDD = DVDD = 5 V yielding this full-scale error of –2.5 LSB. A system zero-scale and full-scale calibration will remove this error altogether.

7 DAC linearity and ac specifications are calculated using: reduced code range of 48 to 4095, 0 to VREF, reduced code range of 100 to 3950, 0 to VDD.

8 Gain Error is a measure of the span error of the DAC.

9 In general terms, the bipolar input voltage range to the primary ADC is given by RangeADC = ±(VREF 2^{RN})/125, where:
VREF = REFIN(+) to REFIN(–) voltage and VREF = 1.25 V when internal ADC VREF is selected.
RN = decimal equivalent of RN2, RN1, RN0
e.g., VREF = 2.5 V and RN2, RN1, RN0 = 1, 1, 0 the RangeADC = ±1.28 V, In unipolar mode, the effective range is 0 V to 1.28 V in our example.

10 1.25V is used as the reference voltage to the ADC when internal VREF is selected via XREF0/XREF1 or AXREF bits in ADC0CON2 and ADC1CON, respectively.

11 In bipolar mode, the Auxiliary ADC can only be driven to a minimum of AGND – 30 mV as indicated by the Auxiliary ADC absolute AIN voltage limits. The bipolar range is still –VREF to +VREF; however, the negative voltage is limited to –30 mV.

12 The ADuC845BCP (CSP Package) has been qualified and tested with the base of the CSP Package floating.

13 Pins configured in SPI Mode, pins configured as digital inputs during this test.

14 Pins configured in I^2C Mode only.

15 Flash/EE Memory Reliability Characteristics apply to both the Flash/EE program memory and Flash/EE data memory.

16 Endurance is qualified to 100 Kcycles as per JEDEC Std. 22 method A117 and measured at –40 °C, +25°C, +85°C, and +125°C. Typical endurance at 25°C is 700 Kcycles.

17 Retention lifetime equivalent at junction temperature (TJ) = 55°C as per JEDEC Std. 22, Method A117. Retention lifetime based on an activation energy of 0.6eV will derate with junction temperature.

18 Power Supply current consumption is measured in Normal, Idle, and Power-Down Modes under the following conditions:
Normal Mode: Reset = 0.4 V, Digital I/O pins = open circuit, Core Clk changed via CD bits in PLLCON, Core Executing internal software loop.
Idle Mode: Reset = 0.4 V, Digital I/O pins = open circuit, Core Clk changed via CD bits in PLLCON, PCON.0 = 1, Core Execution suspended in idle mode.
Power-Down Mode: Reset = 0.4 V, All P0 pins and P1.2–P1.7 Pins = 0.4 V, All other digital I/O pins are open circuit, Core Clk changed via CD bits in PLLCON, PCON.1 = 1, Core Execution suspended in power-down mode, OSC turned ON or OFF via OSC_PD bit (PLLCON.7) in PLLCON SFR.

19 DVDD power supply current will increase typically by 3 mA (3 V operation) and 10 mA (5 V operation) during a Flash/EE memory program or erase cycle.

Specifications subject to change without notice

ABSOLUTE MAXIMUM RATINGS[1]
(TA = 25°C unless otherwise noted)

AV_{DD} to AGND	–0.3 V to +7 V
AV_{DD} to DGND	–0.3 V to +7 V
DV_{DD} to AGND	–0.3 V to +7 V
DV_{DD} to DGND	–0.3 V to +7 V
AGND to DGND[2]	–0.3 V to +0.3 V
AV_{DD} to DV_{DD}	–2 V to +5 V
Analog Input Voltage to AGND[3]	–0.3 V to AV_{DD} +0.3 V
Reference Input Voltage to AGND	–0.3 V to AV_{DD} +0.3 V
AIN/REFIN Current (Indefinite)	30 mA
Digital Input Voltage to DGND	–0.3 V to DV_{DD} +0.3 V
Digital Output Voltage to DGND	–0.3 V to DV_{DD} +0.3 V
Operating Temperature Range	–40°C to +125°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
q_{JA} Thermal Impedance	90°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

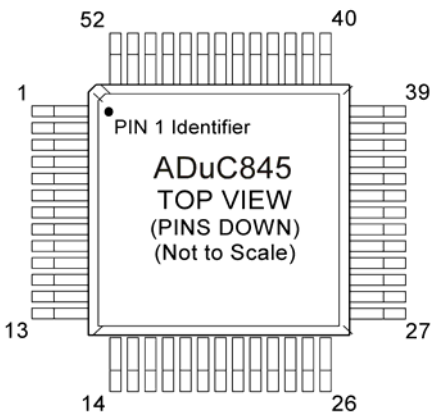
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]AGND and DGND are shorted internally on the ADuC845.

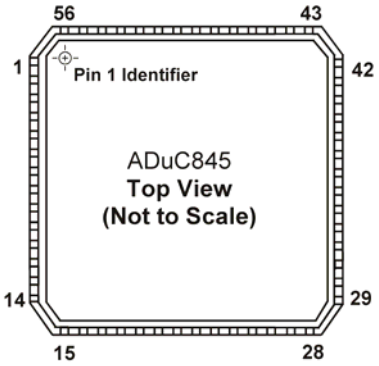
[3]Applies to P1.0 to P1.7 pins operating in analog or digital input modes.

PIN CONFIGURATION

52-Lead MQFP



56-Lead CSP



ORDERING GUIDE

MODEL	Temperature Range	Package Description	Package Option
ADuC845BS62-5	-40 → +125°C	52-Lead Plastic Quad Flatpack, 62kB, 5v	S-52
ADuC845BS62-3	-40 → +125°C	52-Lead Plastic Quad Flatpack, 62kB, 3v	S-52
ADuC845BS8-5	-40 → +125°C	52-Lead Plastic Quad Flatpack, 8kB, 5v	S-52
ADuC845BS8-3	-40 → +125°C	52-Lead Plastic Quad Flatpack, 8kB, 3v	S-52
ADuC845BCP62-5	-40 → +85°C	56-Lead Chip Scale Package, 62kB, 5v	CP-56
ADuC845BCP62-3	-40 → +85°C	56-Lead Chip Scale Package, 62kB, 3v	CP-56
ADuC845BCP8-5	-40 → +85°C	56-Lead Chip Scale Package, 8kB, 5v	CP-56
ADuC845BCP8-3	-40 → +85°C	56-Lead Chip Scale Package, 8kB, 3v	CP-56
EVAL-ADuC845QS		QuickStart™ Development System	
EVAL-ADuC845QSP		QuickStart PLUS Development System	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADuC845 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

Pin No: 52-MQFP	Pin No: 56-CSP	Pin Mnemonic	Type	Description
1	56	P1.0/AIN1	I	By power on default P1.0/AIN1 is configured as the AIN1 Analog Input. AIN1 can be used as a pseudo differential input when used with AINCOM or as the positive input of a fully differential pair when used with AIN2. P1.0 has no digital output driver. It can function as a digital input for which '0' must be written to the port bit. As a digital input, this pin must be driven high or low externally.
2	1	P1.1/AIN2	I	By power on default P1.1/AIN2 is configured as the AIN2 Analog Input. AIN2 can be used as a pseudo differential input when used with AINCOM or as the negative input of a fully differential pair when used with AIN1. P1.1 has no digital output driver. It can function as a digital input for which '0' must be written to the port bit. As a digital input, this pin must be driven high or low externally.
3	2	P1.2/AIN3/REFIN2+	I	By power on default P1.2/AIN3 is configured as the AIN3 Analog Input. AIN3 can be used as a pseudo differential input when used with AINCOM or as the positive input of a fully differential pair when used with AIN4. P1.2 has no digital output driver. It can function as a digital input for which '0' must be written to the port bit. As a digital input, this pin must be driven high or low externally. This pin also functions as a second external differential reference input, positive terminal.
4	3	P1.3/AIN4/REFIN2-	I	By power on default P1.3/AIN4 is configured as the AIN4 Analog Input. AIN4 can be used as a pseudo differential input when used with AINCOM or as the negative input of a fully differential pair when used with AIN3. P1.3 has no digital output driver. It can function as a digital input for which '0' must be written to the port bit. As a digital input, this pin must be driven high or low externally. This pin also functions as a second external differential reference input, negative terminal.
5	4	AVDD	S	Analog Supply Voltage
6	5	AGND	S	Analog Ground.
---	6	AGND	S	A second Analog ground is provided with the CSP version only*
7	7	REFIN-	I	External Differential Reference Input, negative terminal
8	8	REFIN+	I	External Differential Reference Input, positive terminal
9	9	P1.4/AIN5	I	By power on default P1.4/AIN5 is configured as the AIN5 Analog Input. AIN5 can be used as a pseudo differential input when used with AINCOM or as the positive input of a fully differential pair when used with AIN6. P1.0 has no digital output driver. It can function as a digital input for which '0' must be written to the port bit. As a digital input, this pin must be driven high or low externally.
10	10	P1.5/AIN6	I	By power on default P1.5/AIN6 is configured as the AIN6 Analog Input. AIN6 can be used as a pseudo differential input when used with AINCOM or as the negative input of a fully differential pair when used with AIN5. P1.1 has no digital output driver. It can function as a digital input for which '0' must be written to the port bit. As a digital input, this pin must be driven high or low externally.
11	11	P1.6/AIN7/IEXC1	I/O	By power on default P1.6/AIN7 is configured as the AIN7 Analog Input. AIN7 can be used as a pseudo differential input when used with AINCOM or as the positive input of a fully differential pair when used with AIN8. One or Both current sources can also be configured at this pin. P1.0 has no digital output driver. It can function as a digital input for which '0' must be written to the port bit. As a digital input, this pin must be driven high or low externally.

*Note: This pin is provided on the CSP version only.

Pin No: 52-MQFP	Pin No: 56-CSP	Pin Mnemonic	Type	Description
12	12	P1.7/AIN8/IEXC2	I/O	By power on default P1.7/AIN8 is configured as the AIN8 Analog Input. AIN8 can be used as a pseudo differential input when used with AINCOM or as the negative input of a fully differential pair when used with AIN7. One or Both current sources can also be configured at this pin P1.1 has no digital output driver. It can function as a digital input for which '0' must be written to the port bit. As a digital input, this pin must be driven high or low externally.
13	13	AINCOM/DAC	I/O	All analog inputs can be referred to this pin provided a relevant pseudo differential input mode is selected. This pin also functions as an alternative pin out for the DAC.
14	14	DAC	O	The voltage output from the DAC, if enabled, will appear at this pin.
----	15	AIN9*	I	AIN9 can be used as a pseudo differential analog input when used with AINCOM or as the positive input of a fully differential pair when used with AIN10*.
----	16	AIN10*	I	AIN10 can be used as a pseudo differential analog input when used with AINCOM or as the negative input of a fully differential pair when used with AIN9*.
15	17	RESET	I	Reset Input. A high level on this pin for 16 core clock cycles while the oscillator is running resets the device. There is an internal weak pull-down and a Schmitt trigger input stage on this pin.
16-19 22-25	18-21 24-27	P3.0 → P3.7	I/O	P3.0–P3.7 are bi-directional port pins with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 3 pins being pulled externally low will source current because of the internal pull-up resistors. When driving a 0-to-1 output transition, a strong pull-up is active for two core clock periods of the instruction cycle. Port 3 pins also have various secondary functions described below.
16	18	P3.0/RXD		Receiver Data for UART serial Port
17	19	P3.1/TXD		Transmitter Data for UART serial Port
18	20	P3.2/INT0		External Interrupt 0. This pin can also be used as a gate control input to Timer0.
19	21	P3.3/INT1		External Interrupt 1. This pin can also be used as a gate control input to Timer1.
22	24	P3.4/T0		Timer/Counter 0 External Input
23	25	P3.5/T1		Timer/Counter 1 External Input
24	26	P3.6//WR		External Data Memory Write Strobe. Latches the data byte from Port 0 into an external data memory.
25	27	P3.7//RD		External Data Memory Read Strobe. Enables the data from an external data memory to Port 0.
20, 34, 48	22, 36, 51	DVDD	S	Digital Supply Voltage
21, 35, 47	23, 37, 38, 50	DGND	S	Digital Ground.
26	28	SCLK (I2C)	I/O	Serial interface clock for the I2C interface. As an input this pin is a Schmitt triggered input and a weak internal pull-up is present on this pin unless it is outputting logic low. this pin can also be controlled in software as a digital output pin.
27	29	SDATA	I/O	Serial data pin for the I^2C interface. As an input this pin has a weak internal pull-up present unless it is outputting logic low.

*Note: This pin is provided on the CSP version only.

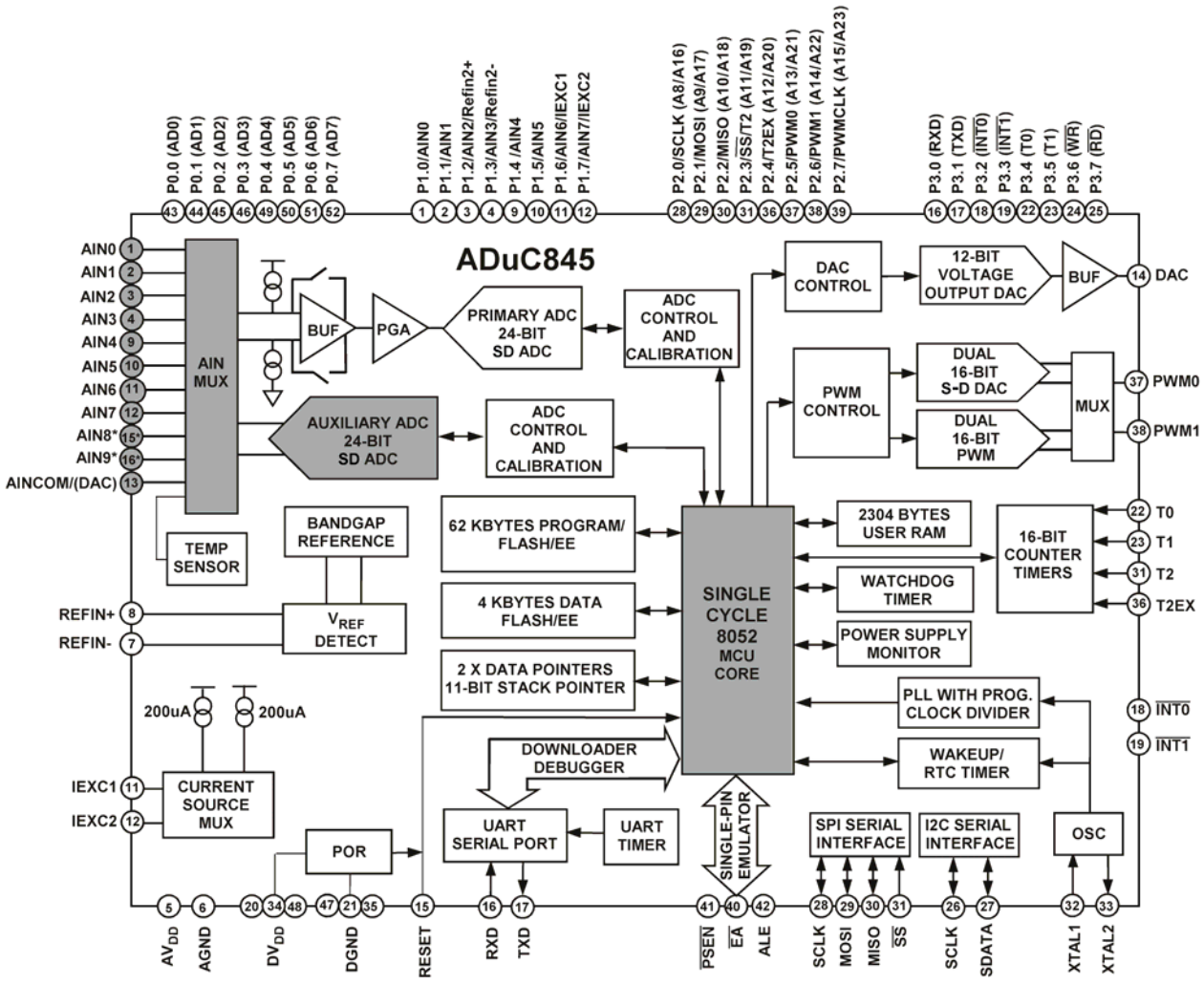
Pin No: 52-MQFP	Pin No: 56-CSP	Pin Mnemonic	Type	Description
28 → 31 36 → 39	30 → 33 39 → 42	P2.0 → P2.7	I/O	Port 2 is a bidirectional port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 2 pins being pulled externally low will source current because of the internal pull-up resistors. Port 2 emits the middle and high order address bytes during accesses to the 24-bit external data memory space. Port 2 pins also have various secondary functions described below.
28	30	P2.0/SCLOCK (SPI)		Serial interface clock for the SPI interface. As an input this pin is a Schmitt triggered input and a weak internal pull-up is present on this pin unless it is outputting logic low.
29	31	P2.1/MOSI		Serial master output/slave input data for the SPI interface. A strong internal pull-up is present on this pin when the SPI interface outputs a logic high. A strong internal pull-down is present on this pin when the SPI interface outputs a logic low.
30	32	P2.2/MISO		Master Input/Slave Output for the SPI Interface. There is a weak pull-up on this input pin.
31	33	P2.3/SS/T2		Slave select input for the SPI Interface is present at this pin. A weak pull-up is present on this pin. On both package options this pin can also be used to provide a clock input to Timer 2. When Enabled, counter 2 is incremented in response to a negative transition on the T2 input pin.
36	39	P2.4/T2EX		This pin can be used to provide a control input to Timer 2. When Enabled, a negative transition on the T2EX input pin will cause a Timer 2 capture or reload event.
37	40	P2.5/PWM0		If the PWM is enabled then the PWM0 output will appear at this pin.
38	41	P2.6/PWM1		If the PWM is enabled then the PWM1 output will appear at this pin.
39	42	P2.7/PWMCLK		If the PWM is enabled then an external PWM clock can be provided at this pin.
32	34	XTAL1	I	Input to the crystal oscillator inverter.
33	35	XTAL2	O	Output from the crystal oscillator inverter. (see "Hardware Design Considerations" for description)
40	43	EA		External Access Enable, Logic Input. When held high, this input enables the device to fetch code from internal program memory locations 0000h to F7FFh. No external program memory access is available on the ADuC845. To determine the mode of code execution, the EA pin is sampled at the end of an external RESET assertion or as part of a device power cycle. EA may also be used as an external emulation I/O pin and therefore the voltage level at this pin must not be changed during normal mode operation as it may cause an emulation interrupt that will halt code execution.
41	44	PSEN		Program Store Enable, Logic Output. It is active every six oscillator periods except during external data memory accesses. This pin remains high during internal program execution. PSEN can also be used to enable serial download mode when pulled low through a resistor at the end of an external RESET assertion or as part of a device power cycle.
42	45	ALE		Address Latch Enable, Logic Output. This output is used to latch the low byte (and page byte for 24-bit data address space accesses) of the address to external memory during external data memory access cycles. It is activated every six oscillator periods except during an external data memory access. It can be disabled by setting the PCON.4 bit in the PCON SFR.

Pin No: 52-MQFP	Pin No: 56-CSP	Pin Mnemonic	Type*	Description
43 → 46 49 → 52	46 → 49 52 → 55	P0.0 → P0.7	I/O	P0.0–P0.7, these pins are part of Port0 which is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float and in that state can be used as high impedance inputs. An external pull-up resistor will be required on P0 outputs to force a valid logic high level externally. Port 0 is also the multiplexed low-order address and data bus during accesses to external data memory. In this application it uses strong internal pull-ups when emitting 1s.

*I = Input, O = Output, S = Supply.

DETAILED BLOCK DIAGRAM WITH PIN NUMBERS

Pin numbers refer to the 52pin MQFP package.



* CSP PACKAGE ONLY. The pin numbers refer to the CSP package only.

Shaded areas are upgrades from the ADuC834, and include a single cycle core, up to 10 ADC input channels (8 on the MQFP package), and the Auxiliary ADC is now 24-bit.

Figure 1: Detailed Block Diagram of the ADuC845

COMPLETE SFR MAP

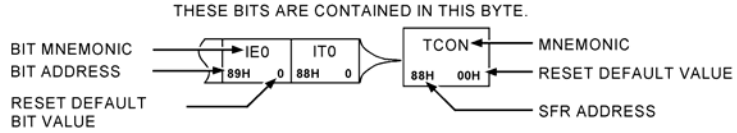
Figure 2 below shows a full SFR memory map and the SFR contents after RESET. NOT USED indicates unoccupied SFR locations. Unoccupied locations in the SFR address space are not implemented; i.e., no register exists at this location. If an unoccupied location is read, an unspecified value is returned. SFR locations that are reserved for future use are shaded (RESERVED) and should not be accessed by user software.

ISPI FFH 0	WCOL FEH 0	SPE FDH 0	SPIM FCH 0	CPOL FBH 0	CPHA FAH 1	SPR1 F9H 0	SPR0 F8H 0	BITS	SPICON F8H 04H
F7H 0	F6H 0	F5H 0	F4H 0	F3H 0	F2H 0	F1H 0	F0H 0	BITS	B F0H 00H
MDO EFH 0	MDE EEH 0	MC0 EDH 0	MDI ECH 0	I2CM EBH 0	I2CRS EAH 0	I2CTX E9H 0	I2CI E8H 0	BITS	I2CCON E8H 00H
E7H 0	E6H 0	E5H 0	E4H 0	E3H 0	E2H 0	E1H 0	E0H 0	BITS	ACC E0H 00H
RDY0 DFH 0	RDY1 DEH 0	CAL DDH 0	NOXREF DCH 0	ERR0 DBH 0	ERR1 DAH 0	D9H 0	D8H 0	BITS	ADCSTAT D8H 00H
CY D7H 0	AC D6H 0	F0 D5H 0	RSI D4H 0	RS0 D3H 0	OV D2H 0	FI D1H 0	P D0H 0	BITS	PSW D0H 00H
TF2 CFH 0	EXF2 CEH 0	RCLK CDH 0	TCLK CCH 0	EXEN2 CBH 0	TR2 CAH 0	CNT2 C9H 0	CAP2 C8H 0	BITS	T2CON C8H 00H
PRE3 C7H 0	PRE2 C6H 0	PRE1 C5H 0	PRE0 C4H 1	WDIR C3H 0	WDS C2H 0	WDE C1H 0	WDWR C0H 0	BITS	WDCON C0H 10H
BFH 0	PADC BEH 0	PT2 BDH 0	PS BCH 0	PT1 BBH 0	PX1 BAH	PT0 B9H 0	PX0 B8H 0	BITS	IP B8H 00H
$\overline{RD}$ B7H 1	$\overline{WR}$ B6H 1	T1 B5H 1	T0 B4H 1	$\overline{INT1}$ B3H 1	$\overline{INT0}$ B2H 1	TXD B1H 1	RXD B0H 1	BITS	P3 B0H FFH
EA AFH 0	EADC AEH 0	ET2 ADH 0	ES ACH 0	ET1 ABH 0	EX1 AAH 0	ET0 A9H 0	EX0 A8H 0	BITS	IE A8H 00H
A7H 1	A6H 1	A5H 1	A4H 1	A3H 1	A2H 1	A1H 1	A0H 1	BITS	P2 A0H FFH
SM0 9FH 0	SM1 9EH 0	SM2 9DH 0	REN 9CH 0	TB8 9BH 0	RB8 9AH 0	T1 99H 0	R1 98H 0	BITS	SCON 98H 00H
97H 1	96H 1	95H 1	94H 1	93H 1	92H 1	T2EX 91H 1	T2 90H 1	BITS	P1 90H FFH
TF1 8FH 0	TR1 8EH 0	TF0 8DH 0	TR0 8CH 0	IE1 8BH 0	IT1 8AH 0	IE0 89H 0	IT0 88H 0	BITS	TCON 88H 00H
87H 1	86H 1	85H 1	84H 1	83H 1	82H 1	81H 1	80H 1	BITS	P0 80H FFH

RESERVED	RESERVED	DACL FBH 00H	DACH FCH 00H	DACCON FDH 00H	RESERVED	RESERVED
RESERVED	I2CADD1 F2H 7FH	NOT USED	RESERVED	RESERVED	RESERVED	SPIDAT F7H 00H
GN0L[2] E9H 55H	GN0M[2] EAH 55H	GN0H[2] EBH 53H	GN1L[2] ECH 9AH	GN1H[2] EDH 59H	RESERVED	RESERVED
OF0L E1H 00H	OF0M E2H 00H	OF0H E3H 80H	OF1L E4H 00H	OF1H E5H 80H	ADC0CON2 E6H 00H	RESERVED
ADC0L D9H 00H	ADC0M DAH 00H	ADC0H DBH 00H	ADC1M DCH 00H	ADC1H DDH 00H	ADC1L DEH 00H	PSMCON DFH DEH
ADCMODE D1H 10H	ADC0CON1 D2H 07H	ADC1CON D3H 00H	SF D4H 45H	ICON D5H 00H	RESERVED	PLLCON D7H 03H
RESERVED	RCAP2L CAH 00H	RCAP2H CBH 00H	TL2 CCH 00H	TH2 CDH 00H	RESERVED	RESERVED
RESERVED	CHIPID C2H 22H	RESERVED	RESERVED	RESERVED	EADRL C6H 00H	EADRH C7H 00H
ECON B9H 00H	RESERVED	RESERVED	EDATA1 BCH 00H	EDATA2 BDH 00H	EDATA3 BEH 00H	EDATA4 BFH 00H
PWM0L B1H 00H	PWM0H B2H 00H	PWM1L B3H 00H	PWM1H B4H 00H	RESERVED	RESERVED	SPH B7H 00H
IEIP2 A9H A0H	RESERVED	RESERVED	RESERVED	RESERVED	PWMCON AEH 00H	CFG845 AFH 00H
TIMECON A1H 00H	HTHSEC[1] A2H 00H	SEC[1] A3H 00H	MIN[1] A4H 00H	HOUR[1] A5H 00H	INTVAL A6H 00H	DPCON A7H 00H
SBUF 99H 00H	I2CDAT 9AH 00H	I2CADD 9BH 55H	RESERVED	T3FD 9DH 00H	T3CON 9EH 00H	RESERVED
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
TMOD 89H 00H	TL0 8AH 00H	TL1 8BH 00H	TH0 8CH 00H	TH1 8DH 00H	RESERVED	RESERVED
SP 81H 07H	DPL 82H 00H	DPH 83H 00H	DPP 84H 00H	RESERVED	RESERVED	PCON 87H 00H

[1] THESE SFRS MAINTAIN THEIR PRE-RESET VALUES AFTER A RESET IF TIMECON.0=1.
[2] CALIBRATION COEFFICIENTS ARE PRECONFIGURED AT POWER-UP TO FACTORY CALIBRATED VALUES.

SFR MAP KEY:



SFR NOTE:
SFRs WHOSE ADDRESSES END IN 0H OR 8H ARE BIT-ADDRESSABLE.

Figure 2: Complete SFR Map

INTRODUCTION

The ADuC845 is a 12.58MIPs 8052 core upgrade to the ADuC834. It includes additional analog inputs for applications requiring more ADC channels. It has all the same features as the ADuC834 but the standard 12-cycle 8052 core has been replaced with a 12.58MIPs single cycle core.

Since the ADuC845 and ADuC834 share the same feature set only the differences between the two chips are documented here. For full documentation on the ADuC834 please consult the datasheet available at http://www.analog.com/microconverter.

GENERAL DESCRIPTION

The ADuC845 is a complete smart transducer front end, integrating two high resolution sigma-delta ADCs with flexible, 10/8-channel input multiplexing, a fast 8-bit MCU, and program/data Flash/EE memory on a single chip.

The two independent ADCs (primary and auxiliary) include flexible input multiplexing, a temperature sensor and a PGA (allowing direct measurement of low level signals). The ADCs with on-chip digital filtering and programmable output data rates are intended for the measurement of wide dynamic range, low frequency signals, such as those in weigh scale, strain-gage, pressure transducer, or temperature measurement applications.

The device operates from a 32 kHz crystal with an on-chip PLL generating a high frequency clock of 12.58 MHz. This clock is routed through a programmable clock divider from which the MCU core clock operating frequency is generated. The microcontroller core is an optimized single cycle 8052 offering up to 12.58MIPs performance while maintaining the 8051 instruction set compatibility.

62 Kbytes of nonvolatile Flash/EE program memory, 4 Kbytes of nonvolatile Flash/EE data memory, and 2304 bytes of data RAM are provided on-chip. The program memory can be configured as data memory to give up to 60 Kbytes of NV data memory in data logging applications.

On-chip factory firmware supports in-circuit serial download and debug modes (via UART), as well as single-pin emulation mode via the EA pin. The ADuC845 is supported by a QuickStart™ development system featuring low cost software and hardware development tools

8052 Instruction Set

The following pages document the number of clock cycles required for each instruction. Most instructions are executed in one or two clock cycles resulting in 12.6MIPs peak performance when operating at PLLCON = 00H.

Timer Operation

Timers on a standard 8052 increment by one with each machine cycle. On the ADuC842 one machine cycle is equal to one clock cycle hence the timers will increment at the same rate as the core clock.

ALE

The output on the ALE pin on the ADuC834 was a clock at 1/6th of the core operating frequency. On the ADuC845 the ALE pin operates as follows….

For a single machine cycle instruction: ALE is high for the first half of the machine cycle and low for the second half. The ALE output is at the core operating frequency. For a two or more machine cycle instruction: ALE is high for the first half of the first machine cycle and then low for the rest of the machine cycles.

External Memory Access

There is no support for external program memory access on the ADuC845, but the ADuC845 can access up to 16M-bytes (24-address bits) of external data memory. When accessing external RAM the EWAIT register may need to be programmed in order to give extra machine cycles to MOVX commands. This is to account for differing external RAM access speeds.

INSTRUCTION TABLE

Optimized Single Cycle 8051 Instruction Set

Mnemonic	Description	Bytes	Cycles
Arithmetic			
ADD A,Rn	Add register to A	1	1
ADD A,@Ri	Add indirect memory to A	1	2
ADD A,dir	Add direct byte to A	2	2
ADD A,#data	Add immediate to A	2	2
ADDC A,Rn	Add register to A with carry	1	1
ADDC A,@Ri	Add indirect memory to A with carry	1	2
ADDC A,dir	Add direct byte to A with carray	2	2
ADD A,#data	Add immediate to A with carry	2	2
SUBB A,Rn	Subtract register from A with borrow	1	1
SUBB A,@Ri	Subtract indirect memory from A with borrow	1	2
SUBB A,dir	Subtract direct from A with borrow	2	2
SUBB A,#data	Subtract immediate from A with borrow	2	2
INC A	Increment A	1	1
INC Rn	Increment register	1	1
INC @Ri	Increment indirect memory	1	2
INC dir	Increment direct byte	2	2
INC DPTR	Increment data pointer	1	3
DEC A	Decrement A	1	1
DEC Rn	Decrement Register	1	1
DEC @Ri	Decrement indirect memory	1	2
DEC dir	Decrement direct byte	2	2
MUL AB	Multiply A by B	1	9
DIV AB	Divide A by B	1	9
DA A	Decimal Adjust A	1	2
Logic			
ANL A,Rn	AND register to A	1	1
ANL A,@Ri	AND indirect memory to A	1	2
ANL A,dir	AND direct byte to A	2	2
ANL A,#data	AND immediate to A	2	2
ANL dir,A	AND A to direct byte	2	2
ANL dir,#data	AND immediate data to direct byte	3	3
ORL A,Rn	OR register to A	1	1
ORL A,@Ri	OR indirect memory to A	1	2
ORL A,dir	OR direct byte to A	2	2
ORL A,#data	OR immediate to A	2	2
ORL dir,A	OR A to direct byte	2	2
ORL dir,#data	OR immediate data to direct byte	3	3
XRL A,Rn	Exclusive-OR register to A	1	1
XRL A,@Ri	Exclusive-OR indirect memory to A	2	2
XRL A,#data	Exclusive-OR immediate to A	2	2
XRL dir,A	Exclusive-OR A to direct byte	2	2
XRL A,dir	Exclusive-OR indirect memory to A	2	2
XRL dir,#data	Exclusive-OR immediate data to direct	3	3
CLR A	Clear A	1	1
CPL A	Complement A	1	1
SWAP A	Swap Nibbles of A	1	1
RL A	Rotate A left	1	1
RLC A	Rotate A left through carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through carry	1	1
Data Transfer			
MOV A,Rn	Move register to A	1	1
MOV A,@Ri	Move indirect memory to A	1	2
MOV Rn,A	Move A to register	1	1
MOV @Ri,A	Move A to indirect memory	1	2
MOV A,dir	Move direct byte to A	2	2
MOV A,#data	Move immediate to A	2	2
MOV Rn,#data	Move register to immediate	2	2

Mnemonic	Description	Bytes	Cycles
MOV dir,A	Move A to direct byte	2	2
MOV Rn, dir	Mov register to direct byte	2	2
MOV dir, Rn	Move direct to register	2	2
MOV @Ri,#data	Move immediate to indirect memory	2	2
MOV dir,@Ri	Move indirect to direct memory	2	2
MOV @Ri,dir	Move direct to indirect memory	2	2
MOV dir,dir	Move direct byte to direct byte	3	3
MOV dir,#data	Move immediate to direct byte	3	3
MOV DPTR,#data	Move immediate to data pointer	3	3
MOVC A,@A+DPTR	Move code byte relative DPTR to A	1	4
MOVC A,@A+PC	Move code byte relative PC to A	1	4
MOVX A,@Ri	Move external (A8) data to A	1	4
MOVX A,@DPTR	Move external (A16) data to A	1	4
MOVX @Ri,A	Move A to external data (A8)	1	4
MOVX @DPTR,A	Move A to external data (A16)	1	4
PUSH dir	Push direct byte onto stack	2	2
POP dir	Pop direct byte from stack	2	2
XCH A,Rn	Exchange A and register	1	1
XCH A,@Ri	Exchange A and indirect memory	1	2
XCHD A,@Ri	Exchange A and indirect memory nibble	1	2
XCH A,dir	Exchange A and direct byte	2	2
Boolean			
CLR C	Clear carry	1	1
CLR bit	Clear direct bit	2	2
SETB C	Set Carry	1	1
SETB bit	Set direct bit	2	2
CPL C	Complement carry	1	1
CPL bit	Complement direct bit	2	2
ANL C,bit	AND direct bit and carry	2	2
ANL C,/bit	AND direct bit inverse to carry	2	2
ORL C,bit	OR direct bit and carry	2	2
ORL C,/bit	OR direct bit inverse to carry	2	2
MOV C,bit	Move direct bit to carry	2	2
MOV bit,C	Move carry to direct bit	2	2
Branching			
JMP @A+DPTR	Jump indirect relative to DPTR	1	3
RET	Return from subroutine	1	4
RETI	Return from interrupt	1	4
ACALL addr11	Absolute jump to subroutine	2	3
AJMP addr11	Absolute jump unconditional	2	3
SJMP rel	Short jump (relative address)	2	3
JC rel	Jump on carry = 1	2	3
JNC rel	Jump on carry = 0	2	3
JZ rel	Jump on accumulator = 0	2	3
JNZ rel	Jump on accumulator ! = 0	2	3
DJNZ Rn,rel	Decrement register, jnz relative	2	3
LJMP	Long jump unconditional	3	4
LCALL addr16	Long jump to subroutine	3	4
JB bit,rel	Jump on direct bit = 1	3	4
JNB bit,rel	Jump on direct bit = 0	3	4
JBC bit,rel	Jump on direct bit = 1 and clear	3	4
CJNE A,dir,rel	Compare A, direct JNE relative	3	4
CJNE A,#data,rel	Compare A, immediate JNE relative	3	4
CJNE Rn,#data,rel	Compare register, immediate JNE relative	3	4
CJNE @Ri,#data,rel	Compare indirect, immediate JNE relative	3	4
DJNZ dir,rel	Decrement direct byte, JNZ relative	3	4
Miscellaneous			
NOP	No operation	1	1

1. One cycle is one clock.
2. MOVX instructions are four cycles when they have 0 wait state. Cycles of MOVX instructions are 4 + n cycles when they have n wait states.
3. LCALL instruction are three cycles when the LCALL instruction comes from an interrupt.

MEMORY7 ORGANISATION

The ADuC845 contains 4 different memory blocks namely:
- 62k/30k/6k Bytes of On-Chip Flash/EE Program Memory
- 4kBytes of On-Chip Flash/EE Data Memory
- 256 Bytes of General Purpose RAM
- 2kBytes of Internal XRAM

(1) Flash/EE Program Memory

The ADuC845 provides up to 62kBytes of Flash/EE program memory to run user code.

When EA is pulled high externally during a power cycle or a hardware reset the part defaults to code execution from its internal 62kBytes of Flash/EE program memory. The ADuC845 does not support the rollover from internal code space to external code space. No external code space is available on the ADuC845.

Permanently embedded firmware allows code to be serially downloaded to the 62kBytes of internal code space via the UART serial port while the device is in-circuit. No external hardware is required.

56kBytes of the program memory can be reprogrammed during runtime hence the code space can be upgraded in the field using a user defined protocol or it can be used as a data memory. This will be discussed in more detail in the Flash/EE Memory section of the datasheet.

(2) Flash/EE Data Memory

4kBytes of Flash/EE Data Memory are available to the user and can be accessed indirectly via a group of registers mapped into the Special Function Register (SFR) area. Access to the Flash/EE Data memory is discussed in detail later as part of the Flash/EE memory section in this data sheet.

(3) General Purpose RAM

The general purpose RAM is divided into two separate memories, namely the upper and the lower 128 bytes of RAM. The lower 128 bytes of RAM can be accessed through direct or indirect addressing while the upper 128 bytes of RAM can only be accessed through indirect addressing as it shares the same address space as the SFR space which can only be accessed through direct addressing.

The lower 128 bytes of internal data memory are mapped as shown in Figure 3. The lowest 32 bytes are grouped into four banks of eight registers addressed as R0 through R7. The next 16 bytes (128 bits), locations 20Hex through 2FHex above the register banks, form a block of directly addressable bit locations at bit addresses 00H through 7FH. The stack can be located anywhere in the internal memory address space, and the stack depth can be expanded up to 2048 bytes.

Reset initializes the stack pointer to location 07 hex. Any call or push pre-increments the SP before loading the stack. Hence loading the stack starts from locations 08 hex which is also the first register (R0) of register bank 1. Thus, if one is going to use more than one register bank, the stack pointer should be initialized to an area of RAM not used for data storage.

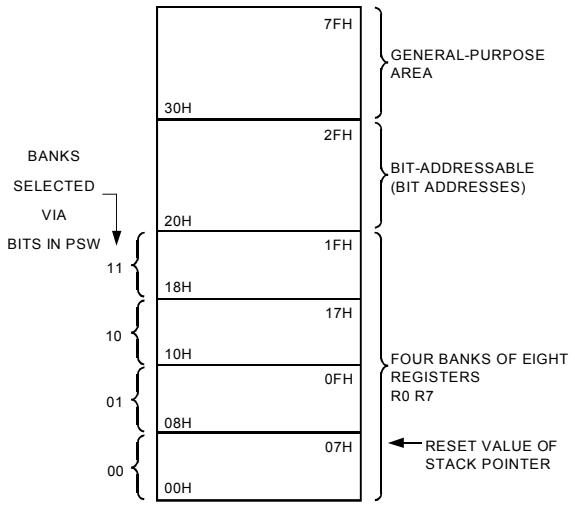


Figure 3. Lower 128 Bytes of Internal Data Memory

(4) Internal XRAM

The ADuC845 contains 2kBytes of on-chip extended data memory. This memory, although on-chip, is accessed via the MOVX instruction. The 2kBytes of internal XRAM are mapped into the bottom 2kBytes of the external address space if the CFG845.0 (see Table III) bit is set, otherwise access to the external data memory will occur just like a standard 8051.

Even with the CFG845.0 bit set access to the external XRAM will occur once the 24 bit DPTR is greater than 0007FFH.

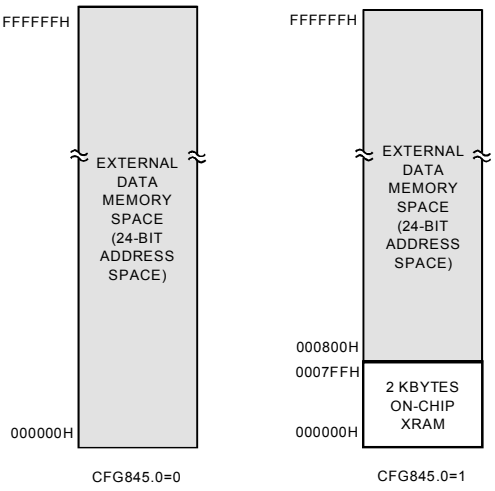


Figure 4: Internal and External XRAM

When accessing the internal XRAM, the P0, P2 port pins as well as the RD and WR strobes will not be output as per a standard 8051 MOVX instruction. This allows the user to use these port pins as standard I/O.

The upper 1792 bytes of the internal XRAM can be configured to be used as an extended 11-bit stack pointer.

By default the stack will operate exactly like an 8052 in that it will rollover from FFh to 00h in the general purpose RAM. On the ADuC845 however it is possible (by setting CFG845.7) to enable the 11-bit extended stack pointer. In this case the stack will rollover from FFh in RAM to 0100h in XRAM.

The 11-bit stack pointer is visable in the SP and SPH SFRs. The SP SFR is located at 81h as with a standard 8052. The SPH SFR is located at B7h. The 3 LSBs of this SFR contain the 3 extra bits necessary to extend the 8-bit stack pointer into an 11-bit stack pointer.

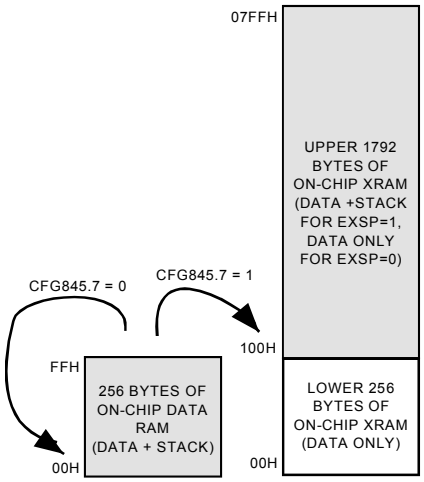


Figure 5. Extended Stack Pointer Operation

External Data Memory (External XRAM)
Just like a standard 8051 compatible core the ADuC845 can access external data memory using a MOVX instruction. The MOVX instruction automatically outputs the various control strobes required to access the data memory.
The ADuC845 however, can access up to 16MBytes of external data memory. This is an enhancement of the 64kBytes external data memory space available on a standard 8051 compatible core.
The external data memory is discussed in more detail in the ADuC845 Hardware Design Considerations section.

SPECIAL FUNCTION REGISTERS (SFRs)
The SFR space is mapped into the upper 128 bytes of internal data memory space and accessed by direct addressing only. It provides an interface between the CPU and all on chip peripherals. A block diagram showing the programming model of the ADuC845 via the SFR area is shown in Figure 6.
All registers except the Program Counter (PC) and the four general-purpose register banks, reside in the SFR area. The SFR registers include control, configuration, and data registers that provide an interface between the CPU and all on-chip peripherals.

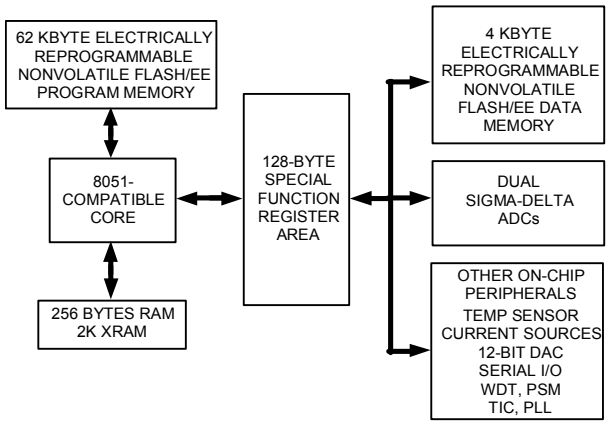


Figure 6. Programming Model

Accumulator SFR (ACC)
ACC is the Accumulator register and is used for math operations including addition, subtraction, integer multiplication and division, and Boolean bit manipulations. The mnemonics for accumulator-specific instructions refer to the Accumulator as A.

B SFR (B)
The B register is used with the ACC for multiplication and division operations. For other instructions it can be treated as a general-purpose scratchpad register.

Data Pointer (DPTR)
The Data Pointer is made up of three 8-bit registers, named DPP (page byte), DPH (high byte) and DPL (low byte). These are used to provide memory addresses for internal and external code access and external data access. It may be manipulated as a 16-bit register (DPTR = DPH, DPL), although INC DPTR instructions will automatically carry over to DPP, or as three independent 8-bit registers (DPP, DPH, DPL).
The ADuC845 supports dual data pointers. Refer to the Dual Data Pointer section later in this datasheet.

Stack Pointer (SP and SPH)
The SP SFR is the stack pointer and is used to hold an internal RAM address that is called the 'top of the stack.' The SP register is incremented before data is stored during PUSH and CALL executions. While the Stack may reside anywhere in on-chip RAM, the SP register is initialized to 07H after a reset. This causes the stack to begin at location 08H.
As mentioned earlier the ADuC845 offers an extended 11-bit stack pointer. The 3 extra bits to make up the 11-bit stack pointer are the 3 LSBs of the SPH byte located at B7h. To enable the SPH SFR the EXSP (CFG845.7) bit must be set otherwise the SPH SFR cannot be read or written to.

Program Status Word (PSW)
The PSW SFR contains several bits reflecting the current status of the CPU as detailed in Table I.

SFR Address	D0H
Power ON Default Value	00H
Bit Addressable	Yes

Table I. PSW SFR Bit Designations

Bit	Name	Description
7	CY	Carry Flag
6	AC	Auxiliary Carry Flag
5	F0	General-Purpose Flag
4	RS1	Register Bank Select Bits
3	RS0	RS1 RS0 Selected Bank 0 0 0 0 1 1 1 0 2 1 1 3
2	OV	Overflow Flag
1	F1	General-Purpose Flag
0	P	Parity Bit

Power Control Register (PCON)
The PCON SFR contains bits for power-saving options and general-purpose status flags as shown in Table II.

SFR Address	87H
Power ON Default Value	00H
Bit Addressable	No

Table II. PCON SFR Bit Designations

Bit	Name	Description
7	SMOD	Double UART Baud Rate
6	SERIPD	SPI Power-Down Interrupt Enable
5	INT0PD	INT0 Power-Down Interrupt Enable
4	ALEOFF	Disable ALE Output
3	GF1	General-Purpose Flag Bit
2	GF0	General-Purpose Flag Bit
1	PD	Power-Down Mode Enable
0	IDL	Idle Mode Enable

845 Configuration Register (CFG845)
The CFG845 SFR contains the necessary bits to configure the internal XRAM and the extended SP. By default it configures the user into 8051 mode. i.e. extended SP is disabled, internal XRAM is disabled.

SFR Address	AFhH
Power ON Default Value	00H
Bit Addressable	No

Table III. CFG845 SFR Bit Designations

Bit	Name	Description
7	EXSP	Extended SP Enable. If this bit is set to 1 then the stack will rollover from SPH/SP = 00FFh to 0100h. If this bit is cleared to 0 then the SPH SFR will be disabled and the stack will rollover from SP=FFh to SP =00h
6	----	----
5	----	----
4	----	----
3	----	----
2	----	----
1	----	----
0	XRAMEN	XRAM Enable Bit If this bit is set to 1 then the internal XRAM will be mapped into the lower 2kBytes of the external address space. If this bit is cleared to 0 then the internal XRAM will not be accessible and the external data memory will be mapped into the lower 2kBytes of external data memory. (see figure 3).

ADC CIRCUIT INFORMATION

The ADuC845 incorporates two (Primary & Auxiliary) 10-channel (8-channel on the MQFP package) 24-bit Σ–Δ ADCs. It also includes an on-chip programmable gain amplifier and digital filtering intended for the measurement of wide dynamic range, low frequency signals such as those in weigh-scale, strain-gauge, pressure transducer, or temperature measurement applications.

The ADuC845 can be configured as four/five fully-differential input channels or as eight/ten pseudo-differential input channels referenced to AINCOM. The primary ADC can be fully buffered internally or can have internal buffering disabled, and can be programmed for one of eight input ranges from ±20 mV to ±2.56V (Vref x 1.024). Buffering the input channel means that the part can handle significant source impedances on the analog input and that R,C filtering (for noise rejection or RFI reduction) can be placed on the analog inputs if required. These input channels are intended to convert signals directly from sensors without the need for external signal conditioning. With internal buffering disabled (relevant bits set/cleared in ADC0CON1) external buffering may be required.
When internal buffer is enabled it will be necessary to offset the negative input channel by 100mV to account for the restricted common-mode input range in the buffer. Internal buffering is not available on the Auxiliary ADC. The Auxiliary ADC is fixed at a gain range of ±2.56V.

Both ADCs employ a sigma-delta conversion technique to realize up to 24 bits of no missing codes performance (20Hz update rate, chop enabled). The sigma-delta modulator converts the sampled input signal into a digital pulse train whose duty cycle contains the digital information. A $Sinc^3$ programmable low-pass filter is then employed to decimate the modulator output data stream to give a valid data conversion result at programmable output rates. The signal chain has two modes of operation, CHOP enabled and CHOP disabled. The CHOP bit in the ADCMODE register enables and disables the chopping scheme.

Signal Chain Overview (CHOP Enabled, CHOP = 0)

With CHOP =0, chopping is enabled, this is the default and gives optimum performance in terms of drift performance. With chopping enabled, the available output rates vary from 5.35 Hz to 105 Hz. A block diagram of the ADC input channel with chop enabled is shown in Figure 7.
The sampling frequency of the modulator loop is many times higher than the bandwidth of the input signal. The integrator in the modulator shapes the quantization noise (which results from the analog-to-digital conversion) so that the noise is pushed toward one-half of the modulator frequency. The output of the sigma-delta modulator feeds directly into the digital filter. The digital filter then band-limits the response to a frequency significantly lower than one-half of the modulator frequency. In this manner, the 1-bit output of the comparator is translated into a band limited, low noise output from the ADuC845 ADC.
The ADuC845 filter is a low-pass, $Sinc^3$ or $(sinx/x)^3$ filter whose primary function is to remove the quantization noise introduced at the modulator. The cut-off frequency and decimated output data rate of the filter are programmable via the SF word loaded in the filter register. The complete signal chain is chopped resulting in excellent dc offset and offset drift specifications and is extremely beneficial in applications where drift, noise rejection, and optimum EMI rejection are important factors.

With chopping, the ADC repeatedly reverses its inputs. The decimated digital output words from the $Sinc^3$ filter, therefore, have a positive offset and negative offset term included. As a result, a final summing stage is included so that each output word from the filter is summed and averaged with the previous filter output to produce a new valid output result to be written to the ADC data register. The programming of the $Sinc^3$ decimation factor is restricted to an 8-bit register called SF, the actual decimation factor is the register value times 8. The decimated output rate from the $Sinc^3$ filter (and the ADC conversion rate) will therefore be:

$$f_{ADC} = \frac{1}{3} \times \frac{1}{8 \times SF} \times f_{MOD}$$

where
f_{ADC} in the ADC conversion rate.
SF is the decimal equivalent of the word loaded to the filter register.
f_{MOD} is the modulator sampling rate of 32.768 kHz.

The chop rate of the channel is half the output data rate:

$$f_{CHOP} = \frac{1}{2 \times f_{ADC}}$$

As shown in the block diagram, the $Sinc^3$ filter outputs alternately contain $+V_{OS}$ and $-V_{OS}$, where V_{OS} is the respective channel offset. This offset is removed by performing a running average of two. This average by two means that the settling time to any change in programming of the ADC will be twice the normal conversion time, while an asynchronous step change on the analog input will not be fully reflected until the third subsequent output.

$$t_{SETTLE} = \frac{2}{f_{ADC}} = 2 \times t_{ADC}$$

The allowable range for SF (Chop Enabled) is 13 to 255 with a default of 69 (45H). The corresponding conversion rates, RMS and Pk-Pk noise performances are shown in Table IV & Table V. Note that the conversion time increases by 0.732 ms for each increment in SF.

With chopping enabled the ADC noise performance is the same as that of the ADuC834.

TABLE IV: Typical Output rms noise (μV) vs Input Range and Update Rate for the ADuC845 with chopping Enabled.

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
13	105.03	1.50	1.50	1.60	1.75	3.50	4.50	6.70	11.75
69	19.79	0.60	0.65	0.65	0.65	0.65	0.95	1.40	2.30
255	5.35	0.35	0.35	0.37	0.37	0.37	0.51	0.82	1.25

TABLE V: Peak to Peak Resolution (bits) vs Input Range and Update Rate for the ADuC845 with chopping Enabled.

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
13	105.03	12	13	14	15	15	15.5	16	16
69	19.79	13.5	14	15	16	17	17.5	18	18.5
255	5.35	14	15	16	17	18	18.5	19	19.5

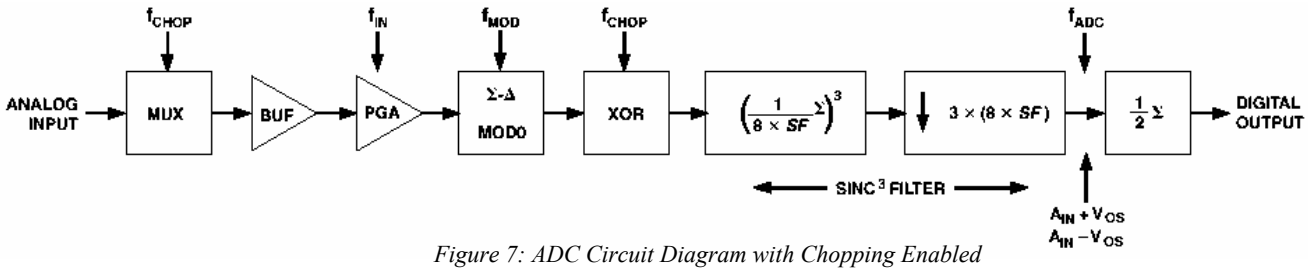


Figure 7: ADC Circuit Diagram with Chopping Enabled

Signal Chain Overview (CHOP Disabled, CHOP = 1)

With CHOP =1 chopping is disabled. With chopping disabled the available output rates vary from 16.06 Hz to 1.365 kHz .The range of applicable SF words is from 3 to 255. When switching between channels with chop disabled, the channel throughput rate is increased over the case where chop is enabled. The drawback with chop disabled is that the drift performance is degraded and calibration is required following a gain change or significant temperature change. A block diagram of the ADC input channel with chop disabled is shown in Figure 8. The signal chain includes a multiplexor, buffer, PGA, sigma-delta modulator, and digital filter. The modulator bit stream is applied to a Sinc^3 filter. The programming of the Sinc^3 decimation factor is restricted to an 8-bit register SF, the actual decimation factor is the register value times 8. The decimated output rate from the Sinc^3 filter (and the ADC conversion rate) will therefore be:

$$f_{ADC} = \frac{1}{8 \times SF} \times f_{MOD}$$

where

f_{ADC} is the ADC conversion rate,

SF is the decimal equivalent of the word loaded to the filter register, valid range is from 3 to 255,

f_{MOD} is the modulator sampling rate of 32.768 kHz.

The settling time to a step input is governed by the digital filter. A synchronized step change will require a settling time of three times the programmed update rate, a channel change can be treated as a synchronized step change. This means that following a synchronized step change, the ADC will require three outputs before the result accurately reflects the new input voltage.

$$t_{SETTLE} = \frac{3}{f_{ADC}} = 3 \times t_{ADC}$$

An unsynchronized step change will require four outputs to accurately reflect the new analog input at its output.

The allowable range for SF is 3 to 255 with a default of 69 (45H). The corresponding conversion rates, RMS and Pk-Pk noise performances are shown in Table VI & Table VII. Note that the conversion time increases by 0.244 ms for each increment in SF.

ADC NOISE PERFORMANCE WITH CHOPPING DISABLED

Tables VI and VII show the output rms noise and output peak-to-peak resolution in bits (rounded to the nearest 0.5 LSB) for some typical output update rates. The numbers are typical and generated at a differential input voltage of 0V. The output update rate is selected via the SF7–SF0 bits in the SF Filter Register. It is important to note that the peak-to-peak resolution figures represent the resolution for which there will be no code flicker within a six-sigma limit. The output noise comes from two sources.The first is the electrical noise in the semiconductor devices (device noise) used in the implementation of the modulator. Secondly, when the analog input is converted to the digital domain, quantization noise is added. The device noise is at a low level and is independent of frequency. The quantization noise starts at an even lower level but rises rapidly with increasing frequency to become the dominant noise source. The numbers in the tables are given for the bipolar input ranges. For the unipolar ranges the rms noise numbers will be the same as the bipolar range, but the peak-to-peak resolution is now based on half the signal range which effectively means losing 1 bit of resolution. Typically, the performance of the ADC with Chop disabled will show a 1LSB degradation over the performance with Chop enabled.

TABLE VI: Typical Output rms noise (μV) vs Input Range and Update Rate for the ADuC845 with chopping disabled.

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
3	1365.0	2.47	2.49	2.37	3.87	7.18	12.61	16.65	32.45
69	59.36	0.961	0.971	0.949	0.922	0.923	1.32	2.03	3.73
255	16.06	0.475	0.468	0.434	0.485	0.458	0.688	1.18	1.78

TABLE VII: Peak to Peak Resolution (bits) vs Input Range and Update Rate for the ADuC845 with chopping disabled.

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
3	1365.0	11	12	14	14	14	14	15	15
69	59.36	13	14	15	16	17	17	18	18
255	16.06	14	15	16	17	18	18	19	19

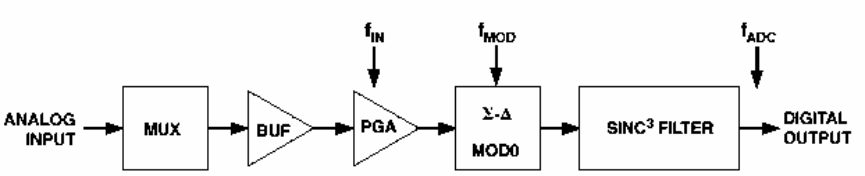


Figure: 8 ADC Circuit with CHOP disabled

Table VIII Auxiliary ADC

Typical Output RMS Noise vs Update Rate*
Output RMS Noise in μV

SF Word	Data Update Rate (Hz)	Input Range 2.5v
13	105.3	10.75
69	19.79	2.00
255	5.35	1.15

* ADC converting in Bipolar Mode

Peak-to-Peak Resolution vs. Update Rate[1]
Peak-to-Peak Resolution in Bits

SF Word	Data Update Rate (Hz)	Input Range 2.5v
13	105.3	16[2]
69	19.79	16
255	5.35	16

[1] ADC converting in Bipolar Mode
[2] In Unipolar mode, peak-to-peak resolution at 105Hz is 15 bits

Reference Inputs

The ADuC845 has two separate differential reference inputs REFIN+/- and REFIN2+/-. While both references are available for use with the primary ADC only the REFIN+/- is available for the auxiliary ADC. The common mode range for these differential references is from AGND to AV_{DD}. The nominal external reference voltage is 2.5v, with the primary and auxiliary reference select bits configured from the ADC0CON2 and ADC1CON respectively.

The ADuC845 can also be configured to use the on-chip band-gap reference, via the XREF0/1 bits in the ADC0CON2 SFR (for primary ADC) or the AXREF bit in ADC1CON (for auxiliary ADC). In this mode of operation the ADCs will see the internal reference of 1.25v, thereby halving all the input ranges. A consequence of using the internal bandgap reference is a noticable degradation in peak-to-peak resolution. For this reason operation with an external reference is strongly recommended.
In applications where the excitation (voltage or current) for the transducer on the analog input also drives the reference inputs for the part, the effect of the of any low frequency noise in the excitation source will be removed as the application is retiometric. If the ADuC845 is not used in a ratiometric configuration then a low noise reference should be used. Recommended references voltage sources for the ADuC845 include ADR421, REF43, REF192.

It should also be noted that the reference inputs provide a high impedance, dynamic load to external connections. Because the impedance of each reference input is dynamic, resistor/capacitor combinations on these pins can cause dc gain errors depending on the output impedance of the source that is driving the referenc inputs. Reference voltage sources, like those mentioned above (e.g. ADR421), will typically have low output impedances and therefore decoupling capacitors of the REFIN+/- or REFIN2+/- inputs would be recommended. Deriving the reference voltage from an external resistor configuration will mean that the reference input sees a significant external source impedance. External decoupling of the REFIN+/- and/or REFIN2+/- inputs would not be recommended in this type of configuration.

Burnout Current Sources
The Primary ADC on the ADuC845 incorporates two 200uA constant current generators, one sourcing current from the AV_{DD} to AIN(+), and one sinking current from AIN(-) to AGND. These currents are only configurable for use on AIN4 → AIN5 and/or AIN6 → AIN7 in differential mode only, from the BO bit in the ICON SFR. These burnout current sources are also only available with full buffering enabled via the BUF0/BUF1 bits in the ADC0CON1 SFR. Once the burnout currents are turned on, a current will flow in the external transducer circuit, and a measurement of the input voltage on the analog input channel can be taken. If the resulting voltage measured is fullscale, it indicates that the transducer has gone open-circuit. If the voltage measured is 0v, it indicates that the transducer has gone short circuit. The current sources work over the normal absolute input voltage range specifications.

Reference Detect Circuit
The main and auxiliary ADC's have the option of using the internal bandgap reference or an external reference applied to the two REFIN pins, by means of the XREF0/1 bits in their respective control registers AD0CON2 and AD1CON. A reference detection circuit is provided to detect whether there is a valid voltage applied to the REFIN+/- pins. This feature arose in connection with strain gauge sensors in weigh-scales where the reference and signal are provided via a cable from the remote sensor. It is desirable to detect whether the cable is disconnected. If either of the pins is floating or if the applied voltage is below a specified threshold then a flag (NOXREF) is set in the ADC status register (ADCSTAT), conversion results are clamped and calibration registers are not updated if a calibration is in progress.
Note: the reference-detect does not look at Refin2+/-.

If, during either an offset or gain calibration, the NOEXREF bit becomes active indicating a incorrect Vref, then the updating of the relevant calibration register is inhibited to avoid loading incorrect data into these registers. The appropriate bits in ADCSTAT (ERR0 or ERR1) get set. If the user is concerned about verifying that a valid reference is in place every time a calibration is performed, the status of the ERR0 and ERR1 bits should be checked at the end of every calibration cycle.

Sinc Filter Register (SF)
The number entered into this register sets the decimation factor of the $Sinc^3$ Filter for the ADC.
The range of operation of the SF word depends on whether ADC Chop is on or off. With Chop off the minimum SF word is 3 and the maximum is 255. This gives an ADC throughput rate from 16.06 Hz to 1.365kHz. With Chop on the minimum SF word is 13 (all values lower than 13 are clamped to 13) and the maximum is 255. This gives an ADC throughput rate from 5.4Hz to 105Hz. See f_{adc} equations in the ADC description section above.
There is one additional feature of the $Sinc^3$ Filter, and that is a second notch filter positioned in the frequency response at 60Hz. This gives simultaneous 50Hz & 60Hz rejection. This 60Hz filter is enabled via the REJ60 bit in the ADCMODE register ADCMODE.6). This notch is only valid for SF words ≥ 68, otherwise ADC errors will occur. This function is only useful with an ADC clock of 32.768kHz. During Calibration the current (user written) value of the SF register is used.

Σ-Δ Modulator
A Σ-Δ ADC generally consists of two main blocks, an analog modulator and a digital filter. In the case of the ADuC845, the analog modulator consists of a difference amplifier, an integrator block, a comparator and a feedback DAC as illustrated in Fig 9

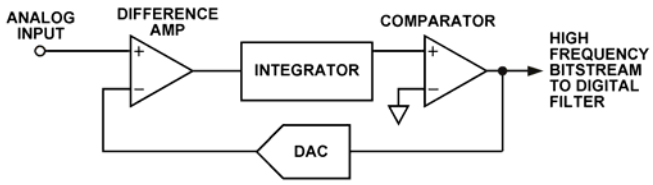


Fig. 9 Σ-Δ Modulator Simplified Block Diagram

In operation, the analog signal is fed to the difference amplifier along with the output from the feedback DAC. The difference between these two signals is integrated and fed to the comparator. The output from the comparator provides the input to the feedback DAC so the system finctions as a negative feedback loop that tries to minimize the difference signal. The digital data that represents the analog input voltage is contained in the duty cycle of the pulse train appearing at the output of the comparator. This duty cycle data can be recovered as a data-word using a subsequent digital filter stage. The sampling frequency of the modulator loop is many times higher than the bandwidth of the input signal. The integrator in the modulator shapes the quantization noise (which results from the analog-to-digital conversion) so that the noise is pushed toward one- half of the modulator frequency.

Digital Filter
The output of the Σ-Δ modulator feeds directly into the digital filter. The digital filter then band-limits the response to a frequency significantly lower than one-half of the modulator frequency. In this manner , the 1-bit output of the comparator is translated into a band-limited, low noise output from the ADuC845 ADCs.

The ADuC845 filter is a low-pass, $Sinc^3$ or $[(SIN\ x)/x]^3$ filter whose primary function is to remove the quantization noise introduced at the modulator. The cutoff frequency and decimated output data rate of the filter are programmable via the SF (Sinc Filter) SFR as described in Table XV and Table XVI.

Figs 10, 11, 12, 13 show the frequency response of the ADC. yielding and overall output rate of 16.6Hz with chop enabled and 50Hz with chop disabled. Also detailed in these plots is the effect of the fixed 60Hz drop-in notch filter. This fixed filter can be enabled or disabled by setting or clearing the REJ60 bit in the ADCMODE register (ADCMODE.6). This 60Hz drop-in notch filter can be enabled for any SF word that yields an ADC throughput that is less than 60Hz (i.e. SF ≥ 69 decimal).

ADC Chopping
Both ADCs on the ADuC845 implement a chopping scheme whereby the ADC repeatedly reverses its inputs. The decimated digital output words from the Sinc3 filter therefore have a positive and negitive offset term included.

As a result, a final summing stage is included in each ADC so that each output word from the filter is summed and averaged with the previous filter output to produce a new valid output result to be

written to the ADCdata SFRs. In this way, while the ADC throughput or update rate is as discussed in Table XV, the time to a valid first result is actually going to be 2 x Tadc.

The chopping scheme incorporated into the ADuC845 results in excellent dc offset and offset drift specifications and is extremely beneficial in applications where drift, noise rejection and optimum EMI rejection are important factors.

ADC chop can be disabled via the Chop bit in the ADCMODE SFR (ADCMODE.3). Setting this bit to a 1 (logic high) disables Chop mode.

Calibration

The ADuC845 incorporates four different calibration modes that can be programmed via the mode bits in the ADCMODE SFR detailed in Table X. Every ADuC845 is calibrated before it leaves the factory. The resulting offset and gain calibration coefficients for both the primary and auxiliary ADCs are stored on-chip in manufacturing–specific Flash/EE memory locations. At powerup or after a reset, these factory calibration registers are automatically downloaded to the ADC calibration registers in the ADuC845 SFR space. Each of the promary and auxiliary ADCs have dedicated calibration SFRs associated which are described in the section ADC SFR INTERFACE**.** However,these factory downloaded calibration values in the ADC calibration SFRs will be overwritten if any one of the four calibration options are initiated and that the ADC is enabled via the ADC enable bits in ADCMODE.

Even though an internal offset calibration mode is described below, it should be recognized that both ADCs are chopped. This chopping scheme inherently minimizes offset and means that an internal offset calibration should never be required. Also, because factory 5V/25°C gain calibration coefficients are automatically present at power-on, an internal full-scale calibration will only be required if the part is being operated at 3V or at temperatures significantly different from 25°C.

The ADuC845 offers “internal” or “system” calibration facilities. For full calibration to occur on the selected ADC, the calibration logic must record the modulator output for two different input conditions. These are “zero-scale” and “full-scale” points. These points are derived by performing a conversion on the different input voltages (zero-scale & full-scale) provided to the input of the modulator during calibration. The result of the “zero-scale” calibration conversion is stored in the Offset Calibration Registers for the appropriate ADC. The result of the “full-scale” calibration conversion is stored in the Gain Calibration Registers for the appropriate ADC. With these readings, the calibration logic can calculate the offset and the gain slope for the input-to-output transfer function of the converter.

During an “internal” zero-scale or full-scale calibration, the respective “zero” input and “full-scale” input are automatically connected to the ADC input pins internally to the device. A “system” calibration, however, expects the system zero-scale and system full-scale voltages to be applied to the external ADC pins before the calibration mode is initiated. In this way, external ADC errors are taken into account and minimized as a result of system calibration. It should also be noted that all ADuC845 ADC calibrations are carried out at the user selected SF word update rate. In order to optimize calibration accuracy it is recommended that the slowest possible update rate be used.

Internally in the ADuC845, the coefficients are normalized before being used to scale the words coming out of the digital filter. The offset calibration coefficient is subtracted from the result prior to the multiplication by the gain coefficient.
From an operational point of view, a calibration should be treated like another ADC conversion. A zero-scale calibration (if required) should always be carried out before a full-scale calibration. System software should monitor the relevant ADC RDY0/1 Bit in the ADCSTAT SFR to determine end of calibration via a polling sequence or interrupt driven routine.

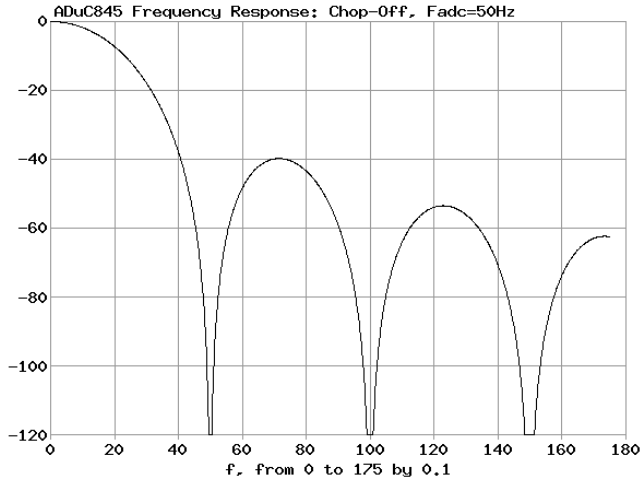


Fig 10

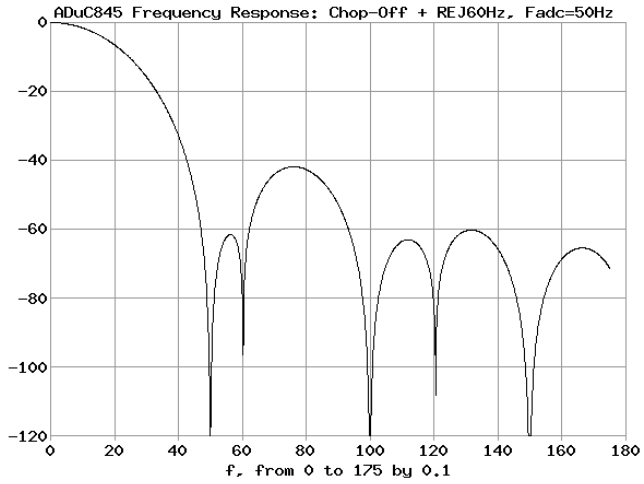


Fig 11

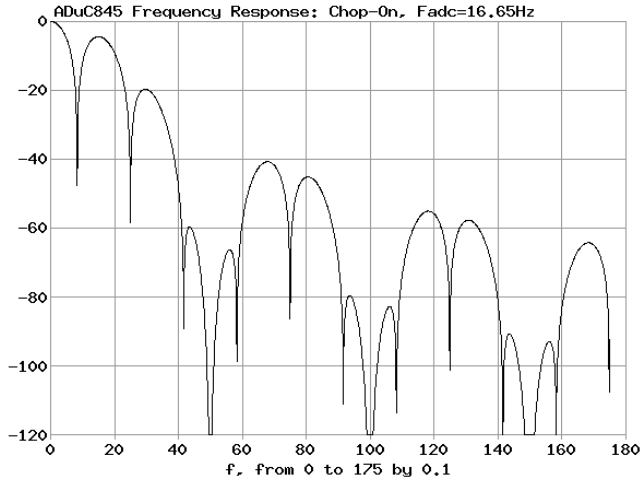


Fig 12

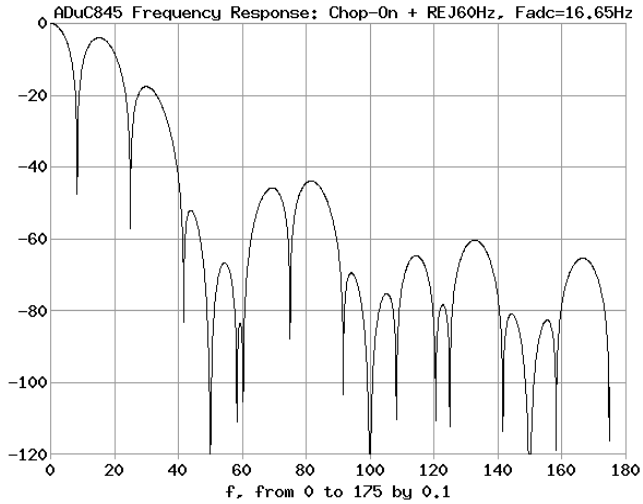


Fig 13

The above plots show the effect of Chop mode and the rej60 Hz filter at 16Hz and 50Hz ADC throughput rates.

Plot 10 ...Fadc = 50Hz, Chop = OFF, REJ60 bit cleared : Good 50Hz rejection, poor 60Hz rejection
Plot 11 ...Fadc = 50Hz, Chop = OFF, REJ60 bit set : Good 50Hz and 60Hz rejection (>67db at 60Hz +/- 1Hz)
Plot 12 ...Fadc = 16.6Hz, Chop = ON, REJ60 bit cleared : Good 50Hz rejection, poor 60Hz rejection)
Plot 13 ...Fadc = 16.6Hz, Chop = ON, REJ60 bit set : Good 50Hz and 60Hz rejection (> 75db at 60Hz +/-1Hz)

ADC SFR INTERFACE

Both ADCs are controlled and configured via a number of SFRs that are mentioned here and described in more detail in the following pages.

ADCSTAT: ADC Status Register. Holds general status of the Primary and Auxiliary ADCs.
ADCMODE: ADC Mode Register. Controls general modes of operation for Primary and Auxiliary ADCs.
ADC0CON1: Primary ADC Control Register 1. Controls specific configuration of Primary ADC.
ADC0CON2: Primary ADC Control Register 2. Controls specific configuration of Primary ADC.
ADC1CON: Auxiliary ADC Control Register. Controls specific configuration of Auxiliary ADC.
SF: Sinc Filter Register. Configures the decimation factor for the $Sinc^3$ filter and thus the Primary and Auxiliary ADC update rates.
ICON: Current Source Control Register. Allows user control of the various on-chip current source options.
ADC0L/M/H: Primary ADC 24-bit conversion result is held in these three 8-bit registers.
ADC1L/M/H: Auxiliary ADC 24-bit conversion result is held in these two 8-bit registers.
OF0L/M/H: Primary ADC 24-bit Offset Calibration Coefficient is held in these three 8-bit registers.
OF1L/H: Auxiliary ADC 16-bit Offset Calibration Coefficient is held in these two 8-bit registers.
GN0L/M/H: Primary ADC 24-bit Gain Calibration Coefficient is held in these three 8-bit registers.
GN1L/H: Auxiliary ADC 16-bit Gain Calibration Coefficient is held in these two 8-bit registers.

ADCSTAT—(ADC Status Register)

This SFR reflects the status of both ADCs including data ready, calibration, and various (ADC-related) error and warning conditions including Refin+/- reference detect and conversion overflow/underflow flags.

SFR Address D8H
Power-On Default Value 00H
Bit Addressable Yes

Table IX. ADCSTAT SFR Bit Designations

Bit	Name	Description
7	RDY0	Ready Bit for Primary ADC. *Set* by hardware on completion of ADC conversion or calibration cycle. *Cleared* directly by the user or indirectly by write to the mode bits to start another Primary ADC conversion or calibration. The Primary ADC is inhibited from writing further results to its data or calibration registers until the RDY0 bit is cleared.
6	RDY1	Ready Bit for Auxiliary ADC. Same definition as RDY0 referred to the Auxiliary ADC.
5	CAL	Calibration Status Bit. *Set* by hardware on completion of calibration. *Cleared* indirectly by a write to the mode bits to start another ADC conversion or calibration.
4	NOXREF	No External Reference Bit *(only active if Primary or Auxiliary ADC is active).* *Set* to indicate that one or both of the REFIN pins is floating or the applied voltage is below a specified threshold. When Set, conversion results are clamped to all ones. Only detects invalid Refin+/-, does not check Refin2+/-. *Cleared* to indicate valid VREF.
3	ERR0	Primary ADC Error Bit. *Set* by hardware to indicate that the result written to the Primary ADC data registers has been clamped to all zeros or all ones. After a calibration, this bit also flags error conditions that caused the calibration registers not to be written. *Cleared* by a write to the mode bits to initiate a conversion or calibration.
2	ERR1	Auxiliary ADC Error Bit. Same definition as ERR0 referred to the Auxiliary ADC.
1	___	Reserved for Future Use
0	___	Reserved for Future Use

ADCMODE (ADC Mode Register)
Used to control the operational mode of both ADCs.
SFR Address D1H
Power-On Default Value 10H
Bit Addressable No

Table X. ADCMODE SFR Bit Designations

Bit	Name	Description
7	——	Reserved for Future Use
6	REJ60	Automatic 60 Hz notch select bit. Setting this bit will place a notch in the frequency response at 60Hz, allowing simultaneous 50 & 60Hz rejection at an SF word of 82. This 60Hz notch can only be set if SF ≥ 68. This second notch is only placed at 60Hz if the ADC clock is at 32.768kHz.
5	ADC0EN	Primary ADC Enable. *Set* by the user to enable the Primary ADC and place it in the mode selected in MD2–MD0 below. *Cleared* by the user to place the Primary ADC in power-down mode.
4	ADC1EN	Auxiliary ADC Enable. *Set* by the user to enable the Auxiliary ADC and place it in the mode selected in MD2–MD0 below. *Cleared* by the user to place the Auxiliary ADC in power-down mode.
3	CHOP	Chop Mode Disable *Set* by the user to disable Chop Mode on both the Primary and Auxiliary ADC allowing greater ADC data throughput . *Cleared* by the user to enable Chop Mode on both the Primary and Auxiliary ADC.
2	MD2	Primary and Auxiliary ADC Mode bits. These bits select the operational mode of the enabled ADC as follows:
1	MD1	MD2 MD1 MD0
0	MD0	0 0 0 ADC Power-Down Mode (Power-On Default)
		0 0 1 Idle Mode. In Idle Mode, the ADC filter and modulator are held in a reset state although the modulator clocks are still provided.
		0 1 0 Single Conversion Mode In Single Conversion Mode, a single conversion is performed on the enabled ADC. On completion of a conversion, the ADC data registers(ADC0H/M/L and/or ADC1H/M/L) are updated. The relevant flags in the ADCSTAT SFR are written, and power-down is re-entered with the MD2–MD0 accordingly being written to 000.
		0 1 1 Continuous Conversion In Continuous Conversion Mode, the ADC data registers are regularly updated at the selected update rate (see SF Register).
		1 0 0 Internal Zero-Scale Calibration Internal short automatically connected to the enabled ADC input(s)
		1 0 1 Internal Full-Scale Calibration Internal or External REFIN+/- or REFIN2+/- VREF(as determined by XREF bits in ADC0CON2 and/or AXREF in ADC1CON) is automatically connected to the enabled ADC input(s) for this calibration.
		1 1 0 System Zero-Scale Calibration User should connect system zero-scale input to the enabled ADC input(s) as selected by CH3-CH0 and ACH3-ACH0 bits in the ADC0CON2 and ADC1CON Registers.
		1 1 1 System Full-Scale Calibration User should connect system full-scale input to the enabled ADC input(s) as selected by CH3-CH0 and ACH3-ACH0 bits in the ADC0CON2 and ADC1CON Registers.

NOTES
1. Any change to the MD bits will immediately reset both ADCs. A write to the MD2–0 Bits with no change is also treated as a reset. (See exception to this in Note 3 below.)
2 If ADC0CON is written when ADC0EN = 1, or if ADC0EN is changed from 0 to 1, then both ADCs are also immediately reset. In other words, the Primary ADC is given priority over the Auxiliary ADC and any change requested on the primary ADC is immediately responded to.
3. On the other hand, if ADC1CON is written or if ADC1EN is changed from 0 to 1, only the Auxiliary ADC is reset. For example, if the Primary ADC is continuously converting when the Auxiliary ADC change or enable occurs, the primary ADC continues undisturbed. Rather than allow the Auxiliary ADC to operate with a phase difference from the primary ADC, the Auxiliary ADC will fall into step with the outputs of the primary ADC. The result is that the first conversion time for the Auxiliary ADC will be delayed up to three outputs while the Auxiliary ADC update rate is synchronized to the Primary ADC.
4. Once ADCMODE has been written with a calibration mode, the RDY0/1 bits (ADCSTAT) are reset and the calibration commences. On completion, the appropriate calibration registers are written, the relevant bits in ADCSTAT are written, and the MD2–0 bits are reset to 000 to indicate the ADC is back in power-down mode.
5. Any calibration request of the Auxiliary ADC while the temperature sensor is selected will fail to complete. Although the RDY1 bit will be set at the end of the calibration cycle, no update of the calibration SFRs will take place and the ERR1 bit will be set.
6. Calibrations are performed at maximum SF (see SF SFR) value guaranteeing optimum calibration operation.

ADC0CON1 (Primary ADC Control Register)
ADC0CON is used to configure the Primary ADC for Buffer, unipolar or bipolar coding and ADC range configuration.

ADC0CON1 Primary ADC Control SFR
SFR Address D2H
Power-On Default Value 07H
Bit Addressable No

Table XI. ADC0CON1 SFR Bit Designations

Bit	Name	Description
7	BUF1	Buffer Configuration Bits
6	BUF0	BUF1 BUF0 Buffer Configuration 0 0 ADC0+ and ADC0- are buffered 0 1 Reserved For Future Use 1 0 Buffer Bypass 1 1 Reserved for Future Use.
5	UNI	Primary ADC Unipolar Bit. *Set* by user to enable unipolar coding, i.e., zero differential input will result in 0x000000 output. *Cleared* by user to enable bipolar coding, zero differential input will result in 0x800000 output.
4	——	Reserved for Future Use
3	——	Reserved for Future Use
2	RN2	Primary ADC Range Bits. Written by the user to select the Primary ADC input range as follows:
1	RN1	RN2 RN1 RN0 Selected Primary ADC Input Range (VREF = 2.5 V)
0	RN0	0 0 0 ±20 mV (0 mV–20 mV in Unipolar Mode) 0 0 1 ±40 mV (0 mV–40 mV in Unipolar Mode) 0 1 0 ±80 mV (0 mV–80 mV in Unipolar Mode) 0 1 1 ±160 mV (0 mV–160 mV in Unipolar Mode) 1 0 0 ±320 mV (0 mV–320 mV in Unipolar Mode) 1 0 1 ±640 mV (0 mV–640 mV in Unipolar Mode) 1 1 0 ±1.28 V (0 V–1.28 V in Unipolar Mode) 1 1 1 ±2.56 V (0 V–2.56 V in Unipolar Mode)

ADC0CON2 (Primary ADC Channel Select Register)
ADC0CON2 is used to select the channel for the Primary ADC

ADC0CON2 Primary ADC Channel Select Register
SFR Address E6H
Power-On Default Value 00H
Bit Addressable No

Table XII. ADC0CON2 SFR Bit Designations

Bit	Name	Description
7	XREF1	Primary ADC External Reference Select Bit.
6	XREF0	*Set* by user to enable the Primary ADC to use the external reference via REFIN+/- or REFIN2+/-. *Cleared* by user to enable the Primary ADC to use the internal bandgap reference (VREF = 1.25 V). XREF1 XREF0 0 0 Internal 1.25v Vref 0 1 Refin+/- 1 0 Refin2+/- (Ain2 / Ain3) 1 1 Reserved for Future Use
5	——	Reserved for Future Use
4	——	Reserved for Future Use
3	CH3	Primary ADC Channel Select Bits. Written by the user to select the Primary ADC Channel as follows
2	CH2	CH3 CH2 CH1 CH0 Selected Primary ADC Input Channel.
1	CH1	0 0 0 0 AIN1 → AINCOM
0	CH0	0 0 0 1 AIN2 → AINCOM
		0 0 1 0 AIN3 → AINCOM
		0 0 1 1 AIN4 → AINCOM
		0 1 0 0 AIN5 → AINCOM
		0 1 0 1 AIN6 → AINCOM
		0 1 1 0 AIN7 → AINCOM
		0 1 1 1 AIN8 → AINCOM
		1 0 0 0 AIN9 → AINCOM (CSP package only). Not a valid selection on MQFP package.
		1 0 0 1 AIN10 → AINCOM (CSP package only). Not a valid selection on MQFP package.
		1 0 1 0 AIN1 → AIN2
		1 0 1 1 AIN3 → AIN4
		1 1 0 0 AIN5 → AIN6
		1 1 0 1 AIN7 → AIN8
		1 1 1 0 AIN9 → AIN10 (CSP package only). Mot a valid selection on MQFP package.
		1 1 1 1 AINCOM → AINCOM

ADC1CON (Auxiliary ADC Control Register)
ADC1CON is used to configure the Auxiliary ADC for reference and channel selection and unipolar or bipolar coding.

ADC1CON Auxiliary ADC Control SFR

SFR Address	D3H
Power-On Default Value	00H
Bit Addressable	No

Table XIII. ADC1CON SFR Bit Designations

Bit	Name	Description
7	——	Reserved for Future Use
6	AXREF	Auxiliary ADC External Reference Bit. *Set* by user to enable the Auxiliary ADC to use the external reference via REFIN(+)/REFIN(–). *Cleared* by user to enable the Auxiliary ADC to use the internal bandgap reference.
5	AUNI	Auxiliary ADC Unipolar Bit. *Set* by user to enable unipolar coding, i.e., zero input will result in 0x000000 output. *Cleared* by user to enable bipolar coding, zero input will result in 0x800000 output.
4	——	Reserved for Future Use
3	ACH3	Auxiliary ADC Channel Select Bits. Written by the user to select the Auxiliary ADC Channel
2	ACH2	ACH3 ACH2 ACH1 ACH0 Selected Auxiliary ADC Input Range (VREF = 2.5 V)
1	ACH1	0 0 0 0 AIN1 → AINCOM
0	ACH0	0 0 0 1 AIN2 → AINCOM
		0 0 1 0 AIN3 → AINCOM
		0 0 1 1 AIN4 → AINCOM
		0 1 0 0 AIN5 → AINCOM
		0 1 0 1 AIN6 → AINCOM
		0 1 1 0 AIN7 → AINCOM
		0 1 1 1 AIN8 → AINCOM
		1 0 0 0 AIN9 → AINCOM (CSP package only). Not a valid selection on MQFP package
		1 0 0 1 AIN10 → INCOM (CSP package only). Not a valid selection on MQFP package
		1 0 1 0 AIN1→ AIN2
		1 0 1 1 AIN3→ AIN4
		1 1 0 0 AIN5→ AIN6
		1 1 0 1 AIN7→ AIN8
		1 1 1 0 TEMPERATRE SENSOR[1, 2, 3.]
		1 1 1 1 AINCOM → AINCOM

NOTES
1. When the temperature sensor is selected, user code must select internal reference via AXREF bit above and clear the AUNI bit (ADC1CON.5) to select bipolar coding.
2. The temperature sensor is factory calibrated to yield conversion results 0x800000 at 0 °C (ADC Chop on).
3. A +1°C change in temperature will result in a +1 LSB change in the ADC1H Register ADC conversion result.

SF (ADC Sinc Filter Control Register)
The SF register is used to configure the decimation factor for the ADC, and as such has a direct influence on the ADC throughput rate.

Sinc Filter Control Register (SF)
SFR Address D4H
Power-On Default Value 45H
Bit Addressable No

Table XIV. Sinc Filter SFR Bit Designations

SF.7	SF.6	SF.5	SF.4	SF.3	SF.2	SF.1	SF.0
0	1	0	0	0	1	0	1

Setting the bits in this register sets the decimation factor of the ADC. This has a direct bearing on the throughput rate of the ADC along with the Chop setting. The two equations used to determine the ADC throughput rate are

Chop ON: $$Fadc\ (Chop\ ON) = \frac{1}{(3 \times 8 \times SFword)} \times 32.768kHz$$ (Where SFword is in decimal)

Chop OFF: $$Fadc\ (Chop\ OFF) = \frac{1}{(8 \times SFword)} \times 32.768kHz$$ (where SFword is in decimal)

Table XV. SF SFR bit examples

CHOP ENABLED (ADCMODE.3 = 0)			
SF (Decimal)	**SF (Hexadecimal)**	**Fadc (Hz)**	**Tadc (ms)**
13	0D	105.3	9.52
69	45	19.79	50.34
255	FF	5.35	186.77
CHOP DISABLED (ADCMODE.3 = 1)			
SF (Decimal)	**SF (Hexadecimal)**	**Fadc (Hz)**	**Tadc (ms)**
3	03	1365.3	0.73
69	45	59.36	16.84
255	FF	16.06	62.25

NONVOLATILE FLASH/EE MEMORY

Flash/EE Memory Overview

The ADuC845 incorporates Flash/EE memory technology on-chip to provide the user with nonvolatile, in-circuit reprogrammable, code and data memory space. Flash/EE memory is a relatively recent type of nonvolatile memory technology and is based on a single transistor cell architecture.
This technology is basically an outgrowth of EPROM technology and was developed through the late 1980s. Flash/EE memory takes the flexible in-circuit reprogrammable features of EEPROM and combines them with the space efficient/density features of EPROM. (See Figure 14).

Because Flash/EE technology is based on a single transistor cell architecture, a Flash memory array, like EPROM, can be implemented to achieve the space efficiencies or memory densities required by a given design.
Like EEPROM, Flash memory can be programmed in-system at a byte level, although it must first be erased; the erase being performed in page blocks. Thus, Flash memory is often and more correctly referred to as Flash/EE memory.

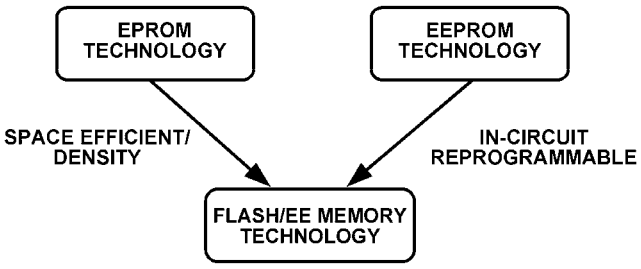


Fig. 14 Flash/EE Memory Development

Overall, Flash/EE memory represents a step closer to the ideal memory device that includes nonvolatility, in-circuit programmability, high density, and low cost. Incorporated in the ADuC845, Flash/EE memory technology allows the user to update program code space in-circuit, without the need to replace onetime programmable (OTP) devices at remote operating nodes.

Flash/EE Memory and the ADuC845

The ADuC845 provides two arrays of Flash/EE memory for user applications. 62 Kbytes of Flash/EE Program space are provided on-chip to facilitate code execution without any external discrete ROM device requirements. The program memory can be programmed in-circuit, using the serial download mode provided, using conventional third party memory programmers, or via any user defined protocol in User Download (ULOAD) Mode.

A 4 Kbyte Flash/EE Data Memory space is also provided on-chip. This may be used as a general-purpose, nonvolatile scratchpad area. User access to this area is via a group of seven SFRs. This space can be programmed at a byte level, although it must first be erased in 4-byte pages.

ADuC845 Flash/EE Memory Reliability

The Flash/EE Program and Data Memory arrays on the ADuC845 are fully qualified for two key Flash/EE memory characteristics, namely Flash/EE Memory Cycling Endurance and Flash/EE Memory Data Retention.

Endurance quantifies the ability of the Flash/EE memory to be cycled through many Program, Read, and Erase cycles. In real terms, a single endurance cycle is composed of four independent, sequential events. These events are defined as:

a. initial page erase sequence
b. read/verify sequence
c. byte program sequence
d. second read/verify sequence

} A single Flash/EE Memory Endurance Cycle

In reliability qualification, every byte in both the program and data Flash/EE memory is cycled from 00 hex to FFhex until a first fail is recorded, signifying the endurance limit of the on-chip Flash/EE memory.

As indicated in the specification pages of this data sheet, the ADuC845 Flash/EE Memory Endurance qualification has been carried out in accordance with JEDEC Specification A117 over the industrial temperature range of –40°C, +25°C, +85°C, and +125°C., (CSP is qualified to +85°C only) The results allow the specification of a minimum endurance figure over supply and temperature of 100,000 cycles, with an endurance figure of 700,000 cycles being typical of operation at 25°C.
Retention quantifies the ability of the Flash/EE memory to retain its programmed data over time. Again, the ADuC845 has been qualified in accordance with the formal JEDEC Retention Lifetime Specification (A117) at a specific junction temperature (T_J = 55°C). As part of this qualification procedure, the Flash/EE memory is cycled to its specified endurance limit described above, before data retention is characterized. This means that the Flash/EE memory is guaranteed to retain its data for its full specified retention lifetime every time the Flash/EE memory is reprogrammed. It should also be noted that retention lifetime, based on an activation energy of 0.6 eV, will derate with T_J as shown in Fig 15.

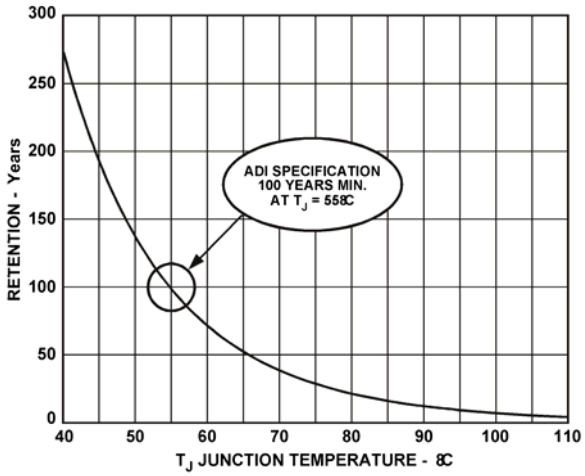


Fig.15. Flash/EE Memory Data Retention

FLASH/EE PROGRAM MEMORY

The ADuC845 contains a 64 Kbyte array of Flash/EE Program Memory. The lower 62 Kbytes of this program memory is available to the user, and can be used for program storage or indeed as additional NV data memory.

The upper 2 Kbytes of this Flash/EE program memory array contain permanently embedded firmware, allowing in circuit serial download, serial debug and non-intrusive single pin emulation. These 2 Kbytes of embedded firmware also contain a power-on configuration routine that downloads factory calibrated coefficients to the various calibrated peripherals (ADC, temperature sensor, current sources, bandgap references and so on).

This 2 Kbyte embedded firmware is hidden from user code. Attempts to read this space will read 0s, i.e., the embedded firmware appears as NOP instructions to user code.

In normal operating mode (power up default) the 62 Kbytes of user Flash/EE program memory appear as a single block. This block is used to store the user code as shown in Fig. 16.

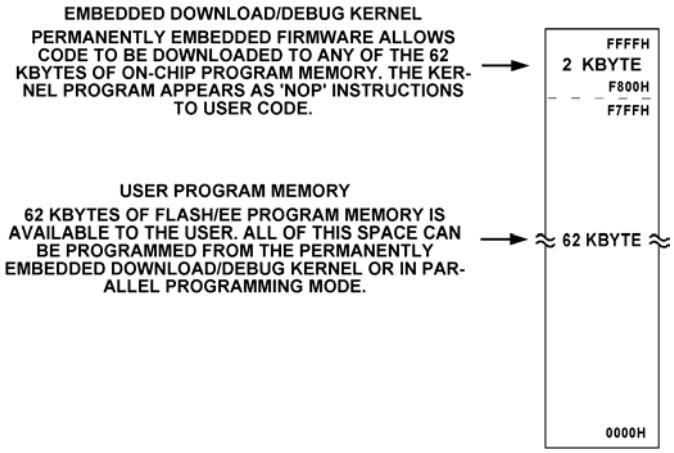


Fig.16. Flash/EE Program Memory Map in NORMAL Mode

In Normal Mode, the 62 Kbytes of Flash/EE program memory can be programmed programmed in two ways, namely:

(1) Serial Downloading (In-Circuit Programming)

The ADuC845 facilitates code download via the standard UART serial port. The ADuC845 will enter Serial Download Mode after a reset or power cycle if the PSEN pin is pulled low through an external 1 kΩ resistor. Once in serial download mode, the hidden embedded download kernel will execute. This allows the user to download code to the full 62 Kbytes of Flash/EE program memory while the device is in circuit in its target application hardware.

A PC serial download executable (WSD.EXE) is provided as part of the ADuC845 QuickStart development system. Tech note uC004 fully describes the serial download protocol that is used by the embedded download kernel. This tech note is available at www.analog.com/microconverter.

(2) Parallel Programming

The Parallel Programming Mode is fully compatible with conventional third party Flash or EEPROM device programmers. A block diagram of the external pin configuration required to support parallel programming is shown in Figure 17. In this mode, Ports 0, and 2 operate as the external address bus interface, P3 operates as the external databus interface and P1.0 operates as the Write Enable strobe. Port 1.1, P1.2, P1.3, and P1.4 are used as a general configuration port that configures the device for various program and erase operations during parallel programming.

Table XVI. Flash/EE Memory Parallel Programming Modes

Port 1 Pins				
P1.4	P1.3	P1.2	P1.1	Programming Mode
0	0	0	0	Erase Flash/EE Program, Data, and Security Mode
1	0	0	1	Read Device Signature/ID
1	0	1	0	Program Code Byte
0	0	1	0	Program Data Byte
1	0	1	1	Read Code Byte
0	0	1	1	Read Data Byte
1	1	0	0	Program Security Modes
1	1	0	1	Read/Verify Security Modes
All other codes				Redundant

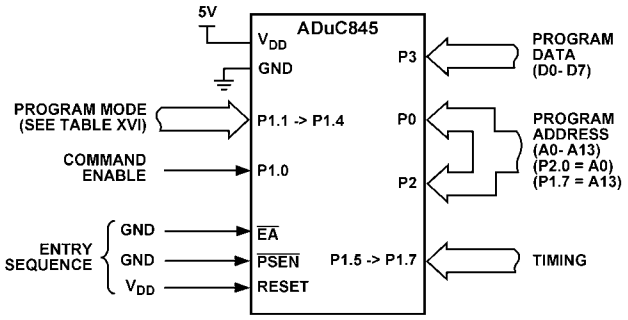


Fig. 17 Flash/EE Memory Parallel Programming

USER DOWNLOAD MODE (ULOAD)

In Figure 16 we can see that it is possible to use the 62 Kbytes of Flash/EE program memory available to the user as one single block of memory. In this mode all of the Flash/EE memory is read only to user code.

However, most of the Flash/EE program memory can also be written to during runtime simply by entering ULOAD Mode. In ULOAD Mode, the lower 56 Kbytes of program memory can be erased and reprogrammed by user software as shown in Figure 18. ULOAD Mode can be used to upgrade your code in the field via any user defined download protocol. Configuring the SPI port on the ADuC845 as a slave, it is possible to completely reprogram the 56 Kbytes of Flash/EE program memory in under 5s (see uC007).

Alternatively ULOAD Mode can be used to save data to the 56 Kbytes of Flash/EE memory. This can be extremely useful in datalogging applications where the ADuC845 can provide up to 60 Kbytes of NV data memory on-chip (4 Kbytes of dedicated Flash/EE data memory also exist).

The upper 6 Kbytes of the 62 Kbytes of Flash/EE program memory is only programmable via serial download or parallel programming. This means that this space appears as read only to user code. Therefore, it cannot be accidently erased or reprogrammed by erroneous code execution. This makes it very suitable to use the 6Kbytes as a bootloader. A Bootload Enable option exists in the serial downloader to "Always RUN from E000h after Reset." If

using a bootloader, this option is recommended to ensure that the bootloader always executes correct code after reset.

Programming the Flash/EE program memory via ULOAD Mode is described in more detail in the description of ECON and also in tech note uC007.

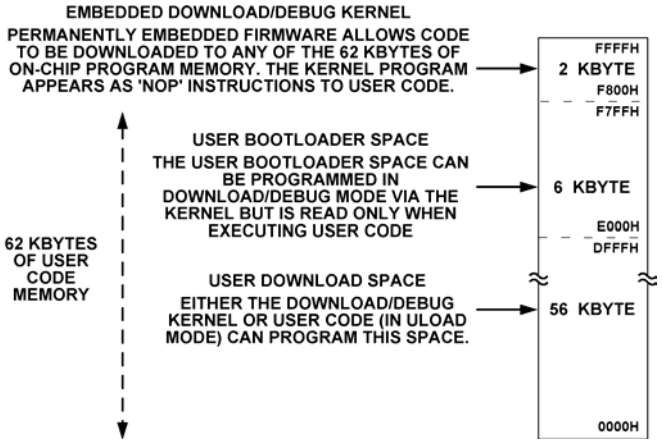


Figure 18. Flash/EE Program Memory Map in ULOAD Mode

Flash/EE Program Memory Security

The ADuC845 facilitates three modes of Flash/EE program memory security. These modes can be independently activated, restricting access to the internal code space. These security modes can be enabled as part of serial download protocol, as described in tech note uC004, or via parallel programming. The ADuC845 offers the following security modes:

Lock Mode

This mode locks the code memory, disabling parallel programming of the program memory. However, reading the memory in Parallel Mode and reading the memory via a MOVC command from external memory are still allowed. This mode is deactivated by initiating an “erase code and data” command in Serial Download or Parallel Programming Modes.

Secure Mode

This mode locks the code memory, disabling parallel programming of the program memory. Reading/Verifying the memory in Parallel Mode and reading the internal memory via a MOVC command from external memory is also disabled. This mode is deactivated by initiating an “erase code and data” command in Serial Download or Parallel Programming Modes.

Serial Safe Mode

This mode disables serial download capability on the device. If Serial Safe Mode is activated and an attempt is made to reset the part into Serial Download Mode, i.e., RESET asserted and deasserted with PSEN low, the part will interpret the serial download reset as a normal reset only. It will therefore not enter Serial Download Mode, but only execute a normal reset sequence. Serial Safe Mode can only be disabled by initiating an “erase code and data” command in parallel programming mode.

Using the Flash/EE Data Memory

The 4 Kbytes of Flash/EE data memory is configured as 1024 pages, each of 4 bytes. As with the other ADuC845 peripherals, the interface to this memory space is via a group of registers mapped in the SFR space. A group of four data registers (EDATA1–4) is used to hold the 4 bytes of data at each page. The page is addressed via the two registers EADRH and EADRL. Finally, ECON is an 8-bit control register that may be written with one of nine Flash/EE memory access commands to trigger various read, write, erase, and verify functions. A block diagram of the SFR interface to the Flash/EE data memory array is shown in Figure 19.

ECON—Flash/EE Memory Control SFR

Programming of either the Flash/EE data memory or the Flash/EE program memory is done through the Flash/EE Memory Control SFR (ECON). This SFR allows the user to read, write, erase or verify the 4 Kbytes of Flash/EE data memory or the 56 Kbytes of Flash/EE program memory.

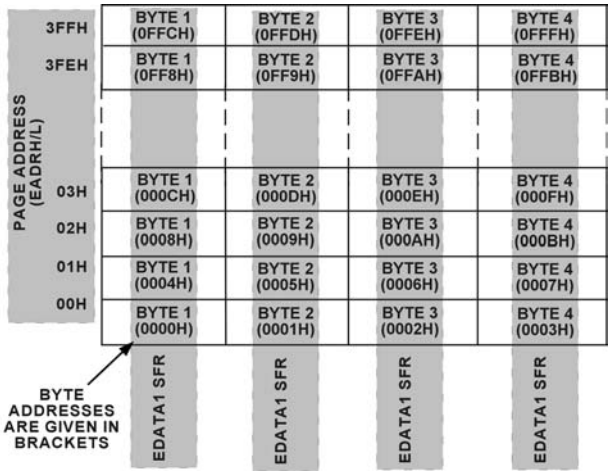


Figure 19. Flash/EE Data Memory Control & Configuration

Table XVII. ECON - Flash/EE Memory Commands

ECON Value	Command Description (Normal Mode, Power on default)	Command Description (ULOAD Mode)
01H Read	Results in 4 Bytes in the Flash/EE data menory, addressed by the page address EADRH/L, being read into EDATA1..4	Not Implemented. Use the MOVC instruction
02H Write	Results in 4 Bytes in EDATA1..4 being written to the Flash/EE data memory, at the page address given by EADRH (0 ≤ EADRH <0400H). Note: The four bytes in the page being addressed must be pre-erased.	Results in bytes 0-255 of internal XRAM being written to the 256 bytes of Flash/EE program memory at the page address given by EADRH/L (
03H	Reserved Command	Reserved Command
04H Verify	Verifies if the data in EDATA1..4 is contained in the page address given by EADRH/L. A subsequent read of the ECON SFR will result in a 0 being read if the verification is valid, or a nonzero value being read to indicate an invalid verification.	Not Implemented. Use the MOVC and MOVX instructions to verify the WRITE in software.
05H Erase Page	Results in the erasure of the 4 Byte page of Flash/EE data memory address by the page address EADRH/L	Results in the 64-Bytes page of FLASH/EE program memory, addressed by the byte address EADRH/L being erased. EADRL can equal and of the 64 locations within the page. A new page starts wheneven EADRL is equal to 00H, 80H or C0H.
06H Erase All	Results in the entire 4Kbytes of Flash/EE data memory.	Results in the erasure of the entire 56 Kbytes of ULOAD.
81H ReadByte	Results in the byte in the flash/EE data memory, addressed by the byte address EADRH/L, being read into EDATA1. (0 ≤ EADRH/L ≤ 0FFFH).	Not implemented. Use the MOVC command
82H WriteByte	Results in the byte in EDATA1 being written into Flash/EE data memory, at the byte address EADRH/L.	Results in the byte in EDATA1 being written into Flash/EE program memory at the byte address EADRH/L (0≤ EADRH/L≤ DFFFH)
0FH EXULOAD	Configures the ECON instructions (above) to operate on Flash/EE data memory.	Enters normal mode, directing subsequent ECON instructions to operate on the Flash/EE data memory.
F0H ULOAD	Enters ULOAD mode, subsequent ECON instructions operate on Flash/EE Program memory	Enables the ECON Instructions to operate on the Flash/EE program memory. ULOAD Entery mode.

I²C SERIAL INTERFACE

The ADuC845 supports a fully licenced* I²C serial interface. The I2C interface is implemented as a full hardware slave and software master. SDATA (pin 27 on MQFP package and pin 29 on CSP package) is the data I/O pin and SCLK (pin 26 on MQFP package and pin 28 on CSP package). The I²C interface on the ADuC845 is fully independent of all other pin/function multiplexing. The I²C interface incorporated on the ADuC845 also includes a second address register (I2CADD1) at SFR address 0xF2 with a default power on value of 0x7F. The I²C interface is always available to the user and is not multiplexed with any other I/O functionality on the chip. This means that on the ADuC845 the I²C and SPI interfaces can be used at the same time. When using the I²C and SPI interfaces simultaneously, because they both utilize the same interrupt routine (vector address 0x3B), when an interrupt occurs from one of these it will be necessary to interrogate each interface to see which one has triggered the ISR request.

Four SFRs are used to control the I²C interface. These are described below.

I2CCON **I²C Control Register**

Function I2C control register.
SFR Address 0xE8
Power-On Default value 0x00
Bit Addressable Yes

Table XVIII. I2CCON SFR Bit Designations

Bit	Name	Description
7	MDO	I²C Software Master Data Output Bit (Master Mode Only). This data bit is used to implement a master I²C transmitter interface in software. Data writted to this bit will be Outputted on the SDATA pin if the data output enable bit (MDE) is set.
6	MDE	I²C Software Output Enable Bit (Master Mode only) Set by the user to enable the SDATA pin as an output (Tx). Cleared by the user to enable the SDATA pin as an input (Rx)
5	MCO	I²C Software Master Clock Output Bit (Master Mode only) This bit is used to implement the SCLK for a master I²C transmitter in software. Data written to this bit will be outputted on the SCLK pin.
4	MDI	I²C Software Master Data Input Bit (Master Mode only) This data bit is used to implement a master I²C receiver interface in software. Data on the SDATA pin is latched into this bit on an SCLK transition if the data output enable (MDE) bit is 0.
3	I2CM	I²C Master/Slave mode bit Set by the user to enable I²C software master mode. Cleared by user to enable I²C hardware slave mode.
2	I2CRS	I²C Reset Bit (Slave Mode only) Set by the user to reset the I²C interface. Cleared by user code for normal I²C operation.
1	I2CTX	I²C Direction Transfer Bit (Slave Mode only) Set by the MicroConverter is the I²C interface is transmitting. Cleared by the MicroConverter is the I²C interface is receiving.
0	I2CI	I²C Interrupt bit (Slave Mode only) Set by the MicroConverter after a byte has been transmitted or received. Cleared by the MicroConverter when the user code reads the I2CDAT SFR. I2CI should not be cleared by user code.

I2CADD **I²C Address Register 1**

Function Holds one of the I²C peripheral addresses for the part. It may be overwritten by user code. Application note uC001 at http://www.analog.com/microconverter describes the format of the I²C standard 7-bit address.
SFR Address 0x9B
Power-On Default value 0x55
Bit Addressable No

I2CADD1 **I²C Address Register 2**

Function As for I2CADD described above.
SFR Address 0xF2
Power On Default value 0x7F
Bit Addressable No

I2CDAT	I^2C Data Register
Function	The I2CDAT SFR is written to by user code to transmit data, or read by user code to read data just received by the I2C interface. Accessing I2CDAT automatically clears any pending I2C interrupt and the I2CI bit in the I2CCON SFR. User code should only access I2CDAT once per interrupt cycle.
SFR Address	0x9A
Power-On Default value	0x00
Bit Addressable	No.

SPI SERIAL INTERFACE

The ADuC845 integrates a complete hardware Serial Peripheral Interface (SPI) interface on-chip. SPI is an industry-standard synchronous serial interface that allows eight bits of data to be synchronously transmitted and received simultaneously, i.e., full duplex. It should be noted that the SPI pins are multiplexed with Port 2 pins (P2.0, P2.1, P2.2 & P2.3). The pins have SPI functionality only if SPE is SET. Otherwise, with SPE cleared standard Port 2 functionality is maintained. SPI can be configured for master or slave operation and typically consists of four pins, namely:

SCLOCK (Serial Clock I/O Pin), Pin 28 (MQFP package), Pin 30 (CSP package)

The master clock (SCLOCK) is used to synchronize the data being transmitted and received through the MOSI and MISO data lines.

A single data bit is transmitted and received in each SCLOCK period. Therefore, a byte is transmitted/received after eight SCLOCK periods. The SCLOCK pin is configured as an output in master mode and as an input in Slave mode. In master mode the bit-rate, polarity, and phase of the clock are controlled by the CPOL, CPHA, SPR0, and SPR1 bits in the SPICON SFR (see Table XV). In Slave mode the SPICON register will have to be configured with the phase and polarity (CPHA and CPOL) as the master as for both Master and Slave mode the data is transmitted on one edge of the SCLOCK signal and sampled on the other.

MISO (Master In, Slave Out Pin), Pin 30 (MQFP package), Pin 32 (CSP package)

The MISO (master in slave out) pin is configured as an input line in Master mode and an output line in Slave mode. The MISO line on the master (data in) should be connected to the MISO line in the slave device (data out). The data is transferred as byte-wide (8-bit) serial data, MSB first.

MOSI (Master Out, Slave In Pin), Pin 29 (MQFP package), Pin31 (CSP package)

The MOSI (master out slave in) pin is configured as an output line in Master mode and an input line in Slave mode. The MOSI line on the master (data out) should be connected to the MOSI line in the slave device (data in). The data is transferred as byte-wide (8-bit) serial data, MSB first.

SS (Slave Select Input Pin), Pin 31 (MQFP package), Pin 33 (CSP package)

The Slave Select (SS) input pin is only used when the ADuC834 is configured in SPI Slave mode. This line is active low. Data is only received or transmitted in Slave mode when the SS pin is low, allowing the ADuC845 to be used in single master, multislave SPI configurations. If CPHA = 1, the SS input may be permanently pulled low. With CPHA = 0, the SS input must be driven low before the first bit in a byte wide transmission or reception and return high again after the last bit in that byte wide transmission or reception. In SPI Slave mode, the logic level on the external SS pin (Pin 13), can be read via the SPR0 bit in the SPICON SFR.

The following SFR registers are used to control the SPI interface.

Table IXX. SPICON SFR Bit Designations

Bit	Name	Description
7	ISPI	SPI Interrupt bit Set by MicroConverter at the end of each SPI transfer Cleared directly by user code or indirectly by reading the SPIDAT SFR
6	WCOL	Write Collision Error Bit Set by MicroConverter if SPIDAT is written to while an SPI transfer is in progress Cleared by user code
5	SPE	SPI Interface Enable Bit Set by user code to enable SPI functionality Cleared by user code to enable standard Port2 functionality
4	SPIM	SPI Master/Slave Mode Select Bit Set by user code to enable Master mode operation (SCLOCK is an output) Cleared by user code to enable Slave mode operation (SCLOCK is an input)
3	CPOL[1]	Clock Polarity Bit Set by user code to enable SCLOCK idle High Cleared by user code to enable SCLOCK idle low
2	CPHA[1]	Clock Phase Select Bit Set by user code if leading SCLOCK edge is to transmit data Cleared by user code if trailing SCLOCK edge is to transmit data.
1	SPR1	SPI Bit-Rate Bits
0	SPR0	SPR1 SPR0 Selected Bit Rate 0 0 $f_{core}/2$ 0 1 $f_{core}/4$ 1 0 $f_{core}/8$ 1 1 $f_{core}/16$

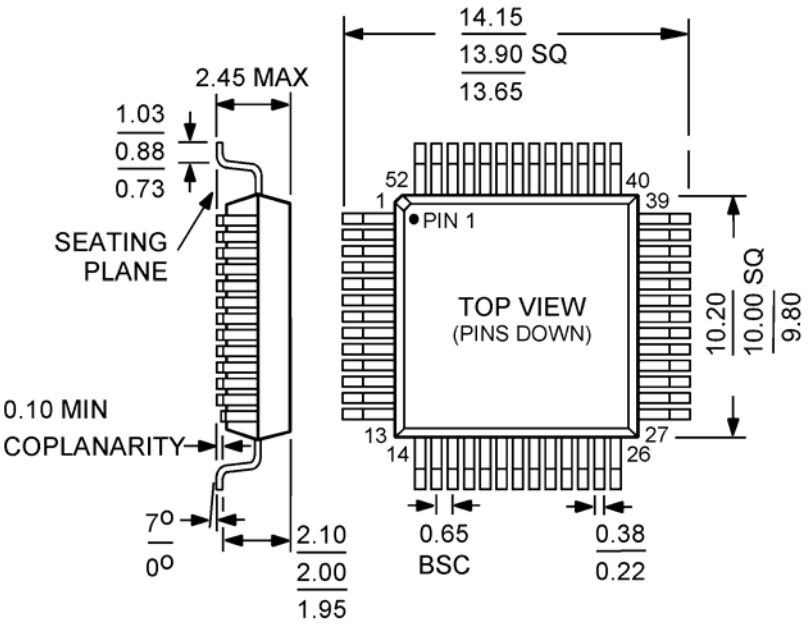
1. The CPOL and CPHA bits should both contain the same values for master and slave devices.

Note: Both SPI & I^2C utilize the same ISR (Vector address 0x3B), therefore when using both SPI & I^2C simultaneously it will be necessary to check the interfaces following an interrupt to determine which one caused the interrupt.

OUTLINE DIMENSIONS

52 LEAD METRIC QUAD FLAT PACK (MQFP)
(S-52)

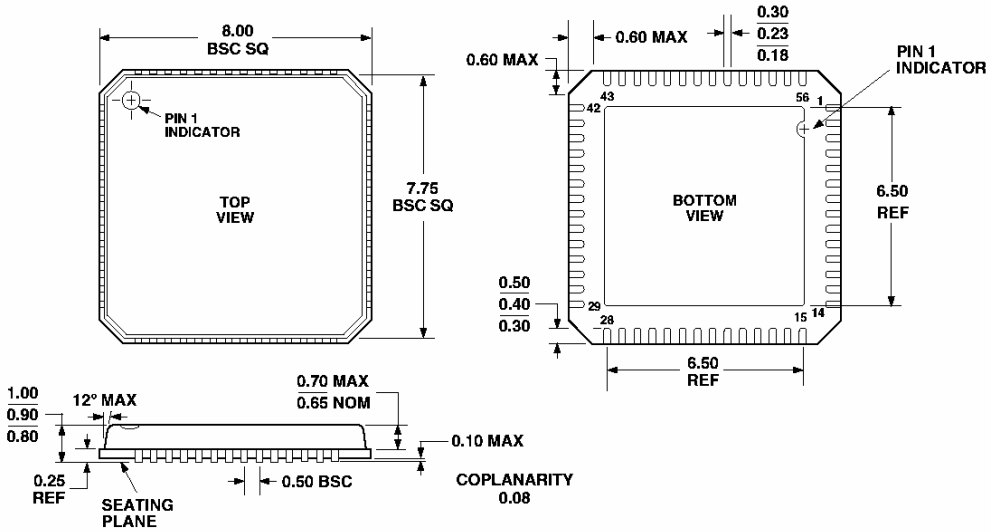
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARD MO-022-AC-1

56-Lead Frame Chip Scale Package [LFCSP]
8x8 mm Body
(CP-56)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VLLD-2