DualCool™ N-Channel NexFET™ Power MOSFET

Check for Samples: CSD16407Q5C

FEATURES

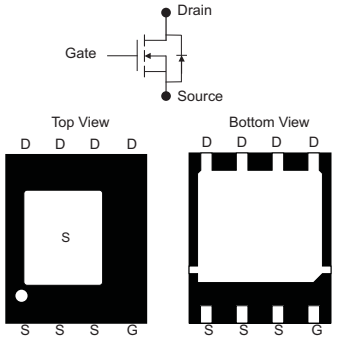
- **Ultralow Q_g and Q_{gd}**
- **DualCool™ Package**
- **Optimized for Two Sided Cooling**
- **Avalanche Rated**
- **Pb Free Terminal Plating**
- **RoHS Compliant**
- **Halogen Free**
- **SON 5-mm × 6-mm Plastic Package**

APPLICATIONS

- **Point-of-Load Synchronous Buck Converter for Applications in Networking, Telecom and Computing Systems**
- **Optimized for Synchronous FET Applications**

DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications.



PRODUCT SUMMARY

V_{DS}	Drain to Source Voltage	25		V
Q_g	Gate Charge Total (4.5V)	13.3		nC
Q_{gd}	Gate Charge Gate to Drain	3.5		nC
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 4.5V	2.5	mΩ
		V_{GS} = 10V	1.8	mΩ
$V_{(th)}$	Threshold Voltage	1.6		V

ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD16407Q5C	SON 5-mm × 6-mm Plastic Package	13-Inch Reel	2500	Tape and Reel

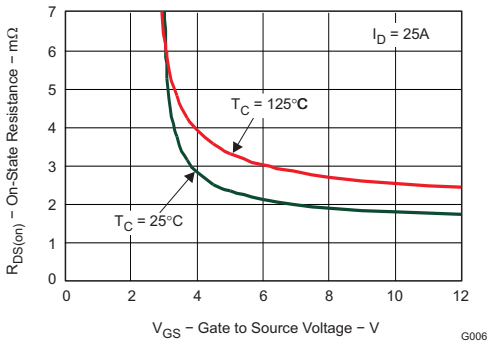
ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	25	V
V_{GS}	Gate to Source Voltage	+16 / –12	V
I_D	Continuous Drain Current, T_C = 25°C	100	A
	Continuous Drain Current(1)	31	A
I_{DM}	Pulsed Drain Current, T_A = 25°C(2)	200	A
P_D	Power Dissipation(1)	3.1	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	–55 to 150	°C
E_{AS}	Avalanche Energy, single pulse I_D = 66A, L = 0.1mH, R_G = 25Ω	218	mJ

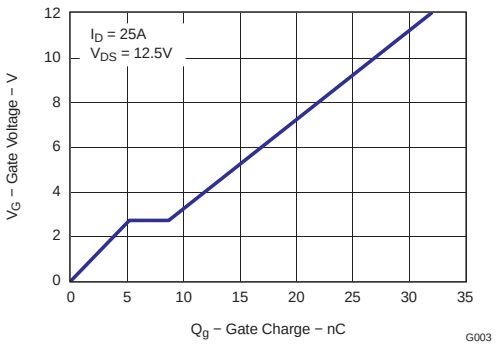
(1) Typical $R_{\theta JA}$ = 40°C/W on 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.

(2) Pulse duration ≤300μs, duty cycle ≤2%

$R_{DS(on)}$ vs V_{GS}



GATE CHARGE



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

DualCool, NexFET are trademarks of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, unless otherwise specified

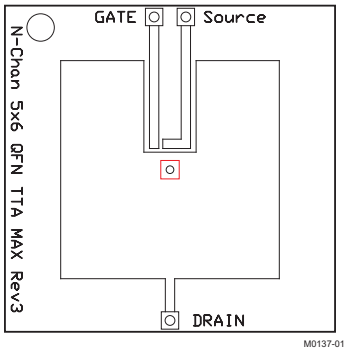
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	V_{GS} = 0V, I_D = 250µA	25			V
I_{DSS}	Drain to Source Leakage Current	V_{GS} = 0V, V_{DS} = 20V			1	µA
I_{GSS}	Gate to Source Leakage Current	V_{DS} = 0V, V_{GS} = +16V / –12V			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	1.3	1.6	1.9	V
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 4.5V, I_D = 25A		2.5	3.3	mΩ
		V_{GS} = 10V, I_D = 25A		1.8	2.4	mΩ
g_{fs}	Transconductance	V_{DS} = 15V, I_D = 25A		111		S
Dynamic Characteristics						
C_{ISS}	Input Capacitance	V_{GS} = 0V, V_{DS} = 12.5V , f = 1MHz		2040	2660	pF
C_{OSS}	Output Capacitance			1600	2080	pF
C_{RSS}	Reverse Transfer Capacitance			115	160	pF
R_g	Series Gate Resistance			1.2	2.4	Ω
Q_g	Gate Charge Total (4.5V)	V_{DS} = 12.5V, I_D = 25A		13.3	18	nC
Q_{gd}	Gate Charge Gate to Drain			3.5		nC
Q_{gs}	Gate Charge Gate to Source			5.3		nC
$Q_{g(th)}$	Gate Charge at Vth			3.1		nC
Q_{OSS}	Output Charge	V_{DS} = 13.5V, V_{GS} = 0V		33		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 12.5V, V_{GS} = 4.5V, I_D = 25A, R_G = 2Ω		11.9		ns
t_r	Rise Time			18.4		ns
$t_{d(off)}$	Turn Off Delay Time			16		ns
t_f	Fall Time			9		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_S = 25A, V_{GS} = 0V		0.8	1	V
Q_{rr}	Reverse Recovery Charge	V_{DD} = 13.5V, I_F = 25A, di/dt = 300A/µs		42		nC
t_{rr}	Reverse Recovery Time	V_{DD} = 13.5V, I_F = 25A, di/dt = 300A/µs		34		ns

THERMAL CHARACTERISTICS

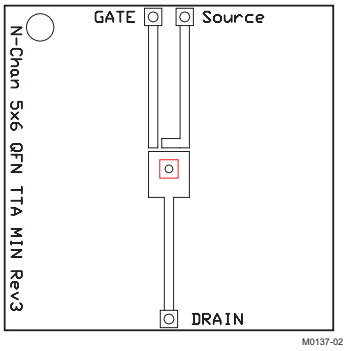
T_A = 25°C, unless otherwise specified

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case (Top Source) (1)			1.2	°C/W
$R_{\theta JC}$	Thermal Resistance Junction to Case (Bottom Drain) (1)			1.1	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (1) (2)			51	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 51°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 121°C/W when mounted on minimum pad area of 2-oz. (0.071-mm thick) Cu.

TYPICAL MOSFET CHARACTERISTICS

T_A = 25°C, unless otherwise specified

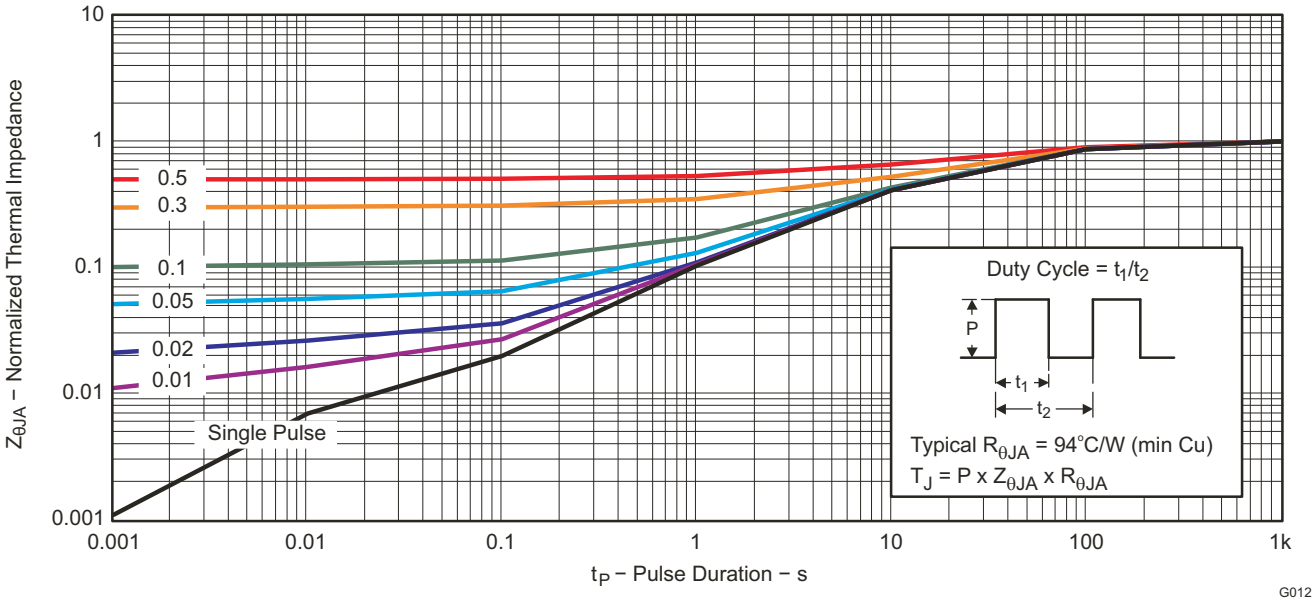


Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

T_A = 25°C, unless otherwise specified

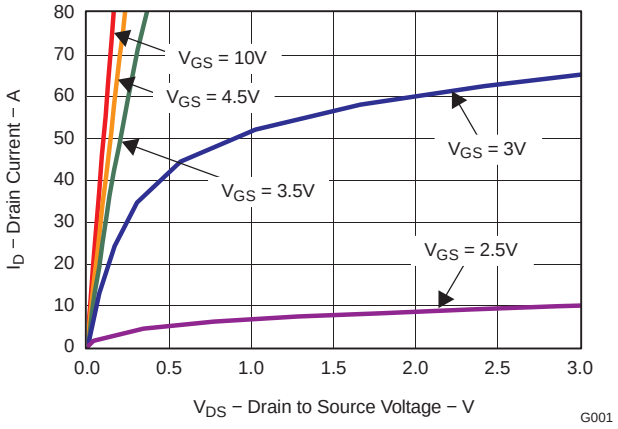


Figure 2. Saturation Characteristics

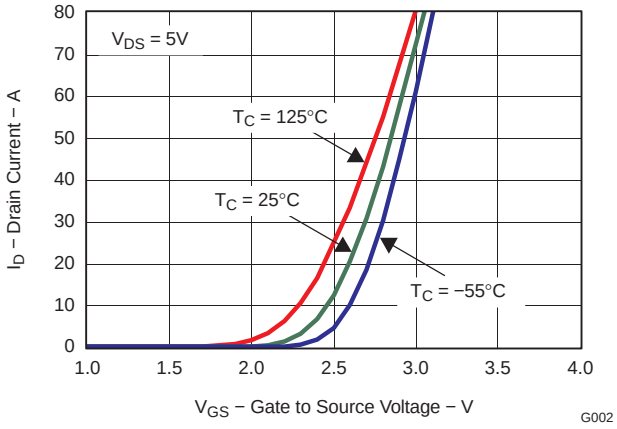


Figure 3. Transfer Characteristics

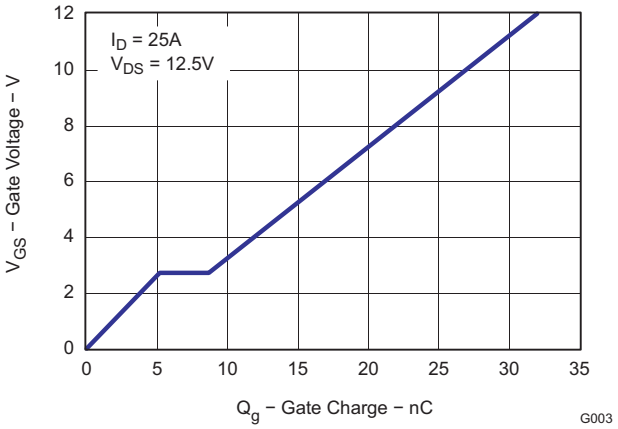


Figure 4. Gate Charge

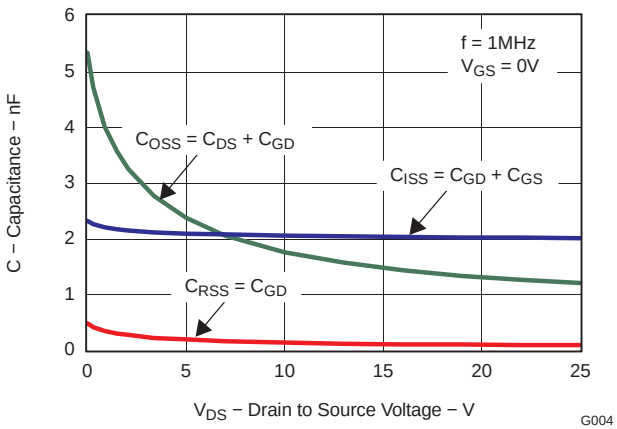


Figure 5. Capacitance

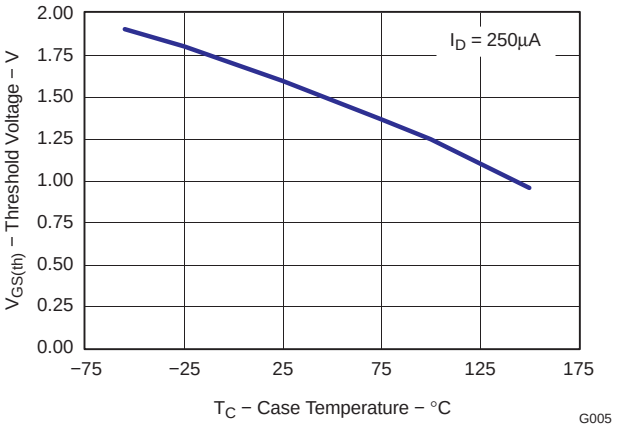


Figure 6. Threshold Voltage vs. Temperature

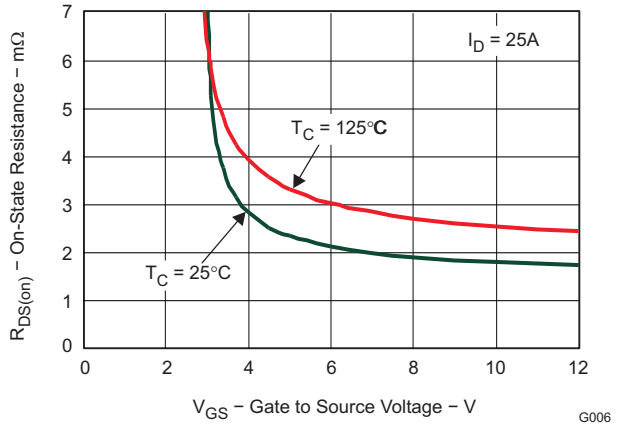


Figure 7. On-State Resistance vs. Gate to Source Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

T_A = 25°C, unless otherwise specified

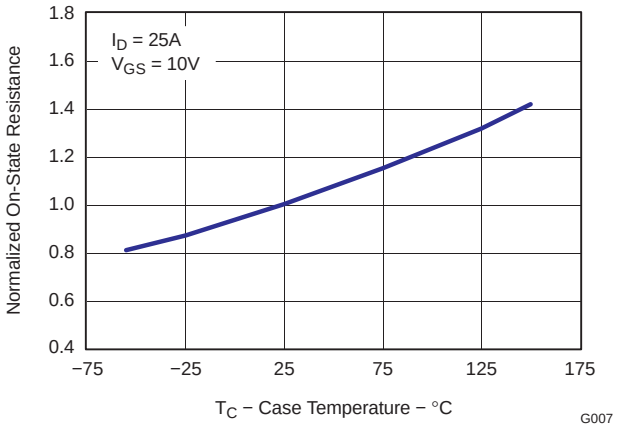


Figure 8. Normalized On-State Resistance vs. Temperature

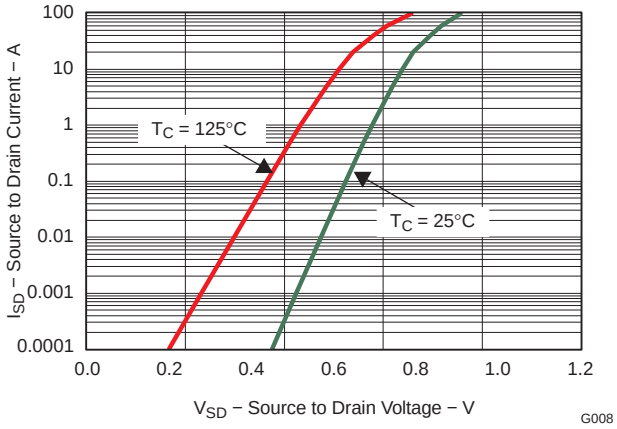


Figure 9. Typical Diode Forward Voltage

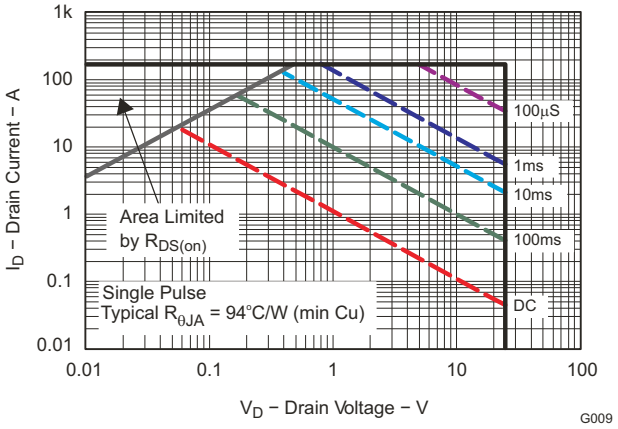


Figure 10. Maximum Safe Operating Area

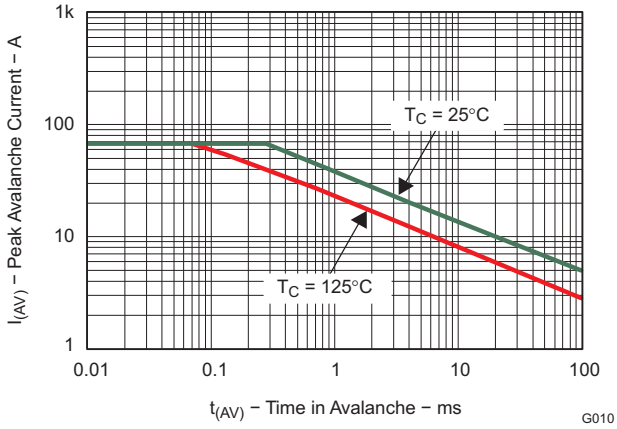


Figure 11. Single Pulse Unclamped Inductive Switching

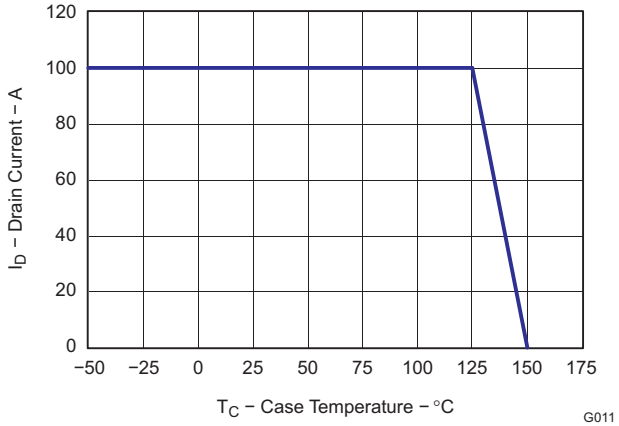
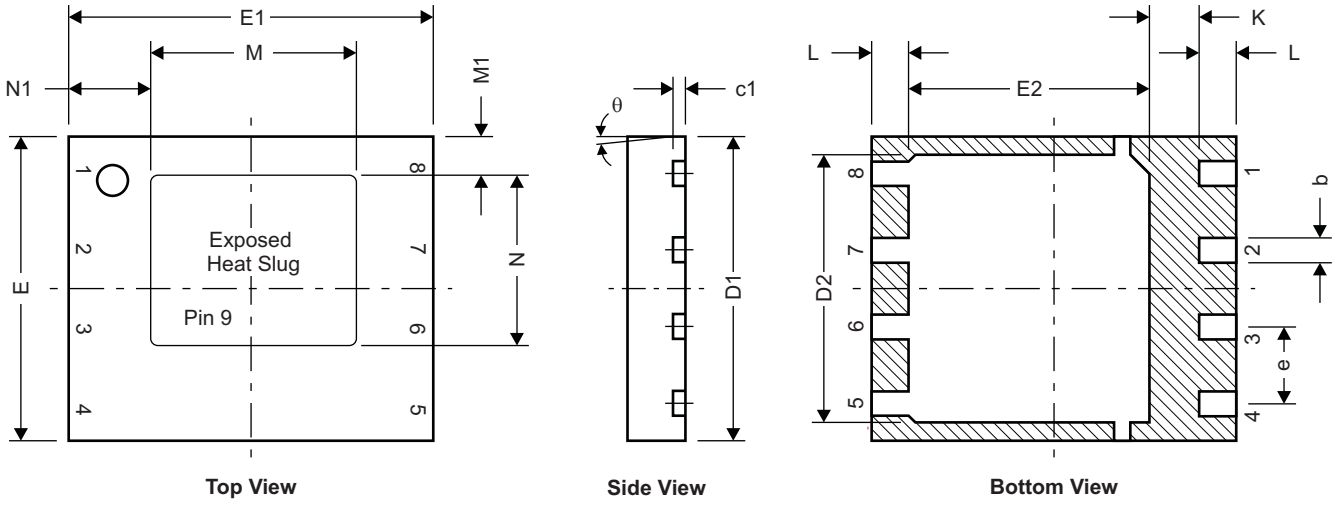
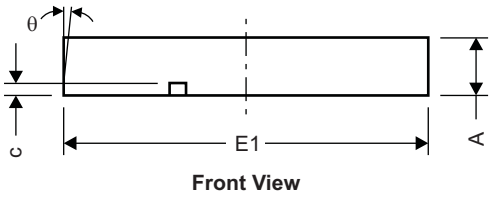


Figure 12. Maximum Drain Current vs. Temperature

MECHANICAL DATA

Q5C Package Dimensions



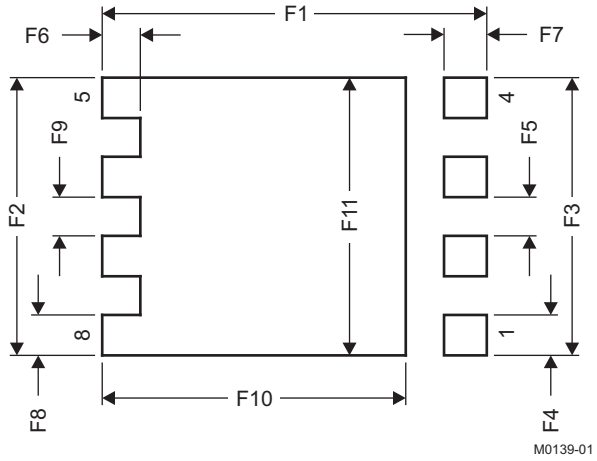


DualCool™ Pinout	
Pin#	**Label**
1, 2, 3, 9	**Source**
4	**Gate**
5, 6, 7, 8	**Drain**

M0162-01

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.950	1.050	0.037	0.039
b	0.360	0.460	0.014	0.018
c	0.150	0.250	0.006	0.010
c1	0.150	0.250	0.006	0.010
D1	4.900	5.100	0.193	0.201
D2	4.320	4.520	0.170	0.178
E	4.900	5.100	0.193	0.201
E1	5.900	6.100	0.232	0.240
E2	3.920	4.12	0.154	0.162
e	1.27 TYP		0.050	
K	0.760	–	0.030	–
L	0.510	0.710	0.020	0.028
θ	–	–	–	–
M	3.250	3.460	0.128	0.136
M1	0.520	0.720	0.020	0.028
N	2.720	2.920	0.107	0.115
N1	1.227	1.427	0.048	0.056

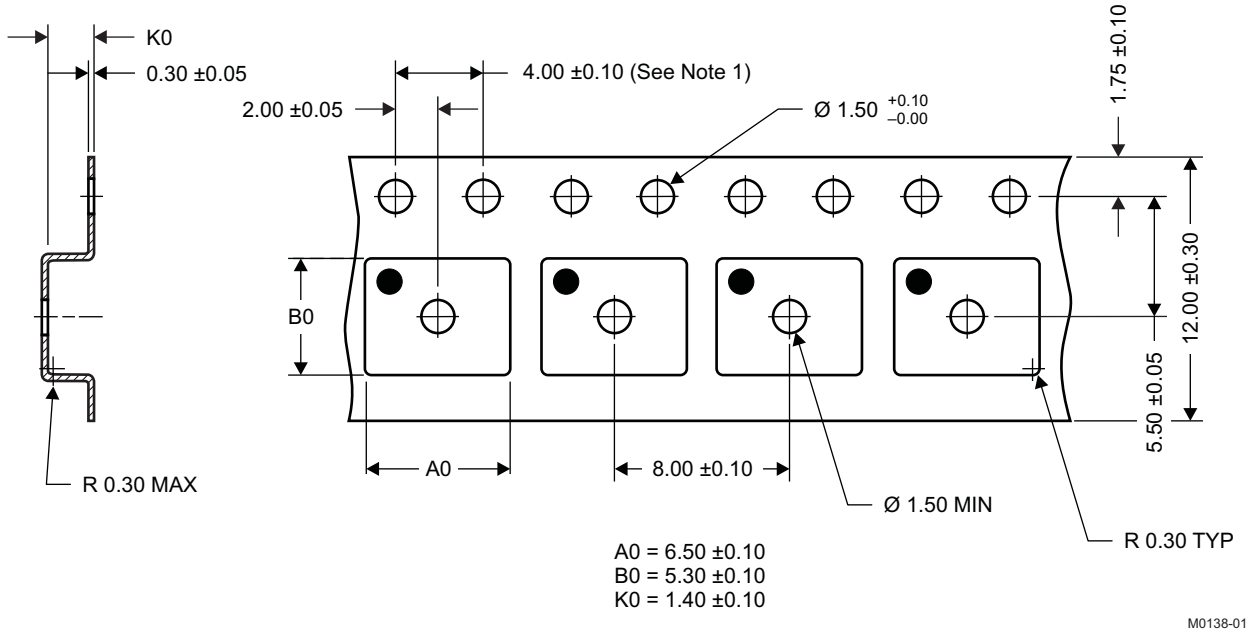
Recommended PCB Pattern



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.460	4.560	0.176	0.180
F3	4.460	4.560	0.176	0.180
F4	0.650	0.700	0.026	0.028
F5	0.620	0.670	0.024	0.026
F6	0.630	0.680	0.025	0.027
F7	0.700	0.800	0.028	0.031
F8	0.650	0.700	0.026	0.028
F9	0.620	0.670	0.024	0.026
F10	4.900	5.000	0.193	0.197
F11	4.460	4.560	0.176	0.180

For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

Q5C Tape and Reel Information



Notes:

1. 10-sprocket hole-pitch cumulative tolerance ±0.2
2. Camber not to exceed 1mm in 100mm, noncumulative over 250mm
3. Material: black static-dissipative polystyrene
4. All dimensions are in mm, unless otherwise specified.
5. Thickness: 0.30 ± 0.05 mm
6. MSL1 260°C (IR and convection) PbF reflow compatible

Package Marking Information

Location

1st Line

CSD = Fixed Characters

NNNNN = 5-digit Product Code

C = DualCool Package

2nd Line (Date Code)

Y = Last digit of the Year

WW = 2-digit Work Week

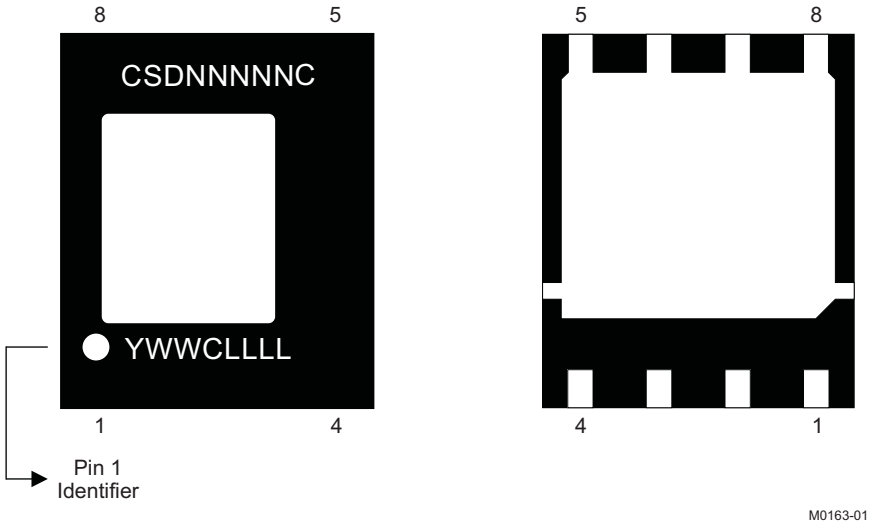
C = Country of Origin

> Philippines = P

> Taiwan = T

> China = C

LLLL = Last 4 digits of the Wafer Lot #



REVISION HISTORY

Changes from Original (October 2009) to Revision A **Page**

- Changed the device From: Procuct Preview To: Production 1
- Changed Application - From: Optimized for Control FET ApplicationsTo: Optimized for Synchronous FET Applications 1
- Changed the pinout illustration. 1
- Changed the Q5C Package Dimensions illustration 6

Changes from Revision A (December 2009) to Revision B **Page**

- Changed the ABSOLUTE MAXIMUM RATINGS table, I_D - Continuous Drain Current value From: 30A To: 31A 1
- Changed Note 1 of the ABSOLUTE MAXIMUM RATINGS table From: Typical $R_{\theta JA}$ = 41°C To: Typical $R_{\theta JA}$ = 40°C 1
- Changed Figure 1 - From: Typical $R_{\theta JA}$ = 98°C/W To: Typical $R_{\theta JA}$ = 94°C/W 3
- Changed Figure 10 - From: Typical $R_{\theta JA}$ = 98°C/W To: Typical $R_{\theta JA}$ = 94°C/W 5
- Changed Figure 11 - X axis values 5

PACKAGING INFORMATION

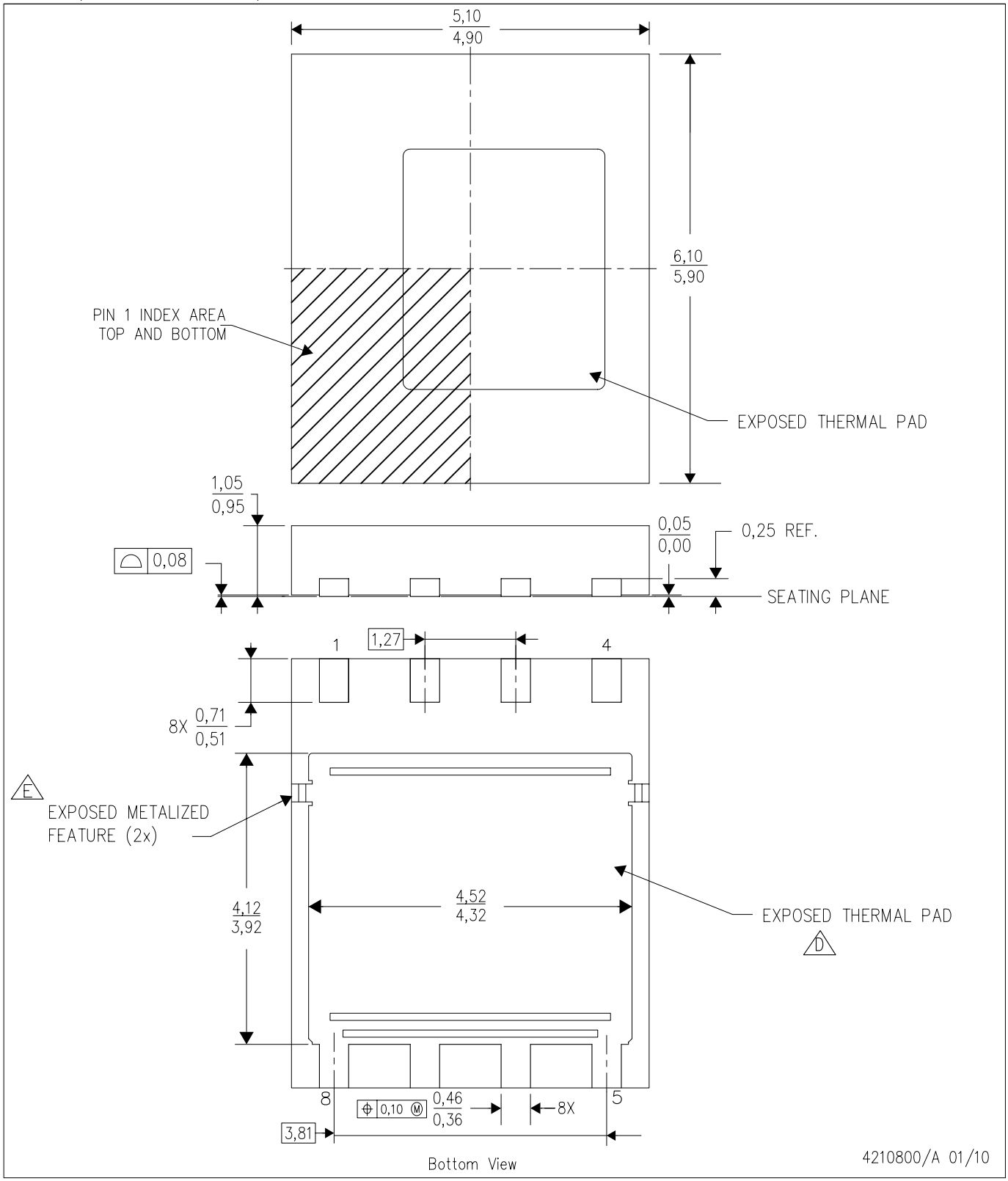
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
CSD16407Q5C	ACTIVE	SON	DQU	8	2500	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

DQU (R–PSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Dual Cool No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. Metalized features are supplier options and may not be on the package.

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DSP	dsp.ti.com	Computers and Peripherals	www.ti.com/computers
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Logic	logic.ti.com	Industrial	www.ti.com/industrial
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Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Space, Avionics & Defense	www.ti.com/space-avionics-defense
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