

N-Channel CICLON NexFET™ Power MOSFETs CSD16412Q5A

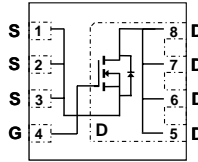


Features

- Ultra Low Qg & Qgd
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free



QFN 5mm x 6mm Plastic Package



Top View

Product Summary

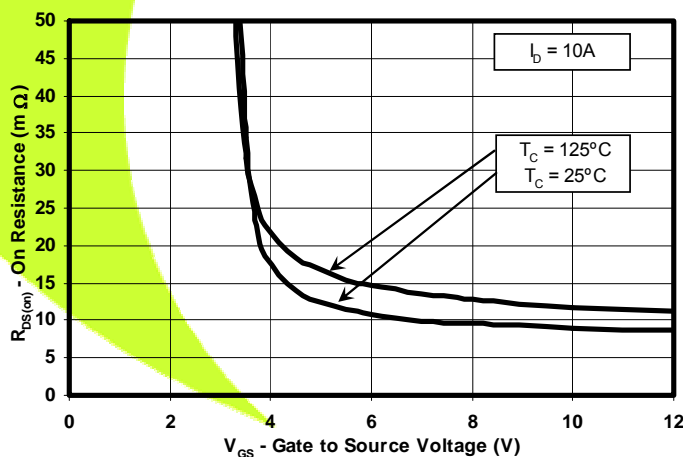
V_{DS}	25	V
Q_g	2.9	nC
Q_{gd}	0.7	nC
$R_{DS(on)}$	$V_{GS}=4.5V$	13 m Ω
	$V_{GS}=10V$	9 m Ω
V_{th}	2.0	V

Maximum Values ($T_A = 25^\circ C$ unless otherwise stated)

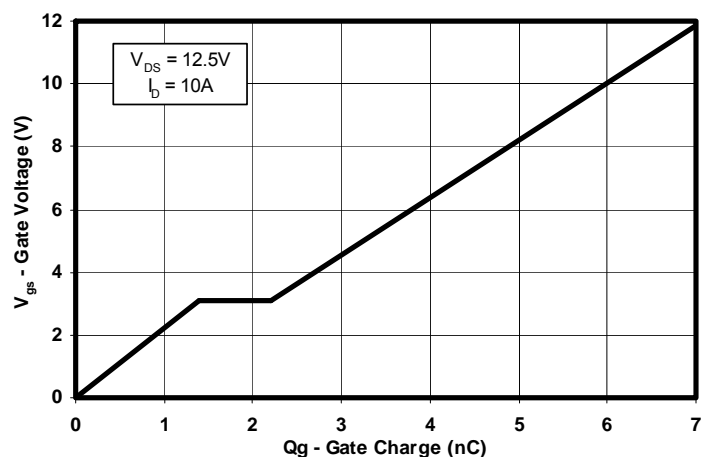
Symbol	Parameter	Value	Units
V_{DS}	Drain to Source Voltage	25	V
V_{GS}	Gate to Source Voltage	+16 / -12	V
I_D	Continuous Drain Current, $T_C = 25^\circ C$	52	A
	Continuous Drain Current ¹	14	A
I_{DM}	Pulsed Drain Current, $T_A = 25^\circ C^2$	108	A
P_D	Power Dissipation ¹	3.0	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ C$
E_{AS}	Avalanche Energy, single pulse $I_D=17A, L = 0.1mH, R_G = 25\Omega$	14	mJ

1. $R_{\theta JA} = 42^\circ C/W$ on 1in² Cu FR4 PCB.
2. Pulse width $\leq 300 \mu s$, duty cycle $\leq 2\%$

$R_{DS(on)}$ vs. V_{GS}



Gate Charge



Ordering Information

Type	Package	Package Media	Qty	Ship
CSD16412Q5A	QFN 5X6 Plastic Package	13 inch reel	2500	Tape and Reel

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CSD16412Q5A



Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise stated)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	$V_{GS} = 0V, I_D = 250\mu A$	25	—	—	V
I_{DSS}	Drain to Source Leakage Current	$V_{GS} = 0V, V_{DS} = 20V$	—	—	1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{DS} = 0V, V_{GS} = +16/-12V$	—	—	100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.7	2.0	2.3	V
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 4.5V, I_D = 10A$	—	13	16	$m\Omega$
		$V_{GS} = 10V, I_D = 10A$	—	9	11	$m\Omega$
g_{fs}	Transconductance	$V_{DS} = 15V, I_D = 10A$	—	33	—	S
Dynamic Characteristics						
C_{ISS}	Input Capacitance	$V_{GS} = 0V, V_{DS} = 12.5V$ $f = 1MHz$	—	410	530	pF
C_{OSS}	Output Capacitance		—	350	450	pF
C_{RSS}	Reverse Transfer Capacitance		—	32	42	pF
R_g	Series Gate Resistance		—	0.6	—	Ω
Q_g	Gate Charge Total (4.5V)	$V_{DS} = 12.5V, I_D = 10A$	—	2.9	3.8	nC
Q_{gd}	Gate Charge Gate to Drain		—	0.7	—	nC
Q_{gs}	Gate Charge Gate to Source		—	1.4	—	nC
$Q_{g(th)}$	Gate Charge at V_{th}		—	0.9	—	nC
Q_{OSS}	Output Charge	$V_{DS} = 13V, V_{GS} = 0V$	—	7.0	—	nC
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = 12.5V$ $V_{GS} = 4.5V, I_D = 10A$ $R_G = 15\Omega$	—	8.9	—	ns
t_r	Rise Time		—	19	—	ns
$t_{d(off)}$	Turn Off Delay Time		—	7.0	—	ns
t_f	Fall Time		—	8.9	—	ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	$I_S = 10A, V_{GS} = 0V$	—	0.85	1.0	V
Q_{rr}	Reverse Recovery Charge	$V_{dd} = 13V, I_F = 10A,$ $di/dt = 300A/\mu s$	—	12	—	nC
t_{rr}	Reverse Recovery Time	$V_{dd} = 13V, I_F = 10A,$ $di/dt = 300A/\mu s$	—	16	—	ns

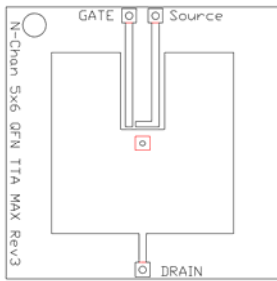
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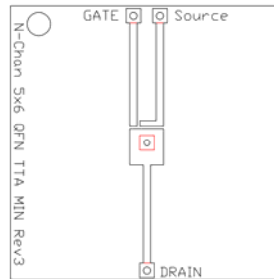
Thermal Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Units
Thermal Characteristics					
$R_{\theta JC}$	Thermal Resistance Junction to Case ³	—	—	3.7	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient ^{3,4}	—	—	53	$^\circ\text{C/W}$

- $R_{\theta JC}$ is determined with the device mounted on a 1in square 2 oz. Cu pad on a 1.5x1.5 in .060in thick FR4 board. $R_{\theta JC}$ is guaranteed by design while $R_{\theta ca}$ is determined by the user's board design.
- Device mounted on FR4 Material with 1in² of 2 oz. Cu.



Max $R_{\theta JA} = 53^\circ\text{C/W}$ when mounted on 1in² of 2 oz. Cu.



Max $R_{\theta JA} = 119^\circ\text{C/W}$ when mounted on min pad area of 2 oz. Cu.

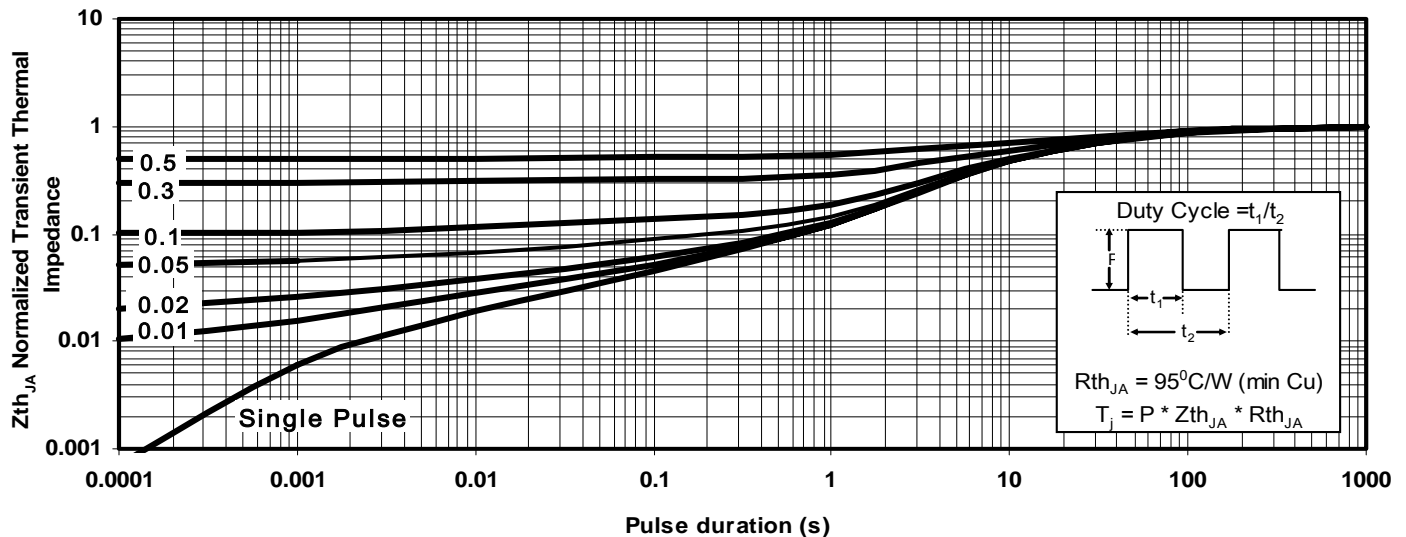


Figure 1: Transient Thermal Impedance

N-Channel CICLON NexFET™ Power MOSFETs CSD16412Q5A



Typical MOSFET Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise stated)

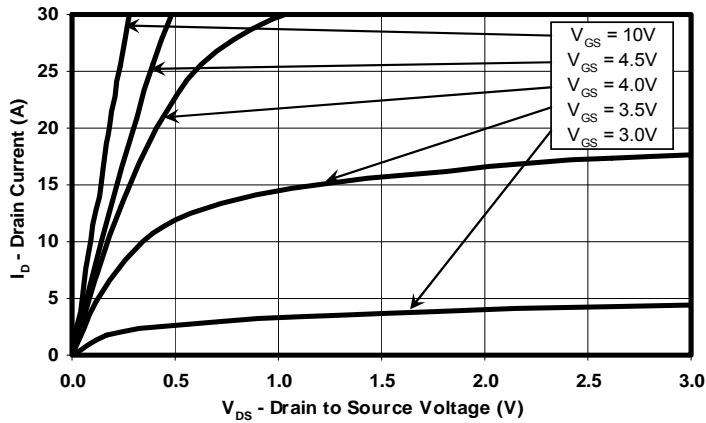


Figure 2: Saturation Characteristics

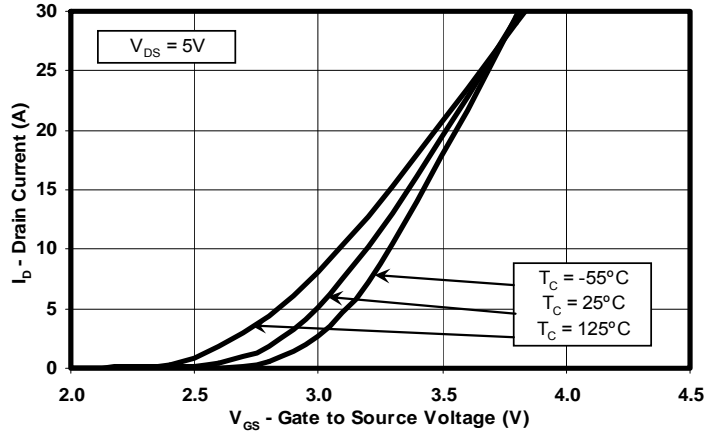


Figure 3: Transfer Characteristics

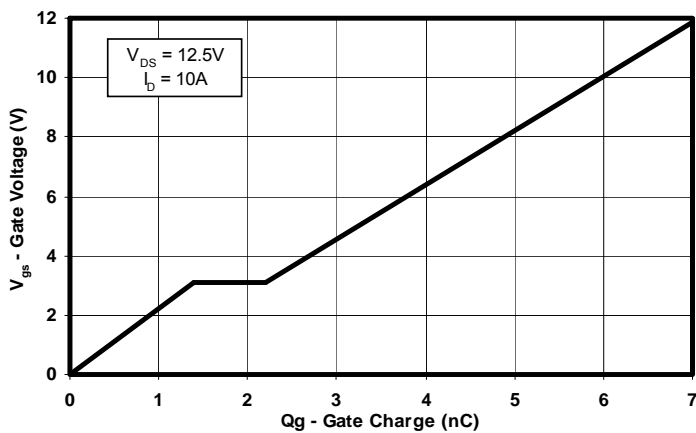


Figure 4: Gate Charge

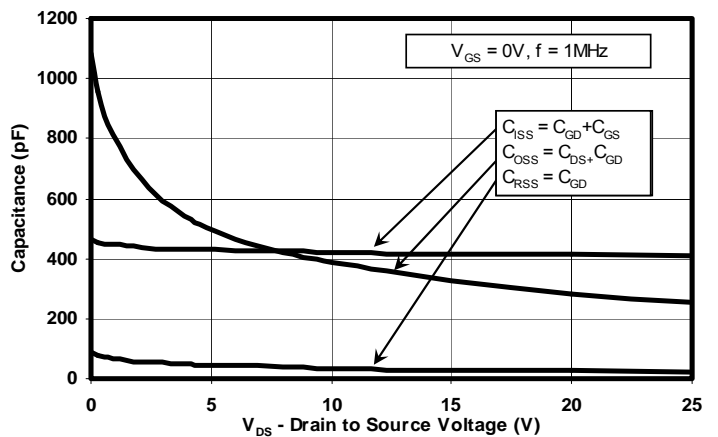


Figure 5: Capacitance

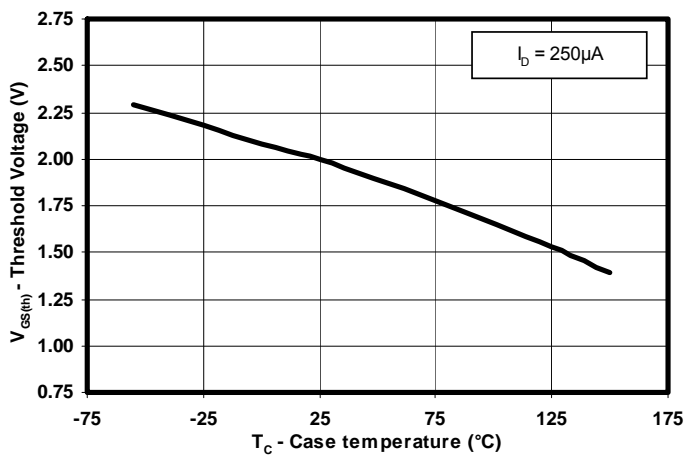


Figure 6: Threshold Voltage vs. Temperature

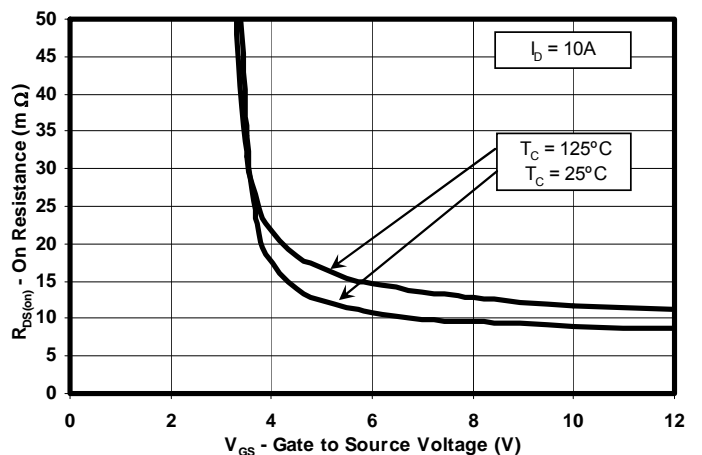


Figure 7: On Resistance vs. Gate Voltage

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Typical MOSFET Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise stated)

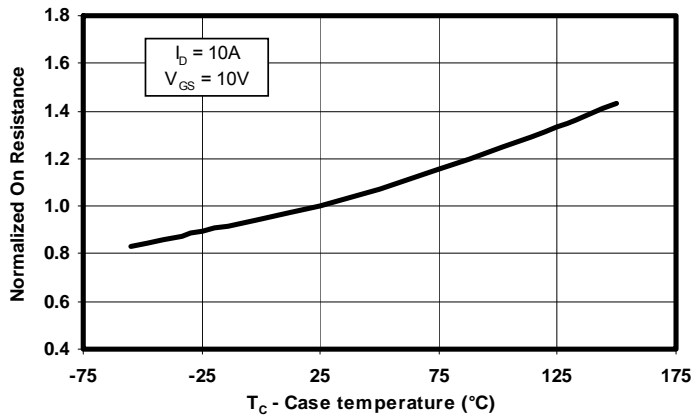


Figure 8: On Resistance vs. Temperature

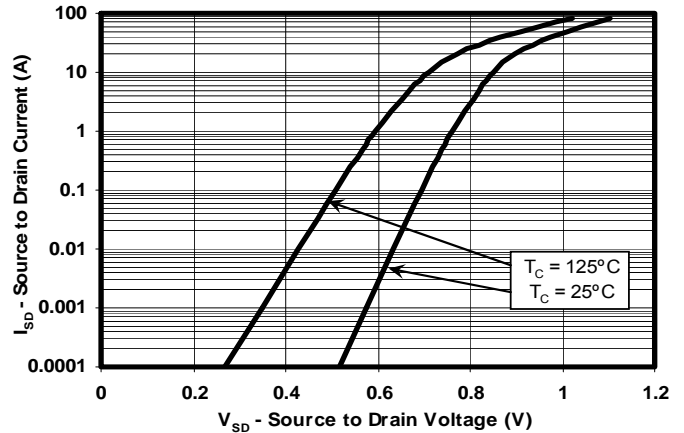


Figure 9: Typical Diode Forward Voltage

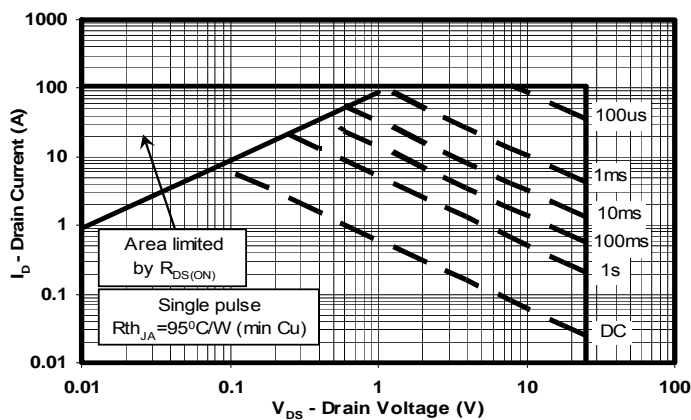


Figure 10: Maximum Safe Operating Area

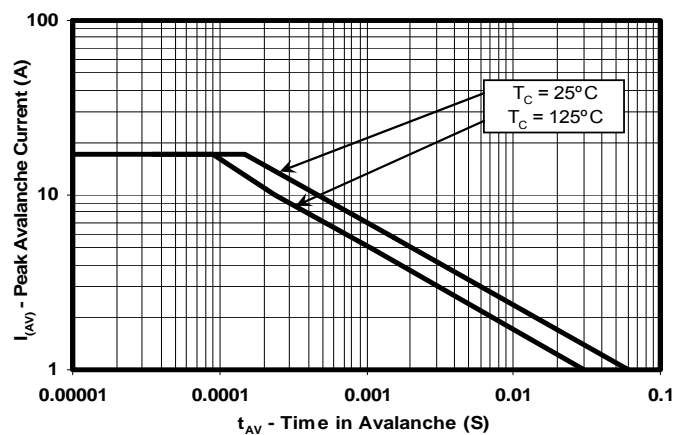


Figure 11: Single Pulse Unclamped Inductive Switching

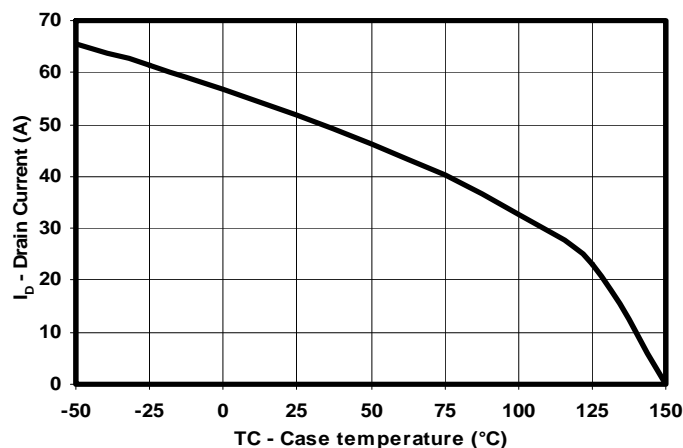
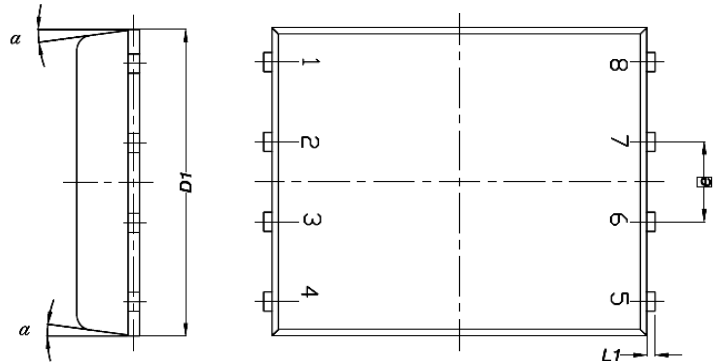
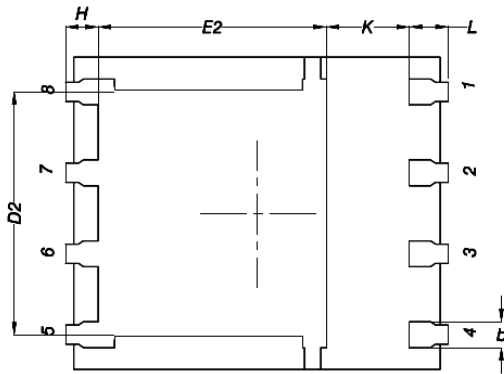


Figure 12: Maximum Drain Current vs. Temperature

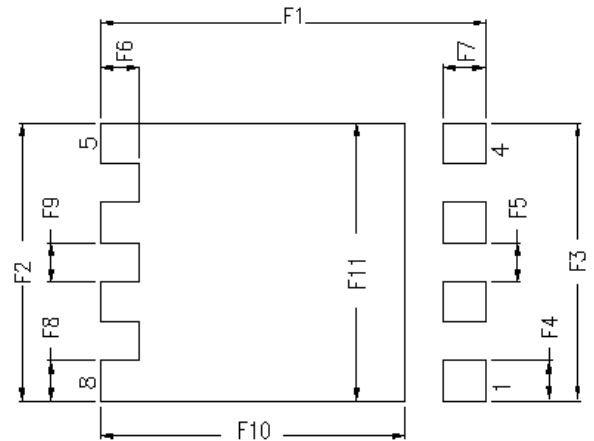
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CDS16412Q5A Package Dimensions



RECOMMENDED PCB PATTERN



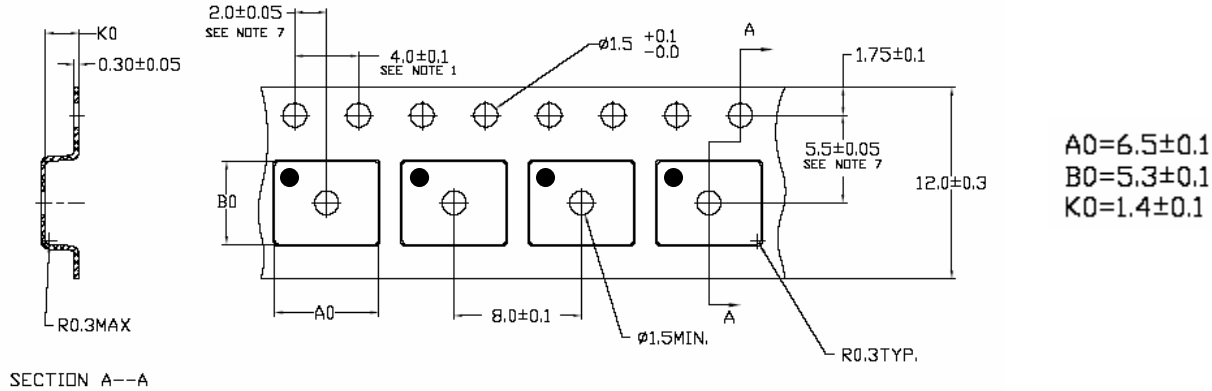
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
b	0.33	0.41	0.51
c	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
a	0°		12°

DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
F1	6.205	6.305	0.244	0.248
F2	4.46	4.56	0.176	0.18
F3	4.46	4.56	0.176	0.18
F4	0.65	0.7	0.026	0.028
F5	0.62	0.67	0.024	0.026
F6	0.63	0.68	0.025	0.027
F7	0.7	0.8	0.028	0.031
F8	0.65	0.7	0.026	0.028
F9	0.62	0.67	0.024	0.026
F10	4.9	5	0.193	0.197
F11	4.46	4.56	0.176	0.18

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Q5A Tape and Reel Information



Note:

1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE +/-0.2
2. CAMBER NOT TO EXCEED 1mm IN 100mm, NONCUMULATIVE OVER 250mm
3. MATERIAL:BLACK STATIC DISSIPATIVE POLYSTYRENE
4. ALL DIMENSIONS ARE IN mm (UNLESS OTHERWISE SPECIFIED)
5. A0 AND B0 MEASURED ON A PLANE 0.3mm ABOVE THE BOTTOM OF THE POCKET

Package Marking Information

Location:

1st Line

CSD = Fixed Characters

NNNN = Product Code

2nd Line (Date Code)

YY = Last 2 digits of the Year

WW = 2-digit Work Week

C = Country of Origin

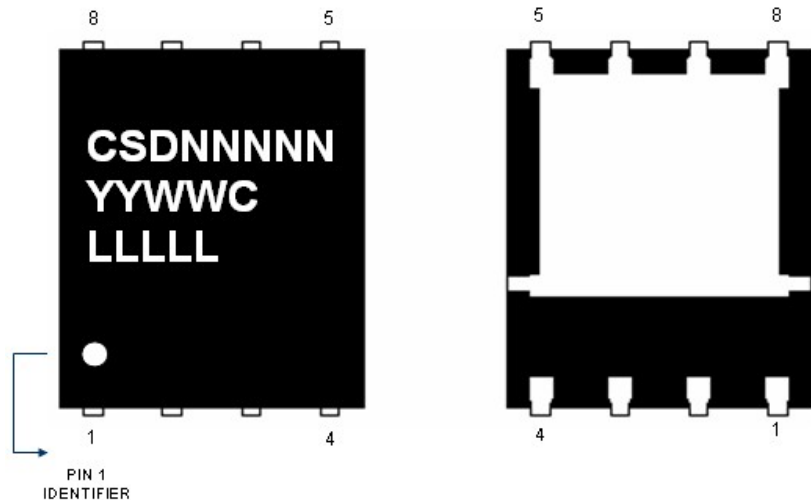
> Philippines = P

> Taiwan = T

> China = C

3rd Line

LLLLL = Last 5 digits of the Wafer Lot #



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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CSD16412Q5A	ACTIVE	SON	DQJ	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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