

Dual P-Channel NexFET™ Power MOSFET

Check for Samples: [CSD75204W15](#)

FEATURES

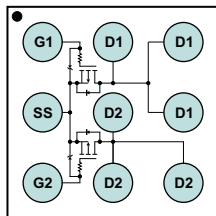
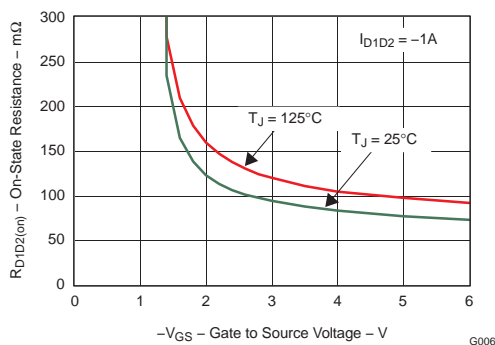
- Dual P-Ch MOSFETs
- Common Source Configuration
- Small Footprint 1.5-mm × 1.5-mm
- Gate-Source Voltage Clamp
- Gate ESD Protection –3kV
- Pb Free
- RoHS Compliant
- Halogen Free

APPLICATIONS

- Battery Management
- Battery Protection

DESCRIPTION

The device has been designed to deliver the lowest on resistance and gate charge in the smallest outline possible with excellent thermal characteristics in an ultra low profile. Low on resistance coupled with the small footprint and low profile make the device ideal for battery operated space constrained applications.

Top View

 $R_{D1D2(on)}$ vs V_{GS}

Table 1. PRODUCT SUMMARY

V_{D1D2}	Drain to Drain Voltage	-20	V
Q_g	Gate Charge Total (-4.5V)	2.8	nC
Q_{gd}	Gate Charge Gate to Drain	0.6	nC
$R_{D1D2(on)}$	Drain to Drain On Resistance	$V_{GS} = -1.8V$	140 mΩ
		$V_{GS} = -2.5V$	105 mΩ
		$V_{GS} = -4.5V$	80 mΩ
$V_{GS(th)}$	Threshold Voltage	-0.7	V

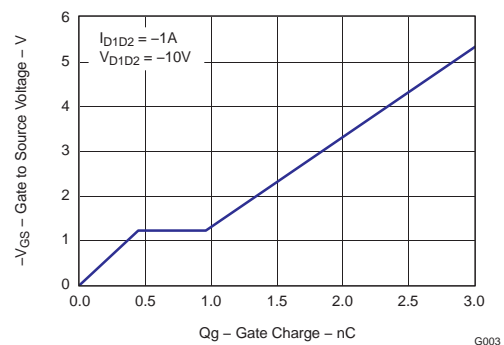
ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD75204W15	1.5-mm × 1.5-mm Wafer Level Package	7-Inch Reel	3000	Tape and Reel

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
V_{D1D2}	Drain to Drain Voltage	-20	V
V_{GS}	Gate to Source Voltage	-6	V
I_{D1D2}	Continuous Drain to Drain Current, $T_C = 25^\circ\text{C}^{(1)}$	-3	A
	Pulsed Drain to Drain Current, $T_C = 25^\circ\text{C}^{(2)}$	-28	A
I_S	Continuous Source Pin Current	-1.2	A
	Pulsed Source Pin Current ⁽²⁾	-15	A
I_G	Continuous Gate Clamp Current	-0.5	A
	Pulsed Gate Clamp Current ⁽²⁾	-7	A
P_D	Power Dissipation ⁽¹⁾	0.7	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

- (1) Per device, both sides in conduction
(2) Pulse duration 10 μs , duty cycle $\leq 2\%$

Gate Charge (Per MOSFET)


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ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise stated). Specifications and graphs are Per MOSFET unless otherwise stated. Drain to Drain measurements are done with both MOSFETs in series (common source configuration).

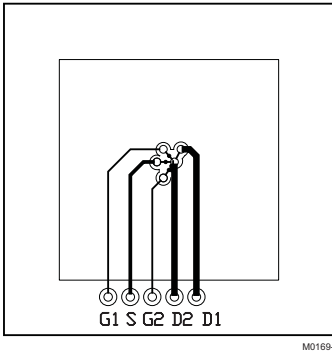
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{D1D2}	Drain to Drain Voltage	$V_{GS} = 0V, I_{D1D2} = -250\mu A$	-20			V
BV_{GSS}	Gate to Source Voltage	$V_{D1D2} = 0V, I_G = -250\mu A$	-6.1		-7.2	V
I_{DDS}	Drain to Source Leakage Current	$V_{GS} = 0V, V_{D1D2} = -16V$			-1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{D1D2} = 0V, V_{GS} = -6V$			-100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{D1D2} = V_{GS}, I_{DS} = -250\mu A$	-0.5	-0.7	-0.9	V
$R_{D1D2(on)}$	Drain to Drain On Resistance	$V_{GS} = -1.8V, I_{D1D2} = -1A$		140	175	$m\Omega$
		$V_{GS} = -2.5V, I_{D1D2} = -1A$		105	130	$m\Omega$
		$V_{GS} = -4.5V, I_{D1D2} = -1A$		80	100	$m\Omega$
g_{fs}	Transconductance	$V_{D1D2} = -10V, I_{D1D2} = -1A$		5.3		S
Dynamic Characteristics						
C_{ISS}	Input Capacitance	$V_{GS} = 0V, V_{D1D2} = -10V,$ $f = 1MHz$		315	410	pF
C_{OSS}	Output Capacitance			128	165	pF
C_{RSS}	Reverse Transfer Capacitance			43	55	pF
Q_g	Gate Charge Total (-4.5V)	$V_{D1D2} = -10V,$ $I_{D1D2} = -1A$		2.8	3.9	nC
Q_{gd}	Gate Charge - Gate to Drain			0.6		nC
Q_{gs}	Gate Charge - Gate to Source			0.5		nC
$Q_{g(th)}$	Gate Charge at V_{th}			0.2		nC
Q_{OSS}	Output Charge		$V_{D1D2} = -9.5V, V_{GS} = 0V$		2.2	
$t_{d(on)}$	Turn On Delay Time	$V_{D1D2} = -10V, V_{GS} = -4.5V,$ $I_{D1D2} = -1A, R_G = 30\Omega$		7.8		ns
t_r	Rise Time			6.7		ns
$t_{d(off)}$	Turn Off Delay Time			45		ns
t_f	Fall Time			26		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	$I_{D1D2} = -1A, V_{GS} = 0V$		0.75	1	V
Q_{rr}	Reverse Recovery Charge	$V_{dd} = -9.5V, I_F = -1A, di/dt = 200A/\mu s$		10.5		nC
t_{rr}	Reverse Recovery Time	$V_{dd} = -9.5V, I_F = -1A, di/dt = 200A/\mu s$		23		ns

THERMAL CHARACTERISTICS

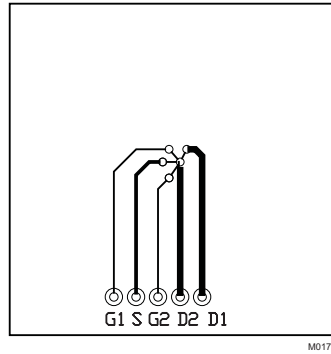
($T_A = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Thermal Resistance Junction to Ambient ^{(1) (2)}			200	$^\circ\text{C}/\text{W}$
	Thermal Resistance Junction to Ambient ^{(3) (2)}			94	$^\circ\text{C}/\text{W}$

- (1) Device mounted on FR4 material with Minimum Cu mounting area.
- (2) Measured with both devices biased in a parallel condition.
- (3) Device mounted on FR4 material with 1-inch² of Cu (2oz).



Max $R_{\theta JA} = 94^{\circ}\text{C/W}$ when mounted on 1 inch² (6.45 cm²) of 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA} = 200^{\circ}\text{C/W}$ when mounted on minimum pad area of 2-oz. (0.071-mm thick) Cu.

TYPICAL MOSFET CHARACTERISTICS

Graphs are Per MOSFET at $T_A = 25^{\circ}\text{C}$, unless stated otherwise. Drain to Drain measurements are done with both MOSFETs in series (common source configuration).

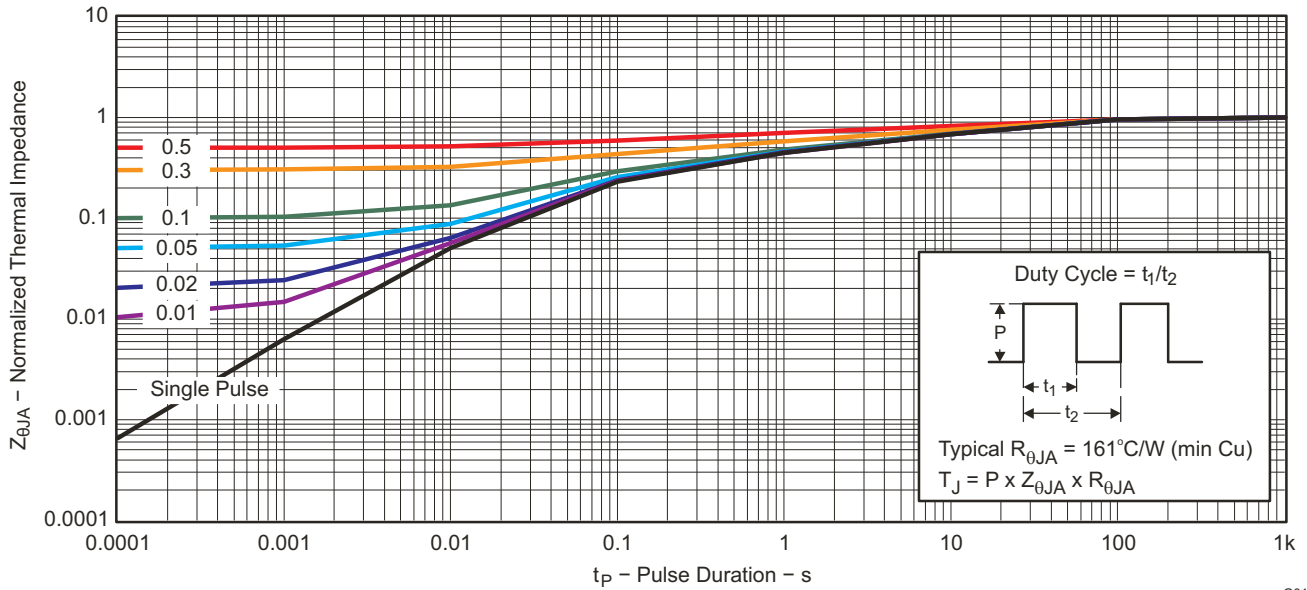


Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

Graphs are Per MOSFET at $T_A = 25^\circ\text{C}$, unless stated otherwise. Drain to Drain measurements are done with both MOSFETs in series (common source configuration).

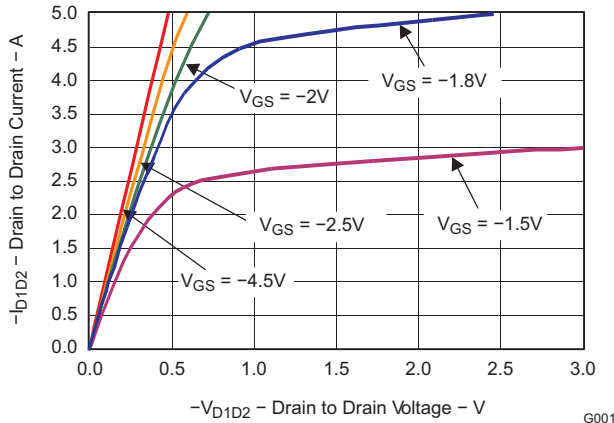


Figure 2. Saturation Characteristics

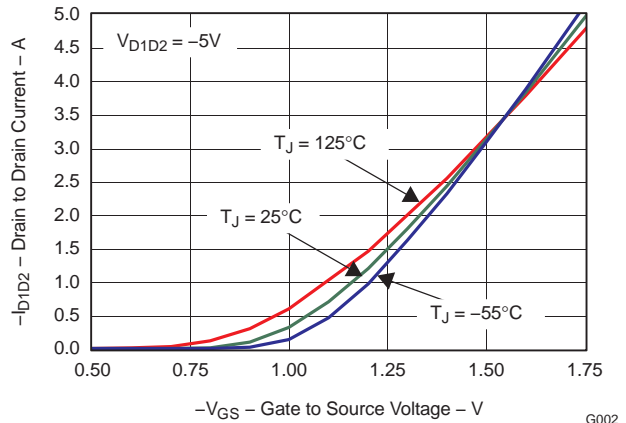


Figure 3. Transfer Characteristics

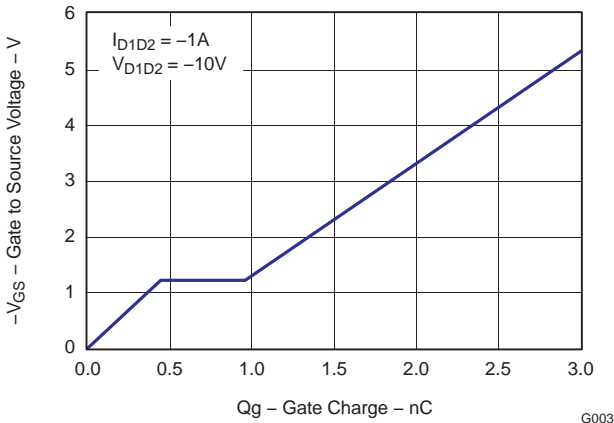


Figure 4. Gate Charge

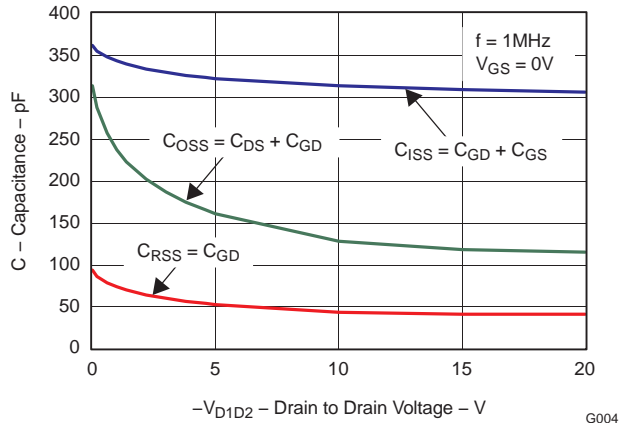


Figure 5. Capacitance

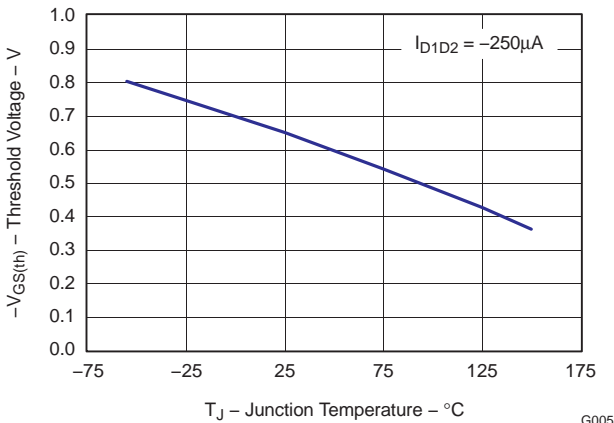


Figure 6. Threshold Voltage vs. Temperature

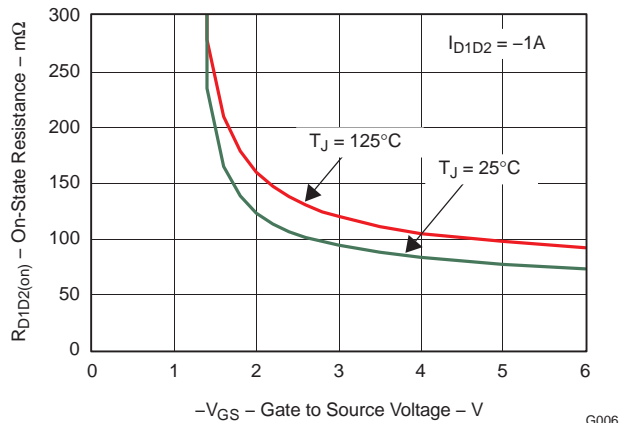


Figure 7. On-State Resistance vs. Gate to Source Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

Graphs are Per MOSFET at $T_A = 25^\circ\text{C}$, unless stated otherwise. Drain to Drain measurements are done with both MOSFETs in series (common source configuration).

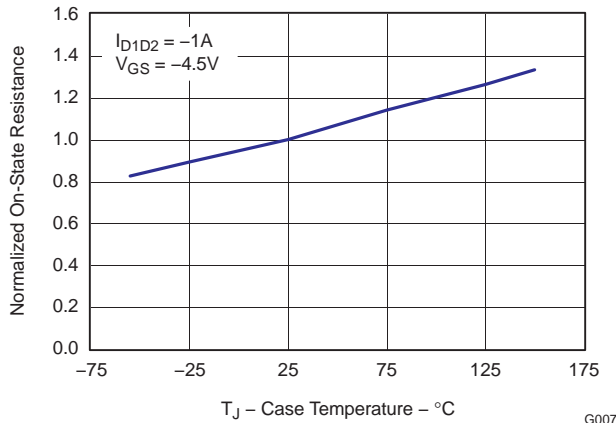


Figure 8. Normalized On-State Resistance vs. Temperature

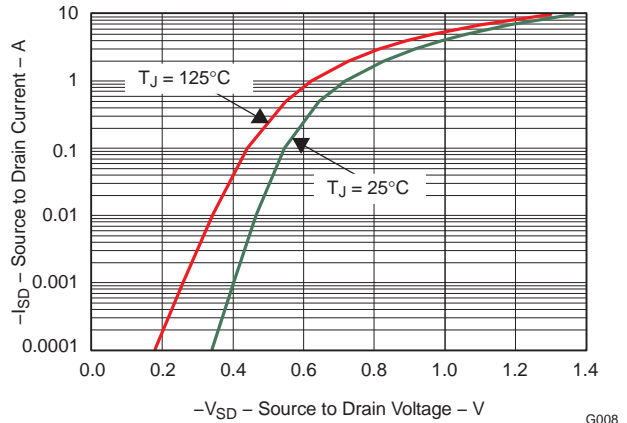


Figure 9. Typical Diode Forward Voltage

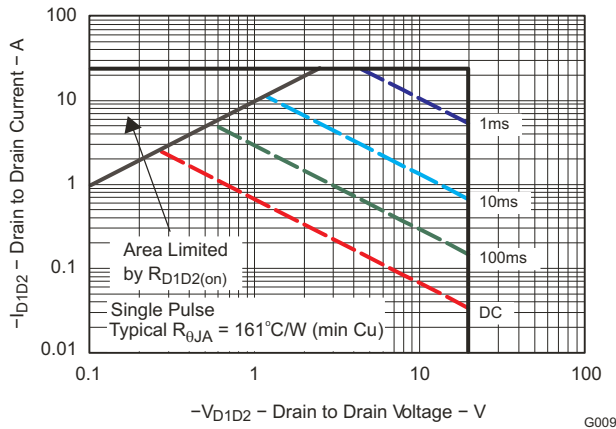


Figure 10. Maximum Safe Operating Area

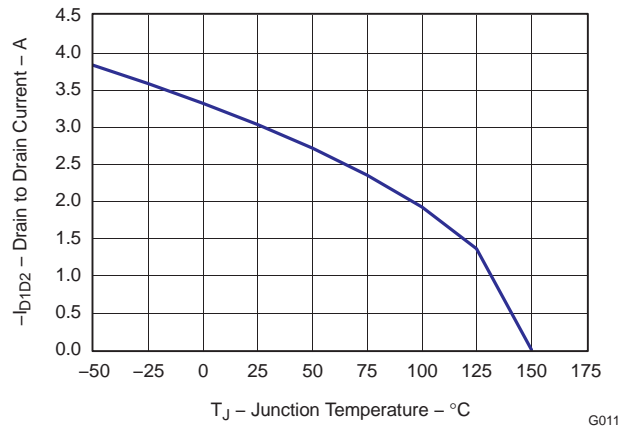
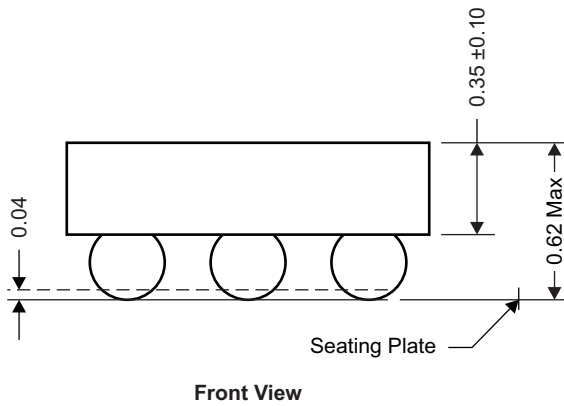
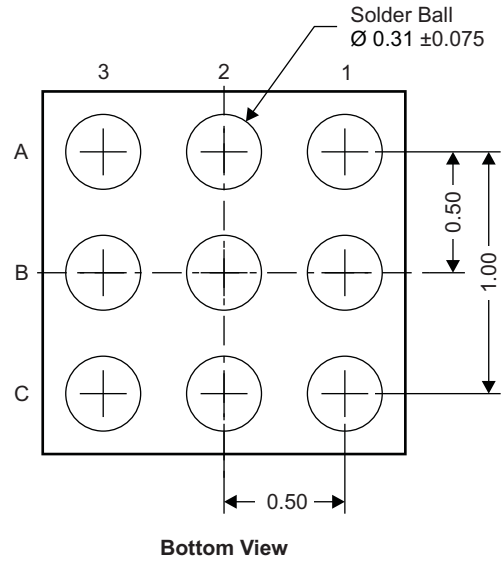
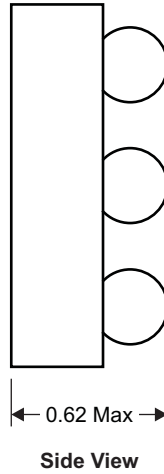
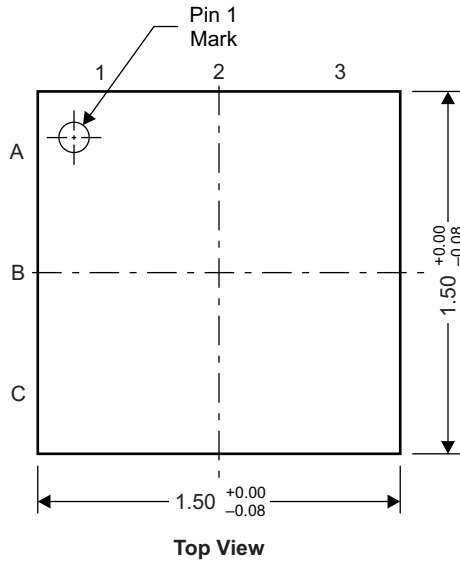


Figure 11. Maximum Drain Current vs. Temperature

MECHANICAL DATA

CSD75202W15 Package Dimensions



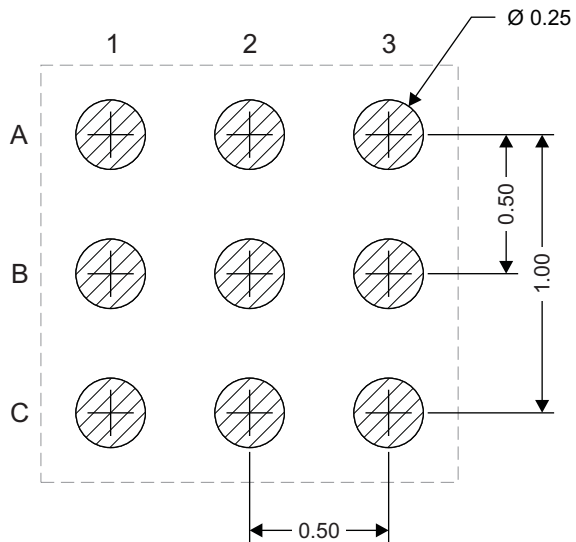
NOTE: All dimensions are in mm (unless otherwise specified)

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Pinout

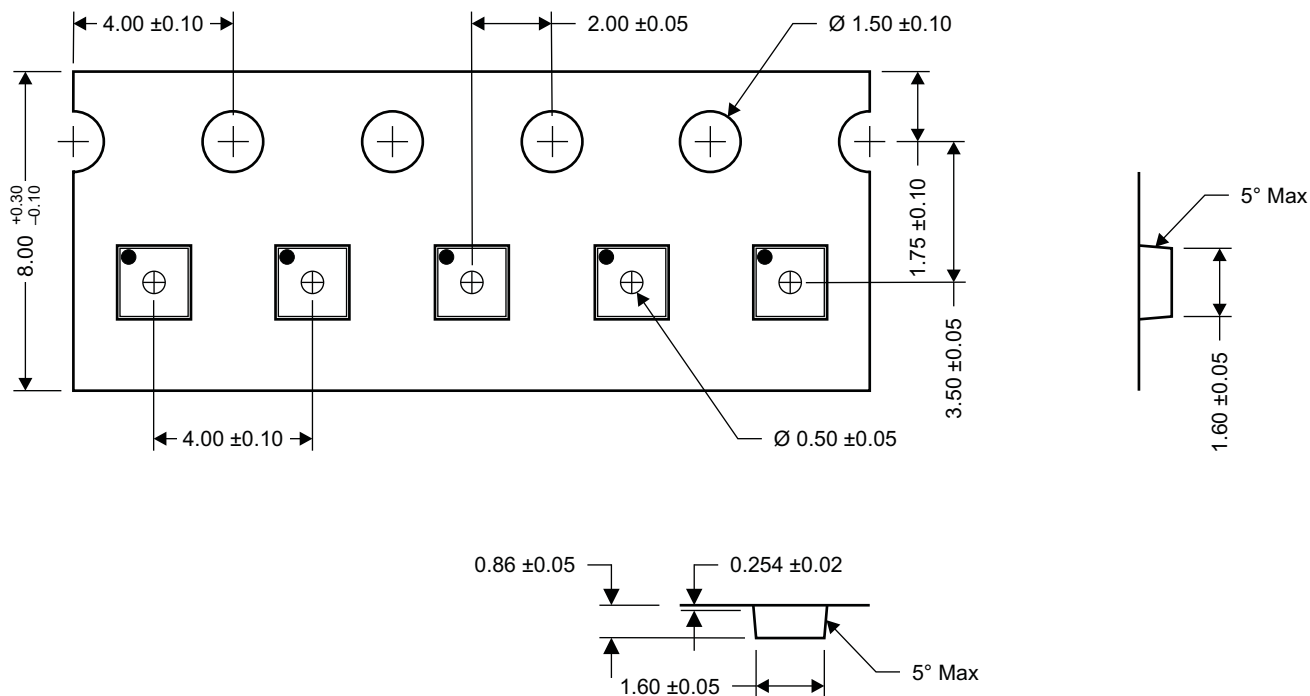
POSITION	DESIGNATION
A1	Gate1
A2, A3, B3	Drain1
C1	Gate2
C2, C3, B2	Drain2
B1	Source Sense

Land Pattern Recommendation



NOTE: All dimensions are in mm (unless otherwise specified)

Tape and Reel Information



NOTE: All dimensions are in mm (unless otherwise specified)

Package Marking Information

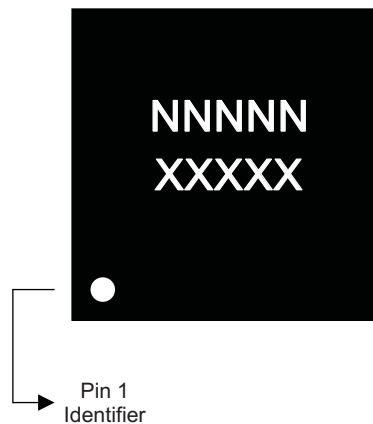
Location

1st Line

Product Code = NNNNN, First 5 digits after CSD (Fixed Text)

2nd Line

XXXXX = Last 5 digits of lot number (Variable Text)



M0174-01

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CSD75204W15	ACTIVE	DSBGA	YZF	9	3000	TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

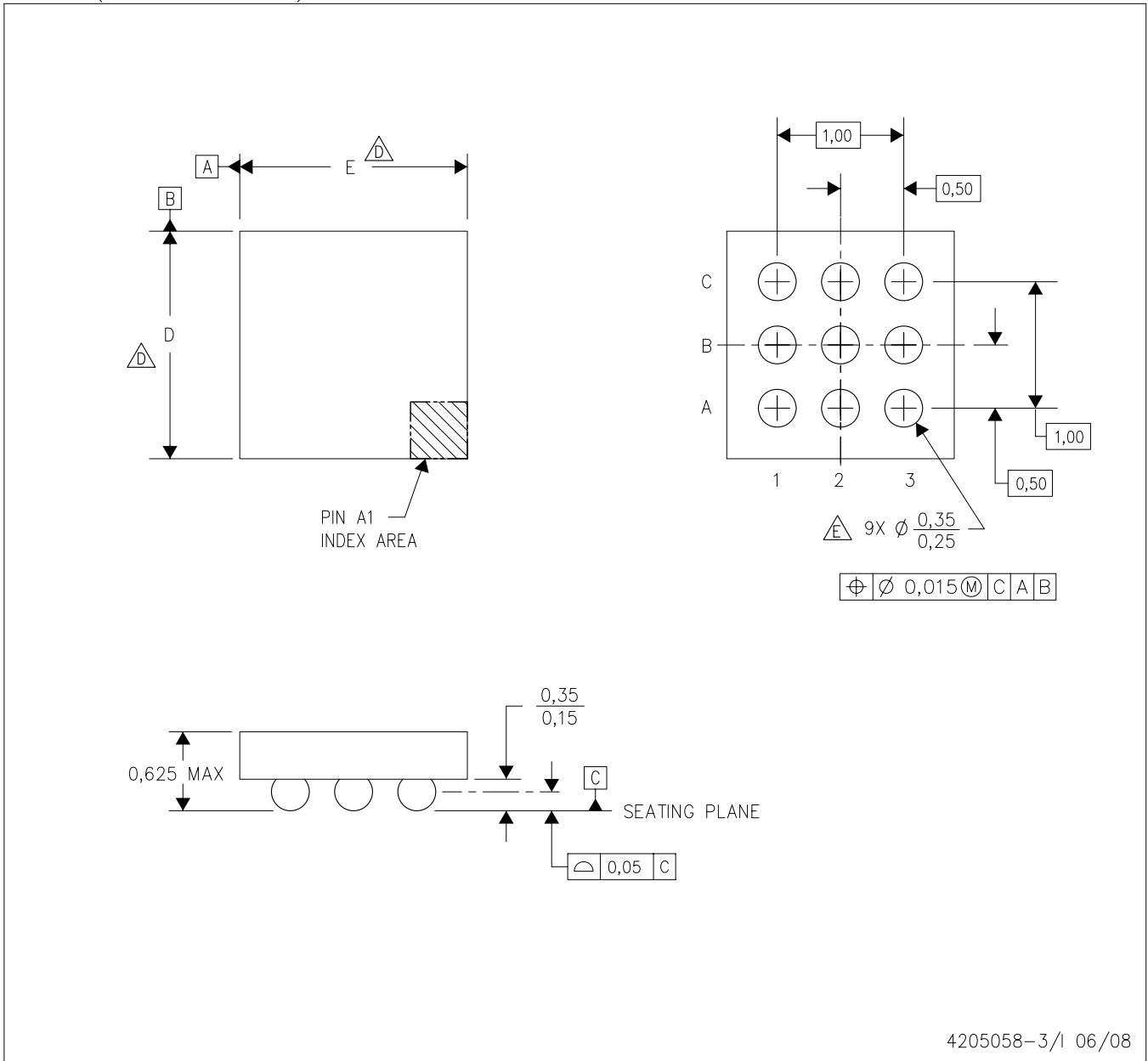
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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YZF (S-XBGA-N9)

DIE-SIZE BALL GRID ARRAY



4205058-3/1 06/08

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 -  Devices in YZF package can have dimension D ranging from 1.44 to 2.15 mm and dimension E ranging from 1.44 to 2.15 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
 - E. Reference Product Data Sheet for array population.
3 x 3 matrix pattern is shown for illustration only.
 - F. This package contains lead-free balls.
Refer to YEF (Drawing #4204181) for tin-lead (SnPb) balls.

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