

FDD5810

N-Channel Logic Level Trench® MOSFET

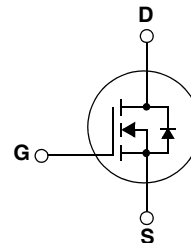
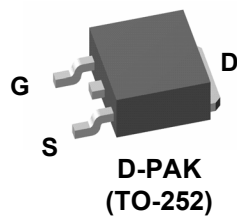
60V, 36A, 27mΩ

Features

- $R_{DS(ON)} = 22m\Omega$ (Typ.), $V_{GS} = 5V$, $I_D = 29A$
- $Q_{g(5)} = 13nC$ (Typ.), $V_{GS} = 5V$
- Low Miller Charge
- Low Q_{rr} Body Diode
- UIS Capability (Single Pulse / Repetitive Pulse)
- Qualified to AEC Q101
- RoHS Compliant

Applications

- Motor / Body Load Control
- ABS Systems
- Powertrain Management
- Injection System
- DC-DC converters and Off-line UPS
- Distributed Power Architecture and VRMs
- Primary Switch for 12V and 24V systems



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	60	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current Continuous ($V_{GS} = 10\text{V}$)	37	A
	Drain Current Continuous ($V_{GS} = 5\text{V}$)	33	A
	Continuous ($T_A = 25^\circ\text{C}$, $V_{GS} = 10\text{V}$, with $R_{\theta JA} = 52^\circ\text{C/W}$)	7.4	A
	Pulsed	Figure 4	A
E_{AS}	Single Pulse Avalanche Energy (Note 1)	45	mJ
P_D	Power Dissipation	72	W
	Derate above 25°C	0.48	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Maximum Thermal resistance Junction to Case TO-252	2.1	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-252, 1in ² copper pad area	52	$^\circ\text{C/W}$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD5810	FDD5810	TO-252AA	330mm	16mm	2500 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

B_{VDSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$	60	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 48\text{V}$	-	-	1	μA
		$V_{GS} = 0\text{V}$	-	-	250	
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	1	1.6	2	V
$R_{DS(ON)}$	Drain to Source On Resistance	$I_D = 32\text{A}$, $V_{GS} = 10\text{V}$	-	18	22	m Ω
		$I_D = 29\text{A}$, $V_{GS} = 5\text{V}$	-	22	27	
		$I_D = 32\text{A}$, $V_{GS} = 10\text{V}$, $T_J = 175^\circ\text{C}$	-	43	53	

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$	-	1420	1890	pF	
C_{oss}	Output Capacitance		-	150	200	pF	
C_{rss}	Reverse Transfer Capacitance		-	65	100	pF	
R_G	Gate Resistance	$f = 1\text{MHz}$	-	3.5	-	Ω	
Q_g	Total Gate Charge at 10V	$V_{GS} = 0\text{V}$ to 10V	$V_{DD} = 30\text{V}$ $I_D = 35\text{A}$	-	24	34	nC
Q_g	Total Gate Charge at 5V	$V_{GS} = 0\text{V}$ to 5V		-	13	18	nC
$Q_{g(th)}$	Threshold Gate Charge	$V_{GS} = 0\text{V}$ to 1V		-	1.3	-	nC
Q_{gs}	Gate to Source Gate Charge			-	4.0	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau			-	2.7	-	nC
Q_{gd}	Gate to Drain "Miller" Charge			-	5.0	-	nC

Switching Characteristics

t_{on}	Turn-On Time	$V_{DD} = 30V, I_D = 35A$ $V_{GS} = 5V, R_{GS} = 11\Omega$	-	-	130	ns
$t_{d(on)}$	Turn-On Delay Time		-	12	-	ns
t_r	Rise Time		-	75	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	26	-	ns
t_f	Fall Time		-	34	-	ns
t_{off}	Turn-Off Time		-	-	90	ns

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 32A$	-	-	1.25	V
		$I_{SD} = 16A$	-	-	1.0	V
t_{rr}	Reverse Recovery Time	$I_F = 35A, di/dt = 100A/\mu s$	-	-	39	ns
Q_{rr}	Reverse Recovery Charge	$I_F = 35A, di/dt = 100A/\mu s$	-	-	35	nC

Notes:

1: Starting $T_J = 25^\circ C, L = 110\mu H, I_{AS} = 28A, V_{DD} = 54V, V_{GS} = 10V.$

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

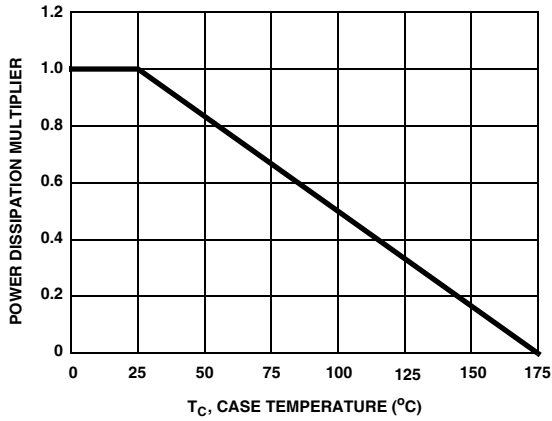


Figure 1. Normalized Power Dissipation vs Case Temperature

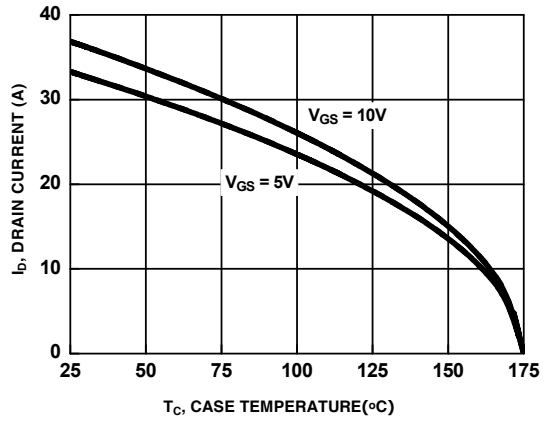


Figure 2. Maximum Continuous Drain Current vs Case Temperature

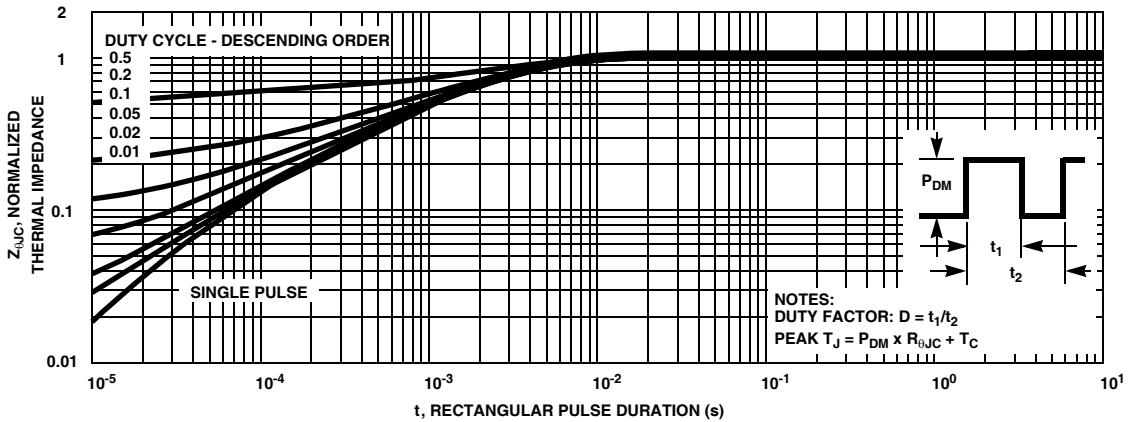


Figure 3. Normalized Maximum Transient Thermal Impedance

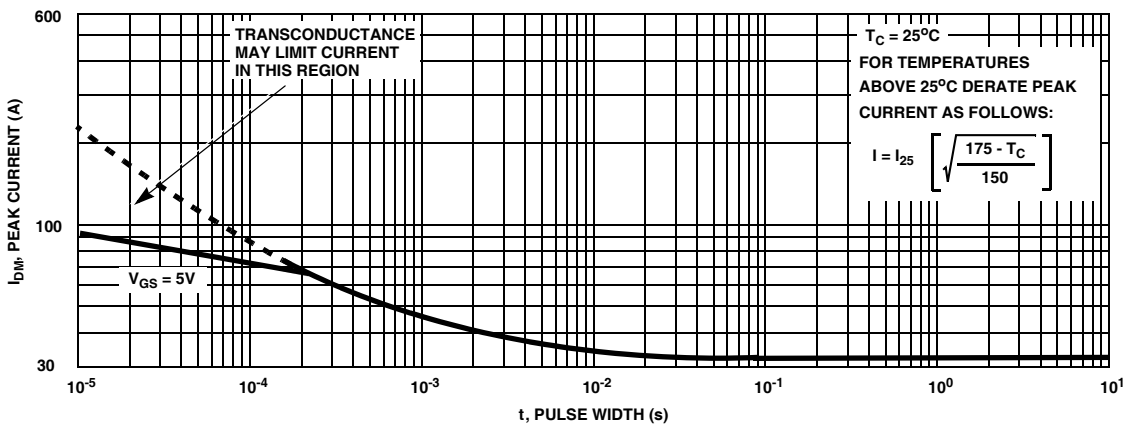


Figure 4. Peak Current Capability

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

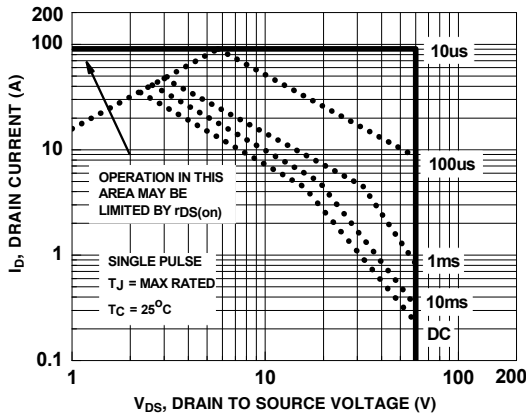
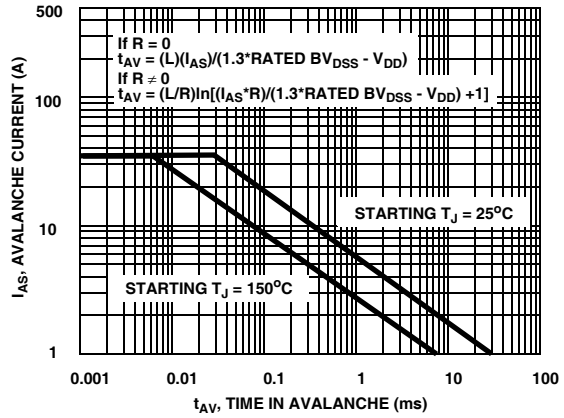


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515
Figure 6. Unclamped Inductive Switching Capability

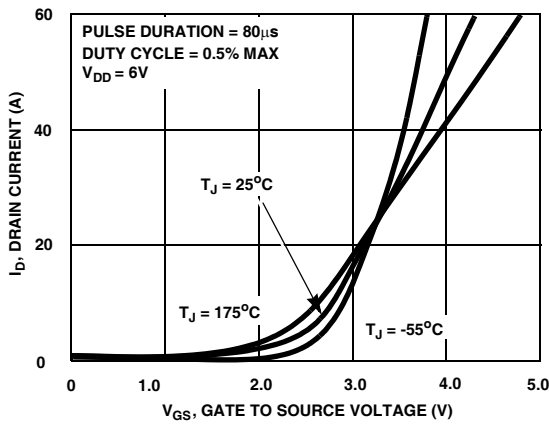


Figure 7. Transfer Characteristics

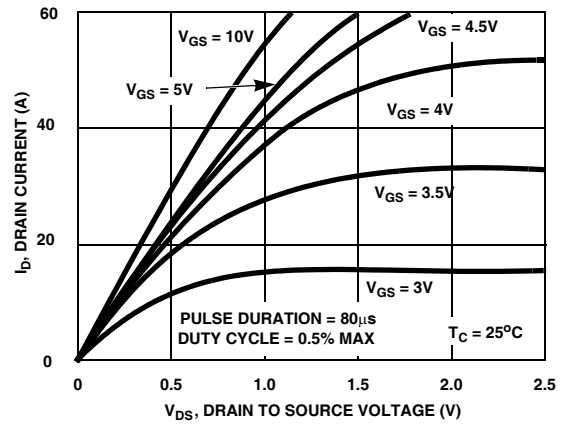


Figure 8. Saturation Characteristics

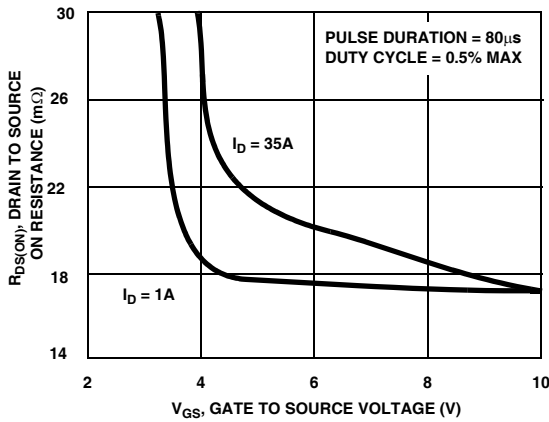


Figure 9. Drain to Source On Resistance vs Gate Voltage and Drain Current

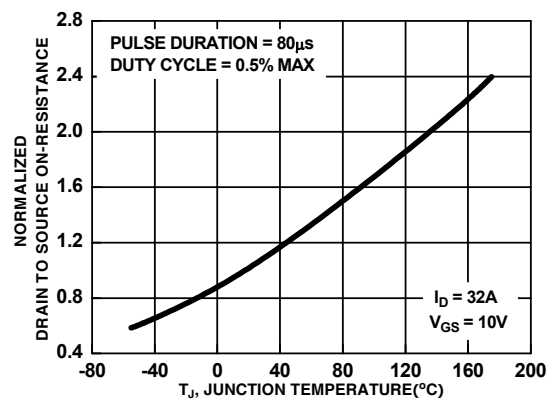


Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

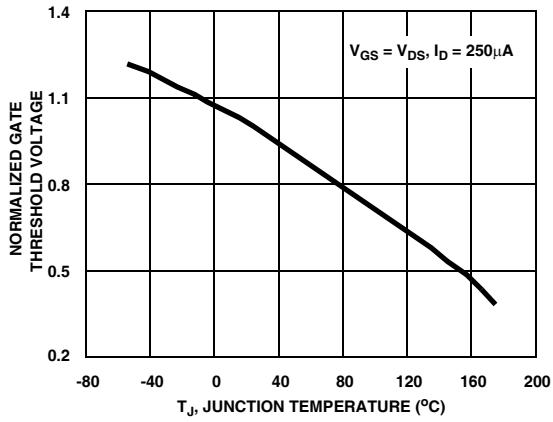


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

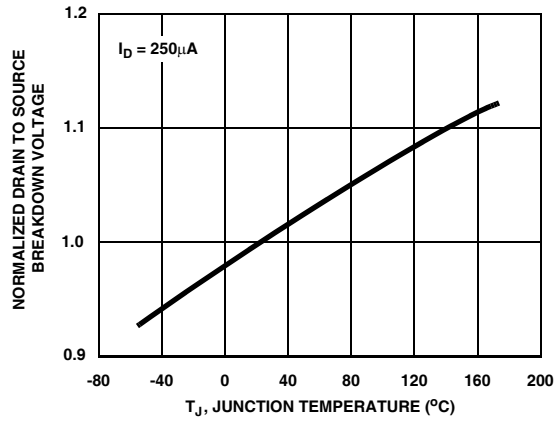


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

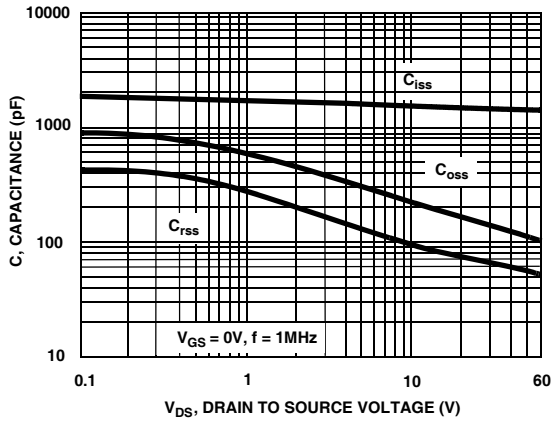


Figure 13. Capacitance vs Drain to Source Voltage

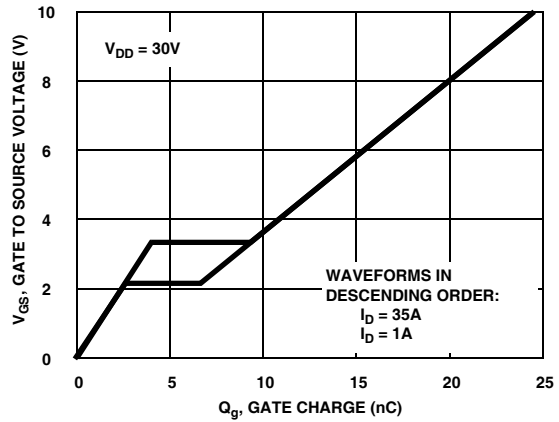


Figure 14. Gate Charge Waveforms for Constant Gate Current



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