

# FDD6796

## N-Channel PowerTrench® MOSFET

25 V, 40 A, 5.7 mΩ

### Features

- Max  $r_{DS(on)}$  = 5.7 mΩ at  $V_{GS} = 10$  V,  $I_D = 20$  A
- Max  $r_{DS(on)}$  = 9.0 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 15.5$  A
- 100% UIL tested
- RoHS Compliant

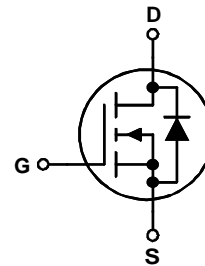
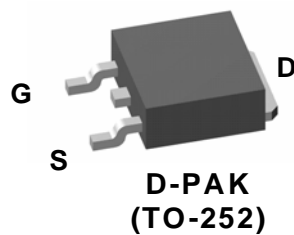


### General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low  $r_{DS(on)}$  and fast switching speed.

### Applications

- Vcore DC-DC for Desktop Computers and Servers
- VRM for Intermediate Bus Architecture



### MOSFET Maximum Ratings $T_C = 25$ °C unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	25	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current -Continuous (Package limited) $T_C = 25$ °C	40	A
	-Continuous (Silicon limited) $T_C = 25$ °C	69	
	-Continuous $T_A = 25$ °C (Note 1a)	20	
	-Pulsed	100	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	39	mJ
$P_D$	Power Dissipation $T_C = 25$ °C	42	W
	Power Dissipation $T_A = 25$ °C (Note 1a)	3.7	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +175	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	40	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD6796	FDD6796	D-PAK (TO-252)	13 "	12 mm	2500 units

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
--------	-----------	-----------------	-----	-----	-----	-------

### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	25			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		6.1		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 20\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$	1.0	1.9	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-6.6		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 20\text{ A}$		4.6	5.7	m $\Omega$
		$V_{GS} = 4.5\text{ V}$ , $I_D = 15.5\text{ A}$		6.6	9.0	
		$V_{GS} = 10\text{ V}$ , $I_D = 20\text{ A}$ , $T_J = 150\text{ }^\circ\text{C}$		6.8	8.5	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}$ , $I_D = 20\text{ A}$		138		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 13\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		1740	2315	pF
$C_{oss}$	Output Capacitance			325	430	pF
$C_{rss}$	Reverse Transfer Capacitance			290	435	pF
$R_g$	Gate Resistance			0.8	1.6	$\Omega$

### Switching Characteristics

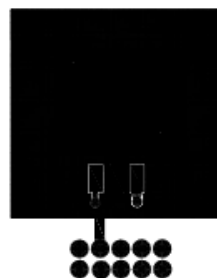
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 13\text{ V}$ , $I_D = 20\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		10	19	ns	
$t_r$	Rise Time			6	11	ns	
$t_{d(off)}$	Turn-Off Delay Time			23	37	ns	
$t_f$	Fall Time			4	10	ns	
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{ V to } 10\text{ V}$		29	41	nC
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{ V to } 4.5\text{ V}$		15	21	nC
$Q_{gs}$	Gate to Source Charge	$V_{DD} = 13\text{ V}$ , $I_D = 20\text{ A}$		4.9		nC	
$Q_{gd}$	Gate to Drain "Miller" Charge			6.2		nC	

### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 3.1\text{ A}$ (Note 2)		0.8	1.2	V
		$V_{GS} = 0\text{ V}$ , $I_S = 20\text{ A}$ (Note 2)		0.9	1.3	
$t_{rr}$	Reverse Recovery Time	$I_F = 20\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		15	26	ns
$Q_{rr}$	Reverse Recovery Charge			3	10	nC

#### Notes:

- 1:  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.



a)  $40\text{ }^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper



b)  $96\text{ }^\circ\text{C/W}$  when mounted on a minimum pad

- 2: Pulse Test: Pulse Width  $< 300\text{ }\mu\text{s}$ , Duty cycle  $< 2.0\%$ .  
 3: Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 0.1\text{ mH}$ ,  $I_{AS} = 28\text{ A}$ ,  $V_{DD} = 23\text{ V}$ ,  $V_{GS} = 10\text{ V}$ .

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

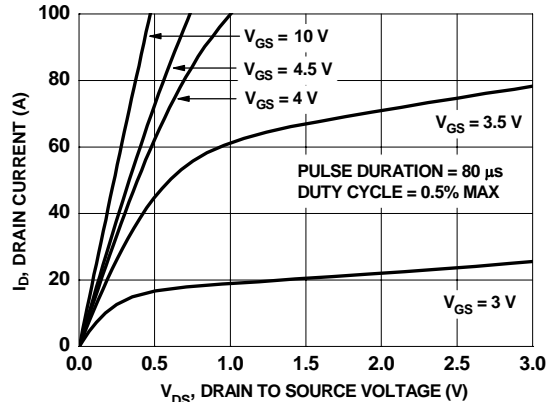


Figure 1. On Region Characteristics

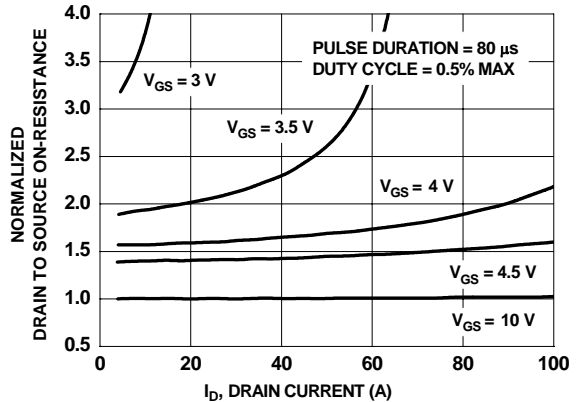


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

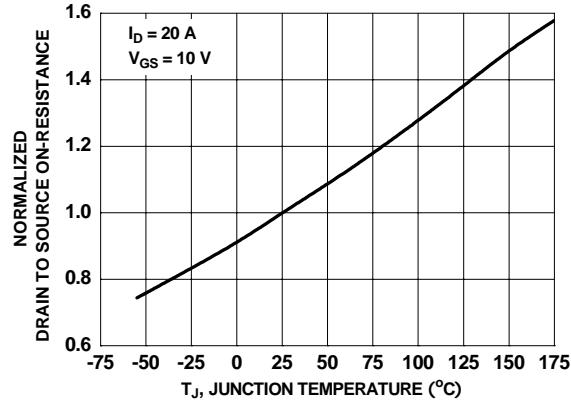


Figure 3. Normalized On Resistance vs Junction Temperature

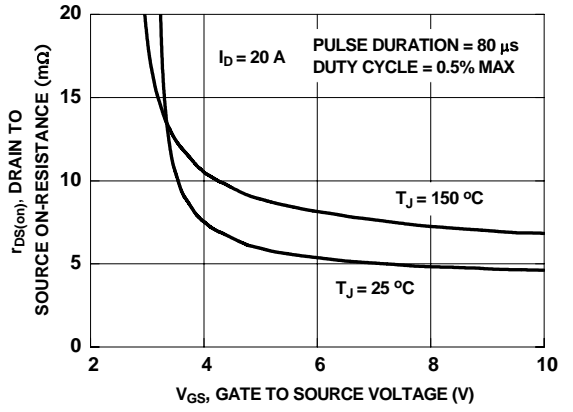


Figure 4. On-Resistance vs Gate to Source Voltage

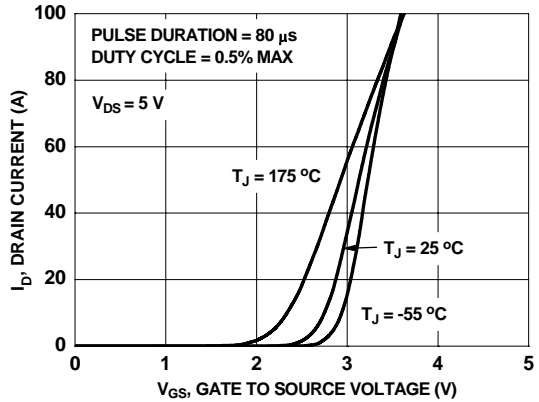


Figure 5. Transfer Characteristics

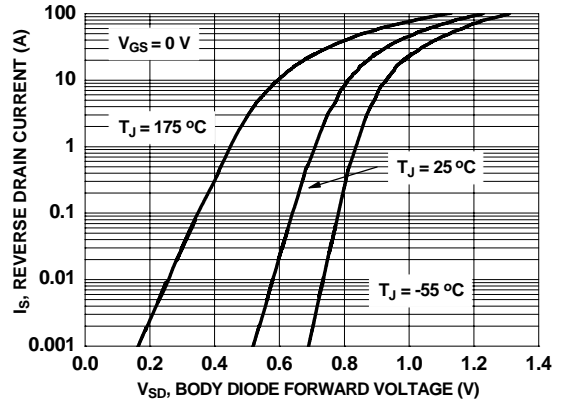
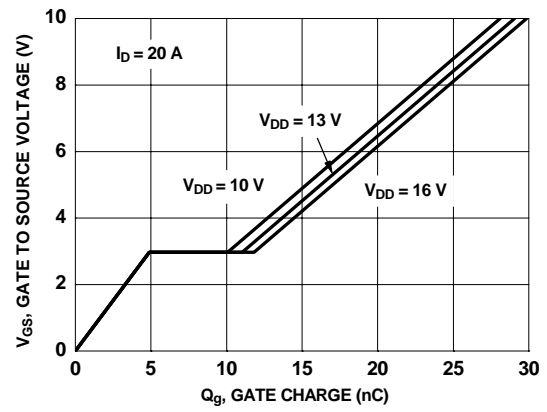
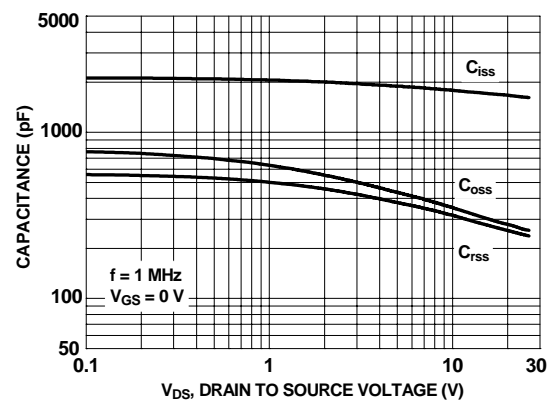


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

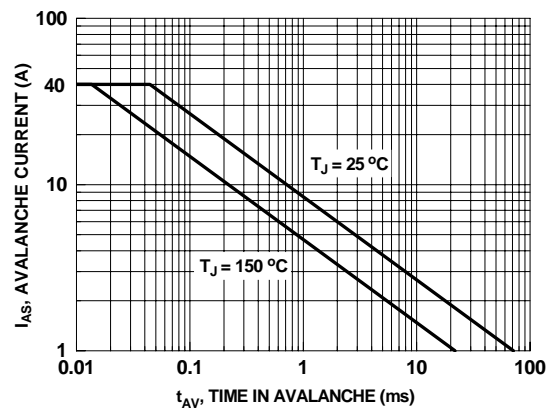
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



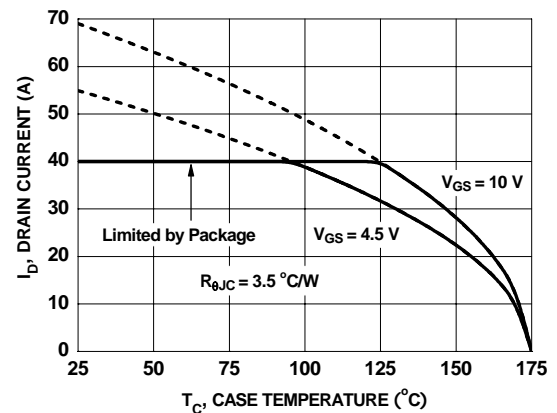
**Figure 7. Gate Charge Characteristics**



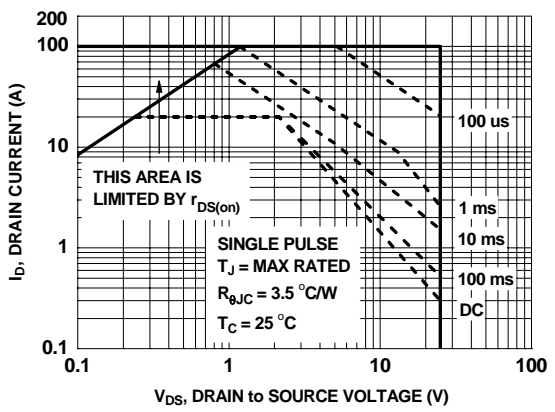
**Figure 8. Capacitance vs Drain to Source Voltage**



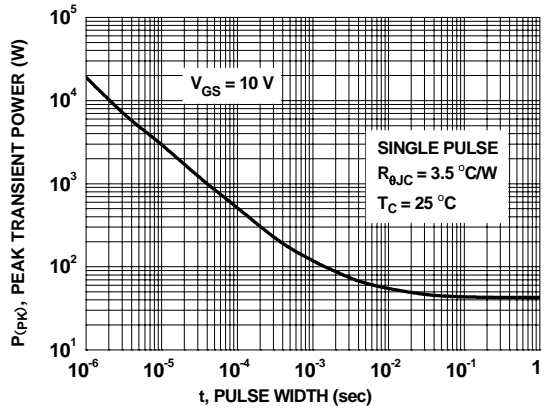
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

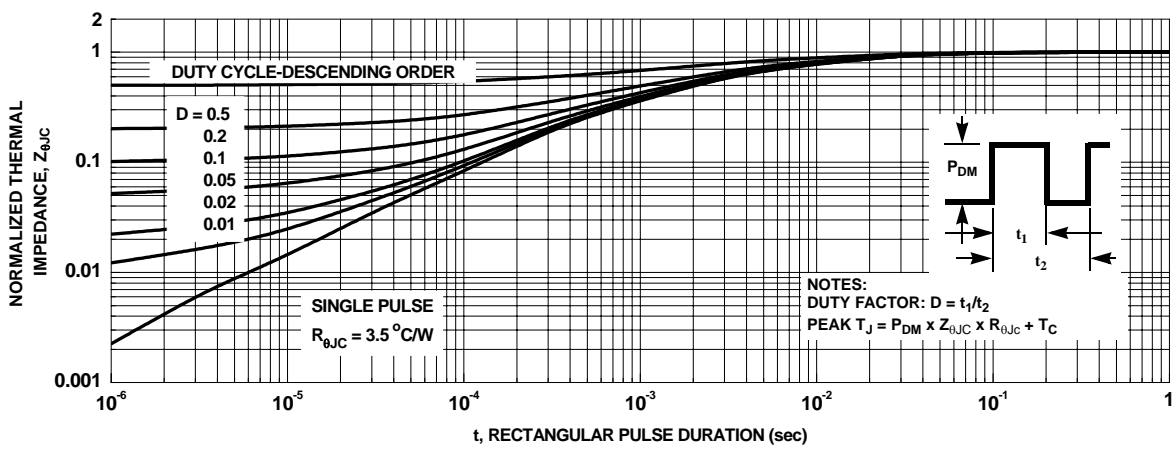


**Figure 11. Forward Bias Safe Operating Area**

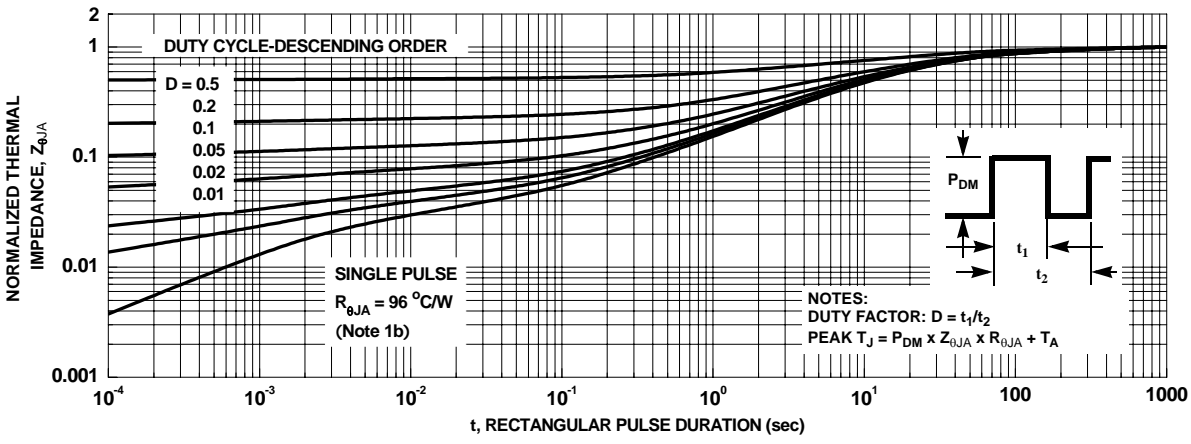


**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 13. Junction-to-Case Transient Thermal Response Curve**





**Figure 14. Junction-to-Ambient Transient Thermal Response Curve**



**TRADEMARKS**

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

- |   |   |   |   |
|---|---|---|---|
| ACEx®   | FPS™  | PDP-SPM™  | The Power Franchise®  |
| Build it Now™   | F-PFS™  | Power-SPM™  | <b>power</b><br>the franchise   |
| CorePLUS™   | FRFET®  | PowerTrench®  | TinyBoost™  |
| CorePOWER™  | Global Power ResourceSM   | Programmable Active Droop™  | TinyBuck™   |
| CROSSVOLT™  | Green FPS™  | QFET®   | TinyLogic®  |
| CTL™  | Green FPS™ e-Series™  | QS™   | TINYOPTO™   |
| Current Transfer Logic™   | GTO™  | Quiet Series™   | TinyPower™  |
| EcoSPARK®   | IntelliMAX™   | RapidConfigure™   | TinyPWM™  |
| EfficientMax™   | ISOPLANAR™  | Saving our world 1mW at a time™   | TinyWire™   |
| EZSWITCH™ *   | MegaBuck™   | SmartMax™   | µSerDes™  |
|  | MICROCOUPLER™   | SMART START™  |  |
|  | MicroFET™   | SPM®  | UHC®  |
| Fairchild®  | MicroPak™   | STEALTH™  | Ultra FRFET™  |
| Fairchild Semiconductor®  | MillerDrive™  | SuperFET™   | UniFET™   |
| FACT Quiet Series™  | MotionMax™  | SuperSOT™-3   | VCX™  |
| FACT®   | Motion-SPM™   | SuperSOT™-6   | VisualMax™  |
| FAST®   | OPTOLOGIC®  | SuperSOT™-8   |   |
| FastvCore™  | OPTOPLANAR®   | SuperMOS™   |   |
| FlashWriter® *  |  |  |   |

\* EZSWITCH™ and FlashWriter® are trademarks of System General Corporation, used under license by Fairchild Semiconductor.

**DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
- A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**PRODUCT STATUS DEFINITIONS**

**Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	This datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I34