FAIRCHILD
SEMICONDUCTOR®

April 2008

FDMA430NZ

Single N-Channel 2.5V Specified PowerTrench® MOSFET

30V, 5.0A, 40mΩ

General Description

This Single N-Channel MOSFET has been designed using Fairchild Semiconductor's advanced Power Trench process to optimize the $R_{DS}(on)$ @V_{GS}=2.5V on special MicroFET leadframe.
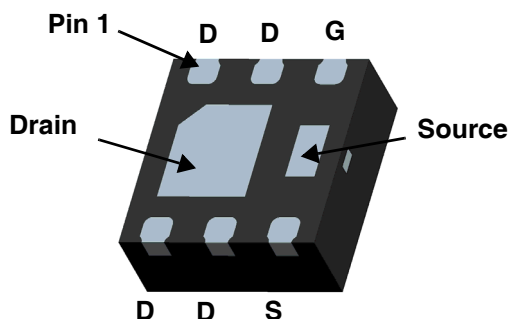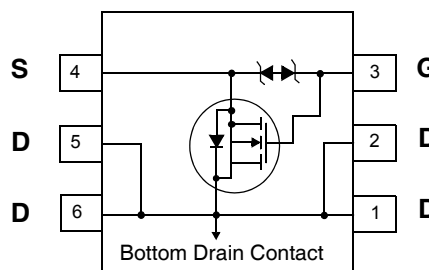
Applications

■ Li-Ion Battery Pack

Features

■ $R_{DS(on)}$ = 40mΩ @ V_{GS} = 4.5 V, I_D = 5.0A

■ $R_{DS(on)}$ = 50mΩ @ V_{GS} = 2.5 V, I_D = 4.5A

■ Low Profile-0.8mm maximum-in the new package MicroFET 2x2 mm

■ HBM ESD protection level > 2.5k V typical (Note 3)

■ RoHS Compliant

MicroFET 2X2 (Bottom View)

Pin 1, D, D, G, Drain, Source, D, D, S

S 4, G 3, D 5, D 2, D 6, D 1

Bottom Drain Contact

Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		±12	V
I_D	Drain Current -Continuous	(Note 1a)	5.0	A
	-Pulsed		20	
P_D	Power dissipation (Steady State)	(Note 1a)	0.9	W
		(Note 1b)	2.4	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	145	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1b)	52	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
430	FDMA430NZ	7"	12mm	3000 units

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Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V , I_D = 250µA	30			V
$\dfrac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250µA, Referenced to 25°C		25.2		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24V, V_{GS} = 0V,			1	µA
I_{GSS}	Gate-Body Leakage,	V_{GS} = ±12V, V_{DS} = 0V			±10	µA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	0.6	0.81	1.5	V
$\dfrac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250µA, Referenced to 25°C		-3.2		mV/°C
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 4.5V, I_D = 5.0A		23.6	40	mΩ
		V_{GS} = 4.0V, I_D = 5.0A		23.9	41	
		V_{GS} = 3.1V, I_D =4.5A		25.4	43	
		V_{GS} = 2.5V, I_D =4.5A		27.6	50	
		V_{GS} = 4.5V, I_D =5.0A, T_J =150°C		37.0	61	
g_{FS}	Forward Transconductance	V_{DS} = 5V, I_D =5.0A		25.6		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 10V, V_{GS} =0V, f = 1.0MHz		600	800	pF
C_{oss}	Output Capacitance			110	150	pF
C_{rss}	Reverse Transfer Capacitance			75	115	pF
R_G	Gate Resistance	f = 1.0MHz		3.5		Ω
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 10V, I_D = 1A V_{GS} = 4.5V, R_{GEN} = 6Ω		8.3	17	ns
t_r	Turn-On Rise Time			7.1	15	ns
$t_{d(off)}$	Turn-Off Delay Time			18.1	37	ns
t_f	Turn-Off Fall Time			6.0	12	ns
Q_g	Total Gate Charge	V_{DS} = 10V, I_D = 5.0A, V_{GS} = 4.5V		7.3	11	nC
Q_{gs}	Gate-Source Charge			0.8	2	nC
Q_{gd}	Gate-Drain Charge			1.9	3	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current				2.0	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0V, I_S = 2.0A		0.69	1.2	V
t_{rr}	Diode Reverse Recovery Time	I_F = 5.0A, di/dt = 100A/µs			17	ns
Q_{rr}	Diode Reverse Recovery Charge				5	nC

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.
    a.   145°C/W when mounted on a minimum pad of 2 oz copper
    b.   52°C/W when mounted on a 1 in² pad of 2 oz copper
2. Pulse Test: Pulse Width < 300 µs, Duty Cycle < 2.0%
3. The diode connected between the gate and the source serves only as proection against ESD. No gate overvoltage rating is implied.

FDMA430NZ Single N-Channel 2.5V specified PowerTrench® MOSFET

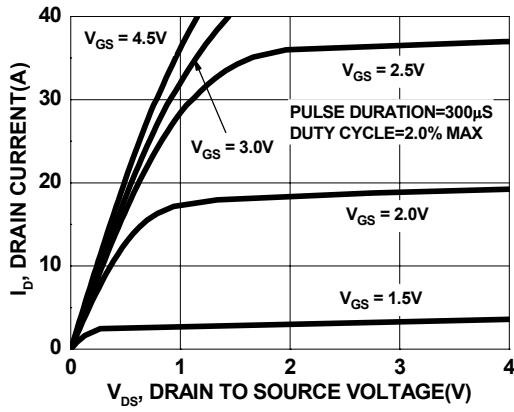**Typical Characteristics** T_J = 25°C unless otherwise noted
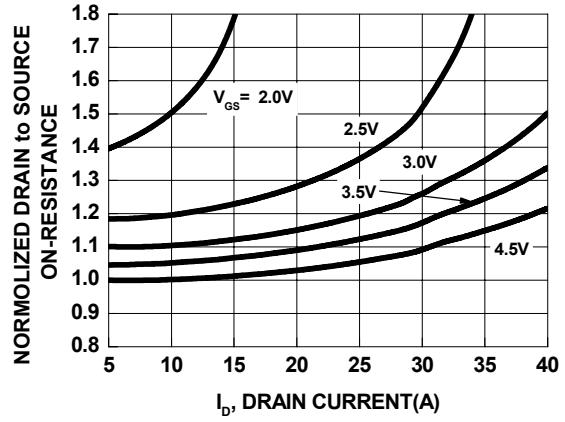
Figure 1. On Region Characteristics

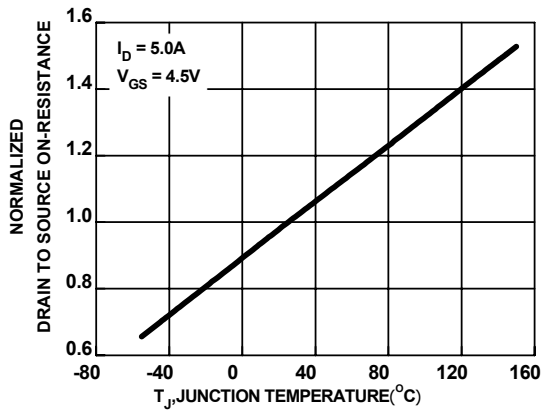Figure 2. On-Resistance vs Drain Current and Gate Voltage

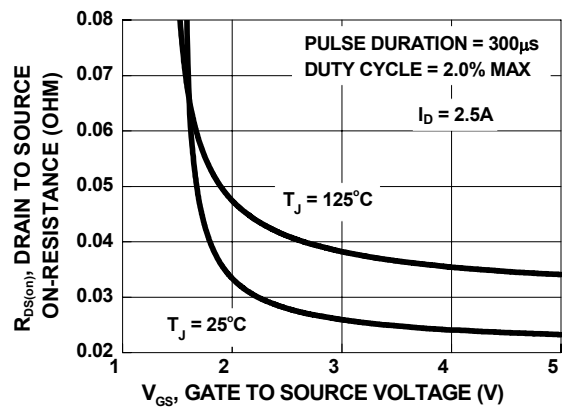Figure 3. Normalized On Resistance vs Junction Temperature

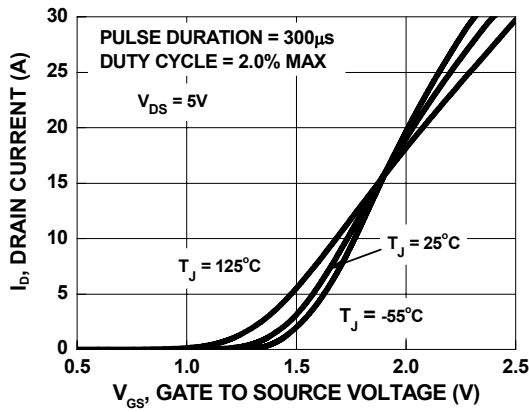Figure 4. On-Resistance vs Gate to Source Votlage
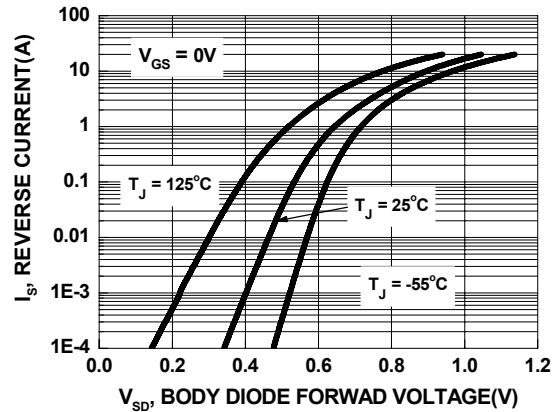

Figure 5. Transfer Characteristics

Figure 6. Source to Drain Diode Forward Voltage vs Source Current

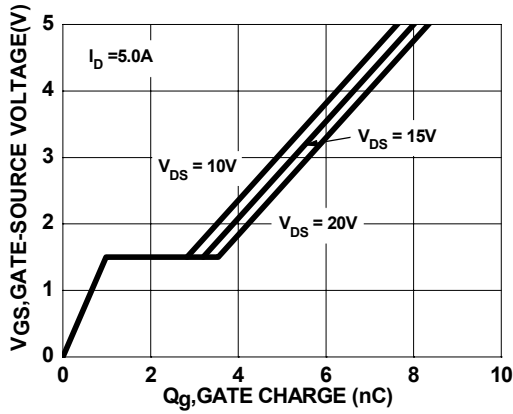## Typical Characteristics T_J = 25°C unless otherwise noted

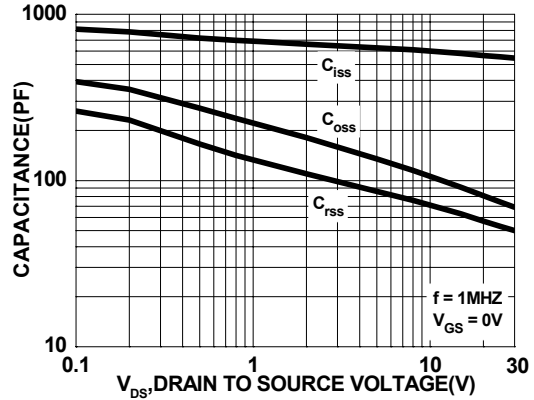**Figure 7. Gate Charge Characteristics**

Figure 8. Capacitance vs Drain to Source Voltage
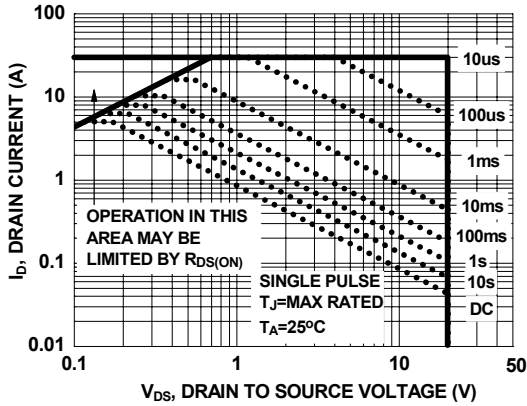

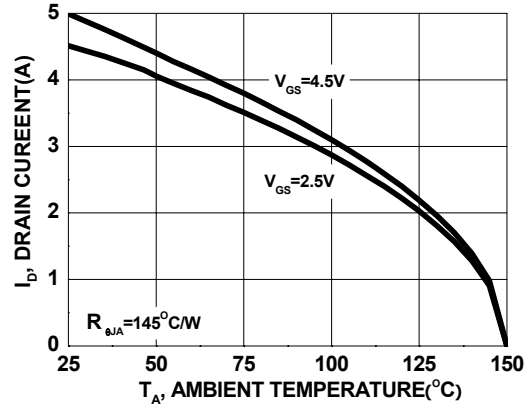**Figure 9. Safe Operating Area**

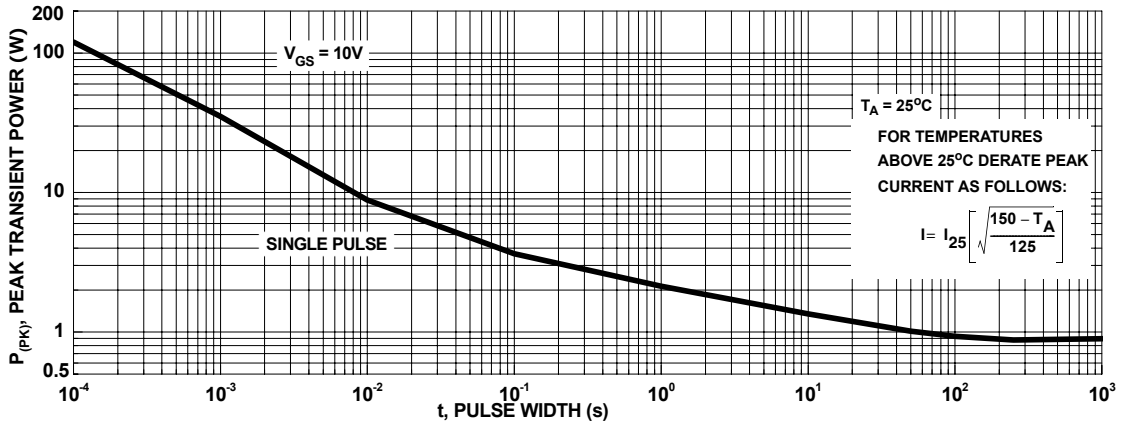**Figure 10. Maximum Continuous Drain Current vs Ambient Temperature**

Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25°C unless otherwise noted
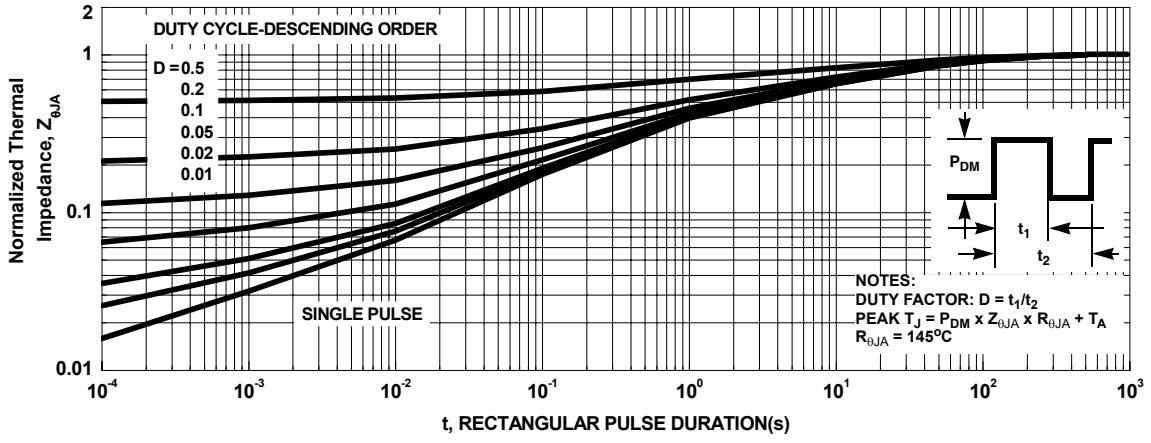
Figure 12. Transient Thermal Response Curve

DUTY CYCLE-DESCENDING ORDER

D = 0.5
0.2
0.1
0.05
0.02
0.01

SINGLE PULSE

Normalized Thermal Impedance, $Z_{\theta JA}$

t, RECTANGULAR PULSE DURATION(s)

NOTES:
DUTY FACTOR: D = t_1/t_2
PEAK T_J = P_{DM} x $Z_{\theta JA}$ x $R_{\theta JA}$ + T_A
$R_{\theta JA}$ = 145°C

Dimensional Outline and Pad Layout

2X | 0.10 | C

2.000   A

B

2.000

PIN#1 LOCATION

TOP VIEW   2X | 0.10 | C

0.8 MAX

// | 0.10 | C

(0.20)

0.08 | C   0.05 0.00

SEATING PLANE

SIDE VIEW   C

PIN #1 IDENT

(0.30)

1.000 0.800

1   3

0.33 0.20

(0.56)   1.05 0.95

6   4

0.65

1.30   0.25~0.35

⊕ | 0.10 Ⓜ | C | A | B
     0.05 Ⓜ | C

BOTTOM VIEW

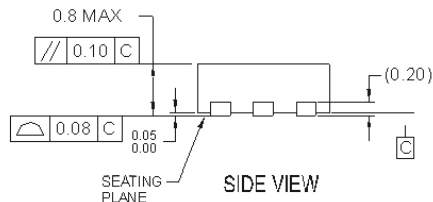NO DRAIN OR GATE TRACES ALLOWED IN THIS AREA

1.00

6   4

1.05   0.66   1.35   2.30

(0.47)

1   3

0.65 TYP   0.40 TYP

RECOMMENDED LAND PATTERN OPT 1

1.00

6   4

1.05   0.66   1.35   2.30

(0.47)

1   3

0.65 TYP   0.40 TYP

RECOMMENDED LAND PATTERN OPT 2

NOTES:

A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-229 DATED AUG/2003
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
D. DRAWING FILENAME: MKT-MLP06Lrev2.

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