

MOSFET

Metal Oxide Semiconductor Field Effect Transistor

CoolMOS C6

600V CoolMOS™ C6 Power Transistor
IPx60R950C6

Data Sheet

Rev. 2.0, 2009-08-28
Final

Industrial & Multimarket

600V CoolMOS™ C6 Power Transistor

IPD60R950C6, IPB60R950C6
IPP60R950C6, IPA60R950C6

1 Description

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ C6 series combines the experience of the leading SJ MOSFET supplier with high class innovation. The resulting devices provide all benefits of a fast switching SJ MOSFET while not sacrificing ease of use. Extremely low switching and conduction losses make switching applications even more efficient, more compact, lighter, and cooler.

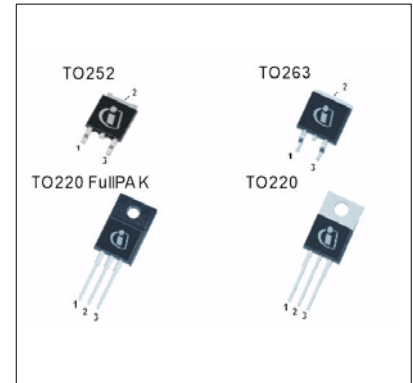
Features

- Extremely low losses due to very low FOM $R_{DS(on)} \cdot Q_g$ and E_{oss}
- Very high commutation ruggedness
- Easy to use/drive
- JEDEC¹⁾ qualified, Pb-free plating

Applications

PFC stages, hard switching PWM stages and resonant switching PWM stages for e.g. PC Silverbox, Adapter, LCD & PDP TV, Lighting, Server, Telecom, UPS and Solar.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.



RoHS

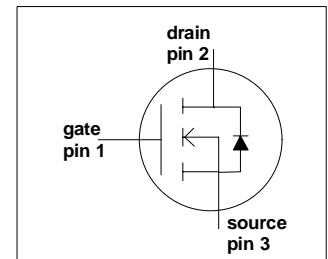


Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	650	V
$R_{DS(on),max}$	0.95	Ω
$Q_{g,typ}$	13	nC
$I_{D,pulse}$	12	A
$E_{oss} @ 400V$	1.3	μJ
Body diode dv/dt	500	V/ns

Type / Ordering Code	Package	Marking	Related Links
IPD60R950C6	PG-TO252	6R950C6	IFX C6 Product Brief IFX C6 Portfolio IFX CoolMOS Webpage IFX Design tools
IPB60R950C6	PG-TO263		
IPP60R950C6	PG-TO220		
IPA60R950C6	PG-TO220 FullPAK		

1) J-STD20 and JESD22

Table of Contents

Description	2
Table of Contents	3
Maximum Ratings	4
Thermal characteristics	5
Electrical characteristics	6
Electrical characteristics diagrams	8
Test circuits	13
Package outlines	14
Revision History	18

2 Maximum Ratings

at $T_j = 25\text{ °C}$, unless otherwise specified.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	4.4	A	$T_C = 25\text{ °C}$
				2.8		$T_C = 100\text{ °C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	12	A	$T_C = 25\text{ °C}$
Avalanche energy, single pulse	E_{AS}	-	-	46	mJ	$I_D = 0.8\text{ A}$, $V_{DD} = 50\text{ V}$ (see table 21)
Avalanche energy, repetitive	E_{AR}	-	-	0.13		$I_D = 0.8\text{ A}$, $V_{DD} = 50\text{ V}$
Avalanche current, repetitive	I_{AR}	-	-	0.8	A	
MOSFET dv/dt ruggedness	dv/dt	-	-	50	V/ns	$V_{DS} = 0 \dots 480\text{ V}$
Gate source voltage	V_{GS}	-20	-	20	V	static
		-30		30		AC ($f > 1\text{ Hz}$)
Power dissipation for TO-220, TO-252, TO-263	P_{tot}	-	-	37	W	$T_C = 25\text{ °C}$
Power dissipation for TO-220 FullPAK	P_{tot}	-	-	26	W	$T_C = 25\text{ °C}$
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	
Mounting torque TO-220		-	-	60	Ncm	M3 and M3.5 screws
				50		M2.5 screws
TO-220FP				50		
Continuous diode forward current	I_S	-	-	3.9	A	$T_C = 25\text{ °C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	12	A	$T_C = 25\text{ °C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	15	V/ns	$V_{DS} = 0 \dots 480\text{ V}$, $I_{SD} \leq I_D A$, $T_j = 125\text{ °C}$
Maximum diode commutation speed ³⁾	di/dt			500	A/μs	(see table 22)

1) Limited by $T_{j,max}$. Maximum duty cycle $D = 0.75$

2) Pulse width t_p limited by $T_{j,max}$

3) Identical low side and high side switch with identical R_G

3 Thermal characteristics

Table 3 Thermal characteristics TO-220 (IPP60R950C6)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	3.41	°C/W	leaded
Thermal resistance, junction - ambient	R_{thJA}	-	-	62		
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6 mm (0.063 in.) from case for 10 s

Table 4 Thermal characteristics TO-220FullIPAK (IPA60R950C6)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	4.9	°C/W	leaded
Thermal resistance, junction - ambient	R_{thJA}	-	-	80		
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6 mm (0.063 in.) from case for 10 s

Table 5 Thermal characteristics TO-263 (IPB60R950C6),TO-252 (IPD60R950C6)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	3.41	°C/W	SMD version, device on PCB, minimal footprint
Thermal resistance, junction - ambient	R_{thJA}	-	-	62		
				35		
Soldering temperature, wave- & reflowsolderin allowed	T_{sold}	-	-	260	°C	reflow MSL1

1) Device on 40mm*40mm*1.5 epoxy PCB FR4 with 6cm² (one layer, 70µm thick) copper area for drain connection. PCB is vertical without air stream cooling

4 Electrical characteristics

Electrical characteristics, at $T_J=25\text{ °C}$, unless otherwise specified

Table 6 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	$V_{GS}=0\text{ V}, I_D=0.25\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.5	3	3.5		$V_{DS}=V_{GS}, I_D=0.13\text{ mA}$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=600\text{ V}, V_{GS}=0\text{ V}, T_J=25\text{ °C}$
		-	10	-		$V_{DS}=600\text{ V}, V_{GS}=0\text{ V}, T_J=150\text{ °C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.86	0.95	Ω	$V_{GS}=10\text{ V}, I_D=1.5\text{ A}, T_J=25\text{ °C}$
		-	2.22	-		$V_{GS}=10\text{ V}, I_D=1.5\text{ A}, T_J=150\text{ °C}$
Gate resistance	R_G	-	16	-	Ω	$f=1\text{ MHz}, \text{open drain}$

Table 7 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition	
		Min.	Typ.	Max.			
Input capacitance	C_{iss}	-	280	-	pF	$V_{GS}=0\text{ V}, V_{DS}=100\text{ V}, f=1\text{ MHz}$	
Output capacitance	C_{oss}	-	21	-			
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	-	14	-			$V_{GS}=0\text{ V}, V_{DS}=0\dots480\text{ V}$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	-	57	-			$I_D=\text{constant}, V_{GS}=0\text{ V}, V_{DS}=0\dots480\text{ V}$
Turn-on delay time	$t_{d(on)}$	-	10	-	ns	$V_{DD}=400\text{ V}, V_{GS}=10\text{ V}, I_D=1.9\text{ A}, R_G=12.2\text{ }\Omega$ (see table 20)	
Rise time	t_r	-	8	-			
Turn-off delay time	$t_{d(off)}$	-	60	-			
Fall time	t_f	-	13	-			

1) $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

2) $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

Table 8 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
IGate to source charge	Q_{gs}	-	1.5	-	nC	$V_{DD}=480\text{ V}$, $I_D=1.9\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	Q_{gd}	-	6.5	-		
Gate charge total	Q_g	-	13	-		
Gate plateau voltage	$V_{plateau}$	-	5.4	-	V	

Table 9 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	$V_{GS}=0\text{ V}$, $I_F=1.9\text{ A}$, $T_j=25\text{ °C}$
Reverse recovery time	t_{rr}	-	220	-	ns	$V_R=400\text{ V}$, $I_F=1.9\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$ (see table 22)
Reverse recovery charge	Q_{rr}	-	1.5	-	μC	
Peak reverse recovery current	I_{rrm}	-	12	-	A	

5 Electrical characteristics diagrams

Table 10

Power dissipation TO-220, TO-252, TO-263	Power dissipation TO-220 FullPAK
$P_{tot} = f(T_c)$	$P_{tot} = f(T_c)$

Table 11

Max. transient thermal impedance TO-220, TO-252, TO-263	Max. transient thermal impedance TO-220 FullPAK
$Z_{(thJC)} = f(t_p)$; parameter: $D = t_p/T$	$Z_{(thJC)} = f(t_p)$; parameter: $D = t_p/T$

Electrical characteristics diagrams

Table 12

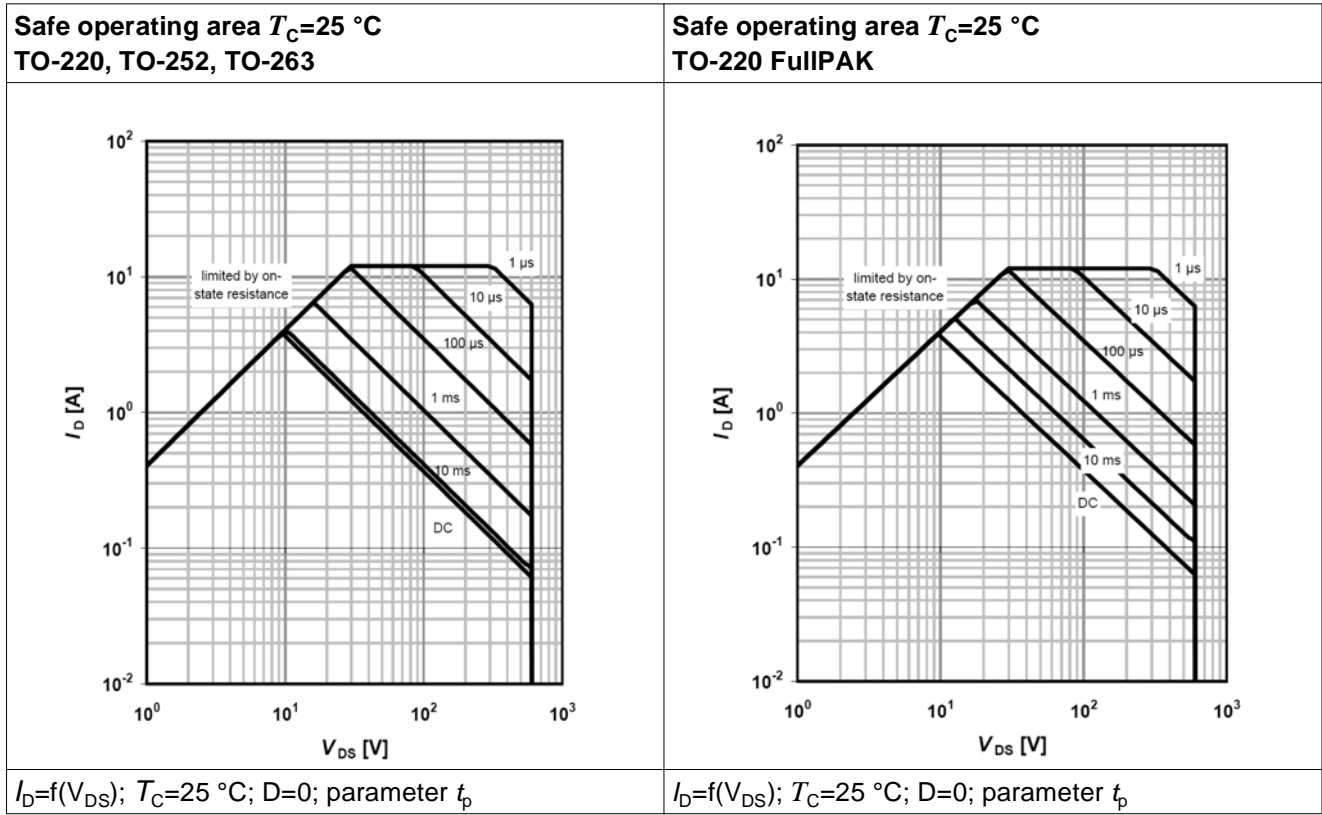


Table 13

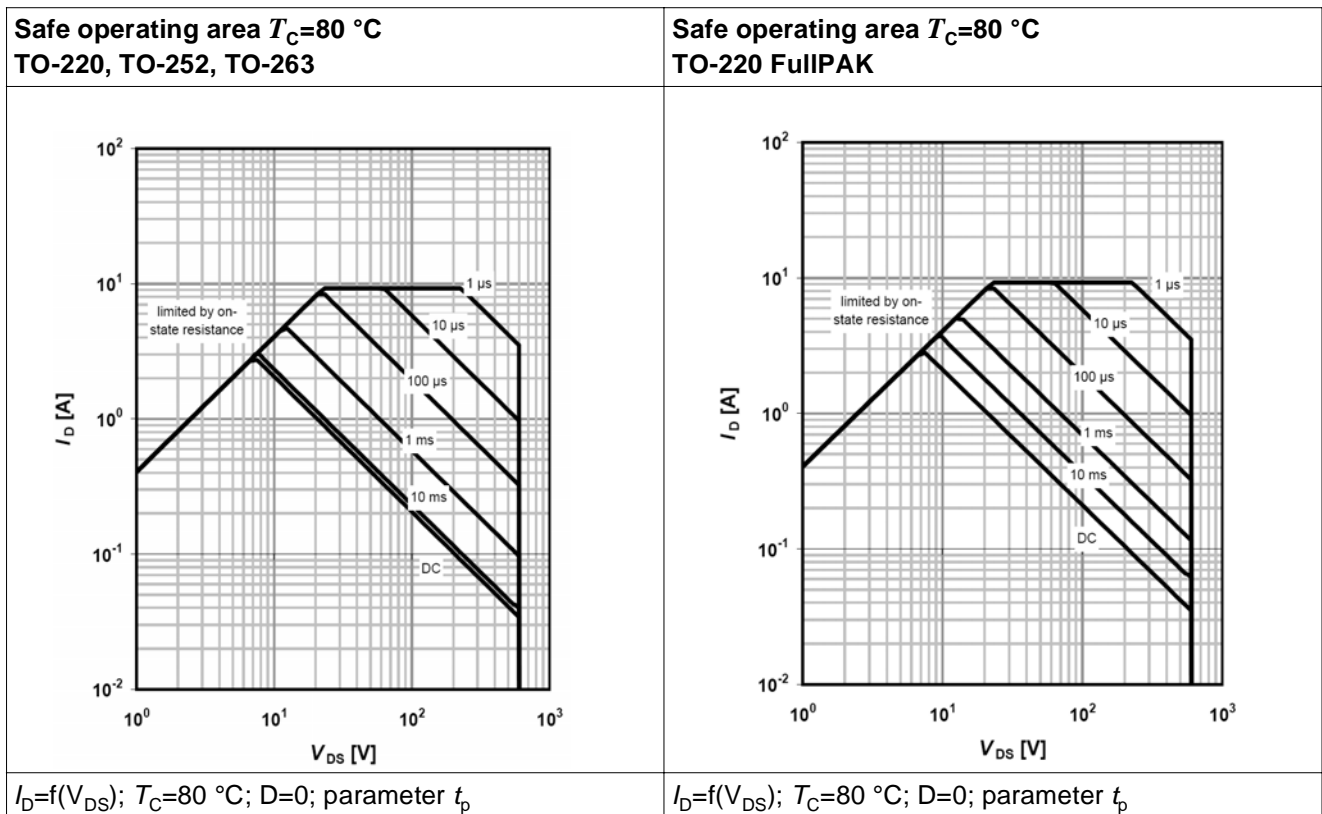


Table 14

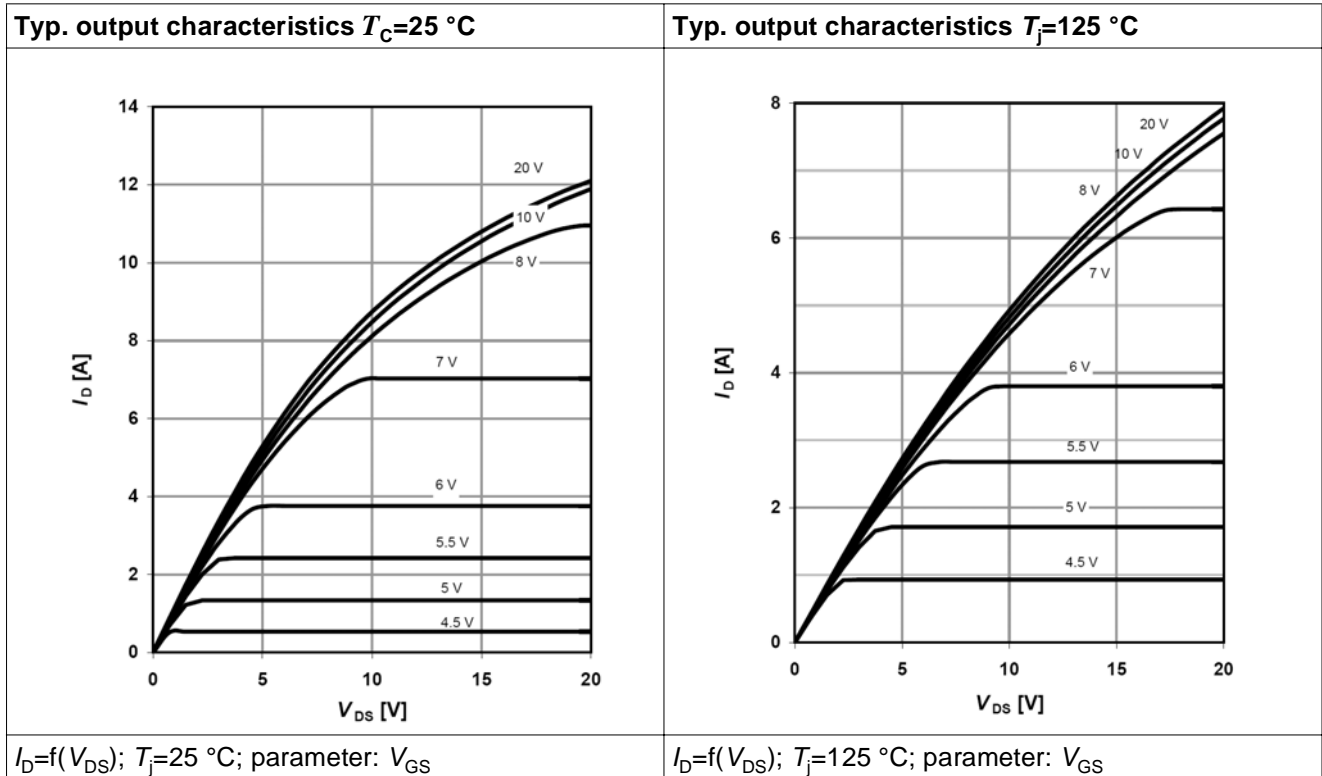


Table 15

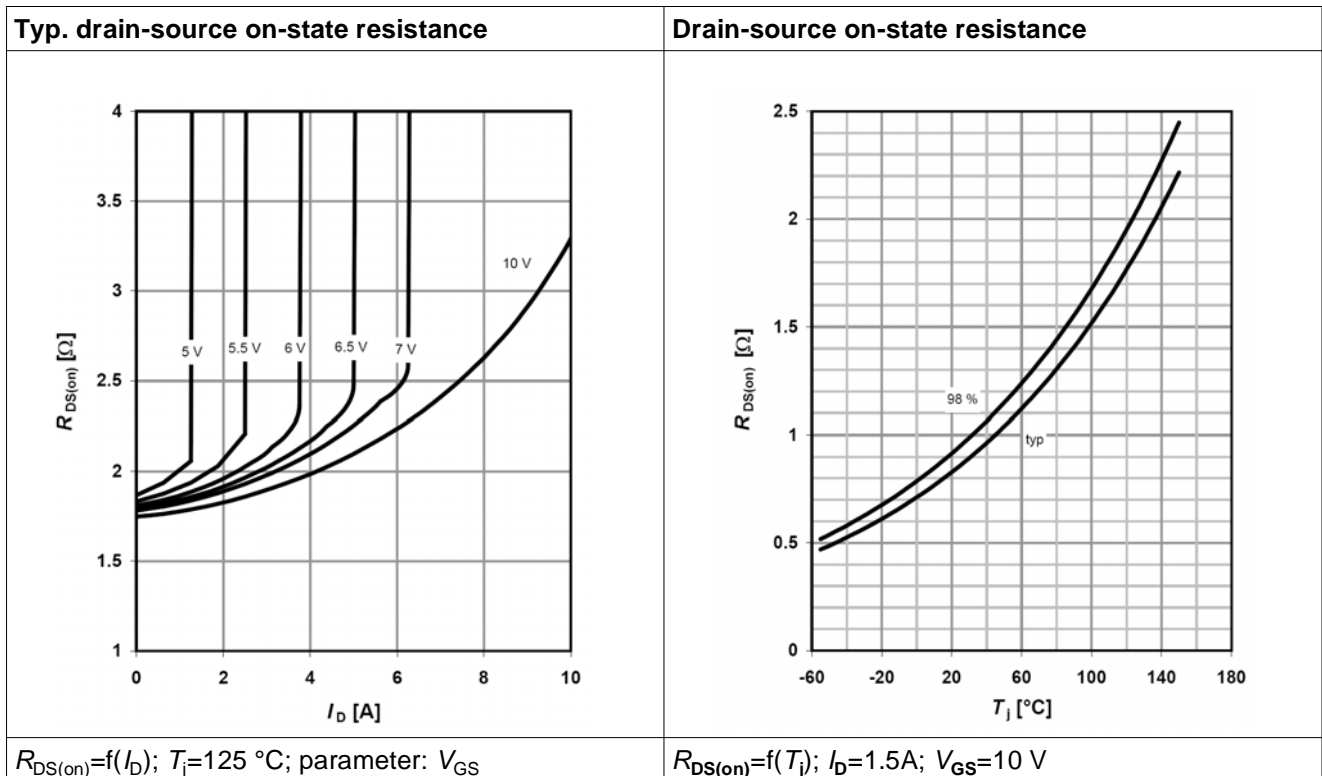


Table 16

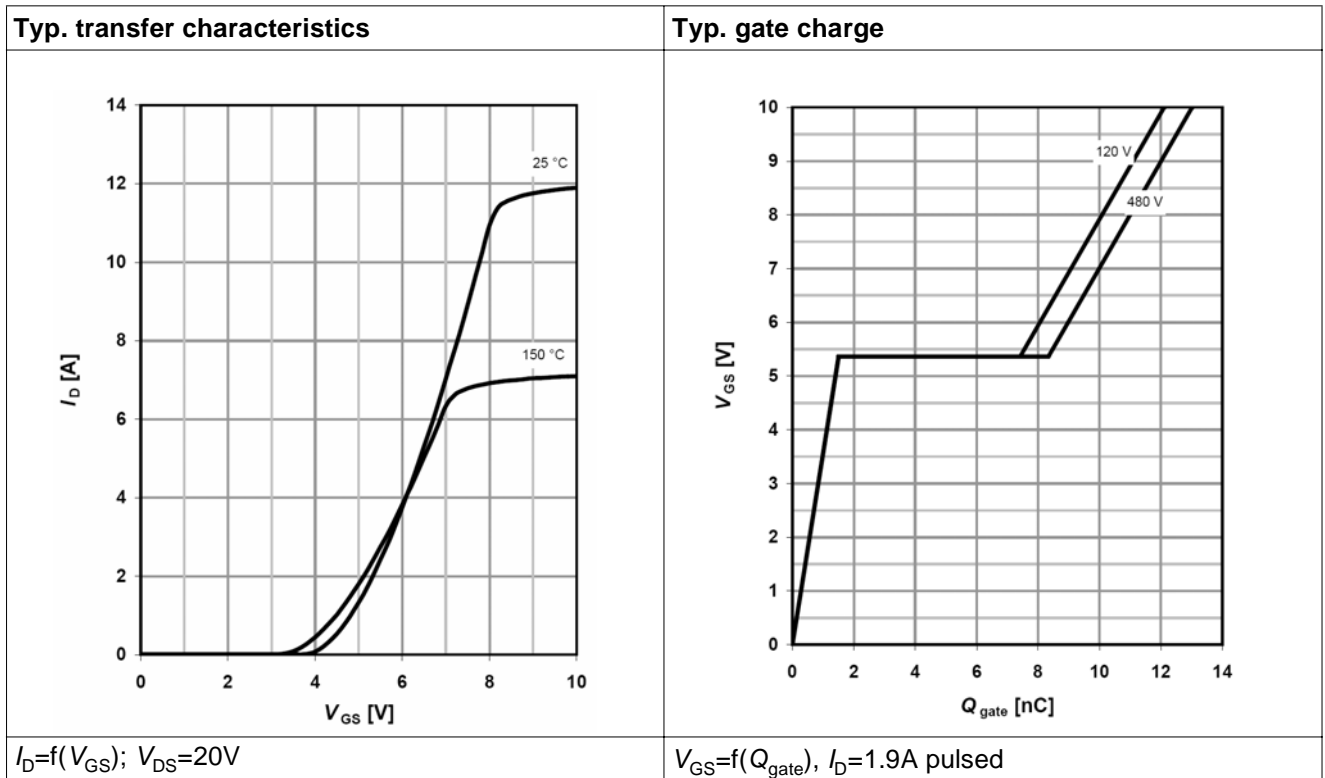


Table 17

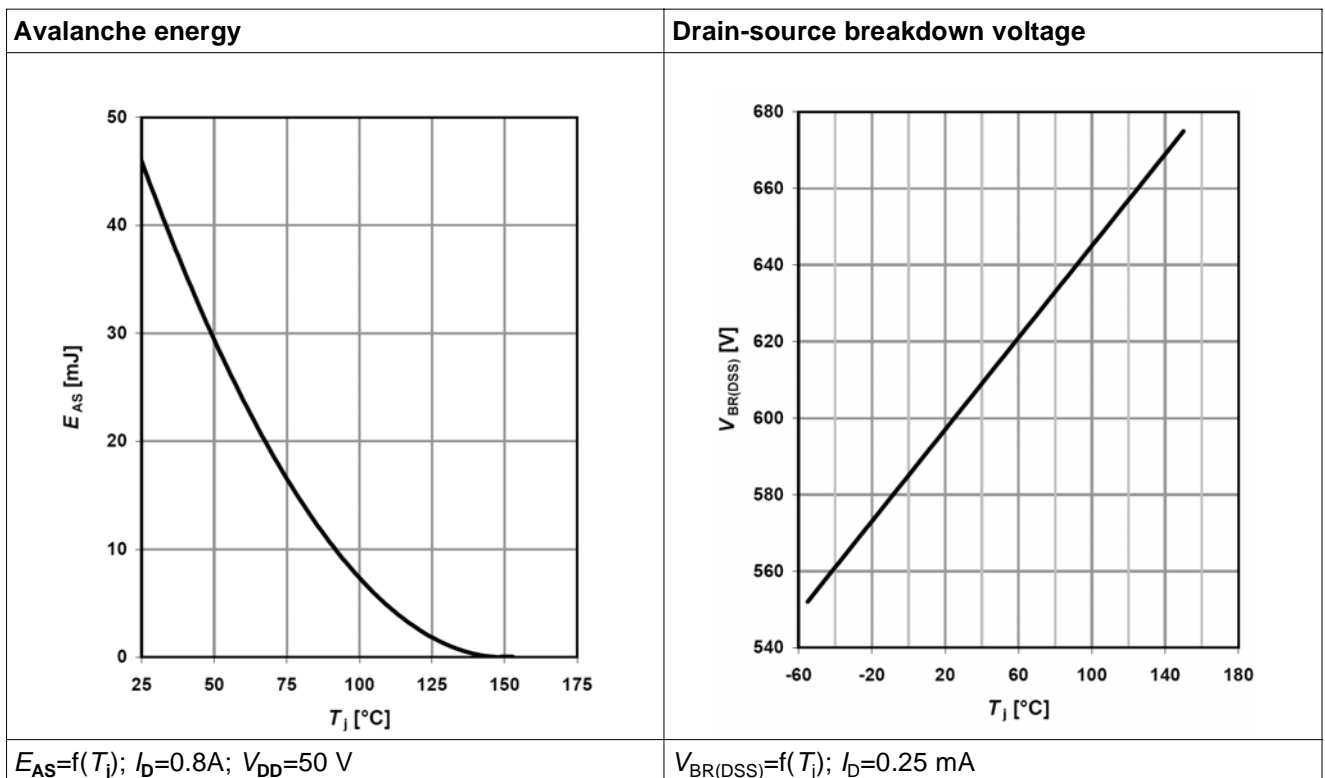


Table 18

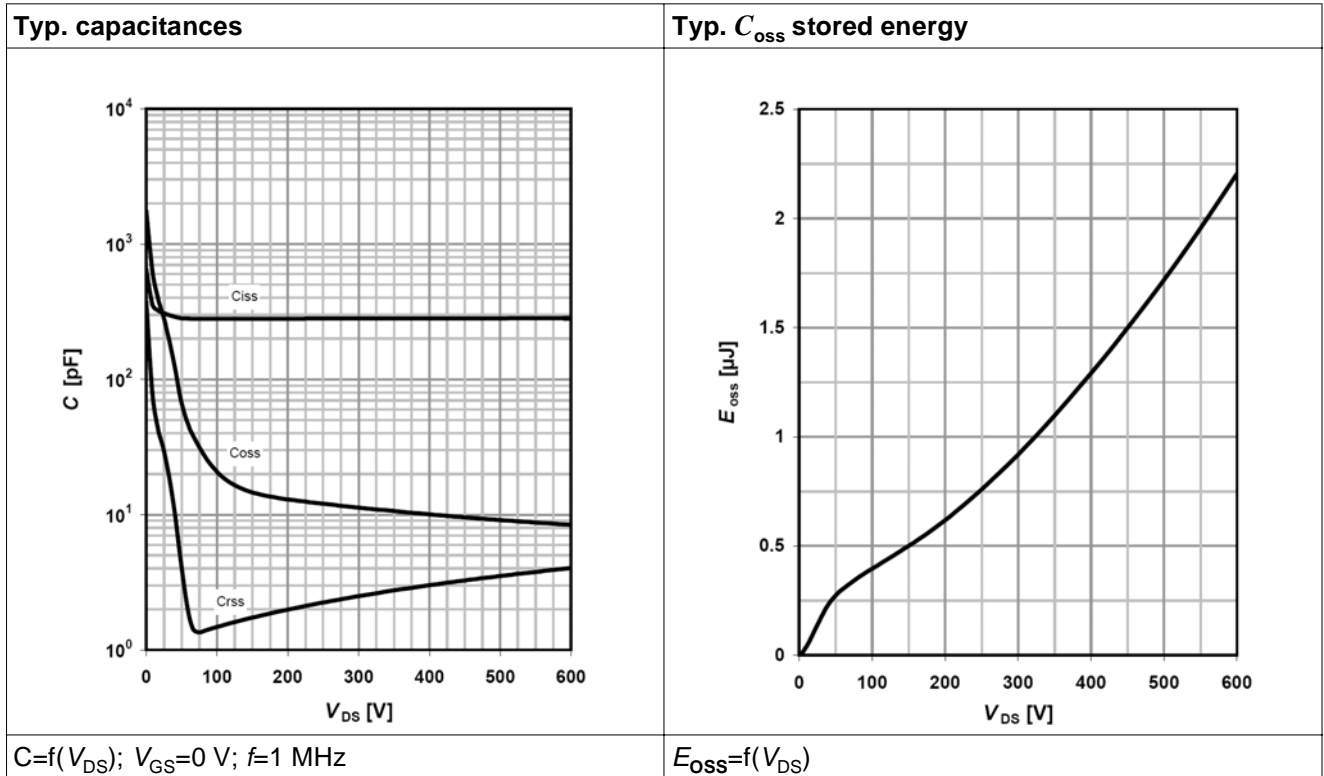
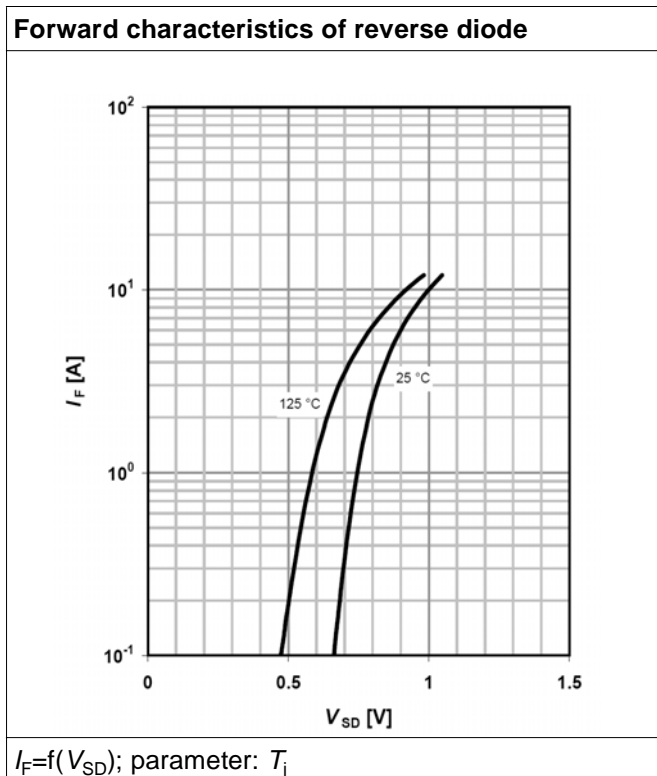


Table 19



6 Test circuits

Table 20 Switching times test circuit and waveform for inductive load

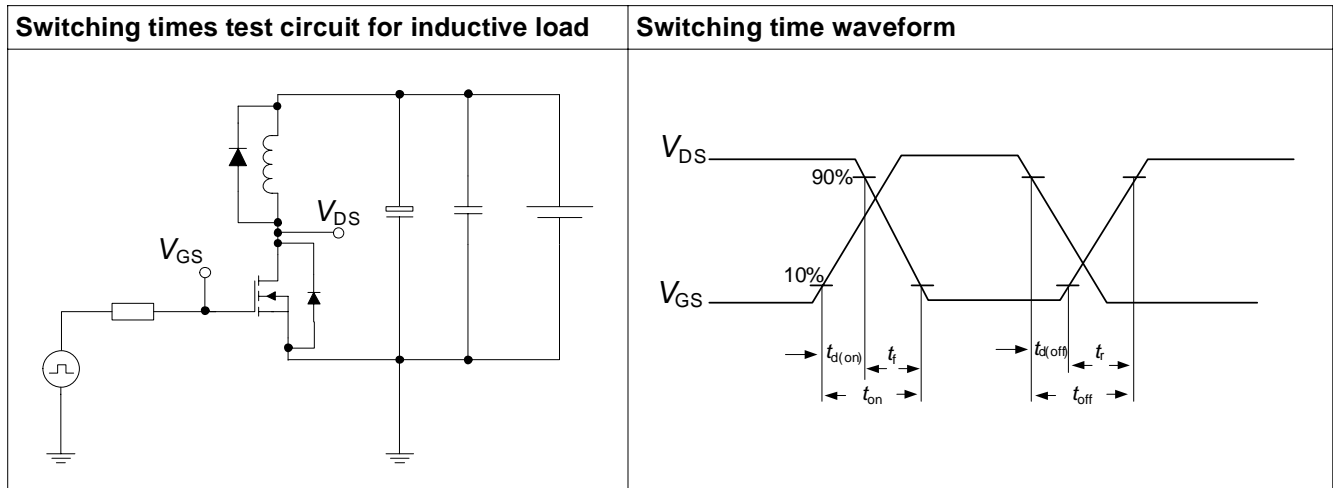


Table 21 Unclamped inductive load test circuit and waveform

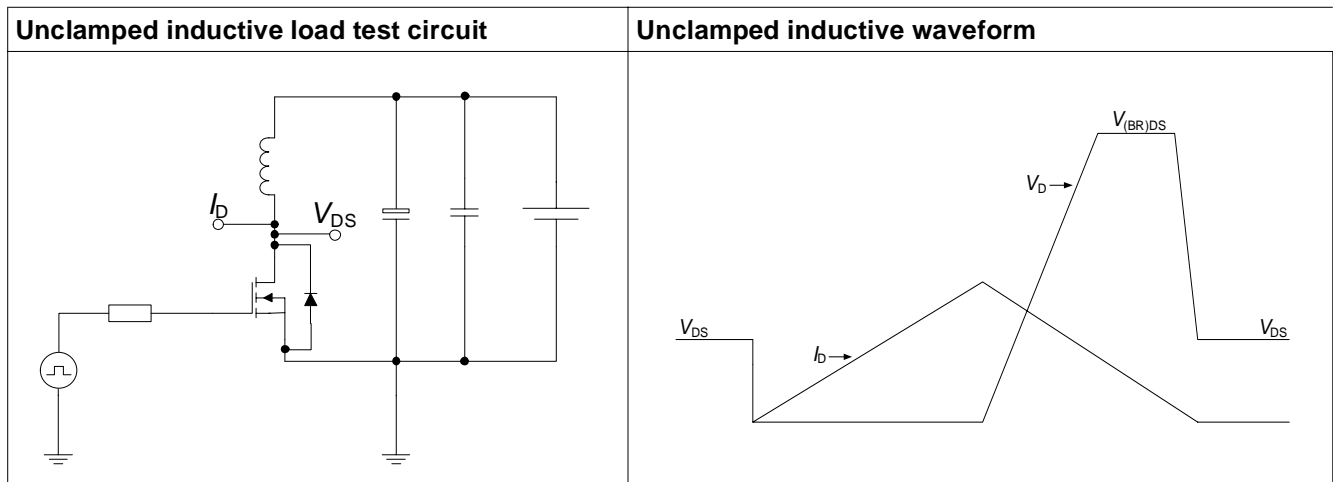
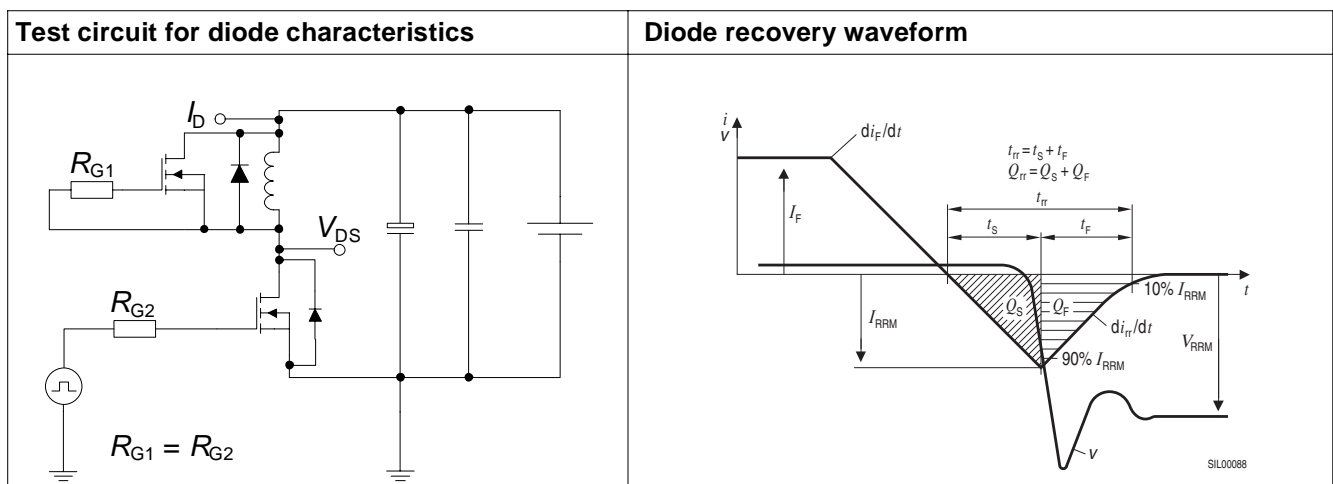
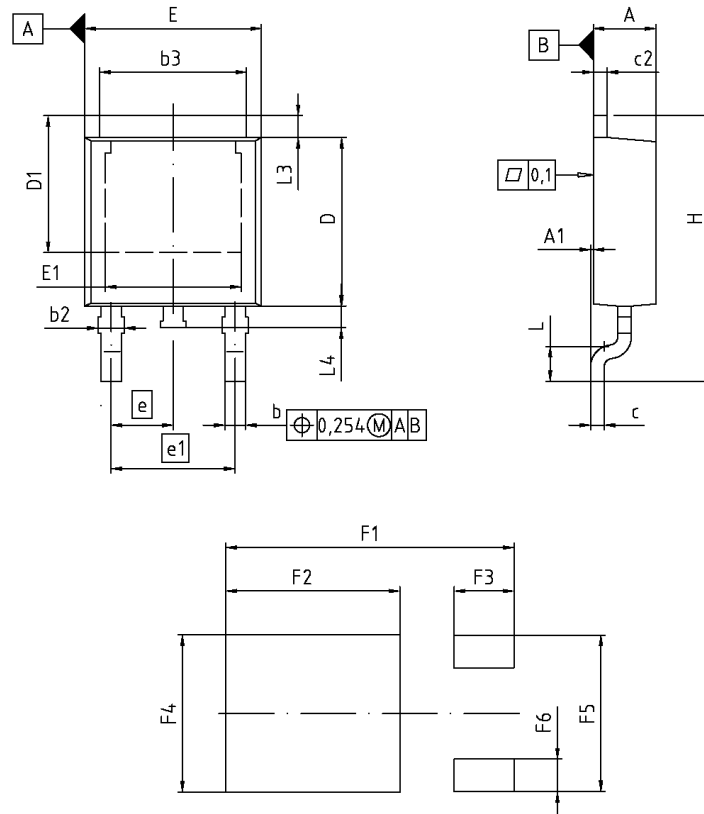


Table 22 Test circuit and waveform for diode characteristics



7 Package outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.16	2.41	0.085	0.095
A1	0.00	0.15	0.000	0.006
b	0.64	0.89	0.025	0.035
b2	0.65	1.15	0.026	0.045
b3	5.00	5.50	0.197	0.217
c	0.46	0.60	0.018	0.024
c2	0.46	0.98	0.018	0.039
D	5.97	6.22	0.235	0.245
D1	5.02	5.84	0.198	0.230
E	6.40	6.73	0.252	0.265
E1	4.70	5.21	0.185	0.205
e	2.29		0.090	
e1	4.57		0.180	
N	3		3	
H	9.40	10.48	0.370	0.413
L	1.18	1.70	0.046	0.067
L3	0.90	1.25	0.035	0.049
L4	0.51	1.00	0.020	0.039
F1	10.50	10.70	0.413	0.421
F2	6.30	6.50	0.248	0.256
F3	2.10	2.30	0.083	0.091
F4	5.70	5.90	0.224	0.232
F5	5.66	5.86	0.223	0.231
F6	1.10	1.30	0.043	0.051

DOCUMENT NO.
Z8B00003328

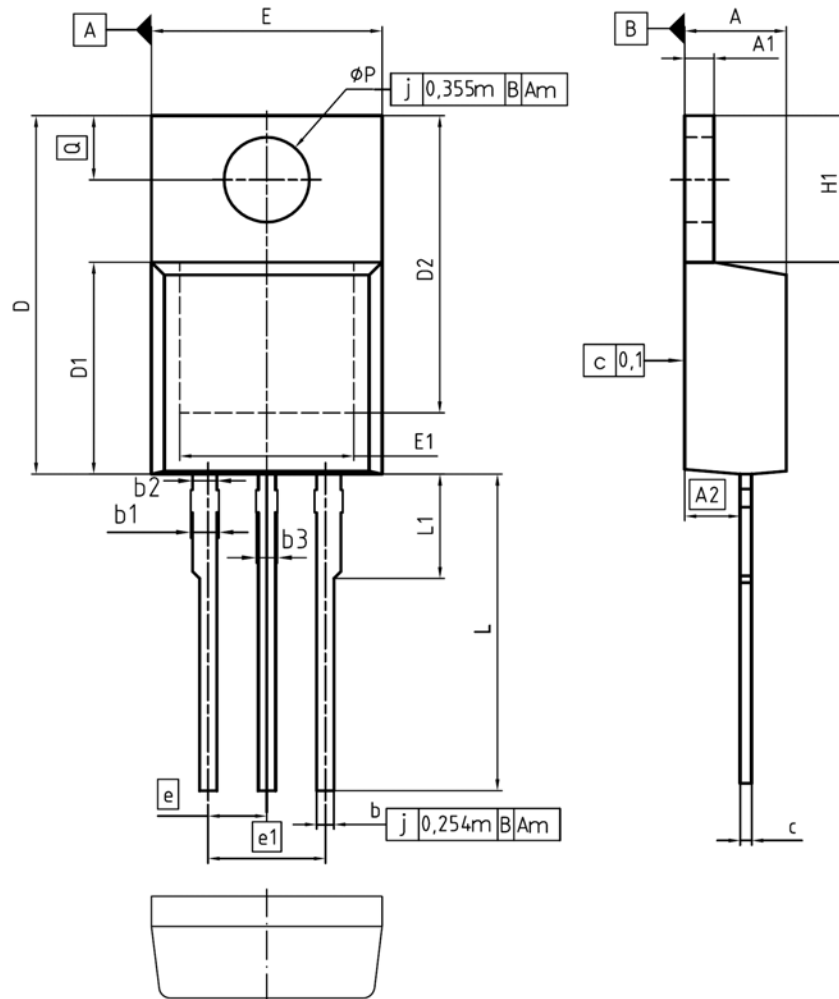
SCALE

EUROPEAN PROJECTION

ISSUE DATE
19-10-2007

REVISION
03

Figure 1 Outlines TO-252, dimensions in mm/inches



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	1.17	1.40	0.046	0.055
A2	2.15	2.72	0.085	0.107
b	0.65	0.86	0.026	0.034
b1	0.95	1.40	0.037	0.055
b2	0.95	1.15	0.037	0.045
b3	0.65	1.15	0.026	0.045
c	0.33	0.60	0.013	0.024
D	14.81	15.95	0.583	0.628
D1	8.51	9.45	0.335	0.372
D2	12.19	13.10	0.480	0.516
E	9.70	10.36	0.382	0.408
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	3		3	
H1	5.90	6.90	0.232	0.272
L	13.00	14.00	0.512	0.551
L1	-	4.80	-	0.189
øP	3.60	3.89	0.142	0.153
Q	2.60	3.00	0.102	0.118

DOCUMENT NO.
Z8B00003318

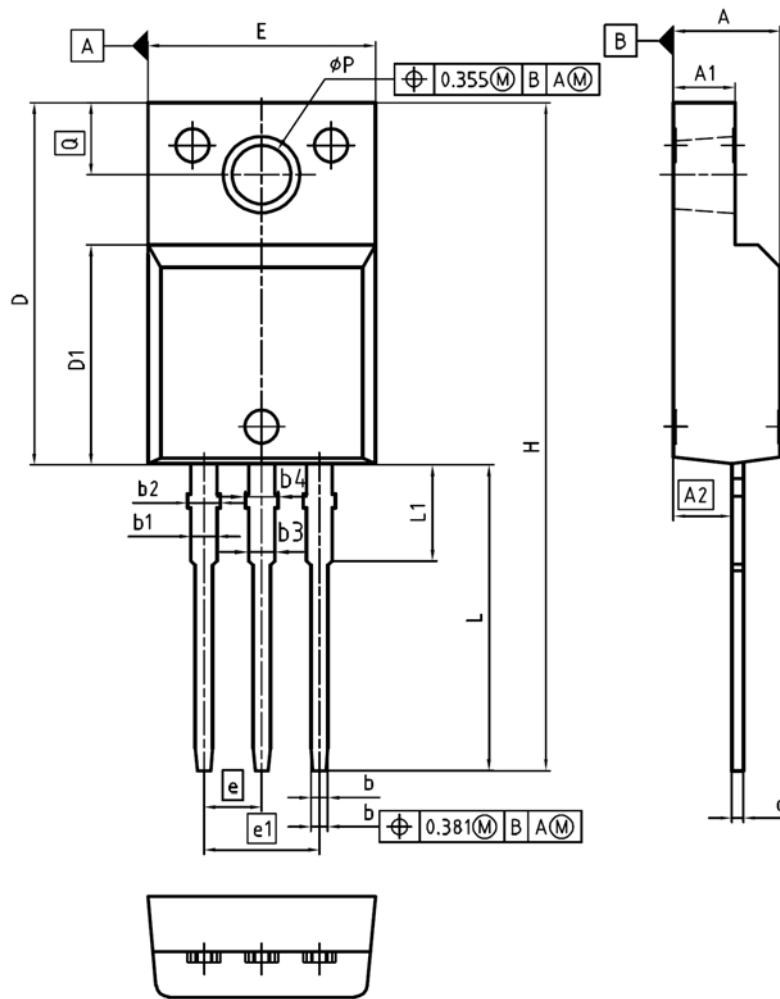
SCALE

EUROPEAN PROJECTION

ISSUE DATE
23-08-2007

REVISION
05

Figure 2 Outlines TO-220, dimensions in mm/inches



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.55	4.85	0.179	0.191
A1	2.55	2.85	0.100	0.112
A2	2.42	2.72	0.095	0.107
b	0.65	0.85	0.026	0.033
b1	0.95	1.33	0.037	0.052
b2	0.95	1.51	0.037	0.059
b3	0.65	1.33	0.026	0.052
b4	0.65	1.51	0.026	0.059
c	0.40	0.63	0.016	0.025
D	15.85	16.15	0.624	0.636
D1	9.53	9.83	0.375	0.387
E	10.35	10.65	0.407	0.419
e	2.54		0.100	
e1	5.08		0.200	
N	3		3	
H	29.45	29.75	1.159	1.171
L	13.45	13.75	0.530	0.541
L1	3.15	3.45	0.124	0.136
øP	2.95	3.20	0.116	0.126
Q	3.15	3.50	0.124	0.138

DOCUMENT NO.
Z8B00003319

SCALE

EUROPEAN PROJECTION

ISSUE DATE
08-03-2007

REVISION
03

Figure 3 Outlines TO-220 FullIPAK, dimensions in mm/inches

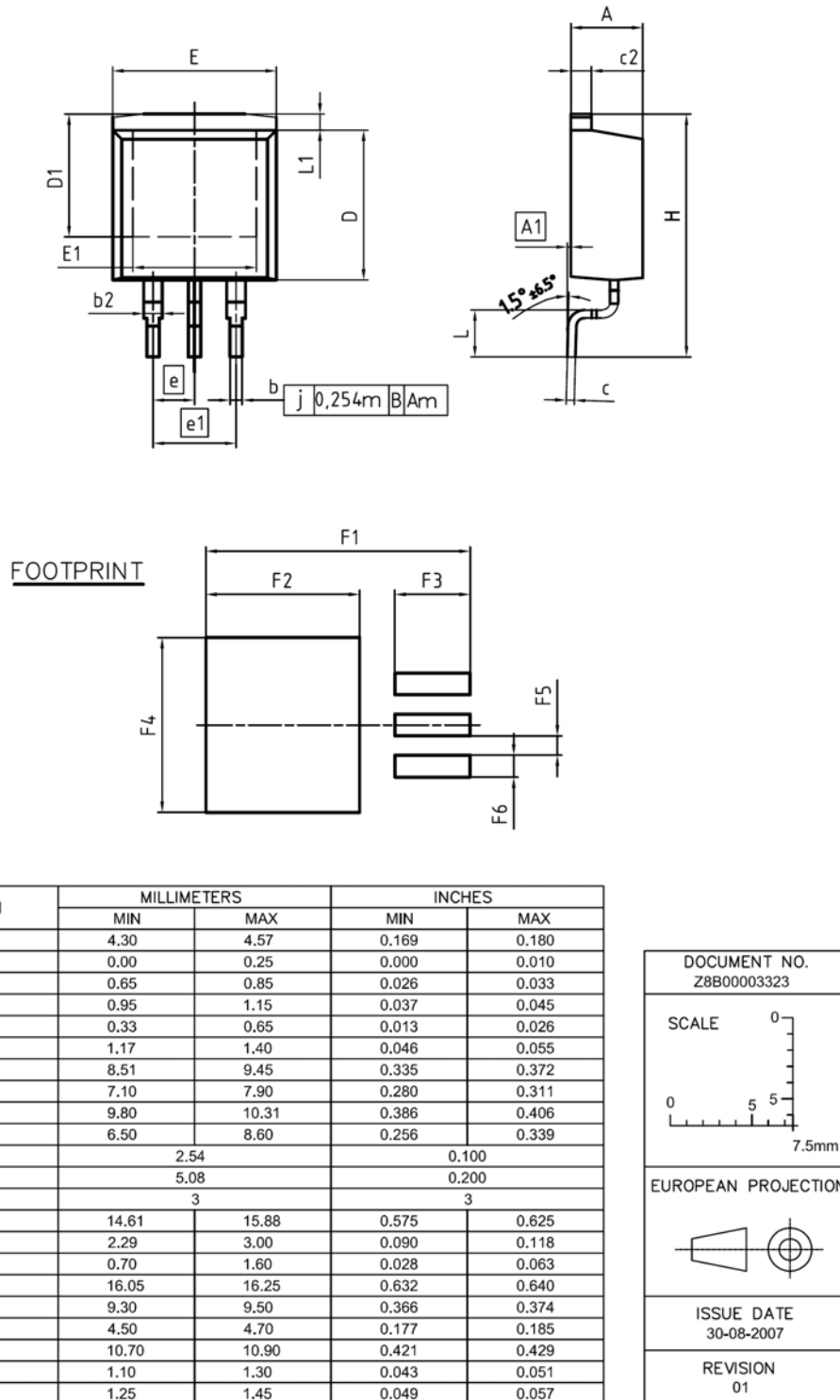


Figure 4 Outlines TO-263, dimensions in mm/inches

8 Revision History

CoolMOS C6 600V CoolMOS™ C6 Power Transistor

Revision History: 2009-08-28, Rev. 2.0

Previous Revision:

Revision	Subjects (major changes since last revision)
2.0	Release of final data sheet

We Listen to Your Comments

Any information within this document that you feel is wrong, unclear or missing at all?
Your feedback will help us to continuously improve the quality of this document.

Please send your proposal (including a reference to this document) to: erratum@infineon.com



Edition 2009-08-28

Published by

Infineon Technologies AG

81726 Munich, Germany

© 2009 Infineon Technologies AG

All Rights Reserved.

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.