International
IOR Rectifier

PD - 95545

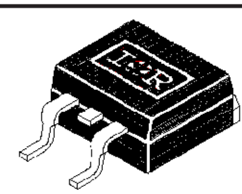
IRFBC40ASPbF

HEXFET® Power MOSFET

Applications

- Switch Mode Power Supply (SMPS)
- Uninterruptable Power Supply
- High speed power switching
- Lead-Free

V_{DSS}	Rds(on) max	I_D
600V	**1.2Ω**	**6.2A**



D^2Pak

Benefits

- Low Gate Charge Qg results in Simple Drive Requirement
- Improved Gate, Avalanche and dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective Coss Specified (See AN 1001)

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V⑥	6.2	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V⑥	3.9	
I_{DM}	Pulsed Drain Current ①⑥	25	
P_D @T_C = 25°C	Power Dissipation	125	W
	Linear Derating Factor	1.0	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③⑥	6.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Typical SMPS Topology:

- Single transistor Forward

Notes ① through ⑤ are on page 9

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	600	–––	–––	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	–––	0.66	–––	V/°C	Reference to 25°C, I_D = 1mA⑥
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	–––	–––	1.2	Ω	V_{GS} = 10V, I_D = 3.7A ①
$V_{GS(th)}$	Gate Threshold Voltage	2.0	–––	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{DSS}	Drain-to-Source Leakage Current	–––	–––	25	μA	V_{DS} = 600V, V_{GS} = 0V
		–––	–––	250		V_{DS} = 480V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	–––	–––	100	nA	V_{GS} = 30V
	Gate-to-Source Reverse Leakage	–––	–––	-100		V_{GS} = -30V

Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	3.4	–––	–––	S	V_{DS} = 50V, I_D = 3.7A
Q_g	Total Gate Charge	–––	–––	42	nC	I_D = 6.2A
Q_{gs}	Gate-to-Source Charge	–––	–––	10		V_{DS} = 480V
Q_{gd}	Gate-to-Drain ("Miller") Charge	–––	–––	20		V_{GS} = 10V, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	–––	13	–––	ns	V_{DD} = 300V
t_r	Rise Time	–––	23	–––		I_D = 6.2A
$t_{d(off)}$	Turn-Off Delay Time	–––	31	–––		R_G = 9.1Ω
t_f	Fall Time	–––	18	–––		R_D = 47Ω,See Fig. 10 ④
C_{iss}	Input Capacitance	–––	1036	–––	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	–––	136	–––		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	–––	7.0	–––		ƒ = 1.0MHz, See Fig. 5
C_{oss}	Output Capacitance	–––	1487	–––		V_{GS} = 0V, V_{DS} = 1.0V, ƒ = 1.0MHz
C_{oss}	Output Capacitance	–––	36	–––		V_{GS} = 0V, V_{DS} = 480V, ƒ = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	–––	48	–––		V_{GS} = 0V, V_{DS} = 0V to 480V ⑤

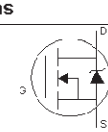
Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	–––	570	mJ
I_{AR}	Avalanche Current①	–––	6.2	A
E_{AR}	Repetitive Avalanche Energy①	–––	13	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	–––	1.0	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted, steady-state)*	–––	40	

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	–––	–––	6.2	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	–––	–––	25		
V_{SD}	Diode Forward Voltage	–––	–––	1.5	V	T_J = 25°C, I_S = 6.2A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	–––	431	647	ns	T_J = 25°C, I_F = 6.2A
Q_{rr}	Reverse RecoveryCharge	–––	1.8	2.8	μC	di/dt = 100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

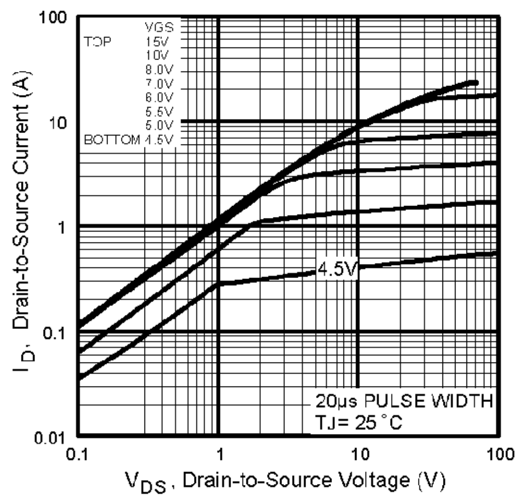


Fig 1. Typical Output Characteristics,

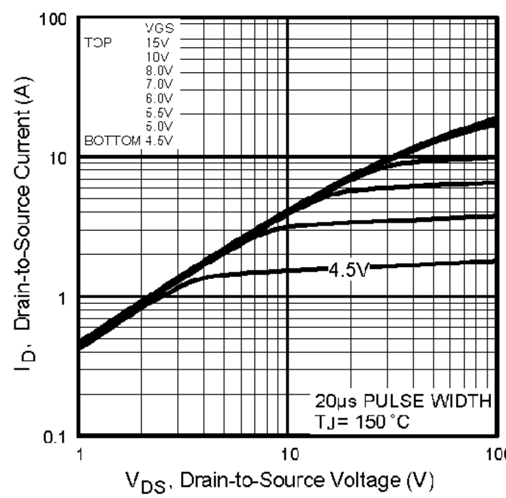


Fig 2. Typical Output Characteristics,

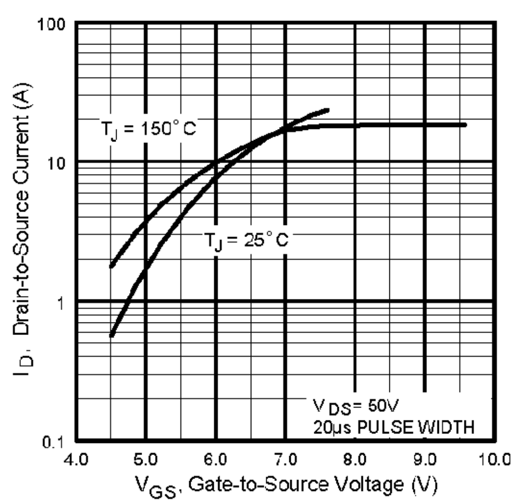


Fig 3. Typical Transfer Characteristics

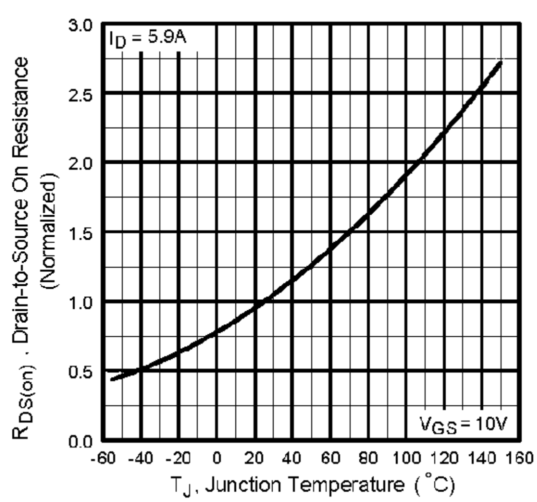


Fig 4. Normalized On-Resistance Vs. Temperature

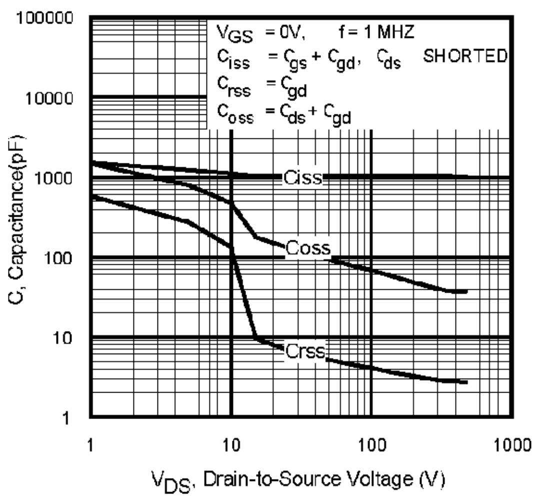


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

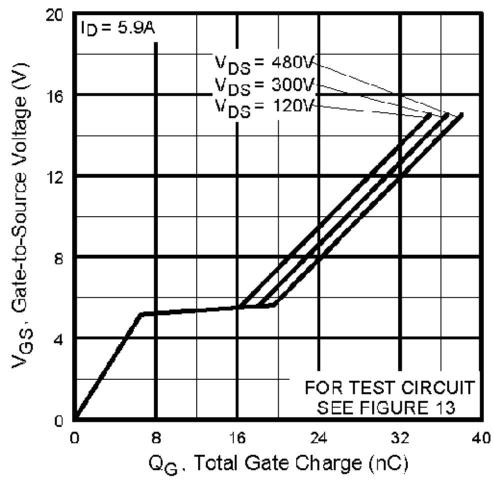


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

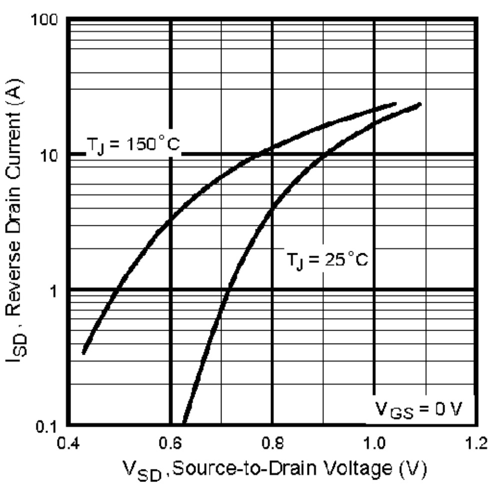


Fig 7. Typical Source-Drain Diode Forward Voltage

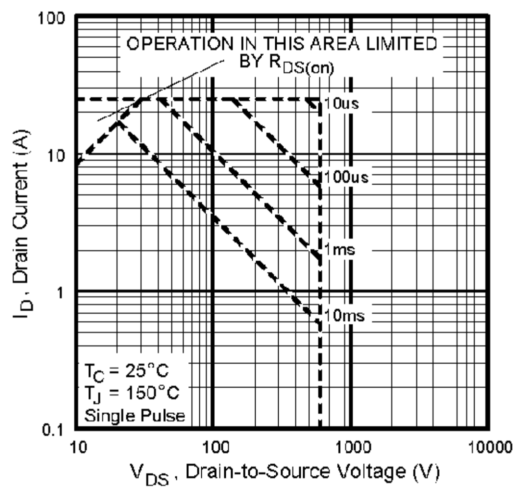


Fig 8. Maximum Safe Operating Area

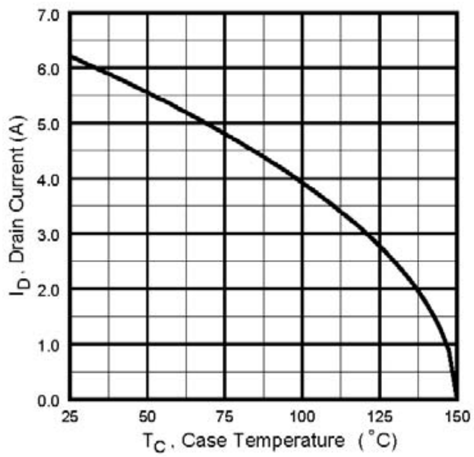


Fig 9. Maximum Drain Current Vs. Case Temperature

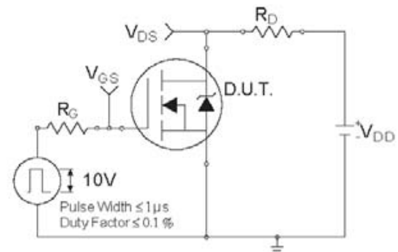


Fig 10a. Switching Time Test Circuit

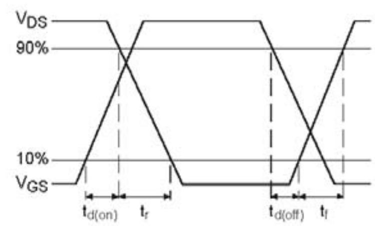


Fig 10b. Switching Time Waveforms

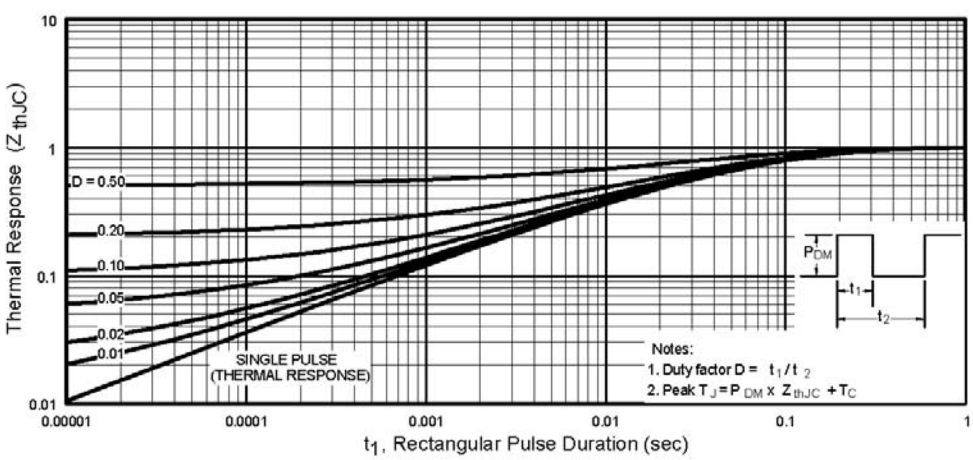


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

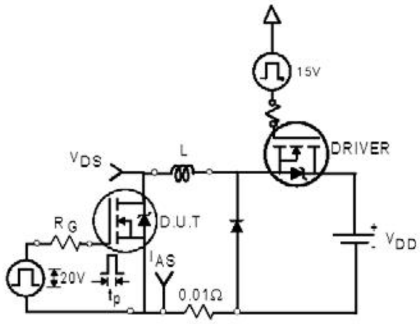


Fig 12a. Unclamped Inductive Test Circuit

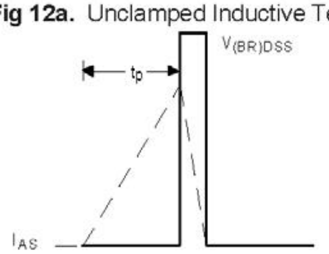


Fig 12b. Unclamped Inductive Waveforms

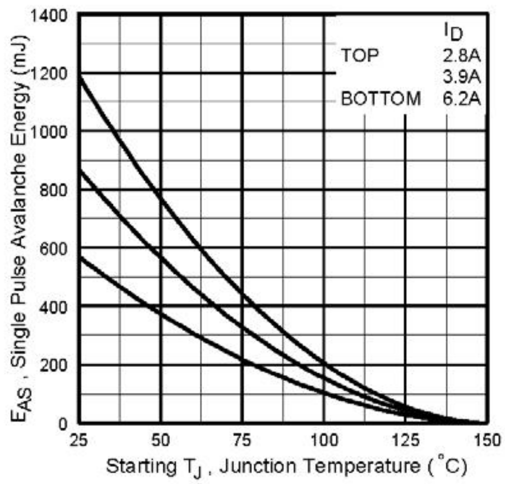


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

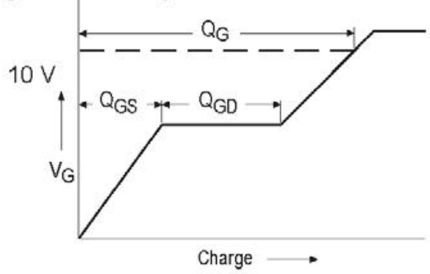


Fig 13a. Basic Gate Charge Waveform

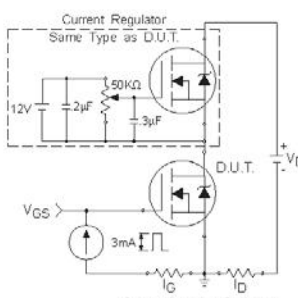


Fig 13b. Gate Charge Test Circuit

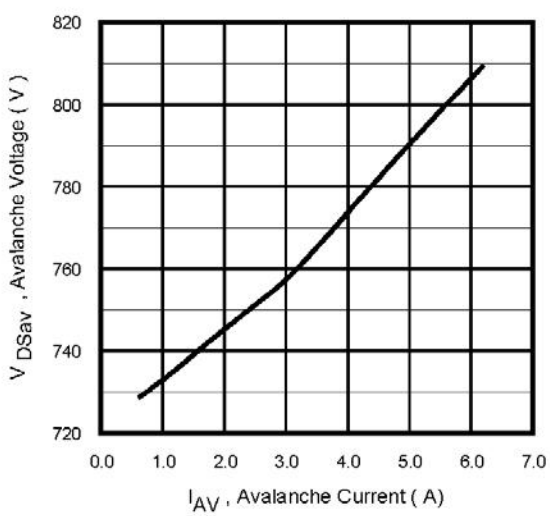


Fig 12d. Typical Drain-to-Source Voltage Vs. Avalanche Current

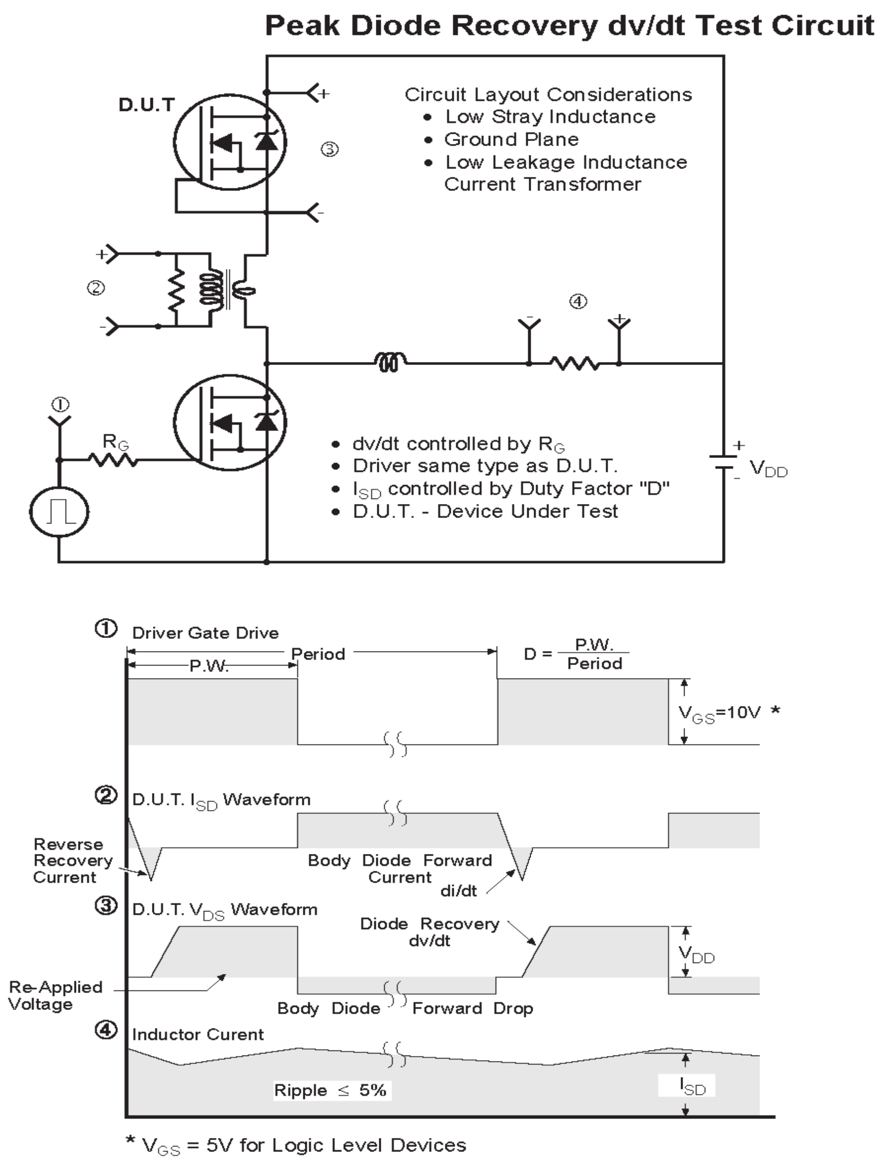
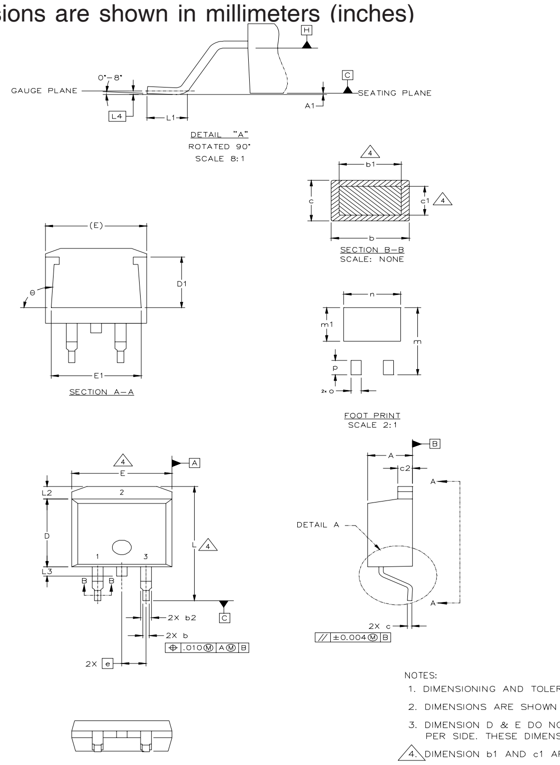


Fig 14. For N-Channel HEXFETS

D2Pak Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1		0.127		.005	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	4
b2	1.14	1.40	.045	.055	
c	0.43	0.63	.017	.025	
c1	0.38	0.74	.015	.029	4
c2	1.14	1.40	.045	.055	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	14.61	15.88	.575	.625	
L1	1.78	2.79	.070	.110	
L2		1.65		.065	
L3	1.27	1.78	.050	.070	
L4	0.25 BSC		.010 BSC		
m	17.78		.700		
m1	8.89		.350		
n	11.43		.450		
o	2.08		.082		
p	3.81		.150		
θ	90°	93°	90°	93°	

LEAD ASSIGNMENTS

HEXFET	IGBTs, CoPACK	DIODES
1.– GATE	1.– GATE	1.– ANODE *
2.– DRAIN	2.– COLLECTOR	2.– CATHODE
3.– SOURCE	3.– EMITTER	3.– ANODE

* PART DEPENDENT.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

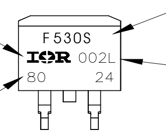
D2Pak Part Marking Information (Lead-Free)

EXAMPLE: THIS IS AN IRF530S WITH LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line position indicates "Lead-Free"

INTERNATIONAL RECTIFIER LOGO

ASSEMBLY LOT CODE



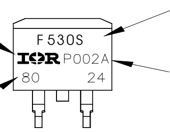
PART NUMBER

DATE CODE
YEAR 0 = 2000
WEEK 02
LINE L

OR

INTERNATIONAL RECTIFIER LOGO

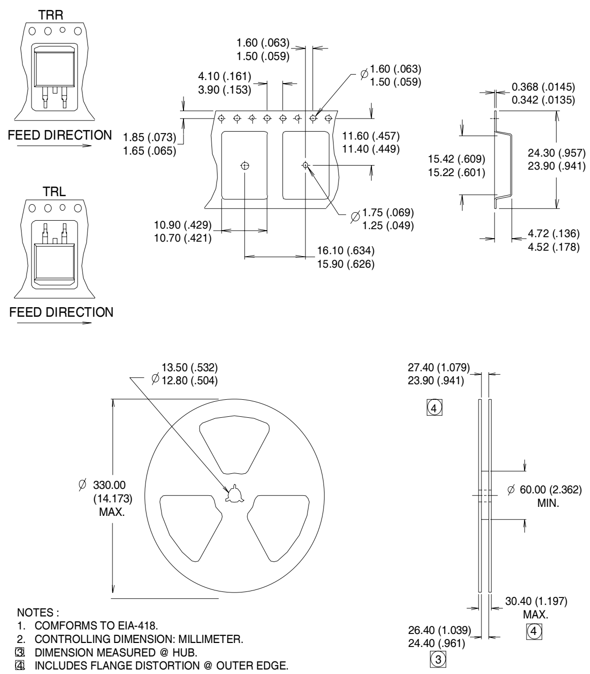
ASSEMBLY LOT CODE



PART NUMBER

DATE CODE
P = DESIGNATES LEAD-FREE PRODUCT (OPTIONAL)
YEAR 0 = 2000
WEEK 02
A = ASSEMBLY SITE CODE

D^2Pak Tape & Reel Infomation



Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting $T_J = 25°C$, $L = 29.6mH$ $R_G = 25\Omega$, $I_{AS} = 6.2A$. (See Figure 12)

③ $I_{SD} \leq 6.2A$, $di/dt \leq 88A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150°C$

④ Pulse width $\leq$ 300µs; duty cycle $\leq$ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

⑥ Uses IRFBC40A data and test conditions

* When mounted on FR-4 board using minimum recommended footprint.
For recommended footprint and soldering techniques refer to application note #AN-994.

Data and specifications subject to change without notice.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903

07/04

Notice

The products described herein were acquired by Vishay Intertechnology, Inc., as part of its acquisition of International Rectifier's Power Control Systems (PCS) business, which closed in April 2007. Specifications of the products displayed herein are pending review by Vishay and are subject to the terms and conditions shown below.

Specifications of the products displayed herein are subject to change without notice. Vishay Intertechnology, Inc., or anyone on its behalf, assumes no responsibility or liability for any errors or inaccuracies.

Information contained herein is intended to provide a product description only. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Vishay's terms and conditions of sale for such products, Vishay assumes no liability whatsoever, and disclaims any express or implied warranty, relating to sale and/or use of Vishay products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright, or other intellectual property right.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications. Customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Vishay for any damages resulting from such improper use or sale.

International Rectifier®, IR®, the IR logo, HEXFET®, HEXSense®, HEXDIP®, DOL®, INTERO®, and POWIRTRAIN® are registered trademarks of International Rectifier Corporation in the U.S. and other countries. All other product names noted herein may be trademarks of their respective owners.