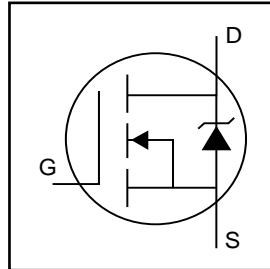


# IRFBC40S/L

HEXFET® Power MOSFET

- Surface Mount (IRFBC40S)
- Low-profile through-hole (IRFBC40L)
- Available in Tape & Reel (IRFBC40S)
- Dynamic dv/dt Rating
- 150°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated



$$V_{DS} = 600V$$

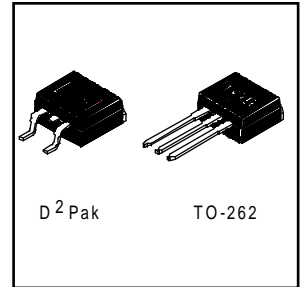
$$R_{DS(on)} = 1.2\Omega$$

$$I_D = 6.2A$$

## Description

Third generation HEXFETs from international Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D<sup>2</sup>Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D<sup>2</sup>Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application. The through-hole version (IRFBC40L) is available for low-profile applications.



## Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D$ @ $T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ⑤	6.2	A
$I_D$ @ $T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ⑤	3.9	
$I_{DM}$	Pulsed Drain Current ①⑤	25	
$P_D$ @ $T_A = 25^\circ C$	Power Dissipation	3.1	W
$P_D$ @ $T_C = 25^\circ C$	Power Dissipation	130	W
	Linear Derating Factor	1.0	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 20	V
$E_{AS}$	Single Pulse Avalanche Energy ②⑤	570	mJ
$I_{AR}$	Avalanche Current ①	6.2	A
$E_{AR}$	Repetitive Avalanche Energy ①	13	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑤	3.0	V/ns
$T_J$	Operating Junction and	-55 to + 150	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	

## Thermal Resistance

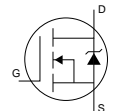
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.0	°C/W
$R_{\theta JA}$	Junction-to-Ambient ( PCB Mounted, steady-state)**	—	40	

## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	600	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.70	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1mA$ ⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	1.2	$\Omega$	$V_{GS} = 10V, I_D = 3.7A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$g_{fs}$	Forward Transconductance	4.7	—	—	S	$V_{DS} = 100V, I_D = 3.7A$ ⑤
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	100	$\mu A$	$V_{DS} = 600V, V_{GS} = 0V$
		—	—	500		$V_{DS} = 480V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
$Q_g$	Total Gate Charge	—	—	60	nC	$I_D = 6.2A$
$Q_{gs}$	Gate-to-Source Charge	—	—	8.3		$V_{DS} = 3600V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	—	30		$V_{GS} = 10V$ , See Fig. 6 and 13 ④ ⑤
$t_{d(on)}$	Turn-On Delay Time	—	13	—	ns	$V_{DD} = 300V$
$t_r$	Rise Time	—	18	—		$I_D = 6.2A$
$t_{d(off)}$	Turn-Off Delay Time	—	55	—		$R_G = 9.1\Omega$
$t_f$	Fall Time	—	20	—		$R_D = 47\Omega$ , See Fig. 10 ④ ⑤
$L_S$	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
$C_{iss}$	Input Capacitance	—	1300	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	160	—		$V_{DS} = 25V$
$C_{rss}$	Reverse Transfer Capacitance	—	30	—		$f = 1.0MHz$ , See Fig. 5 ⑤

## Source-Drain Ratings and Characteristics

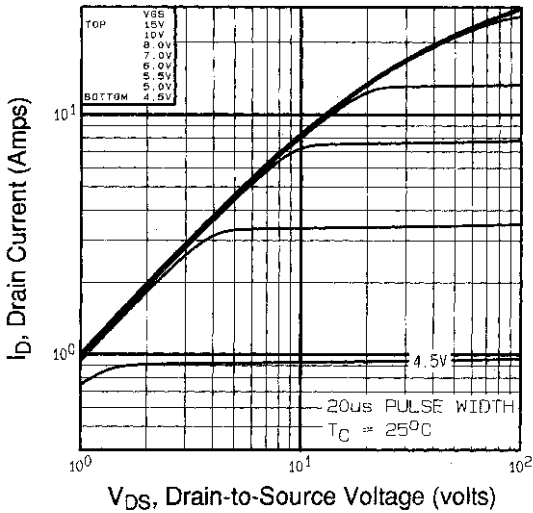
	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	6.2	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	25		
$V_{SD}$	Diode Forward Voltage	—	—	1.5	V	$T_J = 25^\circ\text{C}, I_S = 6.2A, V_{GS} = 0V$ ④
$t_{rr}$	Reverse Recovery Time	—	450	940	ns	$T_J = 25^\circ\text{C}, I_F = 6.2A$
$Q_{rr}$	Reverse Recovery Charge	—	3.8	7.9	$\mu C$	$di/dt = 100A/\mu s$ ④ ⑤
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$ )				



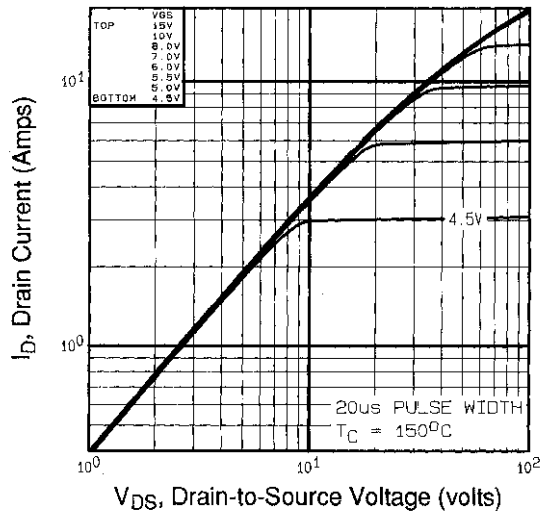
### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )
- ②  $V_{DD} = 50V$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 27mH$   
 $R_G = 25\Omega, I_{AS} = 6.2A$ . (See Figure 11)
- ③  $I_{SD} \leq 6.2A, di/dt \leq 80A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$
- ④ Pulse width  $\leq 300\mu s$ ; duty cycle  $\leq 2\%$ .
- ⑤ Uses IRFBC40 data and test conditions

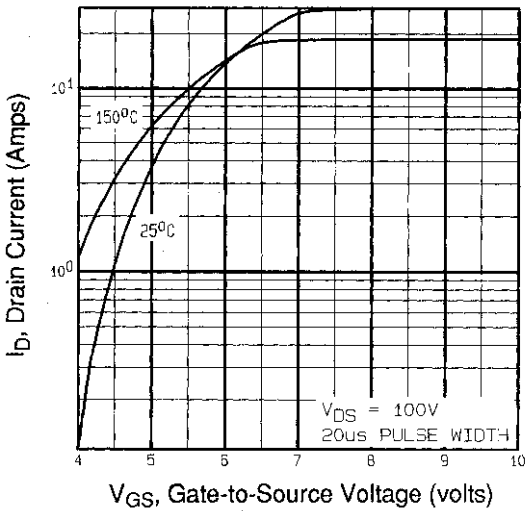
\*\* When mounted on 1" square PCB (FR-4 or G-10 Material ).  
For recommended footprint and soldering techniques refer to application note #AN-994.



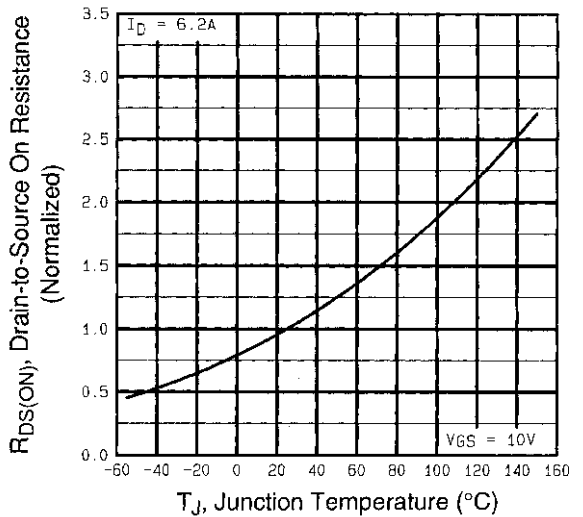
**Fig 1.** Typical Output Characteristics,



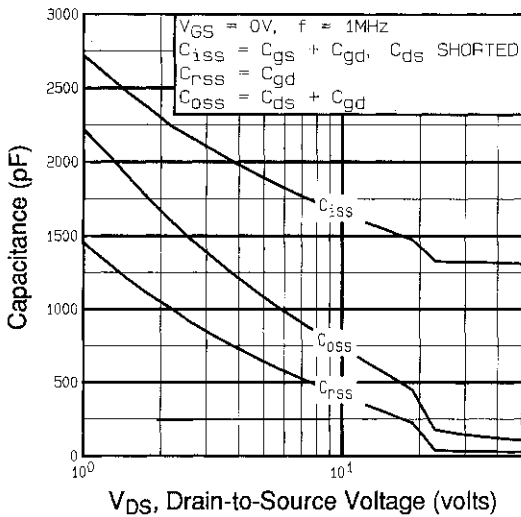
**Fig 2.** Typical Output Characteristics,



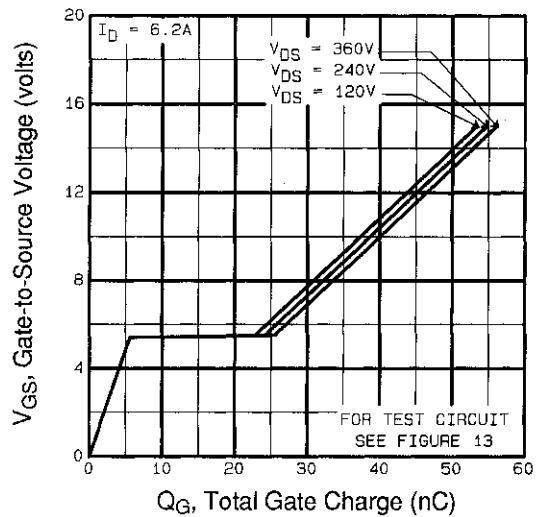
**Fig 3.** Typical Transfer Characteristics



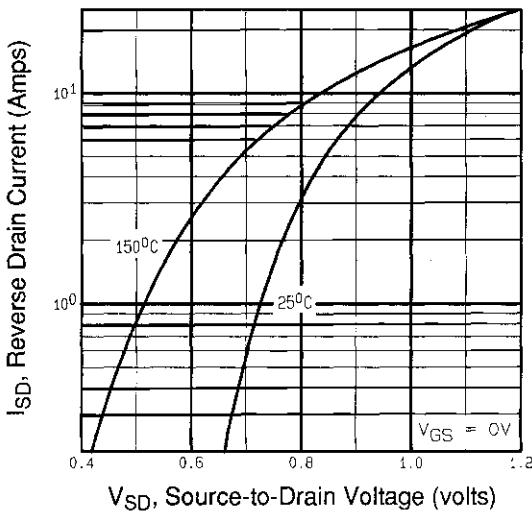
**Fig 4.** Normalized On-Resistance Vs. Temperature



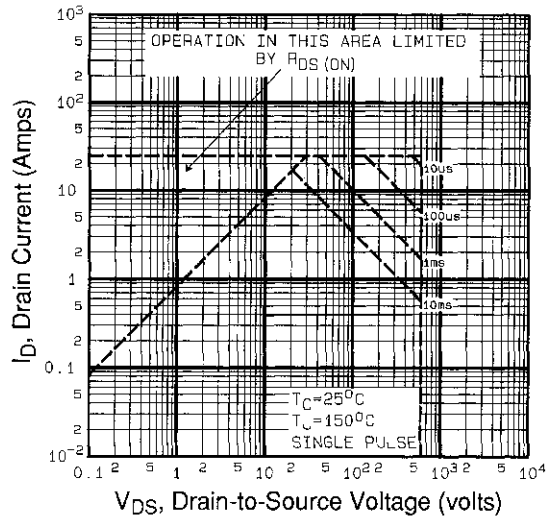
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



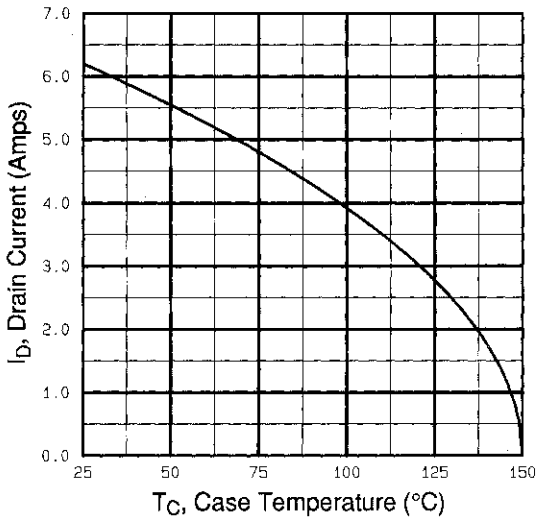
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



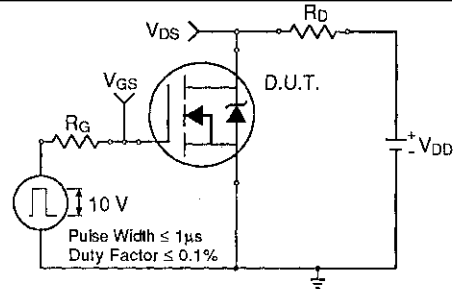
**Fig 7.** Typical Source-Drain Diode Forward Voltage



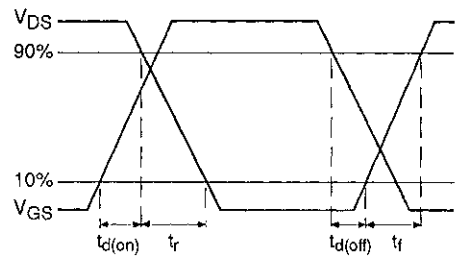
**Fig 8.** Maximum Safe Operating Area



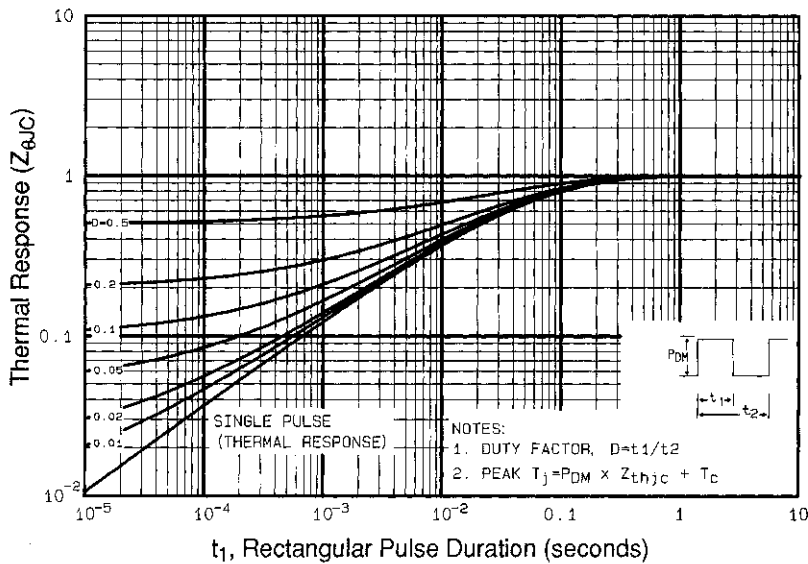
**Fig 9.** Maximum Drain Current Vs. Case Temperature



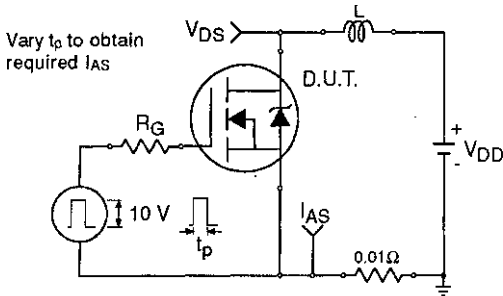
**Fig 10a.** Switching Time Test Circuit



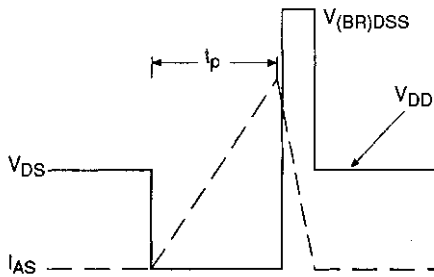
**Fig 10b.** Switching Time Waveforms



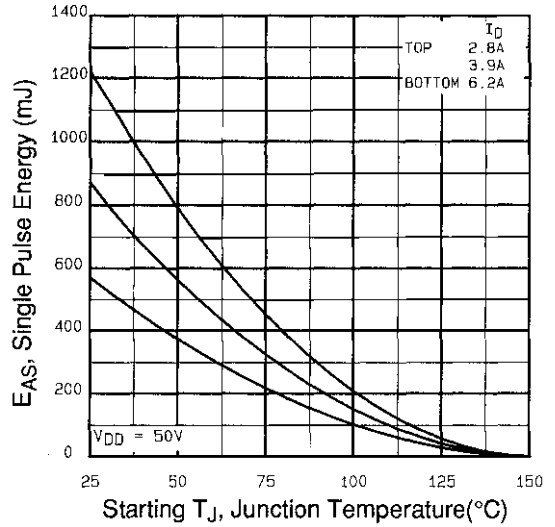
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



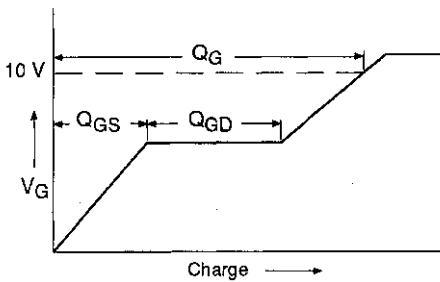
**Fig 12a.** Unclamped Inductive Test Circuit



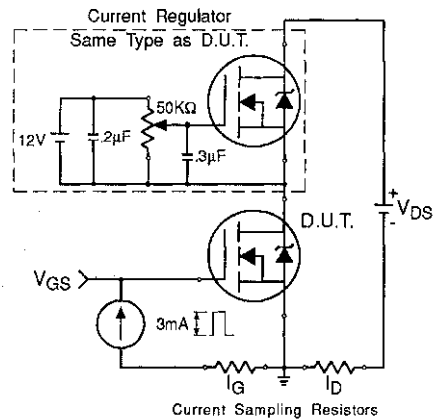
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

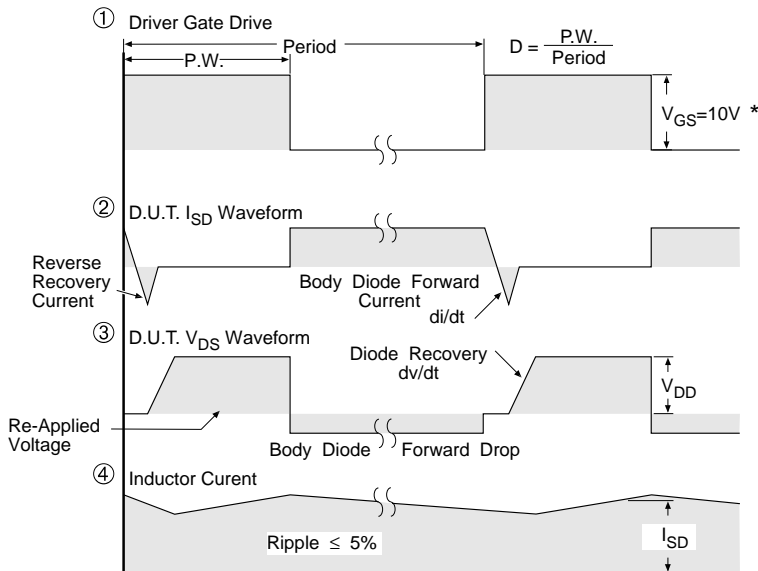
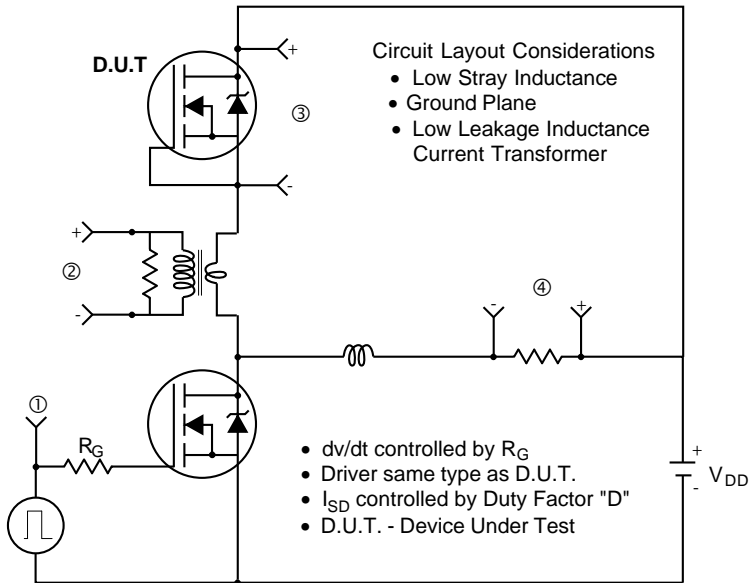


**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit

## Peak Diode Recovery dv/dt Test Circuit



\*  $V_{GS} = 5V$  for Logic Level Devices

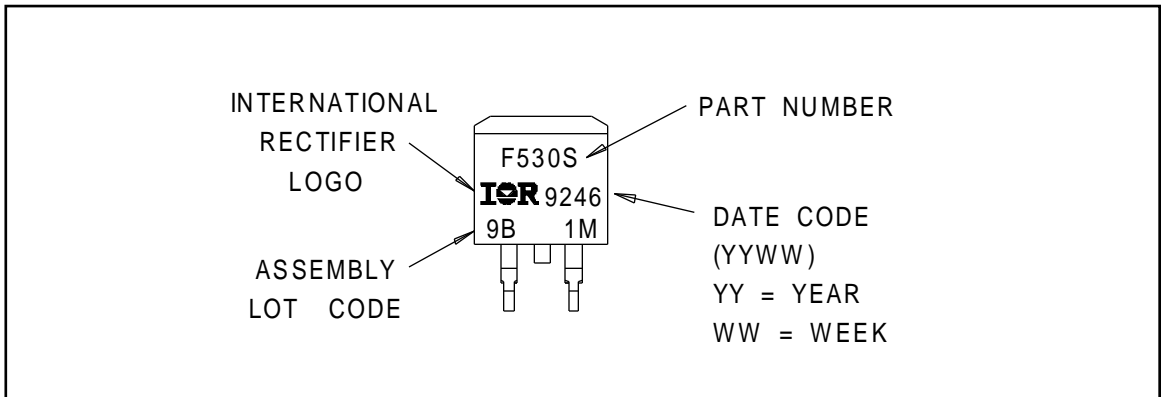
**Fig 14.**For N-Channel HEXFETS

## D<sup>2</sup>Pak Package Outline



## Part Marking Information

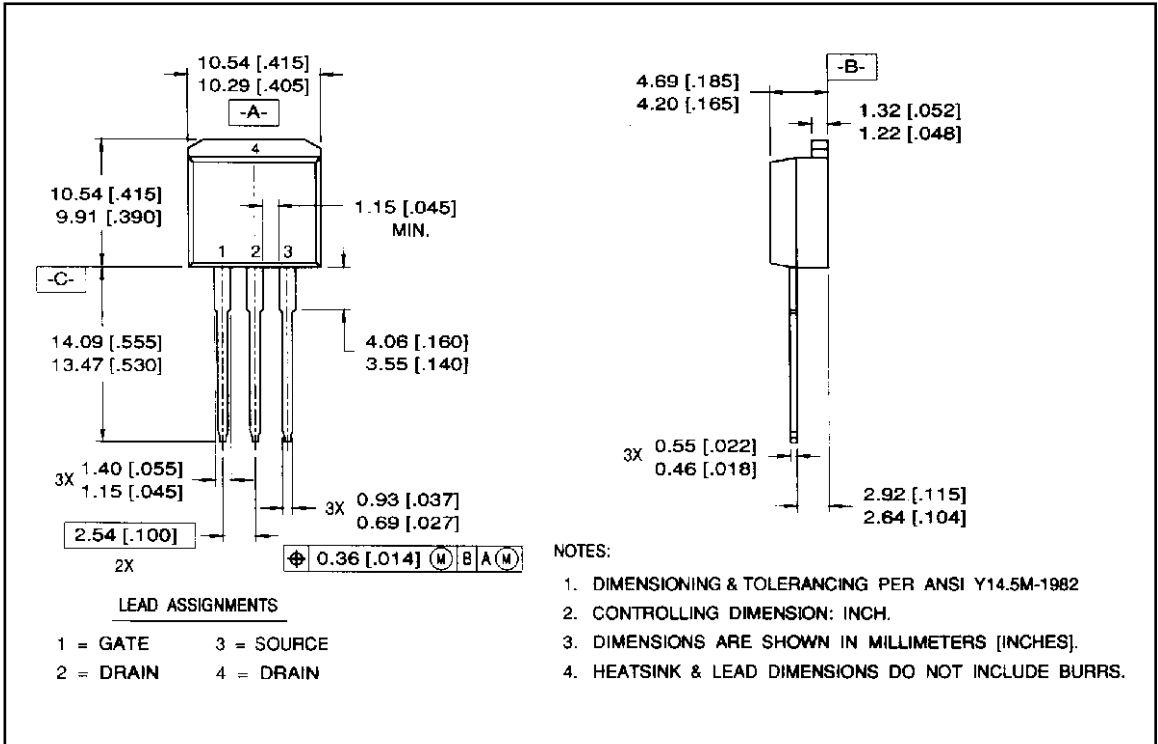
### D<sup>2</sup>Pak





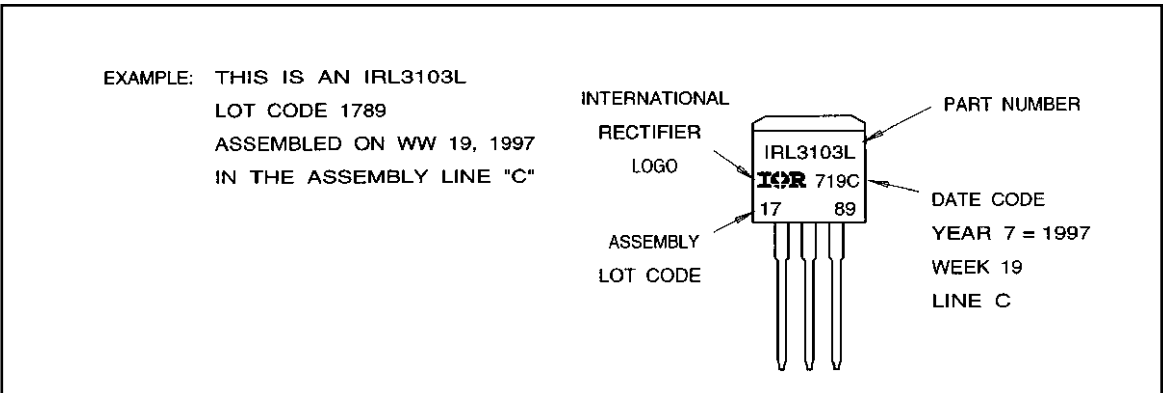
## Package Outline

### TO-262 Outline



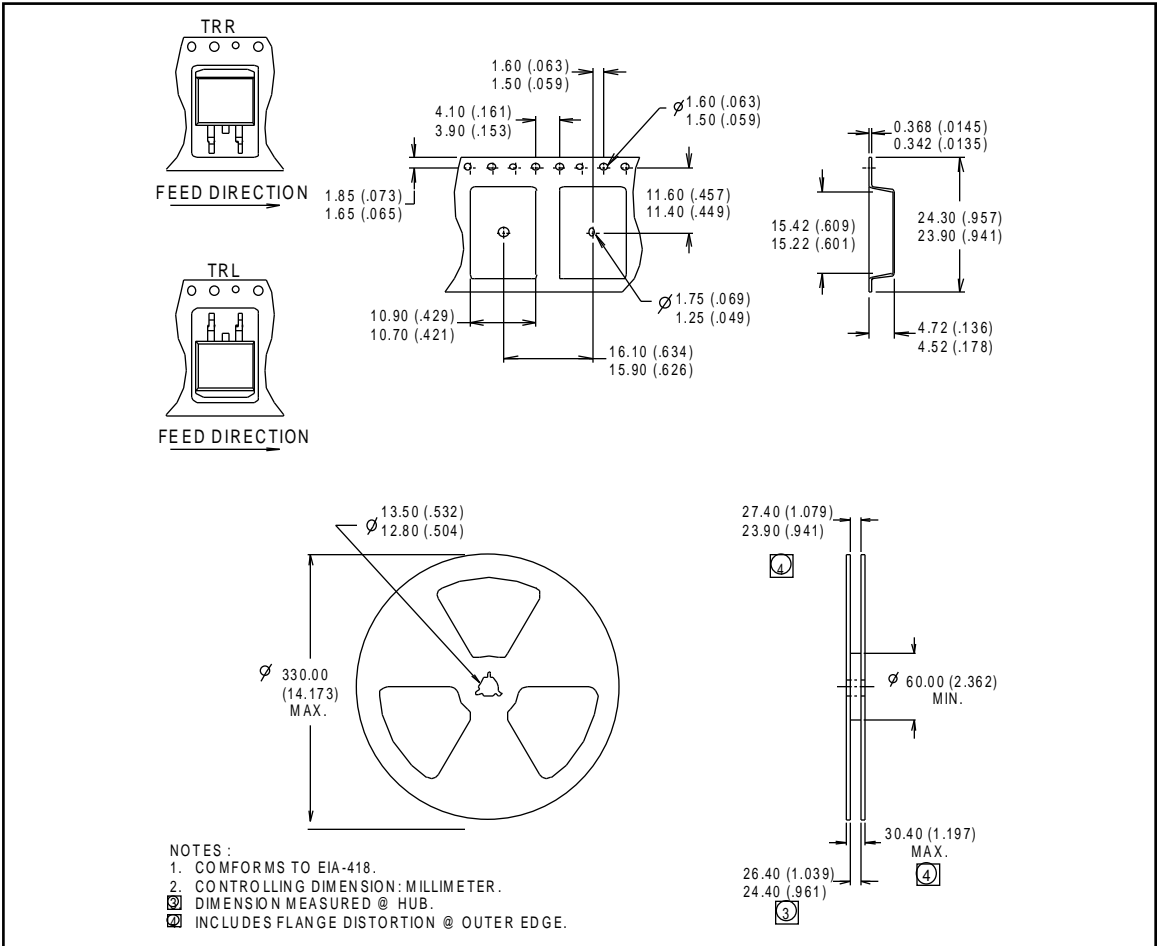
## Part Marking Information

### TO-262



## Tape & Reel Information

D<sup>2</sup>Pak



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Data and specifications subject to change without notice 9/01



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