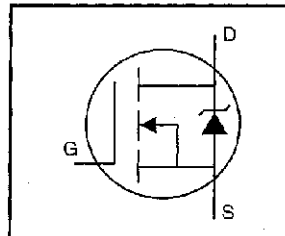


# IRFBE20PbF

## HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Lead-Free



$$V_{DSS} = 800V$$

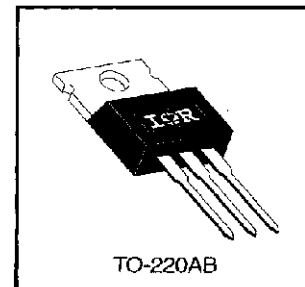
$$R_{DS(on)} = 6.5\Omega$$

$$I_D = 1.8A$$

### Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



### Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	1.8	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	1.2	
$I_{DM}$	Pulsed Drain Current ①	7.2	
$P_D @ T_C = 25^\circ C$	Power Dissipation	54	W
	Linear Derating Factor	0.43	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy ②	180	mJ
$I_{AR}$	Avalanche Current ①	1.8	A
$E_{AR}$	Repetitive Avalanche Energy ①	5.4	mJ
dv/dt	Peak Diode Recovery dv/dt ③	2.0	V/ns
$T_J$	Operating Junction and	-55 to +150	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting Torque, 6-32 or M3 screw	10 lbf·in (1.1 N·m)	


### Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	2.3	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	62	

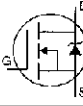
# IRFBE20PbF

International  
IR Rectifier

## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

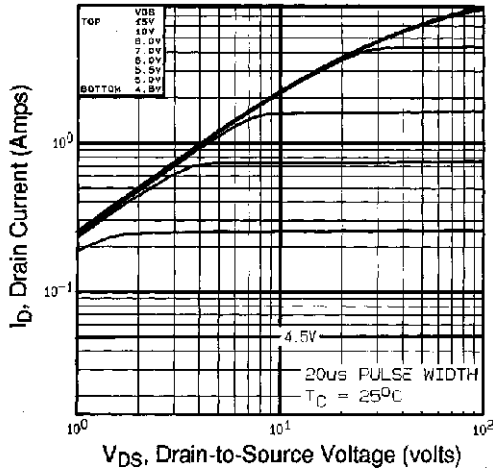
	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	800	—	—	V	$V_{GS}=0V, I_D=250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.98	—	V/°C	Reference to $25^\circ\text{C}, I_D=1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	6.5	$\Omega$	$V_{GS}=10V, I_D=1.1A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}, I_D=250\mu A$
$g_{fs}$	Forward Transconductance	0.80	—	—	S	$V_{DS}=100V, I_D=1.1A$ ④
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	100 500	$\mu A$	$V_{DS}=800V, V_{GS}=0V$ $V_{DS}=640V, V_{GS}=0V, T_J=125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS}=20V$
	Gate-to-Source Reverse Leakage	—	—	-100	nA	$V_{GS}=-20V$
$Q_g$	Total Gate Charge	—	—	38	nC	$I_D=1.8A$
$Q_{gs}$	Gate-to-Source Charge	—	—	5.0	nC	$V_{DS}=400V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	—	21	nC	$V_{GS}=10V$ See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	8.2	—	ns	$V_{DD}=400V$ $I_D=1.8A$ $R_G=18\Omega$ $R_D=230\Omega$ See Figure 10 ④
$t_r$	Rise Time	—	17	—		
$t_{d(off)}$	Turn-Off Delay Time	—	58	—		
$t_f$	Fall Time	—	27	—		
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact 
$L_S$	Internal Source Inductance	—	7.5	—		
$C_{iss}$	Input Capacitance	—	530	—	pF	$V_{GS}=0V$ $V_{DS}=25V$ $f=1.0\text{MHz}$ See Figure 5
$C_{oss}$	Output Capacitance	—	150	—		
$C_{rbs}$	Reverse Transfer Capacitance	—	90	—		

## Source-Drain Ratings and Characteristics

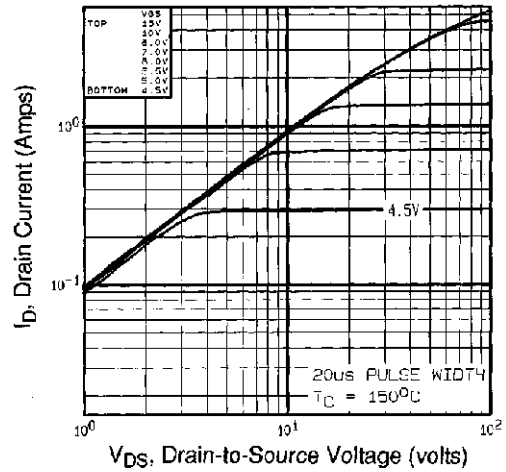
	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	1.8	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	7.2		
$V_{SD}$	Diode Forward Voltage	—	—	1.4	V	$T_J=25^\circ\text{C}, I_S=1.8A, V_{GS}=0V$ ④
$t_{rr}$	Reverse Recovery Time	—	380	570	ns	$T_J=25^\circ\text{C}, I_F=1.8A$
$Q_{rr}$	Reverse Recovery Charge	—	0.94	1.4	$\mu C$	$di/dt=100A/\mu s$ ④
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$ )				

### Notes:

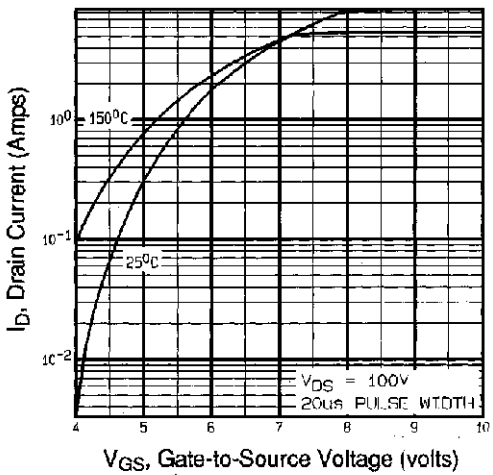
- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ②  $V_{DD}=50V$ , starting  $T_J=25^\circ\text{C}$ ,  $L=104\text{mH}$ ,  $R_G=25\Omega$ ,  $I_{AS}=1.8A$  (See Figure 12)
- ③  $I_{SD}\leq 1.8A$ ,  $di/dt\leq 80A/\mu s$ ,  $V_{DD}\leq 600V$ ,  $T_J\leq 150^\circ\text{C}$
- ④ Pulse width  $\leq 300\mu s$ ; duty cycle  $\leq 2\%$ .



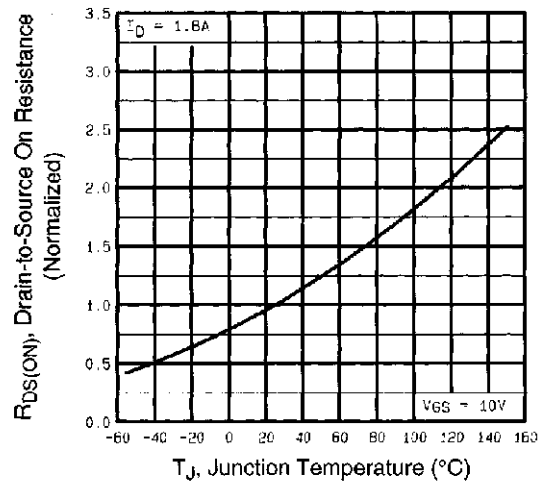
**Fig 1.** Typical Output Characteristics,  
 $T_C=25^\circ\text{C}$



**Fig 2.** Typical Output Characteristics,  
 $T_C=150^\circ\text{C}$

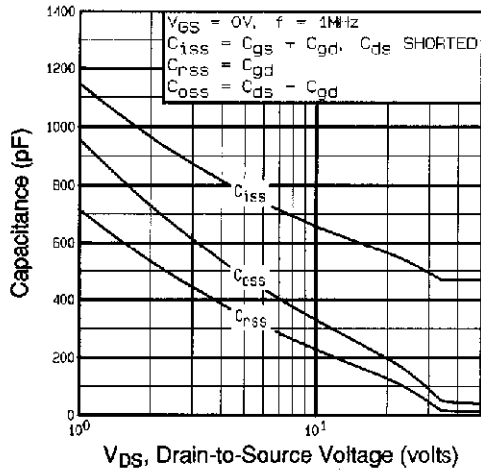


**Fig 3.** Typical Transfer Characteristics

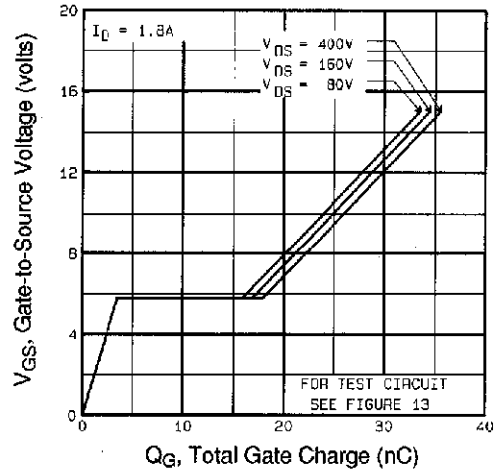


**Fig 4.** Normalized On-Resistance  
Vs. Temperature

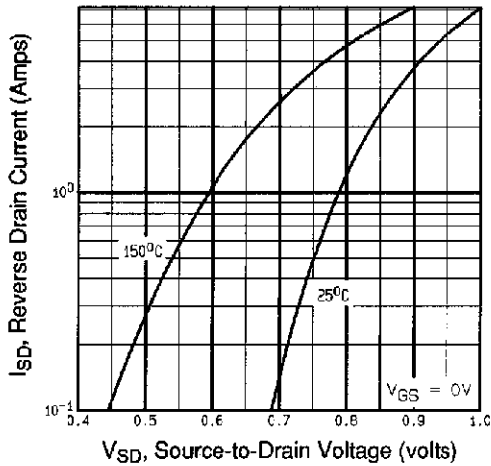
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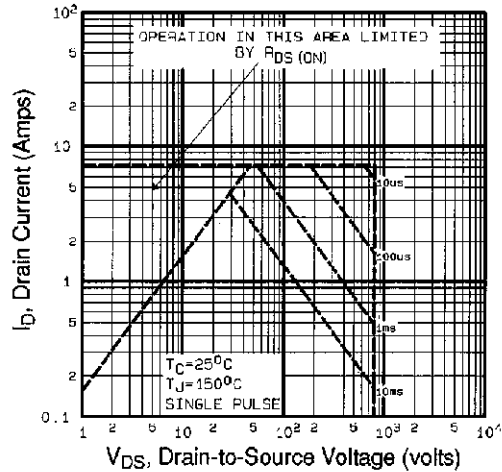
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage

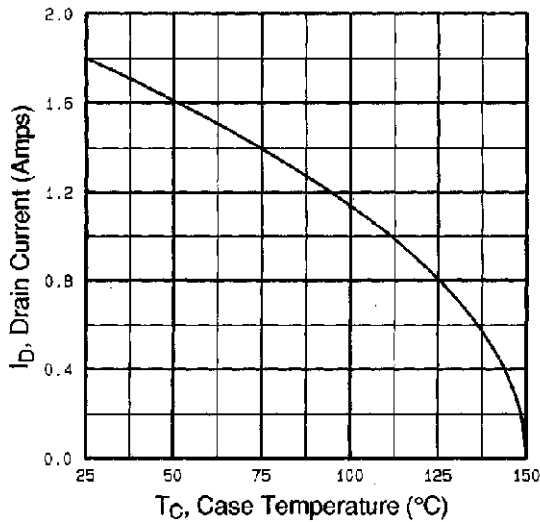


**Fig 7.** Typical Source-Drain Diode Forward Voltage

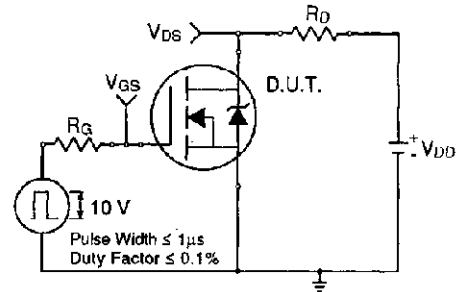


**Fig 8.** Maximum Safe Operating Area

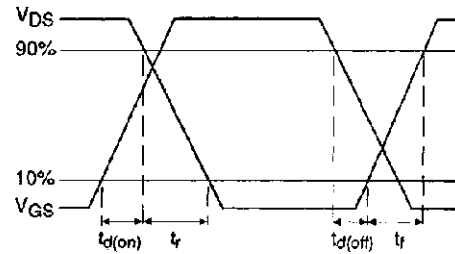
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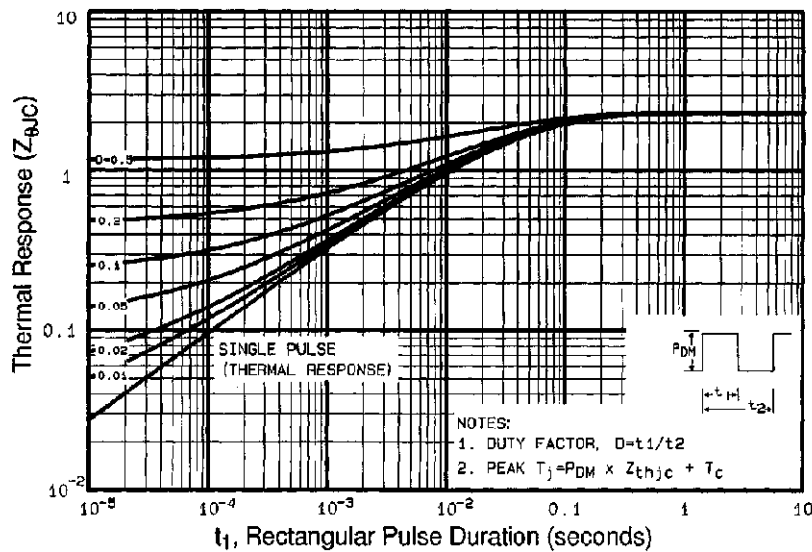
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit



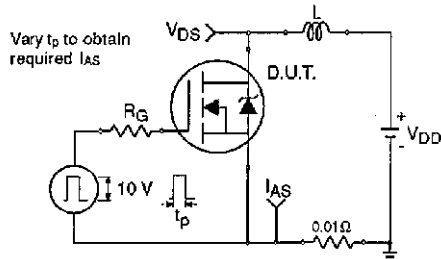
**Fig 10b.** Switching Time Waveforms



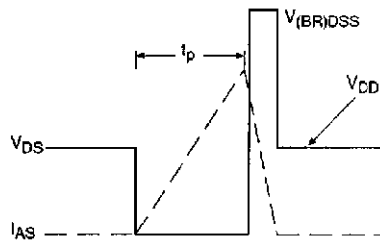
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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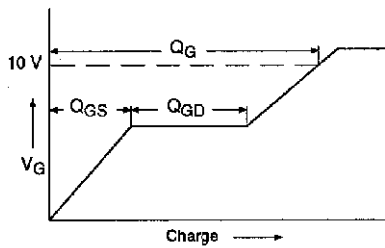
International  
**IR** Rectifier



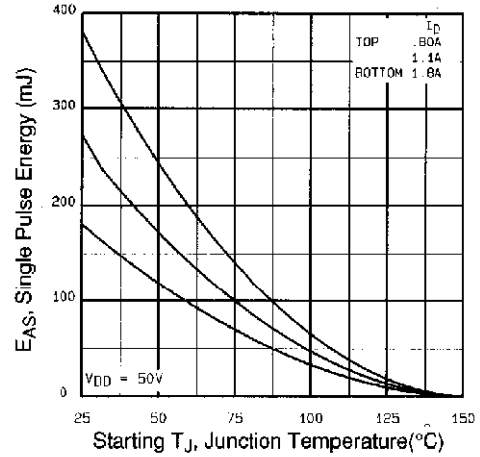
**Fig 12a.** Unclamped Inductive Test Circuit



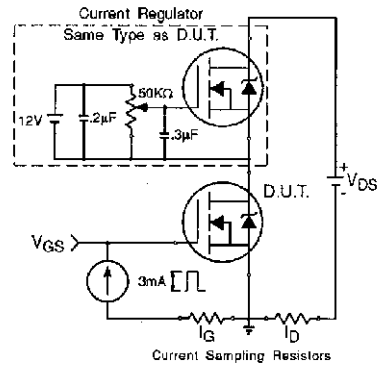
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform

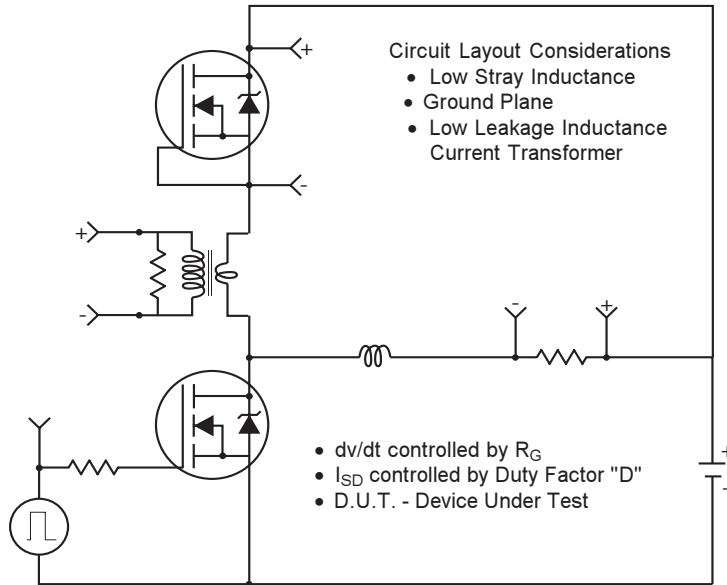


**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



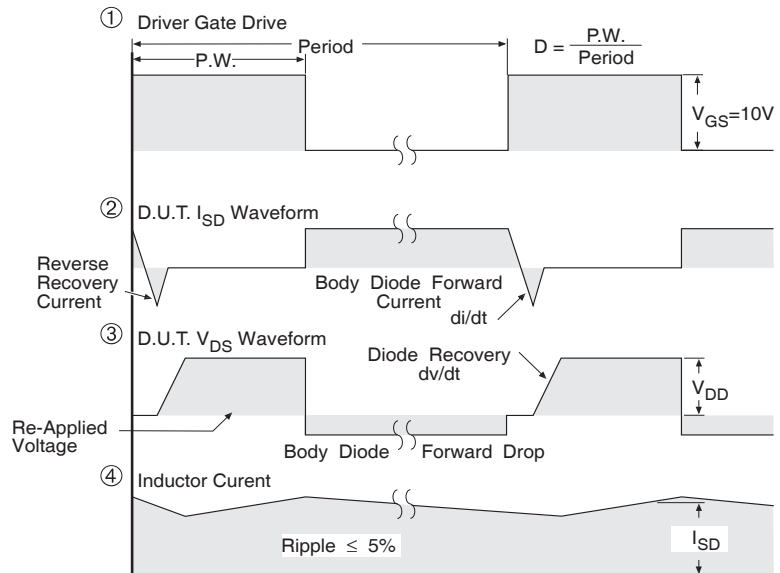
**Fig 13b.** Gate Charge Test Circuit

## Peak Diode Recovery dv/dt Test Circuit



\* Reverse Polarity for P-Channel

\*\* Use P-Channel Driver for P-Channel Measurements



\*\*\*  $V_{GS} = 5.0V$  for Logic Level and 3V Drive Devices

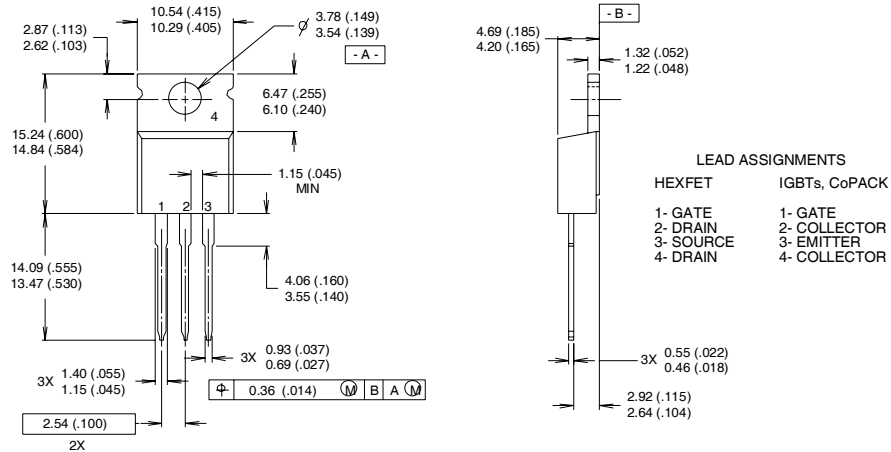
**Fig. 14** For N and P Channel HEXFETS

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## TO-220AB Package Outline

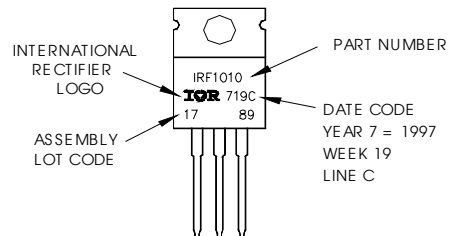
Dimensions are shown in millimeters (inches)



- NOTES:
- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
  - 2 CONTROLLING DIMENSION : INCH
  - 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
  - 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

## TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"  
**Note:** "P" in assembly line position indicates "Lead-Free"



Data and specifications subject to change without notice.



IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105  
 TAC Fax: (310) 252-7903  
 08/04





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