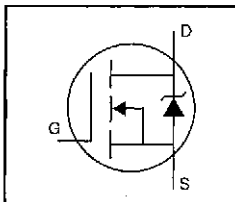


HEXFET® Power MOSFET

- Isolated Package
- High Voltage Isolation = 2.5KV RMS ③
- Sink to Lead Creepage Dist. = 4.8mm
- Dynamic dv/dt Rating
- Low Thermal Resistance



$$V_{DSS} = 500V$$

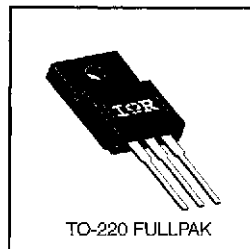
$$R_{DS(on)} = 3.0\Omega$$

$$I_D = 2.1A$$

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 Fullpak eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heatsink using a single clip or by a single screw fixing.



TO-220 FULLPAK
**DATA
SHEETS**
Absolute Maximum Ratings

| | Parameter | Max. | Units |
|-----------------------------|--|--------------------|-------|
| I_D @ $T_C = 25^\circ C$ | Continuous Drain Current, $V_{GS} @ 10V$ | 2.1 | |
| I_D @ $T_C = 100^\circ C$ | Continuous Drain Current, $V_{GS} @ 10V$ | 1.3 | A |
| I_{DM} | Pulsed Drain Current ① | 8.4 | |
| P_D @ $T_C = 25^\circ C$ | Power Dissipation | 30 | W |
| | Linear Derating Factor | 0.24 | W/°C |
| V_{GS} | Gate-to-Source Voltage | ± 20 | V |
| E_{AS} | Single Pulse Avalanche Energy ② | 110 | mJ |
| I_{AR} | Avalanche Current ③ | 2.1 | A |
| E_{AR} | Repetitive Avalanche Energy ④ | 3.0 | mJ |
| dv/dt | Peak Diode Recovery dv/dt ⑤ | 3.5 | V/ns |
| T_J | Operating Junction and Storage Temperature Range | -55 to +150 | °C |
| T_{STG} | | | |
| | | | |
| | Mounting Torque, 6-32 or M3 screw | 10 lb•in (1.1 N•m) | |


Thermal Resistance

| | Parameter | Min. | Typ. | Max. | Units |
|-----------------|---------------------|------|------|------|-------|
| $R_{\theta JC}$ | Junction-to-Case | — | — | 4.1 | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient | — | — | 65 | |

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Test Conditions |
|--------------------------------------|--------------------------------------|------|------|------|-------|--|
| V _{(BR)DSS} | Drain-to-Source Breakdown Voltage | 500 | — | — | V | V _{GS} =0V, I _D =250μA |
| ΔV _{(BR)DSS/ΔT_J} | Breakdown Voltage Temp. Coefficient | — | 0.59 | — | V/°C | Reference to 25°C, I _D =1mA |
| R _{DS(on)} | Static Drain-to-Source On-Resistance | — | — | 3.0 | Ω | V _{GS} =10V, I _D =1.3A ④ |
| V _{GS(th)} | Gate Threshold Voltage | 2.0 | — | 4.0 | V | V _{DS} =V _{GS} , I _D =250μA |
| g _{fs} | Forward Transconductance | 1.5 | — | — | S | V _{DS} =50V, I _D =1.3A ④ |
| I _{DSS} | Drain-to-Source Leakage Current | — | — | 25 | μA | V _{DS} =500V, V _{GS} =0V |
| I _{GSS} | Gate-to-Source Forward Leakage | — | — | 100 | nA | V _{DS} =400V, V _{GS} =0V, T _J =125°C |
| | Gate-to-Source Reverse Leakage | — | — | -100 | nA | V _{GS} =20V |
| Q _g | Total Gate Charge | — | — | 24 | nC | I _D =2.1A |
| Q _{gs} | Gate-to-Source Charge | — | — | 3.3 | nC | V _{DS} =400V |
| Q _{gd} | Gate-to-Drain ("Miller") Charge | — | — | 13 | nC | V _{GS} =10V See Fig. 6 and 13 ④ |
| t _{d(on)} | Turn-On Delay Time | — | 8.0 | — | ns | V _{DD} =250V |
| t _r | Rise Time | — | 8.6 | — | | I _D =2.1A |
| t _{d(off)} | Turn-Off Delay Time | — | 33 | — | | R _G =18Ω |
| t _f | Fall Time | — | 16 | — | | R _D =120Ω See Figure 10 ④ |
| L _D | Internal Drain Inductance | — | 4.5 | — | nH | Between lead, 6 mm (0.25in.) from package and center of die contact |
| L _S | Internal Source Inductance | — | 7.5 | — | |  |
| C _{iss} | Input Capacitance | — | 360 | — | pF | V _{GS} =0V |
| C _{oss} | Output Capacitance | — | 92 | — | | V _{DS} =25V |
| C _{rss} | Reverse Transfer Capacitance | — | 37 | — | | f=1.0MHz See Figure 5 |
| C | Drain to Sink Capacitance | — | 12 | — | pF | f=1.0MHz |

Source-Drain Ratings and Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Test Conditions |
|-----------------|--|--|------|------|-------|---|
| I _S | Continuous Source Current (Body Diode) | — | — | 2.1 | A | MOSFET symbol showing the integral reverse p-n junction diode.  |
| I _{SM} | Pulsed Source Current (Body Diode) ① | — | — | 8.0 | | |
| V _{SD} | Diode Forward Voltage | — | — | 1.6 | V | T _J =25°C, I _S =2.1A, V _{GS} =0V ④ |
| t _{rr} | Reverse Recovery Time | — | 260 | 520 | ns | T _J =25°C, I _F =2.1A |
| Q _{rr} | Reverse Recovery Charge | — | 0.70 | 1.4 | μC | di/dt=100A/μs ④ |
| t _{on} | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D) | | | | |

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ② V_{DD}=50V, starting T_J=25°C, L=44mH R_G=25Ω, I_{AS}=2.1A (See Figure 12)
- ③ I_{SD}≤2.1A, di/dt≤50A/μs, V_{DD}≤V_{(BR)DSS}, T_J≤150°C
- ④ t=60s, f=60Hz
- ⑤ Pulse width ≤ 300 μs; duty cycle ≤2%.

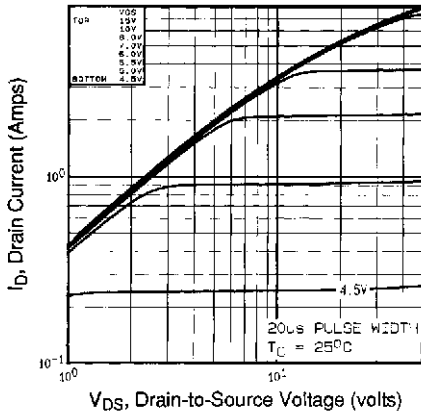


Fig 1. Typical Output Characteristics, $T_C=25^\circ\text{C}$

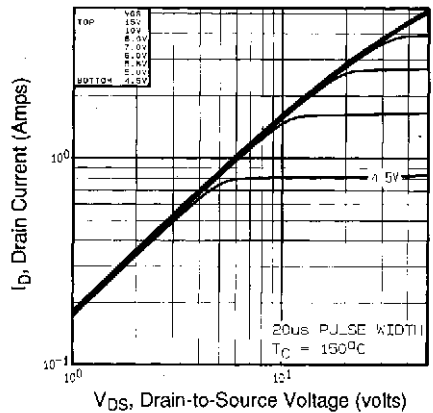


Fig 2. Typical Output Characteristics, $T_C=150^\circ\text{C}$

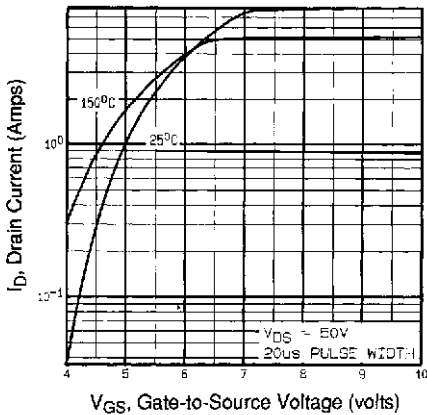


Fig 3. Typical Transfer Characteristics

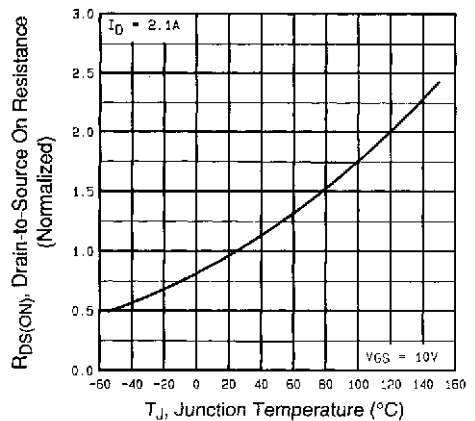


Fig 4. Normalized On-Resistance Vs. Temperature

DATA SHEETS

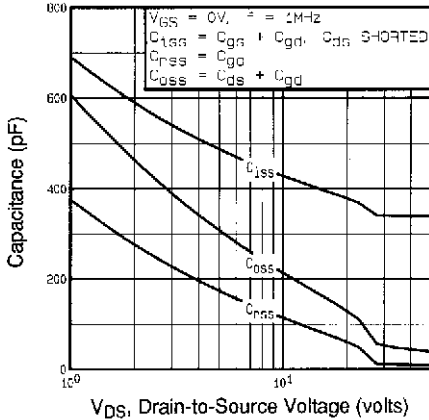


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

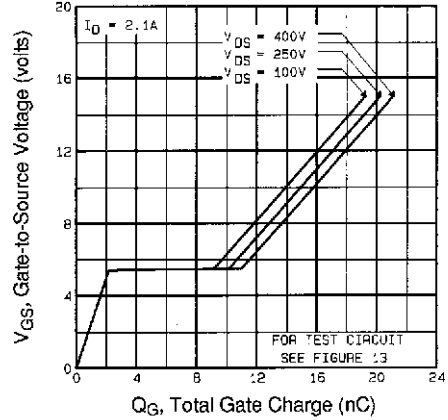


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

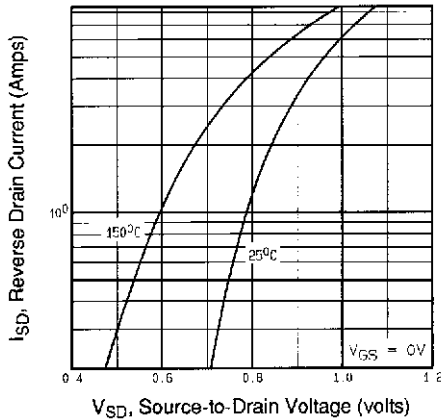


Fig 7. Typical Source-Drain Diode Forward Voltage

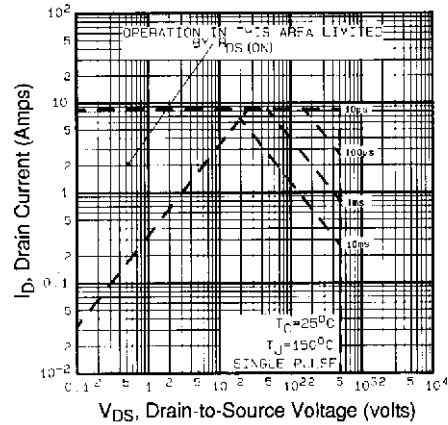


Fig 8. Maximum Safe Operating Area

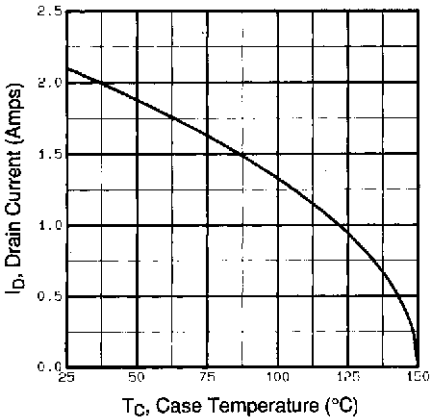


Fig 9. Maximum Drain Current Vs. Case Temperature

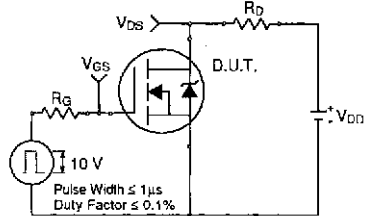


Fig 10a. Switching Time Test Circuit

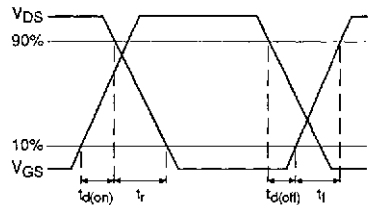


Fig 10b. Switching Time Waveforms

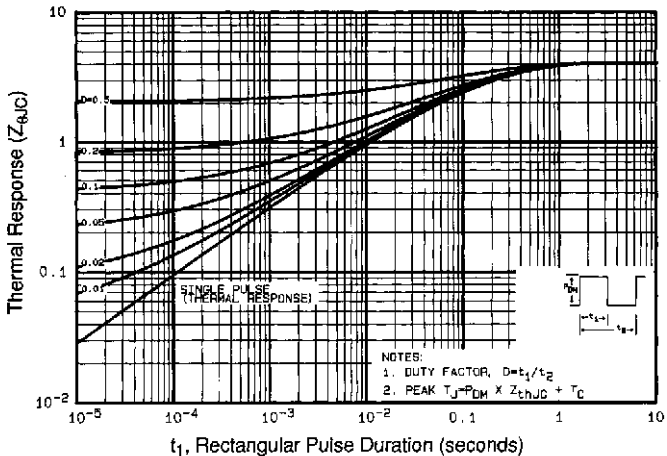


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

DATA SHEETS

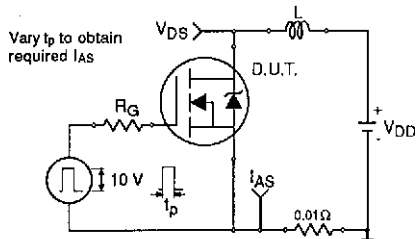


Fig 12a. Unclamped Inductive Test Circuit

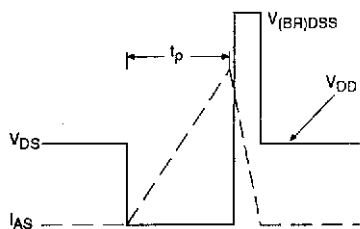


Fig 12b. Unclamped Inductive Waveforms

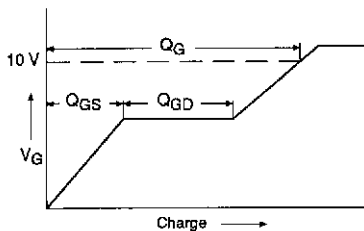


Fig 13a. Basic Gate Charge Waveform

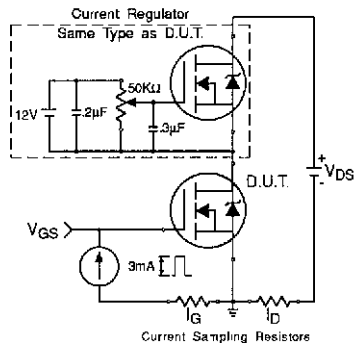


Fig 13b. Gate Charge Test Circuit

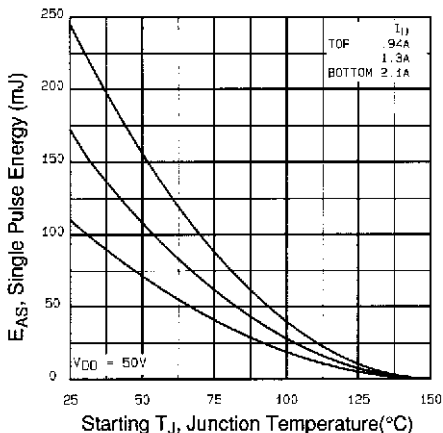


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

Appendix A: Figure 14, Peak Diode Recovery dv/dt Test Circuit – See page 1505

Appendix B: Package Outline Mechanical Drawing – See page 1510

Appendix C: Part Marking Information – See page 1517



Notice

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