

# IRFP23N50LPbF

## SMPS MOSFET

HEXFET® Power MOSFET

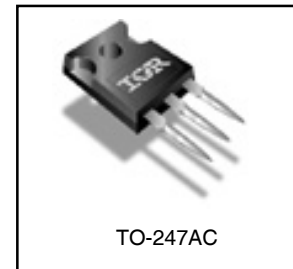
### Applications

- Zero Voltage Switching SMPS
- Telecom and Server Power Supplies
- Uninterruptible Power Supplies
- Motor Control applications
- Lead-Free

### Features and Benefits

- SuperFast body diode eliminates the need for external diodes in ZVS applications.
- Lower Gate charge results in simpler drive requirements.
- Enhanced dv/dt capabilities offer improved ruggedness.
- Higher Gate voltage threshold offers improved noise immunity.

$V_{DSS}$	$R_{DS(on)}$ typ.	$T_{rr}$ typ.	$I_D$
500V	0.190Ω	170ns	23A



### Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D$ @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS}$ @ 10V	23	A
$I_D$ @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS}$ @ 10V	15	
$I_{DM}$	Pulsed Drain Current ①	92	
$P_D$ @ $T_C = 25^\circ\text{C}$	Power Dissipation	370	W
	Linear Derating Factor	2.9	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	14	V/ns
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	

### Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	23	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	92		
$V_{SD}$	Diode Forward Voltage	—	—	1.5	V	$T_J = 25^\circ\text{C}$ , $I_S = 14\text{A}$ , $V_{GS} = 0\text{V}$ ④
$t_{rr}$	Reverse Recovery Time	—	170	250	ns	$T_J = 25^\circ\text{C}$ , $I_F = 23\text{A}$
		—	220	330		$T_J = 125^\circ\text{C}$ , $di/dt = 100\text{A}/\mu\text{s}$ ④
$Q_{rr}$	Reverse Recovery Charge	—	560	840	nC	$T_J = 25^\circ\text{C}$ , $I_S = 23\text{A}$ , $V_{GS} = 0\text{V}$ ④
		—	980	1500		$T_J = 125^\circ\text{C}$ , $di/dt = 100\text{A}/\mu\text{s}$ ④
$I_{RRM}$	Reverse Recovery Current	—	7.6	11	A	$T_J = 25^\circ\text{C}$
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

# IRFP23N50LPbF

International  
IR Rectifier

Static @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.27	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	0.190	0.235	$\Omega$	$V_{GS} = 10V, I_D = 14A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	50	$\mu A$	$V_{DS} = 500V, V_{GS} = 0V$
		—	—	2.0	mA	$V_{DS} = 400V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100	nA	$V_{GS} = -30V$
$R_G$	Internal Gate Resistance	—	1.2	—	$\Omega$	$f = 1MHz, \text{open drain}$

Dynamic @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	12	—	—	S	$V_{DS} = 50V, I_D = 14A$
$Q_g$	Total Gate Charge	—	—	150	nC	$I_D = 23A$ $V_{DS} = 400V$ $V_{GS} = 10V, \text{See Fig. 7 \& 15 } \textcircled{4}$
$Q_{gs}$	Gate-to-Source Charge	—	—	44		
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	—	72		
$t_{d(on)}$	Turn-On Delay Time	—	26	—	ns	$V_{DD} = 250V$ $I_D = 23A$ $R_G = 6.0\Omega$ $V_{GS} = 10V, \text{See Fig. 11a \& 11b } \textcircled{4}$
$t_r$	Rise Time	—	94	—		
$t_{d(off)}$	Turn-Off Delay Time	—	53	—		
$t_f$	Fall Time	—	45	—		
$C_{iss}$	Input Capacitance	—	3600	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0MHz, \text{See Fig. 5}$ $V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz$ $V_{GS} = 0V, V_{DS} = 400V, f = 1.0MHz$ $V_{GS} = 0V, V_{DS} = 0V \text{ to } 400V \textcircled{5}$
$C_{oss}$	Output Capacitance	—	380	—		
$C_{riss}$	Reverse Transfer Capacitance	—	37	—		
$C_{oss}$	Output Capacitance	—	4800	—		
$C_{oss}$	Output Capacitance	—	100	—		
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	220	—		
$C_{oss \text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related)	—	160	—		

## Avalanche Characteristics

Symbol	Parameter	Typ.	Max.	Units
$E_{AS}$	Single Pulse Avalanche Energy ②	—	410	mJ
$I_{AR}$	Avalanche Current ①	—	23	A
$E_{AR}$	Repetitive Avalanche Energy ①	—	37	mJ

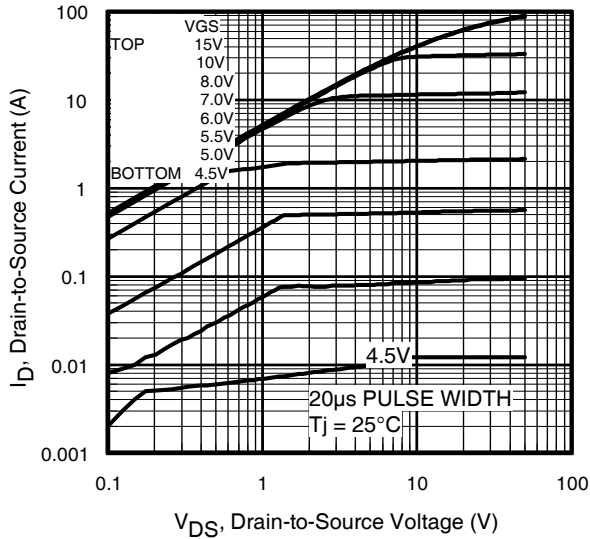
## Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.34	$^\circ\text{C/W}$
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	40	

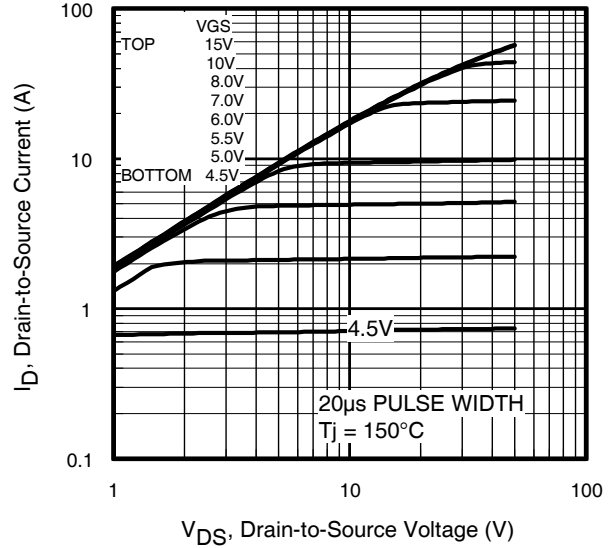
### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See Fig. 11).
- ② Starting  $T_J = 25^\circ\text{C}, L = 1.5mH, R_G = 25\Omega, I_{AS} = 23A, dv/dt = 14V/ns$ . (See Figure 12).
- ③  $I_{SD} \leq 23A, di/dt \leq 430A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$ .
- ④ Pulse width  $\leq 300\mu s$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{oss \text{ eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .  
 $C_{oss \text{ eff. (ER)}}$  is a fixed capacitance that stores the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

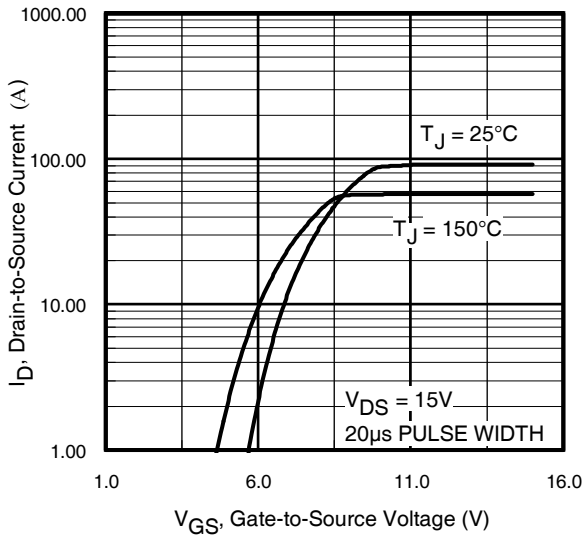
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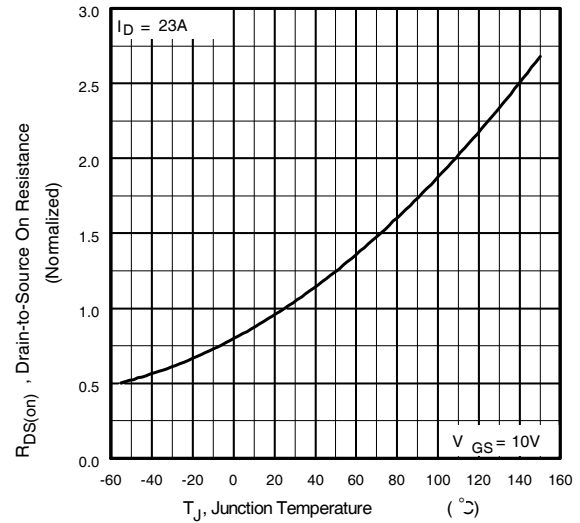
**Fig 1.** Typical Output Characteristics



**Fig 2.** Typical Output Characteristics

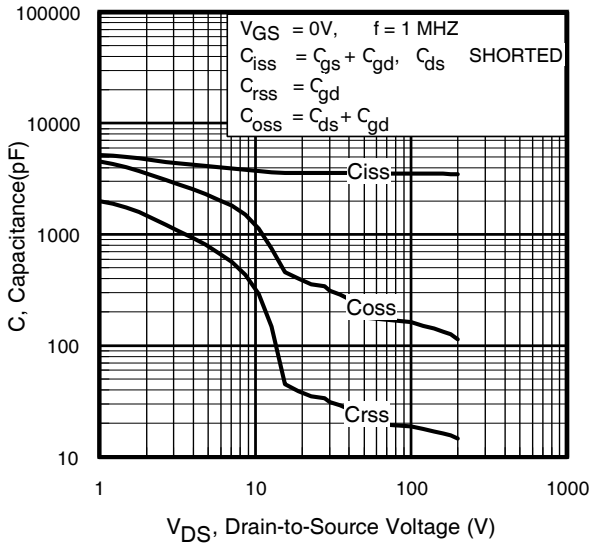


**Fig 3.** Typical Transfer Characteristics

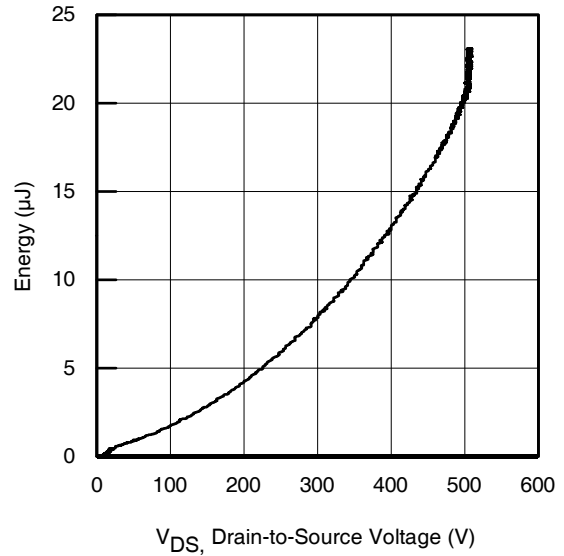


**Fig 4.** Normalized On-Resistance Vs. Temperature

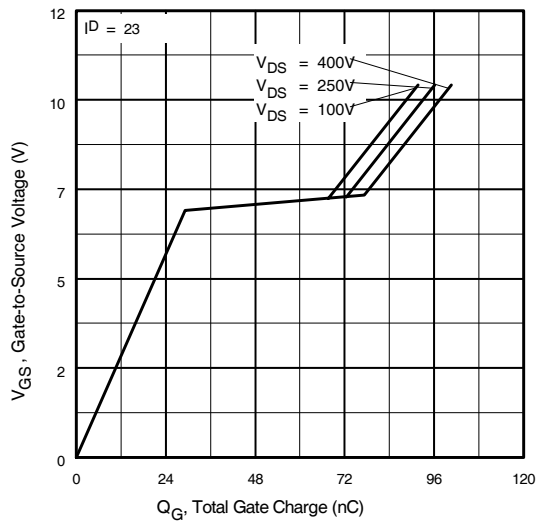
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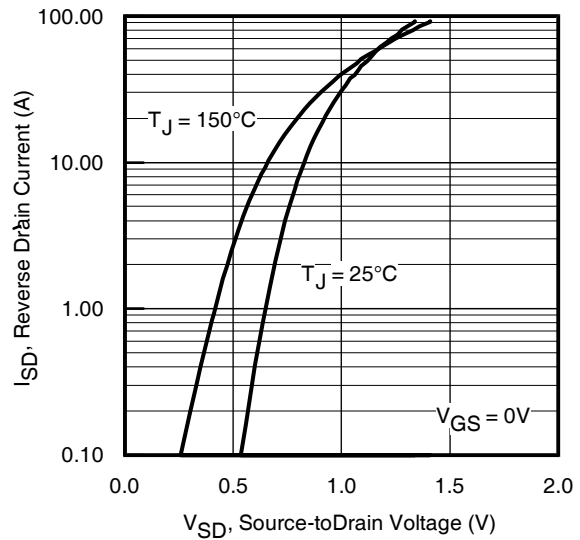
**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage



**Fig 6.** Typ. Output Capacitance Stored Energy vs.  $V_{DS}$

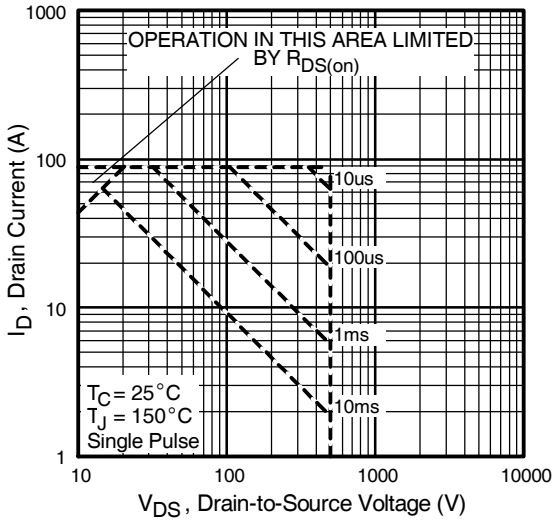


**Fig 7.** Typical Gate Charge vs. Gate-to-Source Voltage

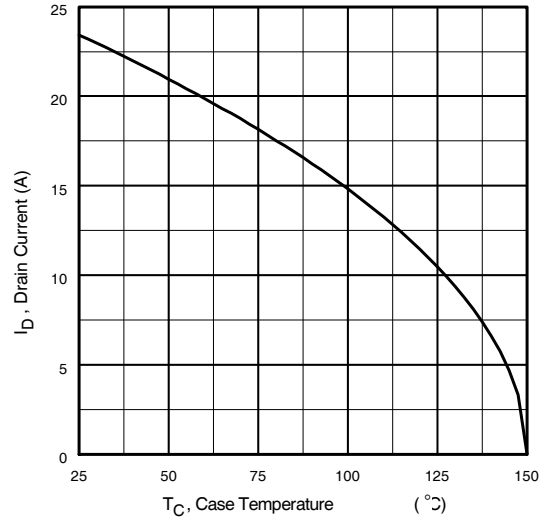


**Fig 8.** Typical Source-Drain Diode Forward Voltage

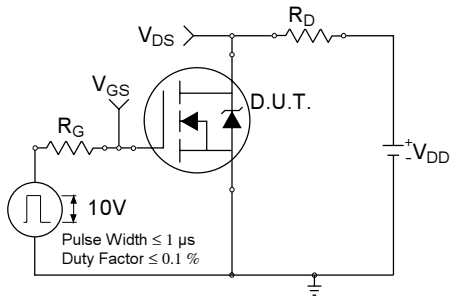
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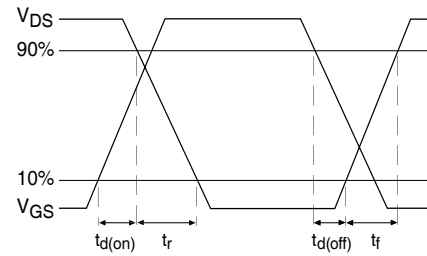
**Fig 9.** Maximum Safe Operating Area



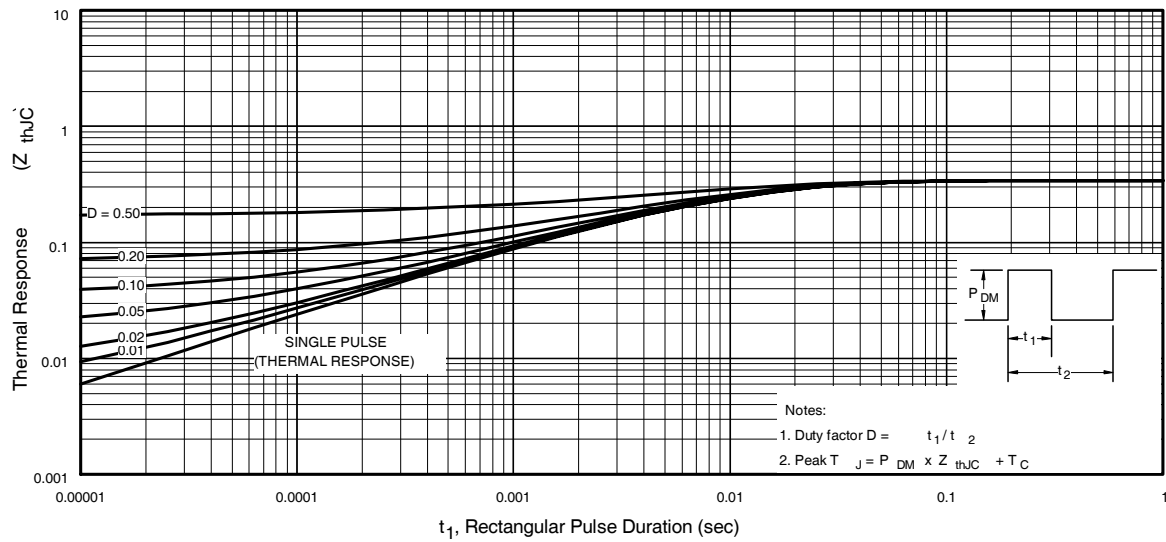
**Fig 10.** Maximum Drain Current vs. Case Temperature



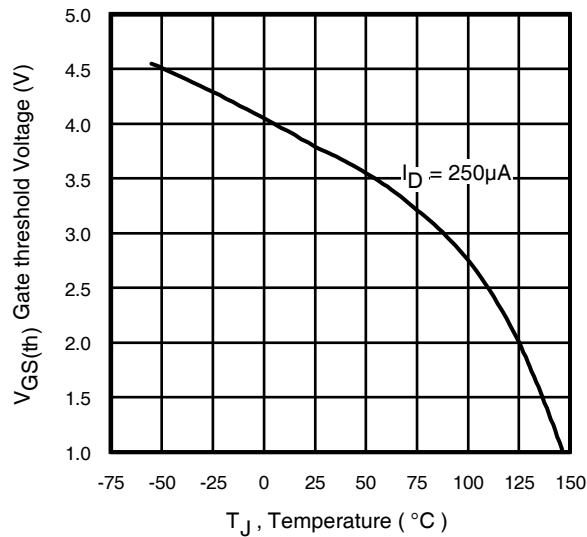
**Fig 11a.** Switching Time Test Circuit



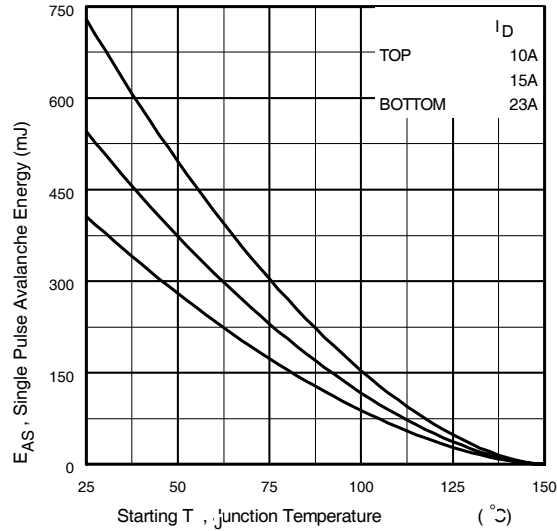
**Fig 11b.** Switching Time Waveforms



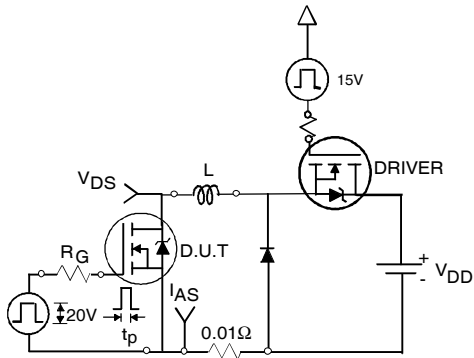
**Fig 12.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



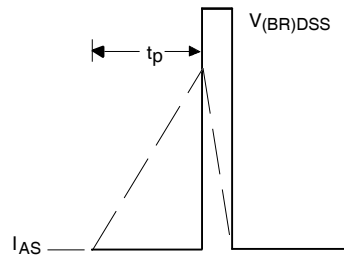
**Fig 13.** Threshold Voltage vs. Temperature



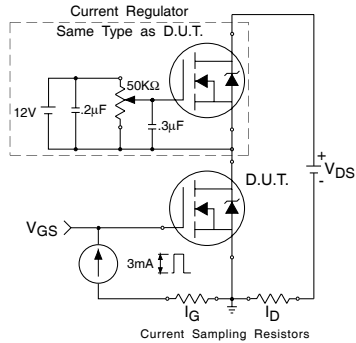
**Fig 14.** Maximum Avalanche Energy Vs. Drain Current



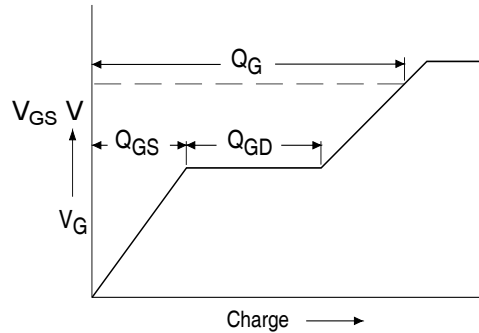
**Fig 15a.** Unclamped Inductive Test Circuit



**Fig 15b.** Unclamped Inductive Waveforms

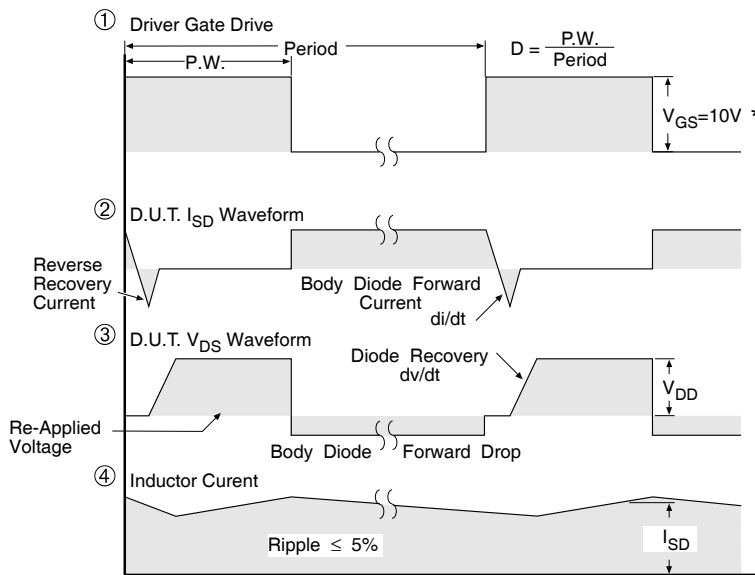
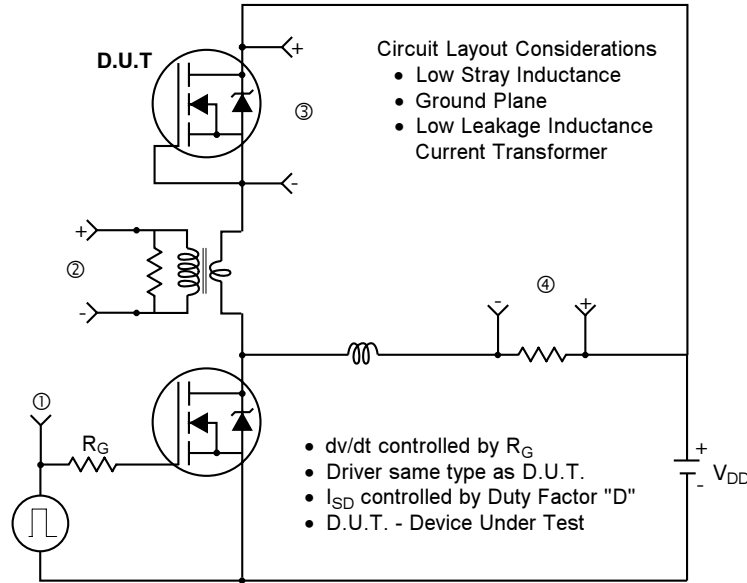


**Fig 16a.** Gate Charge Test Circuit



**Fig 16b.** Basic Gate Charge Waveform

## Peak Diode Recovery dv/dt Test Circuit



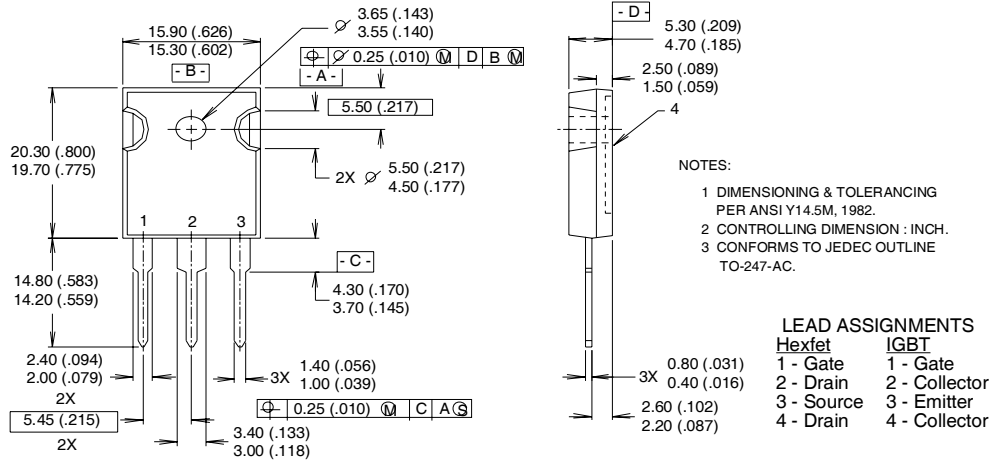
\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 17.** For N-Channel HEXFET® Power MOSFETs



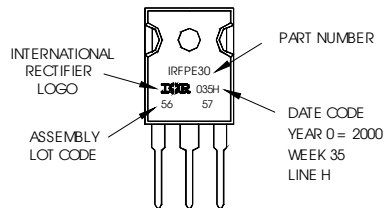
## TO-247AC Package Outline

Dimensions are shown in millimeters (inches)



## TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30  
 WITH ASSEMBLY  
 LOT CODE 5657  
 ASSEMBLED ON WW 35, 2000  
 IN THE ASSEMBLY LINE "H"  
**Note:** "P" in assembly line  
 position indicates "Lead-Free"



**TO-247AC package is not recommended for Surface Mount Application.**

Data and specifications subject to change without notice.  
 This product has been designed and qualified for the Industrial market.  
 Qualification Standards can be found on IR's Web site.



## Notice

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