

IRFPS30N60KPbF

HEXFET® Power MOSFET

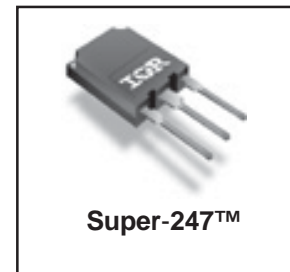
Applications

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching
- Lead-Free

V _{DSS}	R _{DS(on)} typ.	I _D
600V	160mΩ	30A

Benefits

- Low Gate Charge Qg results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current



Absolute Maximum Ratings

	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	30	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	19	
I _{DM}	Pulsed Drain Current ①	120	
P _D @ T _C = 25°C	Power Dissipation	450	W
	Linear Derating Factor	3.6	W/°C
V _{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	13	V/ns
T _J	Operating Junction and Storage Temperature Range	-55 to + 150	°C
T _{STG}			
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

Avalanche Characteristics

Symbol	Parameter	Typ.	Max.	Units
E _{AS}	Single Pulse Avalanche Energy②	—	520	mJ
I _{AR}	Avalanche Current①	—	30	A
E _{AR}	Repetitive Avalanche Energy①	—	45	mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case④	—	0.28	°C/W
R _{θCS}	Case-to-Sink, Flat, Greased Surface	0.24	—	
R _{θJA}	Junction-to-Ambient④	—	40	

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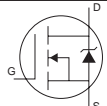
Static @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	600	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS/ΔT_J}	Breakdown Voltage Temp. Coefficient	—	0.66	—	V/°C	Reference to 25°C, I _D = 1mA ^⑥
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	160	190	mΩ	V _{GS} = 10V, I _D = 18A ^④
V _{GS(th)}	Gate Threshold Voltage	3.0	—	5.0	V	V _{DS} = V _{GS} , I _D = 250μA
I _{DSS}	Drain-to-Source Leakage Current	—	—	50	μA	V _{DS} = 600V, V _{GS} = 0V
		—	—	250		V _{DS} = 480V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 30V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -30V

Dynamic @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g _{fs}	Forward Transconductance	16	—	—	S	V _{DS} = 50V, I _D = 18A
Q _g	Total Gate Charge	—	—	220	nC	I _D = 30A
Q _{gs}	Gate-to-Source Charge	—	—	64		V _{DS} = 480V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	110		V _{GS} = 10V ^④
t _{d(on)}	Turn-On Delay Time	—	29	—	ns	V _{DD} = 300V
t _r	Rise Time	—	120	—		I _D = 30A
t _{d(off)}	Turn-Off Delay Time	—	56	—		R _G = 3.9 Ω
t _f	Fall Time	—	50	—		V _{GS} = 10V ^④
C _{iss}	Input Capacitance	—	5870	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	530	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	54	—		f = 1.0MHz
C _{oss}	Output Capacitance	—	6920	—		V _{GS} = 0V, V _{DS} = 1.0V, f = 1.0MHz
C _{oss}	Output Capacitance	—	140	—		V _{GS} = 0V, V _{DS} = 480V, f = 1.0MHz
C _{oss eff.}	Effective Output Capacitance	—	270	—		V _{GS} = 0V, V _{DS} = 0V to 480V ^⑤

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	30	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ^①	—	—	120		
V _{SD}	Diode Forward Voltage	—	—	1.5	V	T _J = 25°C, I _S = 30A, V _{GS} = 0V ^④
t _{rr}	Reverse Recovery Time	—	640	960	ns	T _J = 25°C, I _F = 30A
Q _{rr}	Reverse Recovery Charge	—	11	16	μC	di/dt = 100A/μs ^④
I _{RRM}	Reverse Recovery Current	—	31	—	A	
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting T_J = 25°C, L = 1.1mH, R_G = 25Ω, I_{AS} = 30A
- ③ I_{SD} ≤ 30A, di/dt ≤ 630A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 150°C
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%.
- ⑤ C_{oss eff.} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DS}
- ⑥ R_G is measured at T_J approximately 90°C

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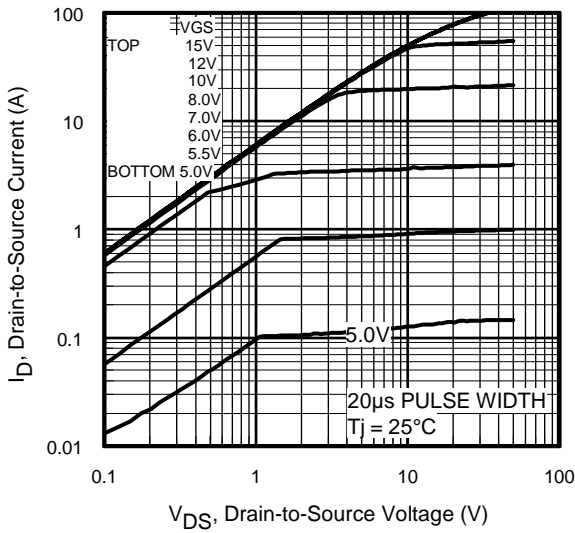


Fig 1. Typical Output Characteristics

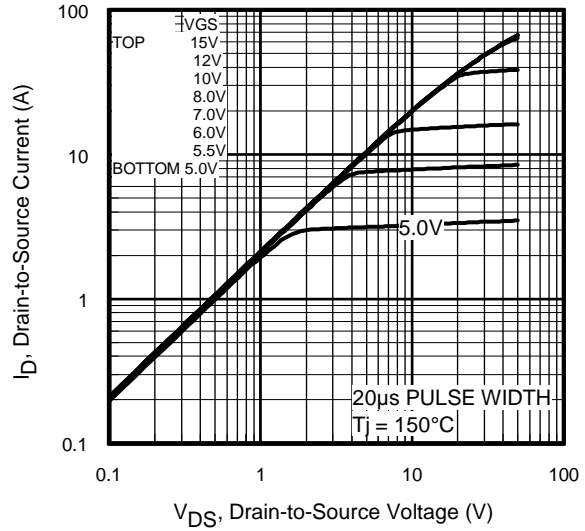


Fig 2. Typical Output Characteristics

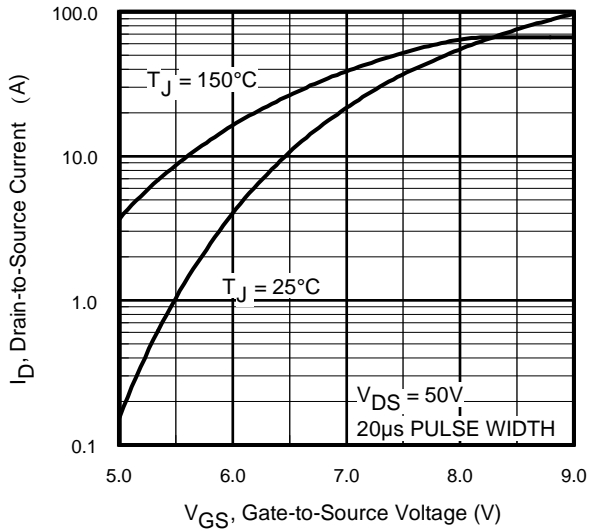


Fig 3. Typical Transfer Characteristics

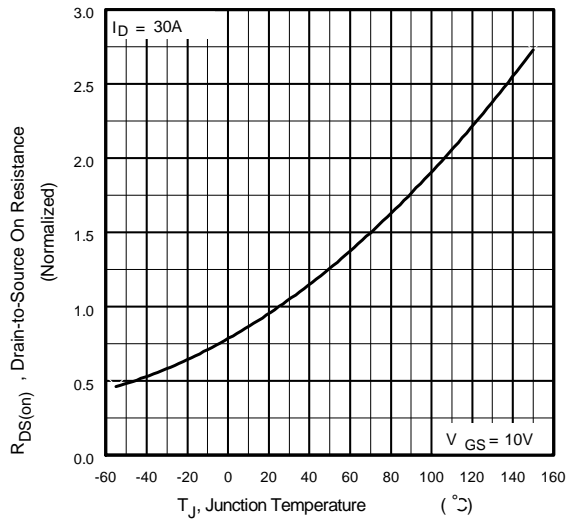


Fig 4. Normalized On-Resistance Vs. Temperature

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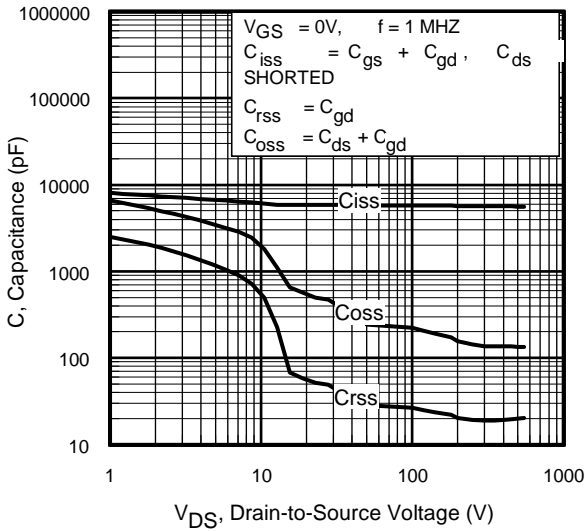


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

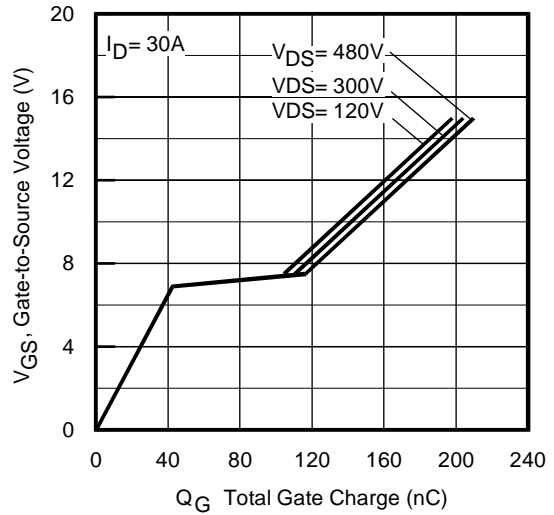


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

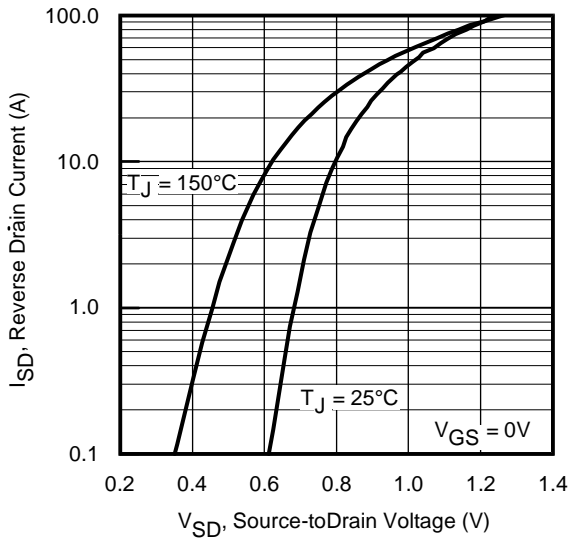


Fig 7. Typical Source-Drain Diode Forward Voltage

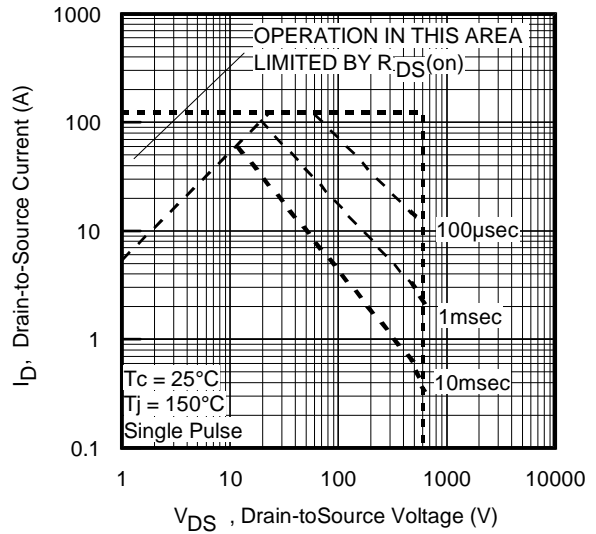


Fig 8. Maximum Safe Operating Area

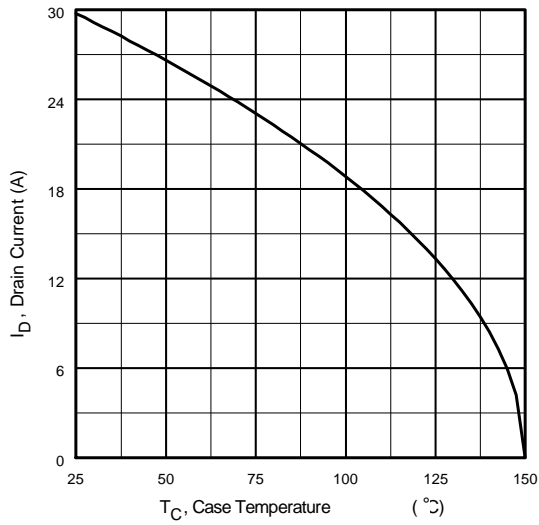


Fig 9. Maximum Drain Current Vs. Case Temperature



Fig 10a. Switching Time Test Circuit

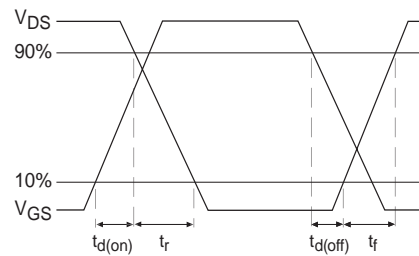


Fig 10b. Switching Time Waveforms

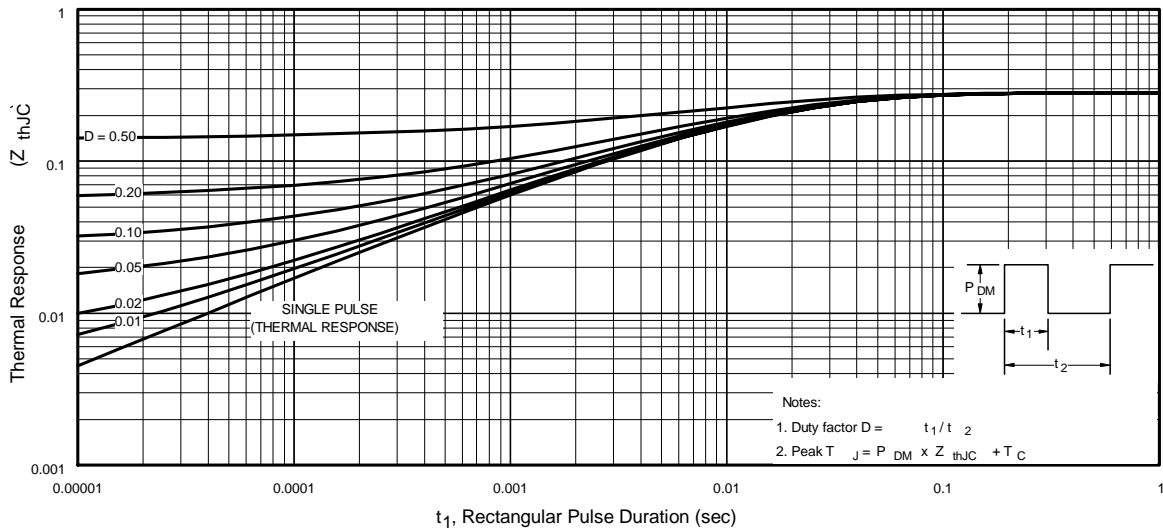


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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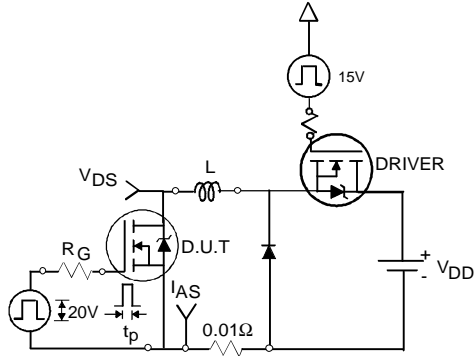


Fig 12a. Unclamped Inductive Test Circuit

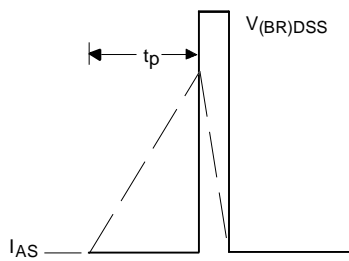


Fig 12b. Unclamped Inductive Waveforms

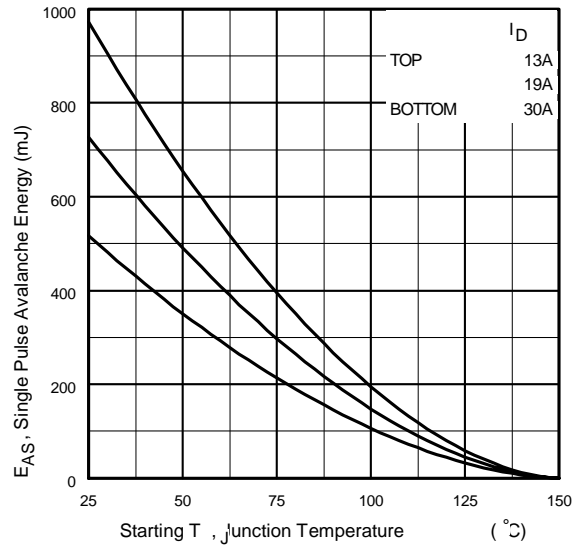


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

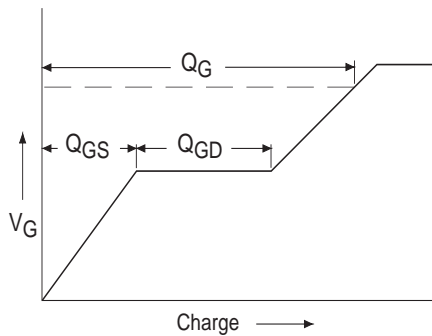


Fig 13a. Basic Gate Charge Waveform

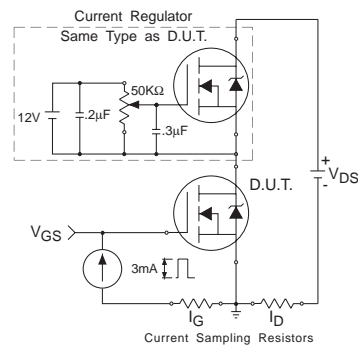
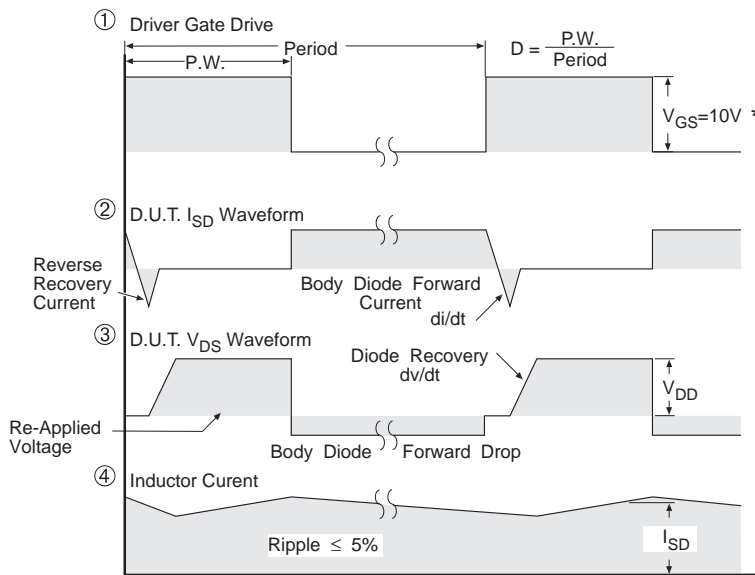
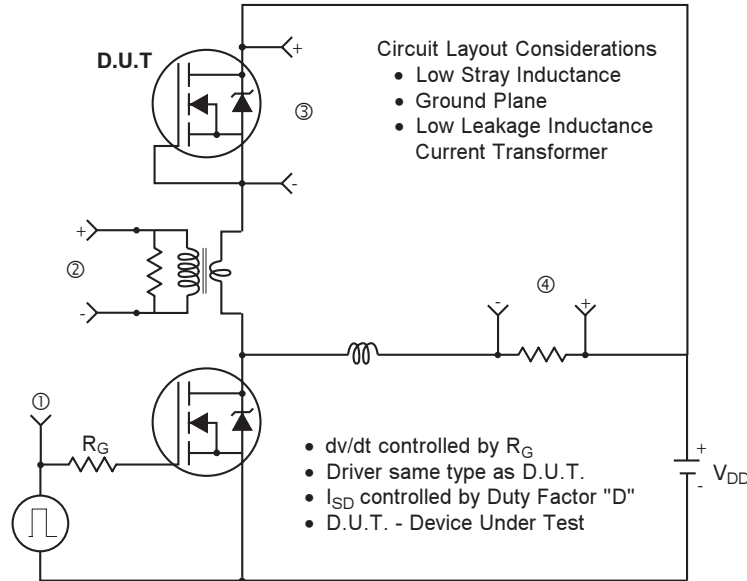


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



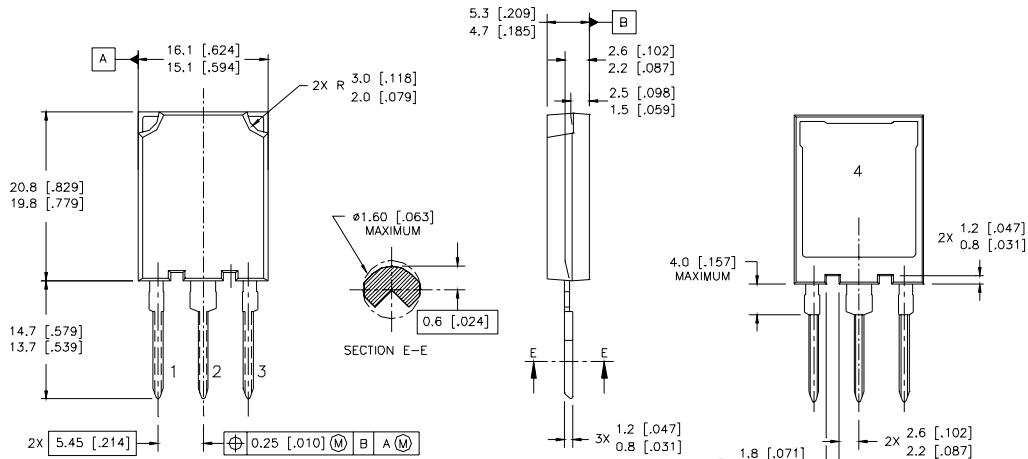
* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFET® Power MOSFETs

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Case Outline and Dimensions — Super-247

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NOTES:

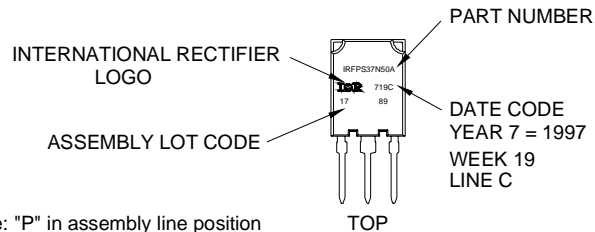
1. DIMENSIONS & TOLERANCING PER ASME Y14.5M-1994
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETRES [INCHES]

LEAD ASSIGNMENTS

MOSFET	IGBT
1 - GATE	1 - GATE
2 - DRAIN	2 - COLLECTOR
3 - SOURCE	3 - EMITTER
4 - DRAIN	4 - COLLECTOR

Super-247 (TO-274AA) Part Marking Information

EXAMPLE: THIS IS AN IRFPS37N50A WITH
ASSEMBLY LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



Note: "P" in assembly line position indicates "Lead-Free"

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

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09/04



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