

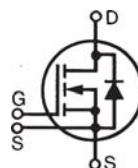
HiPerFET™

Power MOSFETs

Single Die MOSFET

IXFN280N085

N-Channel Enhancement Mode
Avalanche Rated, High dv/dt, Low t_{rr}



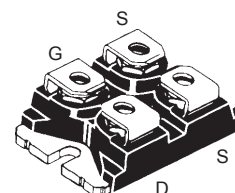
$$V_{DSS} = 85V$$

$$I_{D25} = 280A$$

$$R_{DS(on)} \leq 4.4m\Omega$$

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ C$ to $150^\circ C$	85	V
V_{DGR}	$T_J = 25^\circ C$ to $150^\circ C$, $R_{GS} = 1M\Omega$	85	V
V_{GSS}	Continuous	± 20	V
V_{GSM}	Transient	± 30	V
I_{D25}	$T_C = 25^\circ C$, Chip capability	280	A
$I_{L(RMS)}$	Terminal current limit	100	A
I_{DM}	$T_C = 25^\circ C$, pulse width limited by T_{JM}	1120	A
I_{AR}	$T_C = 25^\circ C$	200	A
E_{AS}	$T_C = 25^\circ C$	4	J
dv/dt	$I_S \leq I_{DM}$, $V_{DD} \leq V_{DSS}$, $T_J \leq 150^\circ C$	5	V/ns
P_d	$T_C = 25^\circ C$	700	W
T_J		-55 ... +150	$^\circ C$
T_{JM}		150	$^\circ C$
T_{stg}		-55 ... +150	$^\circ C$
V_{ISOL}	50/60 Hz, RMS $t = 1min$	2500	V~
	$I_{ISOL} \leq 1mA$ $t = 1s$	3000	V~
M_d	Mounting torque	1.5/13	Nm/lb.in.
	Terminal connection torque	1.3/11.5	Nm/lb.in.
Weight		30	g

miniBLOC, SOT-227 B(IXFN)
E153432



G = Gate D = Drain
S = Source

Either Source terminal at miniBLOC can be used as Main or Kelvin Source

Features

- International standard packages
- miniBLOC, with Aluminium nitride isolation
- Low $R_{DS(on)}$ HDMOS™ process
- Rugged polysilicon gate cell structure
- Unclamped Inductive Switching (UIS) rated
- Low package inductance
- Fast intrinsic Rectifier

Applications

- DC-DC converters
- Battery chargers
- Switched-mode and resonant-mode power supplies
- DC choppers
- Temperature and lighting controls

Advantages

- Easy to mount
- Space savings
- High power density

Symbol	Test Conditions	Characteristic Values		
		$(T_J = 25^\circ C, \text{ unless otherwise specified})$		
		Min.	Typ.	Max.
BV_{DSS}	$V_{GS} = 0V, I_D = 3mA$	85		V
$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 8mA$	2.0		4.0 V
I_{GSS}	$V_{GS} = \pm 20V, V_{DS} = 0V$			± 200 nA
I_{DSS}	$V_{DS} = V_{DSS}$			100 μA
	$V_{GS} = 0V$ $T_J = 125^\circ C$			2 mA
$R_{DS(on)}$	$V_{GS} = 10V, I_D = 100A, \text{ Note 1}$			4.4 $m\Omega$

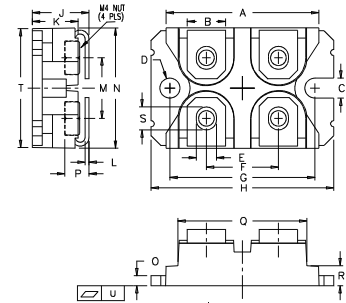
Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, unless otherwise specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$V_{DS} = 10\text{V}, I_D = 60\text{A}$, Note 1	50	85	S
C_{iss}	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}, f = 1\text{MHz}$		18.4	nF
C_{oss}			6.7	nF
C_{rss}			2.9	nF
$t_{d(on)}$	Resistive Switching Times $V_{GS} = 10\text{V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 100\text{A}$ $R_G = 2\Omega$ (External)		41	ns
t_r			67	ns
$t_{d(off)}$			90	ns
t_f			57	ns
$Q_{g(on)}$		$V_{GS} = 10\text{V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 100\text{A}$		440
Q_{gs}			65	nC
Q_{gd}			230	nC
R_{thJC}			0.18	$^\circ\text{C/W}$
R_{thCS}		0.05		$^\circ\text{C/W}$

Source-Drain Diode

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, unless otherwise specified)	Characteristic Values		
		Min.	Typ.	Max.
I_S	$V_{GS} = 0\text{V}$			280 A
I_{SM}	Repetitive, pulse width limited by T_{JM}			1120 A
V_{SD}	$I_F = 100\text{A}, V_{GS} = 0\text{V}$, Note 1			1.2 V
t_{rr}	$I_F = 50\text{A}, -di/dt = 100\text{A}/\mu\text{s}, V_R = 50\text{V}$			200 ns
Q_{RM}			0.76	μC
I_{RM}			8.00	A

Note 1: Pulse test, $t \leq 300\mu\text{s}$; duty cycle, $d \leq 2\%$.

miniBLOC, SOT-227 B



M4 screws (4x) supplied

Dim.	Millimeter		Inches	
	Min.	Max.	Min.	Max.
A	31.50	31.88	1.240	1.255
B	7.80	8.20	0.307	0.323
C	4.09	4.29	0.161	0.169
D	4.09	4.29	0.161	0.169
E	4.09	4.29	0.161	0.169
F	14.91	15.11	0.587	0.595
G	30.12	30.30	1.186	1.193
H	38.00	38.23	1.496	1.505
J	11.68	12.22	0.460	0.481
K	8.92	9.60	0.351	0.378
L	0.76	0.84	0.030	0.033
M	12.60	12.85	0.496	0.506
N	25.15	25.42	0.990	1.001
O	1.98	2.13	0.078	0.084
P	4.95	5.97	0.195	0.235
Q	26.54	26.90	1.045	1.059
R	3.94	4.42	0.155	0.174
S	4.72	4.85	0.186	0.191
T	24.59	25.07	0.968	0.987
U	-0.05	0.1	-0.002	0.004

PRELIMINARY TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from data gathered during objective characterizations of preliminary engineering lots; but also may yet contain some information supplied during a pre-production design evaluation. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

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IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,931,844 5,049,961 5,237,481 6,162,665 6,404,065 B1 6,683,344 6,727,585 7,005,734 B2 7,157,338B2
4,850,072 5,017,508 5,063,307 5,381,025 6,259,123 B1 6,534,343 6,710,405 B2 6,759,692 7,063,975 B2
4,881,106 5,034,796 5,187,117 5,486,715 6,306,728 B1 6,583,505 6,710,463 6,771,478 B2 7,071,537

Fig. 1. Extended Output Characteristics @ 25°C

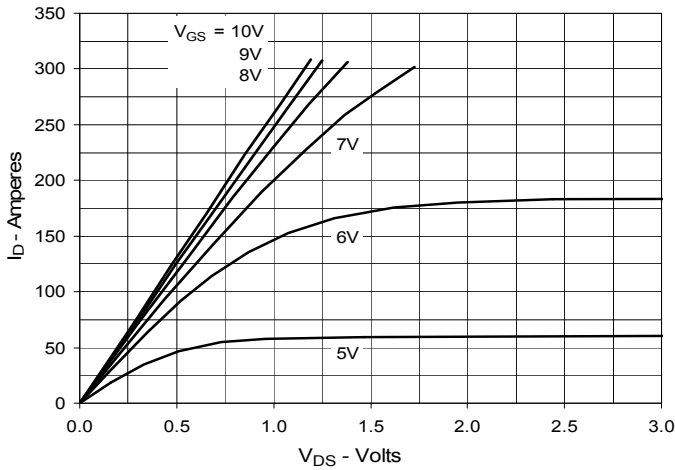


Fig. 2. Output Characteristics @ 125°C

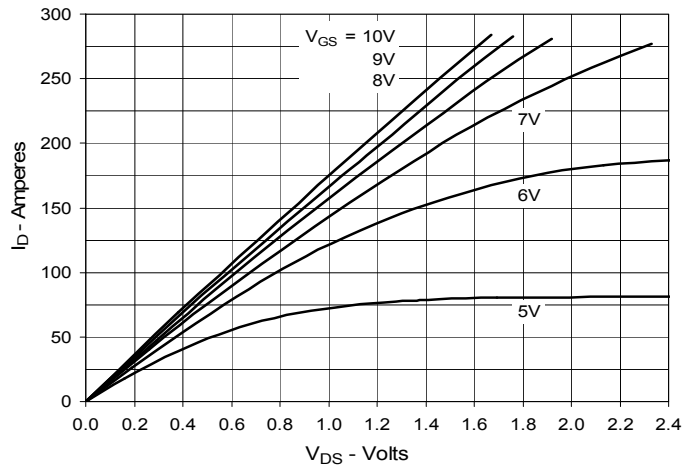


Fig. 3. $R_{DS(on)}$ Normalized to $I_D = 140A$ Value vs. Junction Temperature

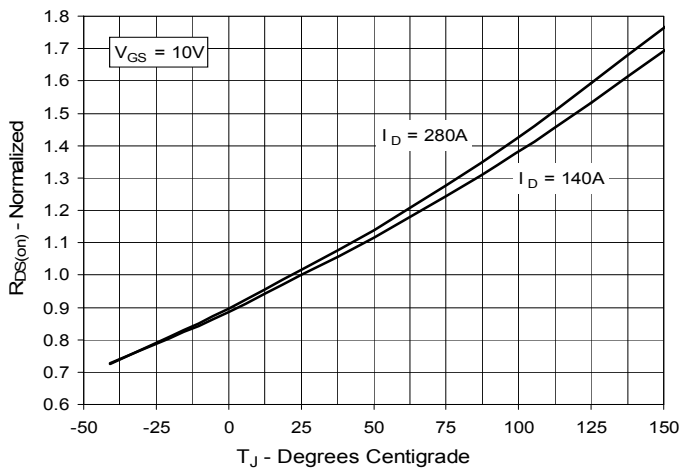


Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 140A$ Value vs. Drain Current

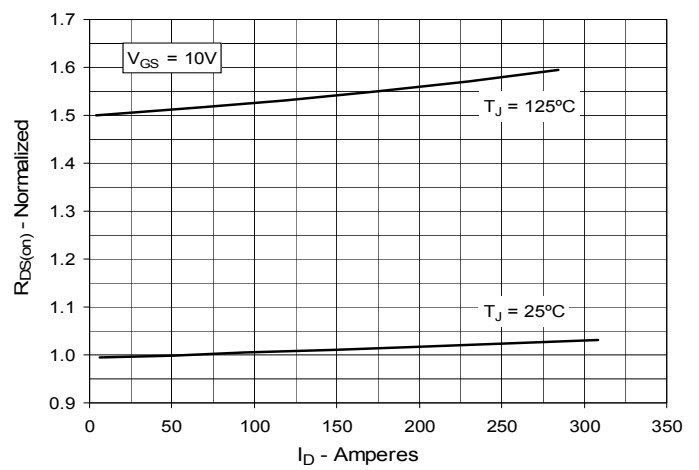


Fig. 5. Maximum Drain Current vs. Case Temperature

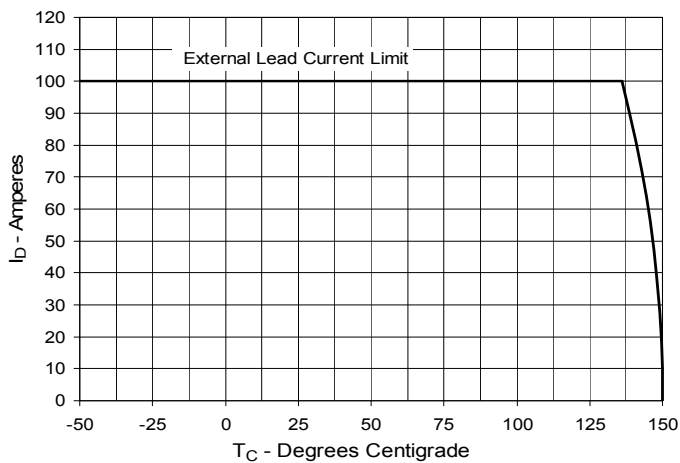


Fig. 6. Forward Voltage Drop of Intrinsic Diode

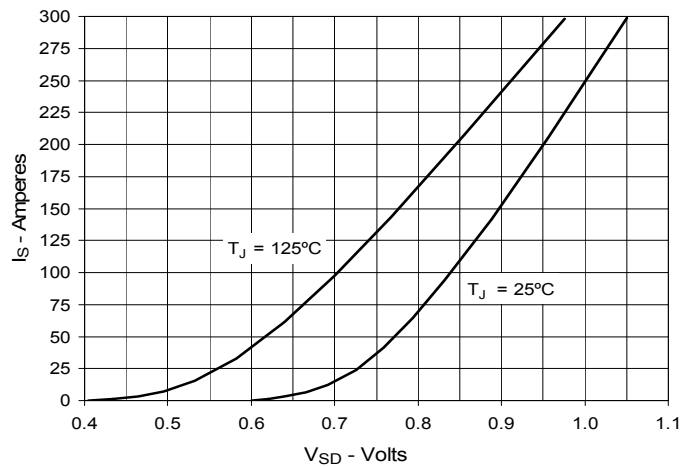
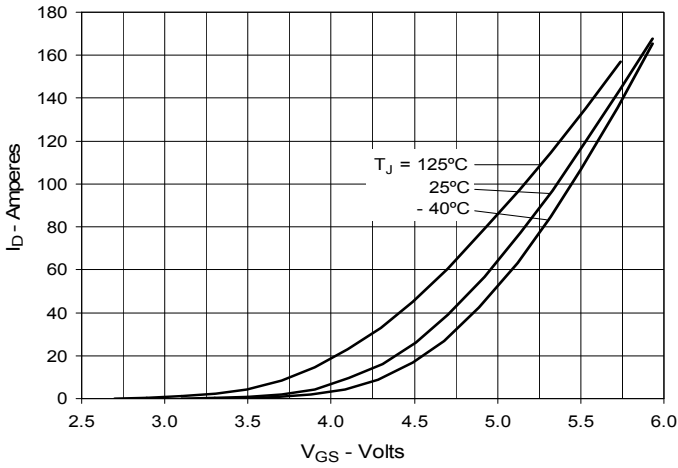
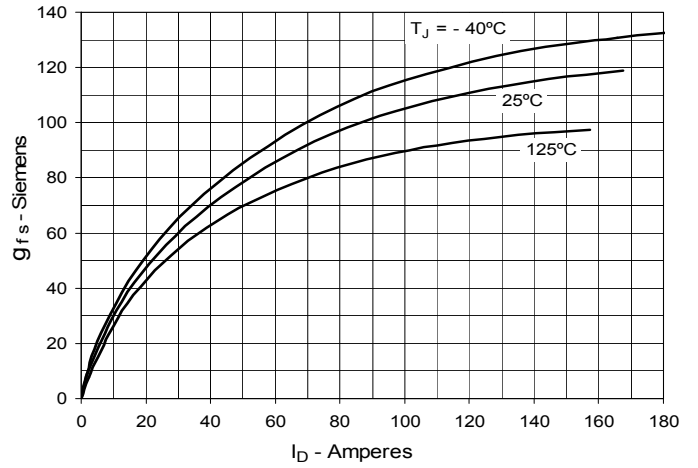
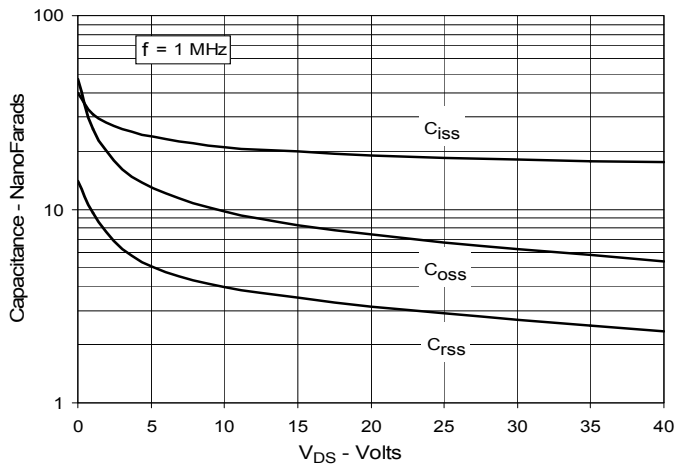
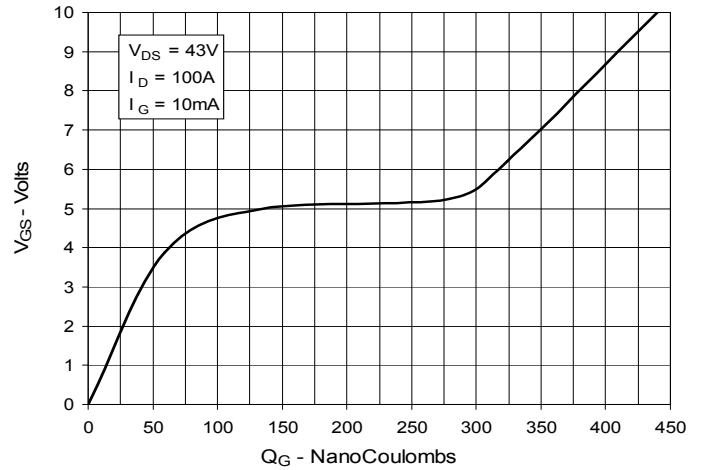
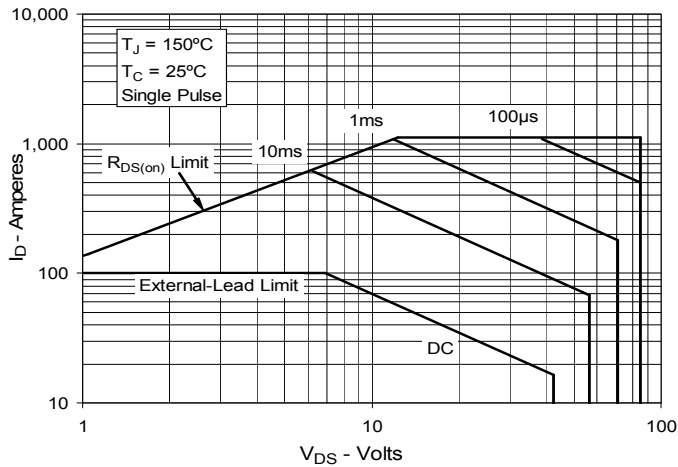


Fig. 7. Input Admittance

Fig. 8. Transconductance

Fig. 9. Capacitance

Fig. 10. Gate Charge

Fig. 11. Forward-Bias Safe Operating Area

Fig. 12. Maximum Transient Thermal Impedance
