

NTD23N03R

Power MOSFET

23 Amps, 25 Volts, N-Channel DPAK

Features

- Pb-Free Packages are Available
- Planar HD3e Process for Fast Switching Performance
- Low $R_{DS(on)}$ to Minimize Conduction Loss
- Low C_{iss} to Minimize Driver Loss
- Low Gate Charge
- Optimized for High Side Switching Requirements in High-Efficiency DC-DC Converters

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	25	Vdc
Gate-to-Source Voltage – Continuous	V_{GS}	± 20	Vdc
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	5.6	$^\circ\text{C/W}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	22.3	W
Drain Current	I_D	23	A
– Continuous @ $T_C = 25^\circ\text{C}$, Chip	I_D	17.1	A
– Continuous @ $T_C = 25^\circ\text{C}$, Limited by Package	I_{DM}	40	A
Thermal Resistance, Junction-to-Ambient (Note 1)	$R_{\theta JA}$	76	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	1.64	W
Drain Current – Continuous @ $T_A = 25^\circ\text{C}$	I_D	4.5	A
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	110	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	1.14	W
Drain Current – Continuous @ $T_A = 25^\circ\text{C}$	I_D	3.8	A
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	260	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. When surface mounted to an FR4 board using 0.5 sq in pad size.
2. When surface mounted to an FR4 board using minimum recommended pad size.

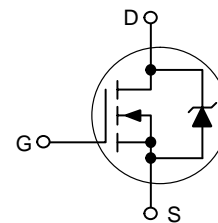


ON Semiconductor®

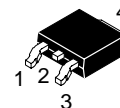
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
25 V	32 m Ω	23 A

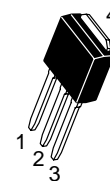
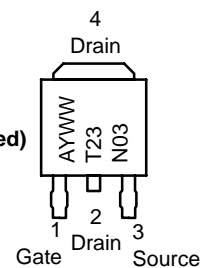
N-CHANNEL



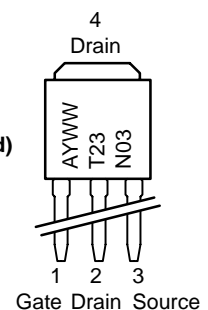
MARKING DIAGRAMS



DPAK CASE 369AA
(Surface Mounted)
STYLE 2



DPAK-3 CASE 369D
(Straight Lead)
STYLE 2



T23N03 = Device Code
A = Assembly Location
Y = Year
WW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

NTD23N03R

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Characteristics	Symbol	Min	Typ	Max	Unit
-----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 3) (V _{GS} = 0 Vdc, I _D = 250 μAdc) Temperature Coefficient (Positive)	V _{(br)DSS}	25 –	28 –	– –	Vdc mV/°C
Zero Gate Voltage Drain Current (V _{DS} = 20 Vdc, V _{GS} = 0 Vdc) (V _{DS} = 20 Vdc, V _{GS} = 0 Vdc, T _J = 150°C)	I _{DSS}	– –	– –	1.0 10	μAdc
Gate-Body Leakage Current (V _{GS} = ±20 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	–	–	±100	nAdc

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (Note 3) (V _{DS} = V _{GS} , I _D = 250 μAdc) Threshold Temperature Coefficient (Negative)	V _{GS(th)}	1.0 –	1.8 –	2.0 –	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 3) (V _{GS} = 4.5 Vdc, I _D = 6 Adc) (V _{GS} = 10 Vdc, I _D = 6 Adc)	R _{DS(on)}	– –	50.3 32.3	60 45	mΩ
Forward Transconductance (Note 3) (V _{DS} = 10 Vdc, I _D = 6 Adc)	g _{FS}	–	13	–	Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 20 Vdc, V _{GS} = 0 V, f = 1 MHz)	C _{iss}	–	225	–	pF
Output Capacitance		C _{oss}	–	108	–	
Transfer Capacitance		C _{rss}	–	48	–	

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	(V _{GS} = 10 Vdc, V _{DD} = 10 Vdc, I _D = 6 Adc, R _G = 3 Ω)	t _{d(on)}	–	2.0	–	ns
Rise Time		t _r	–	14.9	–	
Turn-Off Delay Time		t _{d(off)}	–	9.9	–	
Fall Time		t _f	–	2.0	–	
Gate Charge	(V _{GS} = 4.5 Vdc, I _D = 6 Adc, V _{DS} = 10 Vdc) (Note 3)	Q _T	–	3.76	–	nC
		Q ₁	–	1.7	–	
		Q ₂	–	1.6	–	

SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I _S = 6 Adc, V _{GS} = 0 Vdc) (Note 3) (I _S = 6 Adc, V _{GS} = 0 Vdc, T _J = 125°C)	V _{SD}	– –	0.87 0.74	1.2 –	Vdc
Reverse Recovery Time	(I _S = 6 Adc, V _{GS} = 0 Vdc, di _S /dt = 100 A/μs) (Note 3)	t _{rr}	–	8.7	–	ns
		t _a	–	5.2	–	
		t _b	–	3.5	–	
Reverse Recovery Stored Charge		Q _{RR}	–	0.003	–	μC

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

NTD23N03R

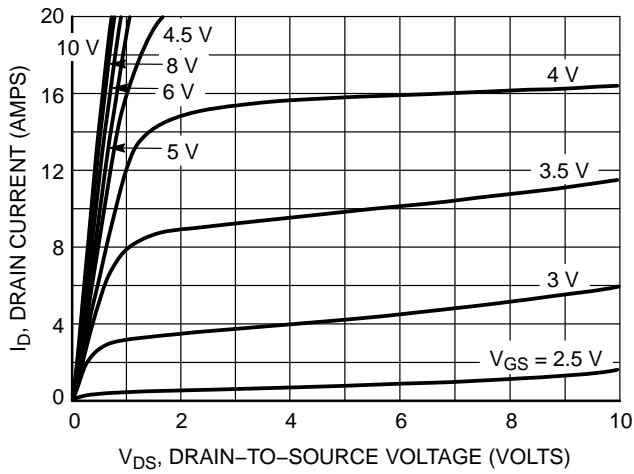


Figure 1. On-Region Characteristics

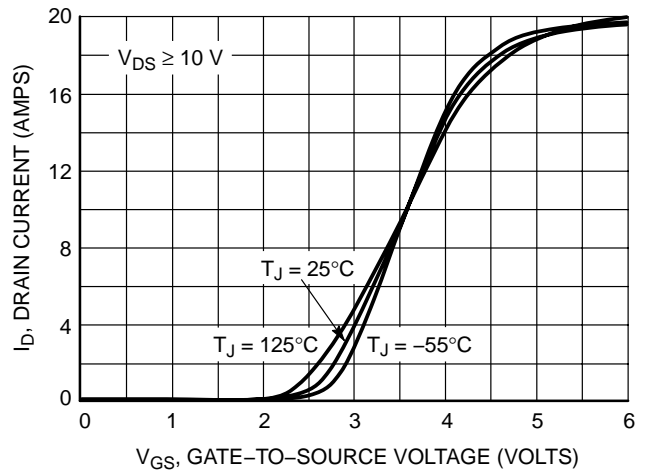


Figure 2. Transfer Characteristics

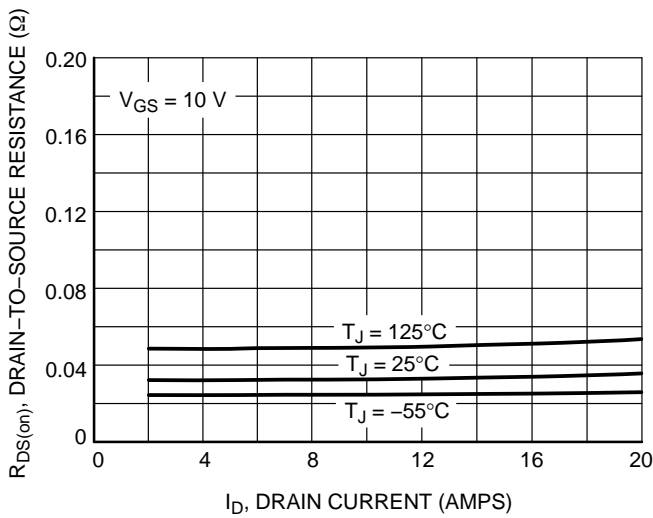


Figure 3. On-Resistance versus Drain Current and Temperature

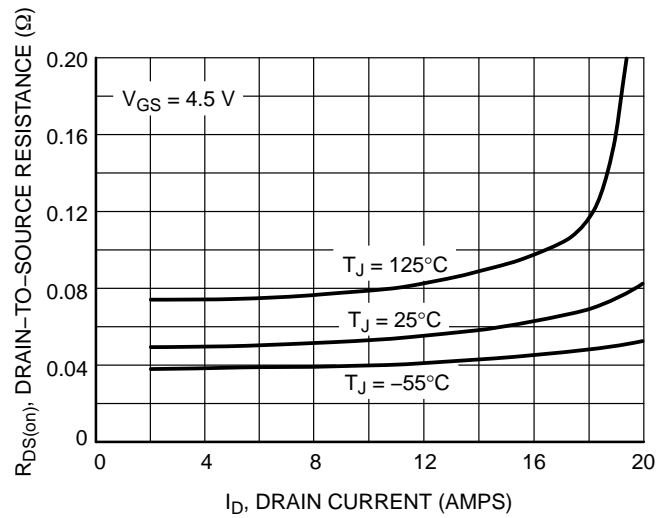


Figure 4. On-Resistance versus Drain Current and Temperature

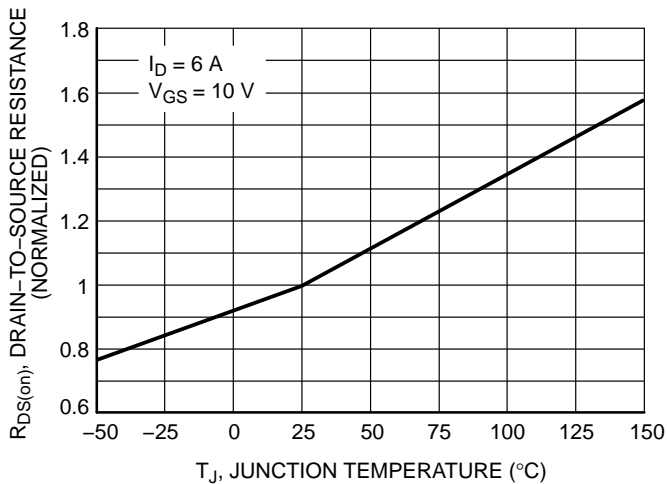


Figure 5. On-Resistance Variation with Temperature

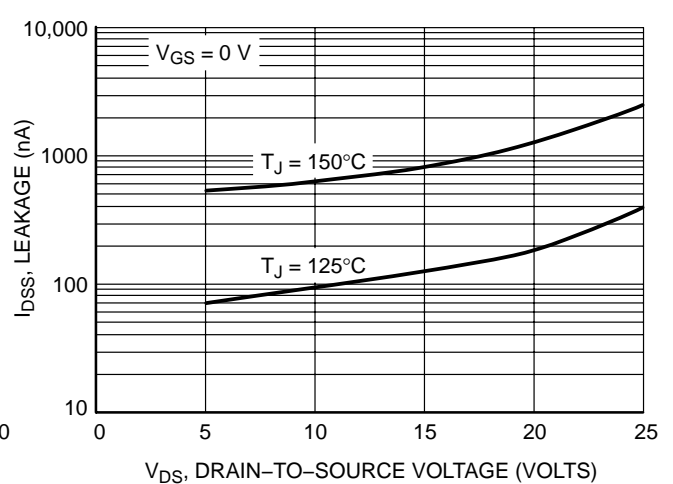


Figure 6. Drain-to-Source Leakage Current versus Voltage

NTD23N03R

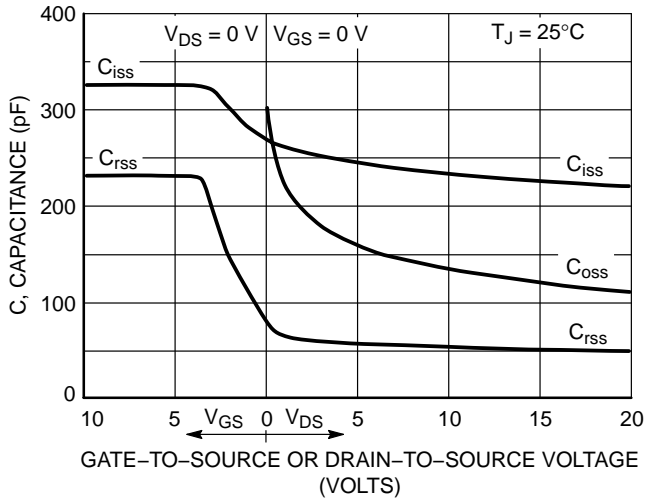


Figure 7. Capacitance Variation

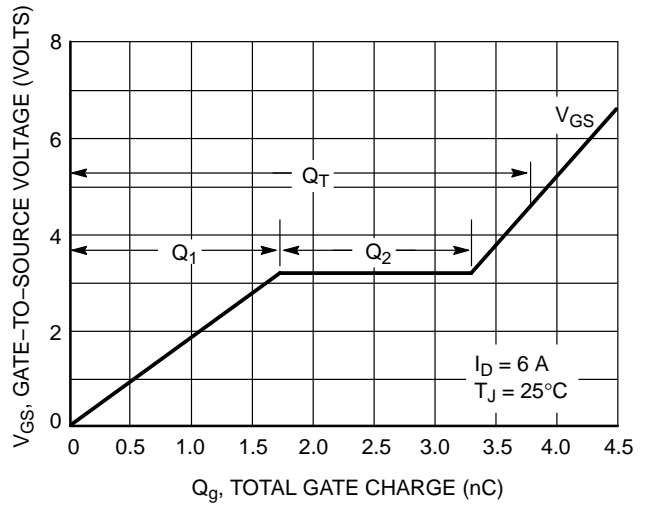


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

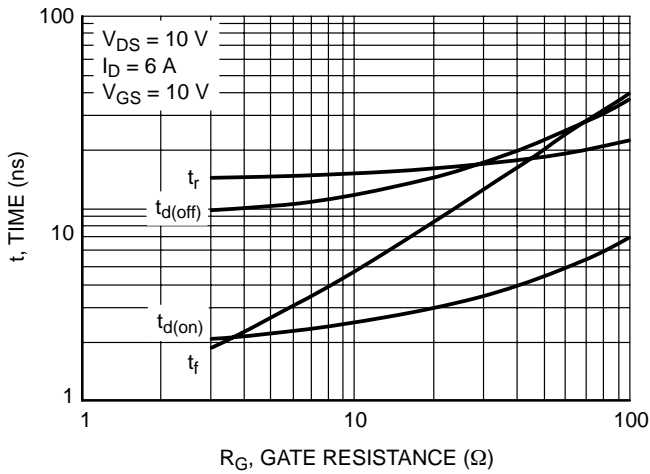


Figure 9. Resistive Switching Time Variation versus Gate Resistance

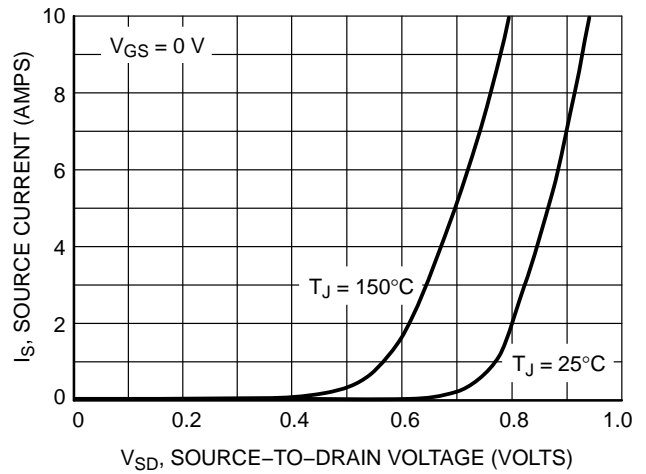


Figure 10. Diode Forward Voltage versus Current

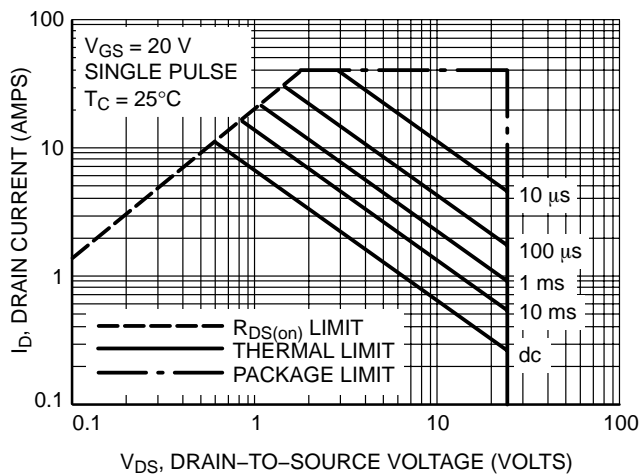


Figure 11. Maximum Rated Forward Biased Safe Operating Area

NTD23N03R

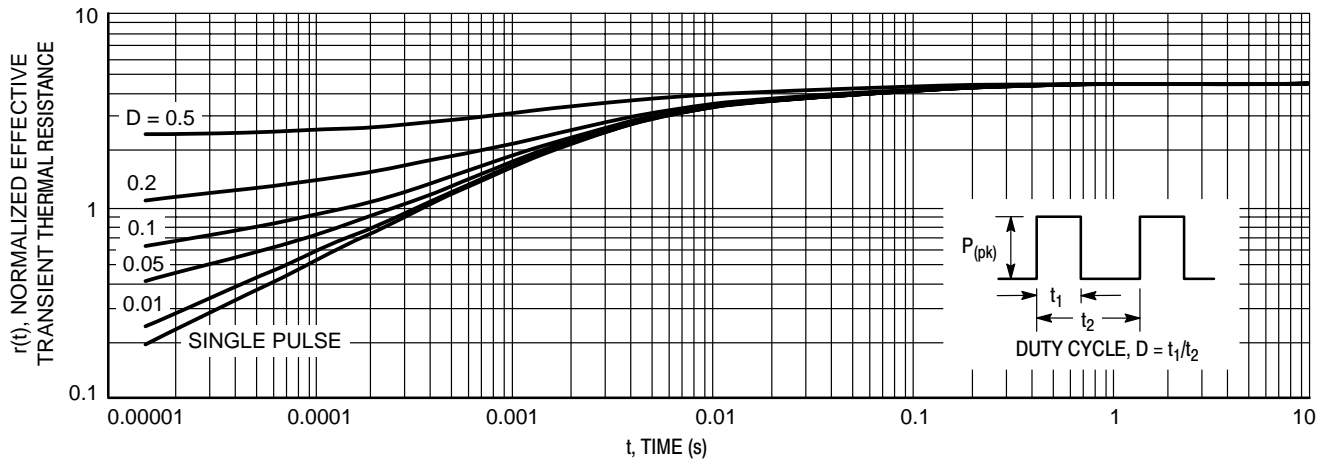


Figure 12. Thermal Response

ORDERING INFORMATION

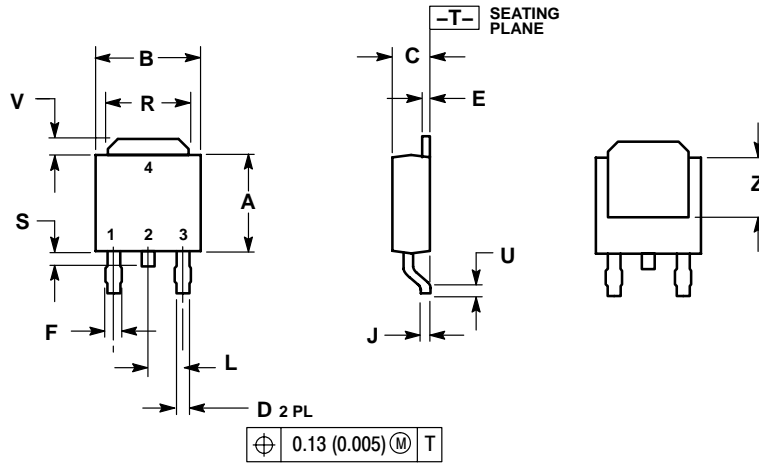
Device	Package	Shipping†
NTD23N03R	DPAK	75 Units/Rail
NTD23N03RG	DPAK (Pb-Free)	75 Units/Rail
NTD23N03R-1	DPAK-3	75 Units/Rail
NTD23N03R-1G	DPAK (Pb-Free)	75 Units/Rail
NTD23N03RT4	DPAK	2500 Tape & Reel
NTD23N03RT4G	DPAK (Pb-Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTD23N03R

PACKAGE DIMENSIONS

DPAK
CASE 369AA-01
ISSUE O

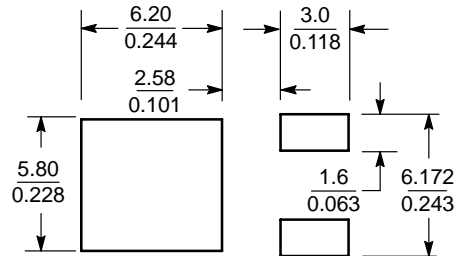


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.025	0.035	0.63	0.88
E	0.018	0.024	0.46	0.61
F	0.033	0.045	0.83	1.14
J	0.018	0.023	0.46	0.58
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

- STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

SOLDERING FOOTPRINT*



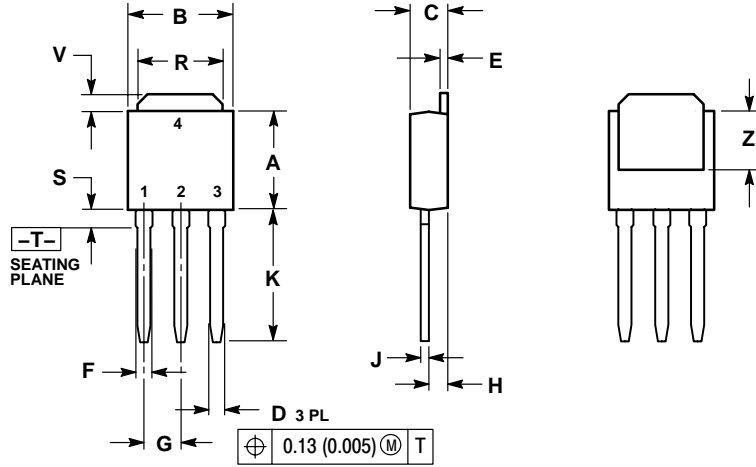
SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NTD23N03R

PACKAGE DIMENSIONS

DPAK-3
CASE 369D-01
ISSUE B



NOTES:


1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 2:

- PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NTD23N03R

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA

Phone: 480-829-7710 or 800-344-3860 Toll Free USA/Canada

Fax: 480-829-7709 or 800-344-3867 Toll Free USA/Canada

Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

Order Literature: <http://www.onsemi.com/litorder>

For additional information, please contact your
local Sales Representative.