PSMN102-200Y

N-channel TrenchMOS standard level FET

Rev. 01 — 29 April 2008 Product data sheet

1. Product profile

1.1 General description

N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology.

1.2 Features

- Low body Q_r
- Fast switching

1.3 Applications

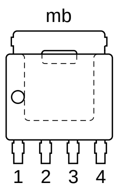
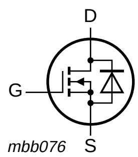
- Industrial DC motor control
- DC-to-DC converters
- Class D audio
- Switched-mode power supplies

1.4 Quick reference data

- $V_{DS} \leq 200$ V
- $R_{DSon} \leq 102$ mΩ
- $I_D \leq 21.5$ A
- $Q_{GD} = 10.1$ nC (typ)

2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Symbol
1, 2, 3	source (S)	 SOT669 (LFPAK)	
4	gate (G)		
mb	mounting base; connected to drain (D)		

3. Ordering information

Table 2. Ordering information

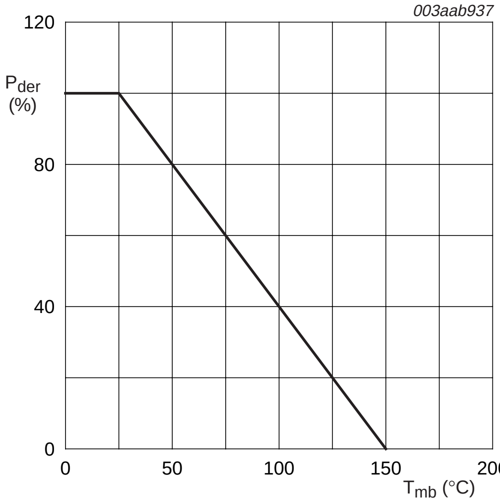
Type number	Package		
	Name	Description	Version
PSMN102-200Y	LFPAK	plastic single-ended surface-mounted package; 4 leads	SOT669

4. Limiting values

Table 3. Limiting values

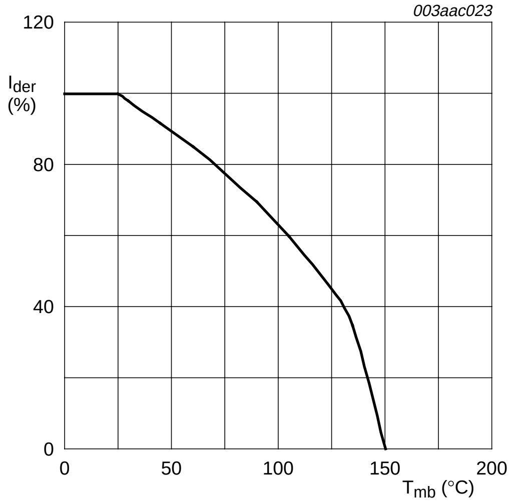
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 150 °C	-	200	V
V_{DGR}	drain-gate voltage	25 °C ≤ T_j ≤ 150 °C; R_{GS} = 20 kΩ	-	200	V
V_{GS}	gate-source voltage		-	±20	V
I_D	drain current	T_{mb} = 25 °C; V_{GS} = 10 V; see Figure 2 and 3	-	21.5	A
		T_{mb} = 100 °C; V_{GS} = 10 V; see Figure 2	-	13.6	A
I_{DM}	peak drain current	T_{mb} = 25 °C; pulsed; t_p ≤ 10 µs; see Figure 3	-	65	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; see Figure 1	-	113	W
T_{stg}	storage temperature		–55	+150	°C
T_j	junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current	T_{mb} = 25 °C	-	52	A
I_{SM}	peak source current	T_{mb} = 25 °C; pulsed; t_p ≤ 10 µs	-	208	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; I_D = 10.8 A; t_p = 0.14 ms; V_{DS} ≤ 200 V; R_{GS} = 50 Ω; V_{GS} = 10 V; starting at T_j = 25 °C	-	202	mJ



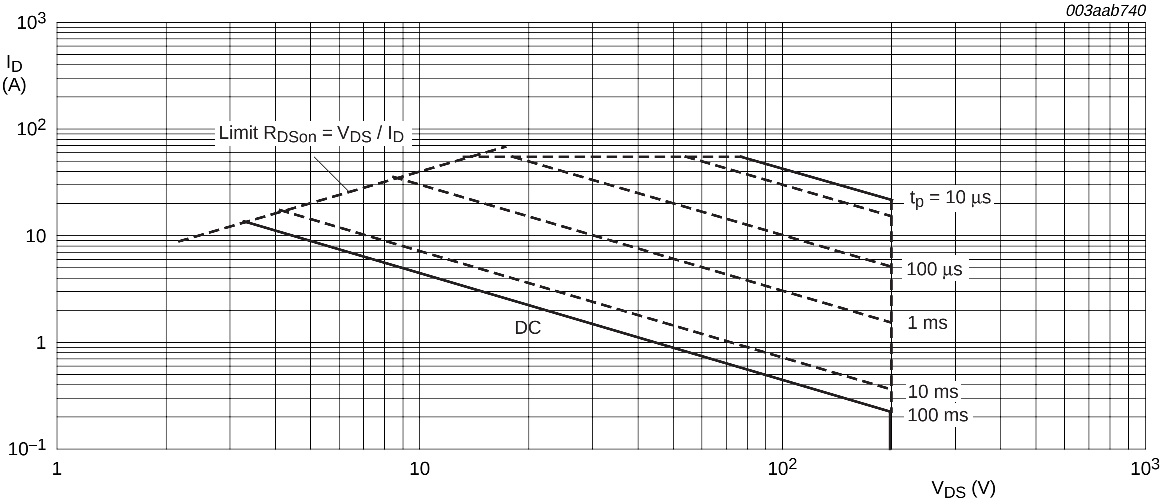
$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\ \%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature



$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\ \%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	[1]	-	-	1.1	K/W

[1] Mounted on a printed-circuit board; vertical in still air.

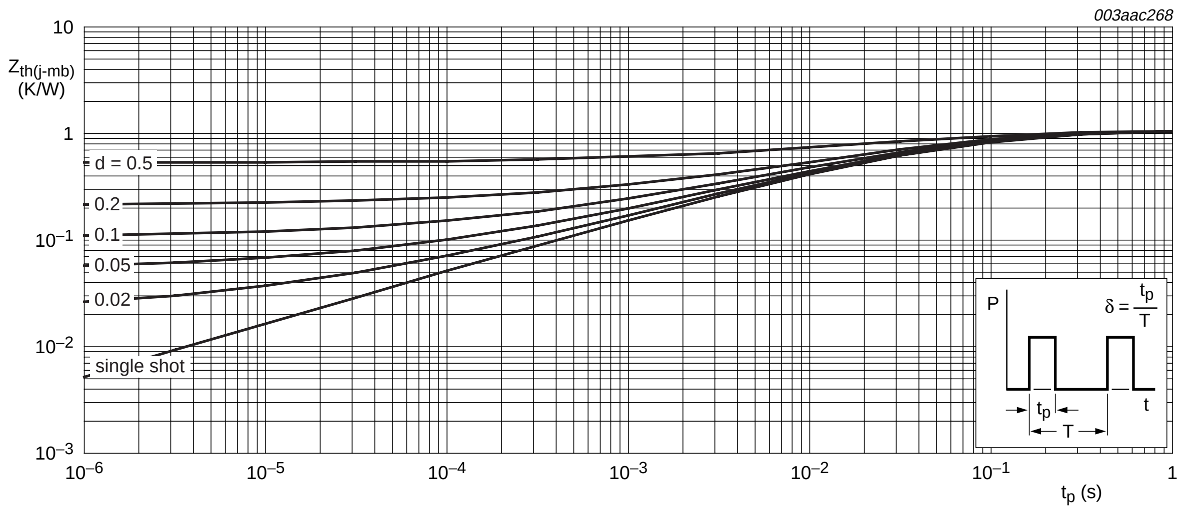


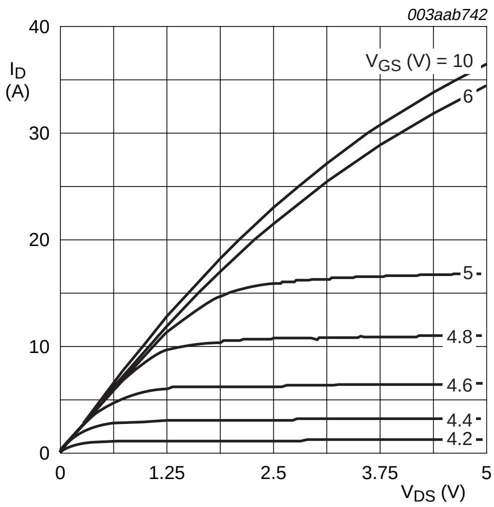
Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 5. Characteristics

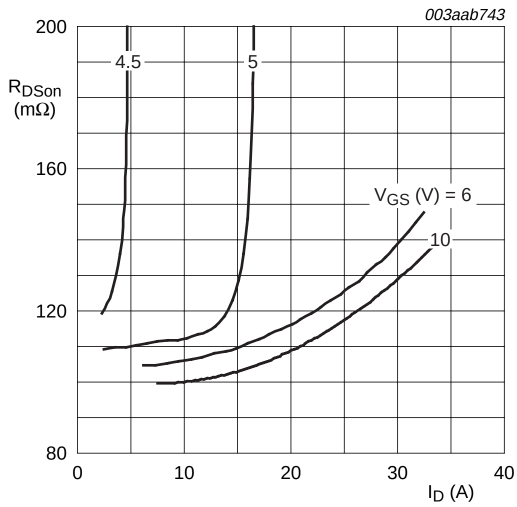
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V					
			T_j = 25 °C	200	-	-	V
			T_j = –55 °C	178	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; see Figure 9 and 10					
			T_j = 25 °C	2	3	4	V
			T_j = 150 °C	1	-	-	V
			T_j = –55 °C	-	-	4.4	V
I_{DSS}	drain leakage current	V_{DS} = 160 V; V_{GS} = 0 V					
			T_j = 25 °C	-	-	1	µA
			T_j = 150 °C	-	-	100	µA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0 V		-	-	100	nA
R_G	gate resistance	f = 1 MHz		-	1.1	-	Ω
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 12 A; see Figure 6 and 8					
			T_j = 25 °C	-	86	102	mΩ
			T_j = 150 °C	-	206	245	mΩ
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 12 A; V_{DS} = 100 V; V_{GS} = 10 V; see Figure 11 and 12		-	30.7	-	nC
Q_{GS}	gate-source charge			-	6.3	-	nC
Q_{GD}	gate-drain charge			-	10.1	-	nC
$V_{GS(pl)}$	gate-source plateau voltage			-	4.6	-	V
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 30 V; f = 1 MHz; see Figure 14		-	1568	-	pF
C_{oss}	output capacitance			-	170	-	pF
C_{rss}	reverse transfer capacitance			-	55	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 100 V; R_L = 5.8 Ω; V_{GS} = 10 V; R_G = 5.6 Ω		-	14.2	-	ns
t_r	rise time			-	29.5	-	ns
$t_{d(off)}$	turn-off delay time			-	33	-	ns
t_f	fall time			-	28	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 12 A; V_{GS} = 0 V; see Figure 13		-	0.9	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = –100 A/µs; V_{GS} = 0 V		-	143	-	ns
Q_r	recovered charge			-	268	-	nC



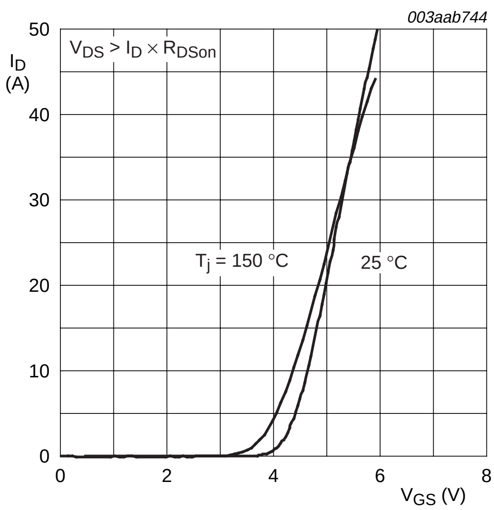
$T_j = 25\ °C$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



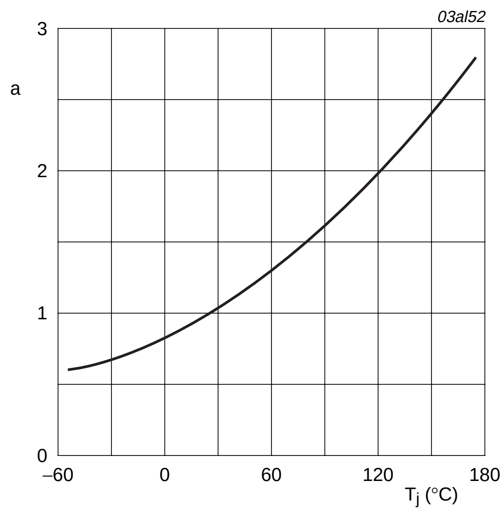
$T_j = 25\ °C$

Fig 6. Drain-source on-state resistance as a function of drain current; typical values



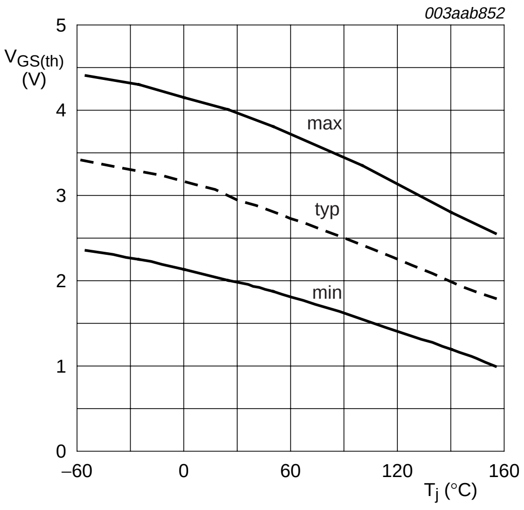
$T_j = 25\ °C$ and $150\ °C$; $V_{DS} > I_D \times R_{DSon}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



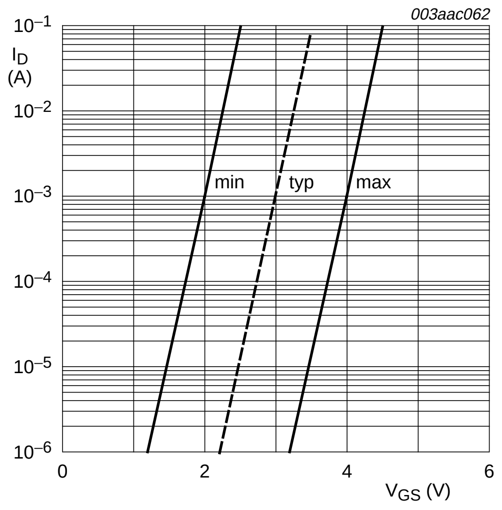
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



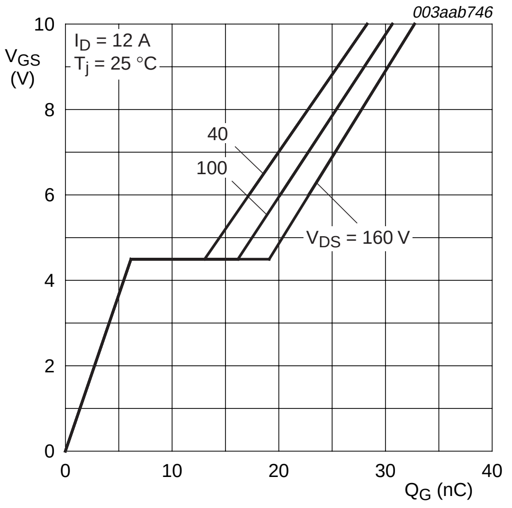
I_D = 1 mA; V_{DS} = V_{GS}

Fig 9. Gate-source threshold voltage as a function of junction temperature



T_j = 25 °C; V_{DS} = 5 V

Fig 10. Sub-threshold drain current as a function of gate-source voltage



I_D = 12 A; V_{DS} = 40, 100 and 160 V

Fig 11. Gate-source voltage as a function of gate charge; typical values

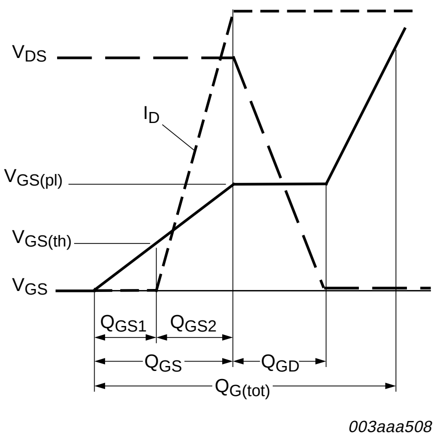
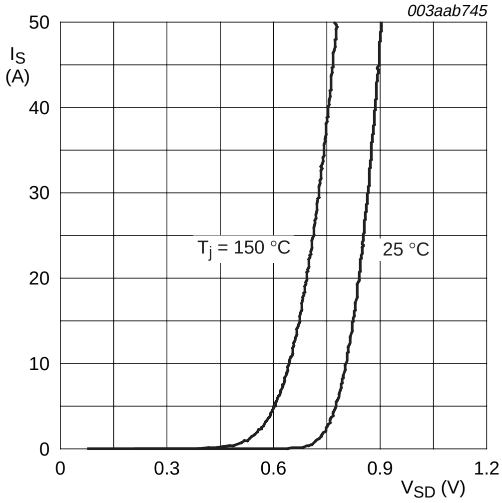
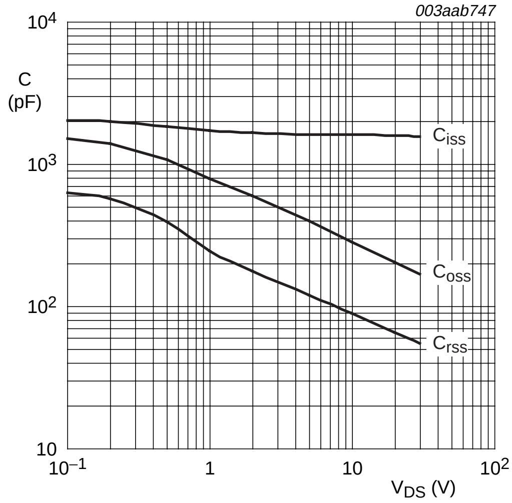


Fig 12. Gate charge waveform definitions



T_j = 25 °C and 150 °C; V_{GS} = 0 V

Fig 13. Source current as a function of source-drain voltage; typical values

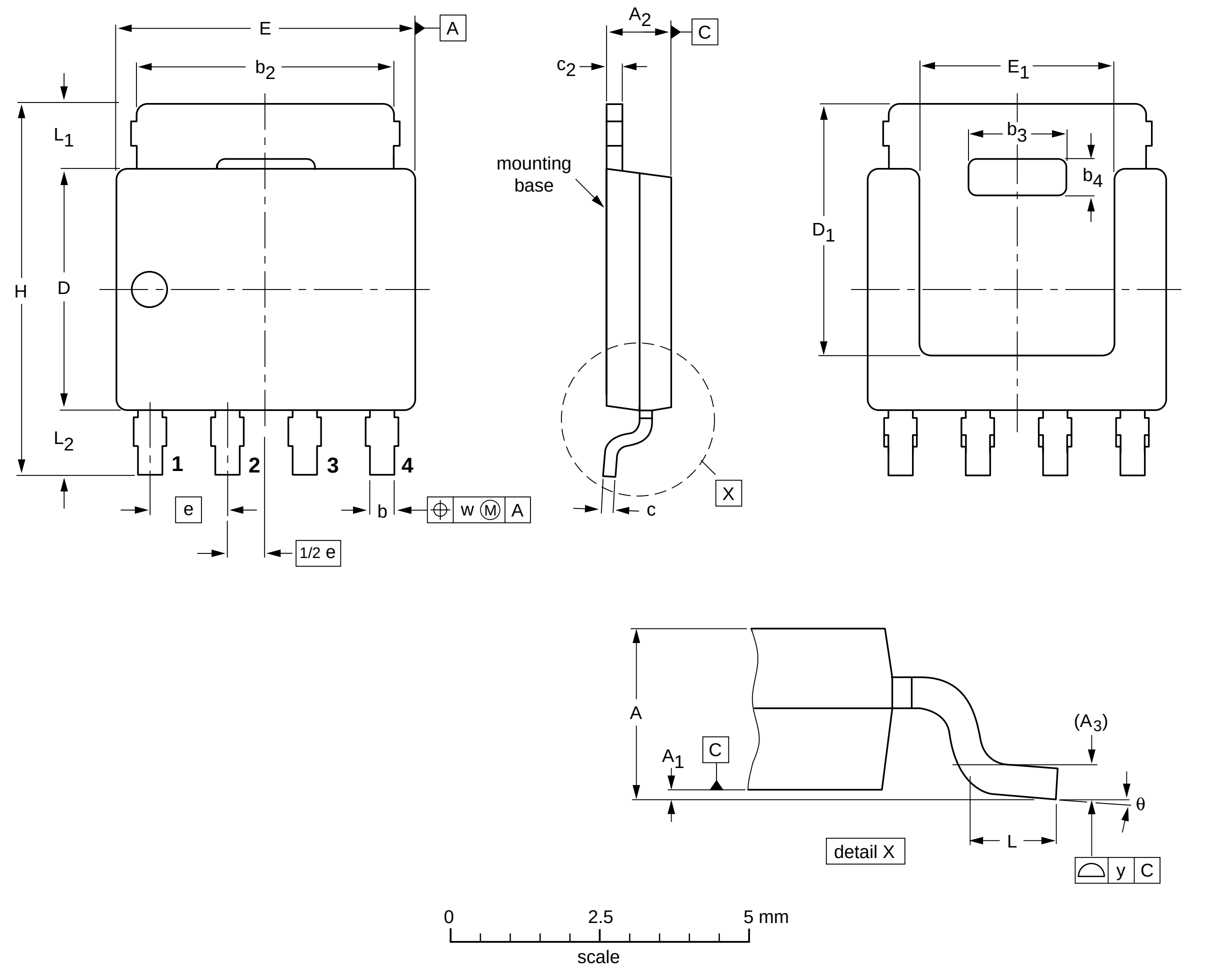


V_{GS} = 0 V; f = 1 MHz

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (LFPAK); 4 leads **SOT669**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	A_2	A_3	b	b_2	b_3	b_4	c	c_2	D(1)	D_1(1) max	E(1)	E_1(1)	e	H	L	L_1	L_2	w	y	θ
mm	1.20 1.01	0.15 0.00	1.10 0.95	0.25	0.50 0.35	4.41 3.62	2.2 2.0	0.9 0.7	0.25 0.19	0.30 0.24	4.10 3.80	4.20	5.0 4.8	3.3 3.1	1.27	6.2 5.8	0.85 0.40	1.3 0.8	1.3 0.8	0.25	0.1	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT669		MO-235				~~04-10-13~~ 06-03-16

Fig 15. Package outline SOT669 (LFPAK)

8. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN102-200Y_1	20080429	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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11. Contents

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