



N-Channel 30-V (D-S) MOSFET



RoHS COMPLIANT

PRODUCT SUMMARY			
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ)
30	0.015 at $V_{GS} = 10$ V	12	16 nC
	0.0175 at $V_{GS} = 4.5$ V	12	

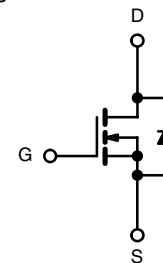
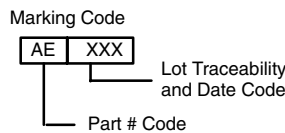
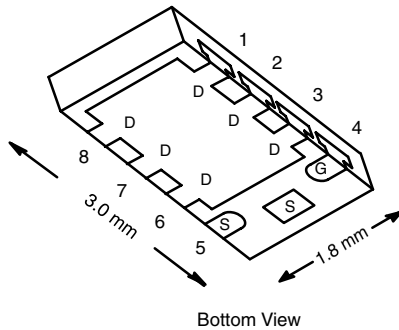
FEATURES

- TrenchFET® Power MOSFET
- New Thermally Enhanced PowerPAK® ChipFET® Package
 - Small Footprint Area
 - Low On-Resistance
 - Thin 0.8-mm Profile

APPLICATIONS

- Load Switch, PA Switch, and Battery Switch for Portable Applications

PowerPAK® ChipFET® Single



N-Channel MOSFET

Ordering Information: Si5482DU-T1—E3 (Lead (Pb)-free)

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 12	
Continuous Drain Current ($T_J = 150$ °C)	$T_C = 25$ °C	I_D	12 ^a	A
	$T_C = 70$ °C		12 ^a	
	$T_A = 25$ °C		11.1 ^{b, c}	
	$T_A = 70$ °C		8.8 ^{b, c}	
Pulsed Drain Current		I_{DM}	40	
Continuous Source-Drain Diode Current	$T_C = 25$ °C	I_S	12 ^a	A
	$T_A = 25$ °C		2.6 ^{b, c}	
Maximum Power Dissipation	$T_C = 25$ °C	P_D	31	W
	$T_C = 70$ °C		20	
	$T_A = 25$ °C		3.1 ^{b, c}	
	$T_A = 70$ °C		2 ^{b, c}	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}			260	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	$t \leq 5$ sec	R_{thJA}	34	40	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	3	4	

Notes:

- Package limited.
- Surface Mounted on 1" x 1" FR4 Board.
- $t = 5$ sec.
- See Solder Profile (<http://www.vishay.com/doc?73257>). The PowerPAK ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 90 °C/W.

SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 1 mA	30			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA		24.5		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			-4.3		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	0.6		2	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±12 V			±100	ns
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			1	μA
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C			10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	30			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 7.4 A		0.0125	0.015	Ω
		V _{GS} = 4.5 V, I _D = 6.8 A		0.0145	0.0175	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 7.4 A		35		S
Dynamic^b						
Input Capacitance	C _{iss}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz		1610		pF
Output Capacitance	C _{oss}			210		
Reverse Transfer Capacitance	C _{rss}			120		
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 11.1 A		34	51	nC
		V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 11.1 A		16	24	
Gate-Source Charge	Q _{gs}			3.6		
Gate-Drain Charge	Q _{gd}		3.7			
Gate Resistance	R _g	f = 1 MHz		5.1		Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 1.7 Ω I _D ≅ 8.8 A, V _{GEN} = 4.5 V, R _g = 1 Ω		10	15	ns
Rise Time	t _r			85	130	
Turn-Off Delay Time	t _{d(off)}			30	45	
Fall Time	t _f			10	15	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 1.7 Ω I _D ≅ 8.8 A, V _{GEN} = 10 V, R _g = 1 Ω		5	10	
Rise Time	t _r			10	15	
Turn-Off Delay Time	t _{d(off)}			35	55	
Fall Time	t _f			10	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			12	A
Pulse Diode Forward Current	I _{SM}				40	
Body Diode Voltage	V _{SD}	I _S = 8.8 A, V _{GS} = 0 V		0.8	1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 8.8 A, di/dt = 100 A/μs, T _J = 25 °C		25	50	ns
Body Diode Reverse Recovery Charge	Q _{rr}			18	27	nC
Reverse Recovery Fall Time	t _a			14.5		ns
Reverse Recovery Rise Time	t _b			10.5		

Notes

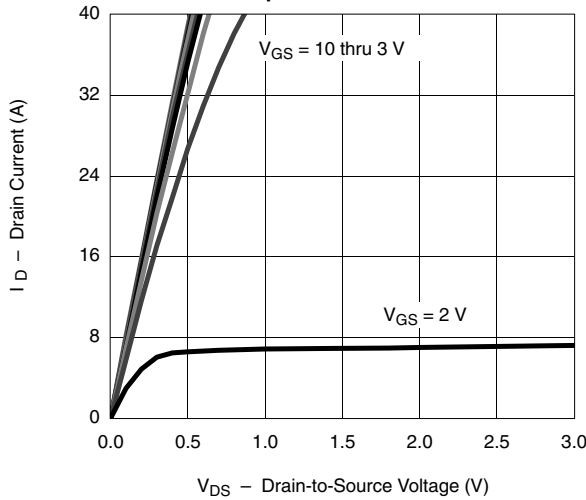
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

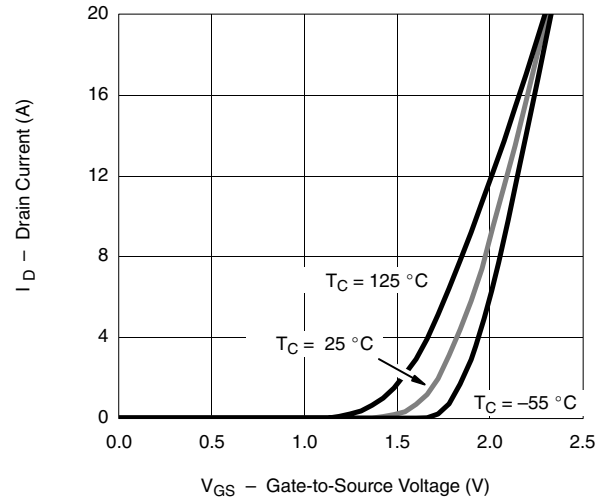


TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

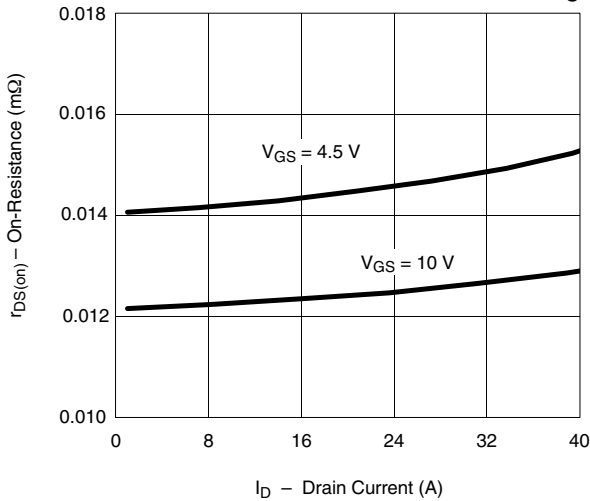
Output Characteristics



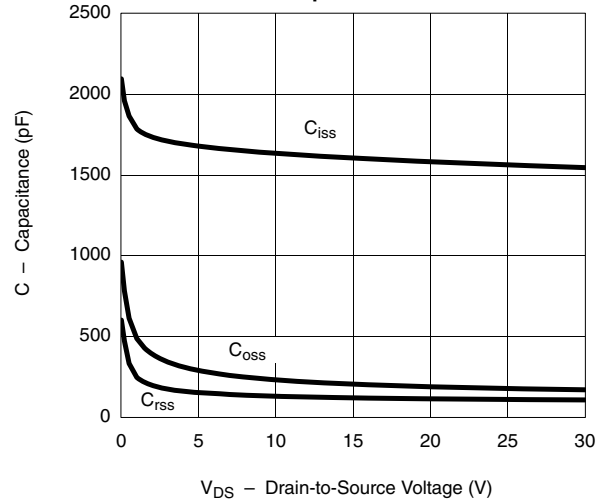
Transfer Characteristics



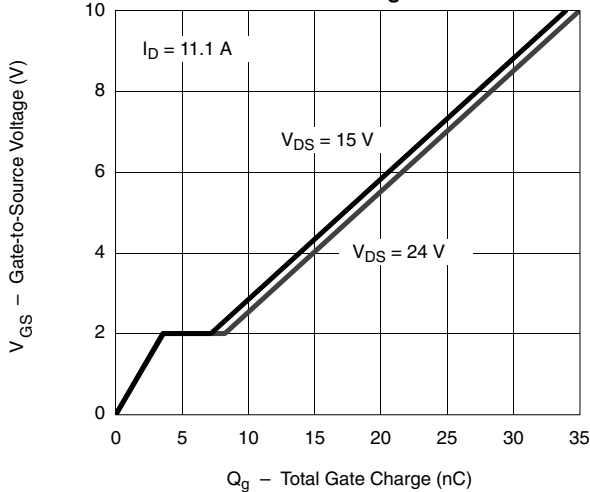
On-Resistance vs. Drain Current and Gate Voltage



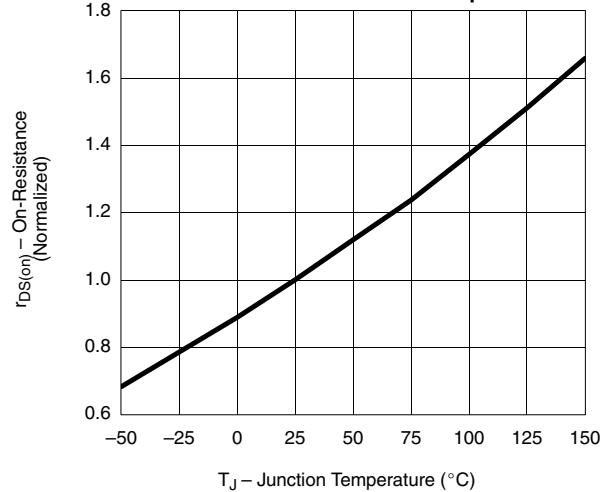
Capacitance



Gate Charge



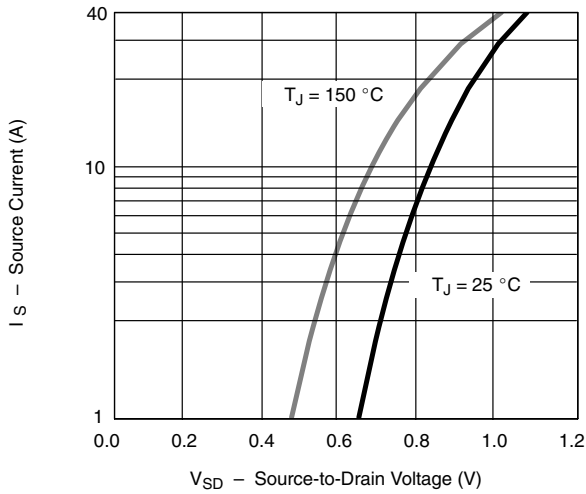
On-Resistance vs. Junction Temperature



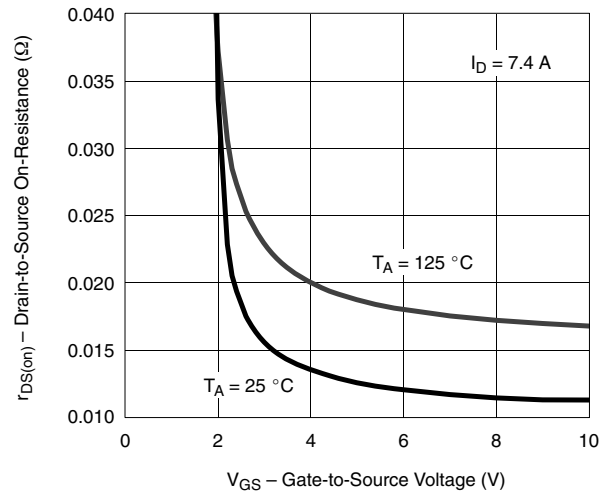


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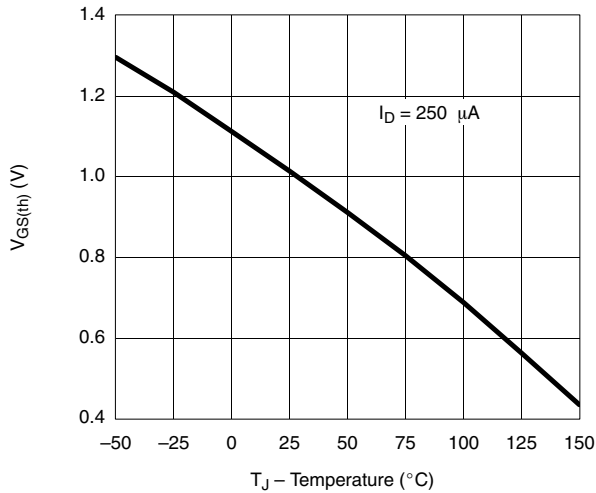
Source-Drain Diode Forward Voltage



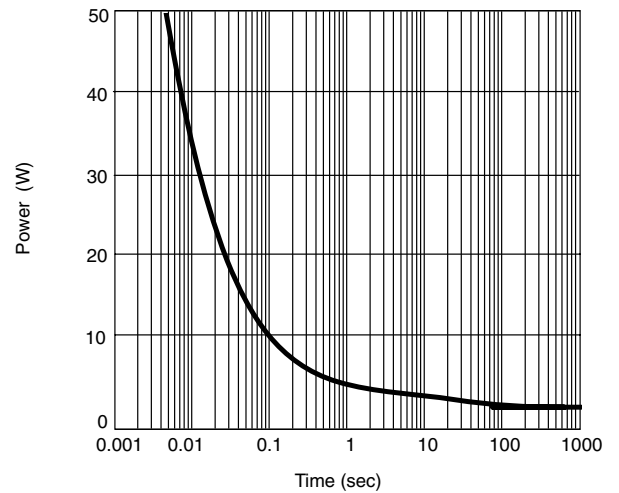
On-Resistance vs. Gate-to-Source Voltage



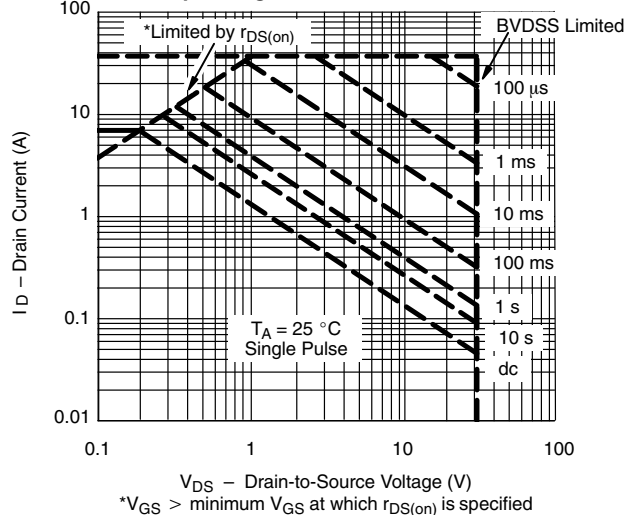
Threshold Voltage



Single Pulse Power, Junction-to-Ambient

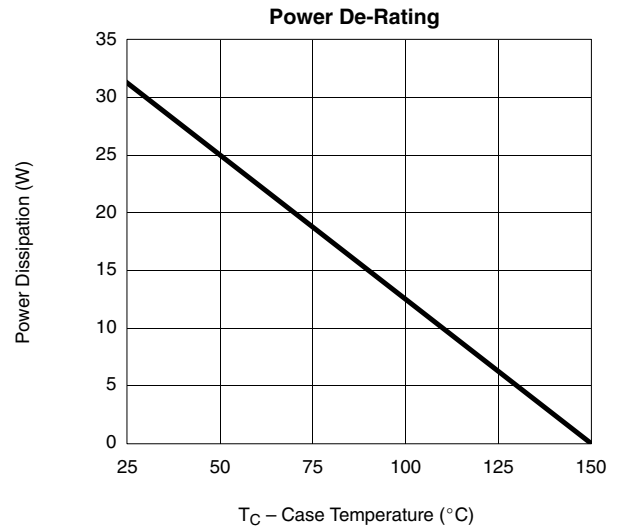
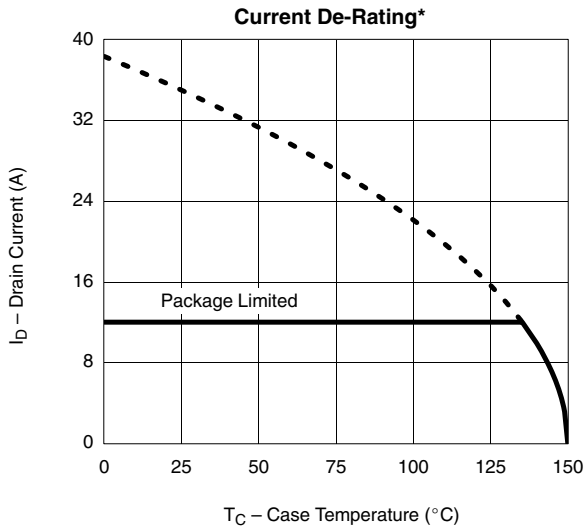


Safe Operating Area, Junction-to-Ambient





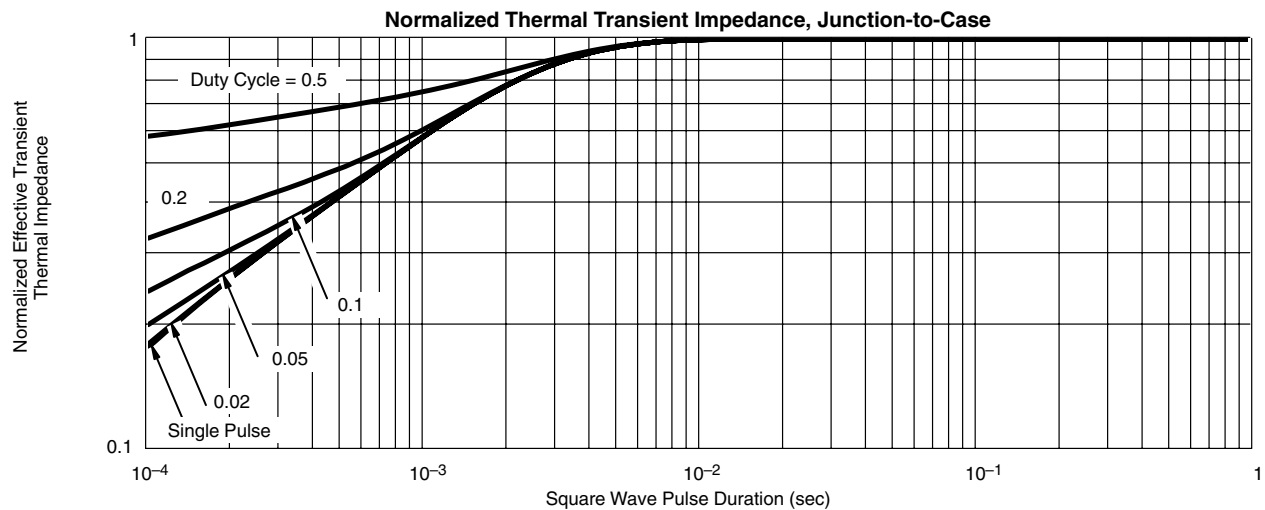
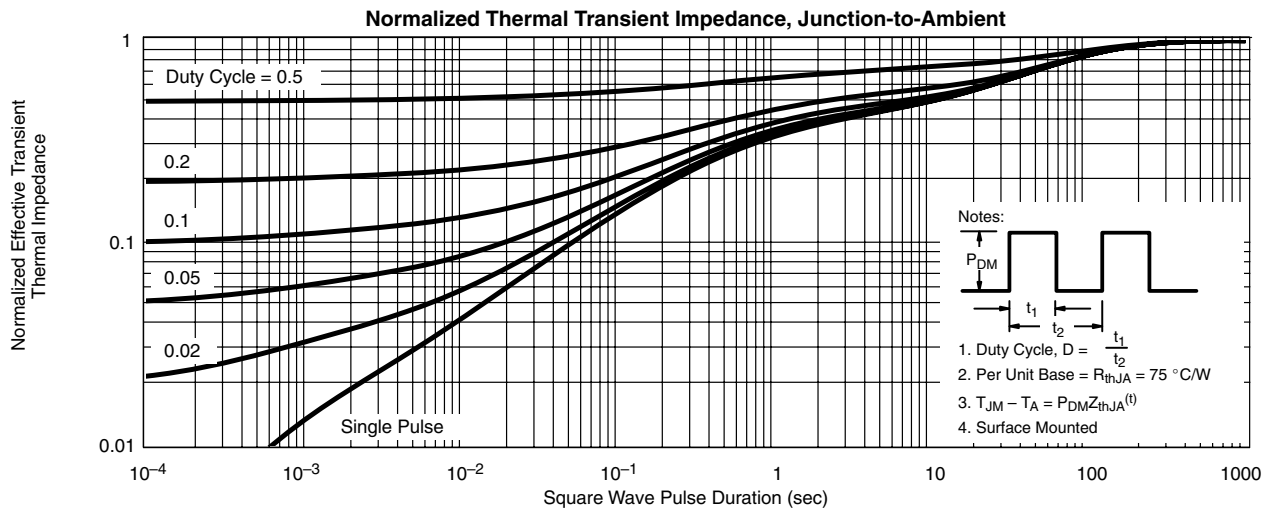
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



*The power dissipation P_D is based on $T_{J(max)} = 150\text{ }^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?73594>.



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