Dual N-Channel 2.5-V (G-S) MOSFET Common Drain, ESD Protection

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.022 at V_{GS} = 4.5 V	6.5
	0.030 at V_{GS} = 2.5 V	5.5

FEATURES

- TrenchFET® Power MOSFET
- ESD Protected: 3000 V

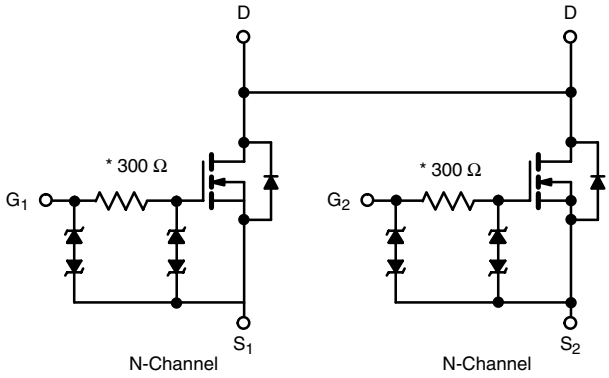
Pb-free Available

RoHS* COMPLIANT

TSSOP-8

Top View

Ordering Information: Si6968BEDQ-T1
Si6968BEDQ-T1-E3 (Lead (Pb)-free)



* Typical value by design

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted					
Parameter		**Symbol**	**10 sec**	**Steady State**	**Unit**
Drain-Source Voltage		V_{DS}	20		V
Gate-Source Voltage		V_{GS}	± 12		
Continuous Drain Current (T_J = 150 °C)[a]	T_A = 25 °C	I_D	6.5	5.2	A
	T_A = 70 °C		5.5	3.5	
Pulsed Drain Current		I_{DM}	30		
Continuous Source Current (Diode Conduction)[a]		I_S	1.5	1.0	
Maximum Power Dissipation[a]	T_A = 25 °C	P_D	1.5	1.0	W
	T_A = 70 °C		0.96	0.64	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typ**	**Max**	**Unit**
Maximum Junction-to-Ambient[a]	t ≤ 10 sec	R_{thJA}	72	83	°C/W
	Steady State		100	120	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	55	70	

Notes:
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

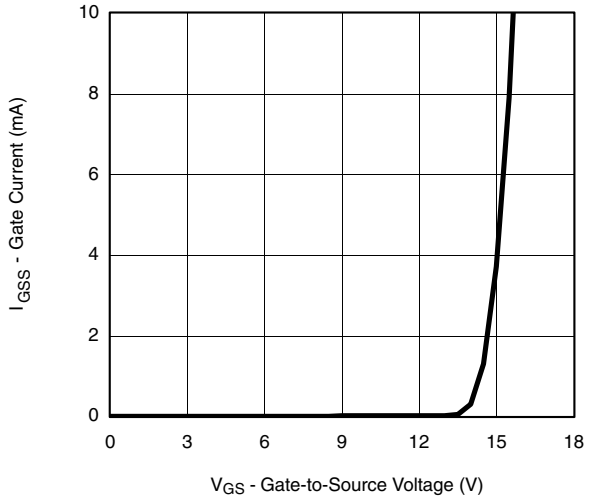
* Pb containing terminations are not RoHS compliant, exemptions may apply.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ[a]**	**Max**	**Unit**
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	0.6		1.6	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 4.5 V			± 200	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V			1	µA
		V_{DS} = 20 V, V_{GS} = 0 V, T_J = 70 °C			25	
On-State Drain Current[b]	$I_{D(on)}$	$V_{DS} \leq$ 5 V, V_{GS} = 4.5 V	30			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 4.5 V, I_D = 6.5 A		0.0165	0.022	Ω
		V_{GS} = 2.5 V, I_D = 5.5 A		0.023	0.030	
Forward Transconductance[b]	g_{fs}	V_{DS} = 10 V, I_D = 6.5 A		30		S
Diode Forward Voltage[b]	V_{SD}	I_S = 1.5 A, V_{GS} = 0 V		0.71	1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 6.5 A		12	18	nC
Gate-Source Charge	Q_{gs}			2.2		
Gate-Drain Charge	Q_{gd}			3.6		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10 V, R_L = 10 Ω $I_D \cong$ 1 A, V_{GEN} = 4.5 V, R_G = 6 Ω		245	365	ns
Rise Time	t_r			330	495	
Turn-Off Delay Time	$t_{d(off)}$			860	1300	
Fall Time	t_f			510	765	

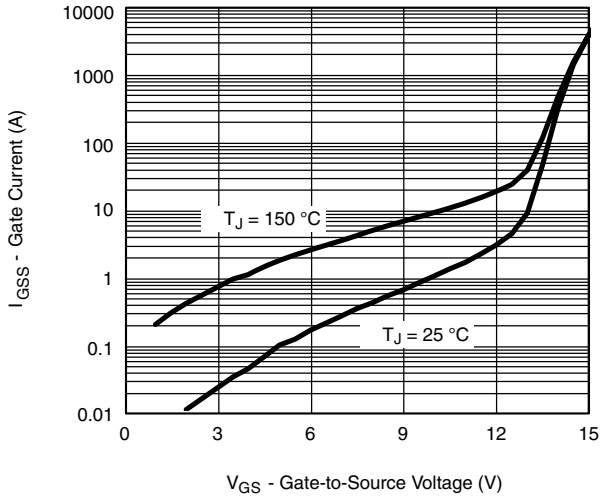
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C unless noted



Gate-Current vs. Gate-Source Voltage



Gate Current vs. Gate-Source Voltage

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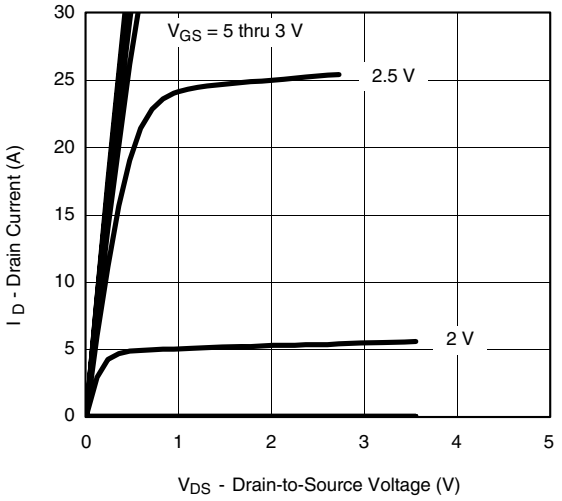
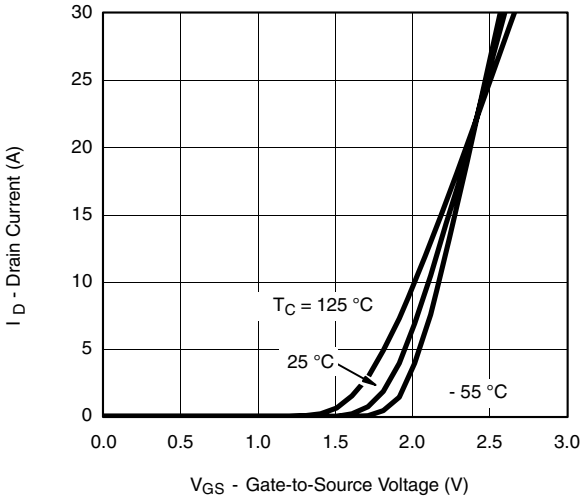
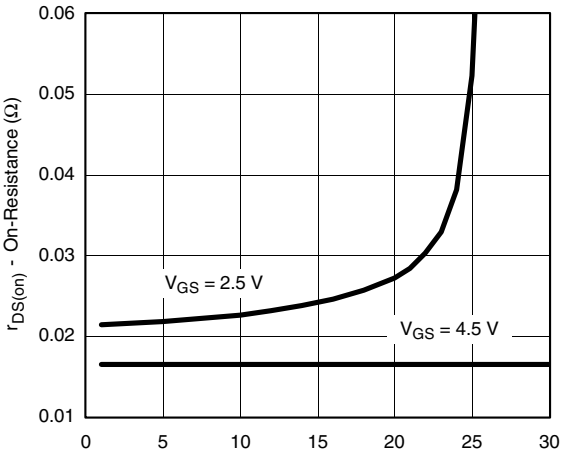


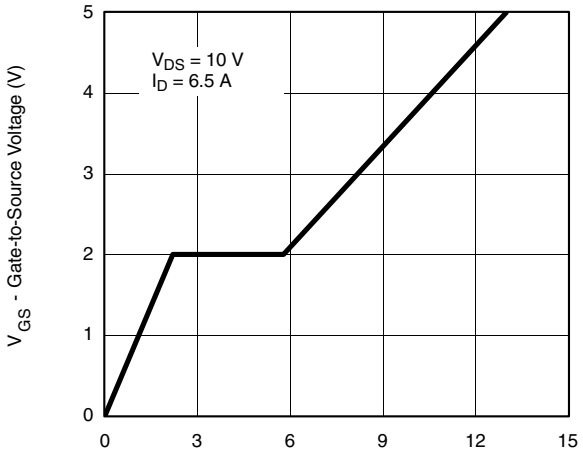
Output Characteristics



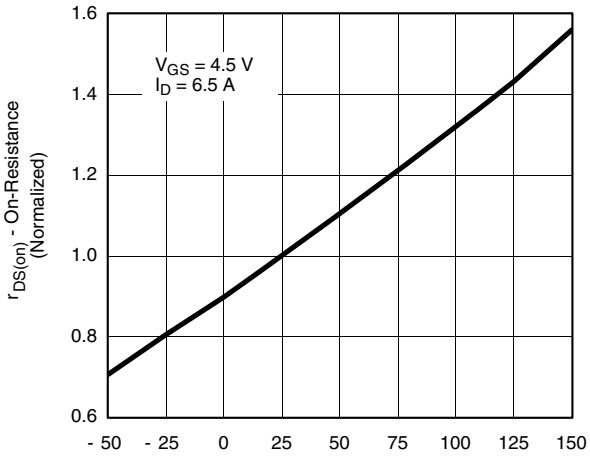
Transfer Characteristics



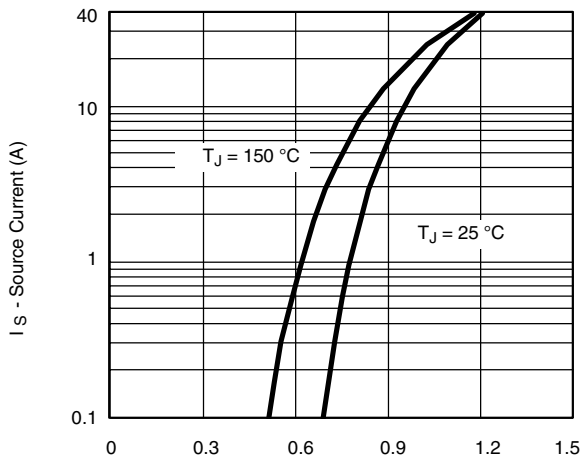
On-Resistance vs. Drain Current



Gate Charge

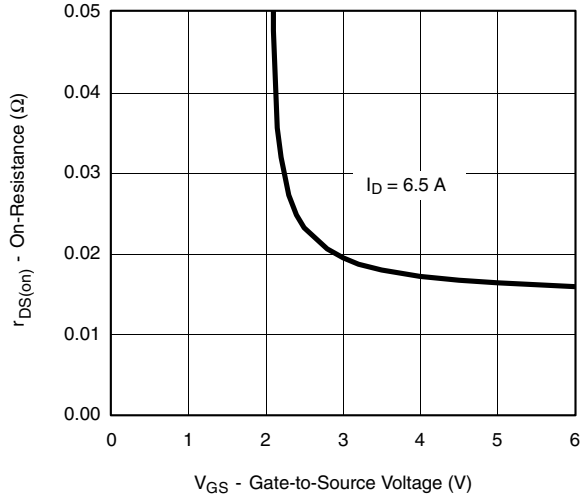


On-Resistance vs. Junction Temperature

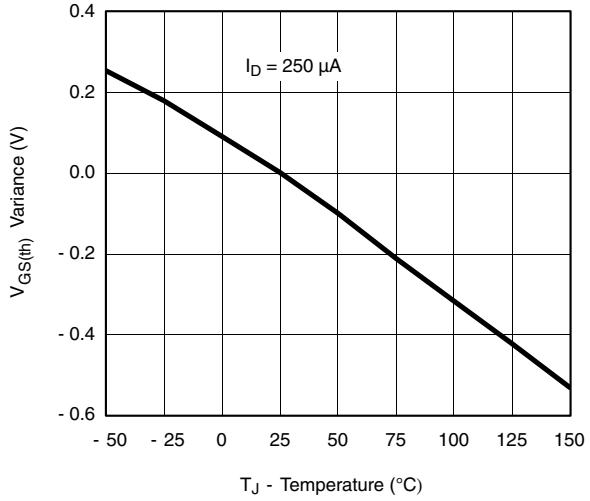


Source-Drain Diode Forward Voltage

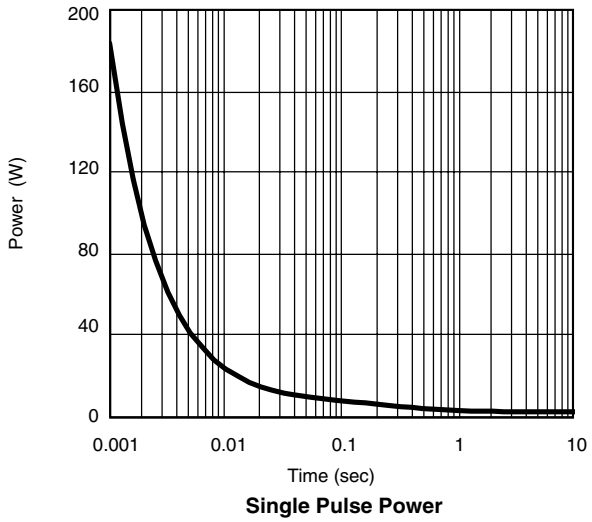
TYPICAL CHARACTERISTICS 25 °C unless noted



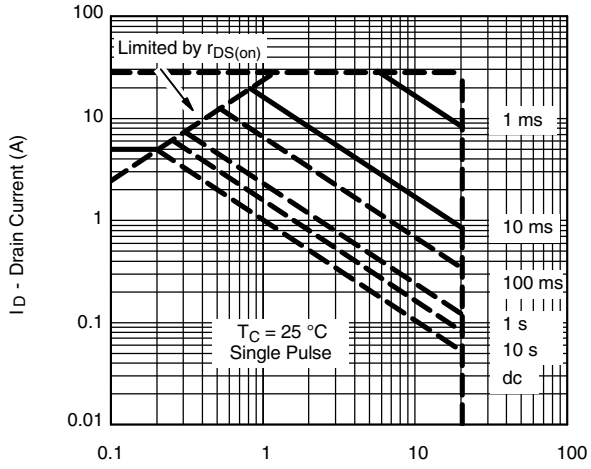
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

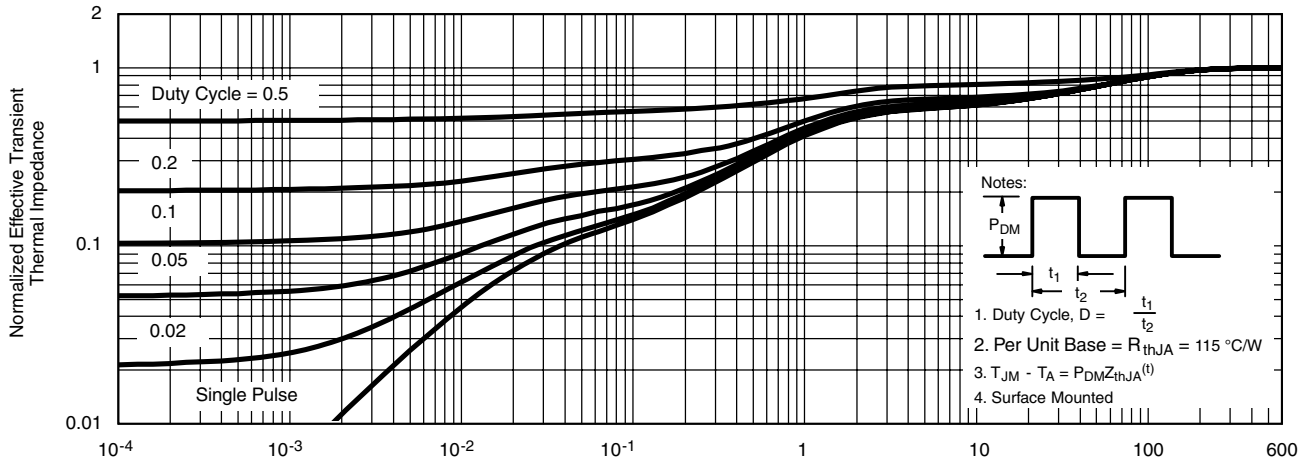


Single Pulse Power



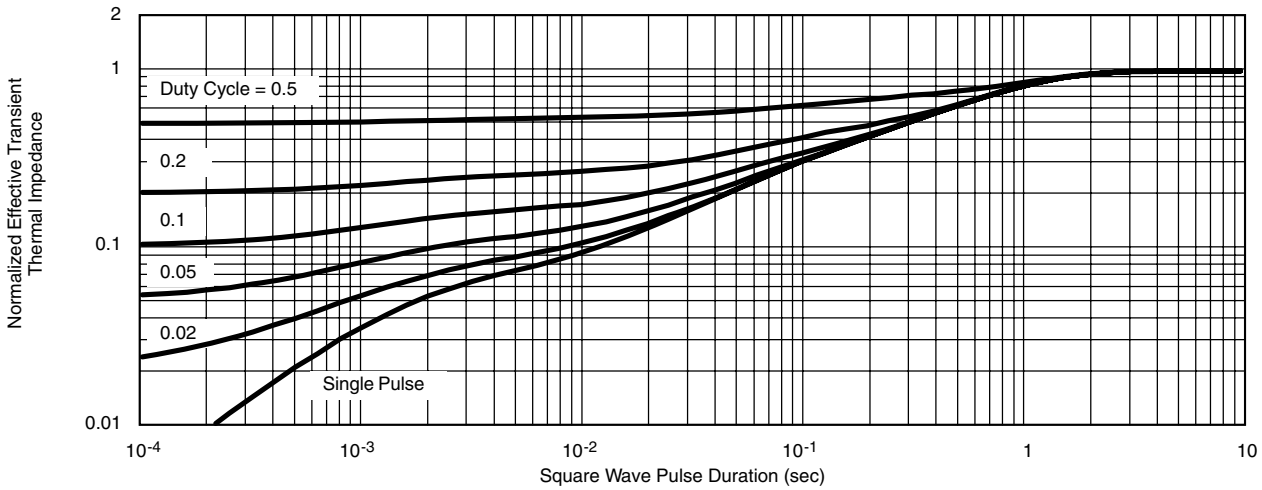
* V_{GS} > minimum V_{GS} at which $r_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Ambient

TYPICAL CHARACTERISTICS 25 °C unless noted



Normalized Thermal Transient Impedance, Junction-to-Foot

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