

Dual N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ)
30	0.025 at $V_{GS} = 10$ V	24	5 nC
	0.033 at $V_{GS} = 4.5$ V	21	

FEATURES

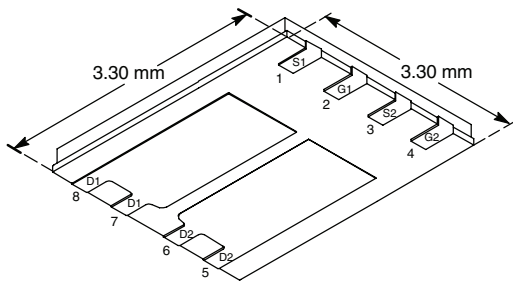
- TrenchFET[®] Power MOSFET

APPLICATIONS

- Synchronous Rectification
- Notebook System Power
- POL

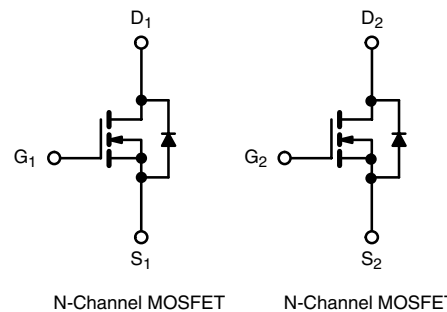


PowerPAK[®] 1212-8



Bottom View

Ordering Information: Si7218DN-T1-E3 (Lead (Pb)-free)



N-Channel MOSFET

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V_{DS}	30	V	
Gate-Source Voltage	V_{GS}	± 20		
Continuous Drain Current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	24	A
		$T_C = 70$ °C	19	
		$T_A = 25$ °C	8 ^{a, b}	
		$T_A = 70$ °C	6.5 ^{a, b}	
Pulsed Drain Current	I_{DM}	35	A	
Continuous Source-Drain Diode Current	I_S	$T_C = 25$ °C		
		$T_A = 25$ °C	2.2 ^{a, b}	
Single Pulse Avalanche Current	I_{AS}	10	mJ	
Single Pulse Avalanche Energy	E_{AS}	5		
Maximum Power Dissipation	P_D	$T_C = 25$ °C	23	W
		$T_C = 70$ °C	14.8	
		$T_A = 25$ °C	2.6 ^{a, b}	
		$T_A = 70$ °C	1.7 ^{a, b}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature) ^{c, d}		260		

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{a, e}	R_{thJA}	38	48	°C/W	
Maximum Junction-to-Case (Drain)	R_{thJC}	4.3	5.4		

Notes:

- Surface Mounted on 1" x 1" FR4 board.
- $t = 10$ s.
- See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 94 °C/W.
- Based on $T_C = 25$ °C.



SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	30			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		35		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-6		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.5		3	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	20			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 8\text{ A}$		0.0205	0.025	Ω
		$V_{GS} = 4.5\text{ V}, I_D = 7\text{ A}$		0.027	0.033	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 8\text{ A}$		20		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		700		pF
Output Capacitance	C_{oss}			110		
Reverse Transfer Capacitance	C_{rss}			50		
Total Gate Charge	Q_g	$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 8\text{ A}$		11	17	nC
		$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 8\text{ A}$		5	7.5	
Gate-Source Charge	Q_{gs}			2.3		
Gate-Drain Charge	Q_{gd}		1.6			
Gate Resistance	R_g	$f = 1\text{ MHz}$		2.3		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 2.3\text{ }\Omega$ $I_D \cong 6.5\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		15	25	ns
Rise Time	t_r			12	20	
Turn-Off Delay Time	$t_{d(off)}$			10	15	
Fall Time	t_f			10	15	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 2.3\text{ }\Omega$ $I_D \cong 6.5\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		10	15	
Rise Time	t_r			10	15	
Turn-Off Delay Time	$t_{d(off)}$			15	25	
Fall Time	t_f			10	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			19	A
Pulse Diode Forward Current	I_{SM}				35	
Body Diode Voltage	V_{SD}	$I_S = 6.5\text{ A}, V_{GS} = 0\text{ V}$		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 6.5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		25	40	ns
Body Diode Reverse Recovery Charge	Q_{rr}			19	30	nC
Reverse Recovery Fall Time	t_a			14		ns
Reverse Recovery Rise Time	t_b			11		

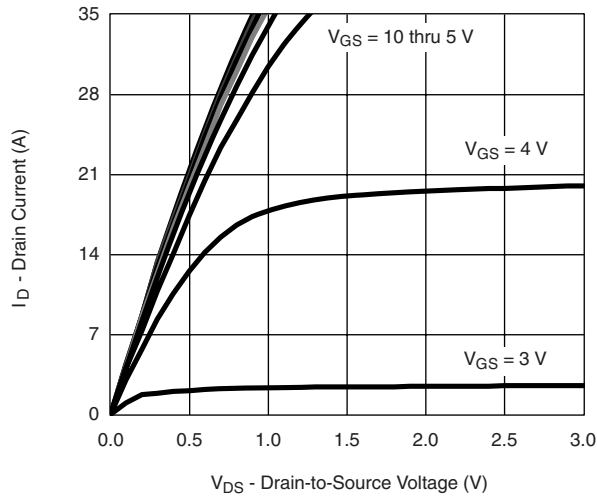
Notes:

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing.

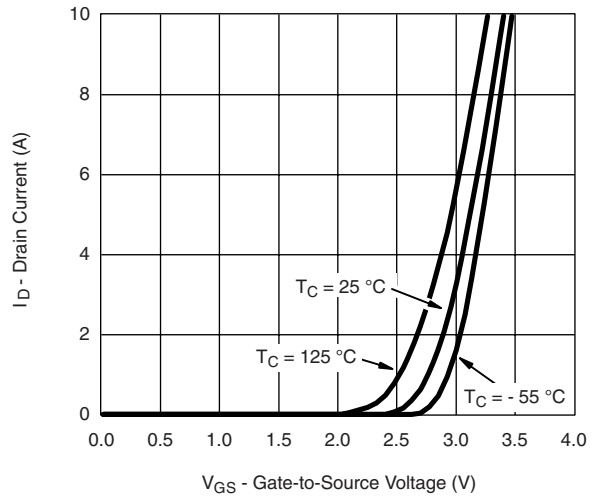
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



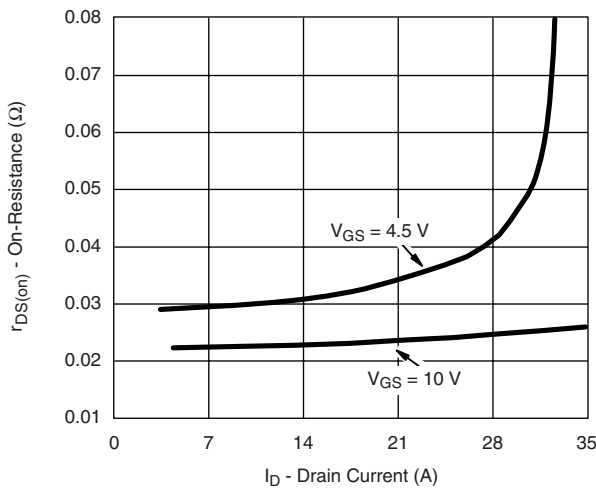
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



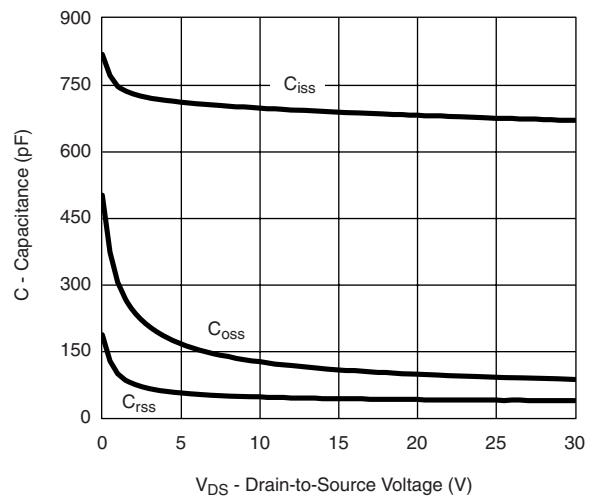
Output Characteristics



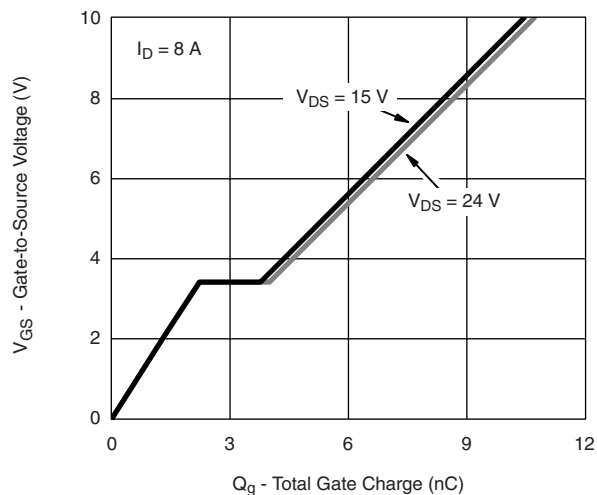
Transfer Characteristics



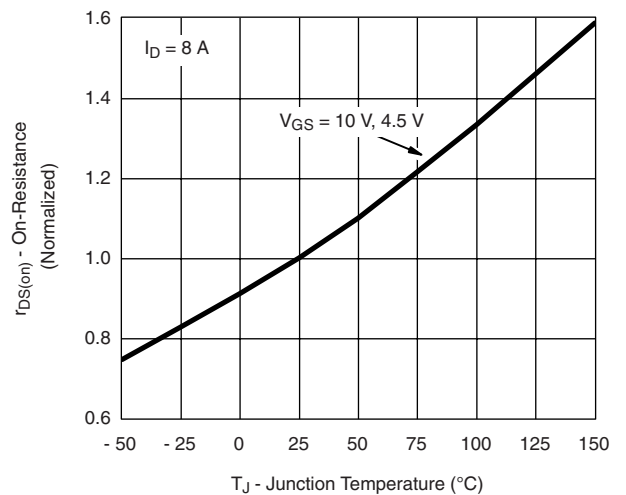
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



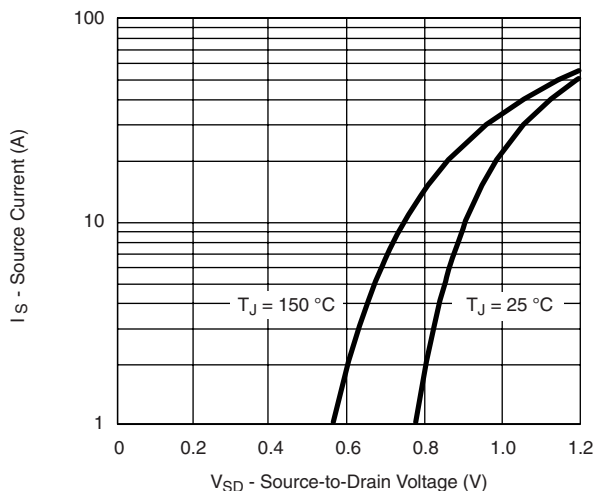
Gate Charge



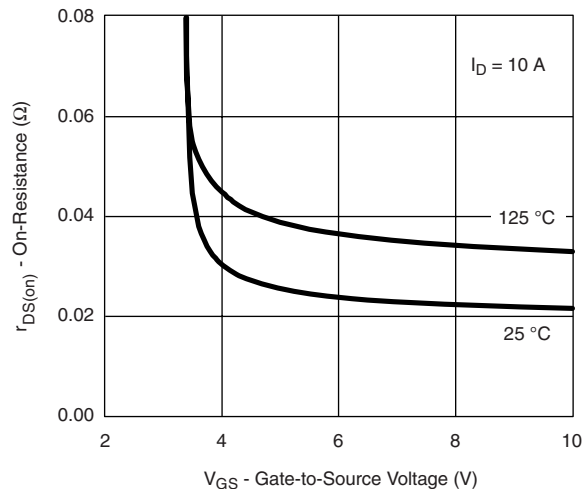
On-Resistance vs. Junction Temperature



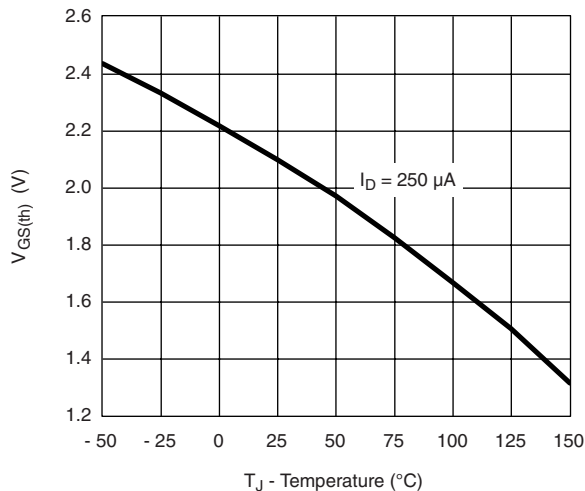
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



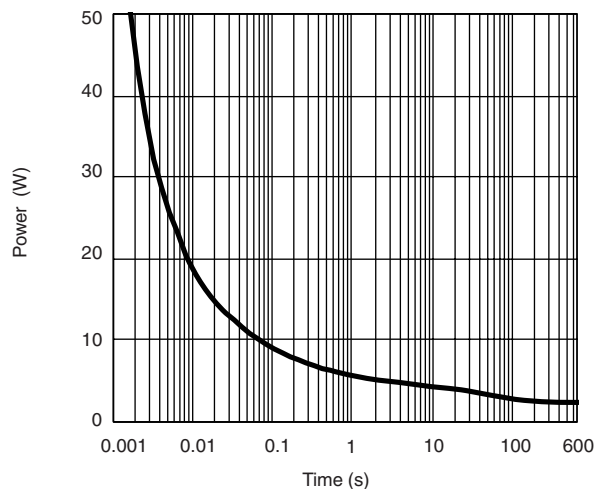
Source-Drain Diode Forward Voltage



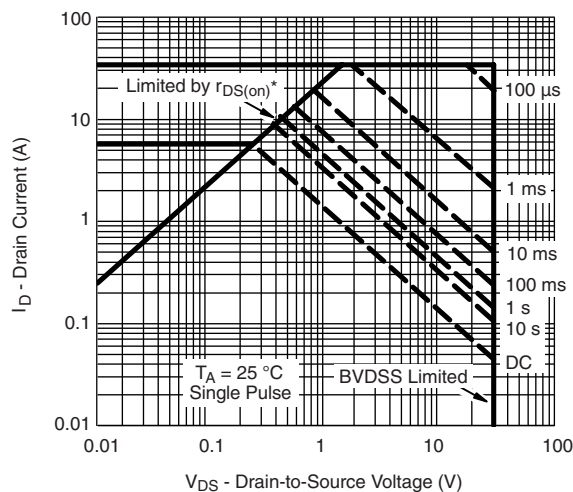
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient

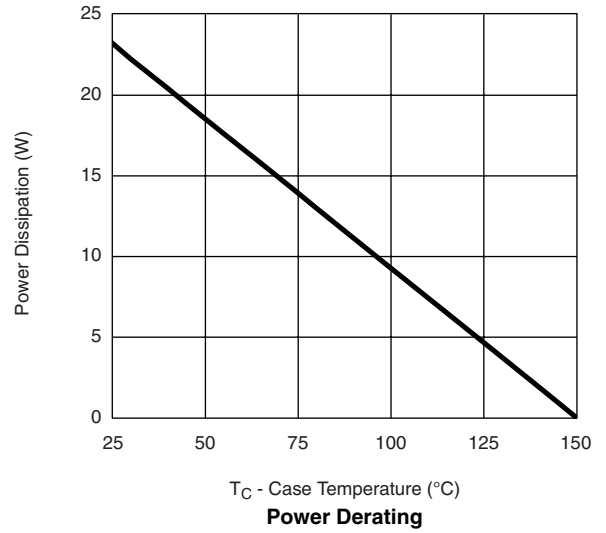
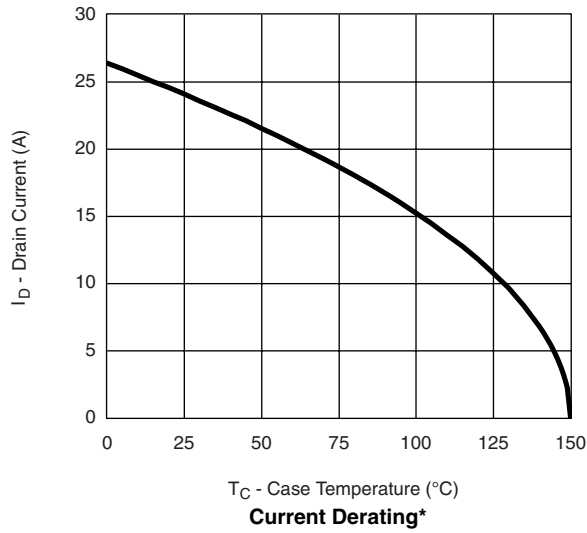


* $V_{GS} >$ minimum V_{GS} at which $r_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient



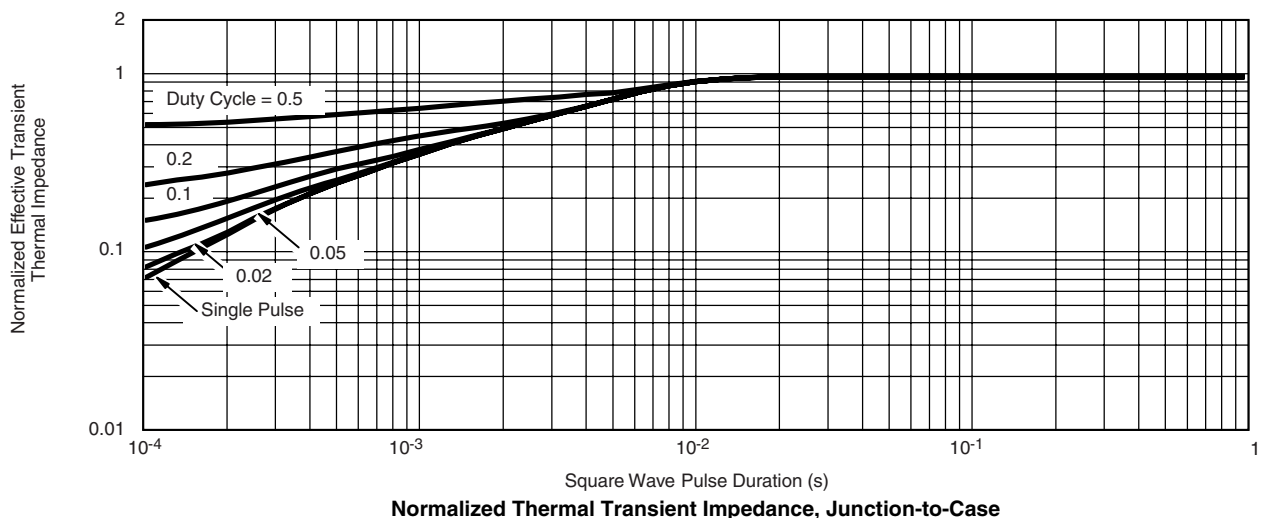
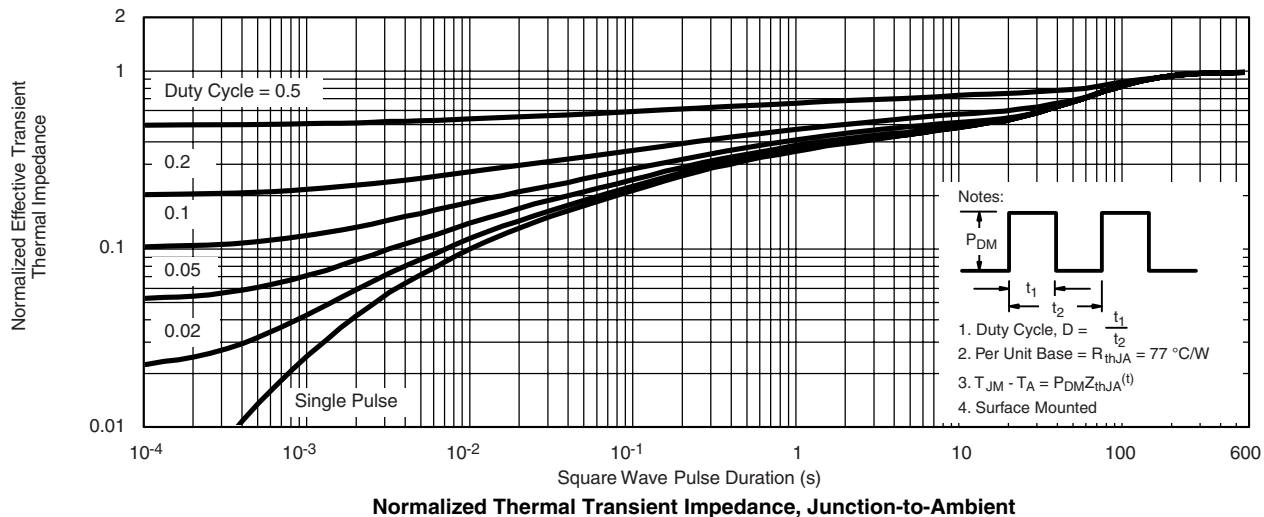
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?73958>.



Notice

Specifications of the products displayed herein are subject to change without notice. Vishay Intertechnology, Inc., or anyone on its behalf, assumes no responsibility or liability for any errors or inaccuracies.

Information contained herein is intended to provide a product description only. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Vishay's terms and conditions of sale for such products, Vishay assumes no liability whatsoever, and disclaims any express or implied warranty, relating to sale and/or use of Vishay products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright, or other intellectual property right.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications. Customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Vishay for any damages resulting from such improper use or sale.