



N-Channel 60-V (D-S) MOSFET



RoHS COMPLIANT

PRODUCT SUMMARY			
V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ)
60	0.058 @ V _{GS} = 10 V	6	13 nC
	0.072 @ V _{GS} = 4.5 V	6	

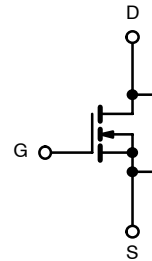
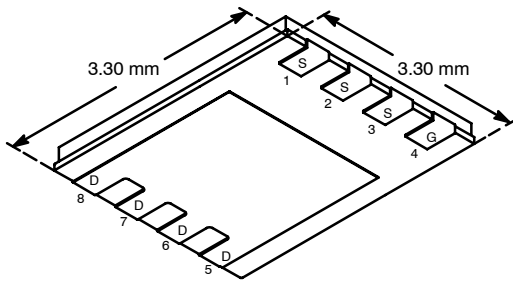
FEATURES

- TrenchFET® Power MOSFET
- Low Thermal Resistance PowerPAK® Package with Small Size and Low 1.07 mm Profile

APPLICATIONS

- CCFL Inverter
- Class-D Amp

PowerPAK 1212-8



Ordering Information: Si7308DN-T1—E3 (Lead (Pb)-Free)

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T _A = 25°C UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V _{DS}	60	V
Gate-Source Voltage		V _{GS}	± 20	
Continuous Drain Current (T _J = 150°C)	T _C = 25°C	I _D	6 ^a	A
	T _C = 70°C		6 ^a	
	T _A = 25°C		5.4 ^{b, c}	
	T _A = 70°C		4.3 ^{b, c}	
Pulsed Drain Current (10 μs Width)		I _{DM}	20	
Continuous Source-Drain Diode Current	T _C = 25°C	I _S	6 ^a	
	T _A = 25°C		2.7 ^{b, c}	
Avalanche Current		I _{AS}	11	
Single-Pulse Avalanche Energy		E _{AS}	6.1	mJ
Maximum Power Dissipation	T _C = 25°C	P _D	19.8	W
	T _C = 70°C		12.7	
	T _A = 25°C		3.2 ^{b, c}	
	T _A = 70°C		2.1 ^{b, c}	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}		R _{thJA}	31	39	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	5	6.3	

Notes:

- Package Limited.
- Surface Mounted on 1" x 1" FR4 Board.
- t = 10 sec
- See Solder Profile (<http://www.vishay.com/doc?73257>). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 81°C/W.

SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	60			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA		55		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			-6		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1		3	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = 20 V			100	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V			1	μA
		V _{DS} = 60 V, V _{GS} = 0 V, T _J = 85°C			10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	20			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 5.4 A		0.046	0.058	Ω
		V _{GS} = 4.5 V, I _D = 4.8 A		0.059	0.072	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 5.4 A		15		S
Dynamic^b						
Input Capacitance	C _{iSS}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz		665		pF
Output Capacitance	C _{oss}			75		
Reverse Transfer Capacitance	C _{rSS}			40		
Total Gate Charge	Q _g	V _{DS} = 30 V, V _{GS} = 10 V, I _D = 5.4 A		13	20	nC
		V _{DS} = 30 V, V _{GS} = 4.5 V, I _D = 5.4 A		6	9	
Gate-Source Charge	Q _{gs}		2.3			
Gate-Drain Charge	Q _{gd}		2.6			
Gate Resistance	R _g	f = 1 MHz		2		Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 30 V, R _L = 7 Ω I _D ≅ 4.3 A, V _{GEN} = 4.5 V, R _g = 1 Ω		15	25	ns
Rise Time	t _r			65	100	
Turn-Off Delay Time	t _{d(off)}			15	25	
Fall Time	t _f			10	15	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 30 V, R _L = 7 Ω I _D ≅ 4.3 A, V _{GEN} = 10 V, R _g = 1 Ω		10	15	
Rise Time	t _r			15	25	
Turn-Off Delay Time	t _{d(off)}			20	30	
Fall Time	t _f			10	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25°C			6	A
Pulse Diode Forward Current	I _{SM}				20	
Body Diode Voltage	V _{SD}	I _S = 1.7 A, V _{GS} = 0 V		0.8	1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 4.3 A, di/dt = 100 A/μs, T _J = 25°C		30	60	ns
Body Diode Reverse Recovery Charge	Q _{rr}			32	50	nC
Reverse Recovery Fall Time	t _a			25		ns
Reverse Recovery Rise Time	t _b			5		

Notes

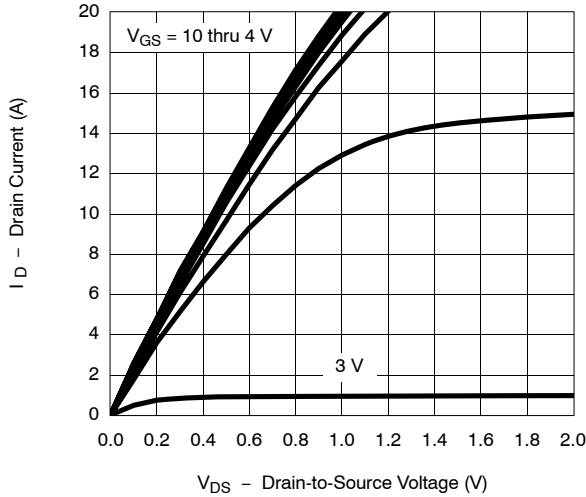
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

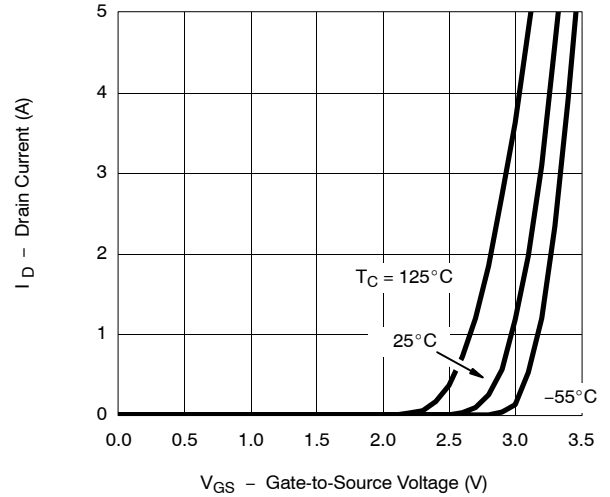


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

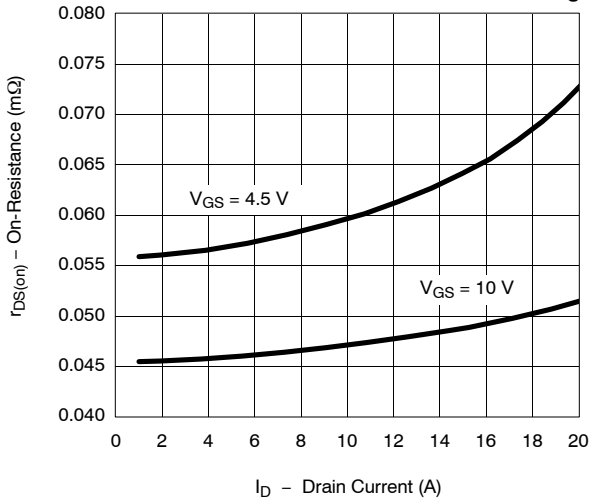
Output Characteristics



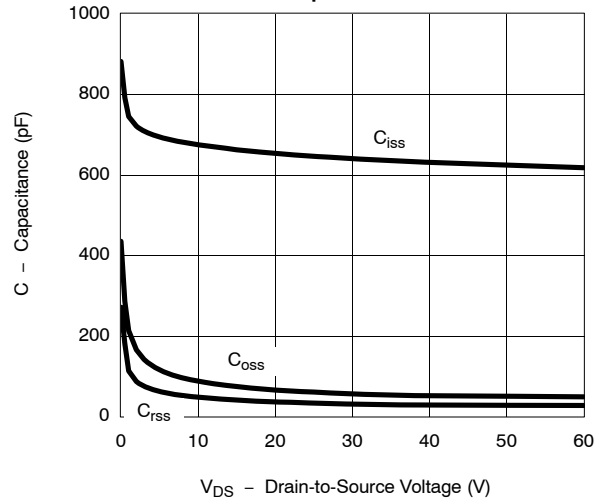
Transfer Characteristics



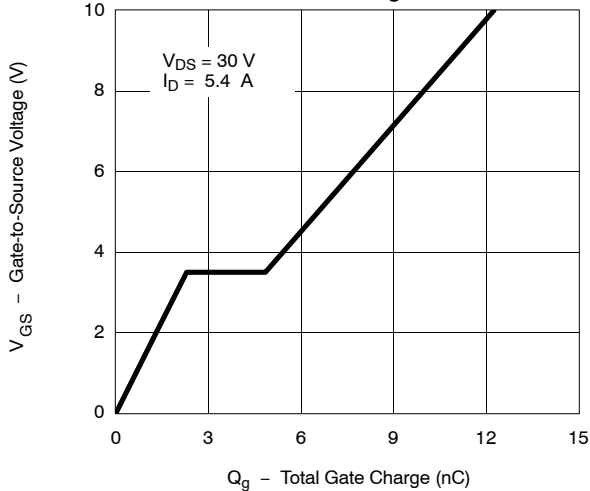
On-Resistance vs. Drain Current and Gate Voltage



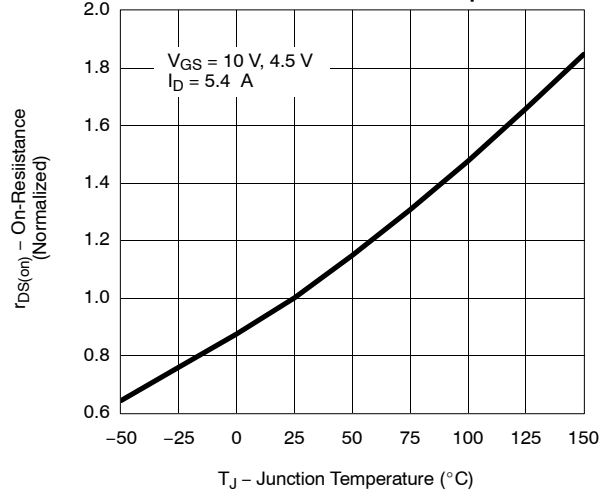
Capacitance



Gate Charge



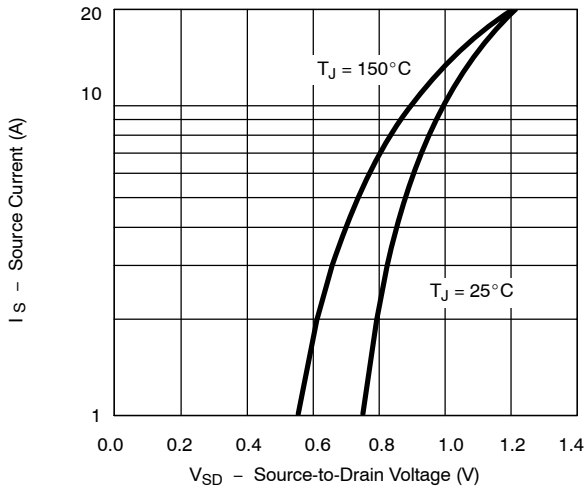
On-Resistance vs. Junction Temperature



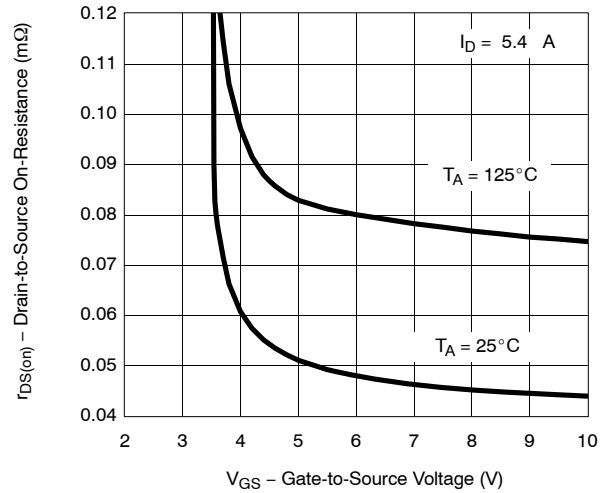


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

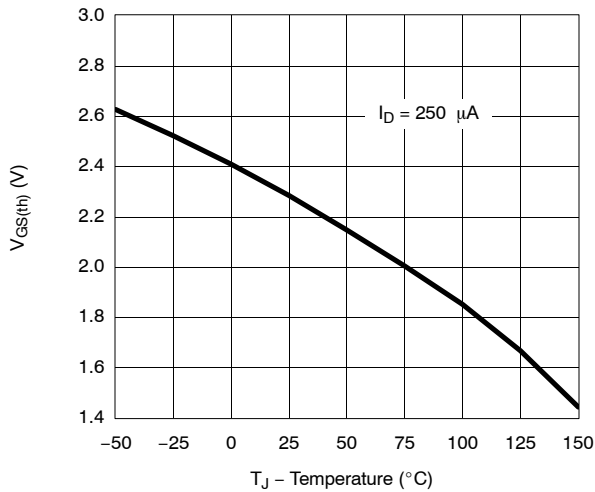
Source-Drain Diode Forward Voltage



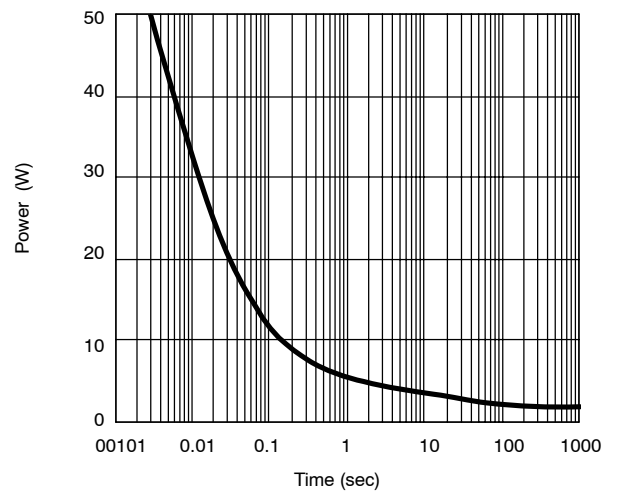
On-Resistance vs. Gate-to-Source Voltage



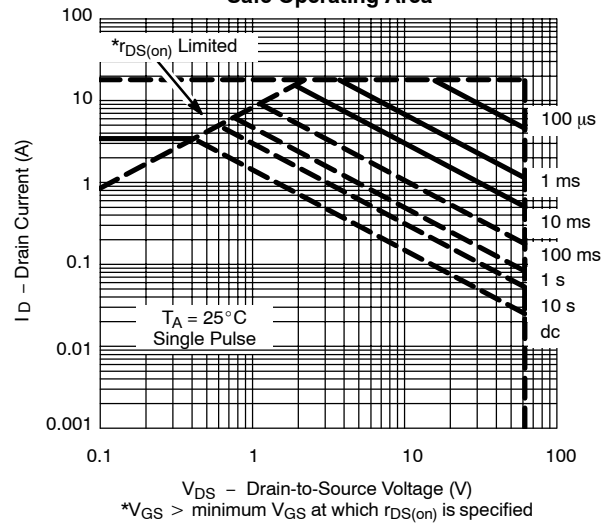
Threshold Voltage



Single Pulse Power, Junction-to-Ambient



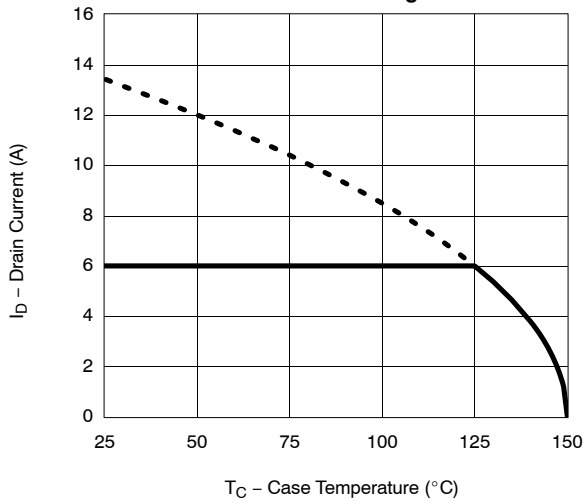
Safe Operating Area



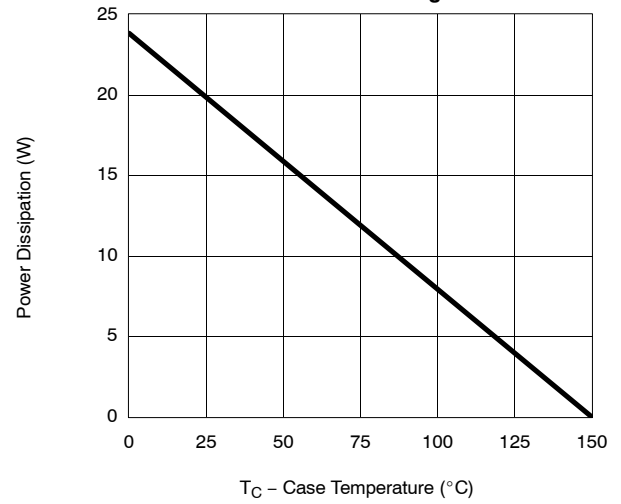


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

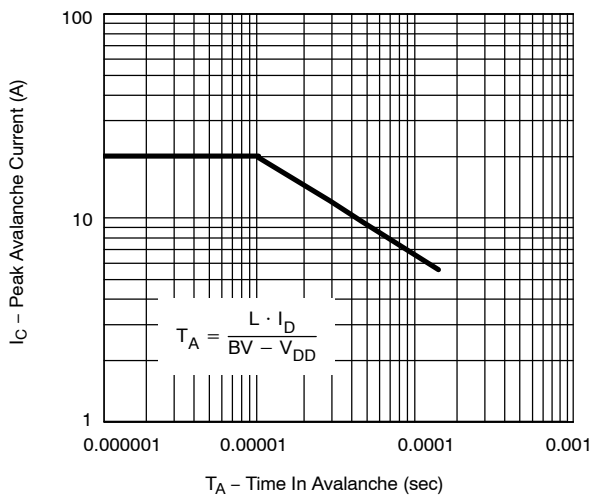
Current De-Rating*



Power De-Rating



Single Pulse Avalanche Capability

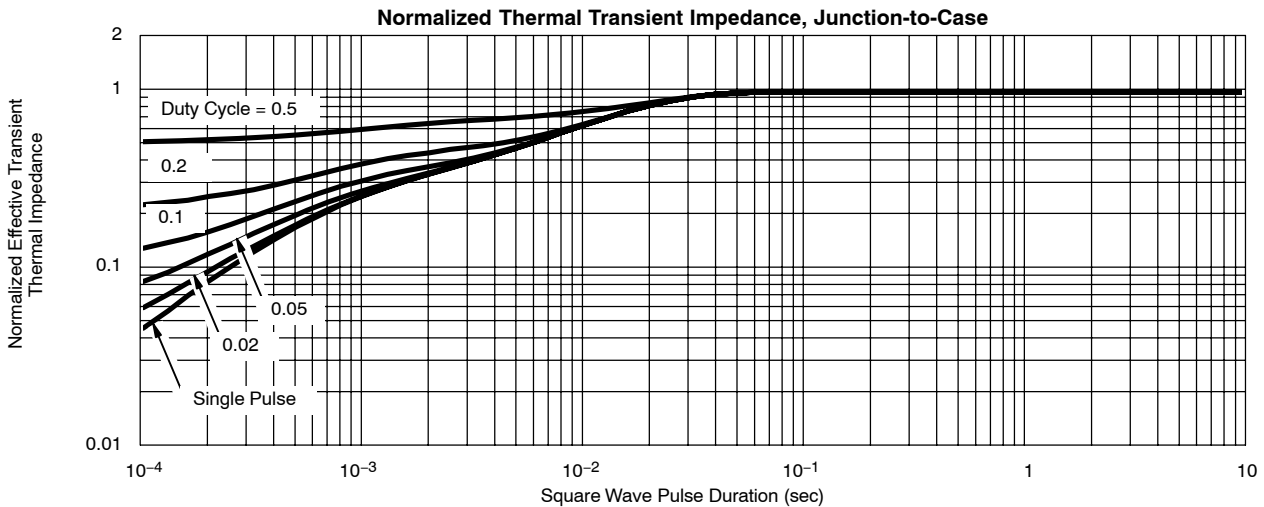
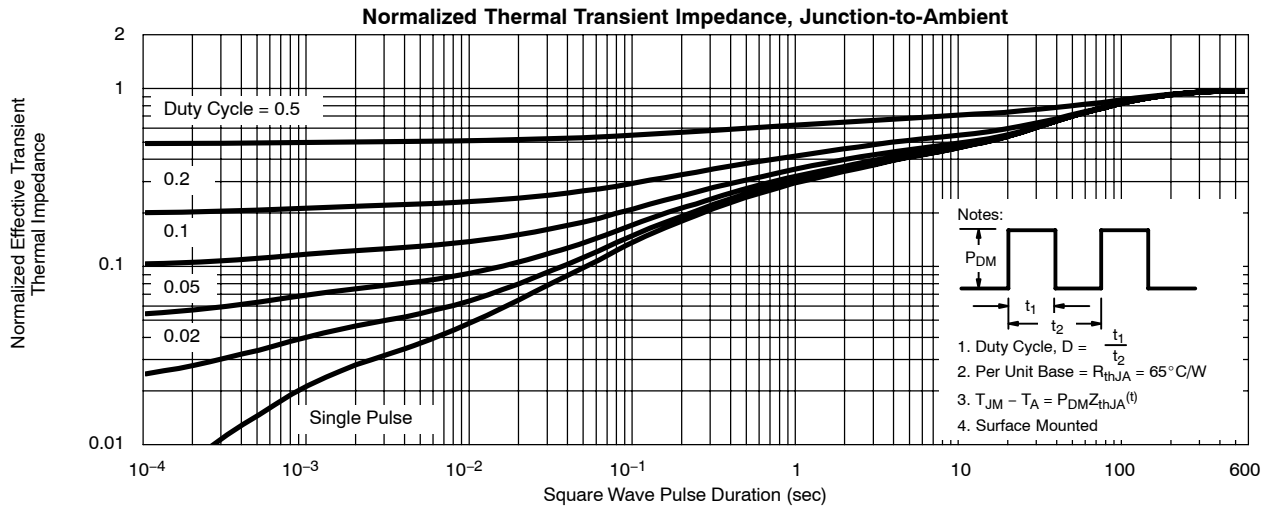


$$T_A = \frac{L \cdot I_D}{BV - V_{DD}}$$

*The power dissipation P_D is based on $T_{J(max)} = 150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?73419>.



Notice

Specifications of the products displayed herein are subject to change without notice. Vishay Intertechnology, Inc., or anyone on its behalf, assumes no responsibility or liability for any errors or inaccuracies.

Information contained herein is intended to provide a product description only. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Vishay's terms and conditions of sale for such products, Vishay assumes no liability whatsoever, and disclaims any express or implied warranty, relating to sale and/or use of Vishay products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright, or other intellectual property right.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications. Customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Vishay for any damages resulting from such improper use or sale.