

P-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ)
-30	0.019 @ $V_{GS} = -4.5$ V	-11	25
	0.031 @ $V_{GS} = -2.5$ V	-8.5	

FEATURES

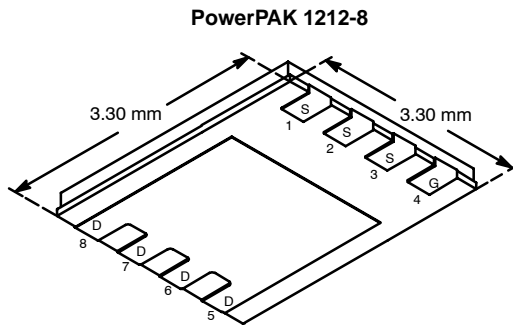
- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package with Low 1.07-mm Profile
- V_{DS} Optimized for Load Switch
- 100% R_g Tested



RoHS
COMPLIANT

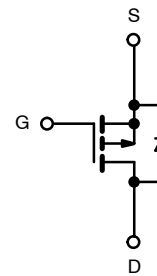
APPLICATIONS

- Load Switch



Bottom View

Ordering Information: Si7409ADN-T1—E3 (Lead (Pb)-Free)



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	V_{DS}	-30		V	
Gate-Source Voltage	V_{GS}	± 12			
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	-11	-7	A
		$T_A = 85^\circ\text{C}$	-7.9	-5	
Pulsed Drain Current	I_{DM}	-40			
continuous Source Current (Diode Conduction) ^a	I_S	-3.2	-1.3		
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	3.8	1.5	W
		$T_A = 85^\circ\text{C}$	2.0	0.8	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$	
Soldering Recommendations (Peak Temperature) ^{b, c}		260			

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 10$ sec	26	33	$^\circ\text{C/W}$
		Steady State	65	81	
Maximum Junction-to-Case	R_{thJC}	1.9	2.4		

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- See Reliability Manual for profile. The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.



SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)

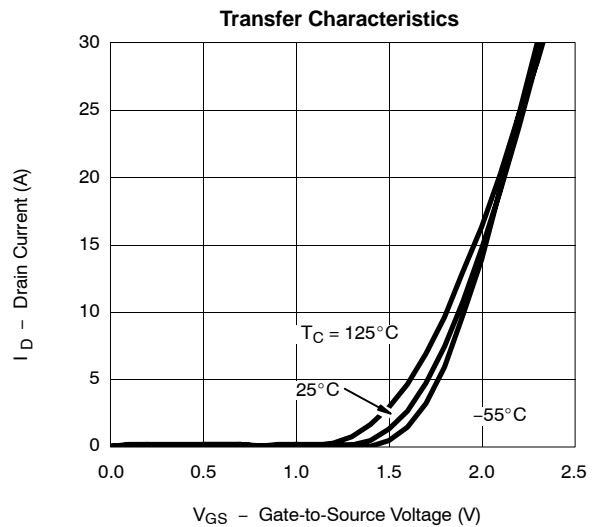
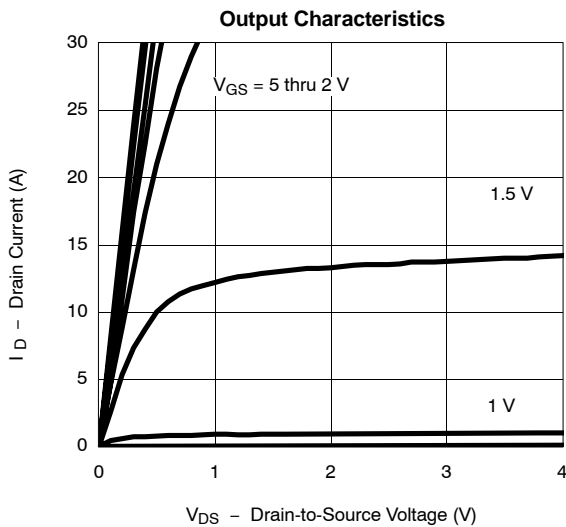
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-0.6		-1.5	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±12 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -30 V, V _{GS} = 0 V			-1	μA
		V _{DS} = -30 V, V _{GS} = 0 V, T _J = 85 °C			-5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≤ -5 V, V _{GS} = -4.5 V	-40			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = -4.5 V, I _D = -11 A		0.0015	0.019	Ω
		V _{GS} = -2.5 V, I _D = -8.5 A		0.025	0.031	
Forward Transconductance ^a	g _{fs}	V _{DS} = -15 V, I _D = -11 A		40		S
Diode Forward Voltage ^a	V _{SD}	I _S = -3.2 A, V _{GS} = 0 V		-0.7	-1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = -15 V, V _{GS} = -4.5 V, I _D = -11 A		25	40	nC
Gate-Source Charge	Q _{gs}			5		
Gate-Drain Charge	Q _{gd}			9		
Gate Resistance	R _g	f = 1.0 MHz	3.3	6.5	10	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = -15 V, R _L = 15 Ω I _D ≅ -1 A, V _{GEN} = -4.5 V, R _g = 6 Ω		30	45	ns
Rise Time	t _r			50	75	
Turn-Off Delay Time	t _{d(off)}			115	175	
Fall Time	t _f			75	115	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = -3.2 A, di/dt = 100 A/μs		60	90	ns
Reverse Recovery Charge	Q _{rr}			100	150	

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

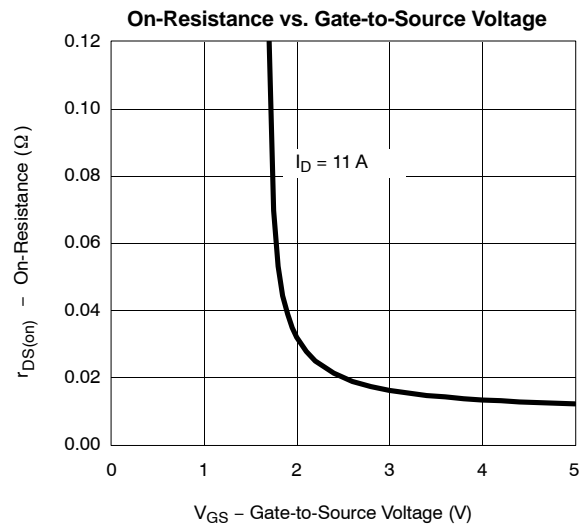
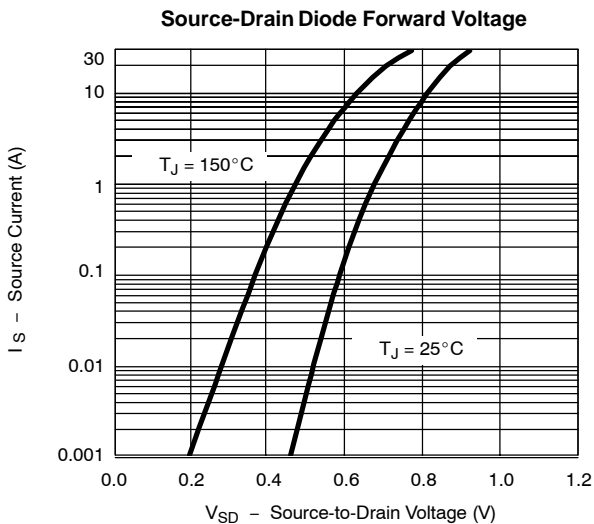
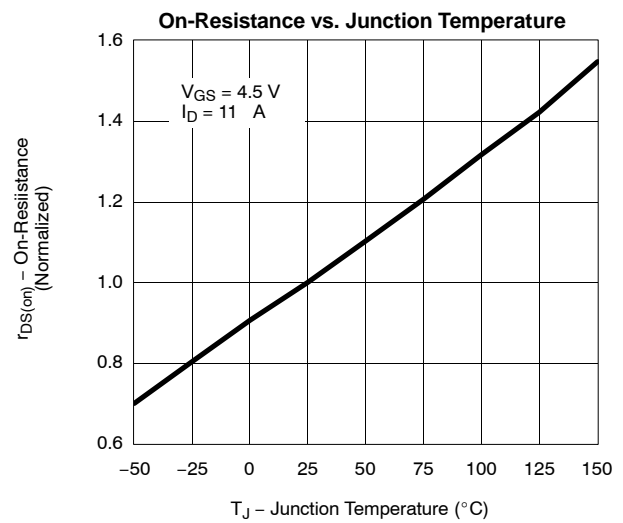
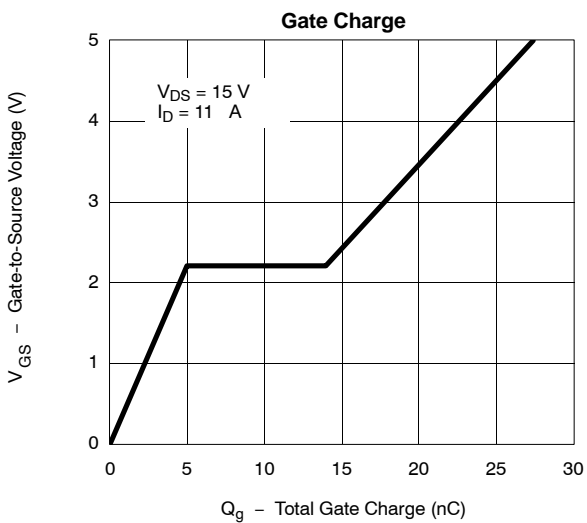
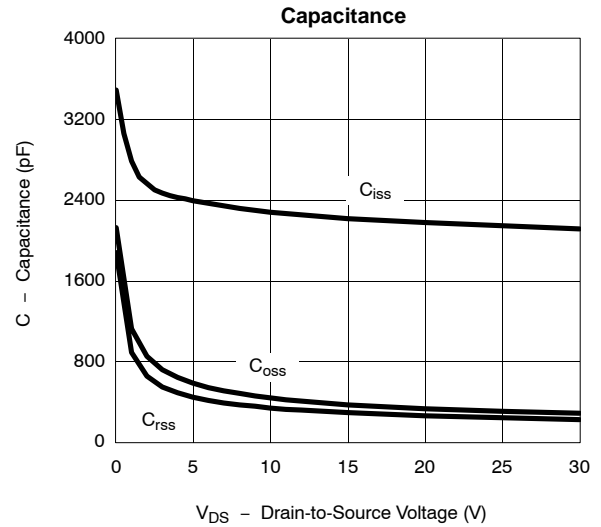
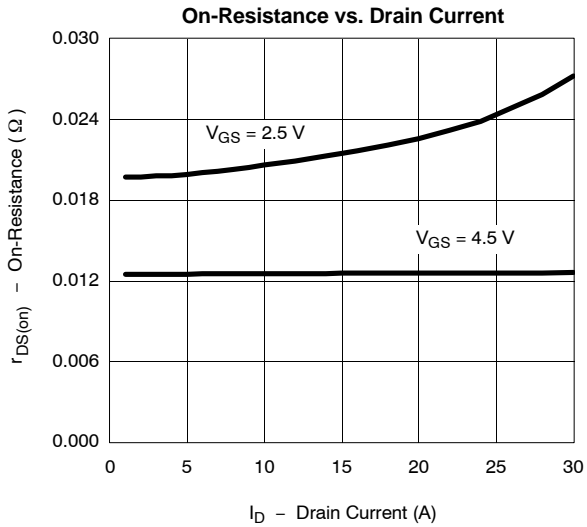
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



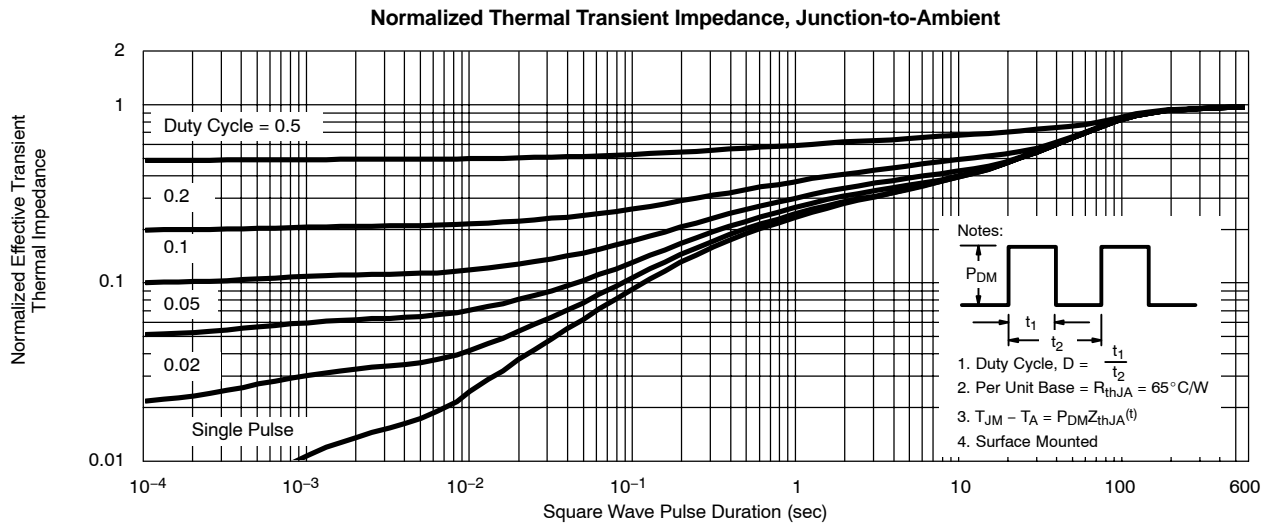
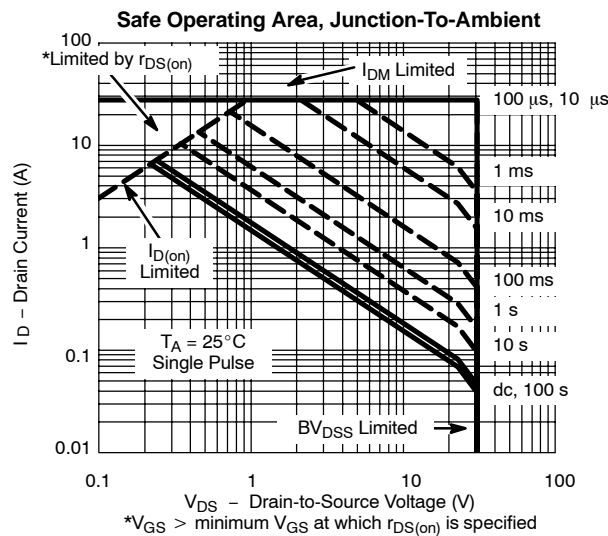
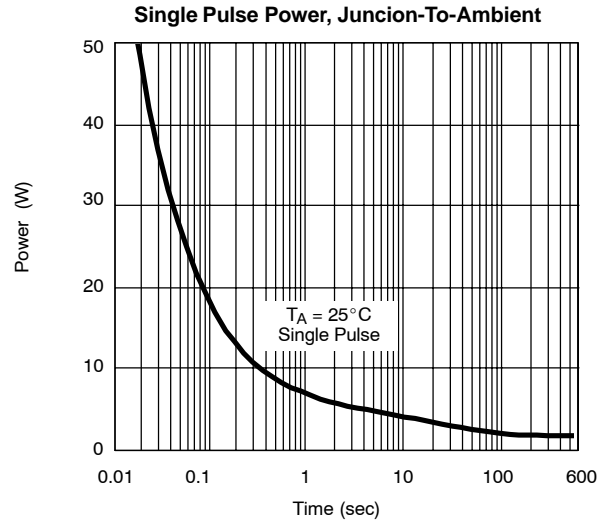
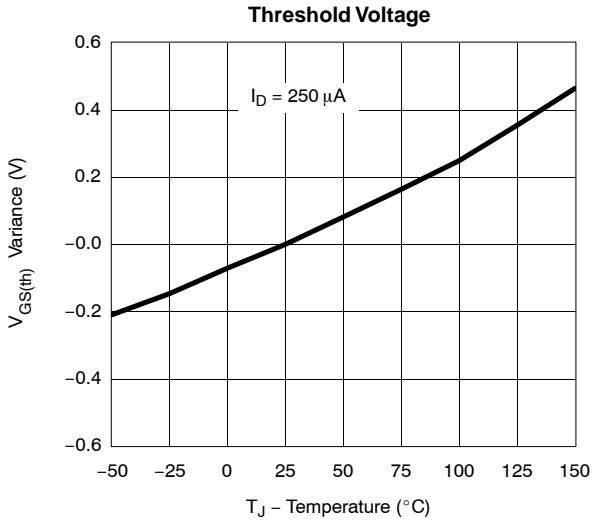


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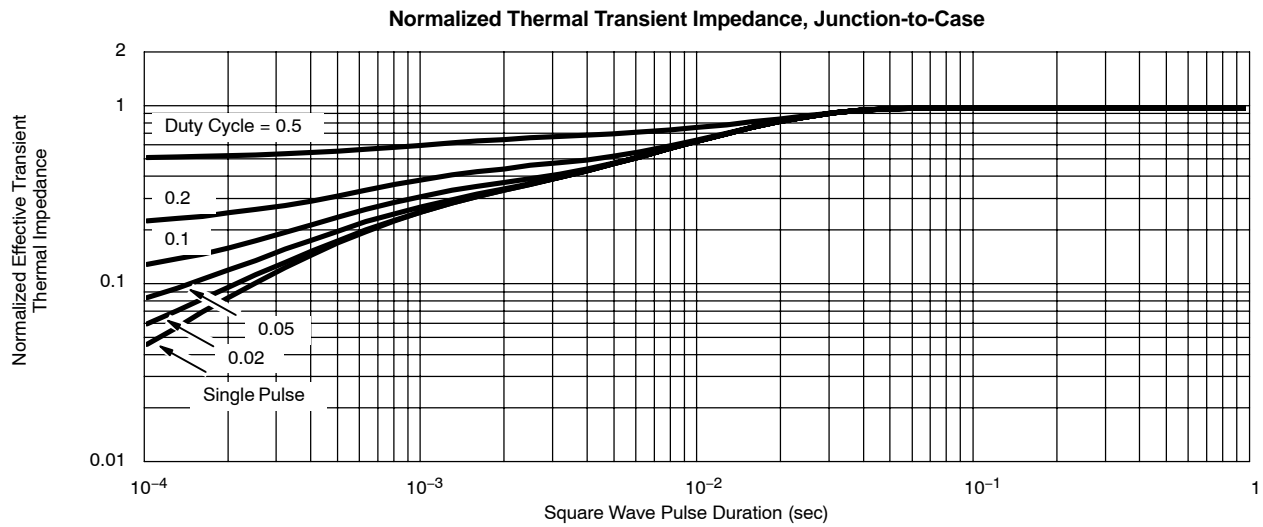


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TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



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