

N- and P-Channel 12-V (D-S) MOSFET

PRODUCT SUMMARY			
	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N-Channel	12	0.017 at $V_{GS} = 4.5$ V	11.8
		0.025 at $V_{GS} = 2.5$ V	9.8
P-Channel	-12	0.032 at $V_{GS} = -4.5$ V	-8.9
		0.053 at $V_{GS} = -2.5$ V	-6.9

FEATURES

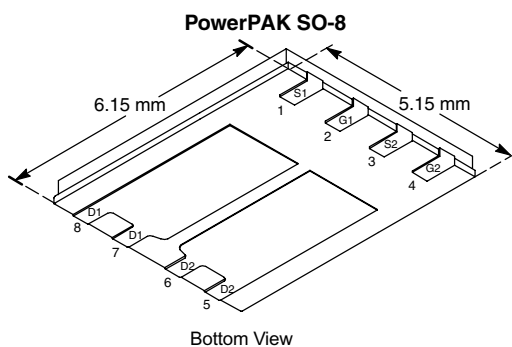
- TrenchFET[®] Power MOSFET
- New Low Thermal Resistance PowerPAK[®] Package with Low 1.07-mm Profile
- PWM Optimized for High Efficiency
- 100 % R_g Tested



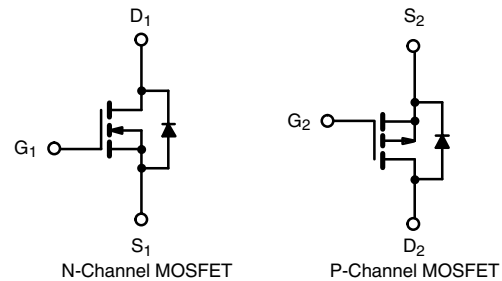
RoHS*
COMPLIANT

APPLICATIONS

- Point-of-Load Synchronous Rectifier
 - 5 V or 3.3 V BUS Step Down
 - Q_g Optimized for 500-kHz Operation
- Synchronous Buck, Shoot-Thru Resistant



Ordering Information: Si7540DP-T1
Si7540DP-T1—E3 (Lead (Pb)-free)



ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted							
Parameter	Symbol	N-Channel		P-Channel		Unit	
		10 secs	Steady	10 secs	Steady		
Drain-Source Voltage	V_{DS}	12		-12		V	
Gate-Source Voltage	V_{GS}	± 8					
Continuous Drain Current ($T_J = 150$ °C) ^a	I_D	$T_A = 25$ °C	11.8	7.6	-8.9	-5.7	A
		$T_A = 70$ °C	9.5	6.1	-7.1	-4.6	
Pulsed Drain Current	I_{DM}	20				A	
Continuous Source Current (Diode Conduction) ^a	I_S	2.9	1.1	-2.9	-1.1		
Maximum Power Dissipation ^a	P_D	$T_A = 25$ °C	3.5	1.4	3.5	1.4	W
		$T_A = 70$ °C	2.2	0.9	2.2	0.9	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150				°C	
Soldering Recommendations (Peak Temperature) ^{b,c}		260					

THERMAL RESISTANCE RATINGS							
Parameter	Symbol	N-Channel		P-Channel		Unit	
		Typical	Maximum	Typical	Maximum		
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 10$ sec	26	35	26	35	°C/W
		Steady State	60	85	60	85	
Maximum Junction-to-Case (Drain)	R_{thJC}	3.9	5.5	3.9	5.5		

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
 b. See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
 c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

* Pb containing terminations are not RoHS compliant, exemptions may apply.

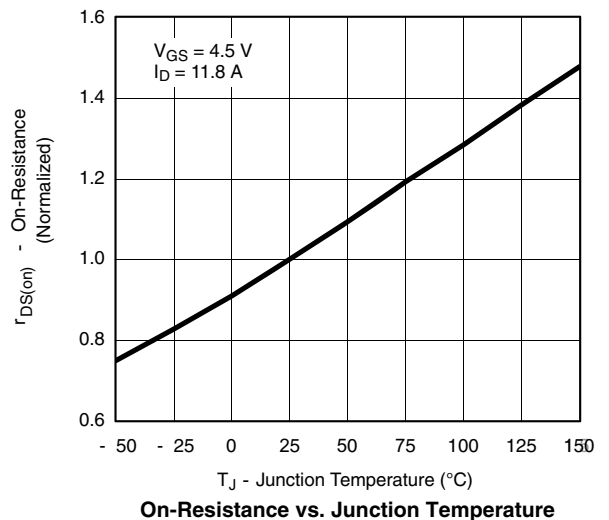
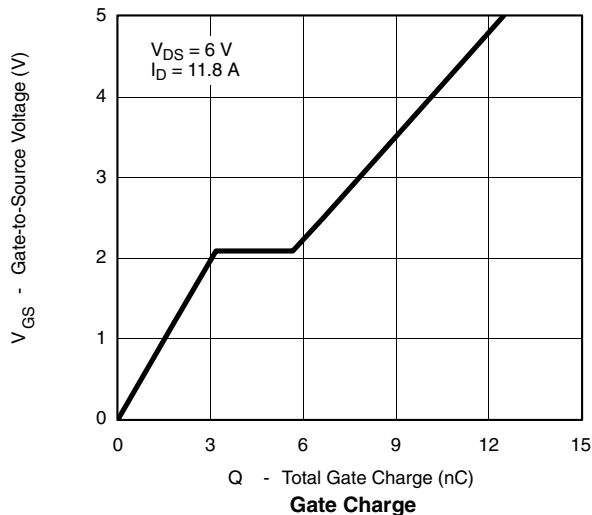
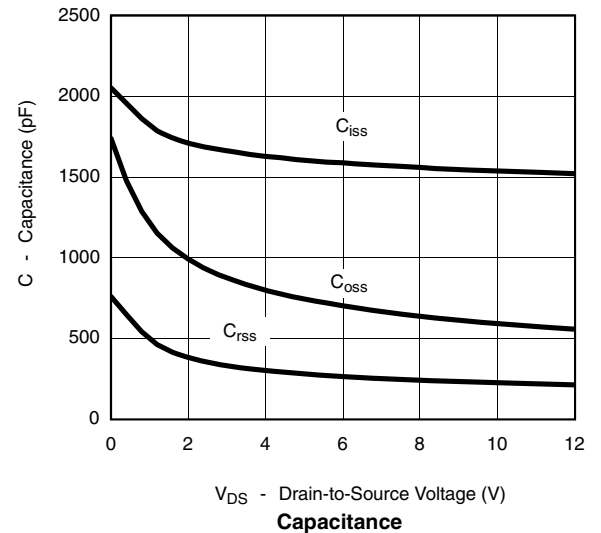
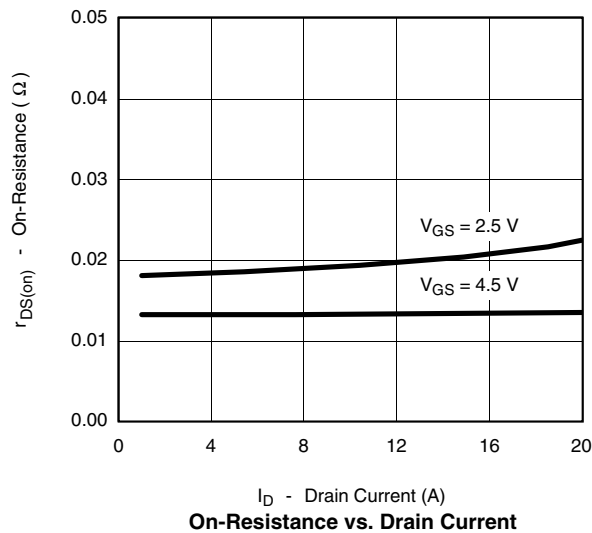
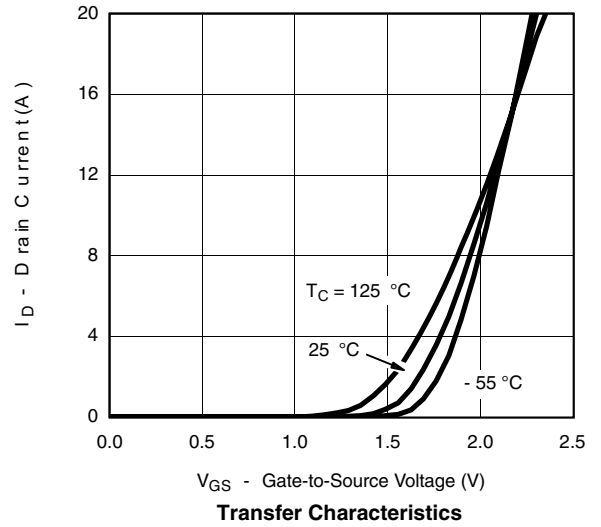
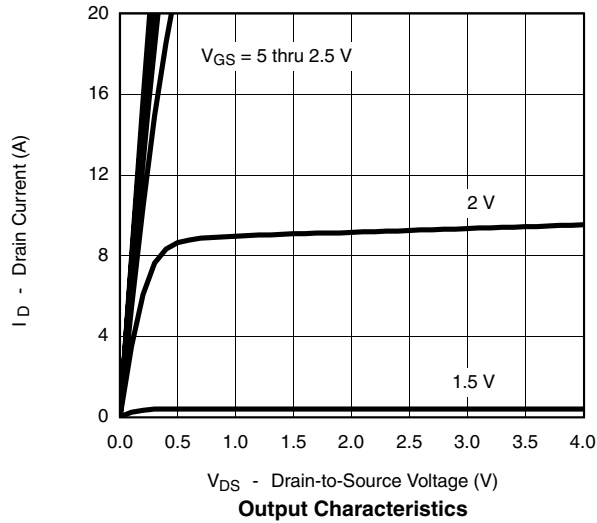
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Static							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	N-Ch	0.6		1.5	V
		$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-0.6		-1.5	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$	N-Ch P-Ch			± 100 ± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 12\text{ V}, V_{GS} = 0\text{ V}$	N-Ch			1	μA
		$V_{DS} = -12\text{ V}, V_{GS} = 0\text{ V}$	P-Ch			-1	
		$V_{DS} = 12\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	N-Ch			5	
		$V_{DS} = -12\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	P-Ch			-5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 4.5\text{ V}$	N-Ch	20			A
		$V_{DS} \leq -5\text{ V}, V_{GS} = -4.5\text{ V}$	P-Ch	-20			
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 11.8\text{ A}$	N-Ch		0.014	0.017	Ω
		$V_{GS} = -4.5\text{ V}, I_D = -8.9\text{ A}$	P-Ch		0.026	0.032	
		$V_{GS} = 2.5\text{ V}, I_D = 9.8\text{ A}$	N-Ch		0.020	0.025	
		$V_{GS} = -2.5\text{ V}, I_D = -6.9\text{ A}$	P-Ch		0.043	0.053	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 5\text{ V}, I_D = 11.8\text{ A}$	N-Ch		32		S
		$V_{DS} = -5\text{ V}, I_D = -8.9\text{ A}$	P-Ch		23		
Diode Forward Voltage ^a	V_{SD}	$I_S = 2.9\text{ A}, V_{GS} = 0\text{ V}$	N-Ch		0.77	1.2	V
		$I_S = -2.9\text{ A}, V_{GS} = 0\text{ V}$	P-Ch		-0.8	-1.2	
Dynamic^b							
Total Gate Charge	Q_g	N-Channel $V_{DS} = 6\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 11.8\text{ A}$ P-Channel $V_{DS} = -6\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -8.9\text{ A}$	N-Ch		11.5	17	nC
Gate-Source Charge	Q_{gs}		P-Ch		13	20	
Gate-Drain Charge	Q_{gd}		N-Ch		3.2		
Gate Resistance	R_g		N-Ch	0.5	1.7	2.5	Ω
			P-Ch	1.5	3.5	5.6	
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 6\text{ V}, R_L = 6\text{ }\Omega$ $I_D \cong 1\text{ A}, V_{GEN} = 4.5\text{ V}, R_G = 6\text{ }\Omega$	N-Ch		30	45	ns
Rise Time	t_r		P-Ch		35	55	
Turn-Off Delay Time	$t_{d(off)}$	P-Channel $V_{DD} = -6\text{ V}, R_L = 6\text{ }\Omega$ $I_D \cong -1\text{ A}, V_{GEN} = -4.5\text{ V}, R_G = 6\text{ }\Omega$	N-Ch		50	75	
			P-Ch		42	65	
Fall Time	t_f		N-Ch		60	90	
			P-Ch		54	85	
Source-Drain Reverse Recovery Time	t_{rr}		N-Ch		25	40	
			P-Ch		17	30	
			N-Ch		40	80	
			P-Ch		40	80	

Notes

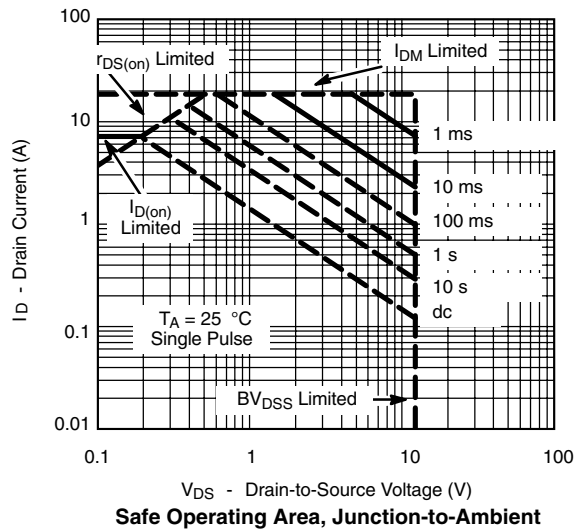
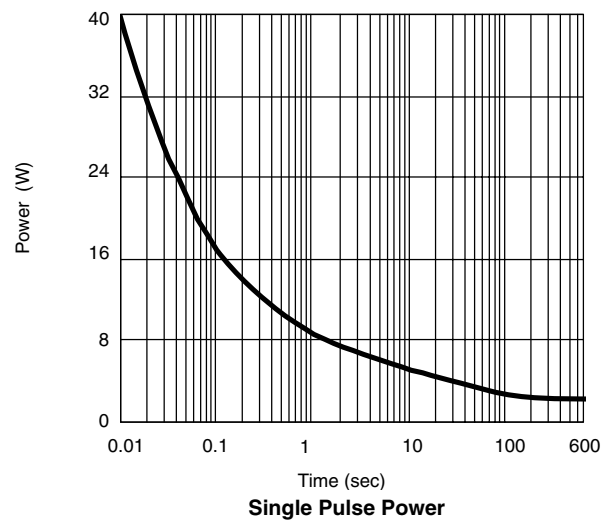
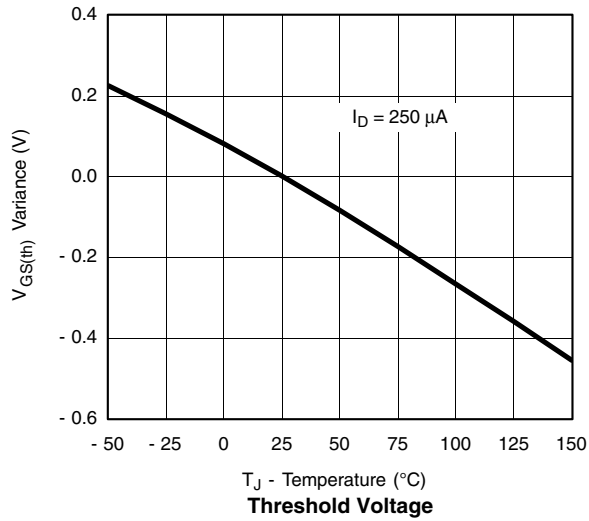
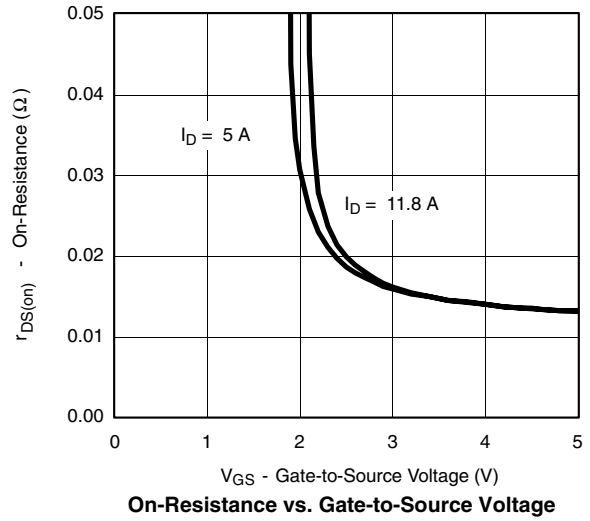
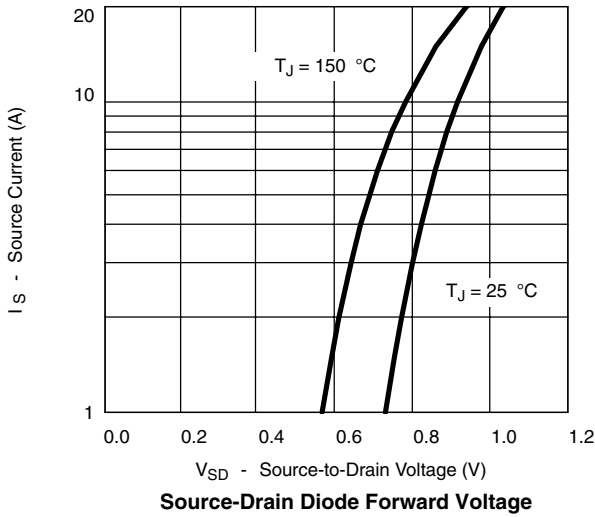
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless noted

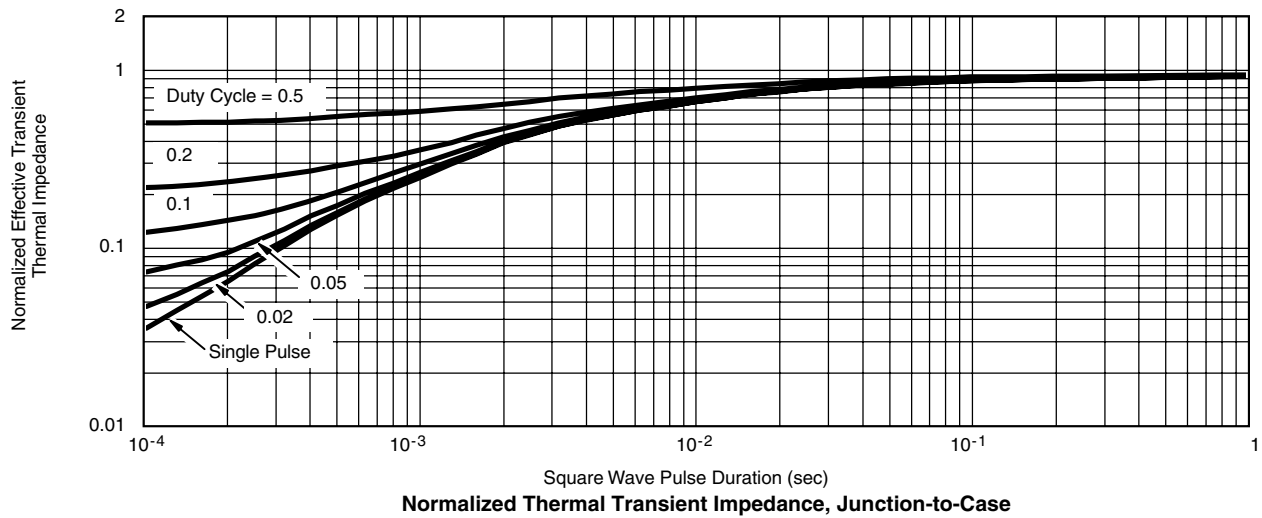
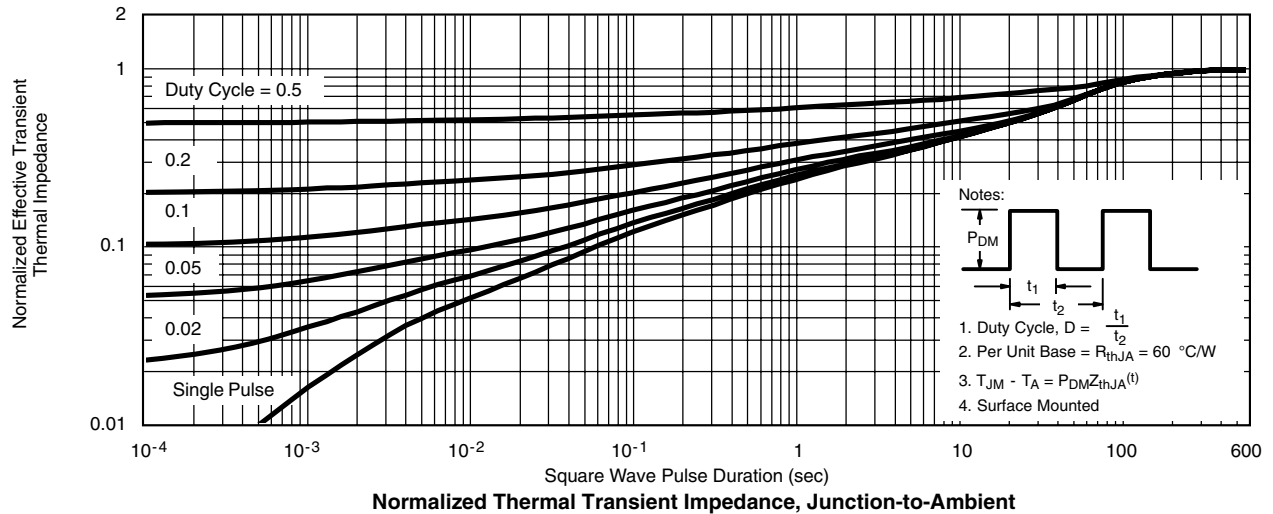


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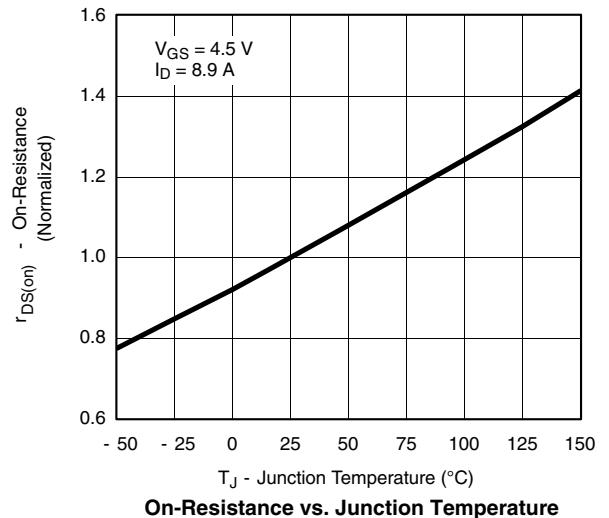
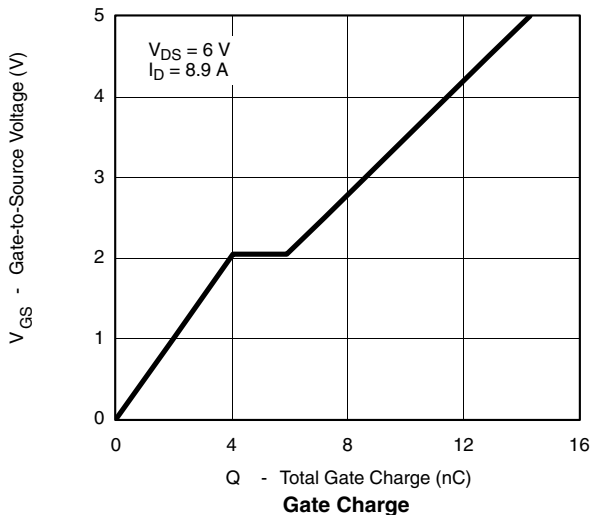
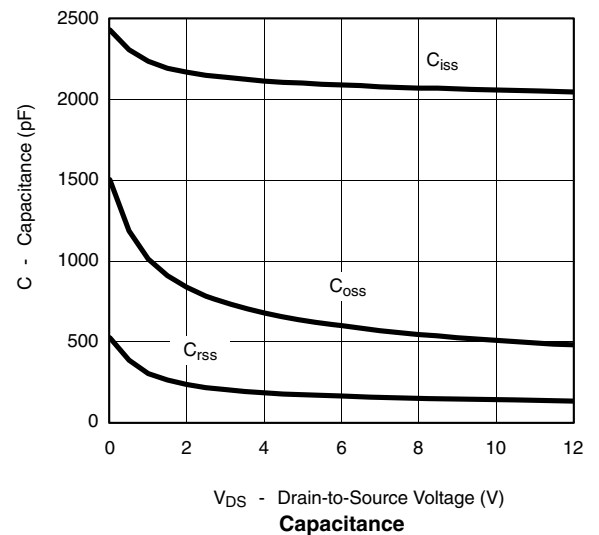
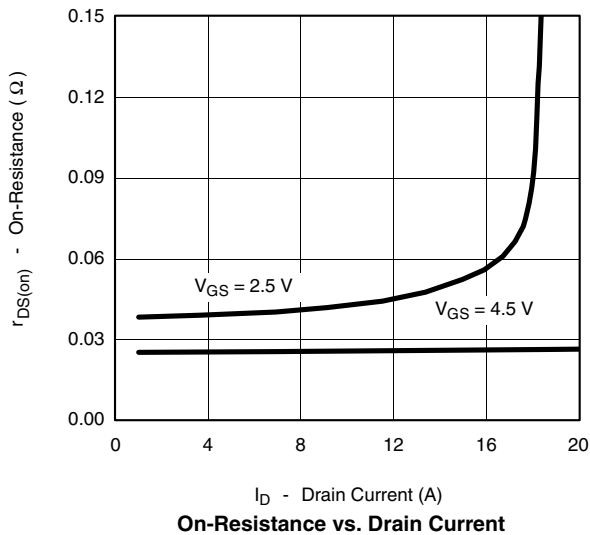
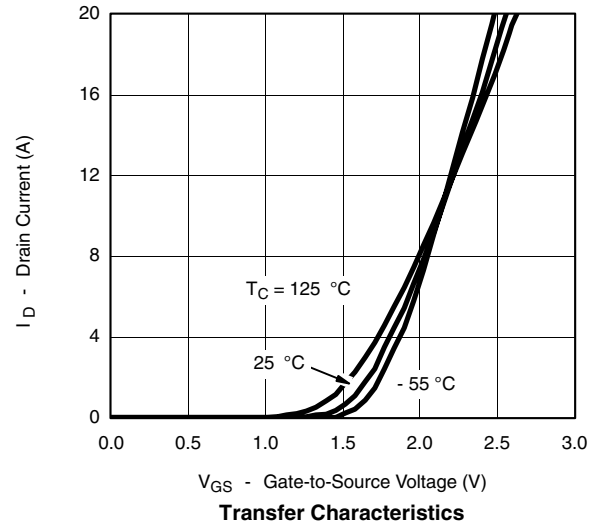
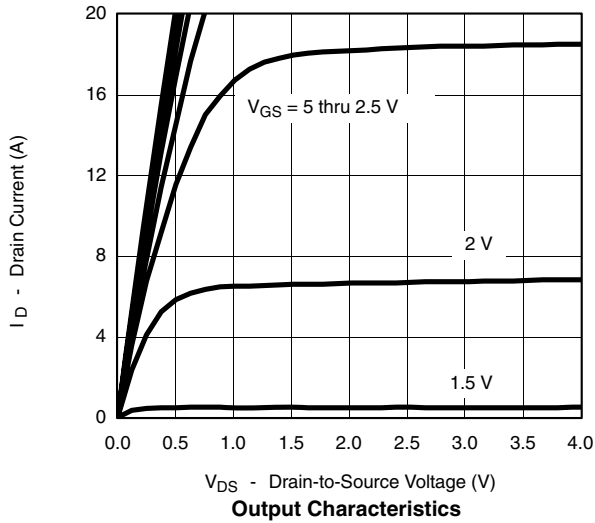




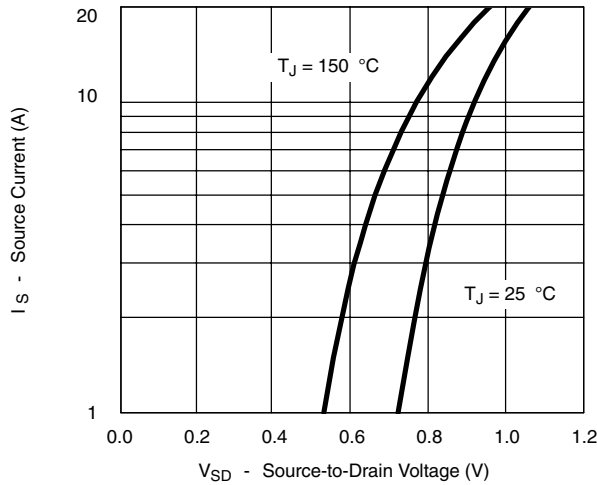
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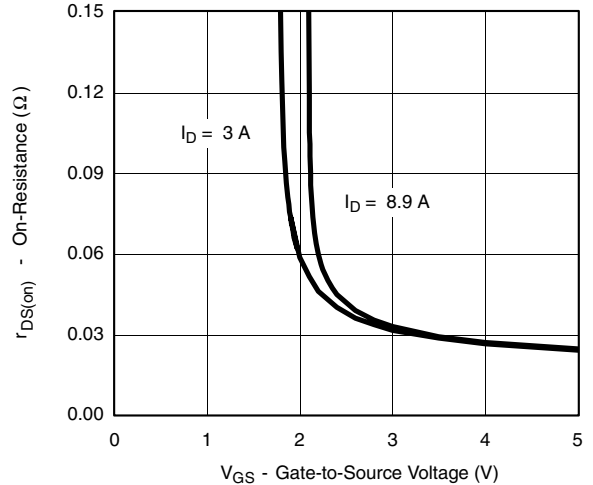
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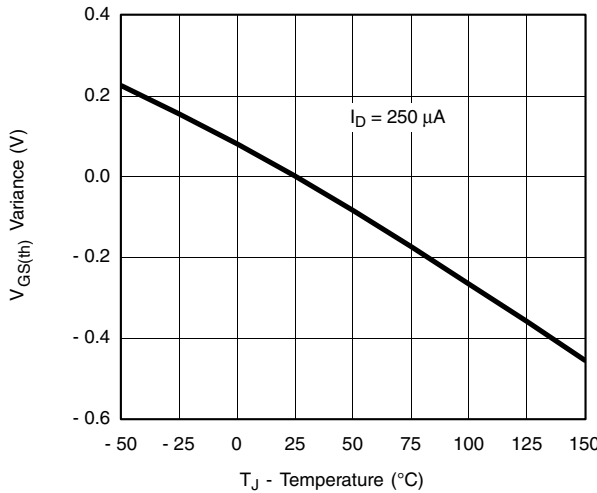
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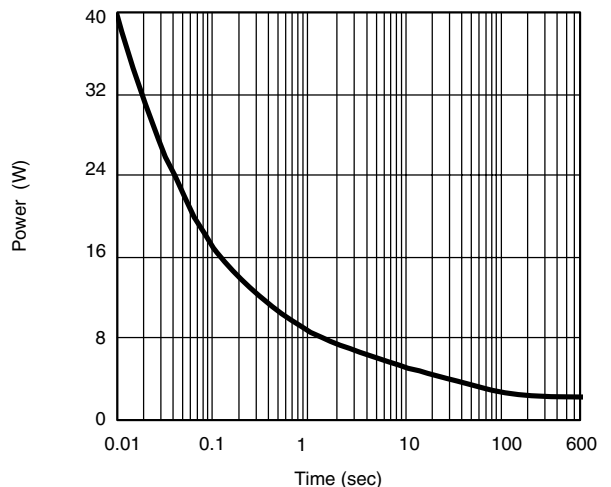
Source-Drain Diode Forward Voltage



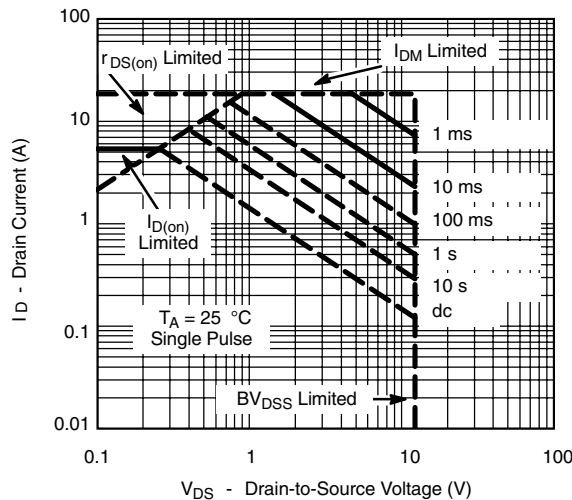
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

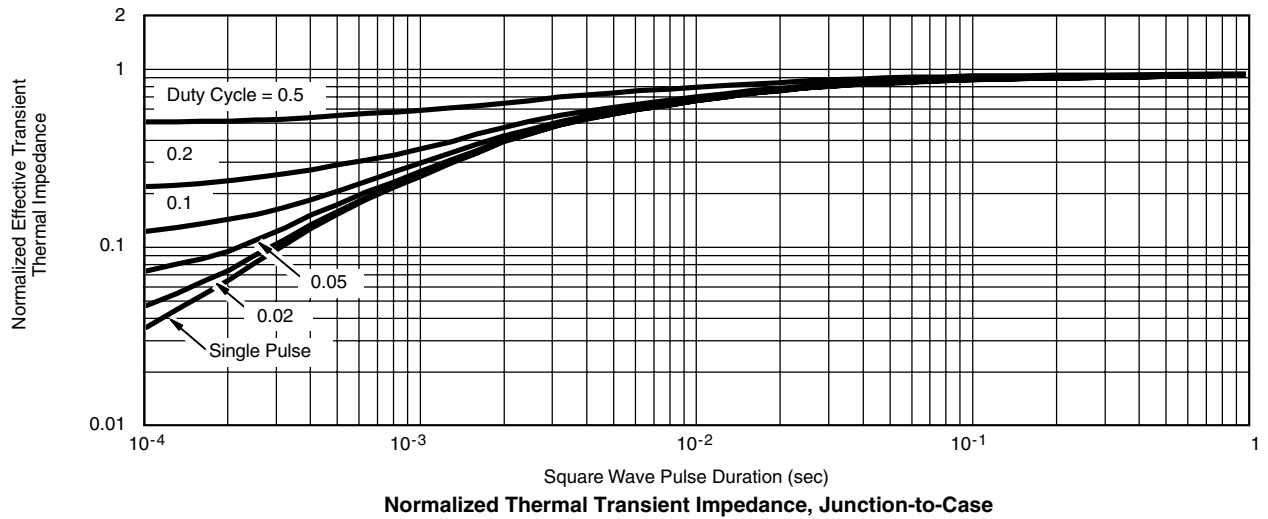
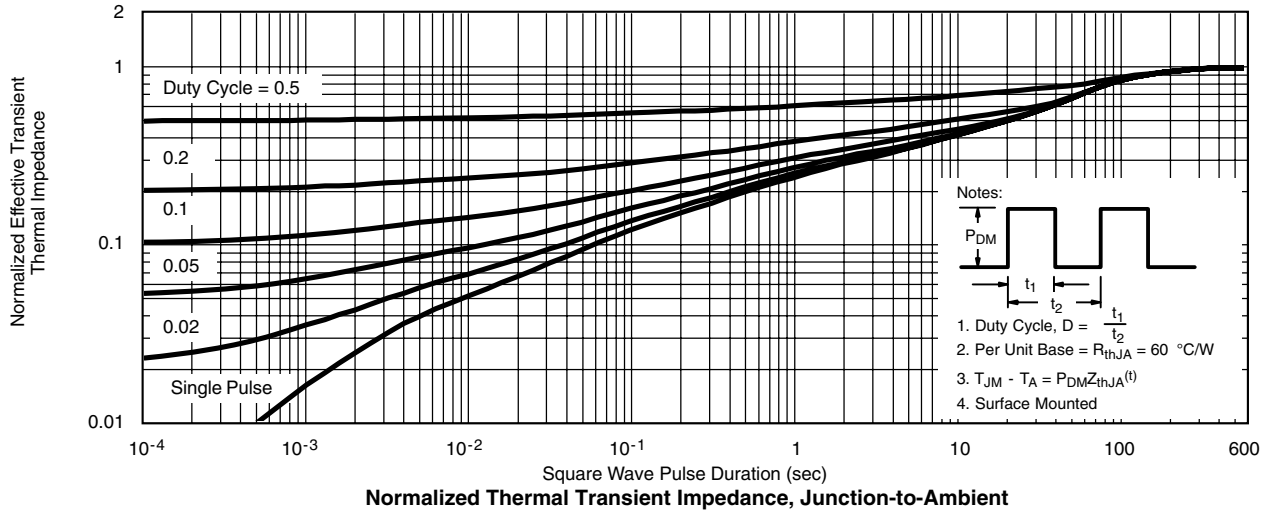


Single Pulse Power



Safe Operating Area, Junction-to-Ambient

P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless noted



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