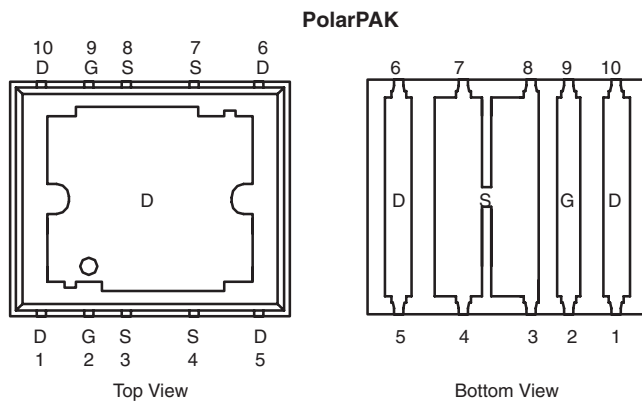


## N-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	r <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>a</sup>		Q <sub>g</sub> (Typ)
		Silicon Limit	Package Limit	
20	0.0034 at V <sub>GS</sub> = 10 V	138	50	24 nC
	0.0055 at V <sub>GS</sub> = 4.5 V	108	50	

[Package Drawing](http://www.vishay.com/doc?73398)  
<http://www.vishay.com/doc?73398>



Top surface is connected to pins 1, 5, 6, and 10

Ordering Information: SiE822DF-T1-E3 (Lead (Pb)-free)

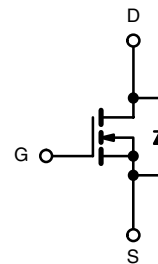
### FEATURES

- TrenchFET<sup>®</sup> Power MOSFET
- Ultra Low Thermal Resistance Using Top-Exposed PolarPAK<sup>®</sup> Package for Double-Sided Cooling
- Leadframe-Based New Encapsulated Package
  - Die Not Exposed
  - Same Layout Regardless of Die Size
- Low Q<sub>gd</sub>/Q<sub>gs</sub> Ratio Helps Prevent Shoot-Through
- 100 % R<sub>g</sub> and UIS Tested



### APPLICATIONS

- VRM
- DC-DC Conversion
- Synchronous Rectification



N-Channel MOSFET

[For Related Documents](http://www.vishay.com/ppg?74451)  
<http://www.vishay.com/ppg?74451>

ABSOLUTE MAXIMUM RATINGS T <sub>A</sub> = 25 °C, unless otherwise noted			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	20	V
Gate-Source Voltage	V <sub>GS</sub>	± 20	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	138 (Silicon Limit)	A
		50 <sup>a</sup> (Package Limit)	
		50 <sup>a</sup>	
		31 <sup>b, c</sup>	
Pulsed Drain Current	I <sub>DM</sub>	80	
		24.8 <sup>b, c</sup>	
Continuous Source-Drain Diode Current	I <sub>S</sub>	50 <sup>a</sup>	
		4.3 <sup>b, c</sup>	
Single Pulse Avalanche Current	I <sub>AS</sub>	30	mJ
Avalanche Energy	E <sub>AS</sub>	45	
Maximum Power Dissipation	P <sub>D</sub>	104	W
		66	
		5.2 <sup>b, c</sup>	
		3.3 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 50 to 150	°C
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>		260	

Notes:

- Package limited is 50 A.
- Surface Mounted on 1" x 1" FR4 board.
- t = 10 sec.
- See Solder Profile (<http://www.vishay.com/doc?73257>). The PolarPAK is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

**THERMAL RESISTANCE RATINGS**

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a, b</sup>	$t \leq 10$ sec	$R_{thJA}$	20	24	°C/W
Maximum Junction-to-Case (Drain Top) <sup>a</sup>	Steady State	$R_{thJC}$ (Drain)	1	1.2	
Maximum Junction-to-Case (Source) <sup>a, c</sup>		$R_{thJC}$ (Source)	2.8	3.4	

Notes:

- a. Surface Mounted on 1" x 1" FR4 board.  
b. Maximum under Steady State conditions is 68 °C/W.  
c. Measured at source pin (on the side of the package).

**SPECIFICATIONS**  $T_J = 25$  °C, unless otherwise noted

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0$ V, $I_D = 250$ $\mu$ A	20			V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250$ $\mu$ A		24.1		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$		-7.1			
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250$ $\mu$ A	1.5	2.3	3.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 20$ V, $V_{GS} = 0$ V			1	$\mu$ A
		$V_{DS} = 20$ V, $V_{GS} = 0$ V, $T_J = 55$ °C			10	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5$ V, $V_{GS} = 10$ V	25			A
Drain-Source On-State Resistance <sup>a</sup>	$r_{DS(on)}$	$V_{GS} = 10$ V, $I_D = 18.3$ A		0.0028	0.0034	$\Omega$
		$V_{GS} = 4.5$ V, $I_D = 14.5$ A		0.0045	0.0055	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15$ V, $I_D = 18.3$ A		90		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 10$ V, $V_{GS} = 0$ V, $f = 1$ MHz		4200		pF
Output Capacitance	$C_{oss}$		1000			
Reverse Transfer Capacitance	$C_{rss}$		320			
Total Gate Charge	$Q_g$	$V_{DS} = 10$ V, $V_{GS} = 10$ V, $I_D = 20$ A		52	78	nC
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 10$ V, $V_{GS} = 4.5$ V, $I_D = 20$ A		24	36	
Gate-Drain Charge	$Q_{gd}$			13		
Gate Resistance	$R_g$		$f = 1$ MHz		1.0	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 10$ V, $R_L = 1$ $\Omega$ $I_D \cong 10$ A, $V_{GEN} = 4.5$ V, $R_g = 1$ $\Omega$		50	75	ns
Rise Time	$t_r$		220	330		
Turn-Off Delay Time	$t_{d(off)}$		35	55		
Fall Time	$t_f$		20	30		
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 20$ V, $R_L = 1$ $\Omega$ $I_D \cong 10$ A, $V_{GEN} = 10$ V, $R_g = 1$ $\Omega$		15	25	
Rise Time	$t_r$		25	40		
Turn-Off Delay Time	$t_{d(off)}$		35	55		
Fall Time	$t_f$		10	15		
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25$ °C			50	A
Pulse Diode Forward Current <sup>a</sup>	$I_{SM}$				80	
Body Diode Voltage	$V_{SD}$	$I_S = 10$ A		0.8	1.2	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = 10$ A, $di/dt = 100$ A/ $\mu$ s, $T_J = 25$ °C		40	60	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			36	60	nC
Reverse Recovery Fall Time	$t_a$			19		ns
Reverse Recovery Rise Time	$t_b$			21		

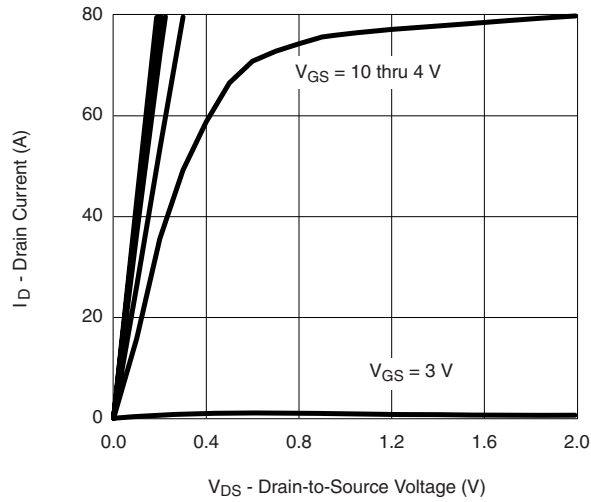
Notes:

- a. Pulse test; pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2$  %  
b. Guaranteed by design, not subject to production testing.

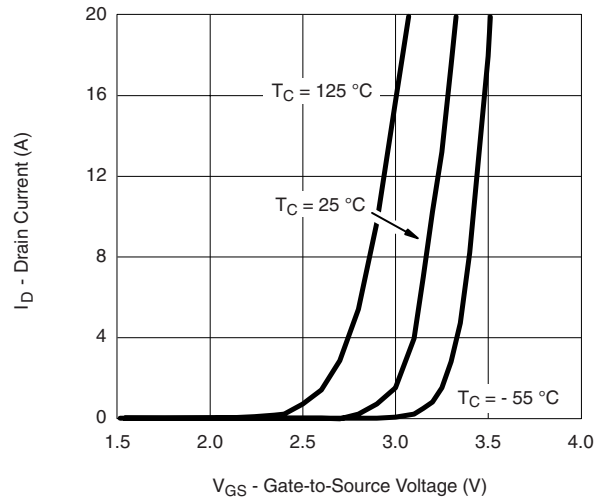
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



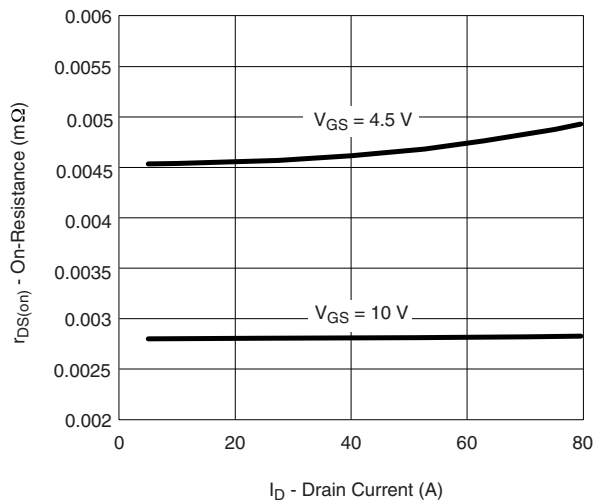
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



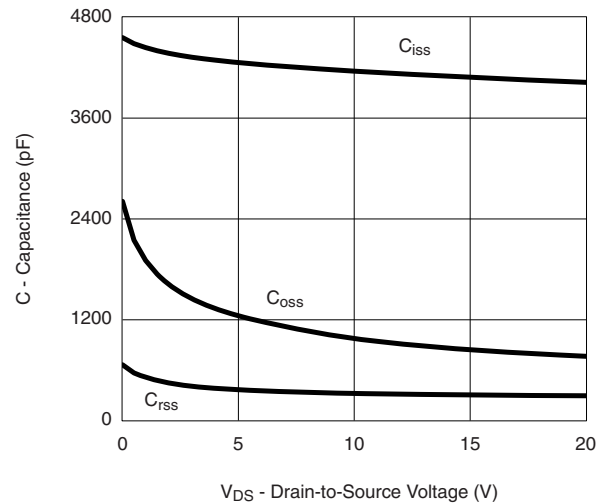
**Output Characteristics**



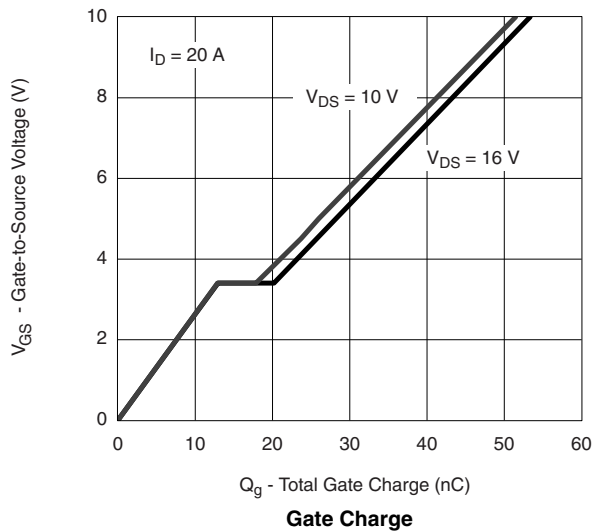
**Transfer Characteristics**



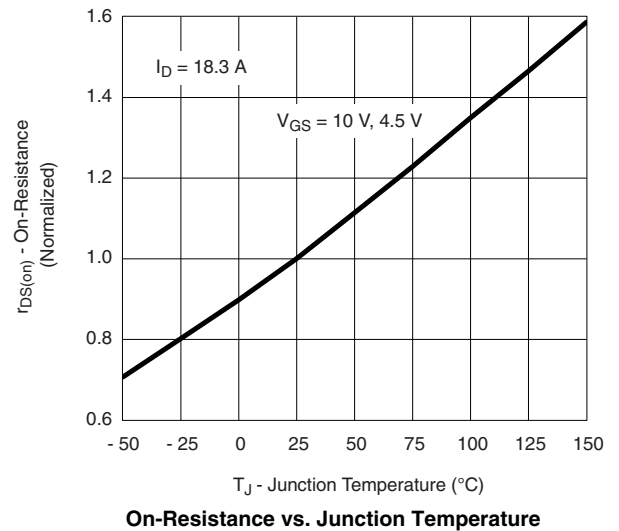
**On-Resistance vs. Drain Current**



**Capacitance**



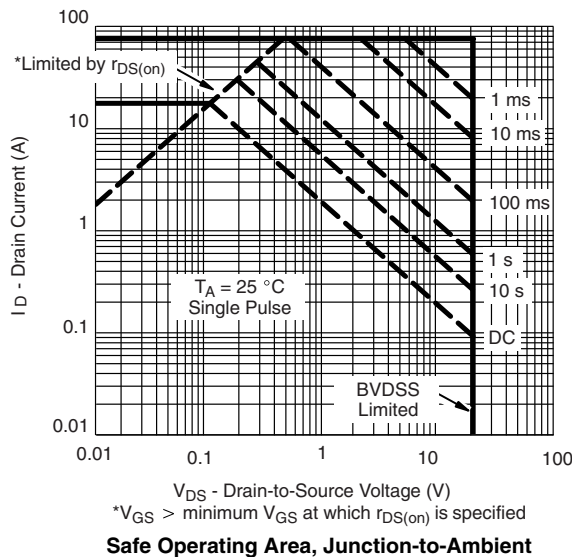
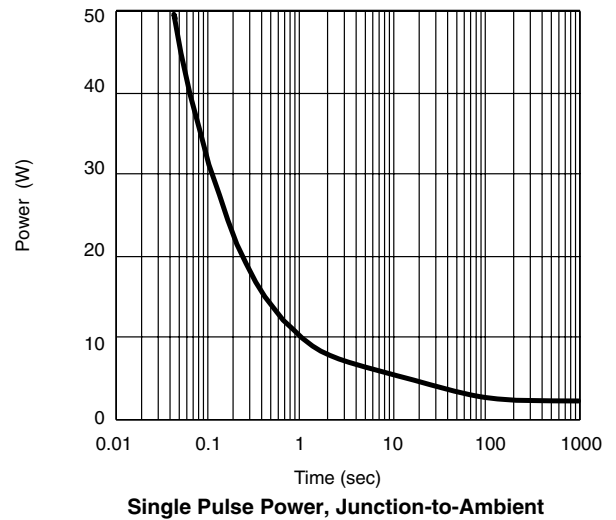
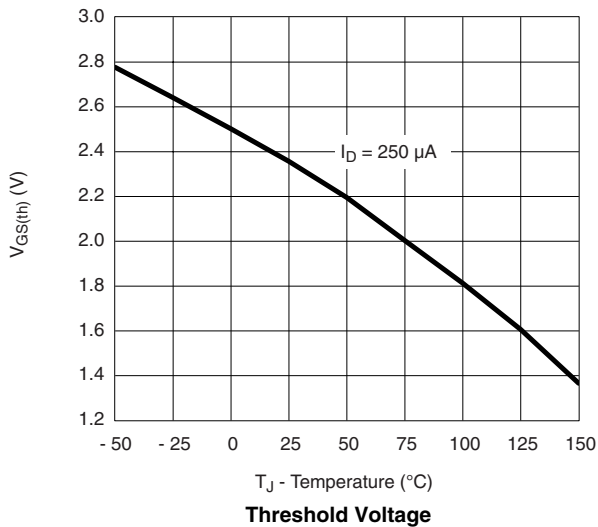
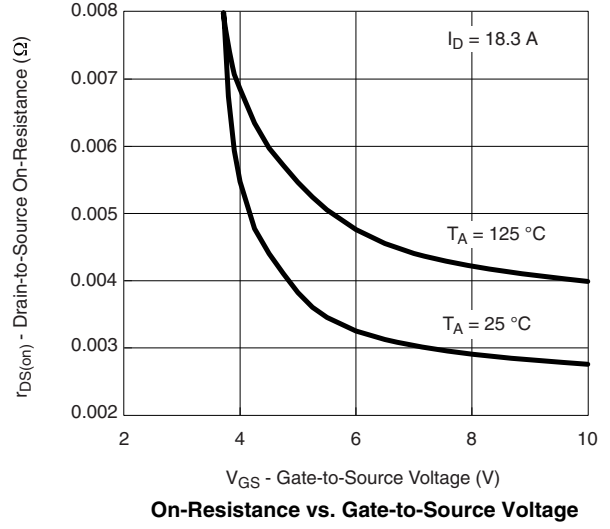
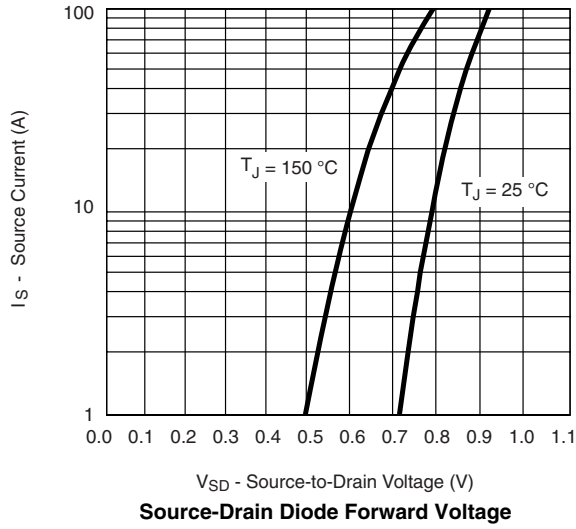
**Gate Charge**



**On-Resistance vs. Junction Temperature**

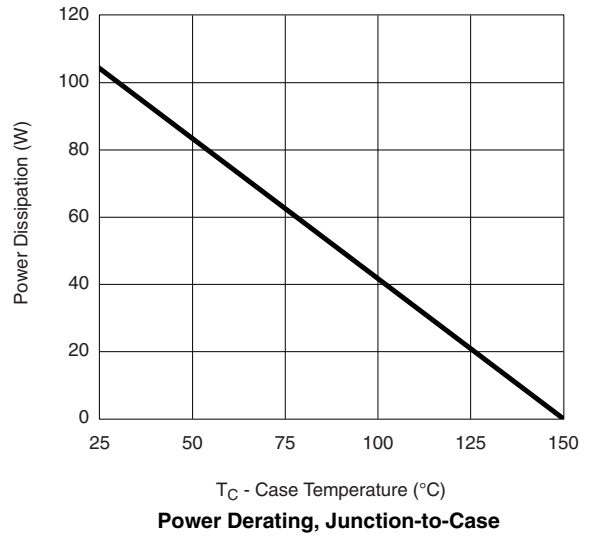
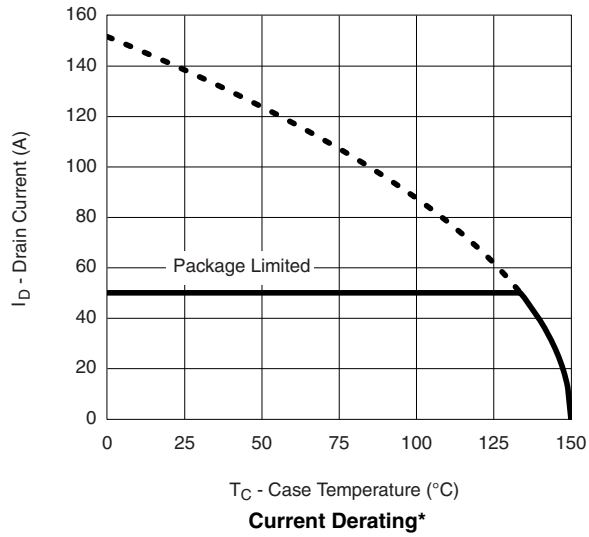


**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted





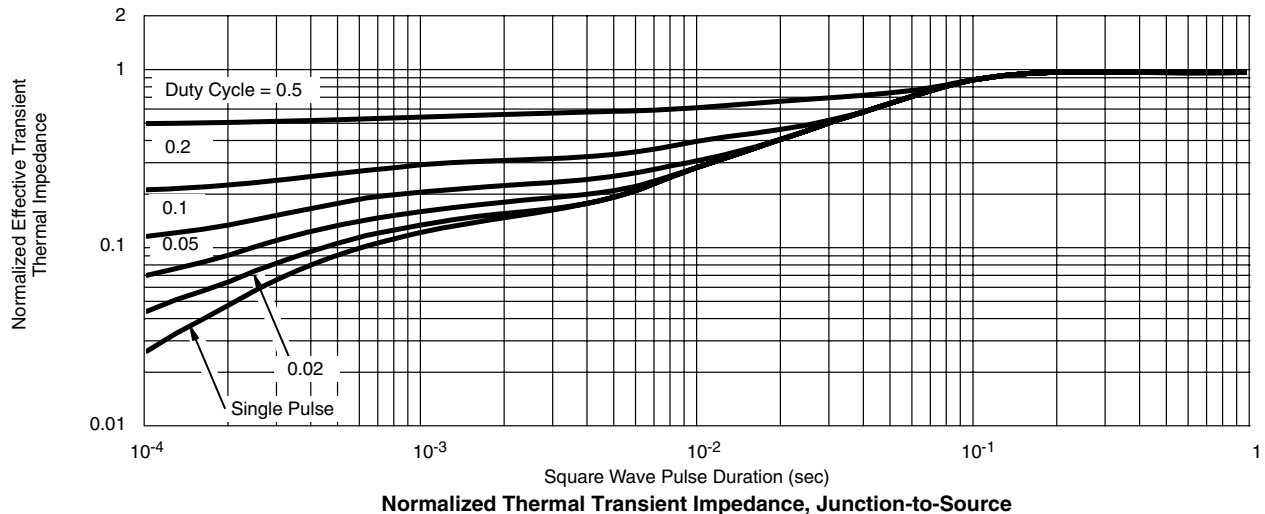
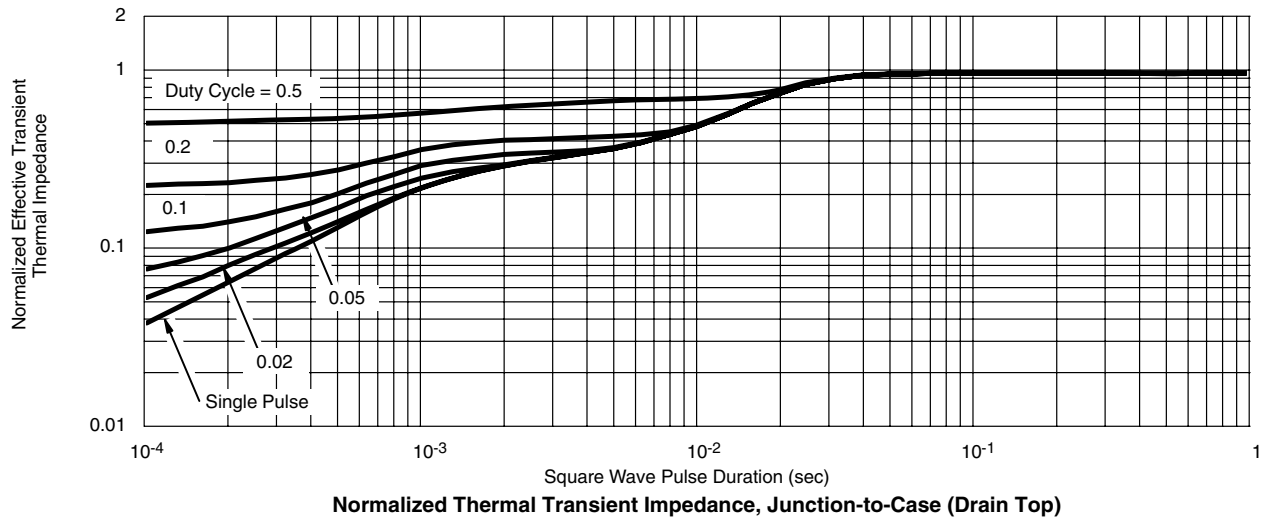
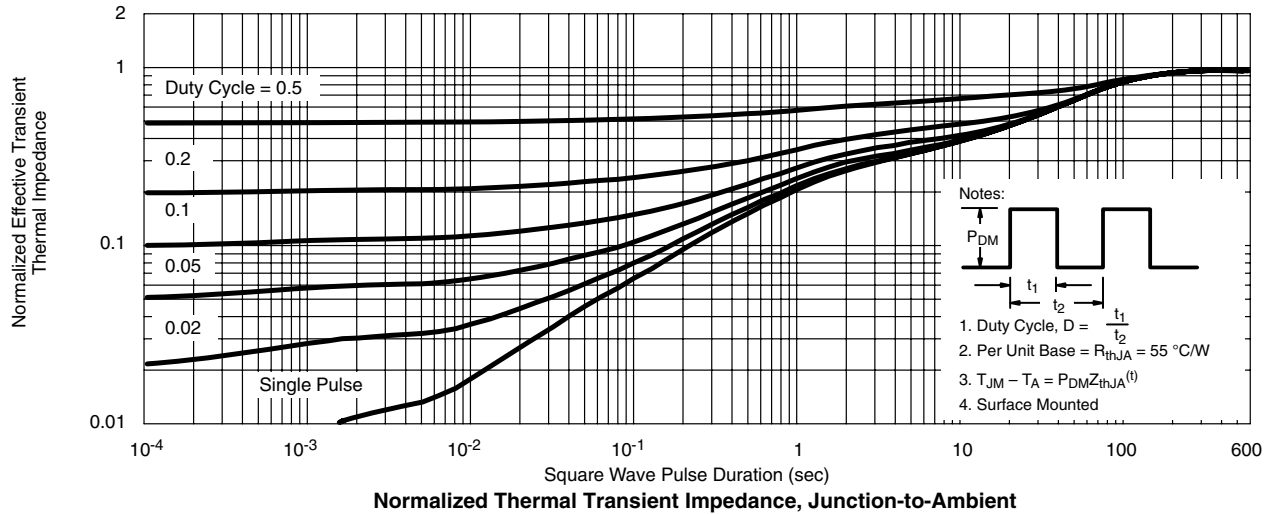
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



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