



# STL50NH3LL

N-channel 30 V - 0.011  $\Omega$  - 13 A - PowerFLAT™ (6x5)  
ultra low gate charge STripFET™ Power MOSFET

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STL50NH3LL	30V	<0.013 $\Omega$	13A <sup>(4)</sup>

- Improved die-to-footprint ratio
- Very low profile package (1 mm max)
- Very low thermal resistance
- Very low gate charge
- Low threshold device

## Applications

- Switching application

## Description

This application specific Power MOSFET is the latest generation of STMicroelectronics unique “STripFET™” technology. The resulting transistor is optimized for low on-resistance and minimal gate charge. The Chip-scaled PowerFLAT™ package allows a significant board space saving, still boosting the performance.

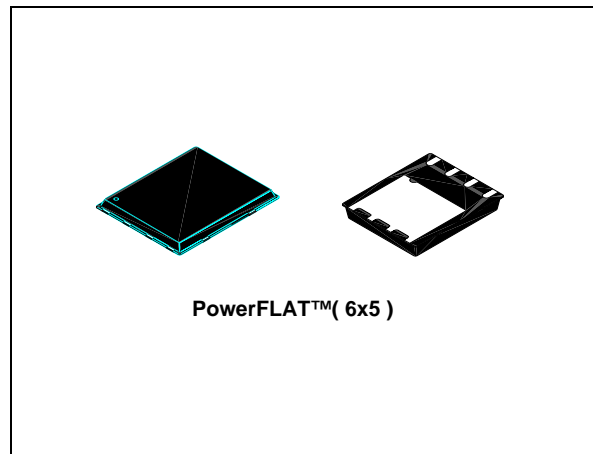


Figure 1. Internal schematic diagram

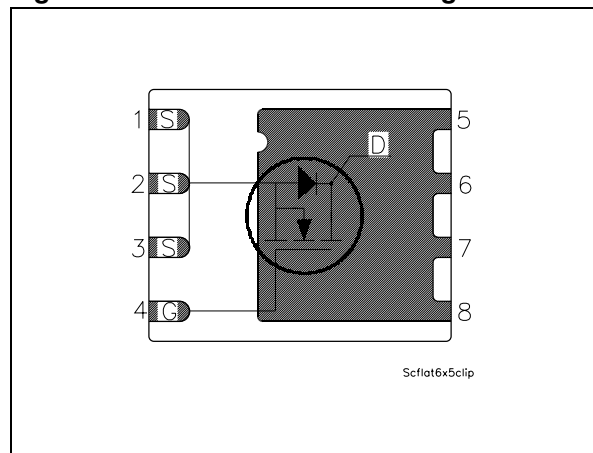


Table 1. Device summary

Order code	Marking	Package	Packaging
STL50NH3LL	L50NH3LL	PowerFLAT™ (6x5)	Tape & reel

## Contents:

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	30	V
$V_{GS}^{(1)}$	Gate-source voltage	$\pm 16$	V
$V_{GS}^{(2)}$	Gate-source voltage	$\pm 18$	V
$I_D^{(3)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	27	A
$I_D^{(4)}$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	8.1	A
$I_{DM}^{(5)}$	Drain current (pulsed)	108	A
$I_D^{(4)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	13	A
$P_{TOT}^{(4)}$	Total dissipation at $T_C = 25^\circ\text{C}$	4	W
$P_{TOT}^{(3)}$	Total dissipation at $T_C = 25^\circ\text{C}$	60	W
	Derating factor	0.03	W/ $^\circ\text{C}$
$T_J$	Operating junction temperature	-55 to 150	$^\circ\text{C}$
$T_{stg}$	Storage temperature		

1. Continuous mode
2. Guaranteed for test time  $\leq 15\text{ms}$
3. The value is rated according  $R_{thj-c}$  and is limited by wire bonding
4. The value is rated according  $R_{thj-pcb}$
5. Pulse width limited by safe operating area

**Table 3. Thermal resistance**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case (Drain)	2.08	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-ambient	31.3	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1inch<sup>2</sup>, 2oz Cu,  $t < 10\text{sec}$

**Table 4. Avalanche data**

Symbol	Parameter	Value	Unit
$I_{AV}$	Not-repetitive avalanche current	7.5	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25^\circ\text{C}$ , $I_d = I_{AV}$ )	150	mJ

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 25\ 0\mu A, V_{GS} = 0$	30			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating},$ $V_{DS} = \text{Max rating} @ 125^{\circ}C$			1 10	$\mu A$ $\mu A$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 16\ V$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu A$	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\ V, I_D = 6.5\ A$ $V_{GS} = 4.5\ V, I_D = 6.5\ A$		0.011 0.012	0.013 0.015	$\Omega$ $\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 10\ V, I_D = 6.5\ A$		32		S
$C_{iss}$	Input capacitance	$V_{DS} = 25\ V, f = 1\ MHz,$ $V_{GS} = 0$		965		pF
$C_{oss}$	Output capacitance			285		pF
$C_{rss}$	Reverse transfer capacitance			38		pF
$Q_g$	Total gate charge	$V_{DD} = 15\ V, I_D = 13\ A$ $V_{GS} = 4.5\ V$ (see Figure 8)		9	12	nC
$Q_{gs}$	Gate-source charge			3.7		nC
$Q_{gd}$	Gate-drain charge			3		nC
$R_G$	Gate input resistance	f=1 MHz gate DC bias = 0 test signal level = 20 mV open drain	0.5	1.5	2.5	$\Omega$

1. Pulsed: pulse duration=300  $\mu s$ , duty cycle 1.5%

**Table 7. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=15\text{ V}$ , $I_D=6.5\text{ A}$ , $R_G=4.7\ \Omega$ , $V_{GS}=4.5\text{ V}$ (see Figure 14)		15		ns
$t_r$	Rise time			32		ns
$t_{d(off)}$	Turn-off delay time			18		ns
$t_f$	Fall time			8.5		ns

**Table 8. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current				13	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				52	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=13\text{ A}$ , $V_{GS}=0$			1.3	V
$t_{rr}$	Reverse recovery time	$I_{SD}=13\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD}=20\text{ V}$ , $T_j=150\text{ }^\circ\text{C}$ (see Figure 16)		24		ns
$Q_{rr}$	Reverse recovery charge			17.4		nC
$I_{RRM}$	Reverse recovery current			1.45		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

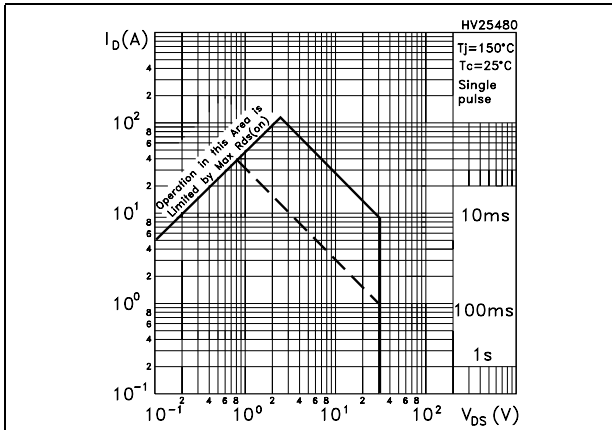


Figure 3. Thermal impedance

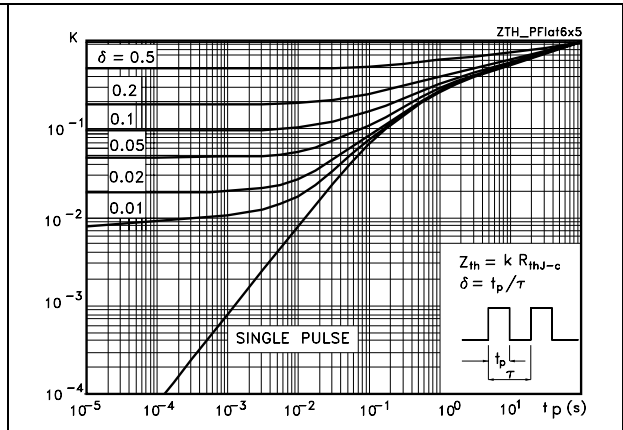


Figure 4. Output characteristics

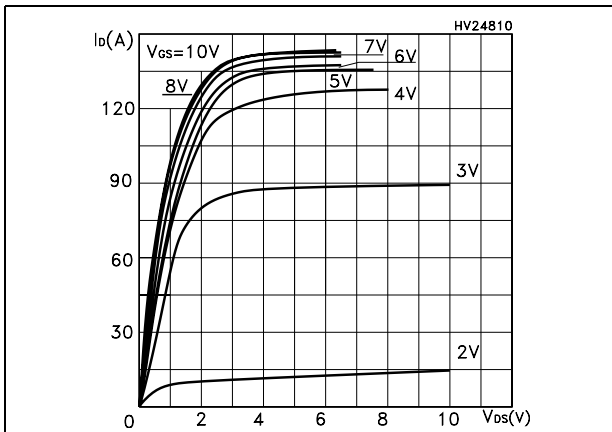


Figure 5. Transfer characteristics

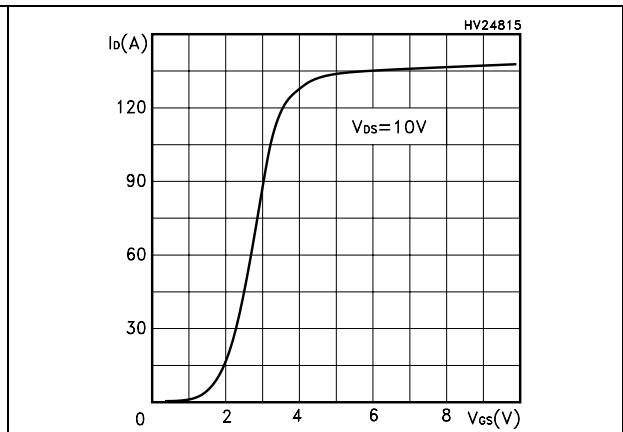


Figure 6. Transconductance

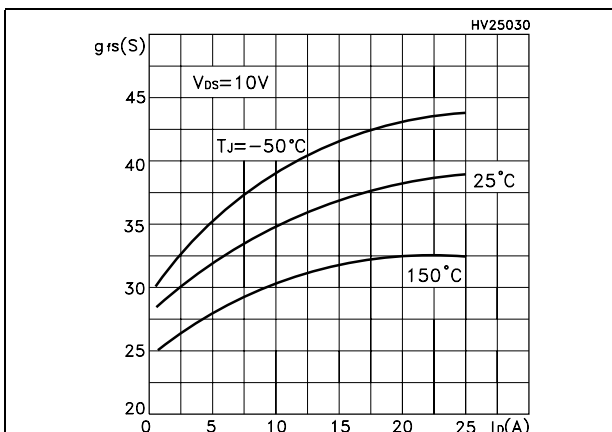


Figure 7. Static drain-source on resistance

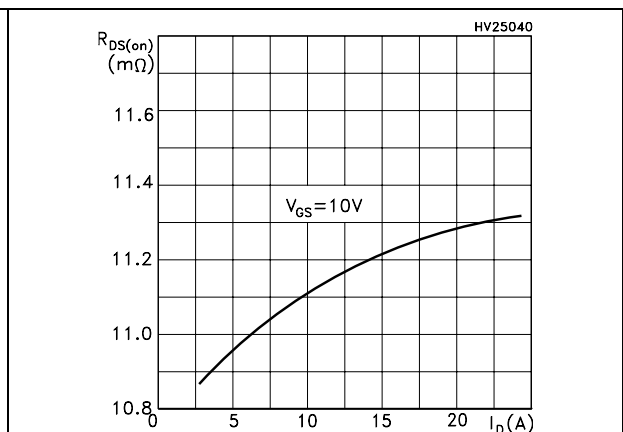


Figure 8. Gate charge vs. gate-source voltage Figure 9. Capacitance variations

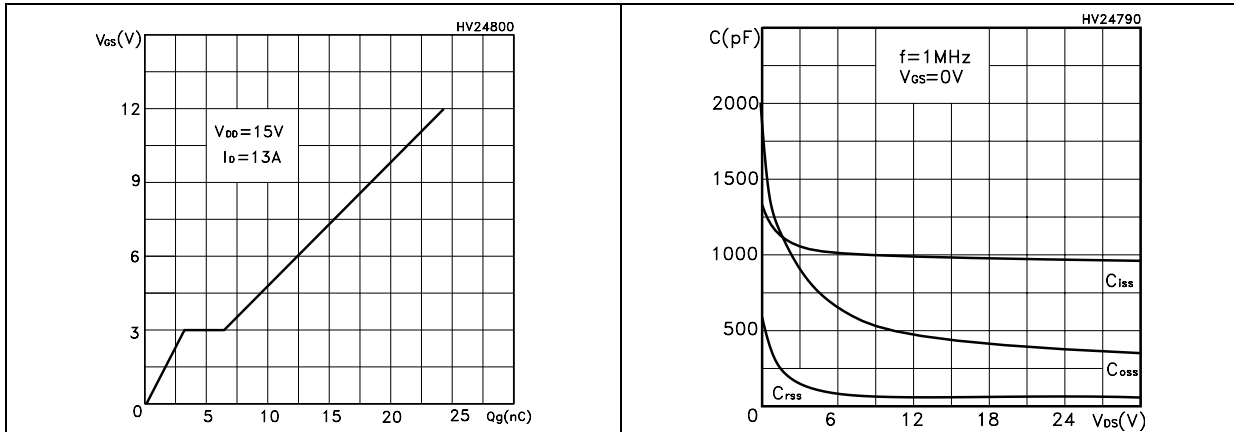


Figure 10. Normalized gate threshold voltage vs. temperature Figure 11. Normalized on resistance vs. temperature

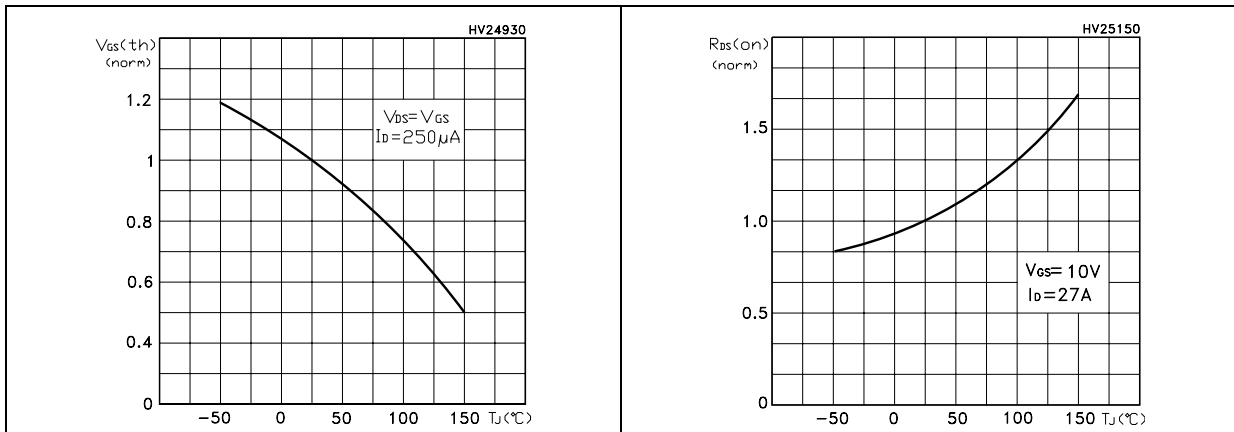
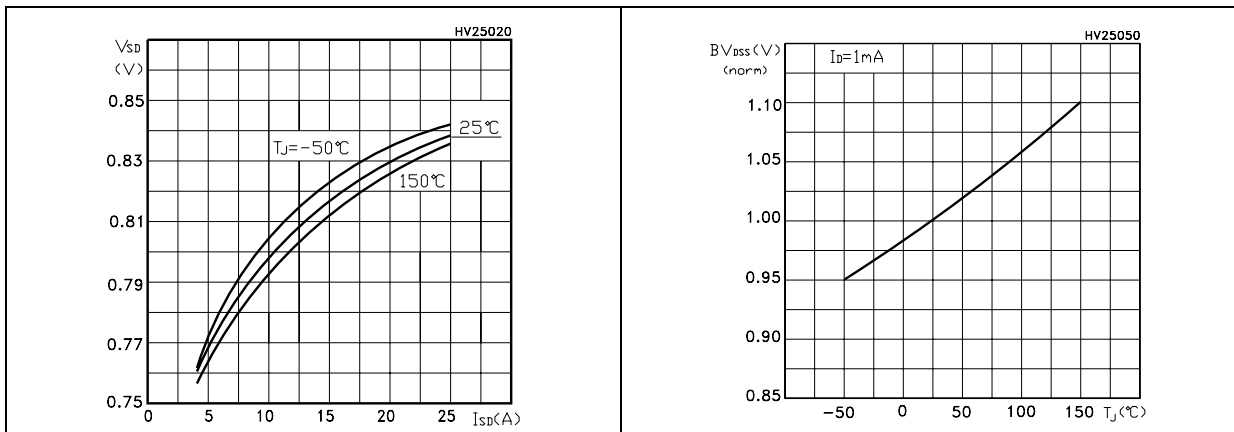


Figure 12. Source-drain diode forward characteristics Figure 13. Normalized  $B_{VDSS}$  vs. temperature



### 3 Test circuit

Figure 14. Switching times test circuit for resistive load

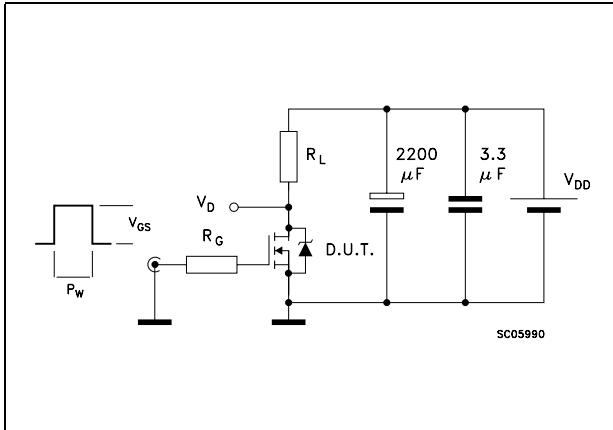


Figure 15. Gate charge test circuit

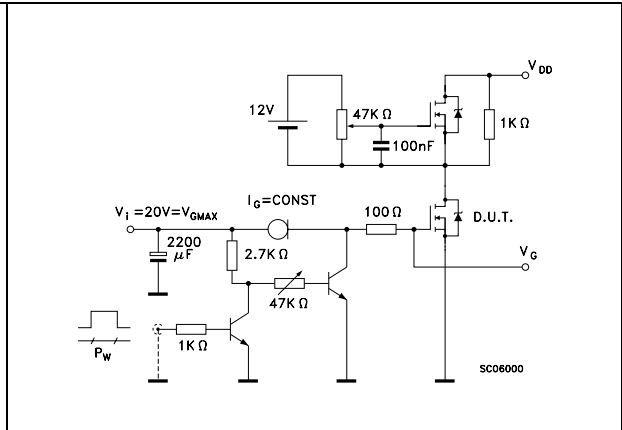


Figure 16. Test circuit for inductive load switching and diode recovery times

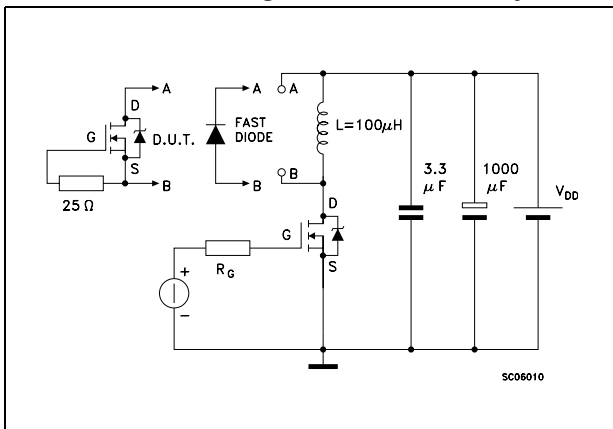


Figure 17. Unclamped inductive load test circuit

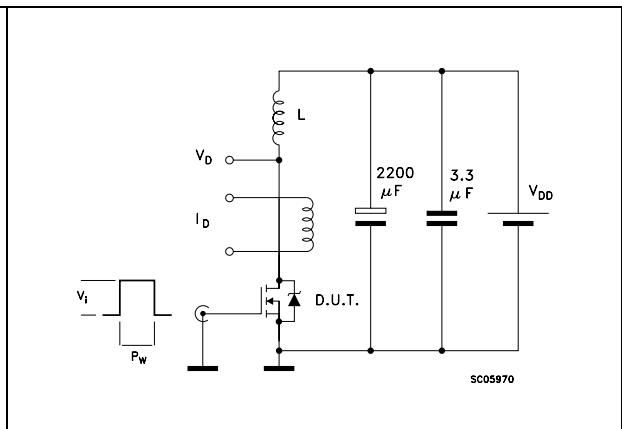


Figure 18. Unclamped inductive waveform

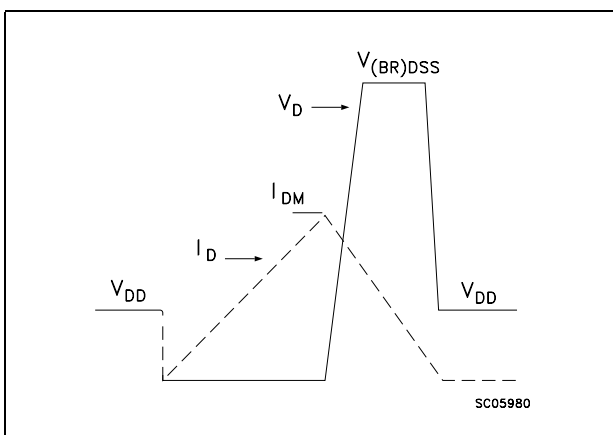
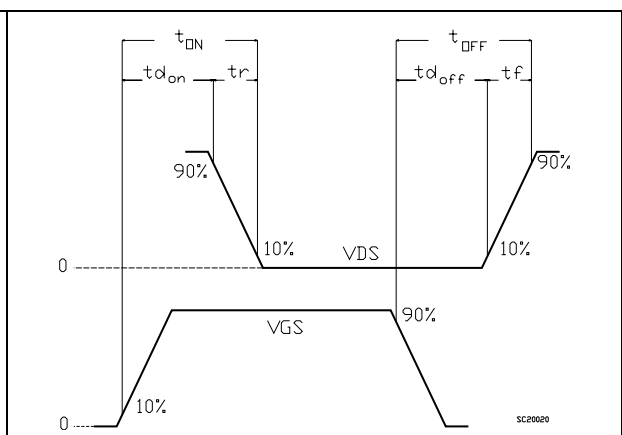


Figure 19. Switching time waveform



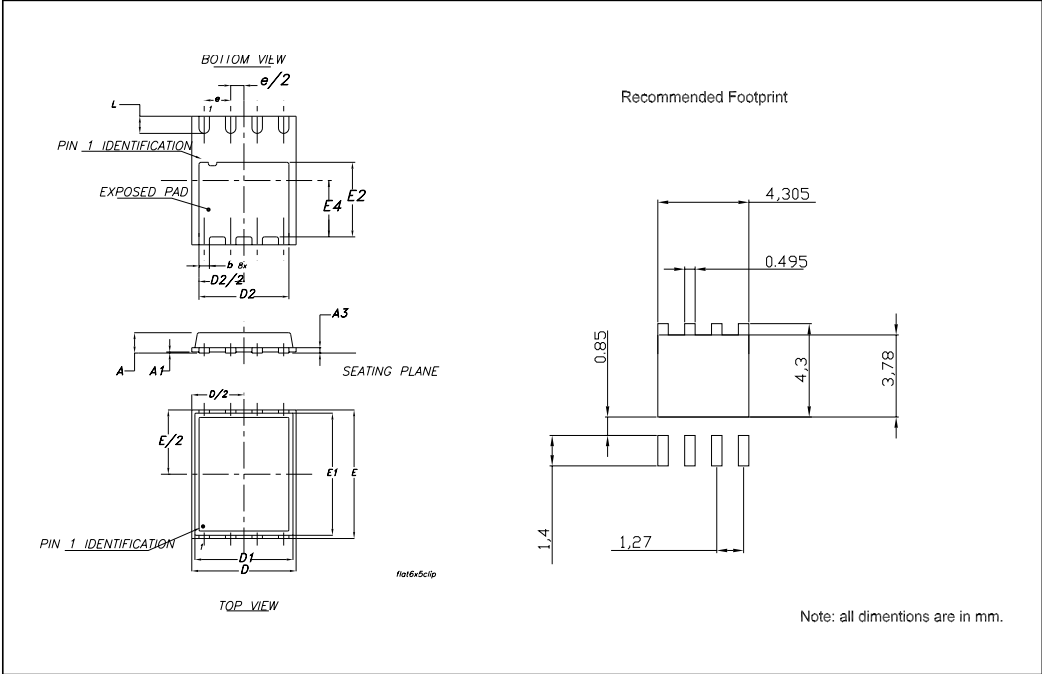


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

**PowerFLAT™ (6x5) MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	0.80	0.83	0.93	0.031	0.032	0.036
A1		0.02	0.05		0.0007	0.0019
A3		0.20			0.007	
b	0.35	0.40	0.47	0.013	0.015	0.018
D		5.00			0.196	
D1		4.75			0.187	
D2	4.15	4.20	4.25	0.163	0.165	0.167
E		6.00			0.236	
E1		5.75			0.226	
E2	3.43	3.48	3.53	0.135	0.137	0.139
E4	2.58	2.63	2.68		0.103	0.105
e		1.27			0.050	
L	0.70	0.80	0.90	0.027	0.031	0.035



## 5 Revision history

**Table 9. Revision history**

Date	Revision	Changes
21-Jul-2005	1	First Release
14-Apr-2005	2	Final version
20-Jun-2005	3	Updated mechanical data
22-Jun-2005	4	New Rg value on <a href="#">Table 7</a>
30-Sep-2005	5	Inserted ecopack indication
04-Jan-2006	6	New footprint
30-Mar-2006	7	New template
27-Jul-2006	8	Updated <a href="#">Figure 2</a>
06-Sep-2006	9	New template, no content change
11-Dec-2007	10	Updated E <sub>AS</sub> value on <a href="#">Table 4: Avalanche data</a>

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