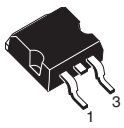
STB80PF55
STP80PF55

P-channel 55V - 0.016Ω - 80A - TO-220 - D²PAK
STripFET™ II Power MOSFET

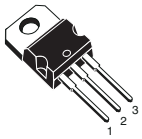
General features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STP80PF55	55V	<0.018Ω	80A
STB80PF55	55V	<0.018Ω	80A

- Extremely dv/dt capability
- 100% avalanche tested
- Application oriented characterization



D²PAK

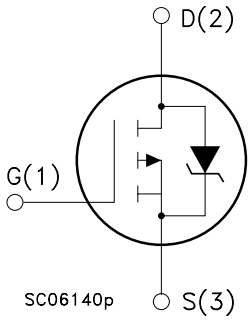


TO-220

Description

This Power MOSFET is the laest development of STMicroelectronics unique “Single feature size™”strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Internal schematic diagram



Applications

- Switching application

Order codes

Part number	Marking	Package	Packaging
STP80PF55	P80PF55	TO-220	Tube
STB80PF55	B80PF55	D²PAK	Tape & reel

Contents

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	55	V
V_{GS}	Gate-source voltage	±16	V
I_D (1)	Drain current (continuous) at T_C = 25°C	80	A
I_D	Drain current (continuous) at T_C = 100°C	57	A
I_{DM} (2)	Drain current (pulsed)	320	A
P_{TOT}	Total dissipation at T_C = 25°C	300	W
	Derating factor	2	W/°C
dv/dt (3)	Peak diode recovery voltage slope	7	V/ns
E_{AS} (4)	Single pulse avalanche energy	1.4	J
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 175	°C

1. Current limited by package
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 40A$, di/dt ≤ 300 A/µs, V_{DD}=80% $V_{(BR)DSS}$
4. Starting Tj=25°C, I_D=80A, V_{DD}=40V

Note: For the P-CHANNEL MOSFET actual polarity of voltages and current has to be reversed

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.5	°C/W
$R_{thj\text{-}a}$	Thermal resistance junction-ambient max	62.5	°C/W
T_l	Maximum lead temperature for soldering purpose	300	°C

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250mA, V_{GS} = 0	55			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating, T_C=125°C			1 10	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±16V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V, I_D = 40A		0.016	0.018	Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs}	Forward transconductance	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$, I_D= 40A		32		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25V, f = 1MHz, V_{GS} = 0		5500 1130 600		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	I_D = 25A, V_{DD} = 80V, V_{GS} = 10V *(see Figure 14)*		190 27 65	258	nC nC nC

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD}=25V, I_D=40A, R_G=4.7Ω, V_{GS}=10V *(see Figure 13)*		35 190		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	V_{DD}=25V, I_D=40A, R_G=4.7Ω, V_{GS}=10V *(see Figure 13)*		165 80		ns ns
$t_{r(Voff)}$ t_f t_c	Off-voltage rise time Fall time Cross-over time	V_{clamp}=40V, I_D=80A, R_G=4.7Ω, V_{GS}=10V *(see Figure 13)*		60 40 85		ns ns ns

Table 6. Source drain diode

Symbol	Parameter	Test condictions	Min	Typ.	Max	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				10 40	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 80A, V_{GS} = 0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 80A, di/dt = 100A/µs V_{DD} = 25V, T_j =150°C		110 495 9		ns µC A

1. Pulse width limited by Tjmax
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5 %

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for TO-220

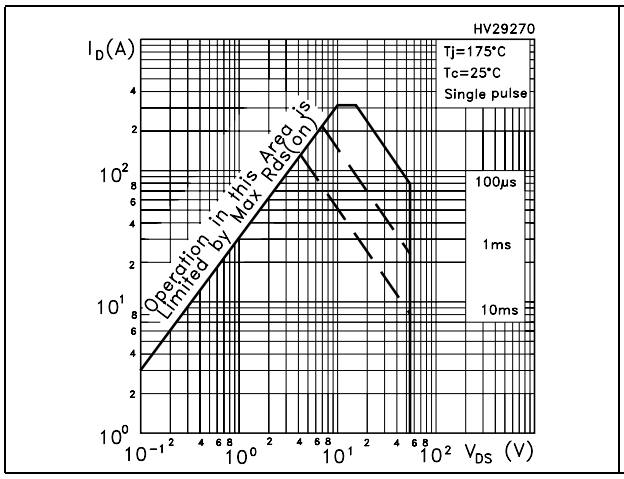


Figure 2. Thermal impedance for TO-220

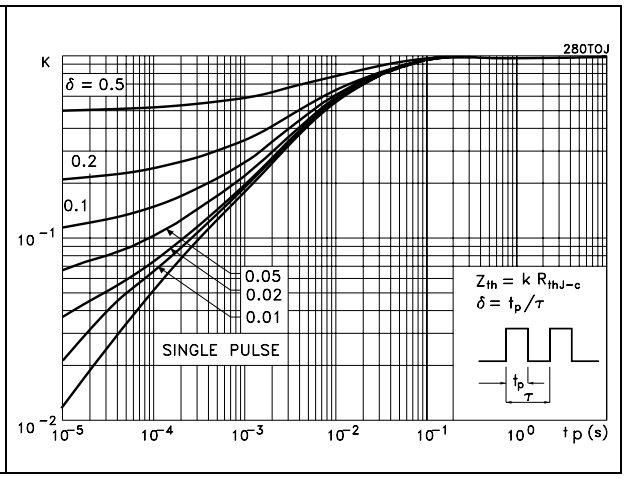


Figure 3. Output characterisics

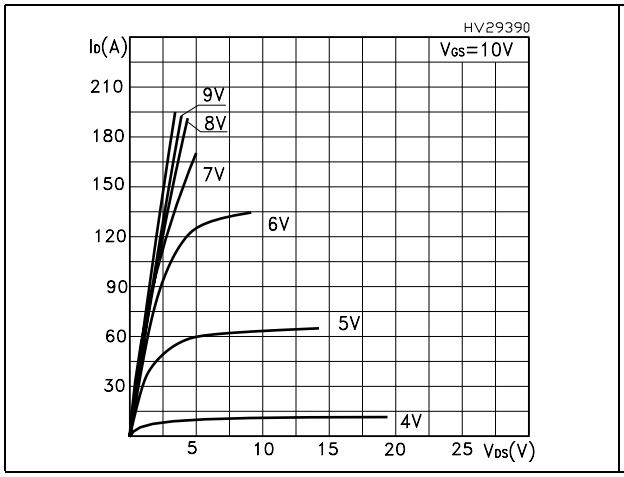


Figure 4. Transfer characteristics

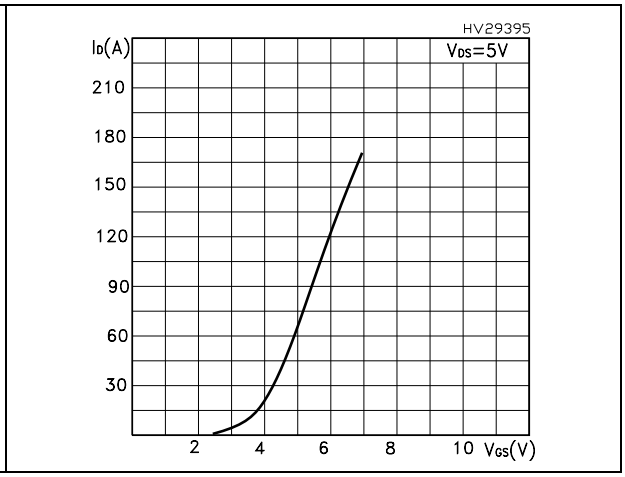


Figure 5. Transconductance

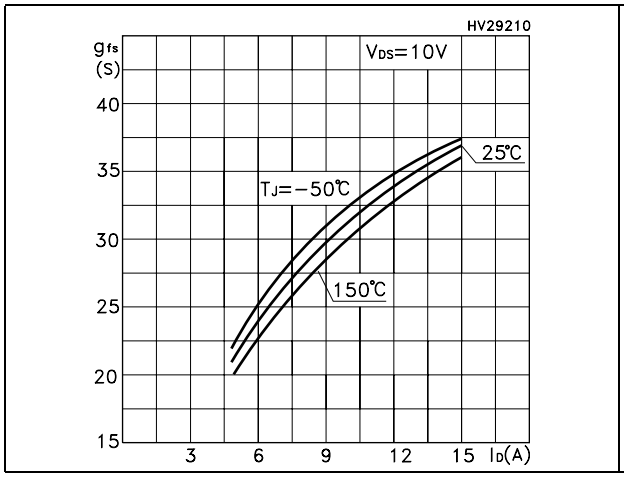


Figure 6. Static drain-source on resistance

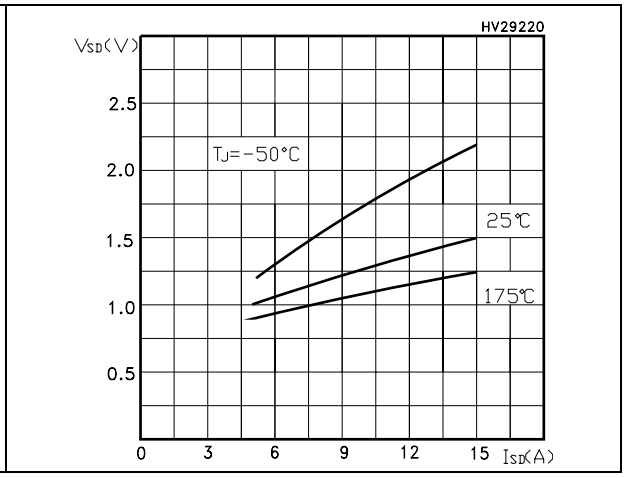


Figure 7. Gate charge vs gate-source voltage

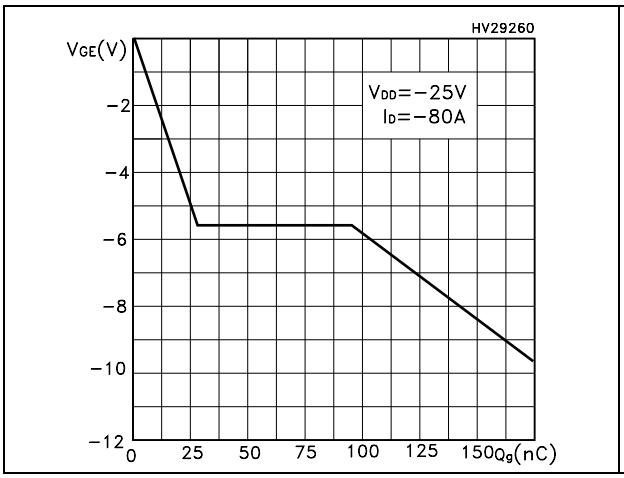


Figure 8. Capacitance variations

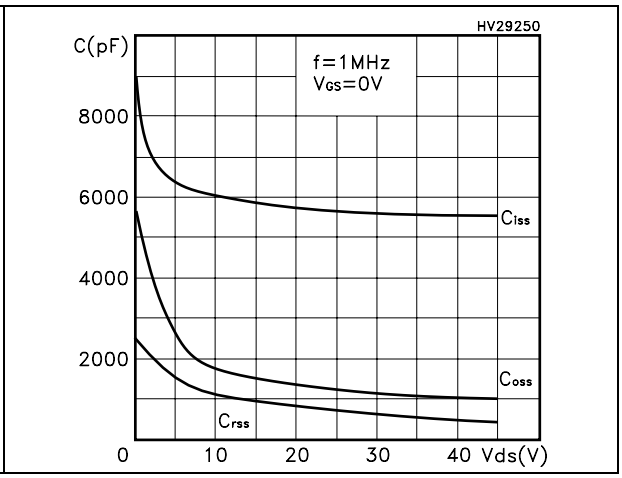


Figure 9. Normalized gate threshold voltage vs temperature

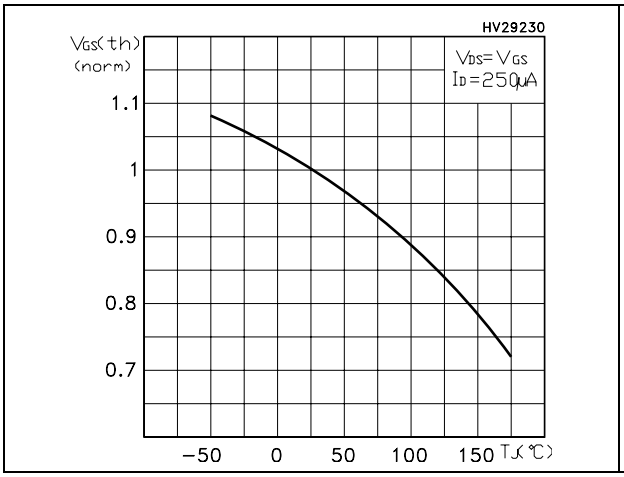


Figure 10. Normalized on resistance vs temperature

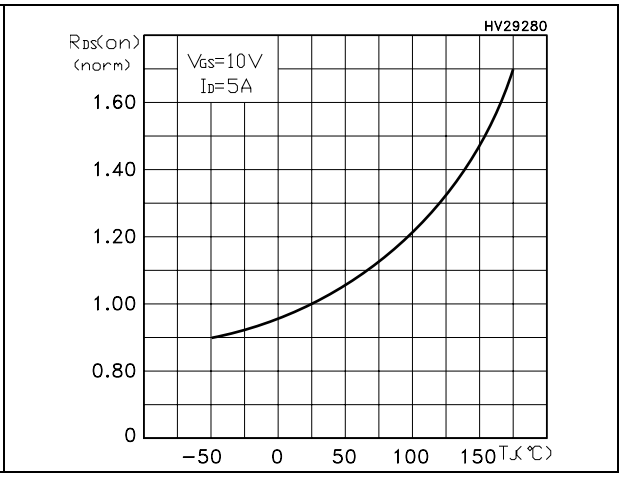


Figure 11. Source-drain diode forward characteristics

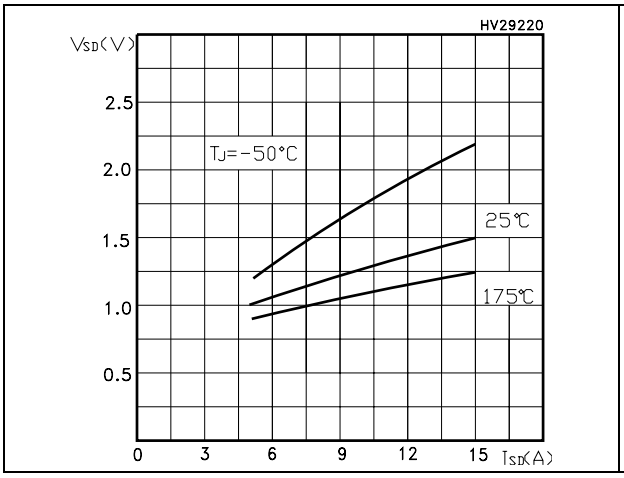
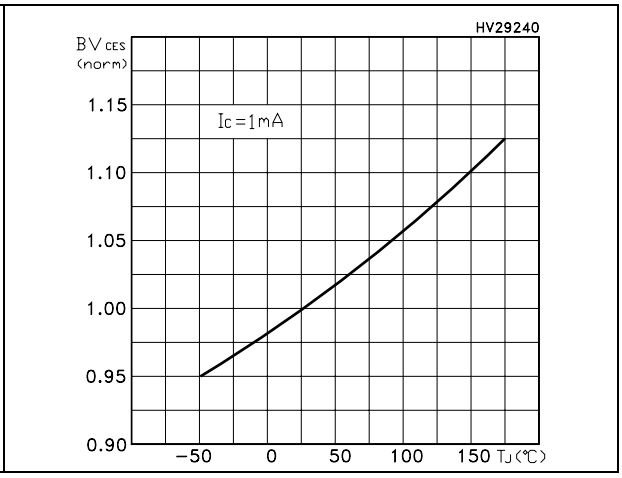


Figure 12. Normalized B_{VDSS} vs temperature



3 Test circuit

Figure 13. Switching times test circuit for resistive load

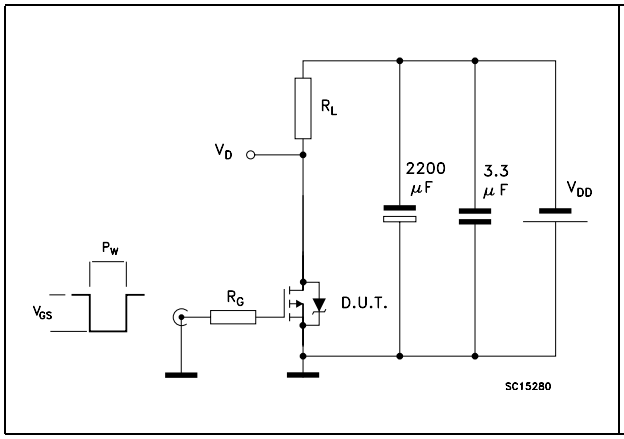


Figure 14. Gate charge test circuit

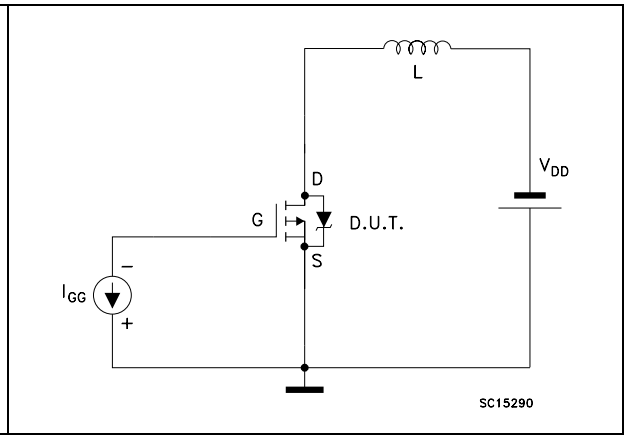
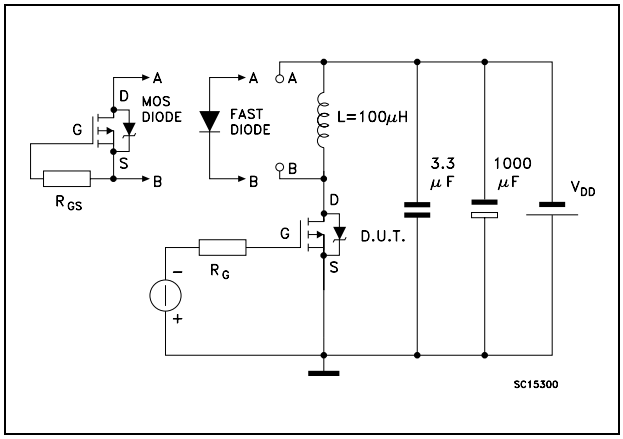


Figure 15. Test circuit for inductive load switching and diode recovery times

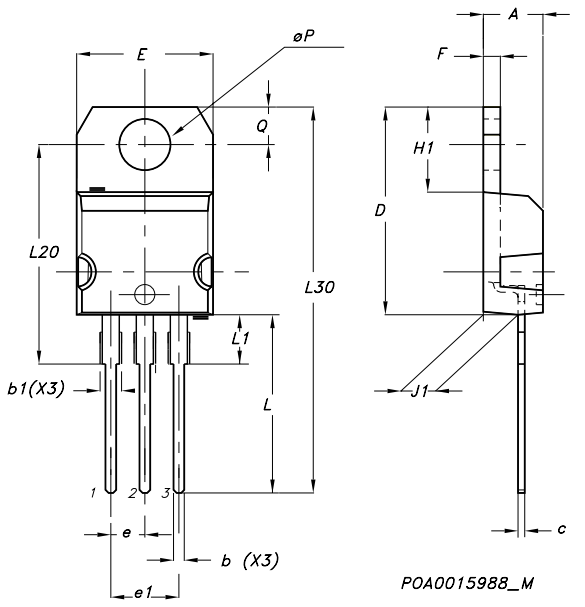


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

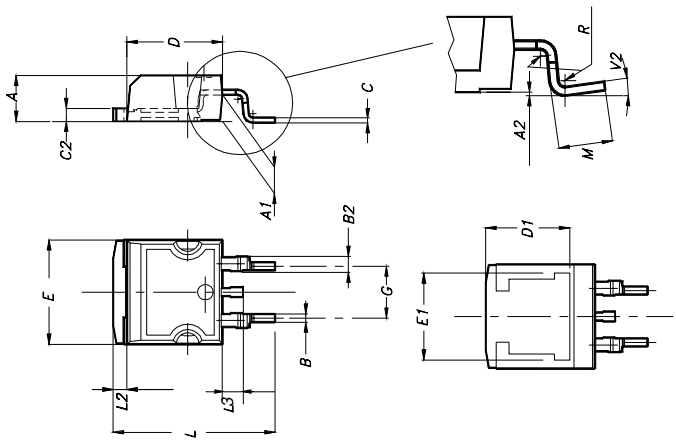
TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0º		4º			



5 Revision history

Table 7. Revision history

Date	Revision	Changes
09-Sep-2004	4	Revalidation
12-Sep-2006	5	New template, D^2PAK added

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