



STS8C5H30L

N-channel 30V - 0.018 Ω - 8A/p-channel 30V - 0.045 Ω - 5A - SO-8
 Low gate charge STripFET™ III MOSFET

Features

Type	V _{DSS}	R _{DS(on)}	I _D
STS8C5H30L(N-channel)	30V	<0.022	8A
STS8C5H30L(P-channel)	30V	<0.056	5A

- Conduction losses reduced
- Switching losses reduced
- Low threshold drive
- Standard outline for easy automated surface mount assembly

Description

This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Application

- Switching application

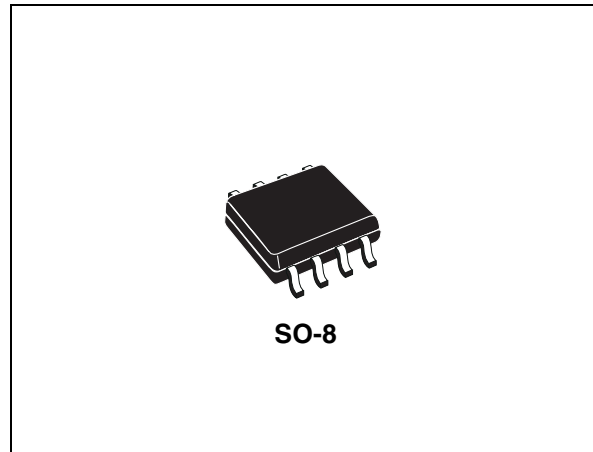


Figure 1. Internal schematic diagram

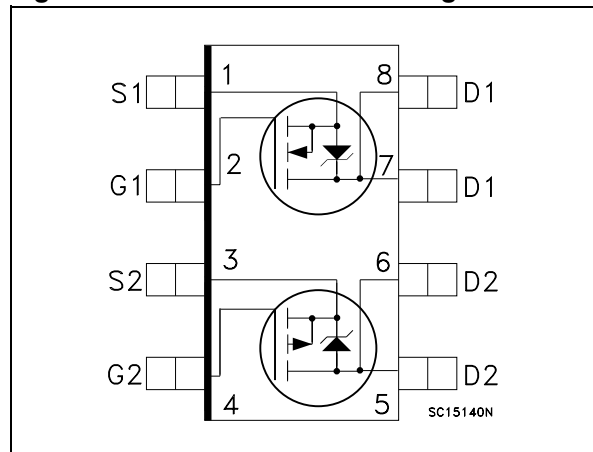


Table 1. Device summary

Part number	Marking	Package	Packaging
STS8C5H30L	S8C5H30L	SO-8	Tape & reel

Note: For the P-channel MOSFET actual polarity of voltages and current has to be reversed

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		N-channel	P-channel	
V_{DS}	Drain-source voltage ($v_{gs} = 0$)	30		V
V_{GS}	Gate- source voltage	± 16	± 16	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$ single operating	8	4.2	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$ single operating	6.4	3.1	A
$I_{DM}^{(1)}$	Drain current (pulsed)	32	16.8	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$ dual operating	1.6		W
	Total dissipation at $T_C = 25^\circ\text{C}$ single operating	2		W
T_{stg}	Storage temperature	-55 to 150		$^\circ\text{C}$
T_j	Operating junction temperature	150		$^\circ\text{C}$

1. Pulse width limited by safe operating area

Table 3. Thermal data

R_{thj-a}	Thermal resistance junction-ambient single operating	62.5	$^\circ\text{C}/\text{W}$
	Thermal resistance junction-ambient dual operating	78	$^\circ\text{C}/\text{W}$
T_l	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

Note: For the P-channel MOSFET actual polarity of voltages and current has to be reversed

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	$I_D = 250 \mu A, V_{GS} = 0$	n-ch	30			V
			p-ch	30			V
I_{DSS}	Zero gate voltage Drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating},$ $T_C = 125^{\circ}C$	n-ch			1	μA
			p-ch			10	μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 16V$ $V_{GS} = \pm 16V$	n-ch			± 100	nA
			p-ch			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	n-ch	1			V
			p-ch	1	1.6	2.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 4A$ $V_{GS} = 10V, I_D = 2.5A$ $V_{GS} = 4.5V, I_D = 4A$ $V_{GS} = 4.5V, I_D = 2.5A$	n-ch		0.018	0.022	Ω
			p-ch		0.045	0.055	Ω
			n-ch		0.020	0.025	Ω
			p-ch		0.070	0.075	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15V, I_D = 4A$ $V_{DS} = 15V, I_D = 2.5A$	n-ch		8.5		S
			p-ch		10		S
C_{iss}	Input capacitance		n-ch		857		pF
			p-ch		1350		pF
C_{oss}	Output capacitance	$V_{DS} = 25V, f = 1 \text{ MHz},$ $V_{GS} = 0$	n-ch		147		pF
			p-ch		490		pF
C_{rss}	Reverse transfer capacitance		n-ch		20		pF
			p-ch		130		pF
Q_g	Total gate charge	N-channel $V_{DD} = 24V, I_D = 8A$ $V_{GS} = 5V$	n-ch		7	10	nC
			p-ch		12.5	16	nC
Q_{gs}	Gate-source charge	P-channel $V_{DD} = 24V, I_D = 4A$ $V_{GS} = 5V$	n-ch		2.5		nC
			p-ch		5		nC
Q_{gd}	Gate-drain charge	$V_{GS} = 5V$ <i>(see Figure 27)</i>	n-ch		2.3		nC
			p-ch		3		nC

1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5.

Note: For the P-channel MOSFET actual polarity of voltages and current has to be reversed

Table 6. Switching times

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time	N-channel $V_{DD} = 15V, I_D = 4A$ $R_G=4.7 \Omega, V_{GS} = 4.5V$	n-ch		12		ns
			p-ch		25		ns
	Rise time	P-channel $V_{DD} = 15V, I_D = 2A$ $R_G=4.7 \Omega, V_{GS} = 4.5V$ <i>(see Figure 26)</i>	n-ch		14.5		ns
			p-ch		35		ns
$t_{d(off)}$ t_f	Turn-off delay time	N-channel $V_{DD} = 15V, I_D = 4A$ $R_G=4.7 \Omega, V_{GS} = 4.5V$	n-ch		23		ns
			p-ch		125		ns
	Fall time	P-channel $V_{DD} = 15V, I_D = 2A$ $R_G=4.7 \Omega, V_{GS} = 4.5V$ <i>(see Figure 26)</i>	n-ch		8		ns
			p-ch		35		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions		Min	Typ.	Max	Unit
I_{SD}	Source-drain current		n-ch			8	A
			p-ch			5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		n-ch			32	A
			p-ch			20	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 8A, V_{GS} = 0$	n-ch			1.5	V
		$I_{SD} = 5A, V_{GS} = 0$	p-ch			1.2	V
t_{rr}	Reverse recovery time	N-channel $I_{SD} = 8A, di/dt = 100A/\mu s$ $V_{DD}=15V, T_j = 150^\circ C$	n-ch		15		ns
			p-ch		45		ns
Q_{rr}	Reverse recovery charge	P-channel $I_{SD} = 5A, di/dt = 100A/\mu s$ $V_{DD}=15V, T_j = 150^\circ C$ <i>(see Figure 28)</i>	n-ch		5.7		nC
			p-ch		36		nC
I_{RRM}	Reverse recovery current	<i>(see Figure 28)</i>	n-ch		0.76		A
			p-ch		1.6		A

1. Pulse width limited by safe operating area.

2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area n-ch

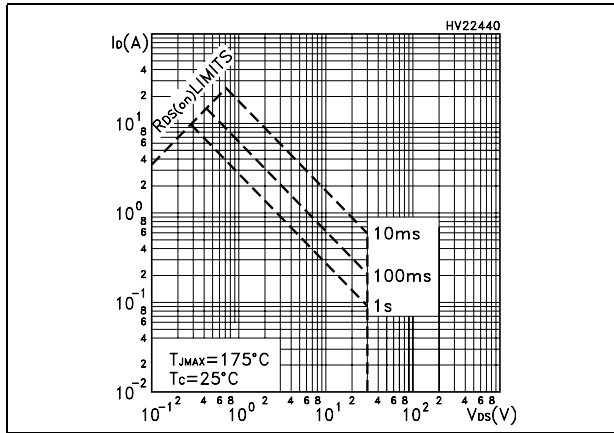


Figure 3. Thermal impedance n-ch

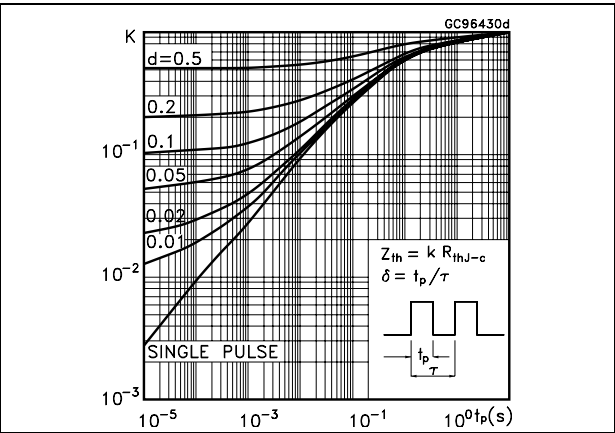


Figure 4. Output characteristics n-ch

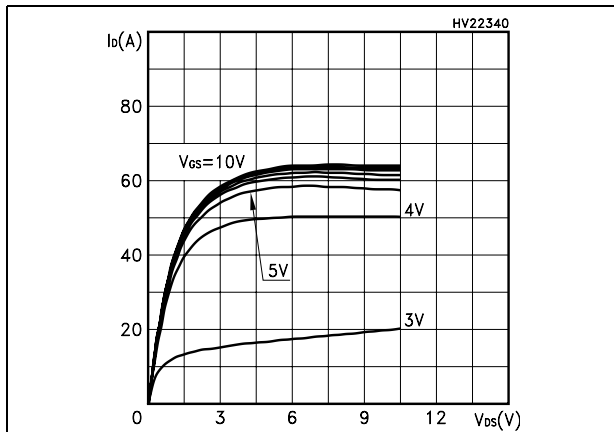


Figure 5. Transfer characteristics n-ch

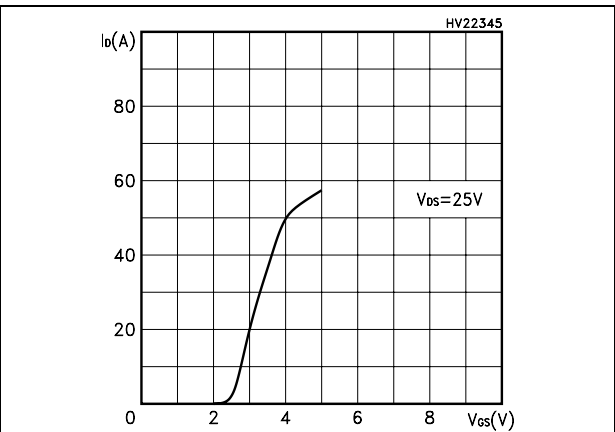


Figure 6. Transconductance n-ch

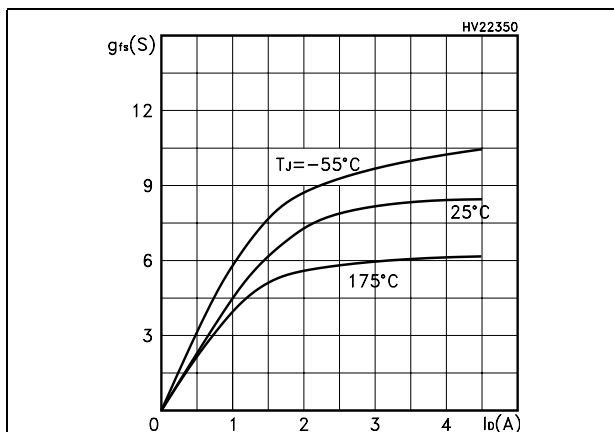


Figure 7. Static drain-source on resistance n-ch

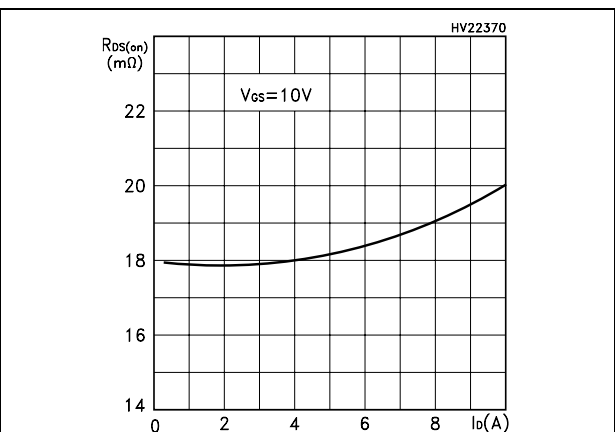


Figure 8. Gate charge vs. gate-source voltage Figure 9. Capacitance variations n-ch n-ch

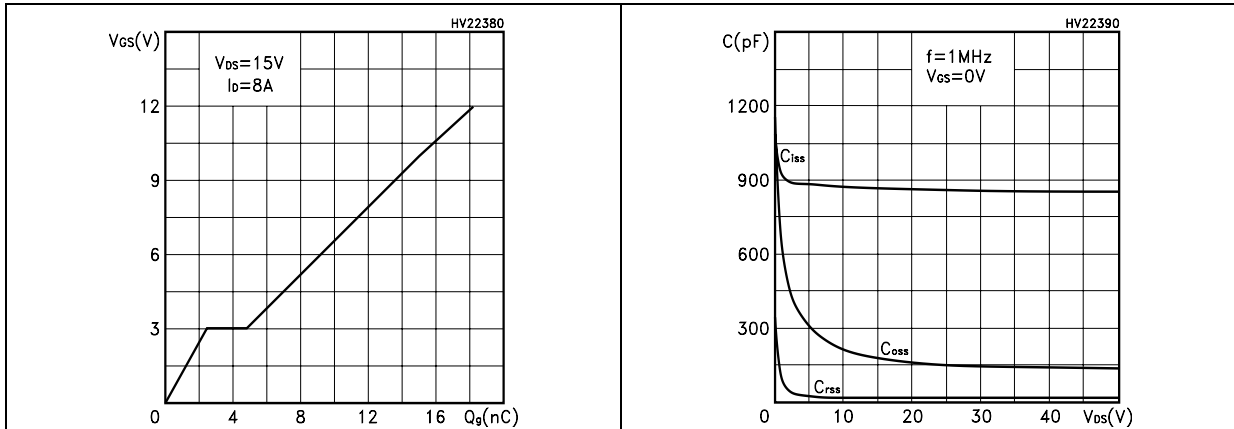


Figure 10. Normalized gate threshold voltage vs. temperature n-ch Figure 11. Normalized on resistance vs. temperature n-ch

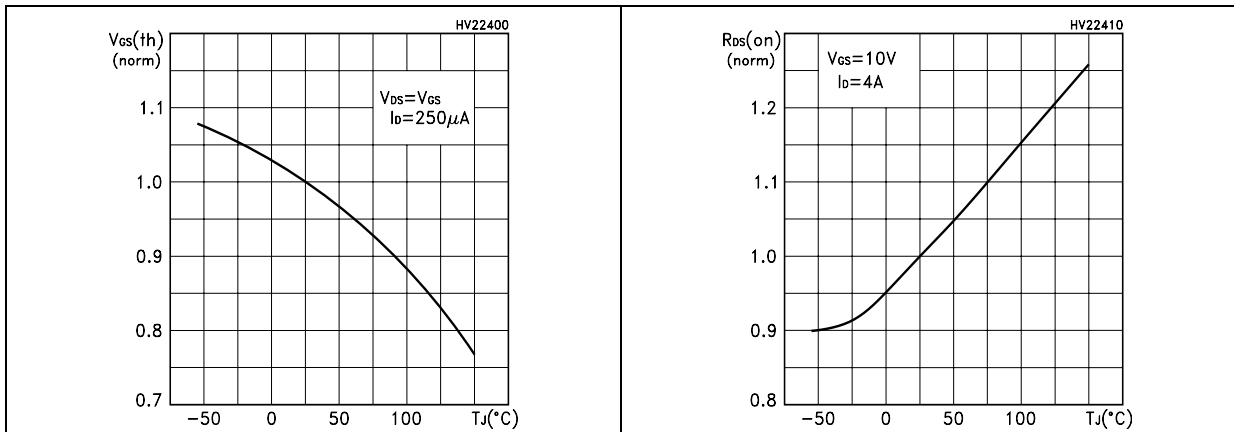


Figure 12. Source-drain diode forward characteristics n-ch Figure 13. Normalized breakdown voltage vs. temperature n-ch

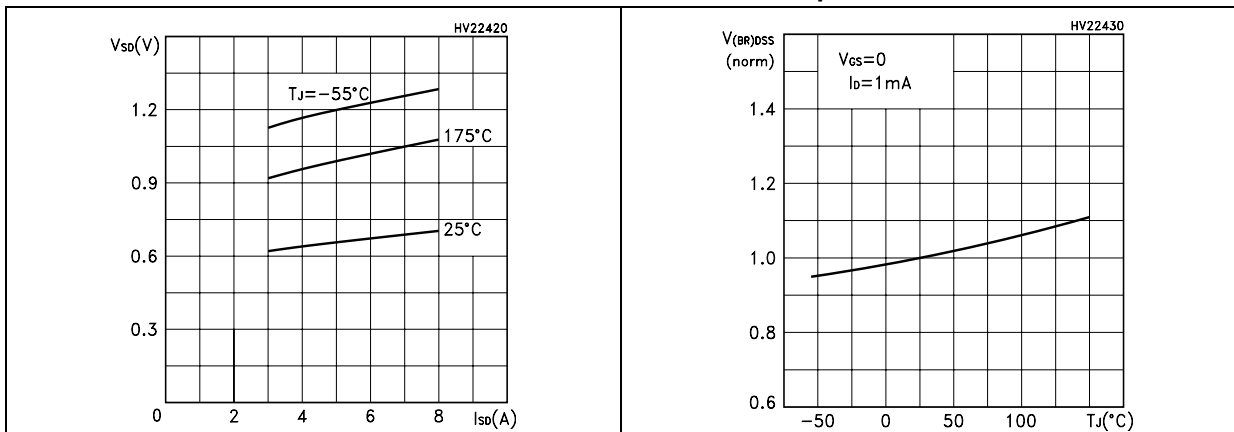


Figure 14. Safe operating area p-ch

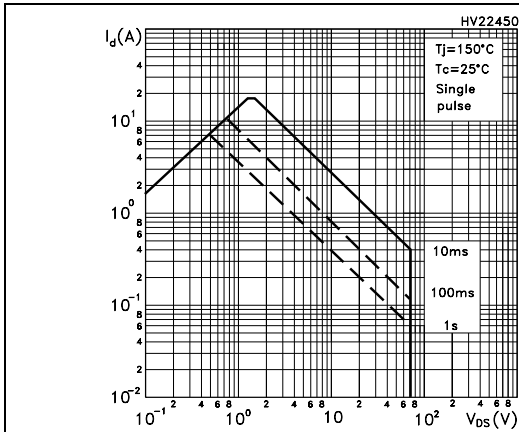


Figure 15. Thermal impedance p-ch

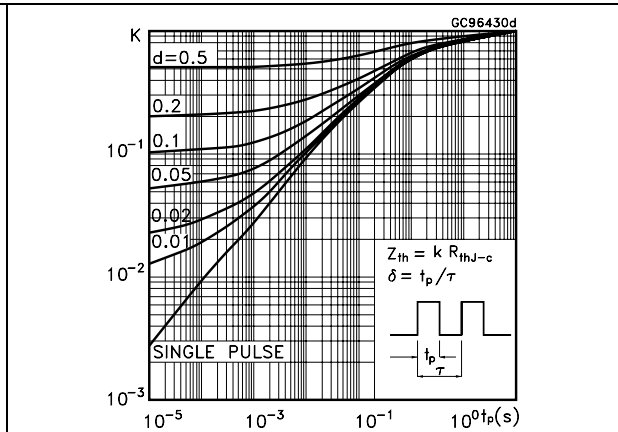


Figure 16. Output characteristics p-ch

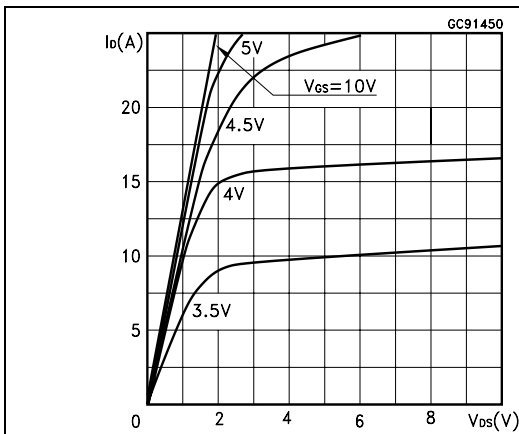


Figure 17. Transfer characteristics p-ch

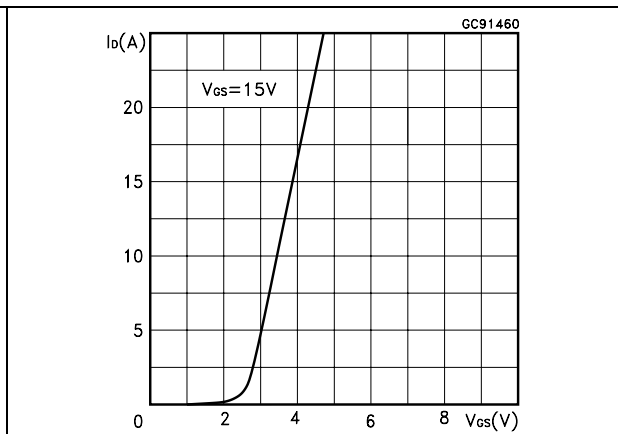


Figure 18. Transconductance p-ch

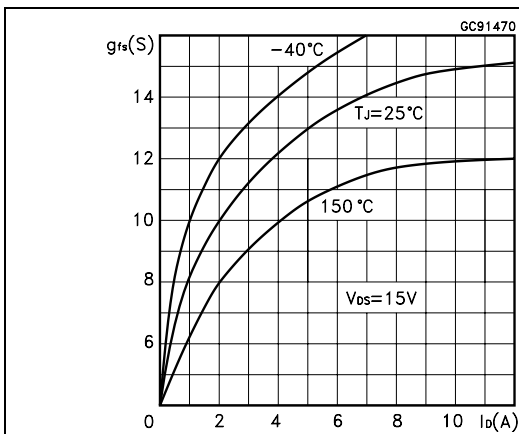


Figure 19. Static drain-source on resistance p-ch

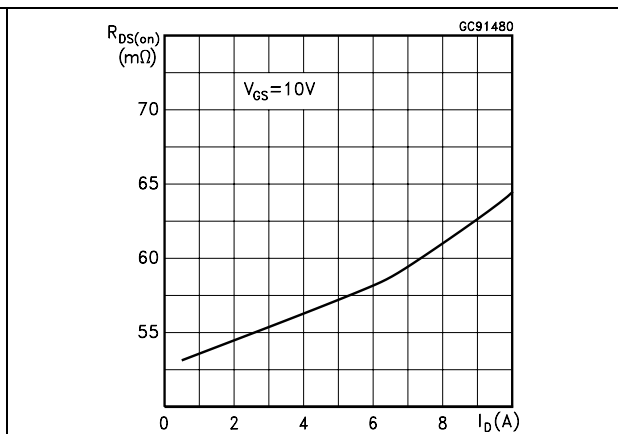


Figure 20. Gate charge vs. gate-source voltage Figure 21. Capacitance variations p-ch

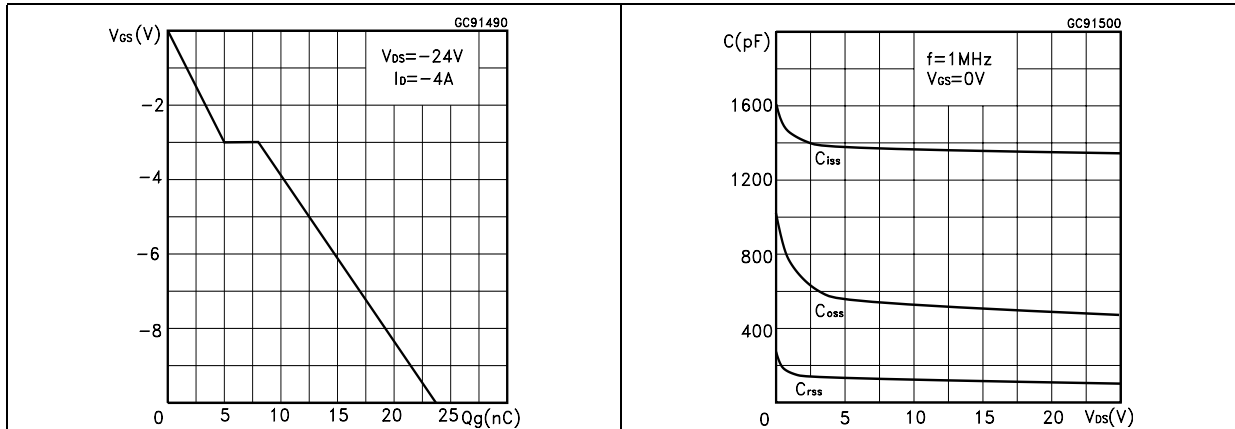


Figure 22. Normalized gate threshold voltage vs. temperature p-ch Figure 23. Normalized on resistance vs. temperature p-ch

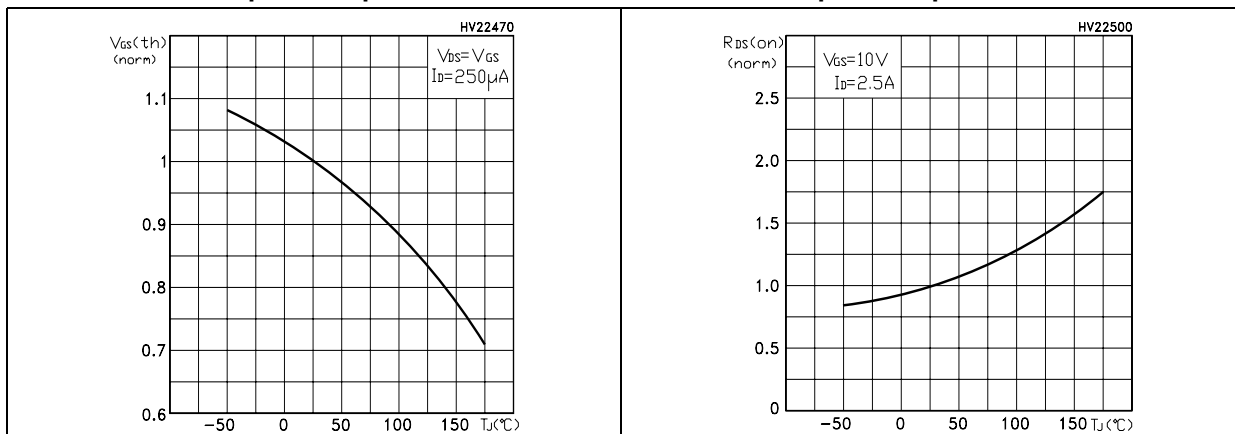
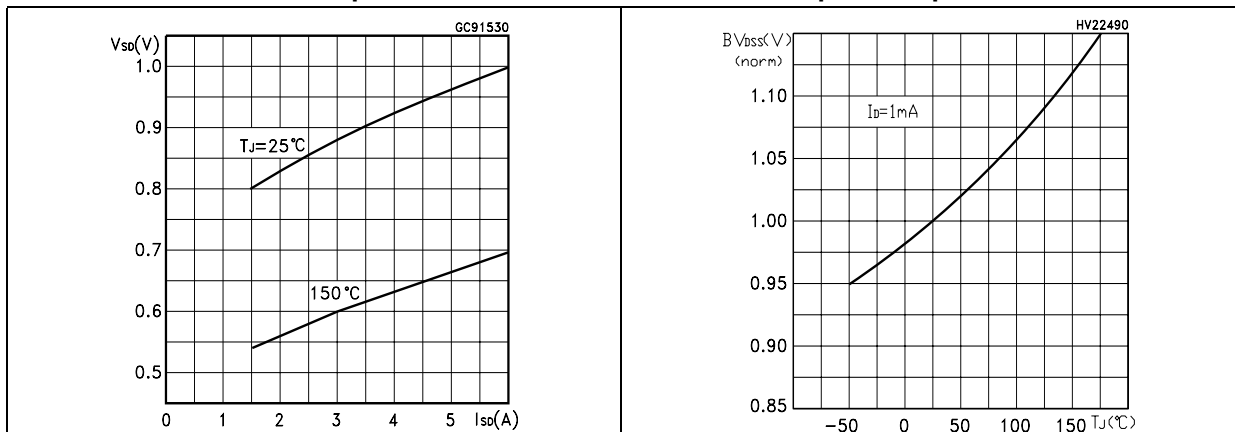


Figure 24. Source-drain diode forward characteristics p-ch Figure 25. Normalized breakdown voltage vs. temperature p-ch



3 Test circuit

Figure 26. Switching times test circuit for resistive load

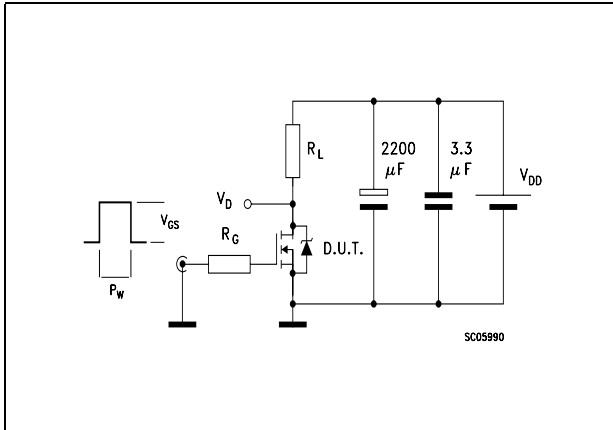


Figure 27. Gate charge test circuit

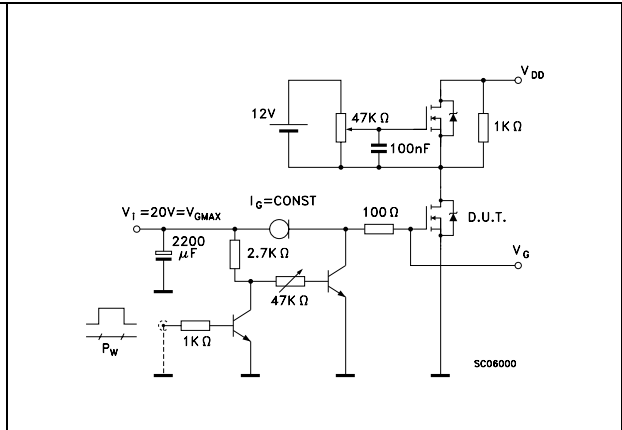


Figure 28. Test circuit for inductive load switching and diode recovery times

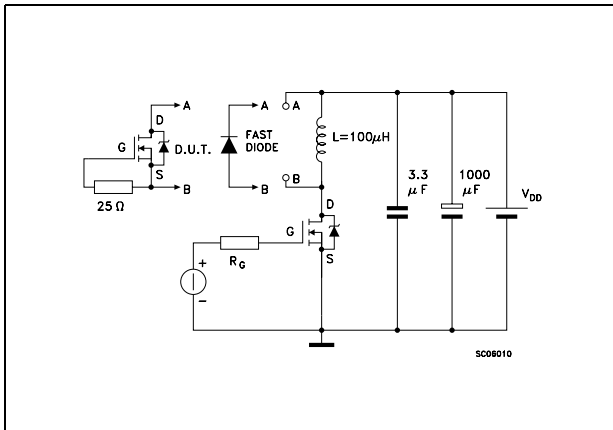


Figure 29. Unclamped Inductive load test circuit

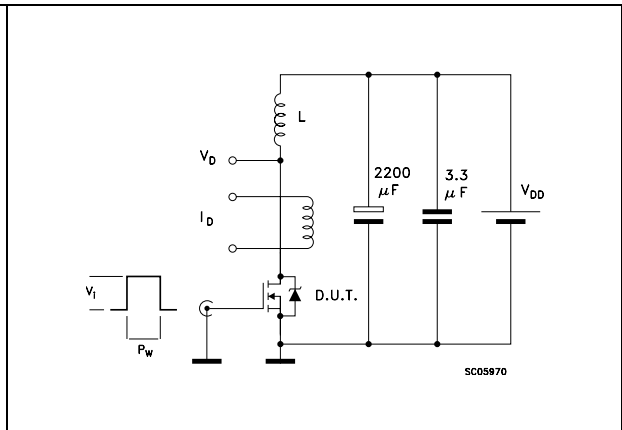


Figure 30. Unclamped inductive waveform

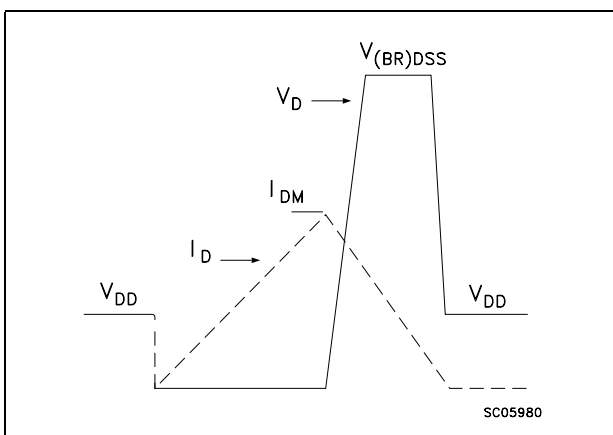
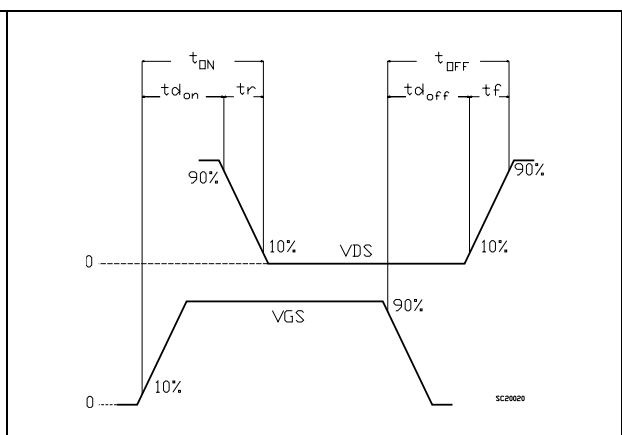


Figure 31. Switching time waveform

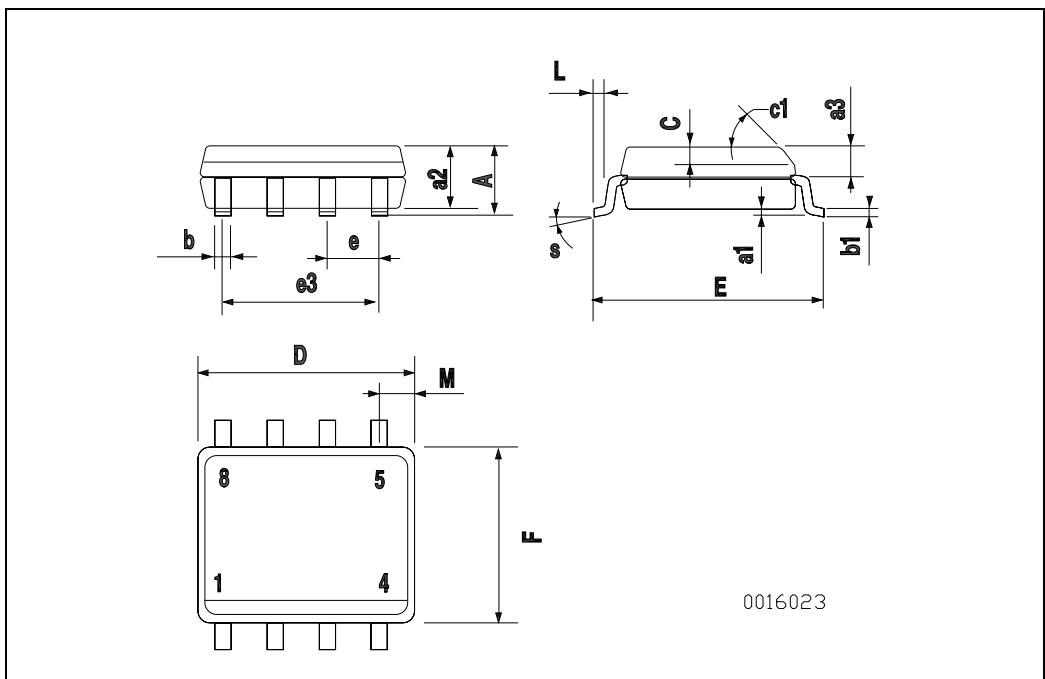


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



5 Revision history

Table 8. Revision history

Date	Revision	Changes
17-Sep-2004	1	First revision
31-Oct-2006	2	The document has been reformatted
30-Jan-2007	3	typo mistake on Table 2 .
23-Jul-2007	4	Figure 14 has been updated

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