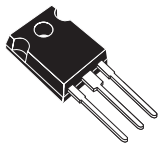
# STW45NM50FD

## N-channel 500V - 0.07Ω - 45A - TO247
## FDmesh™ Power MOSFET (with fast diode)

## General features

| Type | $V_{DSS}$ | $R_{DS(on)}$ | $I_D$ |
|---|---|---|---|
| STW45NM50FD | 500V | <0.1Ω | 45A |

- 100% avalanche tested
- High dv/dt and avalanche capabilities
- Low input capacitance and gate charge
- Low gate input resistance
- Tight process control and high manufacturing yields

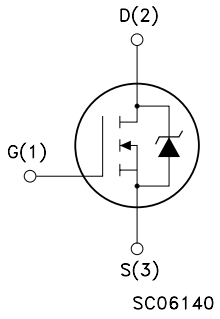


TO-247

## Description

The FDmesh™ associates all advantages of reduced on-resistance and fast switching with an intrinsic fast-recovery body diode. It is therefore strongly recommended for bridge topologies, in particular ZVS phase-shift converters.

## Internal schematic diagram




## Applications

- Switching application

## Order codes

| Part number | Marking | Package | Packaging |
|---|---|---|---|
| STW45NM50FD | W45NM50FD | TO-247 | Tube |

# Contents

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain-source voltage ($V_{GS}$ = 0) | 500 | V |
| $V_{DGR}$ | Drain-gate voltage ($R_{GS}$ = 20KΩ) | 500 | V |
| $V_{GS}$ | Gate-source voltage | ± 30 | V |
| $I_D$ | Drain current (continuous) at $T_C$ = 25°C | 45 | A |
| $I_D$ | Drain current (continuous) at $T_C$=100°C | 28.4 | A |
| $I_{DM}$(1) | Drain current (pulsed) | 180 | A |
| $P_{TOT}$ | Total dissipation at $T_C$ = 25°C | 417 | W |
| | Derating factor | 2.08 | W/°C |
| dv/dt(2) | Peak diode recovery voltage slope | 20 | V/ns |
| $T_J$<br>$T_{stg}$ | Operating junction temperature<br>Storage temperature | -65 to 150 | °C |

1. Pulse width limited by safe operating area
2. $I_{SD}$ ≤45A, di/dt ≤400A/µs, $V_{DD}$ =80%$V_{(BR)DSS}$

**Table 2. Thermal resistance**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thj\text{-}case}$ | Thermal resistance junction-case Max | 0.3 | °C/W |
| $R_{thj\text{-}a}$ | Thermal resistance junction-ambient Max | 30 | °C/W |
| $T_l$ | Maximum lead temperature for soldering purpose | 300 | °C |

**Table 3. Avalanche data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $I_{AR}$ | Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max) | 22.5 | A |
| $E_{AS}$ | Single pulse avalanche energy (starting Tj=25°C, Id=Iar, Vdd=50V) | 800 | mJ |

# 2 Electrical characteristics

($T_{CASE}$=25°C unless otherwise specified)

**Table 4. On/off states**

| Symbol | Parameter | Test condictions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $I_D$ = 250µA, $V_{GS}$= 0 | 500 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current ($V_{GS}$ = 0) | $V_{DS}$ = Max rating,<br>$V_{DS}$ = Max rating @125°C | | | 10<br>100 | µA<br>µA |
| $I_{GSS}$ | Gate body leakage current ($V_{DS}$ = 0) | $V_{GS}$ = ±30V | | | ±100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$= $V_{GS}$, $I_D$ = 250µA | 3 | 4 | 5 | V |
| $R_{DS(on)}$ | Static drain-source on resistance | $V_{GS}$= 10V, $I_D$= 22.5A | | 0.07 | 0.10 | Ω |

**Table 5. Dynamic**

| Symbol | Parameter | Test condictions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $g_{fs}$ (1) | Forward transconductance | $V_{DS}$ >$I_{D(on)}$ x $R_{DS(on)max}$<br>$I_D$ = 22.5A | | 20 | | S |
| $C_{iss}$<br>$C_{oss}$<br>$C_{rss}$ | Input capacitance<br>Output capacitance<br>Reverse transfer capacitance | $V_{DS}$ =25V, f=1 MHz,<br>$V_{GS}$=0 | | 3600<br>1260<br>80 | | pF<br>pF<br>pF |
| $C_{oss\ eq.}$ (2) | Equivalent output capacitance | $V_{GS}$=0, $V_{DS}$ =0V to 400V | | 350 | | pF |
| $Q_g$<br>$Q_{gs}$<br>$Q_{gd}$ | Total gate charge<br>Gate-source charge<br>Gate-drain charge | $V_{DD}$=400V, $I_D$ = 45A<br>$V_{GS}$ =10V<br>(see Figure 13) | | 92<br>22<br>40 | 120 | nC<br>nC<br>nC |
| $R_G$ | Gate input resistance | f=1 MHz Gate DC Bias= 0<br>test signal level = 20mV<br>open drain | | 2 | | Ω |

1. Pulsed: pulse duration=300µs, duty cycle 1.5%
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as $C_{oss}$ when $V_{DS}$ increases from 0 to 80% $V_{DSS}$

**Table 6. Switching times**

| Symbol | Parameter | Test condictions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$<br>$t_r$ | Turn-on delay time<br>Rise time | $V_{DD}$=250 V, $I_D$= 22.5A,<br>$R_G$=4.7Ω, $V_{GS}$=10V<br>(see Figure 14) | | 28<br>28 | | ns<br>ns |
| $t_{r(Voff)}$<br>$t_f$<br>$t_c$ | Off-voltage rise time<br>Fall time<br>Cross-over time | $V_{DD}$=400 V, $I_D$= 45A,<br>$R_G$=4.7Ω, $V_{GS}$=10V<br>(see Figure 14) | | 11<br>25<br>44 | | ns<br>ns<br>ns |

**Table 7. Source drain diode**

| Symbol | Parameter | Test condictions | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain current | | | | 45 | A |
| $I_{SDM}$(1) | Source-drain current (pulsed) | | | | 180 | A |
| $V_{SD}$(2) | Forward on voltage | $I_{SD}$=45A, $V_{GS}$=0 | | | 1.5 | V |
| $t_{rr}$<br>$Q_{rr}$<br>$I_{RRM}$ | Reverse recovery time<br>Reverse recovery charge<br>Reverse recovery current | $I_{SD}$=45A, Tj=25°C<br>di/dt = 100A/µs,<br>$V_{DD}$=100V, (see Figure 17) | | 200<br>1600<br>16 | | ns<br>nC<br>A |
| $t_{rr}$<br>$Q_{rr}$<br>$I_{RRM}$ | Reverse recovery time<br>Reverse recovery charge<br>Reverse recovery current | $I_{SD}$=45A, Tj=150°C<br>di/dt = 100A/µs,<br>$V_{DD}$=100V, (see Figure 17) | | 324<br>4017<br>24.8 | | ns<br>nC<br>A |

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

**Figure 1. Safe operating area**

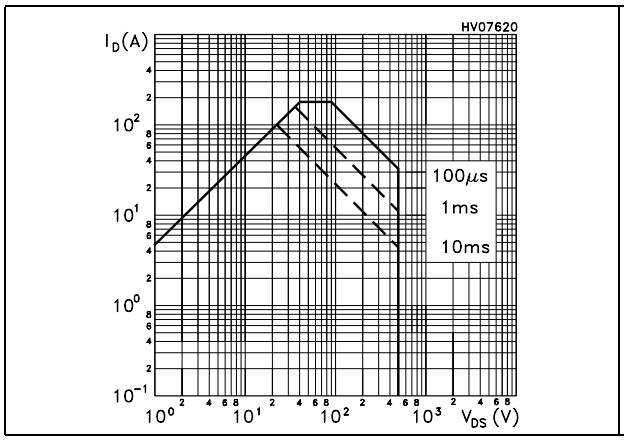



**Figure 2. Thermal impedance**

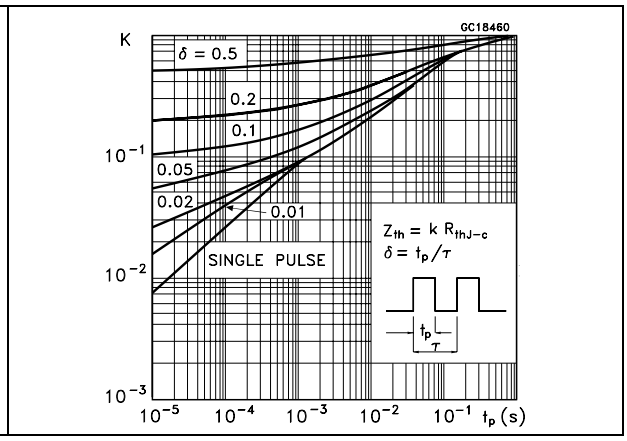



**Figure 3. Output characterisics**

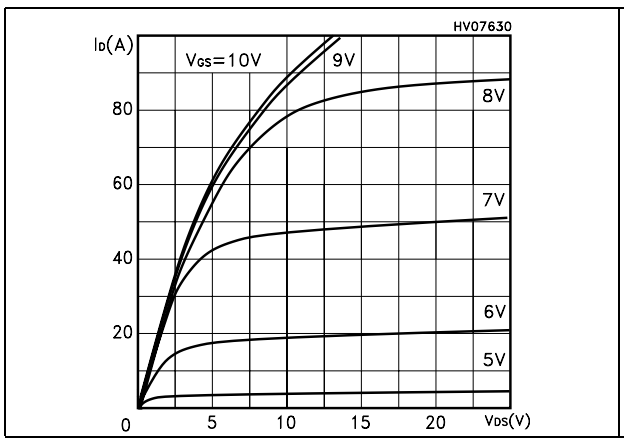



**Figure 4. Transfer characteristics**

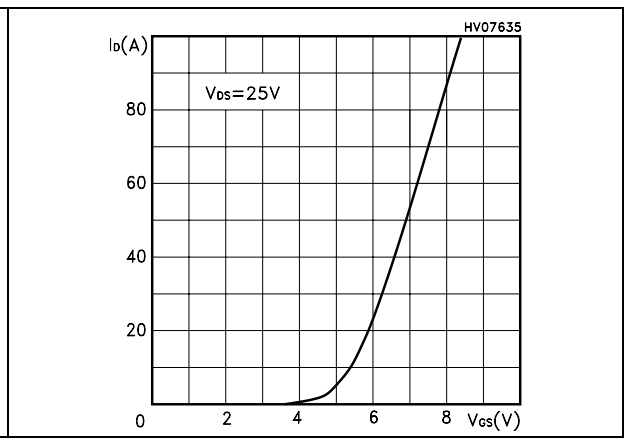



**Figure 5. Transconductance**

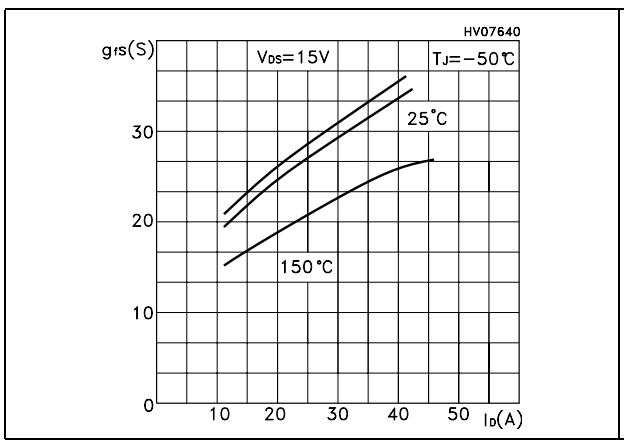



**Figure 6. Static drain-source on resistance**

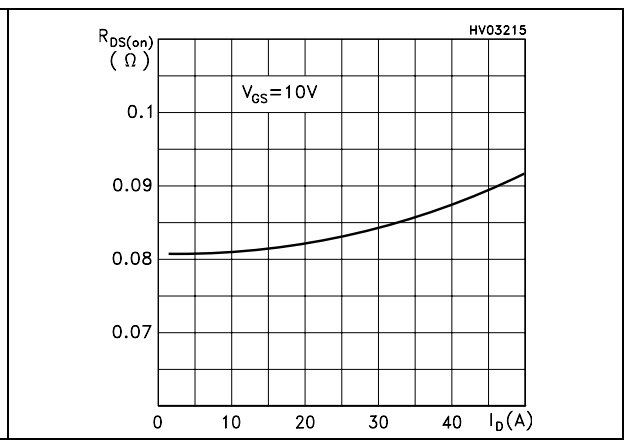


**Figure 7. Gate charge vs gate-source voltage**

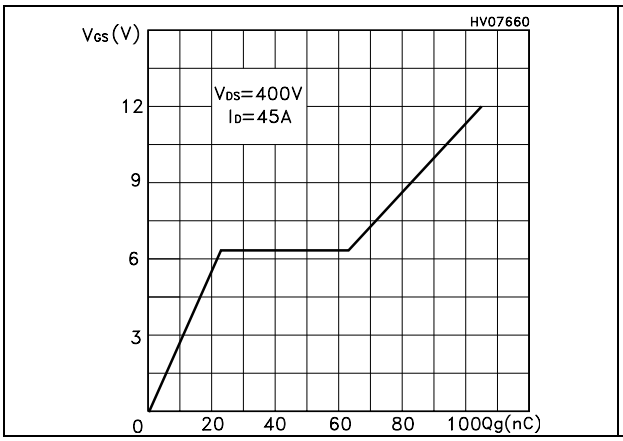



**Figure 8. Capacitance variations**

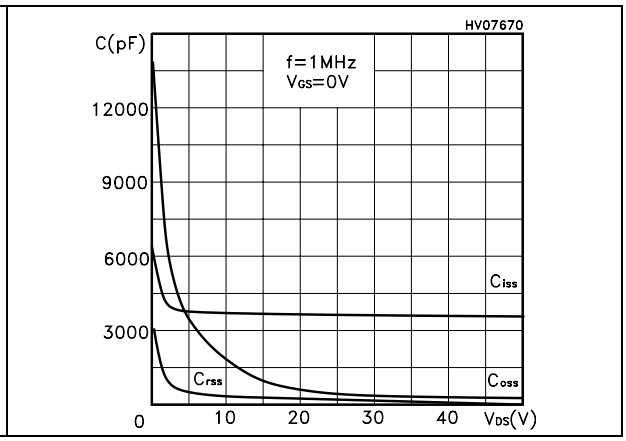



**Figure 9. Normalized gate threshold voltage vs temperature**

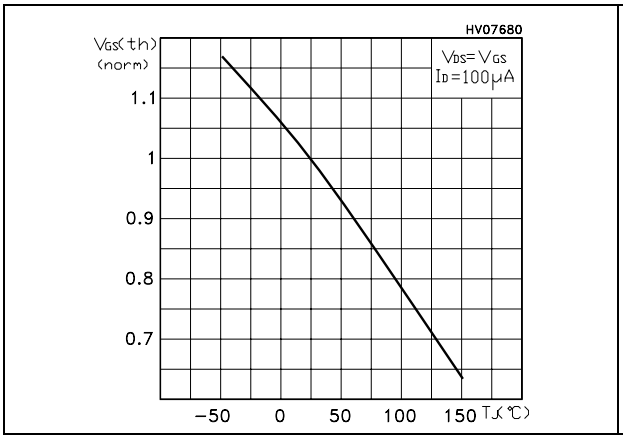



**Figure 10. Normalized on resistance vs temperature**

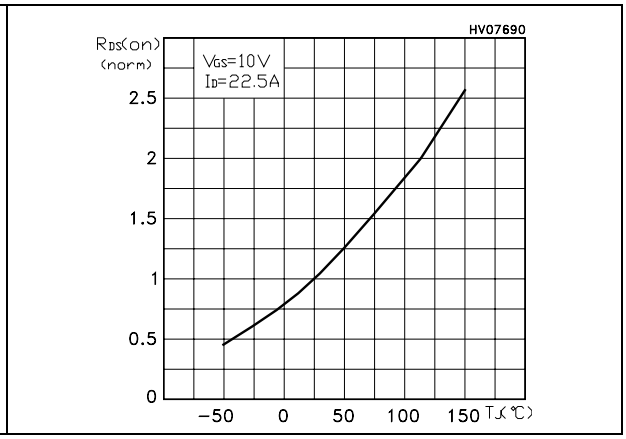
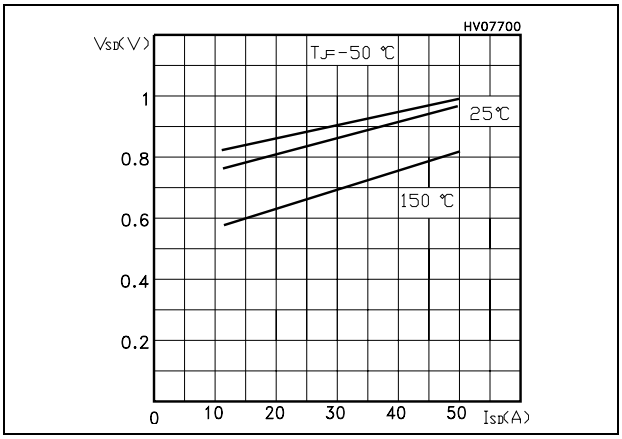



**Figure 11. Source-drain diode forward characteristics**



# 3 Test circuit

**Figure 12. Switching times test circuit for resistive load**

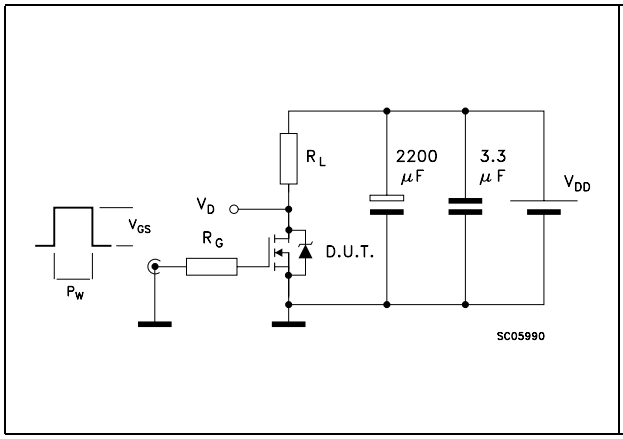



**Figure 13. Gate charge test circuit**

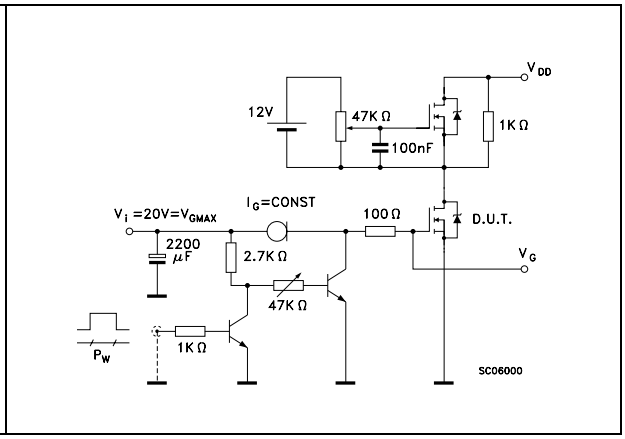



**Figure 14. Test circuit for inductive load switching and diode recovery times**

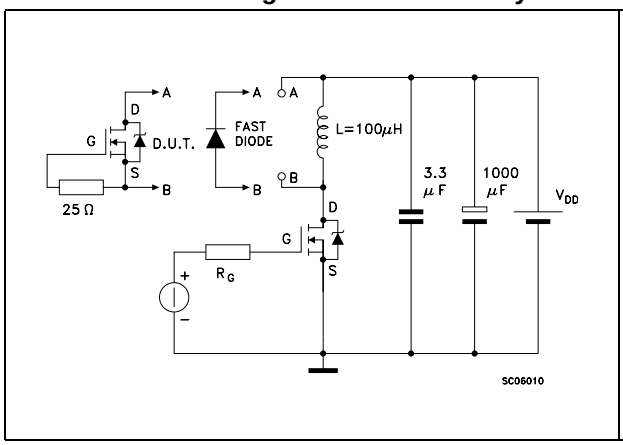



**Figure 15. Unclamped inductive load test circuit**

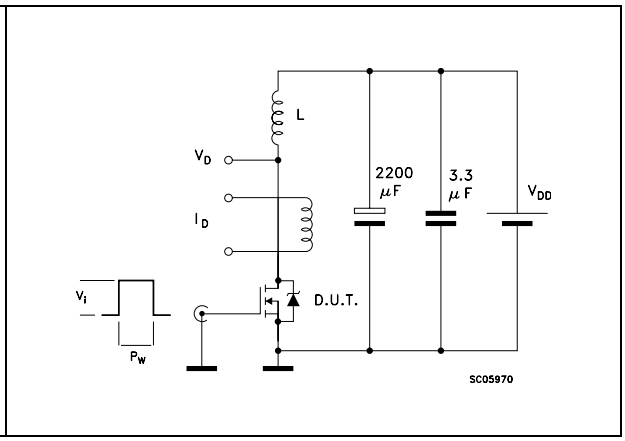



**Figure 16. Unclamped inductive waveform**

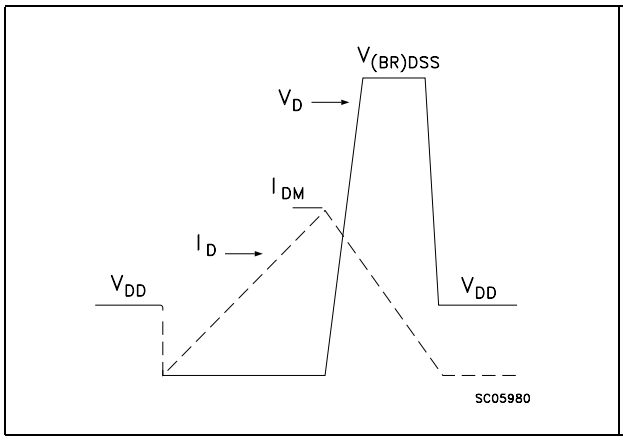
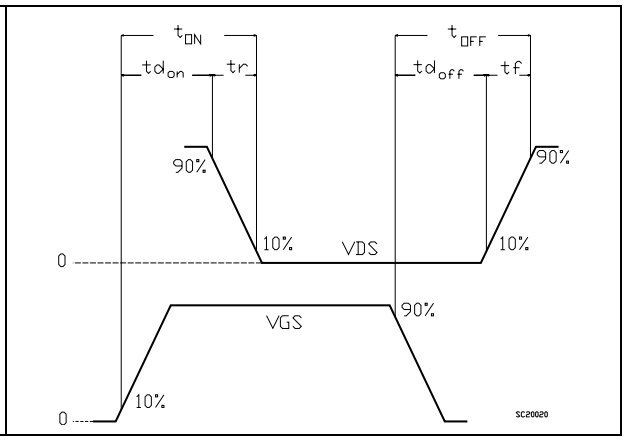



**Figure 17. Switching time waveform**

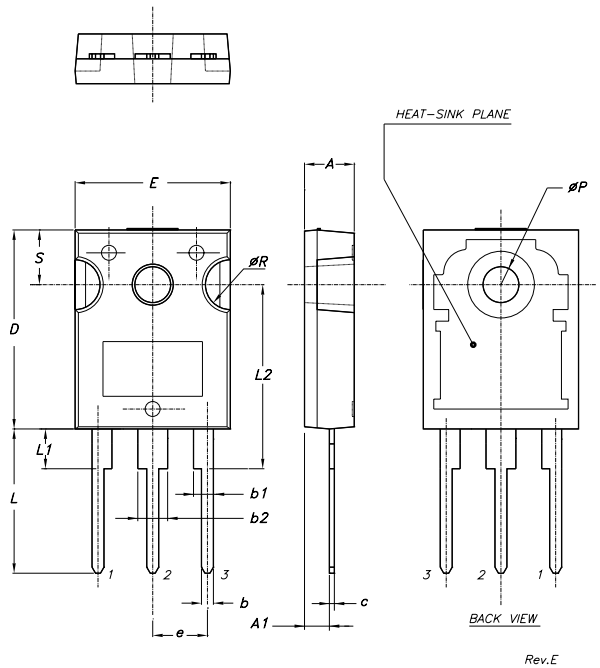


# 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

## TO-247 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | 4.85 | | 5.15 | 0.19 | | 0.20 |
| A1 | 2.20 | | 2.60 | 0.086 | | 0.102 |
| b | 1.0 | | 1.40 | 0.039 | | 0.055 |
| b1 | 2.0 | | 2.40 | 0.079 | | 0.094 |
| b2 | 3.0 | | 3.40 | 0.118 | | 0.134 |
| c | 0.40 | | 0.80 | 0.015 | | 0.03 |
| D | 19.85 | | 20.15 | 0.781 | | 0.793 |
| E | 15.45 | | 15.75 | 0.608 | | 0.620 |
| e | | 5.45 | | | 0.214 | |
| L | 14.20 | | 14.80 | 0.560 | | 0.582 |
| L1 | 3.70 | | 4.30 | 0.14 | | 0.17 |
| L2 | | 18.50 | | | 0.728 | |
| øP | 3.55 | | 3.65 | 0.140 | | 0.143 |
| øR | 4.50 | | 5.50 | 0.177 | | 0.216 |
| S | | 5.50 | | | 0.216 | |



# 5 Revision history

**Table 8. Revision history**

| Date | Revision | Changes |
|---|---|---|
| 05-Apr-2005 | 8 | Modified value on *Table 7.: Source drain diode* |
| 26-Apr-2006 | 9 | New template |

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