

## N-Channel 150-V (D-S) MOSFET

**PRODUCT SUMMARY**

$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)	$Q_g$ (Typ.)
150	0.018 at $V_{GS} = 10$ V	75 <sup>d</sup>	64

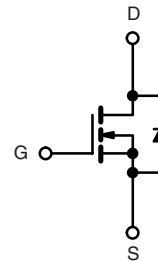
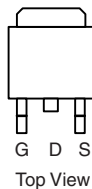
**FEATURES**

- TrenchFET<sup>®</sup> Power MOSFET
- 100 %  $R_g$  and UIS Tested


**RoHS**  
COMPLIANT

**APPLICATIONS**

- Primary Side Switch
- Power Supplies

**TO-263**


N-Channel MOSFET

**Ordering Information:** SUM75N15-18P-E3 (Lead (Pb)-free)

**ABSOLUTE MAXIMUM RATINGS**  $T_C = 25$  °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	150	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 175$ °C)	$I_D$	$T_C = 25$ °C	75 <sup>d</sup>
		$T_C = 70$ °C	70
Pulsed Drain Current	$I_{DM}$	180	A
Avalanche Current	$I_{AS}$	50	
Single Avalanche Energy <sup>a</sup>	$E_{AS}$	125	mJ
Maximum Power Dissipation <sup>a</sup>	$P_D$	$T_C = 25$ °C	312.5 <sup>b</sup>
		$T_A = 25$ °C <sup>c</sup>	3.12
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 150	°C

**THERMAL RESISTANCE RATINGS**

Parameter	Symbol	Limit	Unit
Junction-to-Ambient (PCB Mount) <sup>c</sup>	$R_{thJA}$	40	°C/W
Junction-to-Case (Drain)	$R_{thJC}$	0.4	

Notes:

- Duty cycle  $\leq 1$  %.
- See SOA curve for voltage derating.
- When Mounted on 1" square PCB (FR-4 material).
- Package limited.

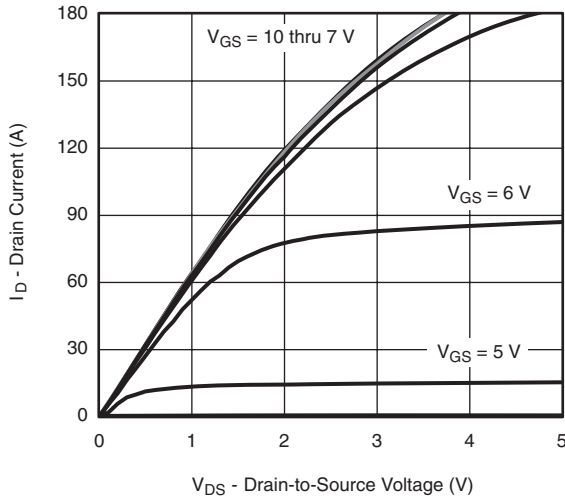
<b>SPECIFICATIONS</b> $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{DS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	150			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.5		4.5	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 250$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 150\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 150\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$			50	
		$V_{DS} = 150\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^\circ\text{C}$			250	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 10\text{ V}, V_{GS} = 10\text{ V}$	120			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		0.0148	0.018	$\Omega$
		$V_{GS} = 10\text{ V}, I_D = 20\text{ A}, T_J = 125\text{ }^\circ\text{C}$		0.0296	0.036	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 20\text{ A}$		55		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 75\text{ V}, f = 1\text{ MHz}$		4180		$\mu\text{F}$
Output Capacitance	$C_{oss}$			235		
Reverse Transfer Capacitance	$C_{rss}$			83		
Total Gate Charge <sup>c</sup>	$Q_g$	$V_{DS} = 75\text{ V}, V_{GS} = 10\text{ V}, I_D = 85\text{ A}$		64	100	nC
Gate-Source Charge <sup>c</sup>	$Q_{gs}$			23		
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			16		
Gate Resistance	$R_g$	$f = 1\text{ MHz}$		2.1	4.2	$\Omega$
Turn-On Delay Time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = 75\text{ V}, R_L = 0.88\text{ }\Omega$ $I_D = 85\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		15	25	ns
Rise Time <sup>c</sup>	$t_r$			10	15	
Turn-Off Delay Time <sup>c</sup>	$t_{d(off)}$			25	40	
Fall Time <sup>c</sup>	$t_f$			8	15	
<b>Source-Drain Diode Ratings and Characteristics</b> $T_C = 25\text{ }^\circ\text{C}$ <sup>b</sup>						
Continuous Current	$I_S$				75	A
Pulsed Current	$I_{SM}$				180	
Forward Voltage <sup>a</sup>	$V_{SD}$	$I_F = 30\text{ A}, V_{GS} = 0\text{ V}$		1.0	1.5	V
Reverse Recovery Time	$t_{rr}$	$I_F = 50\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		130	200	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			8	12	A
Reverse Recovery Charge	$Q_{rr}$			520	1200	nC

Notes:

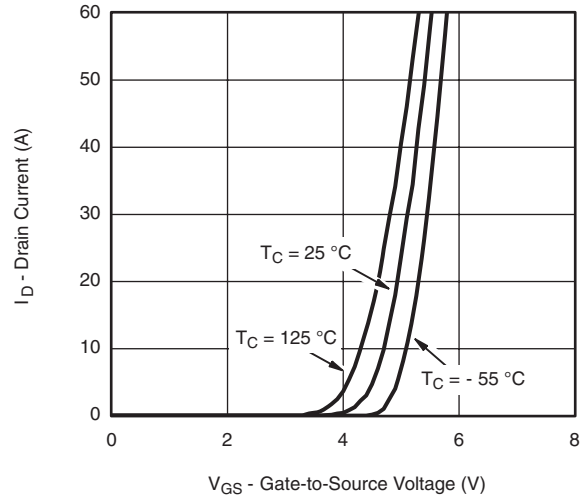
- Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

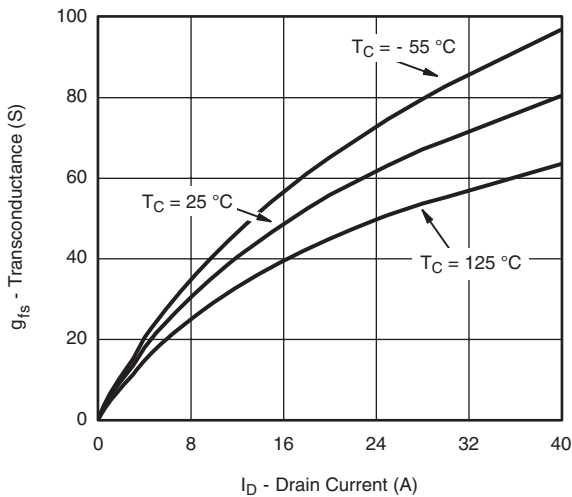
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



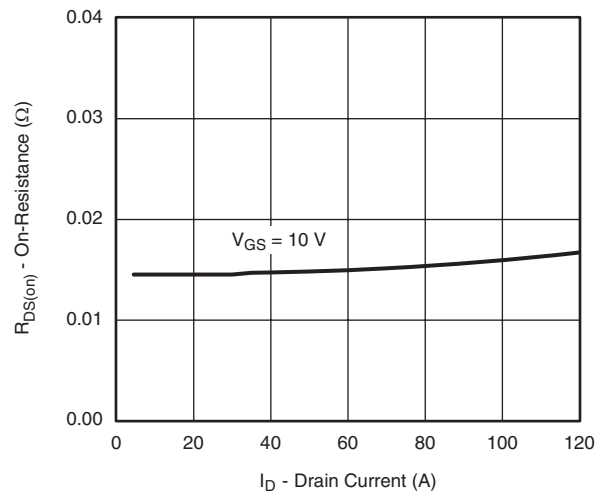
**Output Characteristics**



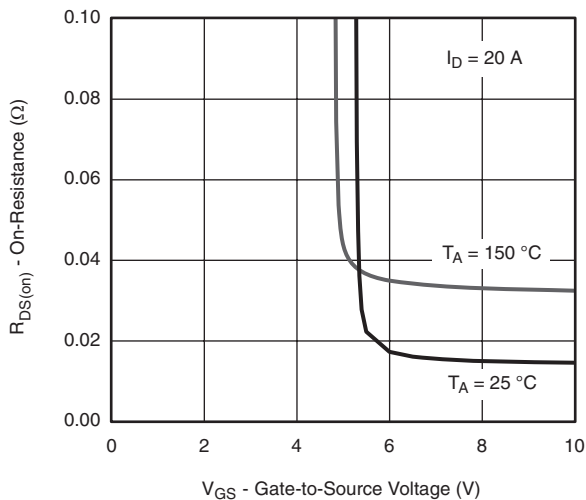
**Transfer Characteristics**



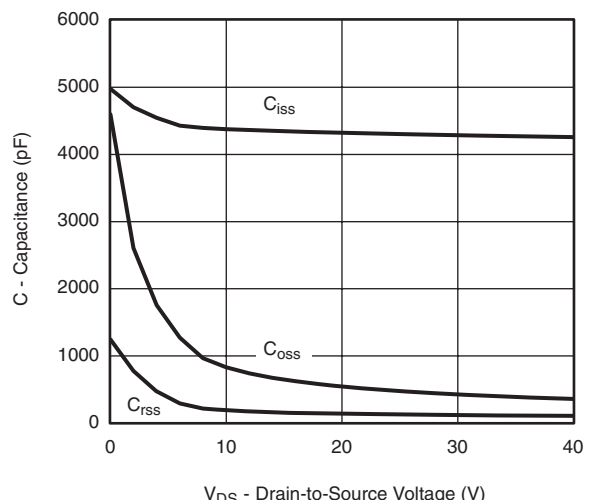
**Transconductance**



**On-Resistance vs. Drain Current**

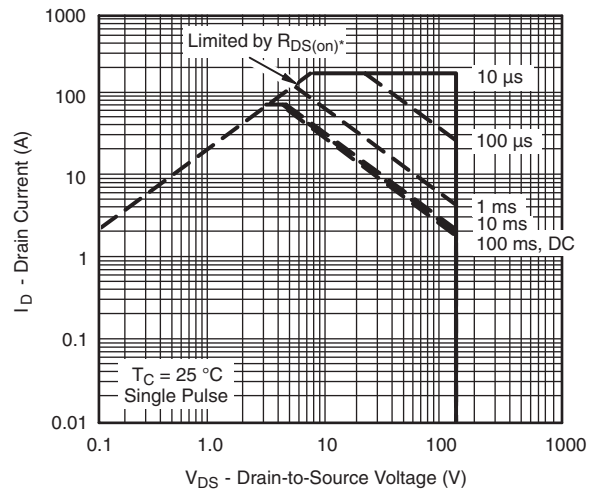
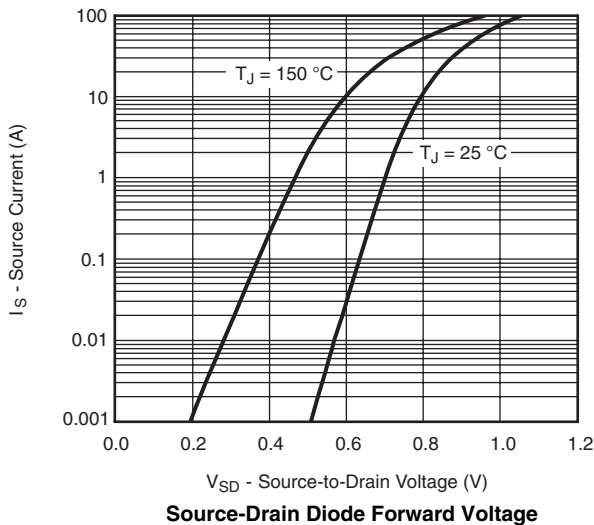
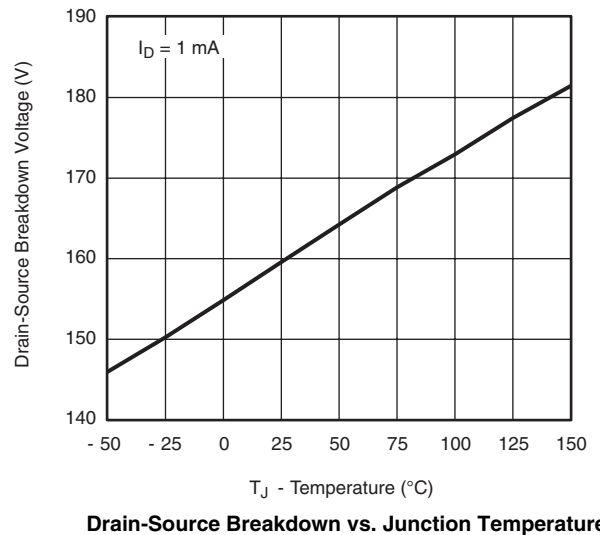
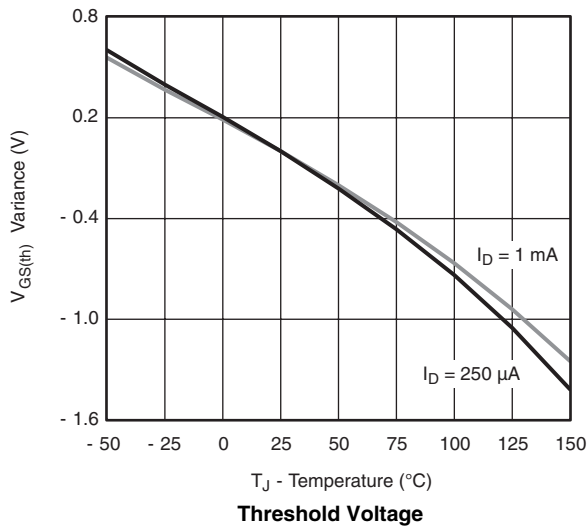
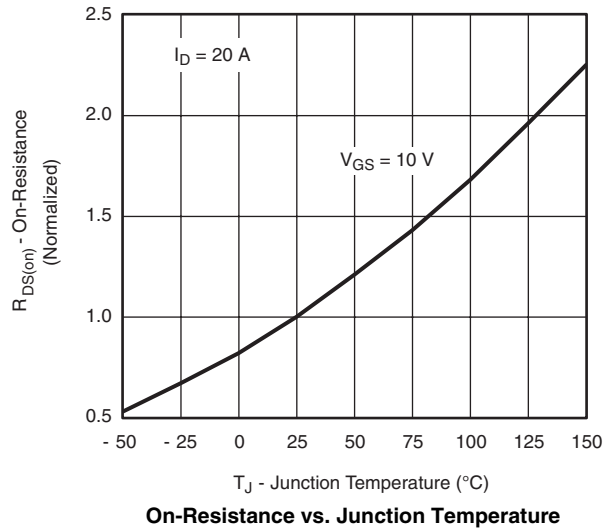
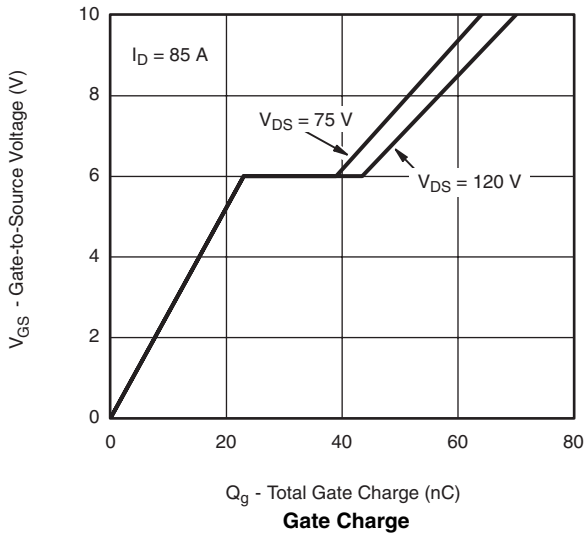


**On-Resistance vs. Gate-to-Source Voltage**



**Capacitance**

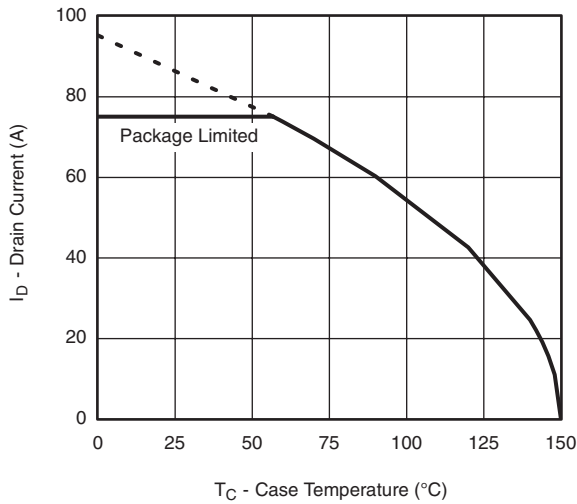
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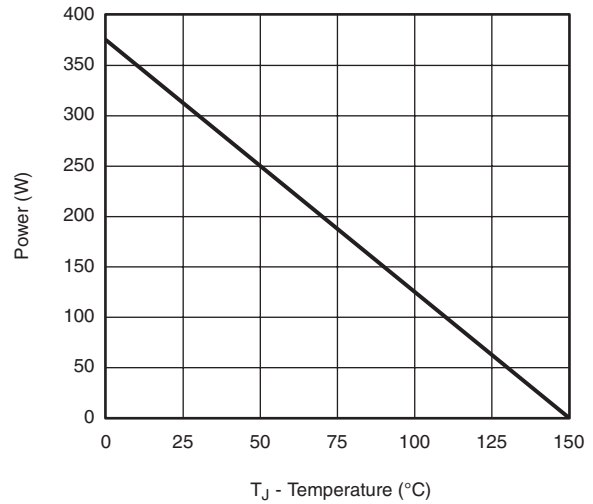
\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

**Safe Operating Area, Junction-to-Case**

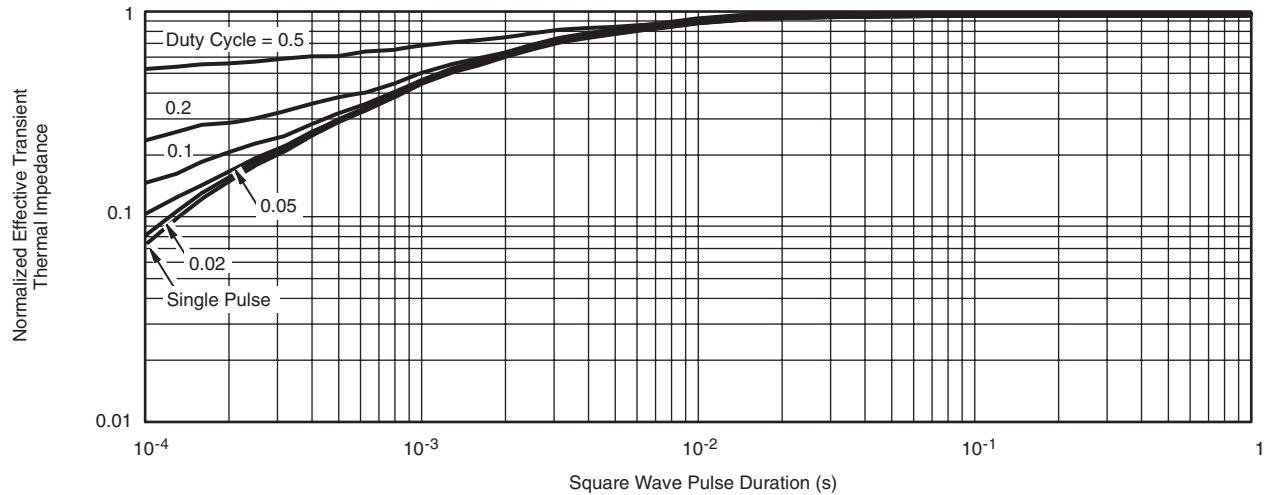
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



**Current Derating\*, Junction-to-Case**



**Power Derating\*, Junction-to-Case**



**Normalized Thermal Transient Impedance, Junction-to-Case**

\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150\text{ °C}$ , using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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