Document Title

16M(1M x 16bit) Normal mode & Page mode with Deep Power Down Static Random Access Memory

Revision history

Rev. No.	History	Issue Date	Remark
0.0	Initial issue	May 24, 2005	Preliminary
1.0	Erase non-Pb-free package type Final version release	March 07, 2007	Final

MEMORY

16M(1M x 16bit) Normal mode & Page mode with Deep Power Down Static Random Access Memory

DESCRIPTION

The A64S06162A is a 16Mb high speed, low power Static Random Access Memory(SRAM) organized as 1,048,576 words by 16 bits and supports Deep Power Down and Page Mode. The A64S06162A is a Pseudo SRAM based on successfully proven DRAM CELL *SRAM* which was specifically developed for cost sensitive, low power computing and communication applications such as mobile cellular phone handsets, personal digital assistants and other battery-operated consumer products.

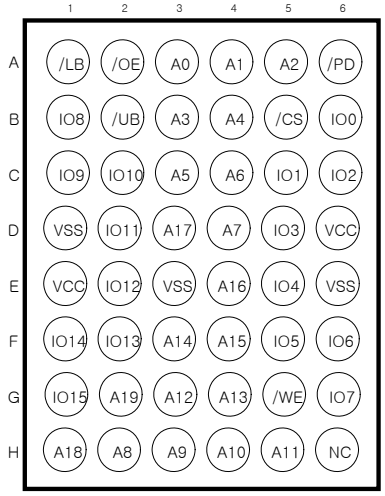
FEATURES

- Standard Asynchronous SRAM Interface with Deep Power Down and Page Mode
- Organization : 1M x 16Bit
- Power Supply Voltage : 2.7 ~ 3.3 V
- Page Size : 4 words
- Page Mode Access (tPAA) : 35ns
- Data Retention Voltage : 2.4V
- Deep Power Down : 5uA
- Tri-state Output and TTL Compatible

PRODUCT FAMILY

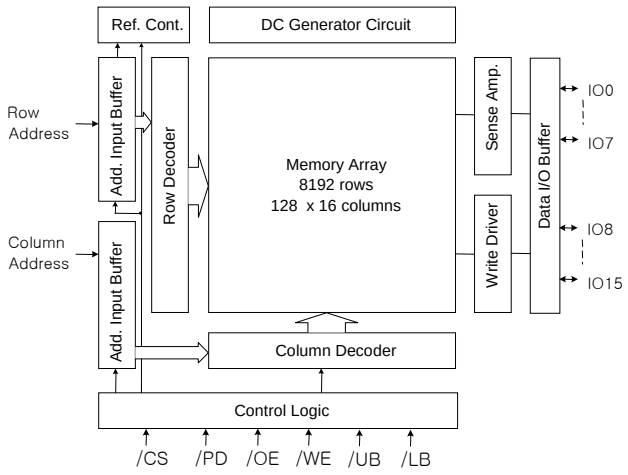
Product Family	Operating Temperature	Voltage	Speed	ISB1 (Max)	IccDR (Max)	ICC1 (Max)	Mode
A64S06162A	-40 ~ 85 ℃	2.7 ~ 3.3 V	70	100uA	100uA	2.0mA	Page

PIN DESCRIPTION



Note : E3 pin (VSS) can be remain as a NC

FUNCTIONAL BLOCK DIAGRAM



Name	Function	Name	Function
/CS	Chip Select Input	VCC	Power
/OE	Output Enable Input	VSS	Ground
/WE	Write Enable Input	/UB	Upper Byte (IO8～15)
A0～A19	Address Input	/LB	Lower Byte (IO0～7)
IO0～IO15	Data Input / Output	/PD	Deep Power Down

PRODUCT LIST

Part Name	Function
A64S06162A-70U	16M, 48-FBGA , 70 ns, 3.0V, -40℃ ~ 85℃

ABSOLUTE MAXIMUM RATING

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	−0.2 to VCC+0.3 V	V
Voltage on Vcc supply relative to Vss	V_{CC}	−0.2 to 3.6	V
Power Dissipation	P_D	1.0	W
Storage temperature	T_{STG}	−55 to 150	℃
Operating Temperature (Extended)	T_A	−40 ~ 85	℃

Note :
Stresses greater than those listed under “ABSOLUTE MAXIMUM RATINGS” may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

TRUTH TABLE

/CS	/PD	/OE	/WE	/LB	/UB	I/O 0~7	I/O 8~15	MODE	Power
X	L	X	X	X	X	High-Z	High-Z	Deselected	Deep Power Down
H	H	X	X	X	X	High-Z	High-Z	Deselected	Standby
X	H	X	X	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	H	L	X	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Data Out	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Data Out	Upper Byte Read	Active
L	H	L	H	L	L	Data Out	Data Out	Word Read	Active
L	H	X	L	L	H	Data In	High-Z	Lower Byte Write	Active
L	H	X	L	H	L	High-Z	Data In	Upper Byte Write	Active
L	H	X	L	L	L	Data In	Data In	Word Write	Active

RECOMMENDED DC OPERATING CONDITIONS [1)]

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage [(5)]	Vcc	2.7	3.0	3.3	V
Ground	Vss	0	0	0	V
Input High Voltage	VIH	0.8*Vcc	-	Vcc+0.2 [2)]	V
Input Low Voltage	VIL	-0.2 [3)]	-	0.4	V

Note :
1.T_A = -40℃ to 85℃, otherwise specified.
2. Overshoot : Vcc + 1.0V in case of pulse width ≤ 20 ns.
3. Undershoot : -1.0V in case of pulse width ≤ 20 ns.
4. Overshoot and undershoot are sampled, not 100% tested.
5. Stable power supply required 100 us before device operation.

CAPACITANCE (T_A = 25 ℃, f = 1.0MHz)

Symbol	Parameter	Condition	Max.	Unit
CIN	Input Capacitance	VIN =0V	8	pF
COUT	Output Capacitance	VIO =0V	10	pF

Note : This parameter is sampled and not 100% tested

DC AND OPERATING CHARACTERISTICS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Leakage Current	ILI	VIN = Vss to Vcc	-1		1	uA
Output Leakage Current	ILO	/CS = VIH, /UB=/LB= VIH or /OE=VIH or /WE=VIL, VIO=Vss to Vcc	-1		1	uA
	Icc1	Cycle Time = 1 us, 100%duty, IIO=0mA, /CS ≤ 0.2V, VIN ≤ 0.2V or VIN ≥ Vcc-0.2V			2.0	mA
	Icc2	Cycle time=Min, IIO=0mA, 100% duty /CS = VIL,VIN=VIL or VIH			20	mA
	Iccp	/CS1 = VIL, CS2=VIH,Tpwc = min Page address cycling			10	mA
Output Low Voltage	VOL	IOL = 2 mA			0.4	V
Output High Voltage	VOH	IOH = -1 mA	2.2			V
Standby Current(TTL)	ISB	/CS=VIH, /UB=/LB= VIH, Other inputs = VIH or VIL			0.3	mA
Standby Current(CMOS)	ISB1	/CS ≥ Vcc-0.2V, /UB=/LB ≥ Vcc-0.2V (/UB,/LB Controlled) Other inputs = 0 or Vcc			100	uA
Deep Power Down Current	ISB2	/PD ≤ Vss+0.2V			5	uA

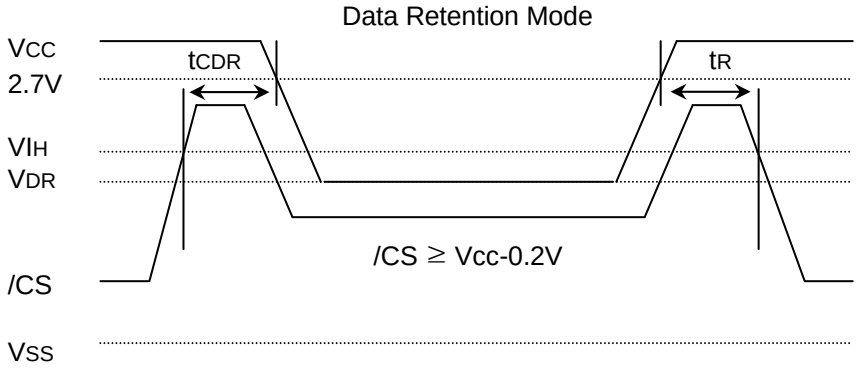
Data Retention Electric Characteristic

T_A = -40℃ to 85℃ (Normal), unless otherwise specified

Item	Symbol	Test Condition	Min	Typ. (1)	Max	Unit
Voltage for Data Retention	V_{DR}	/CS=/PD=V_{IH} > Vcc−0.2V or /UB,/LB≥Vcc−0.2V, V_{IN}≥V_{CC}−0.2V or V_{IN}≤V_{SS} + 0.2V	2.4		3.3	V
Data Retention Current	I_{CCDR}	Vcc=2.4V, /CS=/PD=V_{IH} > Vcc−0.2V or /UB,/LB≥Vcc−0.2V, V_{IN}≥V_{CC}−0.2V or V_{IN}≤V_{SS} + 0.2V			100	uA
Chip Deselect to Data Retention Time	t_{CDR}	Refer to data retention wave form	0	−	−	ns
Operating Recovery Time	t_R		tRC	−	−	ns

(1) V_{CC} = 2.4V, T_A = 25℃

Data Retention Wave Form

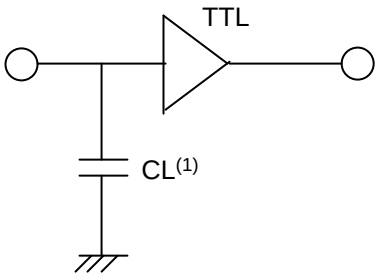


AC TEST CONDITIONS

T_A = -40℃ to 85℃ (Normal), unless otherwise specified

PARAMETER	Value
Input Pulse Level	0.4V to 2.2V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Level	1.5V
Output Load	CL = 30pF + 1TTL Load

AC TEST LOADS



Note : (1) Including jig and scope capacitance

POWER UP TIME

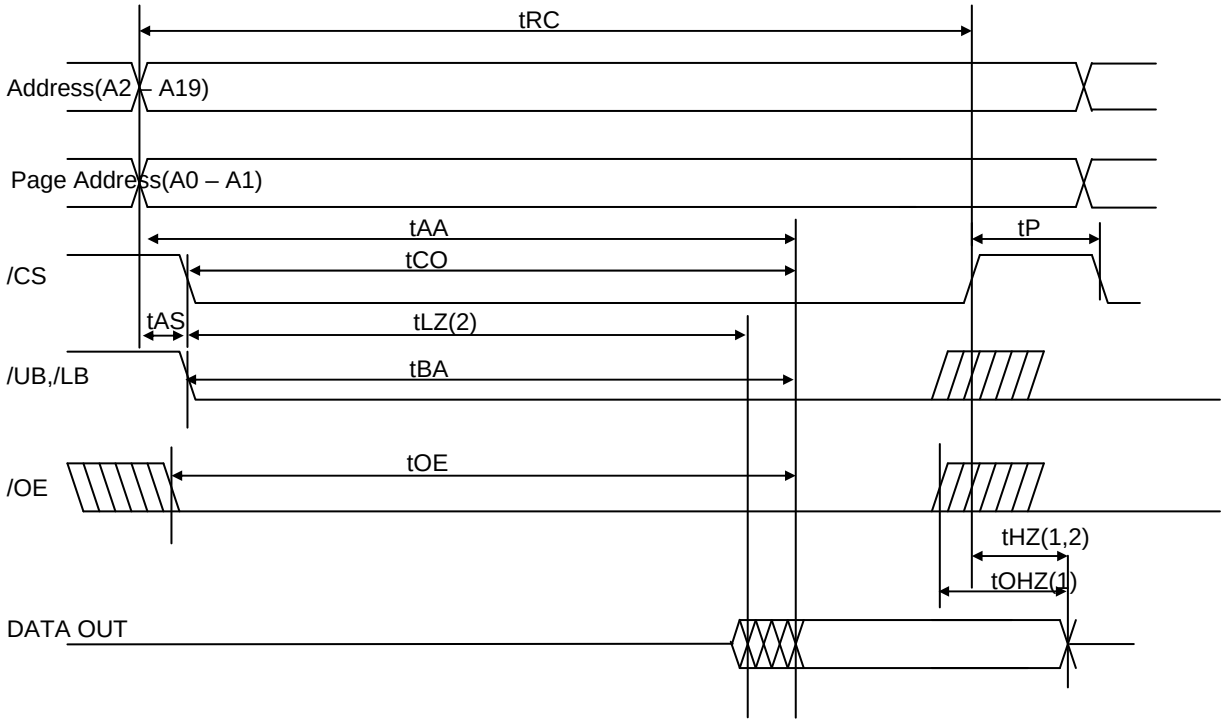
At starting, maintain stable power for a minimum 100us with /CS = /PD = high.

AC CHARACTERISTICS (Vcc = 2.7 ~ 3.3V, T_A = -40 to 85℃)

Parameter List		Symbol	70ns		Unit
			Min	Max	
READ	Read Cycle Time	tRC	70		ns
	Address Set-up Time	tAS	0		ns
	Address Access Time	tAA		70	ns
	Chip Select to Output	tCO		70	ns
	Output Enable to Valid Output	tOE		35	ns
	/UB,/LB Access Time	tBA		70	ns
	Chip select to Low-Z Output	tLZ	10		ns
	/UB, /LB Enable to Low-Z Output	tBLZ	10		ns
	Output Enable to Low-Z Output	tOLZ	5		ns
	Chip Disable to High-Z Output	tHZ	0	25	ns
	/UB, /LB Disable to High-Z Output	tBHZ	0	25	ns
	Output Disable to High-Z Output	tOHZ	0	25	ns
	Output Hold from Address Change	tOH	10		ns
	Page Read Precharge Time	tP	10		ns
	Page Read Cycle Time	tPRC	35		ns
	Page Read Address Access Time	tPAA		35	ns
WRITE	Write Cycle Time	tWC	70		ns
	Chip Select to End of Write	tCW	60		ns
	Address Valid to End of Write	tAW	60		ns
	/UB, /LB Valid to End of Write	tBW	60		ns
	Write Pulse Width	tWP	50		ns
	Write Recovery Time	tWR	0		ns
	Write to Output High-Z	tWHZ	0	20	ns
	Data to Write Time Overlap	tDW	40		ns
	Data Hold from Write Time	tDH	0		ns
	End of Write to Output Low-Z	tOW	5		ns
	Page Write Precharge Time	tP	10		ns
	Page Write Cycle Time	tPWC	35		ns
	Page Write Data to Write Time overlap	tPDW	20		ns
	Page Write Data Hold from Write Time	tPDH	0		ns

TIMING DIAGRAMS

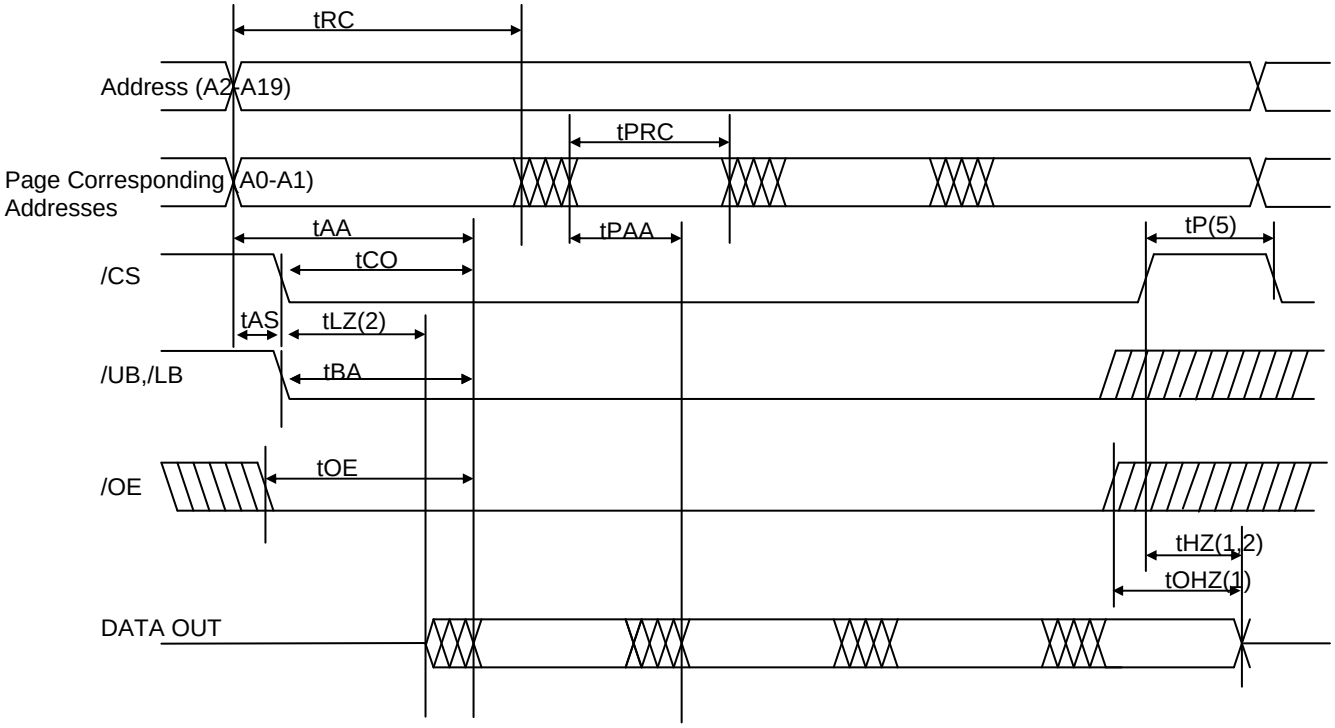
READ CYCLE (/PD = /WE = V_{IH})



Note (READ CYCLE) :

1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels
2. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.
3. /WE is high for the read cycle.
4. Do not access device with cycle timing shorter than tRC for continuous periods > 16us.

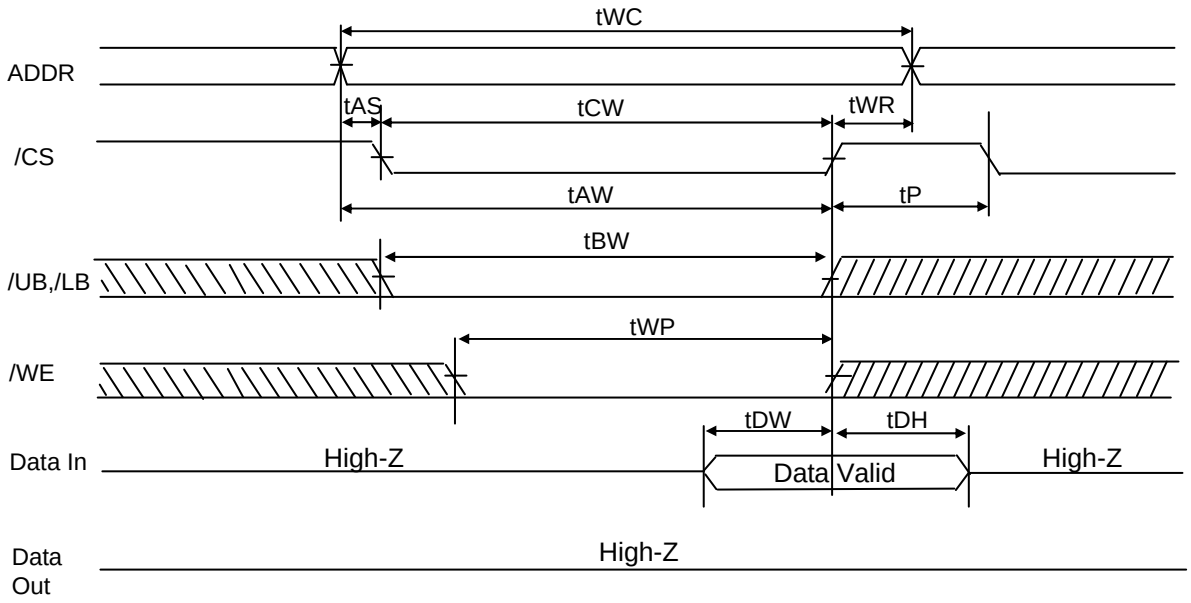
PAGE READ CYCLE (/PD = /WE = V_{IH})



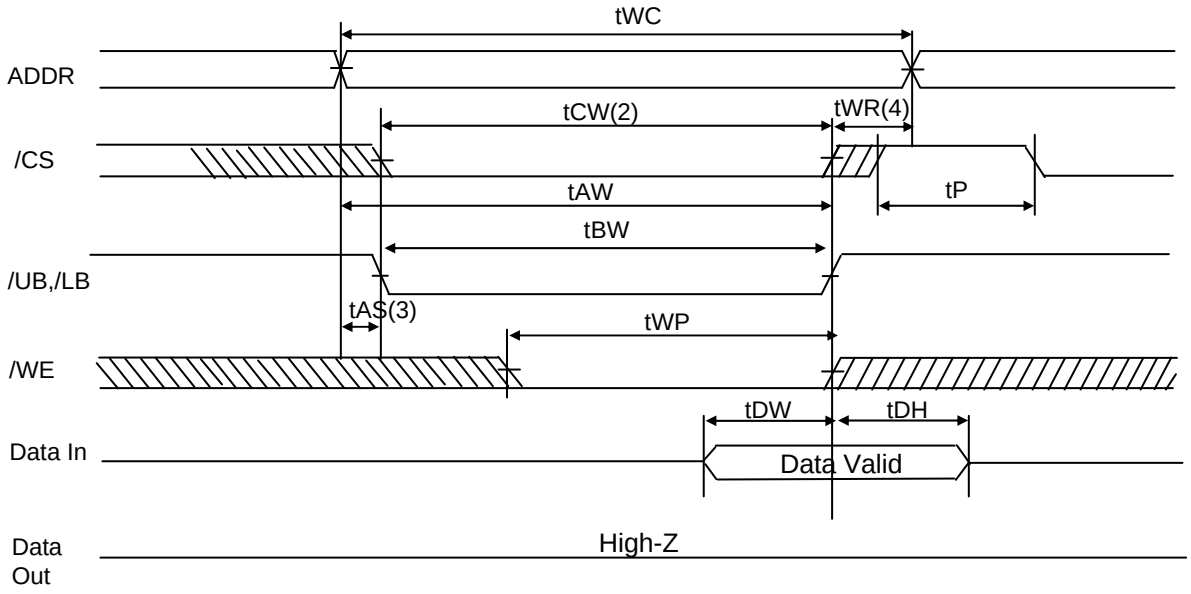
Note (PAGE MODE READ CYCLE) :

1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels
2. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.
3. /WE is high for the read cycle.
4. Do not access device with cycle timing shorter than tRC for continuous periods > 16us.
5. tP (precharge time) should be guaranteed for **new Address**.
6. After initial page access is accomplished, the page mode operation provides fast read access speed of random locations within that page

WRITE CYCLE 1 (/CS Controlled, /PD = V_{IH})



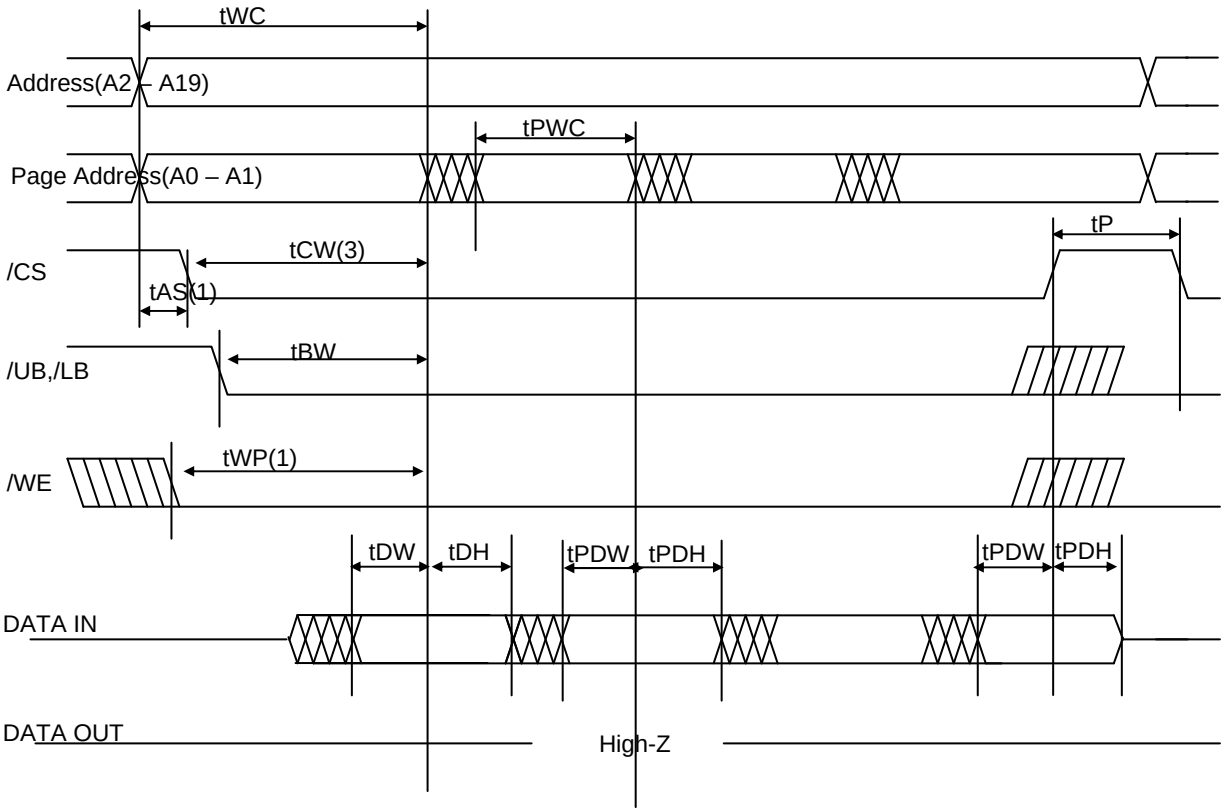
WRITE CYCLE 2 (/UB /LB Controlled, /PD = V_{IH}



Notes (WRITE CYCLE) :

1. A write occurs during the overlap of a low /CS and low /WE. A write begins at the latest transition among /CS going low and /WE going low: A write end at the earliest transition among /CS going high and /WE going high. tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the later of /CS going low to the end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR is applied in case a write ends as /CS.
5. Do not access device with cycle timing shorter than tRC for continuous periods > 16us.

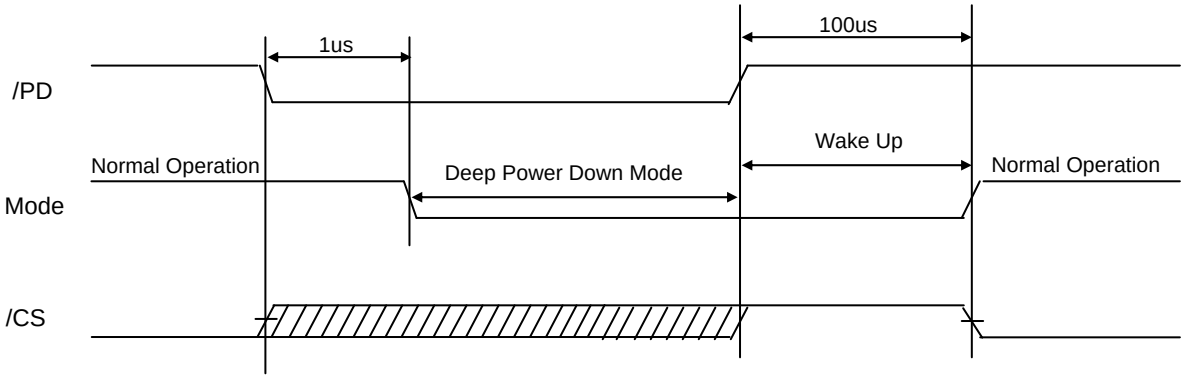
PAGE MODE WRITE CYCLE (/PD = V_{IH})



Notes (PAGE MODE WRITE CYCLE) :

1. A write occurs during the overlap of a low /CS and low /WE.
   A write begins at the latest transition among /CS going low in initial page mode .
   A write end at the earliest transition among /CS going high and **Page Address transition.**
   tWP is measured from the beginning of write to the end of write in initial page access.
2. tPWC is measured from Page Address trasition (After initial page access)
   to Page Address transition or /CS going high.
2. tCW is measured from the later of /CS going low to the end of write in initial page access.
3. tAS is measured from the address valid to the beginning of write.
4. Do not access device with cycle timing shorter than tRC for continuous periods > 16us.
5. tP (precharge time) should be guaranteed for new Page Address.
6. After initial page access is accomplished, the page mode operation provides fast read access speed of random locations within that page

Deep Power Down Mode



Ordering Information

Part No.	Access Time (ns)	Operating Current Max. (mA)	Power Down Mode Standby Current Max. (μA)	Package
A64S06162AG-70F	70	20	5	48B Pb-Free Mini BGA
A64S06162AG-70UF	70	20	5	48B Pb-Free Mini BGA

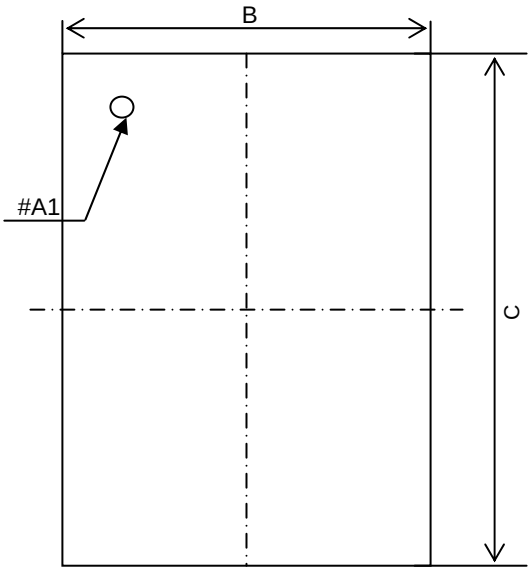
•Note : -U is for -40c ~ 85c temperature grade

PACKAGE DIMENSION FOR BGA TYPE

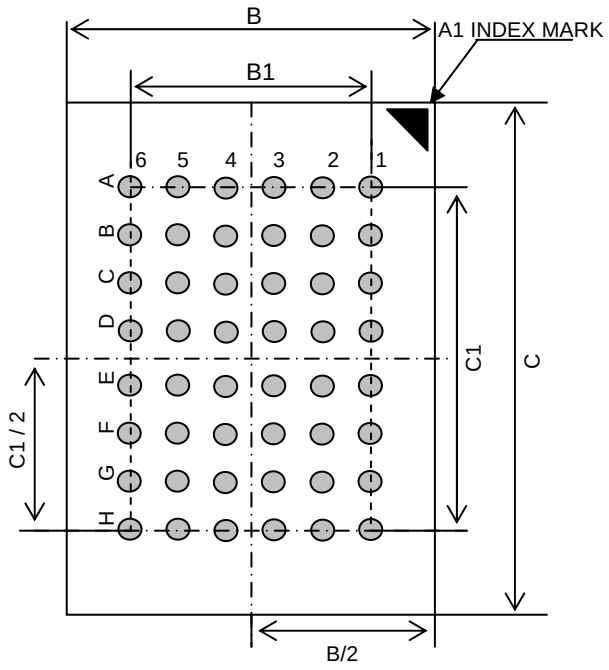
Unit: millimeters

48 BALL FINE PITCH 6mm x 8mm BGA(0.75mm ball pitch)

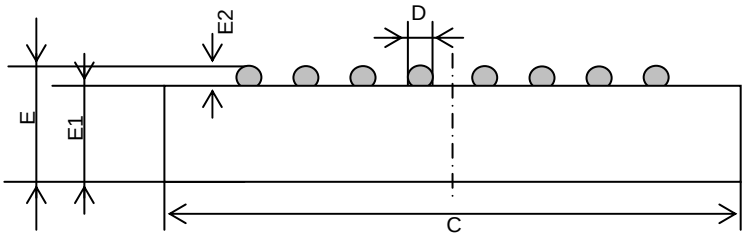
Top View

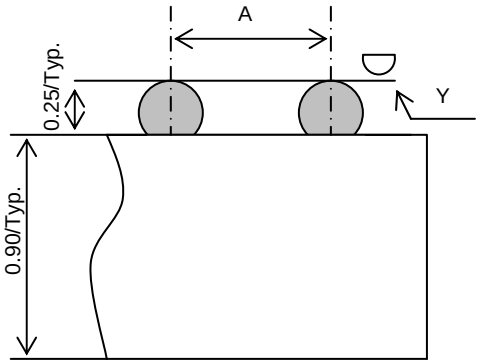


Bottom View



Side View





	Min	Typical	Max
A	–	0.75	–
B	5.90	6.00	6.10
B1	–	3.75	–
C	7.90	8.00	8.10
C1	–	5.25	–
D	0.30	0.35	0.40
E	–	–	1.20
E1	–	–	0.90
E2	0.20	0.25	0.30
Y	–	–	0.10