

11-Bit, 200MSPS, Ultralow-Power ADC with Integrated Analog Buffer and SNRBoost

Check for Samples: [ADS58B18](#)

FEATURES

- **Integrated High-Impedance Analog Input Buffer**
 - **Input Capacitance: 2pF**
 - **DC Resistance: 10kΩ**
- **Maximum Sample Rate: 200MSPS**
- **Ultralow Power**
 - **1.8V Core Power: 202mW**
 - **3.3V Buffer Power: 79mW**
 - **I/O Power: 34mW (DDR LVDS)**
- **Enhanced SNR Using TI-Proprietary SNRBoost Technology**
- **High Dynamic Performance:**
 - **SNR: 66.5dBFS at 150MHz**
 - **SNR: 80dBFS in 20MHz Bandwidth with SNRBoost**
 - **SFDR: 80dBc at 150MHz, –2dBFS Input**
- **Dynamic Power Scaling with Sample Rate**
- **Output Interface**
 - **Double Data Rate (DDR) LVDS with Programmable Swing and Strength**
 - **Standard Swing: 350mV**
 - **Low Swing: 200mV**
 - **Default Strength: 100Ω Termination**
 - **2x Strength: 50Ω Termination**
 - **1.8V Parallel CMOS Interface Also Supported**
- **Programmable Gain up to 6dB for SNR/SFDR Trade-Off**
- **DC Offset Correction**
- **Supports Low Input Clock Amplitude**
- **Package: QFN-48 (7mm × 7mm)**

DESCRIPTION

The ADS58B18 is an 11-bit analog-to-digital converter (ADCs) with sampling rates up to 200MSPS and integrated analog input buffers. This device uses innovative design techniques to achieve high dynamic performance, while consuming extremely low power. The analog input pins have buffers, with benefits of constant performance and input impedance across a wide frequency range. The ADS58B18 is well-suited for multi-carrier, wide bandwidth communications applications.

The ADS58B18 uses TI-proprietary *SNRBoost* technology that can be used to overcome SNR limitation as a result of quantization noise for bandwidth less than Nyquist ($f_s/2$). This device has features such as digital gain and offset correction. The gain option can be used to improve SFDR performance at lower full-scale input ranges, especially at high input frequencies. The integrated dc offset correction loop can be used to estimate and cancel the ADC offset. At lower sampling rates, the ADC automatically operates at scaled-down power with no loss in performance.

The ADS58B18 supports both double data rate (DDR) low-voltage differential signaling (LVDS) and parallel CMOS digital output interfaces. The low data rate of the DDR LVDS interface (maximum 500MBPS) makes it possible to use low-cost field-programmable gate array (FPGA)-based receivers. The ADS58B18 has a low-swing LVDS mode that can be used to further reduce the power consumption. The strength of the LVDS output buffers can also be increased to support 50Ω differential termination.

The ADS58B18 is available in a compact QFN-48 package and is specified over the industrial temperature range (–40°C to +85°C).

PRODUCT PREVIEW


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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FUNCTIONAL BLOCK DIAGRAM

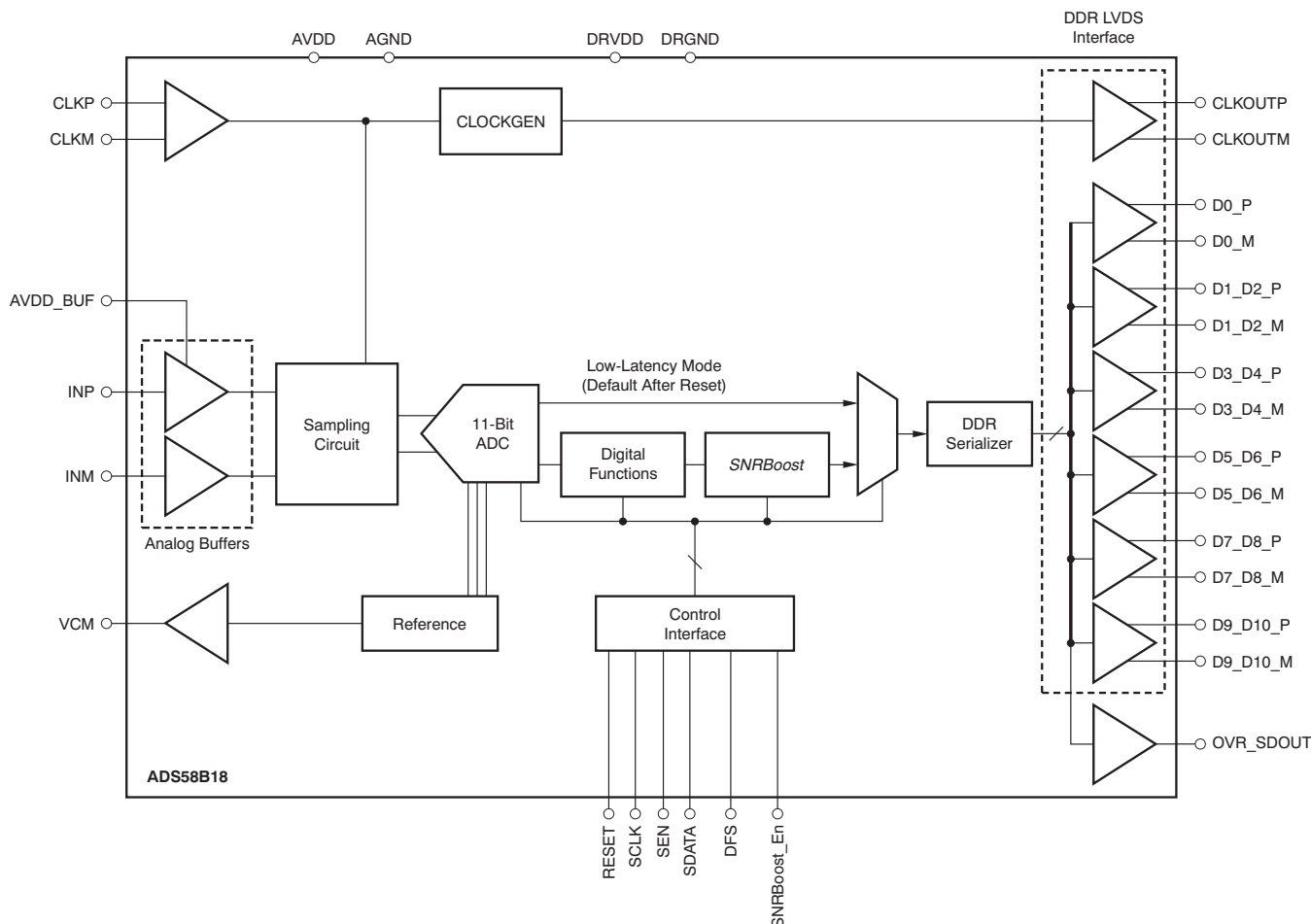


Figure 1. ADS58B18 Block Diagram

ORDERING INFORMATION⁽¹⁾

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	ECO PLAN ⁽²⁾	LEAD/BAL L FINISH	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS58B18	QFN-48	RGZ	-40°C to +85°C	GREEN (RoHS, no Sb/Br)	Cu/NiPdAu	AZ58B18	ADS58B18IRGZR	Tape and reel, TBD
							ADS58B18IRGZT	Tape and reel, TBD

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Eco Plan is the planned eco-friendly classification. Green (RoHS, no Sb/Br): TI defines *Green* to mean Pb-Free (RoHS compatible) and free of Bromine- (Br) and Antimony- (Sb) based flame retardants. Refer to the [Quality and Lead-Free \(Pb-Free\) Data](#) web site for more information.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
ADS58B18IRGZR	PREVIEW	QFN	RGZ	48	2500	TBD	Call TI	Call TI
ADS58B18IRGZT	PREVIEW	QFN	RGZ	48	250	TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

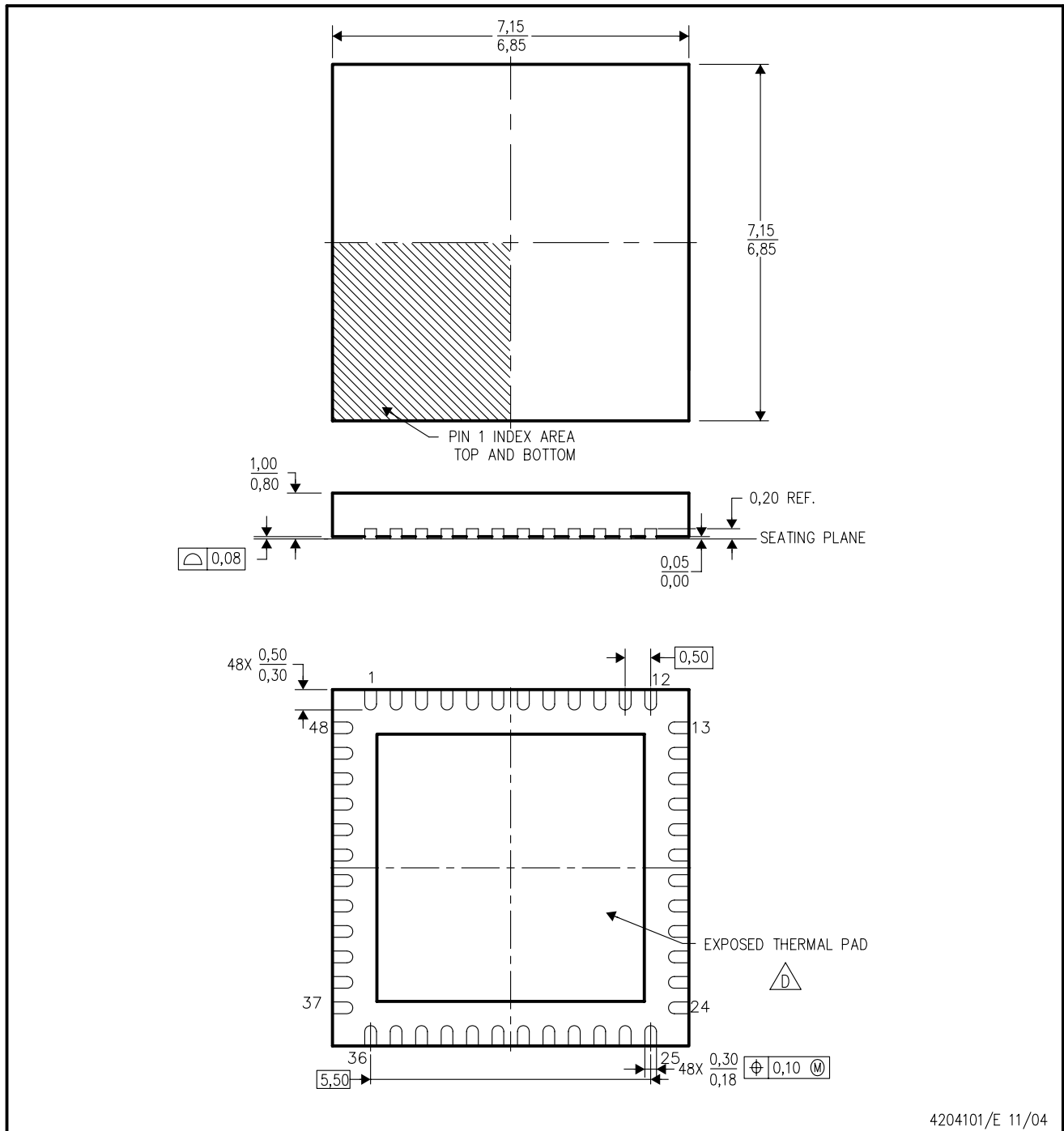
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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RGZ (S-PQFP-N48)

PLASTIC QUAD FLATPACK



4204101/E 11/04

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-leads (QFN) package configuration.
 -  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - E. Falls within JEDEC MO-220.

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