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ADS7950, ADS7951, ADS7952, ADS7953 ADS7954, ADS7955, ADS7956, ADS7957 ADS7958, ADS7959, ADS7960, ADS7961

SLAS605A - JUNE 2008-REVISED JANUARY 2010

12/10/8-Bit, 1 MSPS, 16/12/8/4-Channel, Single-Ended, MicroPower, Serial Interface ADCs

Check for Samples: ADS7950, ADS7951, ADS7952, ADS7953, ADS7954, ADS7955, ADS7956, ADS7957, ADS7958, ADS7959, ADS7960, ADS7961

FEATURES

- 1-MHz Sample Rate Serial Devices
- Product Family of 12/10/8-Bit Resolution
- Zero Latency
- 20-MHz Serial Interface
- Analog Supply Range: 2.7 to 5.25V
- I/O Supply Range: 1.7 to 5.25V
- Two SW Selectable Unipolar, Input Ranges: 0 to 2.5V and 0 to 5V
- Auto and Manual Modes for Channel Selection
- 12,8,4-Channel Devices can Share 16 Channel Device Footprint
- Two Programmable Alarm Levels per Channel
- Four Individually Configurable GPIOs for TSSOP package devices. One GPIO for QFN devices
- Typical Power Dissipation: 14.5 mW (+VA = 5V, +VBD = 3V) at 1 MSPS
- Power-Down Current (1 μA)
- Input Bandwidth (47 MHz at 3dB)
- 38-,30-Pin TSSOP and 32-,24-Pin QFN Packages

APPLICATIONS

- PLC / IPC
- Battery Powered Systems
- Medical Instrumentation
- Digital Power Supplies
- Touch Screen Controllers
- High-Speed Data Acquisition Systems
- High-Speed Closed-Loop Systems

DESCRIPTION

The ADS79XX is a 12/10/8-bit multichannel analog-to-digital converter family. The following table shows all twelve devices from this product family.

The devices include a capacitor based SAR A/D converter with inherent sample and hold.

The devices accept a wide analog supply range from 2.7V to 5.25V. Very low power consumption makes these devices suitable for battery-powered and isolated power supply applications.

A wide 1.7V to 5.25V I/O supply range facilitates a glue-less interface with the most commonly used CMOS digital hosts.

The serial interface is controlled by $\overline{\text{CS}}$ and SCLK for easy connection with microprocessors and DSP.

The input signal is sampled with the falling edge of $\overline{\text{CS}}$. It uses SCLK for conversion, serial data output, and reading serial data in. The devices allow auto sequencing of preselected channels or manual selection of a channel for the next conversion cycle.

There are two software selectable input ranges (0V - 2.5V and 0V - 5V), four individually configurable GPIOs (in case of TSSOP package devices), and two programmable alarm thresholds per channel. These features make the devices suitable for most data acquisition applications.

The devices offer an attractive power-down feature. This is extremely useful for power saving when the device is operated at lower conversion speeds.

The 16/12-channel devices from this family are available in a 38-pin TSSOP and 32 pin QFN package and the 4/8-channel devices are available in a 30-pin TSSOP and 24 pin QFN packages.

MICROPOWER MULTI-CHANNEL ADS79XX FAMILY

NUMBER OF	RESOLUTION					
CHANNELS	12 BIT	10 BIT	8 BIT			
16	ADS7953	ADS7957	ADS7961			
12	ADS7952	ADS7956	ADS7960			
8	ADS7951	ADS7955	ADS7959			
4	ADS7950	ADS7954	ADS7958			



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



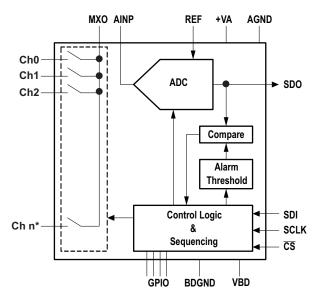
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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ADS79XX BLOCK DIAGRAM



NOTE: n* is number of channels (16,12,8, or 4) depending on the device from the ADS79XX product family.

NOTE: 4 number of GPIO are available in TSSOP package devices only, QFN package devices offer only one GPIO.



ORDERING INFORMATION - 12-BIT

MODEL	MAXIMUM INTEGRAL LINEARITY (LSB)	MAXIMUM DIFFERENTIAL LINEARITY (LSB)	NO MISSING CODES AT RESOLUTION (BIT)	NUMBER OF CHANNELS	PACKAGE TYPE	PACKAGE DESIGNATOR	TEMPERATURE RANGE	ORDERING INFORMATION	TRANSPORT MEDIA QTY																						
					38 pin TSSOP	DBT		ADS7953SBDBT	Tube, 50																						
ADS7953 SB				16	36 piii 1330P	DBT		ADS7953SBDBTR	Reel, 2000																						
ADO1333 OD				10	32 pin QFN	RHB		ADS7953SBRHBT	Tube, 250																						
					32 piii Qi 14	KIID		ADS7953SBRHBR	Reel, 3000																						
					38 pin TSSOP	DBT		ADS7952SBDBT	Tube, 50																						
ADS7952 SB				12	36 piii 1330F	DBT		ADS7952SBDBTR	Reel, 2000																						
AD37932 3B				12	32 pin QFN	RHB		ADS7952SBRHBT	Tube, 250																						
	±1	±1	12		32 pin Qi N	KIID	-40°C to 125°C	ADS7952SBRHBR	Reel, 3000																						
	ΞI	Ξ'	12		30 pin TSSOP	DBT	-40 C to 125 C	ADS7951SBDBT	Tube, 50																						
ADS7951 SB				8	30 piii 1330F	DBT		ADS7951SBDBTR	Reel, 2000																						
AD37931 3B					24 pin QFN	RGE		ADS7951SBRGET	Tube, 250																						
					24 pin Qi N	KGL		ADS7951SBRGER	Reel, 3000																						
					30 pin TSSOP	DBT		ADS7950SBDBT	Tube, 50																						
ADS7950 SB					30 piii 1330F	ж рит тосот — ВВТ		ADS7950SBDBTR	Reel, 2000																						
AD37930 3B					•	24 pin QFN	RGE		ADS7950SBRGET	Tube, 250																					
					24 pin Qi N	KGL		ADS7950SBRGER	Reel, 3000																						
				16	16	38 pin TSSOP	DBT		ADS7953SDBT	Tube, 50																					
ADS7953 S						16	30 pii 1000i	551		ADS7953SDBTR	Reel, 2000																				
AD37333 3							10	10	10	10	10		10	10	10	10	10	10	10	16	16	16	16	16	16	16	16	10	10	32 pin QFN	RHB
					32 pin Qi N	KIID		ADS7953SRHBR	Reel, 3000																						
					38 pin TSSOP	DBT		ADS7952SDBT	Tube, 50																						
ADS7952 S				12	36 piii 1330F	DB1		ADS7952SDBTR	Reel, 2000																						
AD31932 3				12	32 pin QFN	RHB		ADS7952SRHBT	Tube, 250																						
	±1.5	±2	11		32 pin Qi N	KIID	-40°C to 125°C	ADS7952SRHBR	Reel, 3000																						
	11.0	<u></u>			30 pin TSSOP	DBT	-40 O to 125 O	ADS7951SDBT	Tube, 50																						
ADS7951S				8	30 piii 1000i	551		ADS7951SDBTR	Reel, 2000																						
AD379313					24 pin QFN	RGE		ADS7951SRGET	Tube, 250																						
					24 pin Qi N	NGL		ADS7951SRGER	Reel, 3000																						
					30 pin TSSOP	DBT		ADS7950SDBT	Tube, 50																						
ADS7950 S					4	4	30 piii 1330P	DBT		ADS7950SDBTR	Reel, 2000																				
VD91800 9				4	24 pin QFN	RGE		ADS7950SRGET	Tube, 250																						
					24 PIII QFN	KGE		ADS7950SRGER	Reel, 3000																						

ORDERING INFORMATION - 10-BIT

ORDERING INFORMATION - 10-BIT																								
MODEL	MAXIMUM INTEGRAL LINEARITY (LSB)	MAXIMUM DIFFERENTIAL LINEARITY (LSB)	NO MISSING CODES AT RESOLUTION (BIT)	NUMBER OF CHANNELS	PACKAGE TYPE	PACKAGE DESIGNATOR	TEMPERATURE RANGE	ORDERING INFORMATION	TRANSPORT MEDIA QTY															
						20 min TCCOD	DDT		ADS7957SDBT	Tube, 50														
AD07057.0				40	38 pin TSSOP	DBT		ADS7957SDBTR	Reel, 2000															
ADS7957 S				16	32 pin QFN	RHB		ADS7957SRHBT	Tube, 250															
				32 piii Qi N	КПБ		ADS7957SRHBR	Reel, 3000																
									42	20 min TCCOD	DBT		ADS7956SDBT	Tube, 50										
ADS7956 S				40	12	12	10	40		40	10	12	12	12	12	12	38 pin TSSOP	DBT		ADS7956SDBTR	Reel, 2000			
ADS/930 S																	32 pin QFN	RHB		ADS7956SRHBT	Tube, 250			
	±0.5	±0.5	10		32 pin QFN	КПВ	-40°C to 125°C	ADS7956SRHBR	Reel, 3000															
	±0.5	±0.5	10		00 min T000D	30 pin TSSOP	DBT	-40 C to 125 C	ADS7955SDBT	Tube, 50														
ADS7955 S									0	0	•				0	0	0	0	8	30 piii 1330F	ОВТ		ADS7955SDBTR	Reel, 2000
ADS/900 S				0	24 pin OFN	RGE		ADS7955SRGET	Tube, 250															
					24 pin QFN	RGE		ADS7955SRGER	Reel, 3000															
					30 pin TSSOP	DBT		ADS7954SDBT	Tube, 50															
ADS7954 S				4	4	4	4	4	4	4	4	4	4	4	4	30 pm 1550P	DBT		ADS7954SDBTR	Reel, 2000				
AD01904 0																4	24 nin OFN	DOE		ADS7954SRGET	Tube, 250			
					24 pin QFN RGE		NGE		Reel, 3000															



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ORDERING INFORMATION - 8-BIT

MODEL	MAXIMUM INTEGRAL LINEARITY (LSB)	MAXIMUM DIFFERENTIAL LINEARITY (LSB)	NO MISSING CODES AT RESOLUTION (BIT)	NUMBER OF CHANNELS	PACKAGE TYPE	PACKAGE DESIGNATOR	TEMPERATURE RANGE	ORDERING INFORMATION	TRANSPORT MEDIA QTY						
					00 -:- T000D	DBT		ADS7961SDBT	Tube, 50						
ADS7961 S				40	38 pin TSSOP	DBT		ADS7961SDBTR	Reel, 2000						
AD5/961 5				16	22 nin OFN	DUD		ADS7961SRHBT	Tube, 250						
					32 pin QFN	RHB		ADS7961SRHBR	Reel, 3000						
						00 -i- T000D	DDT		ADS7960SDBT	Tube, 50					
40070000							40	40	40	40	40		38 pin TSSOP	DBT	
ADS7960 S				12		51.15		ADS7960SRHBT	Tube, 250						
					32 pin QFN	oin QFN RHB	4000 4- 40500	ADS7960SRHBR	Reel, 3000						
	±0.3	±0.3	8		00 -i- T000D	DBT	-40°C to 125°C	ADS7959SDBT	Tube, 50						
4 DO7050 O					30 pin TSSOP	DBT		ADS7959SDBTR	Reel, 2000						
ADS7959 S				8	O4 = i= OFN	DOE		ADS7959SRGET	Tube, 250						
					24 pin QFN	RGE		ADS7959SRGER	Reel, 3000						
					00 -i- T000D	DDT	1	ADS7958SDBT	Tube, 50						
4007050.0					30 pin TSSOP	DBT		ADS7958SDBTR	Reel, 2000						
ADS7958 S				4		205	1	ADS7958SRGET	Tube, 250						
					24 pin QFN	RGE		ADS7958SRGER	Reel, 3000						

ABSOLUTE MAXIMUM RATINGS(1)

	VALUE	UNIT
AINP or CHn to AGND	-0.3 to +VA +0.3	V
+VA to AGND, +VBD to BDGND	-0.3 to +7.0	V
Digital input voltage to BDGND	-0.3 to (7.0)	V
Digital output to BDGND	-0.3 to (+VA + 0.3)	V
Operating temperature range	-40 to 125	°C
Storage temperature range	-65 to 150	°C
Junction temperature (T _J Max)	150	°C
Power dissipation	$(T_J Max-T_A)/\theta_{JA}$	
θ_{JA} thermal impedance, DBT Package	100.6	°C/W
θ_{JA} thermal impedance, RHB Package	34	°C/W
θ_{JA} thermal impedance, RGE Package	38	°C/W
DBT packaged versions of ADS79XX family devices are rated for MSL2 260°C per the JSTD-020 specifications and the RGE and RHB packaged versions of ADS79XX family devices are rated for MSL3 260C per JSTD-020 specifications		

⁽¹⁾ Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.





ELECTRICAL CHARACTERISTICS, ADS7950/51/52/53

 $+VA = 2.7 \text{ V to } 5.25 \text{ V}, +VBD = 1.7 \text{ V to } 5.25 \text{ V}, \text{ V}_{ref} = 2.5 \text{ V} \pm 0.1 \text{ V}, \text{ T}_{A} = -40 ^{\circ}\text{C} \text{ to } 125 ^{\circ}\text{C}, \text{ f}_{sample} = 1 \text{ MHz (unless otherwise noted)}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT					
5 11 1 1 (1)	Range 1	0		Vref	.,
Full-scale input span ⁽¹⁾	Range 2 while 2Vref ≤ +VA	0		2*Vref	V
Absolute input years	Range 1	-0.20		VREF +0.20	V
Absolute input range	Range 2 while 2Vref ≤ +VA	-0.20		2*VREF +0.20	V
Input capacitance			15		ρF
Input leakage current	T _A = 125°C		61		nA
SYSTEM PERFORMANCE					
Resolution			12		Bits
	ADS795XSB (2)	12			i
No missing codes	ADS795XS ⁽²⁾	11			Bits
	ADS795XSB ⁽²⁾	-1	±0.5	1	. 25 (3)
Integral linearity	ADS795XS ⁽²⁾	-1.5	±0.75	1.5	LSB ⁽³⁾
	ADS795XSB ⁽²⁾	-1	±0.5	1	
Differential linearity	ADS795XS ⁽²⁾	-2	±0.75	1.5	LSB
Offset error ⁽⁴⁾		-3.5	±1.1	3.5	LSB
	Range 1	-2	±0.2	2	
Gain error	Range 2		±0.2		LSB
Total unadjusted error (TUE)			±2		LSB
SAMPLING DYNAMICS					
Conversion time	20 MHz sclk			800	nSec
Acquisition time		325			nSec
Maximum throughput rate	20 MHz sclk			1.0	MHz
Aperture delay			5		nsec
Step response			150		nsec
Over voltage recovery			150		nsec
DYNAMIC CHARACTERISTICS					
Total harmonic distortion (5)	100 kHz		-82		dB
Signal-to-noise ratio	100 kHz, ADS795XSB ⁽²⁾	70	71.7		dB
	100 kHz, ADS795XS ⁽²⁾	70	71.7		
Signal-to-noise + distortion	100 kHz, ADS795XSB ⁽²⁾	69	71.3		dB
	100 kHz, ADS795XS ⁽²⁾	68	71.3		
Spurious free dynamic range	100 kHz		84		dB
Small signal bandwidth	At –3 dB		47		MHz
Channel to channel assessells	Any off-channel with 100kHz, Full-scale input to channel being sampled with DC input (isolation crosstalk).		-95		40
Channel-to-channel crosstalk	From previously sampled to channel with 100kHz, Full-scale input to channel being sampled with DC input (memory crosstalk).		-85		dB

⁽¹⁾ Ideal input span; does not include gain or offset error.

⁽²⁾ ADS795X, where X indicates 0, 1, 2, or 3

⁽³⁾ LSB means Least Significant Bit.

⁽⁴⁾ Measured relative to an ideal full-scale input

⁵⁾ Calculated on the first nine harmonics of the input frequency.



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ELECTRICAL CHARACTERISTICS, ADS7950/51/52/53 (continued)

 $+VA = 2.7 \text{ V to } 5.25 \text{ V}, +VBD = 1.7 \text{ V to } 5.25 \text{ V}, \text{ V}_{ref} = 2.5 \text{ V} \pm 0.1 \text{ V}, \text{ T}_{A} = -40 ^{\circ}\text{C} \text{ to } 125 ^{\circ}\text{C}, \text{ f}_{sample} = 1 \text{ MHz (unless otherwise } 1.0 ^{\circ}\text{C})$ noted)

P	ARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{ref} reference v	oltage at REFP ⁽⁶⁾		2.0	2.5	3.0	V
Reference resis	stance			100		kΩ
ALARM SETTI	NG					
Higher threshol	ld range		0		FFC	Hex
Lower threshold	d range		0		FFC	Hex
DIGITAL INPU	T/OUTPUT					
Logic family		CMOS				
	V _{IH}		0.7*(+VBD)			
	V _{IL}	+VBD = 5 V			0.8	
Logic level	V _{IL}	+VBD = 3 V			3.0 FFC FFC	V
	V _{OH}	At I _{source} = 200 μA	Vdd-0.2			
	V _{OL}	At I _{sink} = 200 μA	0.4			
Data format MS	SB first		MS	B First		
POWER SUPP	LY REQUIREMENTS					
+VA supply vol	tage		2.7	3.3	5.25	V
+VBD supply v	oltage		1.7	3.3	5.25	V
		At +VA = 2.7 to 3.6 V and 1MHz throughput		1.8		mA
Supply current	(narmal mada)	At +VA = 2.7 to 3.6 V static state		1.05		mA
Supply current	(normal mode)	At +VA = 4.7 to 5.25 V and 1 MHz throughput		2.3	3	mA
		At +VA = 4.7 to 5.25 V static state		1.1	5.25 5.25 5.25 1.5	mA
Power-down sta	ate supply current			1		μΑ
+VBD supply co	urrent	$+VA = 5.25V, f_s = 1MHz$		1		mA
Power-up time					1	μSec
Invalid conversions	ions after power up or				1	Number s
TEMPERATUR	RE RANGE	·	. ————			
Specified perfo	rmance		-40		125	°C
		•				

Device is designed to operate over $V_{ref} = 2.0 \text{ V}$ to 3.0 V. However one can expect lower noise performance at $V_{ref} < 2.4 \text{ V}$. This is due to SNR degradation resulting from lowered signal range.

ELECTRICAL CHARACTERISTICS, ADS7954/55/56/57

+VA = 2.7 V to 5.25 V, +VBD = 1.7 V to 5.25 V, $V_{ref} = 2.5 \text{ V} \pm 0.1 \text{ V}$, $T_A = -40 ^{\circ}\text{C}$ to 125 $^{\circ}\text{C}$, $f_{sample} = 1 \text{ MHz}$ (unless otherwise) noted)

PARAMETER	TEST CONDITIONS	MIN	TYP MAX	UNIT
ANALOG INPUT				
Full-scale input span ⁽¹⁾	Range 1	0	Vref	V
Full-scale input span	Range 2 while 2Vref ≤ +VA	0	2*Vref	V
Absolute input range	Range 1	-0.20	VREF +0.20	V
Absolute input range	Range 2 while 2Vref ≤ +VA	-0.20	2*VREF +0.20	V
Input capacitance			15	ρF
Input leakage current	T _A = 125°C		61	nA
SYSTEM PERFORMANCE				
Resolution			10	Bits
No missing codes		10		Bits

Ideal input span; does not include gain or offset error. (1)





ELECTRICAL CHARACTERISTICS, ADS7954/55/56/57 (continued)

+VA = 2.7 V to 5.25 V, +VBD = 1.7 V to 5.25 V, V_{ref} = 2.5 V \pm 0.1 V, T_A = -40°C to 125°C, f_{sample} = 1 MHz (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Integral linearity			-0.5	±0.2	0.5	LSB ⁽²⁾
Differential linea	rity		-0.5	±0.2	0.5	LSB
Offset error ⁽³⁾	•		-1.5	±0.5	1.5	LSB
		Range 1	-1	±0.1	1	
Gain error		Range 2		±0.1		LSB
SAMPLING DY	NAMICS					
Conversion time	ı	20 MHz SCLK			800	nSec
Acquisition time			325			nSec
Maximum throug	ghput rate	20 MHz SCLK			1.0	MHz
Aperture delay				5		nsec
Step response				150		nsec
Over voltage red	covery			150		nsec
DYNAMIC CHA	RACTERISTICS				'	
Total harmonic of	distortion (4)	100 kHz		-80		dB
Signal-to-noise r	atio	100 kHz	60			dB
Signal-to-noise -	+ distortion	100 kHz	60			
Spurious free dy	namic range	100 kHz		82		dB
Full power band	width	At -3 dB		47		MHz
		Any off-channel with 100kHz, Full-scale input to channel being sampled with DC input.		-95		
Channel-to-char	nnel crosstalk	From previously sampled to channel with 100kHz, Full-scale input to channel being sampled with DC input.		-85		dB
EXTERNAL RE	FERENCE INPUT	1 1 1				
V _{ref} reference vo	oltage at REFP		2.0	2.5	3.0	V
Reference resist				100		kΩ
ALARM SETTIN	IG				I	
Higher threshold	I range		000		FFC	Hex
Lower threshold			000		FFC	Hex
DIGITAL INPUT	OUTPUT				I	
Logic family		CMOS				
	V _{IH}		0.7*(+VBD)			
	V _{IL}	+VBD = 5 V			0.8	
Logic level	V _{IL}	+VBD = 3 V			0.4	V
_	V _{OH}	At I _{source} = 200 μA	Vdd-0.2			
	V _{OL}	At I _{sink} = 200 μA	0.4			
Data format MSI			MS	B First		
POWER SUPPL	Y REQUIREMENTS	6	+		· · · · · · · · · · · · · · · · · · ·	
+VA supply volta	age		2.7	3.3	5.25	V
+VBD supply vo			1.7	3.3	5.25	V
		At +VA = 2.7 to 3.6 V and 1MHz throughput		1.8		mA
		At +VA = 2.7 to 3.6 V static state		1.05	1	mA
Supply current (normal mode)	At +VA = 4.7 to 5.25 V and 1 MHz throughput		2.3	3	mA
		At +VA = 4.7 to 5.25 V static state		1.1	1.5	mA

⁽²⁾ LSB means Least Significant Bit.

³⁾ Measured relative to an ideal full-scale input

⁽⁴⁾ Calculated on the first nine harmonics of the input frequency.



ELECTRICAL CHARACTERISTICS, ADS7954/55/56/57 (continued)

+VA = 2.7 V to 5.25 V, +VBD = 1.7 V to 5.25 V, $V_{ref} = 2.5 \text{ V} \pm 0.1 \text{ V}$, $T_A = -40 ^{\circ}\text{C}$ to 125 $^{\circ}\text{C}$, $f_{sample} = 1 \text{ MHz}$ (unless otherwise) noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
Power-down state supply current			1		μА		
+VBD supply current	+VA = 5.25V, f _s = 1MHz		1		mA		
Power-up time				1	μSec		
Invalid conversions after power up or reset				1	Numbers		
TEMPERATURE RANGE							
Specified performance		-40		125	°C		

ELECTRICAL CHARACTERISTICS, ADS7958/59/60/61

 $+VA = 2.7 \text{ V to } 5.25 \text{ V}, +VBD = 1.7 \text{ V to } 5.25 \text{ V}, \text{ V}_{ref} = 2.5 \text{ V} \pm 0.1 \text{ V}, \text{ T}_{A} = -40 ^{\circ}\text{C} \text{ to } 125 ^{\circ}\text{C}, \text{ f}_{sample} = 1 \text{ MHz (unless otherwise } 1.0 ^{\circ}\text{C})$ noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT	·	<u> </u>			
[[] [] [] [] [] [] [] [] [] [Range 1	0		Vref	V
Full-scale input span ⁽¹⁾	Range 2 while 2Vref ≤ +VA	0		2*Vref	V
Abaduta input ranga	Range 1	-0.20		VREF +0.20	V
Absolute input range	Range 2 while 2Vref ≤ +VA	-0.20		2*VREF +0.20	V
Input capacitance			15		ρF
Input leakage current	T _A = 125°C		61		nA
SYSTEM PERFORMANCE					
Resolution			8		Bits
No missing codes		8			Bits
Integral linearity		-0.3	±0.1	0.3	LSB ⁽²⁾
Differential linearity		-0.3	±0.1	0.3	LSB
Offset error ⁽³⁾		-0.5	±0.2	0.5	LSB
Gain error	Range 1	-0.6	±0.1	0.6	LSB
Gain endi	Range 2		±0.1		LOD
SAMPLING DYNAMICS					
Conversion time	20 MHz SCLK			800	nSec
Acquisition time		325			nSec
Maximum throughput rate	20 MHz SCLK			1.0	MHz
Aperture delay			5		nsec
Step response			150		nsec
Over voltage recovery			150		nsec
DYNAMIC CHARACTERISTICS	,	•			
Total harmonic distortion (4)	100 kHz		-75		dB
Signal-to-noise ratio	100 kHz	49			dB
Signal-to-noise + distortion	100 kHz	49			
Spurious free dynamic range	100 kHz		-78		dB
Full power bandwidth	At –3 dB		47		MHz

⁽¹⁾ Ideal input span; does not include gain or offset error.

LSB means Least Significant Bit.

Measured relative to an ideal full-scale input

⁽⁴⁾ Calculated on the first nine harmonics of the input frequency.





ELECTRICAL CHARACTERISTICS, ADS7958/59/60/61 (continued)

+VA = 2.7 V to 5.25 V, +VBD = 1.7 V to 5.25 V, V_{ref} = 2.5 V \pm 0.1 V, T_A = -40°C to 125°C, f_{sample} = 1 MHz (unless otherwise noted)

PAR	AMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
		Any off-channel with 100kHz, Full-scale input to channel being sampled with DC input.		-95		
Channel-to-chanr	nel crosstalk	From previously sampled to channel with 100kHz, Full-scale input to channel being sampled with DC input.		-85	5 3.0 0 FF FF S	dB
ETERNAL REFE	RENCE INPUT					
Vref reference vo	Itage at REFP		2.0	2.5	3.0	V
Reference resista	ance			100		kΩ
ALARM SETTING	G					
Higher threshold	range		000		FF	Hex
Lower threshold r	ange		000		FF	Hex
DIGITAL INPUT/	ОИТРИТ					
Logic family		CMOS				
	V _{IH}		0.7*(+VBD)			
	V _{IL}	+VBD = 5 V			0.8	
Logic level	V _{IL}	+VBD = 3 V			0.4	V
	V _{OH}	At I _{source} = 200 μA	Vdd-0.2			
	V _{OL}	At I _{sink} = 200 μA	0.4			
Data format			MS	B First		
POWER SUPPLY	Y REQUIREMENTS					
+VA supply voltage	ge		2.7	3.3	5.25	V
+VBD supply volt	age		1.7	3.3	5.25	V
		At +VA = 2.7 to 3.6 V and 1MHz throughput		1.8		mA
Committee accomment (m	\	At +VA = 2.7 to 3.6 V static state		1.05		mA
Supply current (n	ormai mode)	At +VA = 4.7 to 5.25 V and 1 MHz throughput		2.3	3	mA
		At +VA = 4.7 to 5.25 V static state		1.1	1.5	mA
Power-down state	e supply current			1		μΑ
+VBD supply curi	rent	+VA = 5.25V, f _s = 1MHz		1		mA
Power-up time					1	μSec
Invalid conversion reset	ns after power up or				1	Numbers
TEMPERATURE	RANGE					
Specified perform	nance		-40		125	°C

TIMING REQUIREMENTS (see Figure 45, Figure 46, Figure 47, and Figure 48)

All specifications typical at -40°C to 125°C, +VA = 2.7 V to 5.25 V (unless otherwise specified)

	PARAMETER	TEST CONDITIONS ⁽¹⁾ (2)	MIN	TYP	MAX	UNIT
		+VBD = 1.8 V			16	
t _{conv}	Conversion time	+VBD = 3 V			16	SCLK
		+VBD = 5 V			16	
		+VBD = 1.8 V	40			
tq	Minimum quiet sampling time needed from bus 3-state to start of next conversion	+VBD = 3 V	40			ns
	o state to start of most conversion	+VBD = 5 V	40			

^{(1) 1.8}V specifications apply from 1.7V to 1.9V, 3V specifications apply from 2.7V to 3.6V, 5V specifications apply from 4.75V to 5.25V.

⁽²⁾ With 50-pF load



TIMING REQUIREMENTS (see Figure 45, Figure 46, Figure 47, and Figure 48) (continued)

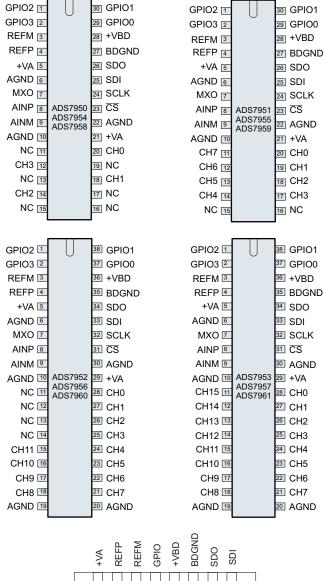
All specifications typical at -40°C to 125°C, +VA = 2.7 V to 5.25 V (unless otherwise specified)

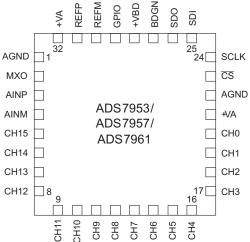
	PARAMETER	TEST CONDITIONS ⁽¹⁾ (2)	MIN	TYP	MAX	UNIT					
		+VBD = 1.8 V			38						
t _{d1}	Delay time, CS low to first data (DO-15) out	+VBD = 3 V			27	ns					
		+VBD = 5 V			17						
		+VBD = 1.8 V	8								
t _{su1}	Setup time, $\overline{\text{CS}}$ low to first rising edge of SCLK	+VBD = 3 V	6			ns					
		+VBD = 5 V	4								
		+VBD = 1.8 V			35						
d2	Delay time, SCLK falling to SDO next data bit valid	+VBD = 3 V			27	ns					
		+VBD = 5 V			17						
		+VBD = 1.8 V	7								
h1	Hold time, SCLK falling to SDO data bit valid	+VBD = 3 V	5			ns					
		+VBD = 5 V	3								
		+VBD = 1.8 V			26						
d ₃	Delay time, 16th SCLK falling edge to SDO 3-state	+VBD = 3 V			22	ns					
		+VBD = 5 V			13						
		+VBD = 1.8 V	2								
t _{su2}	Setup time, SDI valid to rising edge of SCLK	+VBD = 3 V	3			ns					
		+VBD = 5 V	4								
		+VBD = 1.8 V	12								
h2	Hold time, rising edge of SCLK to SDI valid	+VBD = 3 V	10			ns					
		+VBD = 5 V	6			7					
		+VBD = 1.8 V	20								
t _{w1}	Pulse duration CS high	+VBD = 3 V	20			ns					
		+VBD = 5 V	20								
		+VBD = 1.8 V			24						
d4	Delay time CS high to SDO 3-state	+VBD = 3 V			21	ns					
		+VBD = 5 V			12						
		+VBD = 1.8 V	20								
t _{wh}	Pulse duration SCLK high	+VBD = 3 V	20			ns					
		+VBD = 5 V	20								
		+VBD = 1.8 V	20								
wl	Pulse duration SCLK low	+VBD = 3 V	20			ns					
		+VBD = 5 V	20								
		+VBD = 1.8 V			20						
	Frequency SCLK	+VBD = 3 V			20	MHz					
	•	+VBD = 5 V			20						

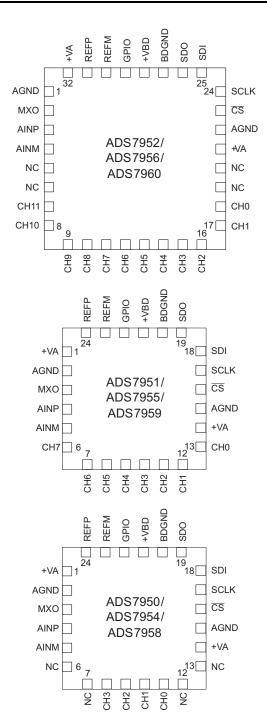


DEVICE INFORMATION

PIN CONFIGURATION (TOP VIEW)







TERMINAL FUNCTIONS - TSSOP PACKAGES

	DEVIC	E NAME							
ADS7953 ADS7957 ADS7961	ADS7952 ADS7956 ADS7960	ADS7951 ADS7955 ADS7959	ADS7950 ADS7954 ADS7958	PIN NAME	I/O	FUNCTION			
	PIN	NO.							
REFERENCE	=								
4	4	4	4	REFP	I	Reference input			
3	3	3	3	REFM	I	Reference ground			



TERMINAL FUNCTIONS - TSSOP PACKAGES (continued)

DEVICE NAME				THORE TOOUT TAC		KAGES (continued)		
ADS7953 ADS7957 ADS7961	ADS7952 ADS7956 ADS7960	ADS7951 ADS7955 ADS7959	ADS7950 ADS7954 ADS7958	PIN NAME	I/O	FUNCTION		
		NO.						
ADC ANALO						[aa.a.		
8	8	8	8	AINP	<u> </u>	Signal input to ADC		
9	9	9	9	AINM	I	ADC input ground		
MULTIPLEXI			-	MAYO		M. Palana and and		
7	7	7	7	MXO	0	Multiplexer output		
28	28	20	20	Ch0	<u> </u>	Analog channels for multiplexer		
27	27	19	18 14	Ch1 Ch2	<u> </u>			
26 25	26 25	18 17	12	Ch2	<u>'</u> 			
	24		-	Ch4	<u>'</u>			
24	23	14		Ch4	<u> </u>			
23	23	12	-	Ch6	<u>'</u>			
21	21	11	-	Cho	<u>'</u>			
18	18	-	-	Ch8	<u>'</u>			
17	17	<u> </u>	-	Ch9	<u>'</u>			
16	16	<u> </u>	-	Ch10	<u>'</u>			
15	15	-	-	Ch11	<u> </u>			
14	-		_	Ch12	· ·			
13	-	-	_	Ch13	<u>.</u>			
12	-	_	_	Ch14	<u> </u>			
11	-	_	-	Ch15	<u>:</u> 			
DIGITAL CO	NTROL SIGN			00	•			
31	31	23	23	CS	1	Chip select input		
32	32	24	24	SCLK	ı	Serial clock input		
33	33	25	25	SDI	l	Serial data input		
34	34	26	26	SDO	0	Serial data output		
GENERAL P		PUTS / OUTP	UTS: These p	ins have prograr	mmable dual	functionality. Refer to Table 8 for functionality		
37	37	29	29	GPIO0	I/O	General purpose input or output		
				High alarm or High/Low alarm	0	Active high output indicating high alarm or high/low alarm depending on programming		
38	38	30	30	GPIO1	I/O	General purpose input or output		
				Low alarm	0	Active high output indicating low alarm		
1	1	1	1	GPIO2	I/O	General purpose input or output		
				Range	1	Selects range: High -> Range 2 / Low -> Range 1		
2	2	2	2	GPIO3	I/O	General purpose input or output		
				PD	1	Active low power down input		
POWER SUF	PPLY AND G	ROUND						
5, 29	5, 29	5, 21	5, 21	+VA	_	Analog power supply		
6, 10, 19, 20, 30	6, 10, 19, 20, 30	6, 10, 22	6, 10, 22	AGND	_	Analog ground		
36	36	28	28	+VBD	_	Digital I/O supply		
35	35	27	27	BDGND	_	Digital ground		
NC PINS								



TERMINAL FUNCTIONS - TSSOP PACKAGES (continued)

	DEVIC	E NAME				
ADS7953 ADS7957 ADS7961	ADS7952 ADS7956 ADS7960	ADS7951 ADS7955 ADS7959	ADS7950 ADS7954 ADS7958	PIN NAME	I/O	FUNCTION
	PIN	I NO.				
_	11, 12, 13, 14	15, 16	11, 13, 15, 16, 17, 19	_	_	Pins internally not connected, do not float these pins

TERMINAL FUNCTIONS - QFN PACKAGES

	DEVIC	E NAME								
ADS7953 ADS7957 ADS7961	ADS7952 ADS7956 ADS7960	ADS7951 ADS7955 ADS7959	ADS7950 ADS7954 ADS7958	PIN NAME	I/O	FUNCTION				
	PIN	NO.								
REFERENCE										
31	31	24	24	REFP	I	Reference input				
30	30	23	23	REFM	I	Reference ground				
ADC ANALO	G INPUT									
3	3	4	4	AINP	I	Signal input to ADC				
4	4	5	5	AINM	I	ADC input ground				
MULTIPLEX	ER	•	•		•	•				
2	2	3	3	MXO	0	Multiplexer output				
20	18	13	11	Ch0	I	Analog-input channels for multiplexer				
19	17	12	10	Ch1	I					
18	16	11	9	Ch2	I					
17	15	10	8	Ch3	I					
16	14	9	=	Ch4	I					
15	13	8	=	Ch5	I					
14	12	7	-	Ch6	I					
13	11	6	-	Ch7	I					
12	10	-	-	Ch8	I					
11	9	-	=	Ch9	I					
10	8	=	=	Ch10	I					
9	7	-	=	Ch11	I					
8	-	-	=	Ch12	I					
7	-	-	-	Ch13	I					
6	=	=	=	Ch14	I					
5	-	-	=	Ch15	I					
DIGITAL CO	NTROL SIGI	NALS								
23	23	16	16	CS	I	Chip select input				
24	24	17	17	SCLK	I	Serial clock input				
25	25	18	18	SDI	I	Serial data input				
26	26	19	19	SDO	0	Serial data output				
GENERAL P	GENERAL PURPOSE INPUT / OUTPUT: This pin has programmable dual functionality. Refer to Table 8 for functionality programming									
29	29	22	22	GPIO0	I/O	General purpose input or output				
				High alarm or High/Low alarm	0	Active high output indicating high alarm or high/low alarm depending on programming				
POWER SUF	PPLY AND G	ROUND								
21, 32	21, 32	1, 14	1, 14	+VA	_	Analog power supply				



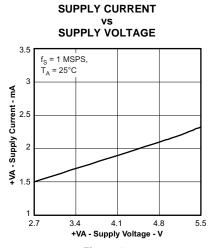


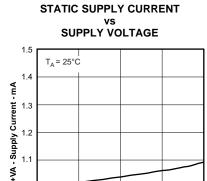
TERMINAL FUNCTIONS - QFN PACKAGES (continued)

	DEVIC	E NAME				
ADS7953 ADS7957 ADS7961	ADS7952 ADS7956 ADS7960	ADS7951 ADS7955 ADS7959	ADS7950 ADS7954 ADS7958	PIN NAME	I/O	FUNCTION
	PIN	NO.				
1, 22	1, 22	2, 15	2, 15	AGND	_	Analog ground
28	28	21	21	+VBD	_	Digital I/O supply
27	27	20	20	BDGND	_	Digital ground
NC PINS						
_	5, 6, 19, 20	_	6, 7, 12, 13	_	_	Pins internally not connected, do not float these pins



TYPICAL CHARATERISTICS (all ADS79XX Family Devices)





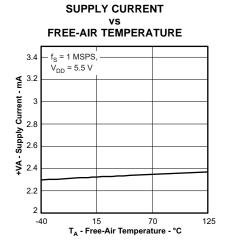


Figure 1.

Figure 2.

4.1

+VA - Supply Voltage - V

4.8

5.5

Figure 3.



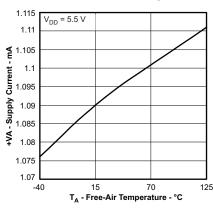
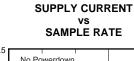
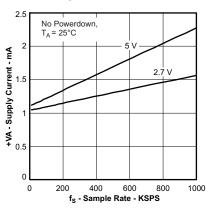


Figure 4.



0.9



SUPPLY CURRENT SAMPLE RATE

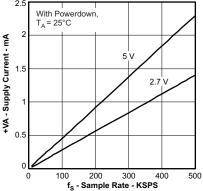


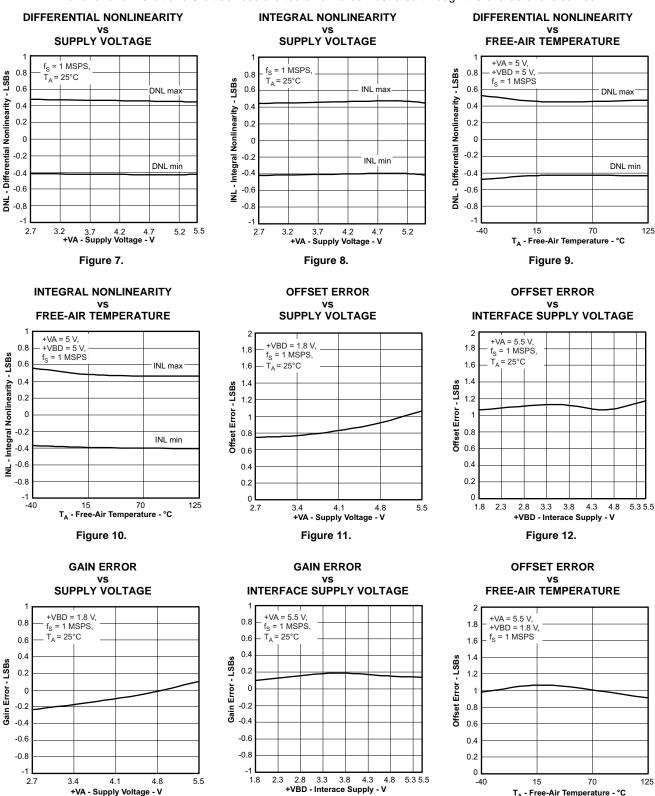
Figure 5.

Figure 6.



TYPICAL CHARACTERISTICS (12-Bit Devices Only)

Variations for 10-bit and 8-bit devices are too small to be illustrated through the characteristic curves



+VA - Supply Voltage - V

Figure 13.

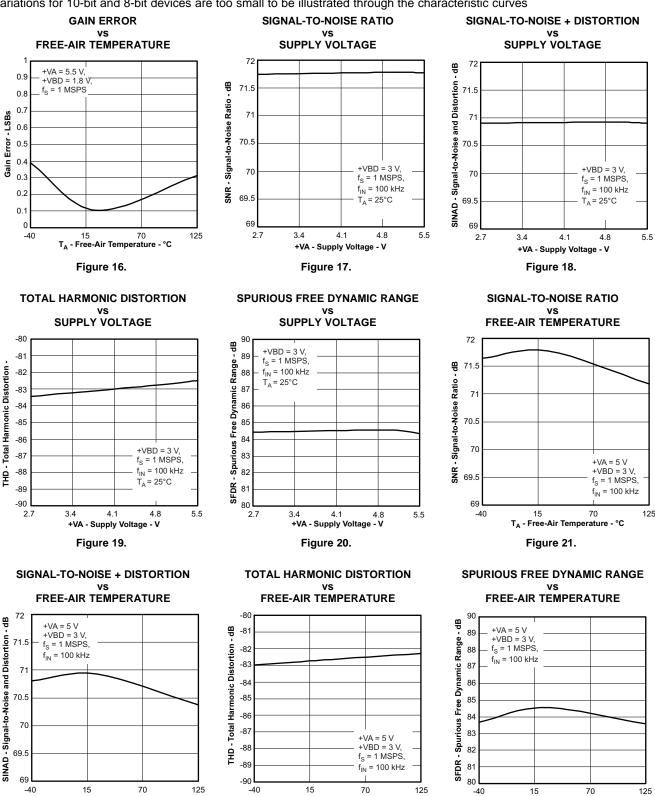
Figure 15.

T_Δ - Free-Air Temperature - °C

Figure 14.



Variations for 10-bit and 8-bit devices are too small to be illustrated through the characteristic curves



T_A - Free-Air Temperature - °C

Figure 22.

Figure 24.

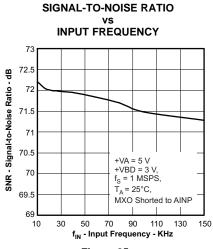
T_A - Free-Air Temperature - °C

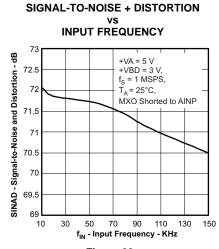
Figure 23.

T_A - Free-Air Temperature - °C



Variations for 10-bit and 8-bit devices are too small to be illustrated through the characteristic curves





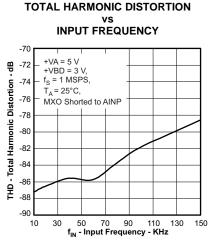


Figure 25.

Figure 26.

Figure 27.

SPURIOUS FREE DYNAMIC RANGE vs INPUT FREQUENCY

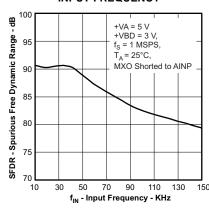


Figure 28.

SIGNAL-TO-NOISE + DISTORTION vs INPUT FREQUENCY (Across Different Source Resistance

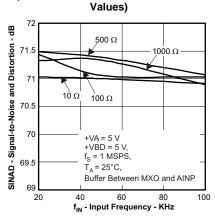


Figure 29.

TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY (Across Different Source Resistance Values)

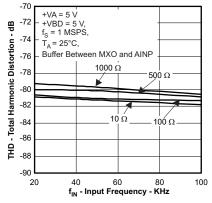


Figure 30.



Variations for 10-bit and 8-bit devices are too small to be illustrated through the characteristic curves

SPURIOUS FREE DYNAMIC RANGE



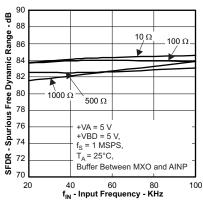


Figure 31.

DIFFERENTIAL NONLINEARITY VARIATION ACROSS CHANNELS

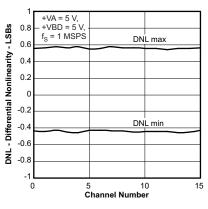


Figure 32.

INTEGRAL NONLINEARITY VARIATION ACROSS CHANNELS

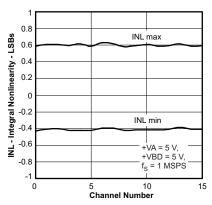


Figure 33.

OFFSET ERROR VARIATION ACROSS CHANNELS

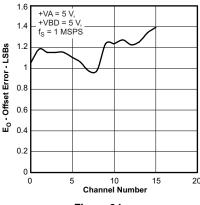


Figure 34.

GAIN ERROR VARIATION ACROSS CHANNELS

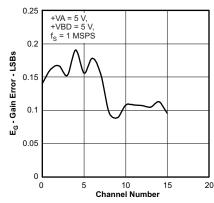


Figure 35.

SIGNAL-TO-NOISE RATIO VARIATION ACROSS CHANNELS

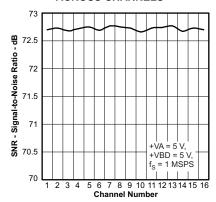
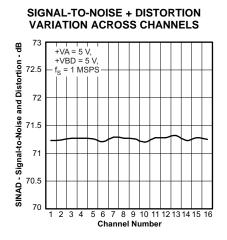
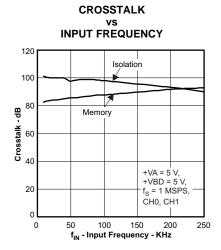


Figure 36.



Variations for 10-bit and 8-bit devices are too small to be illustrated through the characteristic curves





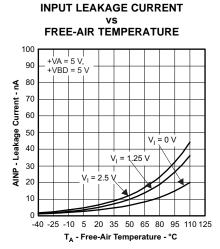
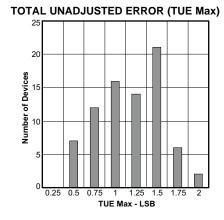


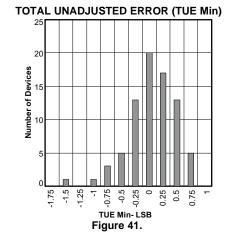
Figure 37.

Figure 38.

Figure 39.









TYPICAL CHARACTERISTICS (12-Bit Devices Only)

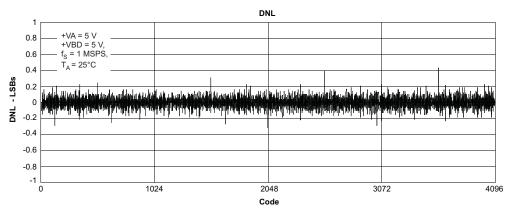


Figure 42.

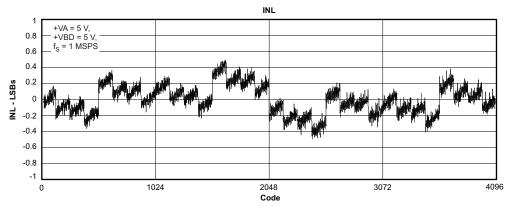


Figure 43.

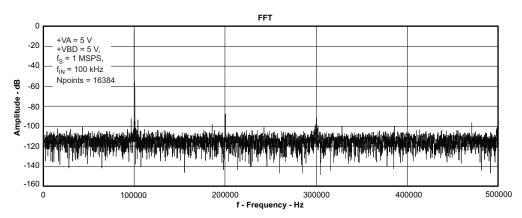


Figure 44.



DETAILED DESCRIPTION

DEVICE OPERATION

The ADS7950 to ADS7961 are 12/10/8-bit multichannel devices. Figure 45, Figure 46, Figure 47, and Figure 48 show device operation timing. Device operation is controlled with CS, SCLK, and SDI. The device outputs its data on SDO.

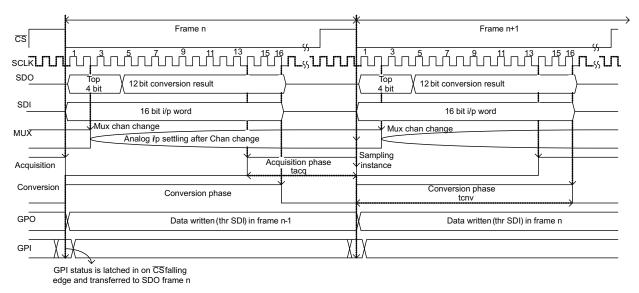


Figure 45. Device Operation Timing Diagram

Each frame begins with the falling edge of \overline{CS} . With the falling edge of \overline{CS} , the input signal from the selected channel is sampled, and the conversion process is initiated. The device outputs data while the conversion is in progress. The 16-bit data word contains a 4-bit channel address, followed by a 12-bit conversion result in MSB first format. There is an option to read the GPIO status instead of the channel address. (Refer to Table 1, Table 2, and Table 5 for more details.)

The device selects a new multiplexer channel on the second SCLK falling edge. The acquisition phase starts on the fourteenth SCLK rising edge. On the next $\overline{\text{CS}}$ falling edge the acquisition phase will end, and the device starts a new frame.

The TSSOP packaged device has four *General Purpose IO* (GPIO) pins, QFN versions have only one GPIO. These four pins can be individually programmed as GPO or GPI. It is also possible to use them for preassigned functions, refer to Table 10. GPO data can be written into the device through the SDI line. The device refreshes the GPO data on the CS falling edge as per the SDI data written in previous frame.

Similarly the device latches GPI status on the \overline{CS} falling edge and outputs the GPI data on the SDO line (if GPI read is enabled by writing DI04=1 in the previous frame) in the same frame starting with the \overline{CS} falling edge.

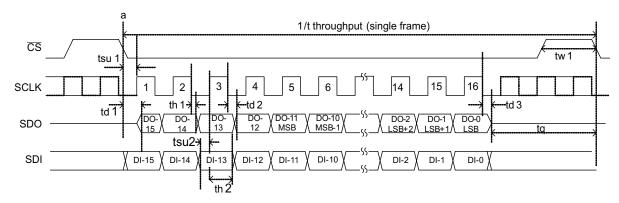


Figure 46. Serial Interface Timing Diagram for 12-Bit Devices (ADS7950/51/52/53)

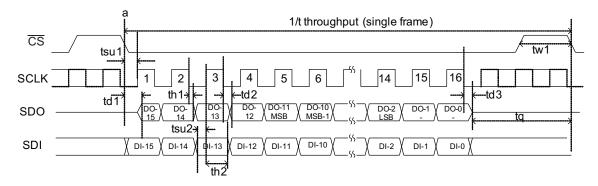


Figure 47. Serial Interface Timing Diagram for 10-Bit Devices (ADS7954/55/56/57)

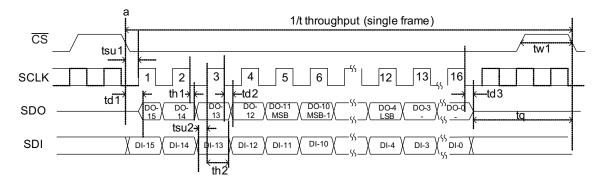


Figure 48. Serial Interface Timing Diagram for 8-Bit Devices (ADS7958/59/60/61)

The falling edge of $\overline{\text{CS}}$ clocks out DO-15 (first bit of the four bit channel address), and remaining address bits are clocked out on every falling edge of SCLK until the third falling edge. The conversion result MSB is clocked out on the 4th SCLK falling edge and LSB on the 15th/13th/11th falling edge respectively for 12/10/8-bit devices. On the 16th falling edge of SCLK, SDO goes to the 3-state condition. The conversion ends on the 16th falling edge of SCLK.

The device reads a sixteen bit word on the SDI pin while it outputs the data on the SDO pin. SDI data is latched on every rising edge of SCLK starting with the 1st clock as shown in Figure 46, Figure 47, and Figure 48.

CS can be asserted (pulled high) only after 16 clocks have elapsed.





The device has two (high and low) programmable alarm thresholds per channel. If the input crosses these limits; the device flags out an alarm on GPIO0/GPIO1 depending on the GPIO program register settings (refer to Table 10). The alarm is asserted (under the alarm conditions) on the 12th falling edge of SCLK in the same frame when a data conversion is in progress. The alarm output is reset on the 10th falling edge of SCLK in the next frame.

The device offers a power-down feature to save power when not in use. There are two ways to powerdown the device. It can be powered down by writing DI05 = 1 in the mode control register (refer to Table 1, Table 2, and Table 5); in this case the device powers down on the 16th falling edge of SCLK in the next data frame. Another way to powerdown the device is through GPIO in the case of the TSSOP packaged devices . GPIO3 can act as the \overline{PD} input (refer to Table 10, to assign this functionality to $\overline{GPIO3}$). This is an asynchronous and active \overline{IOM} input. The device powers down instantaneously after $\overline{GPIO3}$ (\overline{PD}) = 0. The device will power up again on the \overline{CS} falling edge with DI05 = 0 in the mode control register and $\overline{GPIO3}$ (\overline{PD}) = 1.

CHANNEL SEQUENCING MODES

There are three modes for channel sequencing, namely *Manual mode*, *Auto-1 mode*, *Auto-2 mode*. Mode selection is done by writing into the *control register* (refer to Table 1, Table 2, and Table 5). A new multiplexer channel is selected on the second falling edge of SCLK (as shown in Figure 45) in all three modes.

Manual mode: When configured to operate in Manual mode, the next channel to be selected is programmed in each frame and the device selects the programmed channel in the next frame. On powerup or after reset the default channel is 'Channel-0' and the device is in Manual mode.

Auto-1 mode: In this mode the device scans pre-programmed channels in ascending order. A new multiplexer channel is selected every frame on the second falling edge of SCLK. There is a separate 'program register' for pre-programming the channel sequence. Table 3 and Table 4 show Auto-1 'program register' settings.

Once programmed the device retains 'program register' settings until the device is powered down, reset, or reprogrammed. It is allowed to exit and re-enter the Auto-1 mode any number of times without disturbing 'program register' settings.

The Auto-1 program register is reset to FFFF/FF/FF/F hex for the 16/12/8/4 channel devices respectively upon device powerup or reset; implying the device scans all channels in ascending order.

Auto-2 mode: In this mode the user can configure the program register to select the last channel in the scan sequence. The device scans all channels from channel 0 up to and including the last channel in ascending order. The multiplexer channel is selected every frame on the second falling edge of SCLK. There is a separate 'program register' for pre-programming of the last channel in the sequence (multiplexer depth). Table 6 lists the 'Auto-2 prog' register settings for selection of the last channel in the sequence.

Once programmed the device retains program register settings until the device is powered down, reset, or reprogrammed. It is allowed to exit and re-enter Auto-2 mode any number of times, without disturbing the 'program register' settings.

On powerup or reset the bits D9-D6 of the Auto-2 program register are reset to F/B/7/3 hex for the 16/12/8/4 channel devices respectively; implying the device scans all channels in ascending order.

DEVICE PROGRAMMING AND MODE CONTROL

The following section describes device programming and mode control. These devices feature two types of registers to configure and operate the devices in different modes. These registers are referred as 'Configuration Registers'. There are two types of 'Configuration Registers' namely 'Mode control registers' and 'Program registers'.

Mode Control Register

A 'Mode control register' is configured to operate the device in one of three channel sequencing modes, namely Manual mode, Auto-1 Mode, Auto-2 Mode. It is also used to control user programmable features like range selection, device power-down control, GPIO read control, and writing output data into the GPIO.



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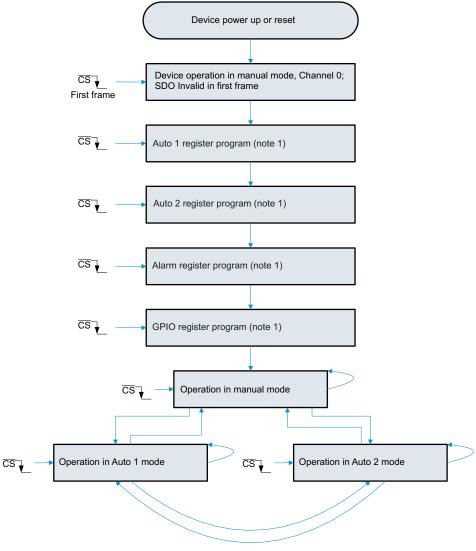
Program Registers

The 'Program registers' are used for device configuration settings and are typically programmed once on powerup or after device reset. There are different program registers such as 'Auto-1 mode programming' for pre-programming the channel sequence, 'Auto-2 mode programming' for selection of the last channel in the sequence, 'Alarm programming' for all 16 channels (or 12,8,4 channels depending on the device) and GPIO for individual pin configuration as GPI or GPO or a pre-assigned function.

DEVICE POWER-UP SEQUENCE

The device power-up sequence is shown in Figure 49. Manual mode is the default power-up channel sequencing mode and Channel-0 is the first channel by default. As explained previously, these devices offer Program Registers to configure user programmable features like GPIO, Alarm, and to pre-program the channel sequence for Auto modes. At 'powerup or on reset' these registers are set to the default values listed in Table 1 to Table 10. It is recommended to program these registers on powerup or after reset. Once configured; the device is ready to use in any of the three channel sequencing modes namely Manual, Auto-1, and Auto-2.





- (1) The device continues its operation in Manual mode channel 0 through out the programming sequence and outputs valid conversion results. It is possible to change channel, range, GPIO by inserting extra frames in between two programming blocks. It is also possible to bypass any programming block if the user does not intent to use that feature.
- (2) It is possible to reprogram the device at any time during operation, regardless of what mode the device is in. During programming the device continues its operation in whatever mode it is in and outputs valid data.

Figure 49. Device Power-Up Sequence

OPERATING IN MANUAL MODE

The details regarding entering and running in Manual channel sequencing mode are illustrated in Figure 50. Table 1 lists the Mode Control Register settings for Manual mode in detail. Note that there are no Program Registers for manual mode.



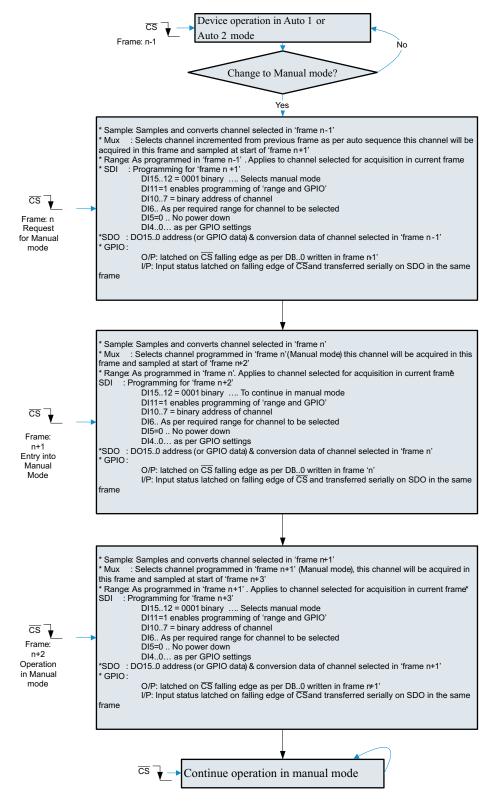


Figure 50. Entering and Running in Manual Channel Sequencing Mode



Table 1. Mode Control Register Settings for Manual Mode

	D=0==			DESCRIPTION							
BITS	RESET STATE	LOGIC STATE		FUNCT	TION						
DI15-12	0001	0001	Selects Manual Mode								
DI11	0	1	Enables programming of	Enables programming of bits DI06-00.							
		0	Device retains values of	Device retains values of DI06-00 from the previous frame.							
DI10-07	0000		data represents the address of the next channel to be selected in the next frame. DI10: MSB and e.g. 0000 represents channel- 0, 0001 represents channel-1 etc.								
DI06	0	0	Selects 2.5V i/p range (Selects 2.5V i/p range (Range 1)							
		1	Selects 5V i/p range (Ra	Selects 5V i/p range (Range 2)							
DI05	0	0	Device normal operation	n (no powerdown)							
		1	Device powers down on	16th SCLK falling edge							
DI04	0	0	SDO outputs current ch result on DO1100.	annel address of the channe	l on DO1512 followed l	by 12 bit conversion					
		1	GPIO3-GPIO0 data (both input and output) is mapped onto DO15-DO12 in the order shown below. Lower data bits DO11-DO00 represent 12-bit conversion result of the current channel.								
			DOI5	DOI4	DOI3	DOI2					
			GPIO3 ⁽¹⁾	GPIO2 ⁽¹⁾	GPIO1 ⁽¹⁾	GPIO0 ⁽¹⁾					
DI03-00	0000		GPIO data for the channels configured as output. Device will ignore the data for the channel which is configured as input. SDI bit and corresponding GPIO information is given below								
			DI03	DI02	DI01	DI00					
			GPIO3 ⁽²⁾	GPIO2 ⁽²⁾	GPIO1 (2)	GPIO0 ⁽²⁾					

⁽¹⁾ GPIO 1 to 3 are available only in TSSOP packaged devices. QFN device offers GPIO 0 only.

⁽²⁾ GPIO 1 to 3 are available only in TSSOP packaged devices. QFN device offers GPIO 0 only.



OPERATING IN AUTO-1 MODE

The details regarding entering and running in Auto-1 channel sequencing mode are illustrated in the flowchart in Figure 51. Table 2 lists the Mode Control Register settings for Auto-1 mode in detail.

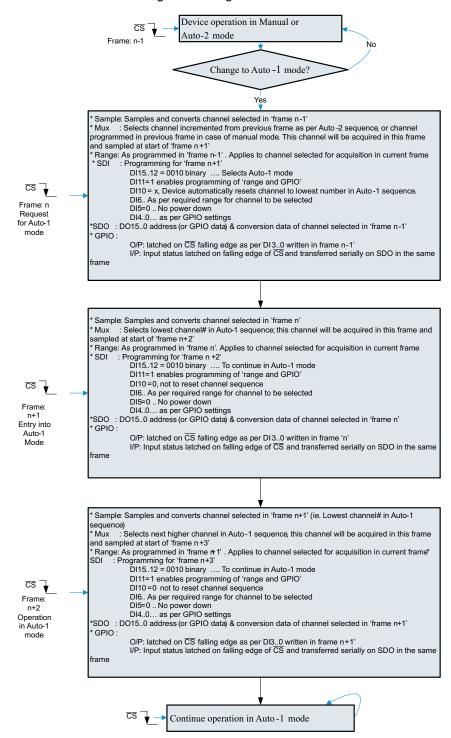


Figure 51. Entering and Running in Auto-1 Channel Sequencing Mode



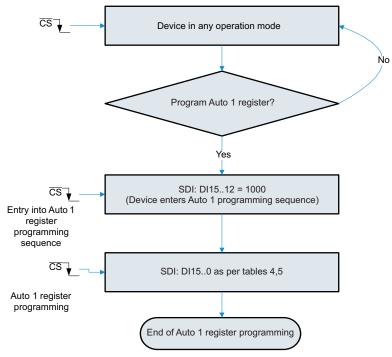
Table 2. Mode Control Register Settings for Auto-1 Mode

	DE055			DESCRIPTION							
BITS	RESET STATE	LOGIC STATE		FUNCT	TION						
DI15-12	0001	0010	Selects Auto-1 Mode								
DI11	0	1	Enables programming of	bits DI10-00.							
		0	Device retains values of	Device retains values of DI10-00 from previous frame.							
DI10	0	1	The channel counter is re	he channel counter is reset to the lowest programmed channel in the Auto-1 Program Register							
		0	The channel counter incr	ne channel counter increments every conversion (No reset)							
DI09-07	000	xxx	Do not care								
DI06	0	0	Selects 2.5V i/p range (R	Selects 2.5V i/p range (Range 1)							
		1	Selects 5V i/p range (Rai	Selects 5V i/p range (Range 2)							
DI05	0	0	Device normal operation	(no powerdown)							
		1	Device powers down on	the 16th SCLK falling edge							
DI04	0	0	SDO outputs current charesult on DO1100.	nnel address of the channe	on DO1512 followed by	12-bit conversion					
		1		n input and output) is mappe 000 represent 12-bit conver							
			DO15	DO14	DO13	DO12					
			GPIO3 ⁽¹⁾ GPIO2 ⁽¹⁾ GPIO1 ⁽¹⁾ GPIO0 ⁽¹⁾								
DI03-00	0000	GPIO data as input. SI	ore the data for the channel	el which is configured							
			DI03 DI02 DI01 DI00								
			GPIO3 ⁽²⁾ GPIO2 ⁽²⁾ GPIO1 ⁽²⁾ GPIO0 ⁽²⁾								

GPIO 1 to 3 are available only in TSSOP packaged devices. QFN device offers GPIO 0 only. GPIO 1 to 3 are available only in TSSOP packaged devices. QFN device offers GPIO 0 only.



The Auto-1 Program Register is programmed (once on powerup or <u>reset</u>) to pre-select the channels for the Auto-1 sequence. Auto-1 Program Register programming requires two \overline{CS} frames for complete programming. In the first \overline{CS} frame the device enters the Auto-1 register programming sequence and in the second frame it programs the Auto-1 Program Register. Refer to <u>Table 2</u>, <u>Table 3</u>, and <u>Table 4</u> for complete details.



NOTE: The device continues its operation in selected mode during programming. SDO is valid, however it is not possible to change the range or write GPIO data into the device during programming.

Figure 52. Auto-1 Register Programming Flowchart

Table 3. Program Register Settings for Auto-1 Mode

DITO	RESET	DESCRIPTION						
BITS	STATE	LOGIC STATE	FUNCTION					
FRAME 1								
DI15-12	NA	1000	Device enters Auto-1 program sequence. Device programming is done in the next frame.					
DI11-00	NA	Do not care						
FRAME 2								
DI15-00	All 1s	1 (individual bit)	A particular channel is programmed to be selected in the channel scanning sequence. The channel numbers are mapped one-to-one with respect to the SDI bits; e.g. DI15 \rightarrow Ch15, DI14 \rightarrow Ch14 DI00 \rightarrow Ch00					
		0 (individual bit)	A particular channel is programmed to be skipped in the channel scanning sequence. The channel numbers are mapped one-to-one with respect to the SDI bits; e.g. DI15 \rightarrow Ch15, DI14 \rightarrow Ch14 DI00 \rightarrow Ch00					

Table 4. Mapping of Channels to SDI Bits for 16,12,8,4 Channel Devices

Device ⁽¹⁾		SDI BITS														
	DI15	DI14	DI13	DI12	DI11	DI10	DI09	DI08	DI07	DI06	DI05	DI04	DI03	DI02	DI01	DI00
16 Chan	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
12 Chan	Χ	Χ	Х	Χ	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
8 Chan	Χ	Χ	Х	Χ	Х	Х	Χ	Х	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
4 Chan	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	1/0	1/0	1/0	1/0

(1) When operating in Auto-1 mode, the device only scans the channels programmed to be selected.



OPERATING IN AUTO-2 MODE

The details regarding entering and running in Auto-2 channel sequencing mode are illustrated in Figure 53. Table 5 lists the Mode Control Register settings for Auto-2 mode in detail.

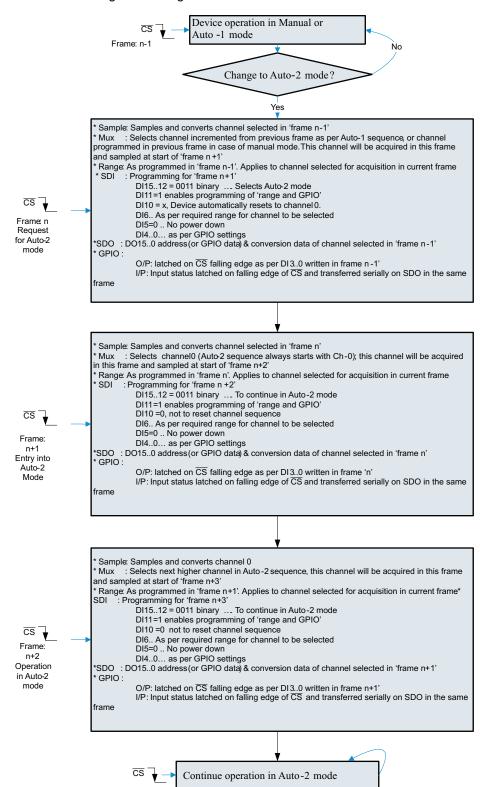


Figure 53. Entering and Running in Auto-2 Channel Sequencing Mode

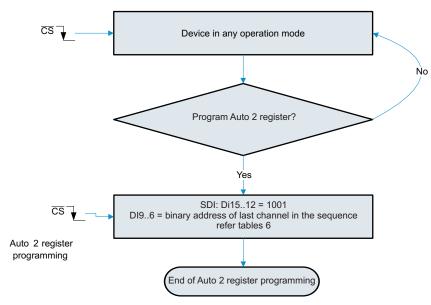


Table 5. Mode Control Register Settings for Auto-2 Mode

	DECET			DESCR	RIPTION						
BITS	RESET STATE	LOGIC STATE	FUNCTION								
DI15-12	0001	0011	Selects Auto-2 Mo	de							
DI11	0	1	Enables programm	nables programming of bits DI10-00.							
		0	Device retains valu	ues of DI10-00 from the pr	revious frame.						
DI10	0	1	Channel number is	reset to Ch-00.							
		0	Channel counter in	ncrements every conversion	on.(No reset).						
DI09-07	000	xxx	Do not care								
DI06	0	0	Selects 2.5V i/p ra	Selects 2.5V i/p range (Range 1)							
		1	Selects 5V i/p rang	Selects 5V i/p range (Range 2)							
DI05	0	0	Device normal ope	eration (no powerdown)							
		1	Device powers dov	wn on the 16th SCLK fallir	ng edge						
DI04	0	0	SDO outputs the current channel address of the channel on DO1512 followed by the 12-bit conversion result on DO1100.								
		1	GPIO3-GPIO0 data (both input and output) is mapped onto DO15-DO12 in the order shown below. Lower data bits DO11-DO00 represent the 12-bit conversion result of the current channel.								
			DO15	DO14	DO13	DO12					
			GPIO3 ⁽¹⁾	GPIO2 ⁽¹⁾	GPIO1 ⁽¹⁾	GPIO0 ⁽¹⁾					
DI03-00	0000			nfigured as output. Device g GPIO information is give		nel which is configured as					
			DI03	DI02	DI01	DI00					
			GPIO3 ⁽¹⁾	GPIO2 ⁽¹⁾	GPIO1 ⁽¹⁾	GPIO0 ⁽¹⁾					

⁽¹⁾ GPIO 1 to 3 are available only in TSSOP packaged devices. QFN device offers GPIO 0 only.

The Auto-2 Program Register is programmed (once on powerup or reset) to pre-select the last channel (or sequence depth) in the Auto-2 sequence. Unlike Auto-1 Program Register programming, Auto-2 Program Register programming requires only 1 $\overline{\text{CS}}$ frame for complete programming. See Figure 54 and Table 6 for complete details.



NOTE: The device continues its operation in the selected mode during programming. SDO is valid, however it is not possible to change the range or write GPIO data into the device during programming.

Figure 54. Auto-2 Register Programming Flowchart



Table 6. Program Register Settings for Auto-2 Mode

BITS	RESET STATE	DESCRIPTION	
		LOGIC STATE	FUNCTION
DI15-12	NA	1001	Auto-2 program register is selected for programming
DI11-10	NA	Do not care	
DI09-06	NA	aaaa	This 4-bit data represents the address of the last channel in the scanning sequence. During device operation in Auto-2 mode, the channel counter starts at CH-00 and increments every frame until it equals "aaaa". The channel counter roles over to CH-00 in the next frame.
DI05-00	NA	Do not care	

CONTINUED OPERATION IN A SELECTED MODE

Once a device is programmed to operate in one of the modes, the user may want to continue operating in the same mode. Mode Control Register settings to continue operating in a selected mode are detailed in Table 7.

Table 7. Continued Operation in a Selected Mode

BITS	RESET STATE	DESCRIPTION	
		LOGIC STATE	FUNCTION
DI15-12	0001	0000	The device continues to operate in the selected mode. In Auto-1 and Auto-2 modes the channel counter increments normally, whereas in the Manual mode it continues with the last selected channel. The device ignores data on DI11-DI00 and continues operating as per the previous settings. This feature is provided so that SDI can be held low when no changes are required in the Mode Control Register settings.
DI11-00	All '0'	Device ignores these bits when DI15-12 is set to 0000 logic state	

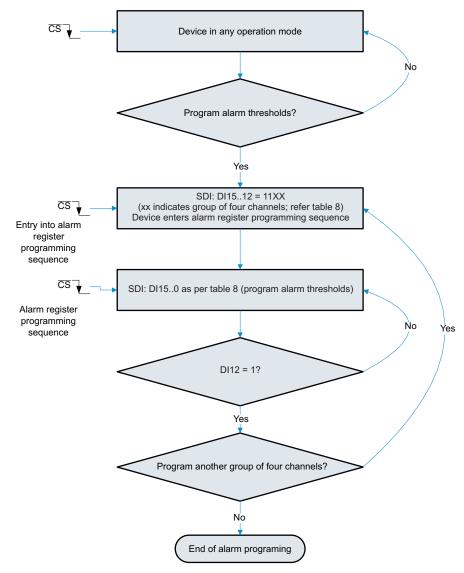
PROGRAMMING ALARM THRESHOLDS

There are two Alarm Program Registers per channel, one for setting the high alarm threshold and the other for setting the low alarm threshold. For ease of programming, two alarm programming registers per channel, corresponding to four consecutive channels, are assembled into one group (a total eight registers). There are four such groups for 16 channel devices and 3/2/1 such groups for 12/8/4 channel devices respectively. The grouping of the various channels for each device in the ADS79XX family is listed in Table 8. The details regarding programming the alarm thresholds are illustrated in the flowchart in Figure 55. Table 9 lists the details regarding the Alarm Program Register settings.

Table 8. Grouping of Alarm Program Registers

GROUP NO.	REGISTERS	APPLICABLE FOR DEVICE
0	High and low alarm for channel 0, 1, 2, and 3	ADS795350, ADS795754, ADS796158
1	High and low alarm for channel 4, 5, 6, and 7	ADS795351, ADS795755, ADS796159
2	High and low alarm for channel 8, 9, 10, and 11	ADS7953 and 52, ADS7957 and 56, ADS7961 and 60
3	High and low alarm for channel 12, 13, 14, and 15	ADS7953, ADS7957, ADS7961

Each alarm group requires 9 $\overline{\text{CS}}$ frames for programming their respective alarm thresholds. In the first frame the device enters the programming sequence and in each subsequent frame it programs one of the registers from the group. The device offers a feature to program less than eight registers in one programming sequence. The device exits the alarm threshold programming sequence in the next frame after it encounters the first 'Exit Alarm Program' bit high.



NOTE: The device continues its operation in selected mode during programming. SDO is valid, however it is not possible to change the range or write GPIO data into the device during programming.

Figure 55. Alarm Program Register Programming Flowchart

Table 9. Alarm Program Register Settings

			raise or raise regram regions.	
BITS	RESET STATE	DESCRIPTION		
		LOGIC STATE	FUNCTION	
FRAME 1				
DI15-12	NA	1100	Device enters 'alarm programming sequence' for group 0	
		1101	Device enters 'alarm programming sequence' for group 1	
		1110	Device enters 'alarm programming sequence' for group 2	
		1111	Device enters 'alarm programming sequence' for group 3	
Note: DI1: format.	5-12 = 11bb is the a	larm progra	imming request for group bb. Here 'bb' represents the alarm programming group number in binary	
DI11-14	NA	Do not care		
FRAME 2	AND ONWARDS			



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Table 9. Alarm Program Register Settings (continued)

			DESCRIPTION						
BITS	RESET STATE	LOGIC STATE	FUNCTION						
DI15-14	NA	СС	Where "cc" represents the lower two bits of the channel number in binary format. The device programs the alarm for the channel represented by the binary number "bbcc". Note that "bb" is programmed in the first frame.						
DI13	NA	1	High alarm register selection						
		0	Low alarm register selection						
DI12	NA	0	Continue alarm programming sequence in next frame						
		1	Exit Alarm Programming in the next frame. Note: If the alarm programming sequence is not terminated using this feature then the device will remain in the alarm programming sequence state and all SDI data will be treated as alarm thresholds.						
DI11-10	NA	xx	Do not care						
DI09-00	All ones for high alarm register and all zeros for low alarm register	word of th Alarm) or compared	t data represents the alarm threshold. The 10-bit alarm threshold is compared with the upper 10-bit e 12-bit conversion result. The device sets off an alarm when the conversion result is higher (High lower (Low Alarm) than this number. For 10-bit devices, all 10 bits of the conversion result are with the set threshold. For 8-bit devices, all 8 bits of the conversion result are compared with DI09 and DI00, 01 are 'do not care'.						

PROGRAMMING GPIO REGISTERS

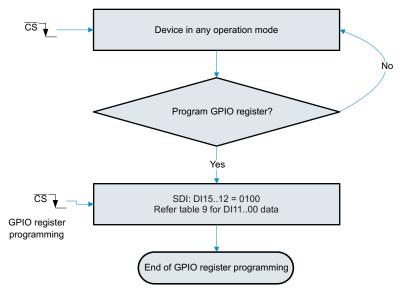
NOTE

GPIO 1 to 3 are available only in TSSOP packaged devices. The QFN device offers 'GPIO 0' only. As a result, all references related to 'GPIO 0' only are valid in the case of QFN package devices.

The device has four General Purpose Input and Output (GPIO) pins. Each of the four pins can be independently programmed as General Purpose Output (GPO) or General Purpose Input (GPI). It is also possible to use the GPIOs for some pre-assigned functions (refer to Table 10 for details). GPO data can be written into the device through the SDI line. The device refreshes the GPO data on every \overline{CS} falling edge as per the SDI data written in the previous frame. Similarly, the device latches GPI status on the \overline{CS} falling edge and outputs it on SDO (if GPI is read enabled by writing DIO4 = 1 during the previous frame) in the same frame starting on the \overline{CS} falling edge.

The details regarding programming the GPIO registers are illustrated in the flowchart in Figure 56. Table 10 lists the details regarding GPIO Register programming settings.





NOTE: The device continues its operation in selected mode during programming. SDO is valid, however it is not possible to change the range or write GPIO data into the device during programming.

Figure 56. GPIO Program Register Programming Flowchart

Table 10. GPIO Program Register Settings

	RESET	DESCRIPTION							
BITS	STATE	LOGIC STATE	FUNCTION						
DI15-12	NA	0100	Device selects GPIO Program Registers for programming.						
DI11-10	00	00	Do not program these bits to any logic state other than '00'						
DI09	0	1	Device resets all registers in the next $\overline{\text{CS}}$ frame to the reset state shown in the corresponding tables (it also resets itself).						
		0	Device normal operation						
DI08	0	1	Device configures GPIO3 as the device power-down input.						
		0	GPIO3 remains general purpose I or O. Program 0 for QFN packaged devices.						
DI07	0	1	Device configures GPIO2 as device range input.						
		0	GPIO2 remains general purpose I or O. Program 0 for QFN packaged devices.						
DI06-04	000	000	GPIO1 and GPIO0 remain general purpose I or O. Valid setting for QFN packaged devices.						
		xx1	Device configures GPIO0 as 'high or low' alarm output. This is an active high output. GPIO1 remains general purpose I or O. Valid setting for QFN packaged devices.						
		010	Device configures GPIO0 as high alarm output. This is an active high output. GPIO1 remains general purpose I or O. Valid setting for QFN packaged devices.						
		100	Device configures GPIO1 as low alarm output. This is an active high output. GPIO0 remains general purpose I or O. Setting not allowed for QFN packaged devices.						
		110	Device configures GPIO1 as low alarm output and GPIO0 as a high alarm output. These are active high outputs. Setting not allowed for QFN packaged devices.						
Note: The	following s	ettings are	valid for GPIO which are not assigned a specific function through bits DI0804						
DI03	0	1	GPIO3 pin is configured as general purpose output. Program 1 for QFN packaged devices.						
		0	GPIO3 pin is configured as general purpose input. Setting not allowed for QFN packaged devices.						
DI02	0	1	GPIO2 pin is configured as general purpose output. Program 1 for QFN packaged devices.						
		0	GPIO2 pin is configured as general purpose input. Setting not allowed for QFN packaged devices.						
DI01	0	1	GPIO1 pin is configured as general purpose output. Program 1 for QFN packaged devices.						
		0	GPIO1 pin is configured as general purpose input. Setting not allowed for QFN packaged devices.						
DI00	0	1	GPIO0 pin is configured as general purpose output. Valid setting for QFN packaged devices.						

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Table 10. GPIO Program Register Settings (continued)

		DESCRIPTION	
BITS	RESET LOGIC STATE		FUNCTION
		0	GPIO0 pin is configured as general purpose input. Valid setting for QFN packaged devices.

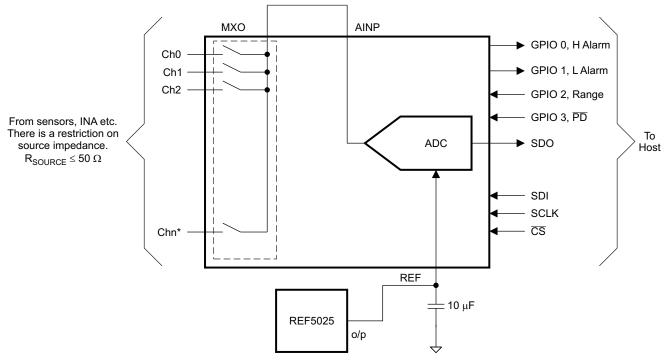


APPLICATION INFORMATION

ANALOG INPUT

The ADS79XX device family offers 12/10/8-bit ADCSs with 16/12/8/4 channel multiplexers for analog input. The multiplexer output is available on the MXO pin. AINP is the ADC input pin. The devices offers flexibility for a system designer as both signals are accessible esternally.

Typically it is convenient to short MXO to the AINP pin so that signal input to each multiplexer channel can be processed independently. In this condition it is recommended to limit source impedance to 50Ω or less. Higher source impedance may affect the signal settling time after a multiplexer channel change. This condition can affect linearity and total harmonic distortion.

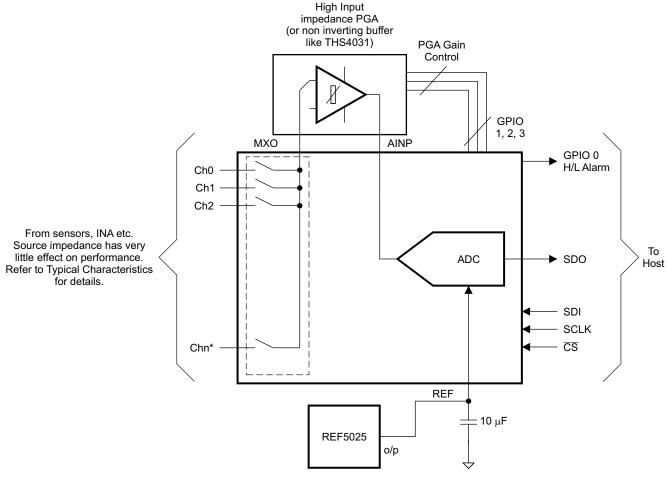


GPIO 1 to 3 are available only in TSSOP packaged devices. QFN device offers 'GPIO 0' only. As a result all references related to 'GPIO 0' only are valid in case of QFN package devices.

Figure 57. Typical Application Diagram Showing MXO Shorted to AINP

Another option is to add a common ADC driver buffer between the MXO and AINP pins. This relaxes the restriction on source impedance to a large extent. Refer to the typical characteristics section for the effect of source impedance on device performance. The typical characteristics show that the device has respectable performance with up to $1k\Omega$ source impedance. This topology (including a common ADC driver) is useful when all channel signals are within the acceptable range of the ADC. In this case the user can save on signal conditioning circuit for each channel.





GPIO 1 to 3 are available only in TSSOP packaged devices. QFN device offers 'GPIO 0' only. As a result all references related to 'GPIO 0' only are valid in case of QFN package devices.

Figure 58. Typical Application Diagram Showing Common Buffer/PGA for all Channels

When the converter samples an input, the voltage difference between AINP and AGND is captured on the internal capacitor array. The (peak) input current through the analog inputs depends upon a number of factors: sample rate, input voltage, and source impedance. The current into the ADS79XX charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current. When the converter goes into hold mode, the input impedance is greater than 1 $G\Omega$.

Care must be taken regarding the absolute analog input voltage. To maintain linearity of the converter, the Ch0 .. Chn and AINP inputs should be within the limits specified. Outside of these ranges, converter linearity may not meet specifications.



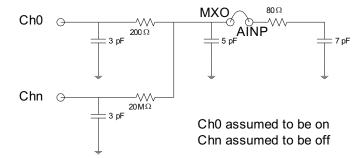


Figure 59. ADC and Mux Equivalent Circuit

REFERENCE

The ADS79XX can operate with an external 2.5V \pm 10mV reference. A clean, low noise, well-decoupled reference voltage on the REF pin is required to ensure good performance of the converter. A low noise band-gap reference like the REF5025 can be used to drive this pin. A 10- μ F ceramic decoupling capacitor is required between the REF and GND pins of the converter. The capacitor should be placed as close as possible to the pins of the device.

POWER SAVING

The ADS79XX devices offer a power-down feature to save power when not in use. There are two ways to powerdown the device. It can be powered down by writing DI05 = 1 in the Mode Control register (refer to Table 1, Table 2 and Table 5); in this case the device powers down on the 16th falling edge of SCLK in the next data frame. Another way to powerdown the device is through GPIO. GPIO3 can act as a \overline{PD} input (refer to Table 10, for assigning this functionality to $\overline{GPIO3}$). This is an asynchronous and active \overline{IOM} input. The device powers down instantaneously after $\overline{GPIO3}$ (\overline{PD}) = 0. The device will powerup again on the \overline{CS} falling edge while DI05 = 0 in the Mode Control register and $\overline{GPIO3}$ (\overline{PD}) = 1.

DIGITAL OUTPUT

As discussed previously in the Device Operation section, the digital output of the ADS79XX devices is SPI compatible. The following table lists the output codes corresponding to various analog input voltages.

Table 11. Ideal Input Voltages and Output Codes for 12-Bit Devices (ADS7950/51/52/53)

DESCRIPTION		ANALOG VALUE	DIGITAL OUTF	TUT
Full scale range	Range 1 \rightarrow V _{ref}	Range 2 → 2xV _{ref}	STRAIGHT BIN	ARY
Least significant bit (LSB)	V _{ref} /4096	2V _{ref} /4096	BINARY CODE	HEX CODE
Full scale	V _{ref} – 1 LSB	2V _{ref} – 1 LSB	1111 1111 1111	FFF
Midscale	V _{ref} /2	V _{ref}	1000 0000 0000	800
Midscale – 1 LSB	V _{ref} /2 – 1 LSB	V _{ref} – 1 LSB	0111 1111 1111	7FF
Zero	0 V	0 V	0000 0000 0000	000

Table 12. Ideal Input Voltages and Output Codes for 10-Bit Devices (ADS7954/55/56/57)

DESCRIPTION		ANALOG VALUE	DIGITAL OUT	TPUT
Full scale range	Range 1 \rightarrow V _{ref}	Range 2 \rightarrow 2×V _{ref}	STRAIGHT BI	NARY
Least significant bit (LSB)	V _{ref} /1024	2V _{ref} /1024	BINARY CODE	HEX CODE
Full scale	V _{ref} – 1 LSB	2V _{ref} – 1 LSB	11 1111 1111	3FF
Midscale	V _{ref} /2	V _{ref}	10 0000 0000	200
Midscale – 1 LSB	V _{ref} /2 – 1 LSB	V _{ref} – 1 LSB	01 1111 1111	1FF
Zero	0 V	0 V	00 0000 0000	000



INSTRUMENTS

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Table 13. Ideal Input Voltages and Output Codes for 8-Bit Devices (ADS7958/59/60/61)

DESCRIPTION		ANALOG VALUE	DIGITAL OUT	PUT
Full scale range	Range 1 \rightarrow V _{ref}	Range 2 \rightarrow 2×V _{ref}	STRAIGHT BIN	IARY
Least significant bit (LSB)	V _{ref} /256	2V _{ref} /256	BINARY CODE	HEX CODE
Full scale	V _{ref} – 1 LSB	2V _{ref} – 1 LSB	1111 1111	FF
Midscale	V _{ref} /2	V_{ref}	1000 0000	80
Midscale – 1 LSB	V _{ref} /2 – 1 LSB	V _{ref} – 1 LSB	0111 1111	7F
Zero	0 V	0 V	0000 0000	00

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REVISION HISTORY

CI	hanges from Original (June 2008) to Revision A	Page
•	Added QFN information to Features	1
•	Added QFN information to Description	1
•	Added QFN information to 12-bit ordering information	3
•	Added QFN information to 10-bit ordering information	3
•	Added QFN information to 8-bit ordering information	4
•	Changed thermal impedance for DBT package in absolute maximum ratings	4
•	Changed thermal impedance for RHB package in absolute maximum ratings	4
•	Changed thermal impedance for RGE package in absolute maximum ratings	4
•	Added V _{ref} = 2.5 V ± 0.1 V to ELECTRICAL CHARACTERISTICS, ADS7950/51/52/53	5
•	Added while 2Vref ≤ +VA to full-scale input span range 2 test conditions	5
•	Added while 2Vref ≤ +VA to full-scale input span range 2 test conditions	5
•	Added Total unadjusted error (TUE) specification	5
•	Changed reference voltage at REFP min and max values	6
•	Added V _{ref} = 2.5 V ± 0.1 V to ELECTRICAL CHARACTERISTICS, ADS7950/51/52/53	6
•	Added Note to ELECTRICAL CHARACTERISTICS, ADS7950/51/52/53	6
•	Added V _{ref} = 2.5 V ± 0.1 V to ELECTRICAL CHARACTERISTICS, ADS7954/55/56/57 test conditions	6
•	Added while 2Vref ≤ +VA to full-scale input span range 2 test conditions	6
•	Added while 2Vref ≤ +VA to full-scale input span range 2 test conditions	6
•	Added V _{ref} = 2.5 V ± 0.1 V to ELECTRICAL CHARACTERISTICS, ADS7954/55/56/57 test conditions	7
•	Changed V _{ref} reference voltage at REFP min value from 2.49 V to 2.0 V	7
•	Changed V _{ref} reference voltage at REFP max value from 2.51 V to 3.0 V	7
•	Added V _{ref} = 2.5 V ± 0.1 V to ELECTRICAL CHARACTERISTICS, ADS7954/55/56/57 test conditions	8
•	Added $V_{ref} = 2.5 \text{ V} \pm 0.1 \text{ V}$ to ELECTRICAL CHARACTERISTICS, ADS7958/59/60/61 test conditions	8
•	Added while 2Vref ≤ +VA to full-scale input span range 2 test conditions	8
•	Added while 2Vref ≤ +VA to full-scale input span range 2 test conditions	8
•	Changed V _{ref} reference voltage at REFP min value from 2.49 V to 2.0 V	9
•	Changed V _{ref} reference voltage at REFP max value from 2.51 V to 3.0 V	9
•	Added V _{ref} = 2.5 V ± 0.1 V to ELECTRICAL CHARACTERISTICS, ADS7958/59/60/61 test conditions	9
•	Changed t _{su1} values from max to min	10
•	Changed t _{su2} values from max to min	10
•	Changed VEE to AGND and VCC to +VA on 38-pin TSSOP pinout	11
•	Added QFN pinout	11
•	Added QFN pinout	12
•	Added QFN pinout	12
•	Added QFN pinout	12
•	Added terminal functions for QFN packages	14
•	Changed ADS7950/4/8 QFN package MXO pin from 7 to 3	14
•	Added TOTAL UNADJUSTED ERROR (TUE Max) graph	21
•	Added TOTAL UNADJUSTED ERROR (TUE Min) graph	21
•	Changed GPIO pins description	23
•	Added device powerdown through GPIO in the case of the TSSOP packaged devices	25
•	Added note to Table 1	29
•	Added note to Table 1	29



TEXAS INSTRUMENTS

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•	Added note to Table 2	3
•	Added note to Table 2	3
•	Added note to Table 5	34
•	Changed DI12 = 1? from No or No to Yes or No in Figure 55	30
•	Added note to Programming GPIO Registers description	3
•	Added QFN information to Table 10	38
•	Added note to Figure 57	40
•	Added note to Figure 58	4



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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Packag Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
ADS7950SBDBT	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7950SBDBTG4	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7950SBDBTR	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7950SBDBTRG4	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7950SBRGER	ACTIVE	VQFN	RGE	24	3000	TBD	Call TI	Call TI
ADS7950SBRGET	ACTIVE	VQFN	RGE	24	250	TBD	Call TI	Call TI
ADS7950SDBT	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7950SDBTG4	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7950SDBTR	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7950SDBTRG4	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7950SRGER	ACTIVE	VQFN	RGE	24	3000	TBD	Call TI	Call TI
ADS7950SRGET	ACTIVE	VQFN	RGE	24	250	TBD	Call TI	Call TI
ADS7951SBDBT	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7951SBDBTG4	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7951SBDBTR	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7951SBDBTRG4	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7951SBRGER	ACTIVE	VQFN	RGE	24	3000	TBD	Call TI	Call TI
ADS7951SBRGET	ACTIVE	VQFN	RGE	24	250	TBD	Call TI	Call TI
ADS7951SDBT	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7951SDBTG4	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7951SDBTR	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7951SDBTRG4	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7951SRGER	ACTIVE	VQFN	RGE	24	3000	TBD	Call TI	Call TI
ADS7951SRGET	ACTIVE	VQFN	RGE	24	250	TBD	Call TI	Call TI
ADS7952SBDBT	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7952SBDBTG4	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7952SBDBTR	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7952SBDBTRG4	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR



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Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp (3)
ADS7952SBRHBR	ACTIVE	QFN	RHB	32	3000	TBD	Call TI	Call TI
ADS7952SBRHBT	ACTIVE	QFN	RHB	32	250	TBD	Call TI	Call TI
ADS7952SDBT	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7952SDBTG4	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7952SDBTR	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7952SDBTRG4	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7952SRHBR	ACTIVE	QFN	RHB	32	3000	TBD	Call TI	Call TI
ADS7952SRHBT	ACTIVE	QFN	RHB	32	250	TBD	Call TI	Call TI
ADS7953SBDBT	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7953SBDBTG4	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAF
ADS7953SBDBTR	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAF
ADS7953SBDBTRG4	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAF
ADS7953SBRHBR	ACTIVE	QFN	RHB	32	3000	TBD	Call TI	Call TI
ADS7953SBRHBT	ACTIVE	QFN	RHB	32	250	TBD	Call TI	Call TI
ADS7953SDBT	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAF
ADS7953SDBTG4	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7953SDBTR	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7953SDBTRG4	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7953SRHBR	ACTIVE	QFN	RHB	32	3000	TBD	Call TI	Call TI
ADS7953SRHBT	ACTIVE	QFN	RHB	32	250	TBD	Call TI	Call TI
ADS7954SDBT	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAF
ADS7954SDBTG4	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAF
ADS7954SDBTR	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7954SDBTRG4	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAF
ADS7954SRGER	ACTIVE	VQFN	RGE	24	3000	TBD	Call TI	Call TI
ADS7954SRGET	ACTIVE	VQFN	RGE	24	250	TBD	Call TI	Call TI
ADS7955SDBT	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)		Level-2-260C-1 YEAR
ADS7955SDBTG4	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7955SDBTR	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAF
ADS7955SDBTRG4	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAF



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Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	n MSL Peak Temp
ADS7955SRGER	ACTIVE	VQFN	RGE	24	3000	TBD	Call TI	Call TI
ADS7955SRGET	ACTIVE	VQFN	RGE	24	250	TBD	Call TI	Call TI
ADS7956SDBT	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YE
ADS7956SDBTG4	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YE
ADS7956SDBTR	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YE
ADS7956SDBTRG4	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YE
ADS7956SRHBR	ACTIVE	QFN	RHB	32	3000	TBD	Call TI	Call TI
ADS7956SRHBT	ACTIVE	QFN	RHB	32	250	TBD	Call TI	Call TI
ADS7957SDBT	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YE
ADS7957SDBTG4	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YE
ADS7957SDBTR	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YE
ADS7957SDBTRG4	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YE
ADS7957SRHBR	ACTIVE	QFN	RHB	32	3000	TBD	Call TI	Call TI
ADS7957SRHBT	ACTIVE	QFN	RHB	32	250	TBD	Call TI	Call TI
ADS7958SDBT	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YE
ADS7958SDBTG4	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YE
ADS7958SDBTR	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YE
ADS7958SDBTRG4	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YE
ADS7958SRGER	ACTIVE	VQFN	RGE	24	3000	TBD	Call TI	Call TI
ADS7958SRGET	ACTIVE	VQFN	RGE	24	250	TBD	Call TI	Call TI
ADS7959SDBT	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YE
ADS7959SDBTG4	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YE
ADS7959SDBTR	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YE
ADS7959SDBTRG4	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YE
ADS7959SRGER	ACTIVE	VQFN	RGE	24	3000	TBD	Call TI	Call TI
ADS7959SRGET	ACTIVE	VQFN	RGE	24	250	TBD	Call TI	Call TI
ADS7960SDBT	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YE
ADS7960SDBTG4	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YE
ADS7960SDBTR	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YE
ADS7960SDBTRG4	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YE



PACKAGE OPTION ADDENDUM

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Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
ADS7960SRHBR	ACTIVE	QFN	RHB	32	3000	TBD	Call TI	Call TI
ADS7960SRHBT	ACTIVE	QFN	RHB	32	250	TBD	Call TI	Call TI
ADS7961SDBT	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7961SDBTG4	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7961SDBTR	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7961SDBTRG4	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7961SRHBR	ACTIVE	QFN	RHB	32	3000	TBD	Call TI	Call TI
ADS7961SRHBT	ACTIVE	QFN	RHB	32	250	TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

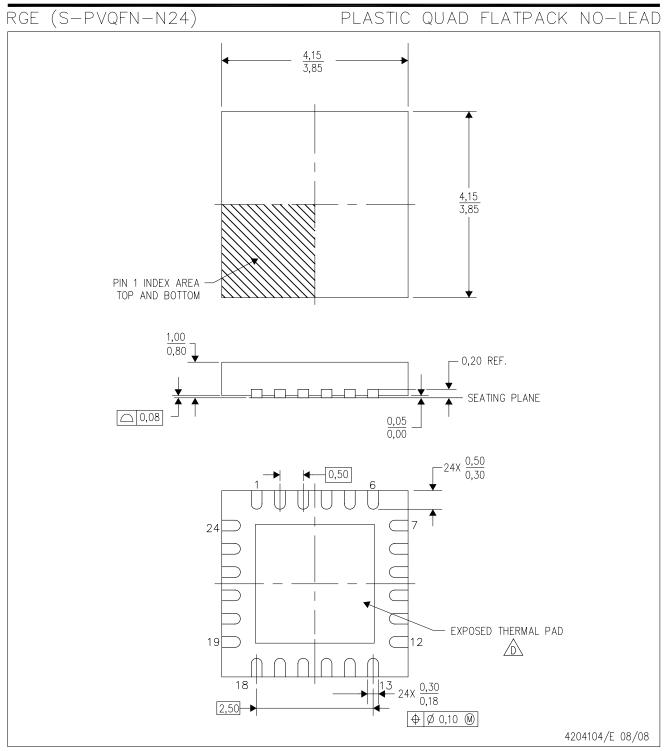
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



- NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-Leads (QFN) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - E. Falls within JEDEC MO-220.



THERMAL PAD MECHANICAL DATA



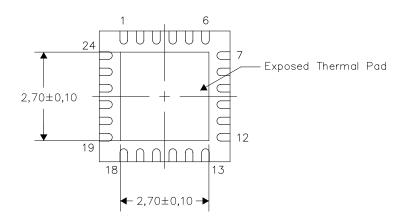
RGE (S-PVQFN-N24)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No—Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



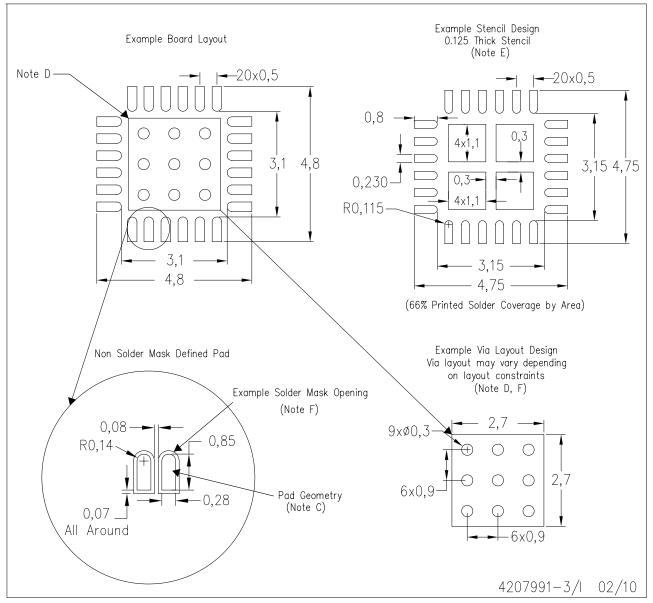
Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGE (S-PVQFN-N24)

PLASTIC QUAD FLATPACK NO-LEAD



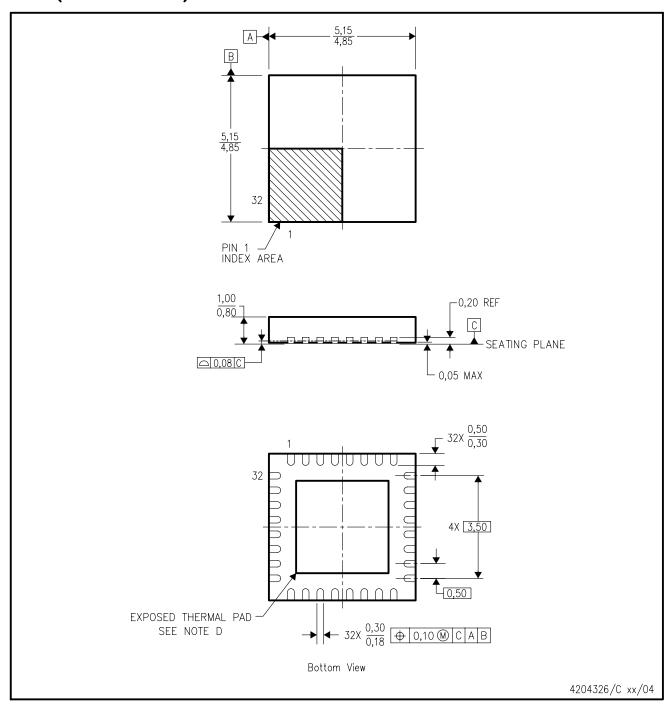
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat—Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com www.ti.com.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.



RHB (S-PQFP-N32)

PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) Package configuration.
- D The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
- E. Falls within JEDEC MO-220.



THERMAL PAD MECHANICAL DATA



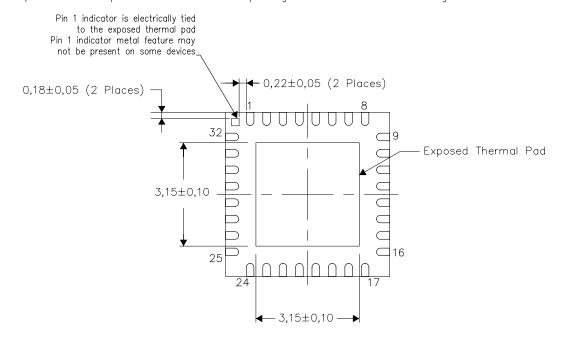
RHB (S-PVQFN-N32)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



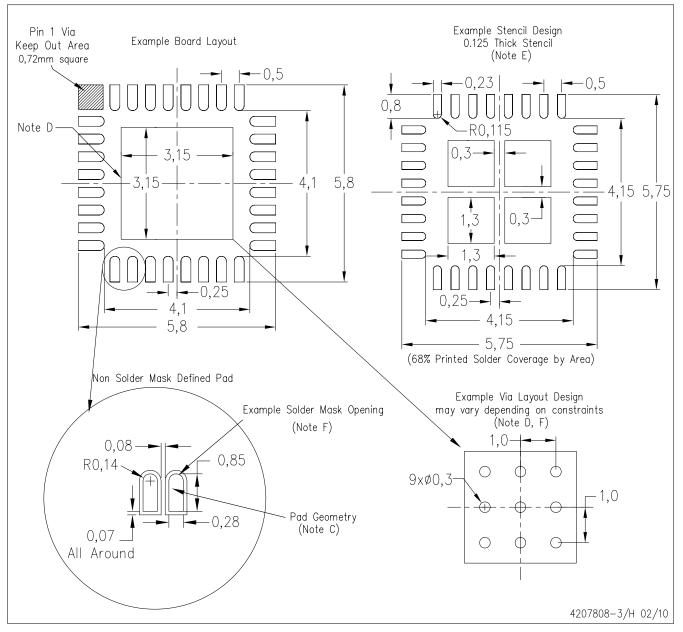
Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RHB (S-PVQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat—Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com http://www.ti.com.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.



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