#### 1. Features

- · Low-voltage and Standard-voltage Operation
  - $-2.7 (V_{CC} = 2.7V \text{ to } 5.5V)$
  - $-1.8 (V_{CC} = 1.8V \text{ to } 5.5V)$
- Three-wire Serial Interface
- 2 MHz Clock Rate (5V) Compatibility
- Self-timed Write Cycle (10 ms max)
- High Reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
- Automotive Grade, Extended Temperature, and Lead-free/Halogen-free Devices Available
- 8-lead PDIP, 8-lead JEDEC SOIC, and 8-lead TSSOP Packages

## 2. Description

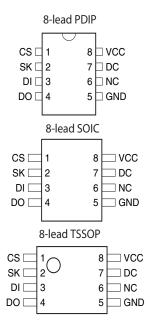
The AT93C46A provides 1024 bits of serial electrically-erasable programmable readonly memory (EEPROM) organized as 64 words of 16 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The AT93C46A is available in space-saving 8lead PDIP, 8-lead JEDEC SOIC, and 8-lead TSSOP packages.

The AT93C46A is enabled through the Chip Select pin (CS) and accessed via a three-wire serial interface consisting of Data Input (DI), Data Output (DO), and Shift Clock (SK). Upon receiving a Read instruction at DI, the address is decoded and the data is clocked out serially on the data output DO pin. The write cycle is completely self-timed and no separate erase cycle is required before write. The write cycle is only enabled when the part is in the erase/write enable state. When CS is brought high following the initiation of a write cycle, the DO pin outputs the ready/busy status of the part.

The AT93C46A is available in 2.7V to 5.5V and 1.8V to 5.5V versions.

Table 2-1.Pin Configuration

Pin Name	Function	
CS	Chip Select	
SK	Serial Data Clock	
DI	Serial Data Input	
DO	Serial Data Output	
GND	Ground	
VCC	Power Supply	



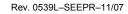


# Three-wire Serial EEPROM

1K (64 x 16)

## **AT93C46A**

Note: Not recommended for new design; please refer to AT93C46E datasheet.







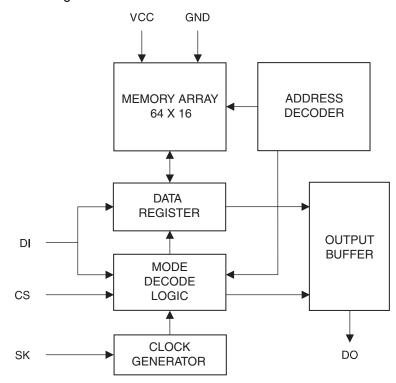
## **Absolute Maximum Ratings\***

Operating Temperature	55°C to +125°C
Storage Temperature	65°C to +150°C
Voltage on Any Pin with Respect to Ground	1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

\*NOTICE:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 2-1. Block Diagram



**Table 2-2.** Pin Capacitance<sup>(1)</sup> Applicable over recommended operating range from  $T_A = 25^{\circ}\text{C}$ , f = 1.0 MHz,  $V_{CC} = +5.0 \text{V}$  (unless otherwise noted)

Symbol	Symbol Test Conditions		Units	Conditions
C <sub>OUT</sub>	Output Capacitance (DO)	5	pF	V <sub>OUT</sub> = 0V
C <sub>IN</sub>	Input Capacitance (CS, SK, DI)	5	pF	V <sub>IN</sub> = 0V

Note: This parameter is characterized and is not 100% tested.

**Table 2-3.** DC Characteristics Applicable over recommended operating range from:  $T_{AI} = -40$ °C to +85°C,  $V_{CC} = +1.8$ V to +5.5V (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Тур	Max	Unit
V <sub>CC1</sub>	Supply Voltage			1.8		5.5	V
V <sub>CC2</sub>	Supply Voltage			2.7		5.5	V
V <sub>CC3</sub>	Supply Voltage			4.5		5.5	V
	0 1 0 11		READ at 1.0 MHz		0.5	2.0	mA
I <sub>cc</sub>	Supply Current	V <sub>CC</sub> = 5.0V	WRITE at 1.0 MHz		0.5	2.0	mA
I <sub>SB1</sub>	Standby Current	V <sub>CC</sub> = 1.8V	CS = 0V		0.4	1.0	μΑ
I <sub>SB2</sub>	Standby Current	V <sub>CC</sub> = 2.7V	CS = 0V		6.0	10.0	μΑ
I <sub>SB3</sub>	Standby Current	V <sub>CC</sub> = 5.0V	CS = 0V		10.0	15.0	μΑ
I <sub>IL</sub>	Input Leakage	V <sub>IN</sub> = 0V to V <sub>CC</sub>	V <sub>IN</sub> = 0V to V <sub>CC</sub>		0.1	1.0	μΑ
I <sub>OL</sub>	Output Leakage	$V_{IN} = 0V \text{ to } V_{CC}$			0.1	1.0	μΑ
V <sub>IL1</sub> (1)	Input Low Voltage	0.714		-0.6		0.8	.,
V <sub>IH1</sub> (1)	Input High Voltage	2.7∨≤\	/ <sub>CC</sub> ≤ 5.5V	2.0		V <sub>CC</sub> + 1	V
V <sub>IL2</sub> <sup>(1)</sup>	Input Low Voltage	4.014)				V <sub>CC</sub> x 0.3	.,
V <sub>IH2</sub> <sup>(1)</sup>	Input High Voltage	$1.8V \le V_{CC} \le 2.7V$		V <sub>CC</sub> x 0.7		V <sub>CC</sub> + 1	V
V <sub>OL1</sub>	Output Low Voltage	0.71/ .1/ 5.51/	I <sub>OL</sub> = 2.1 mA			0.4	V
V <sub>OH1</sub>	Output High Voltage	$2.7V \le V_{CC} \le 5.5V$	$I_{OH} = -0.4 \text{ mA}$	2.4			V

Note: 1.  $V_{IL}$  min and  $V_{IH}$  max are reference only and are not tested.





**Table 2-4.** AC Characteristics Applicable over recommended operating range from  $T_A = -40^{\circ}\text{C}$  to + 85°C,  $V_{CC} = +2.5\text{V}$  to + 5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Тур	Max	Units
$f_{SK}$	SK Clock Frequency	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$	/	0 0 0		2 1 0.25	MHz
t <sub>SKH</sub>	SK High Time	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$	/	250 250 1000			ns
t <sub>SKL</sub>	SK Low Time	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$	/	250 250 1000			ns
t <sub>CS</sub>	Minimum CS Low Time	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$	/	250 250 1000			ns
t <sub>CSS</sub>	CS Setup Time	Relative to SK	$ 4.5V \le V_{CC} \le 5.5V \\ 2.7V \le V_{CC} \le 5.5V \\ 1.8V \le V_{CC} \le 5.5V $	50 50 200			ns
t <sub>DIS</sub>	DI Setup Time	Relative to SK	$ 4.5V \le V_{CC} \le 5.5V \\ 2.7V \le V_{CC} \le 5.5V \\ 1.8V \le V_{CC} \le 5.5V $	100 100 400			ns
t <sub>CSH</sub>	CS Hold Time	Relative to SK		0			ns
t <sub>DIH</sub>	DI Hold Time	Relative to SK	$\begin{array}{l} 4.5V \leq V_{CC} \leq 5.5V \\ 2.7V \leq V_{CC} \leq 5.5V \\ 1.8V \leq V_{CC} \leq 5.5V \end{array}$	100 100 400			ns
t <sub>PD1</sub>	Output Delay to "1"	AC Test	$ 4.5V \le V_{CC} \le 5.5V \\ 2.7V \le V_{CC} \le 5.5V \\ 1.8V \le V_{CC} \le 5.5V $			250 250 1000	ns
t <sub>PD0</sub>	Output Delay to "0"	AC Test	$\begin{array}{c} 4.5 V \leq V_{CC} \leq 5.5 V \\ 2.7 V \leq V_{CC} \leq 5.5 V \\ 1.8 V \leq V_{CC} \leq 5.5 V \end{array}$			250 250 1000	ns
t <sub>SV</sub>	CS to Status Valid	AC Test	$\begin{array}{c} 4.5 \text{V} \leq \text{V}_{CC} \leq 5.5 \text{V} \\ 2.7 \text{V} \leq \text{V}_{CC} \leq 5.5 \text{V} \\ 1.8 \text{V} \leq \text{V}_{CC} \leq 5.5 \text{V} \end{array}$			250 250 1000	ns
t <sub>DF</sub>	CS to DO in High Impedance	AC Test CS = V <sub>IL</sub>	$\begin{array}{c} 4.5 \text{V} \leq \text{V}_{\text{CC}} \leq 5.5 \text{V} \\ 2.7 \text{V} \leq \text{V}_{\text{CC}} \leq 5.5 \text{V} \\ 1.8 \text{V} \leq \text{V}_{\text{CC}} \leq 5.5 \text{V} \end{array}$			100 150 400	ns
t <sub>WP</sub>	Write Cycle Time			0.1	3	10	ms
Endurance <sup>(1)</sup>	5.0V, 25°C			1M			Write Cycle

Note: 1. This parameter is characterized and is not 100% tested.

## 3. Functional Description

The AT93C46A is accessed via a simple and versatile three-wire serial communication interface. Device operation is controlled by seven instructions issued by the host processor. *A valid instruction starts with a rising edge of CS* and consists of a start bit (logic "1") followed by the appropriate op code and the desired memory address location.

**Table 3-1.** Instruction Set for the AT93C46A

			Address	
Instruction	SB	Op Code	x 16	Comments
READ	1	10	$A_5 - A_0$	Reads data stored in memory, at specified address
EWEN	1	00	11XXXX	Write enable must precede all programming modes
ERASE	1	11	$A_5 - A_0$	Erase memory location A <sub>n</sub> – A <sub>0</sub>
WRITE	1	01	$A_5 - A_0$	Writes memory location A <sub>n</sub> – A <sub>0</sub>
ERAL	1	00	10XXXX	Erases all memory locations. Valid only at V <sub>CC</sub> = 4.5V to 5.5V
WRAL	1	00	01XXXX	Writes all memory locations. Valid only at V <sub>CC</sub> = 4.5V to 5.5V
EWDS	1	00	00XXXX	Disables all programming instructions

**READ** (**READ**): The Read (READ) instruction contains the address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the serial output pin DO. Output data changes are synchronized with the rising edges of serial clock SK. It should be noted that a dummy bit (logic "0") precedes the 16-bit data output string.

**ERASE/WRITE ENABLE (EWEN):** To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out. Please note that once in the EWEN state, programming remains enabled until an EWDS instruction is executed or V<sub>CC</sub> power is removed from the part.

**ERASE** (ERASE): The Erase (ERASE) instruction programs all bits in the specified memory location to the logical "1" state. The self-timed erase cycle starts once the Erase instruction and address are decoded. The DO pin outputs the ready/busy status of the part if CS is brought high after being kept low for a minimum of 250 ns ( $t_{CS}$ ). A logic "1" at pin DO indicates that the selected memory location has been erased and the part is ready for another instruction.

**WRITE (WRITE):** The Write (WRITE) instruction contains the 16 bits of data to be written into the specified memory location. The self-timed programming cycle,  $t_{WP}$ , starts after the last bit of data is received at serial data input pin DI. The DO pin outputs the ready/busy status of the part if CS is brought high after being kept low for a minimum of 250 ns ( $t_{CS}$ ). A logic "0" at DO indicates that programming is still in progress. A logic "1" indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions. *A ready/busy status cannot be obtained if the CS is brought high after the end of the self-timed programming cycle, t\_{WP}* 

**ERASE ALL (ERAL):** The Erase All (ERAL) instruction programs every bit in the memory array to the logic "1" state and is primarily used for testing purposes. The DO pin outputs the ready/busy status of the part if CS is brought high after being kept low for a minimum of 250 ns ( $t_{CS}$ ). The ERAL instruction is valid only at  $V_{CC}$  = 5.0V  $\pm$  10%.



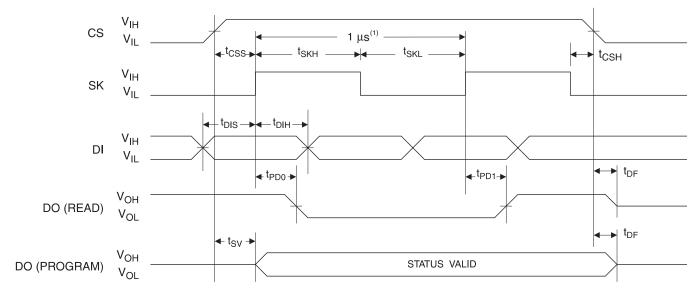


WRITE ALL (WRAL): The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the ready/busy status of the part if CS is brought high after being kept low for a minimum of 250 ns ( $t_{CS}$ ). The WRAL instruction is valid only at  $V_{CC}$  = 5.0V  $\pm$  10%.

**ERASE/WRITE DISABLE (EWDS):** To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the Read instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

## 4. Timing Diagrams

Figure 4-1. Synchronous Data Timing



Note: 1. This is the minimum SK period.

 Table 4-1.
 Organization Key for Timing Diagrams

	AT93C46A		
I/O	x 16		
A <sub>N</sub>	$A_5$		
D <sub>N</sub>	D <sub>15</sub>		

Figure 4-2. READ Timing

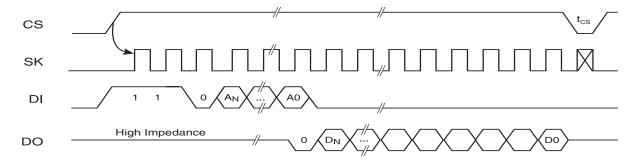
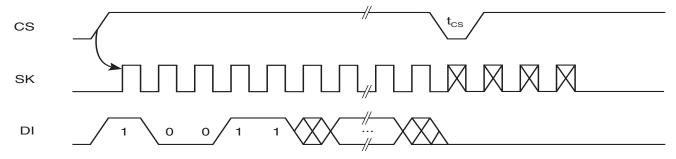
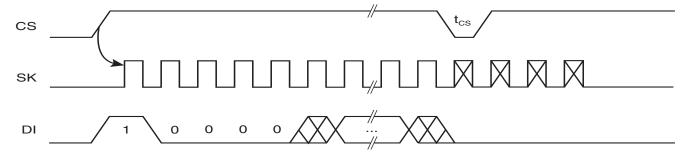


Figure 4-3. EWEN Timing<sup>(1)</sup>



Note: 1. Requires a minimum of nine clock cycles.

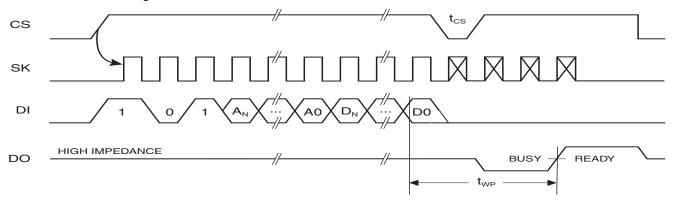
Figure 4-4. EWDS Timing<sup>(1)</sup>



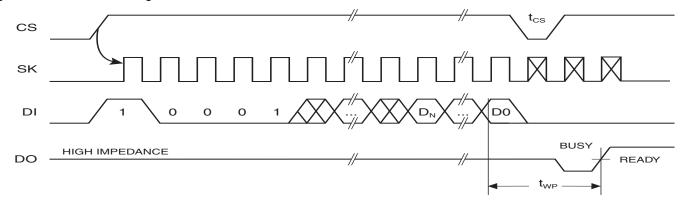
Note: 1. Requires a minimum of nine clock cycles.



Figure 4-5. WRITE Timing



**Figure 4-6.** WRAL Timing<sup>((1)),((2))</sup>



Notes: 1. Valid only at  $V_{CC} = 4.5V$  to 5.5V.

2. Requires a minimum of nine clock cycles.

Figure 4-7. ERASE Timing

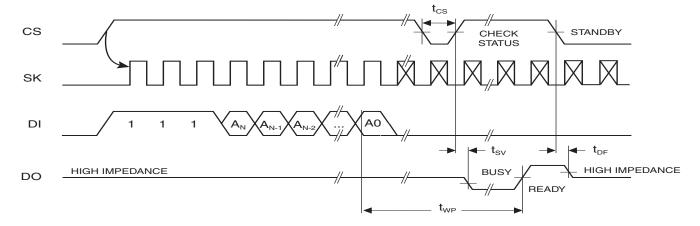
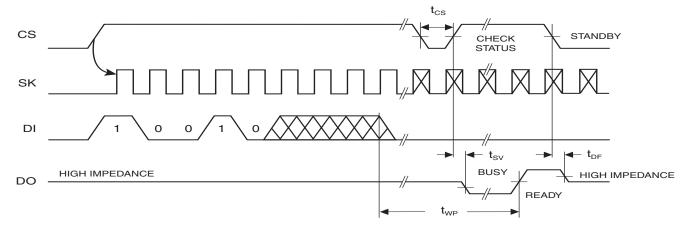


Figure 4-8. ERAL Timing<sup>(1)</sup>



Note: 1. Valid only at  $V_{CC} = 4.5V$  to 5.5V.





# Ordering Information<sup>(1)</sup>

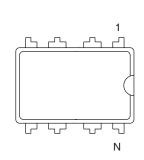
Ordering Code	Package	Operation Range
AT93C46A-10PU-2.7	8P3	
AT93C46A-10PU-1.8	8P3	1 1 6 (1 1 . 1 6 /
AT93C46A-10SU-2.7	8S1	Lead-free/Halogen-free/ Industrial Temperature
AT93C46A-10SU-1.8	8S1	(–40°C to 85°C)
AT93C46A-10TU-2.7	8A2	(=40 C to 65 C)
AT93C46A-10TU-1.8	8A2	

Notes: 1. For 2.7V devices used in the 4.5V to 5.5V range, please refer to performance values in Table 2-3 on page 3 and Table 2-4 on page 4. Not recommended for new design. Please see AT93C46E datasheet.

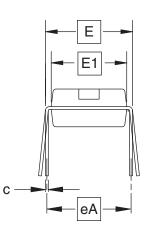
	Package Type				
8P3	8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)				
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)				
8A2	8A2 8-lead, 0.170" Wide, Thin Small Outline Package (TSSOP)				
	Options				
-2.7	<b>-2.7</b> Low Voltage (2.7V to 5.5V)				
-1.8	Low Voltage (1.8V to 5.5V)				

## 5. Packaging Information

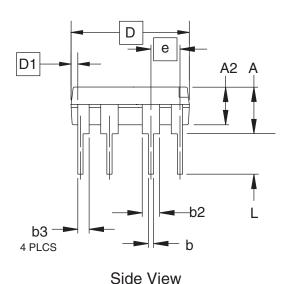
#### 5.1 8P3 - PDIP



Top View



**End View** 



#### **COMMON DIMENSIONS**

(Unit of Measure = inches)

SYMBOL	MIN	NOM	MAX	NOTE
Α			0.210	2
A2	0.115	0.130	0.195	
b	0.014	0.018	0.022	5
b2	0.045	0.060	0.070	6
b3	0.030	0.039	0.045	6
С	0.008	0.010	0.014	
D	0.355	0.365	0.400	3
D1	0.005			3
Е	0.300	0.310	0.325	4
E1	0.240	0.250	0.280	3
е	(			
eA	0.300 BSC			4
L	0.115	0.130	0.150	2

Notes:

- 1. This drawing is for general information only; refer to JEDEC Drawing MS-001, Variation BA for additional information.
- 2. Dimensions A and L are measured with the package seated in JEDEC seating plane Gauge GS-3.
- 3. D, D1 and E1 dimensions do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.010 inch.
- 4. E and eA measured with the leads constrained to be perpendicular to datum.
- 5. Pointed or rounded lead tips are preferred to ease insertion.
- 6. b2 and b3 maximum dimensions do not include Dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25 mm).

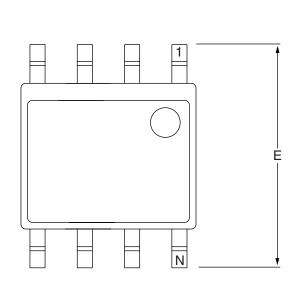
01/09/02



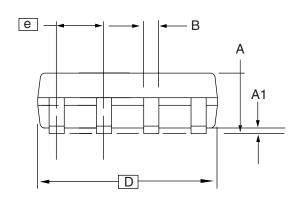




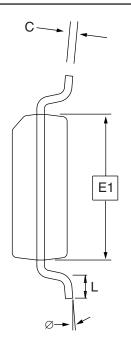
### 5.2 8S1 - JEDEC SOIC



Top View



Side View



**End View** 

## **COMMON DIMENSIONS**

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
А	1.35	_	1.75	
A1	0.10	-	0.25	
b	0.31	_	0.51	
С	0.17	-	0.25	
D	4.80	_	5.00	
E1	3.81	-	3.99	
Е	5.79	_	6.20	
е	1.27 BSC			
L	0.40	_	1.27	
Ø	0°	_	8°	

Note: These drawings are for general information only. Refer to JEDEC Drawing MS-012, Variation AA for proper dimensions, tolerances, datums, etc.

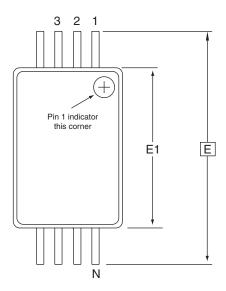
10/7/03

<u>AIMEL</u>

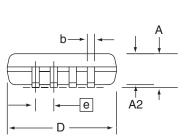
1150 E. Cheyenne Mtn. Blvd. Colorado Springs, CO 80906 **TITLE 8S1**, 8-lead (0.150" Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)

BS1 REV.

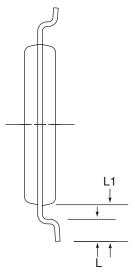
#### 5.3 8A2 - TSSOP



Top View



Side View



**End View** 

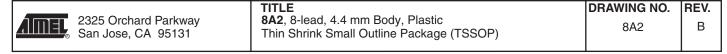
#### **COMMON DIMENSIONS**

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE	
D	2.90	3.00	3.10	2, 5	
Е		6.40 BSC			
E1	4.30	4.40	4.50	3, 5	
Α	_	_	1.20		
A2	0.80	1.00	1.05		
b	0.19	_	0.30	4	
е					
L	0.45	0.60	0.75		
L1	1.00 REF				

- Notes: 1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
  - 2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
  - 3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010 in) per side.
  - 4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
  - 5. Dimension D and E1 to be determined at Datum Plane H.

5/30/02







## **Revision History**

Doc. Rev.	Date	Comments
0539L	11/2007	Modified 'max' values on DC/AC Characteristics tables.
0539K	2/2007	Implemented revision history.  Added Note to page 1 and ordering information; Not recommended for new design; please refer to AT93C46E datasheet.



#### Headquarters

Atmel Corporation

2325 Orchard Parkway San Jose, CA 95131 USA

Tel: 1(408) 441-0311 Fax: 1(408) 487-2600

#### International

Atmel Asia

Room 1219 Chinachem Golden Plaza 77 Mody Road Tsimshatsui East Kowloon Hong Kong

Tel: (852) 2721-9778 Fax: (852) 2722-1369 Atmel Europe

Le Krebs 8, Rue Jean-Pierre Timbaud BP 309 78054 Saint-Quentin-en-Yvelines Cedex France

Tel: (33) 1-30-60-70-00 Fax: (33) 1-30-60-71-11

Atmel Japan

9F, Tonetsu Shinkawa Bldg. 1-24-8 Shinkawa Chuo-ku, Tokyo 104-0033 Japan

Tel: (81) 3-3523-3551 Fax: (81) 3-3523-7581

#### **Product Contact**

Web Site

www.atmel.com

Technical Support

s eeprom@atmel.com

Sales Contact

www.atmel.com/contacts

Literature Requests www.atmel.com/literature

Disclaimer: The information in this document is provided in connection with Atmel products. No license, express or implied, by estoppel or otherwise, to any intellectual property right is granted by this document or in connection with the sale of Atmel products. EXCEPT AS SET FORTH IN ATMEL'S TERMS AND CONDITIONS OF SALE LOCATED ON ATMEL'S WEB SITE, ATMEL ASSUMES NO LIABILITY WHATSOEVER AND DISCLAIMS ANY EXPRESS, IMPLIED OR STATUTORY WARRANTY RELATING TO ITS PRODUCTS INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT. IN NO EVENT SHALL ATMEL BE LIABLE FOR ANY DIRECT, INDIRECT, CONSEQUENTIAL, PUNITIVE, SPECIAL OR INCIDENTAL DAMAGES (INCLUDING, WITHOUT LIMITATION, DAMAGES FOR LOSS OF PROFITS, BUSINESS INTERRUPTION, OR LOSS OF INFORMATION) ARISING OUT OF THE USE OR INABILITY TO USE THIS DOCUMENT, EVEN IF ATMEL HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. Atmel makes no representations or warranties with respect to the accuracy or completeness of the contents of this document and reserves the right to make changes to specifications and product descriptions at any time without notice. Atmel does not make any commitment to update the information contained herein. Unless specifically provided otherwise, Atmel products are not suitable for, and shall not be used in, automotive applications. Atmel's products are not intended, authorized, or warranted for use as components in applications intended to support or sustain life.

© 2007 Atmel Corporation. All rights reserved. Atmel<sup>®</sup>, logo and combinations thereof, and others, are registered trademarks or trademarks of Atmel Corporation or its subsidiaries. Other terms and product names may be trademarks of others.