Dual, 12-Bit, 125MSPS DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **125MSPS UPDATE RATE**
- **SINGLE SUPPLY: +3.3V or +5V**
- **HIGH SFDR: 70dB at f_{OUT} = 20MHz**
- **LOW GLITCH: 2pV-s**
- **LOW POWER: 310mW**
- **INTERNAL REFERENCE**
- **POWER-DOWN MODE: 23mW**

APPLICATIONS

- **COMMUNICATIONS:**
  Base Stations, WLL, WLAN
  Baseband I/Q Modulation
- **MEDICAL/TEST INSTRUMENTATION**
- **ARBITRARY WAVEFORM GENERATORS (ARB)**
- **DIRECT DIGITAL SYNTHESIS (DDS)**

DESCRIPTION

The DAC2902 is a monolithic, 12-bit, dual-channel, high-speed Digital-to-Analog Converter (DAC), and is optimized to provide high dynamic performance while dissipating only 310mW.

Operating with high update rates of up to 125MSPS, the DAC2902 offers exceptional dynamic performance, and enables the generation of very high output frequencies suitable for *Direct IF* applications. The DAC2902 has been optimized for communications applications in which separate I and Q data are processed while maintaining tight gain and offset matching.

Each DAC has a high-impedance differential-current output, suitable for single-ended or differential analog output configurations.

The DAC2902 combines high dynamic performance with a high throughput rate to create a cost-effective solution for a wide variety of waveform-synthesis applications:

- Pin compatibility between family members provides 10-bit (DAC2900), 12-bit (DAC2902), and 14-bit (DAC2904) resolution.
- Pin compatible to the AD9765 dual DAC.
- Gain matching is typically 0.5% of full-scale, and offset matching is specified at 0.02% max.
- The DAC2902 utilizes an advanced CMOS process; the segmented architecture minimizes output glitch energy, and maximizes the dynamic performance.
- All digital inputs are +3.3V and +5V logic compatible. The DAC2902 has an internal reference circuit, and allows use of an external reference.
- The DAC2902 is available in a TQFP-48 package, and is specified over the extended industrial temperature range of –40°C to +85°C.

ABSOLUTE MAXIMUM RATINGS

$+V_A$ to AGND	–0.3V to +6V
$+V_D$ to DGND	–0.3V to +6V
AGND to DGND	–0.3V to +0.3V
$+V_A$ to $+V_D$	–6V to +6V
CLK, PD, WRT to DGND	–0.3V to V_D + 0.3V
D0-D11 to DGND	–0.3V to V_D + 0.3V
I_{OUT}, $I_{\overline{OUT}}$ to AGND	–1V to V_A + 0.3V
GSET to AGND	–0.3V to V_A + 0.3V
REF_{IN}, FSA to AGND	–0.3V to V_A + 0.3V
Junction Temperature	+150°C
Case Temperature	+100°C
Storage Temperature	+125°C

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DAC2902Y	TQFP-48	PFB	–40°C to +85°C	DAC2902Y	DAC2902Y/250	Tape and Reel, 250
"	"	"	"	"	DAC2902Y/1K	Tape and Reel, 1000

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

PRODUCT	EVM ORDERING NUMBER	COMMENT
DAC2902	DAC2902-EVM	Fully populated evaluation board. See user manual for details.

ELECTRICAL CHARACTERISTICS

At T_{MIN} to T_{MAX}, $+V_A$ = +5V, $+V_D$ = +3.3V, differential transformer coupled output, and 50Ω doubly-terminated, unless otherwise noted. Independent Gain mode.

PARAMETER	CONDITIONS	DAC2902Y			UNIT
		MIN	TYP	MAX	
RESOLUTION			12		Bits
Output Update Rate (f_{CLOCK})			125		MSPS
STATIC ACCURACY(1)					
Differential Nonlinearity (DNL)	T_A = +25°C	–2.0	±1	+2.0	LSB
	T_{MIN} to T_{MAX}	–2.5		+2.5	LSB
Integral Nonlinearity (INL)	T_A = +25°C	–2.0	±1	+2.0	LSB
	T_{MIN} to T_{MAX}	–3.0		+3.0	LSB
DYNAMIC PERFORMANCE					
Spurious-Free Dynamic Range (SFDR)	To Nyquist				
f_{OUT} = 1MHz, f_{CLOCK} = 50MSPS	0dBFS Output	72	82		dBc
	–6dBFS Output		77		dBc
	–12dBFS Output		72		dBc
f_{OUT} = 1MHz, f_{CLOCK} = 26MSPS			81		dBc
f_{OUT} = 2.18MHz, f_{CLOCK} = 52MSPS			81		dBc
f_{OUT} = 5.24MHz, f_{CLOCK} = 52MSPS			81		dBc
f_{OUT} = 10.4MHz, f_{CLOCK} = 78MSPS			77		dBc
f_{OUT} = 15.7MHz, f_{CLOCK} = 78MSPS			71		dBc
f_{OUT} = 5.04MHz, f_{CLOCK} = 100MSPS			80		dBc
f_{OUT} = 20.2MHz, f_{CLOCK} = 100MSPS			70		dBc
f_{OUT} = 20.1MHz, f_{CLOCK} = 125MSPS			72		dBc
f_{OUT} = 40.2MHz, f_{CLOCK} = 125MSPS			64		dBc
Spurious-Free Dynamic Range within a Window					
f_{OUT} = 1.0MHz, f_{CLOCK} = 50MSPS	2MHz Span	80	90		dBc
f_{OUT} = 5.02MHz, f_{CLOCK} = 50MSPS	10MHz Span		88		dBc
f_{OUT} = 5.03MHz, f_{CLOCK} = 78MSPS	10MHz Span		88		dBc
f_{OUT} = 5.04MHz, f_{CLOCK} = 125MSPS	10MHz Span		88		dBc
Total Harmonic Distortion (THD)					
f_{OUT} = 1MHz, f_{CLOCK} = 50MSPS			–79	–70	dBc
f_{OUT} = 5.02MHz, f_{CLOCK} = 50MSPS			–77		dBc
f_{OUT} = 5.03MHz, f_{CLOCK} = 78MSPS			–76		dBc
f_{OUT} = 5.04MHz, f_{CLOCK} = 125MSPS			–75		dBc
Multitone Power Ratio	8 Tone with 110kHz Spacing				
f_{OUT} = 2.0MHz to 2.99MHz, f_{CLOCK} = 65MSPS	0dBFS Output		80		dBc

ELECTRICAL CHARACTERISTICS (continued)

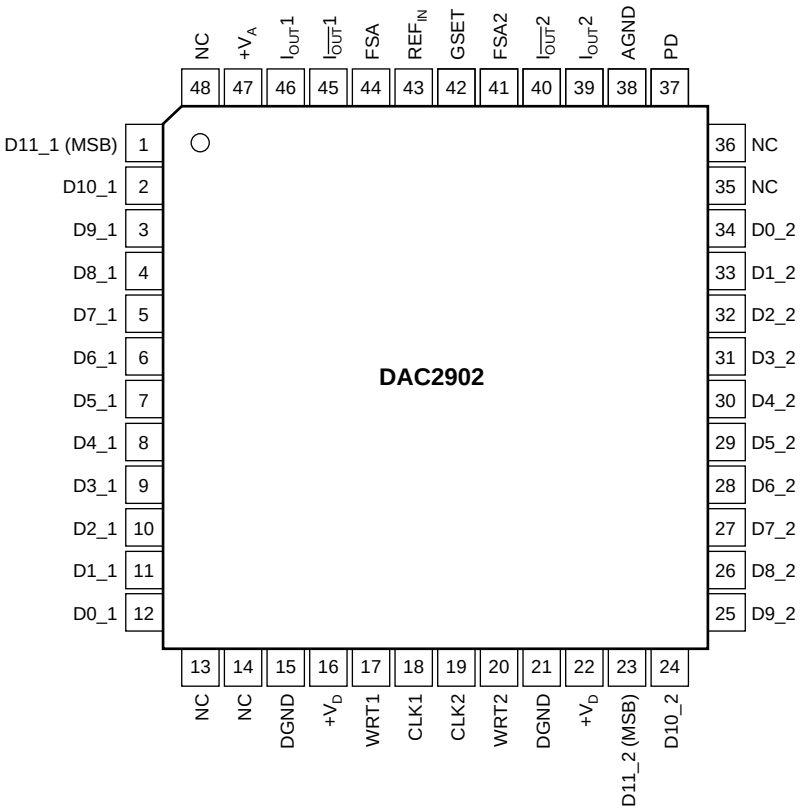
At T_{MIN} to T_{MAX}, $+V_A$ = +5V, $+V_D$ = +3.3V, differential transformer coupled output, and 50Ω doubly-terminated, unless otherwise noted. Independent Gain mode.

PARAMETER	CONDITIONS	DAC2902Y MIN	DAC2902Y TYP	DAC2902Y MAX	UNIT
DYNAMIC PERFORMANCE (Cont.)					
Signal-to-Noise Ratio (SNR)	0dBFS Output		68		dBc
f_{OUT} = 5.02MHz, f_{CLOCK} = 50MHz					
Signal-to-Noise and Distortion (SINAD)	0dBFS Output		67		dBc
f_{OUT} = 5.02MHz, f_{CLOCK} = 50MHz					
Channel Isolation					
f_{OUT} = 1MHz, f_{CLOCK} = 52MSPS			85		dBc
f_{OUT} = 20MHz, f_{CLOCK} = 125MSPS			77		dBc
Output Settling Time(2)	to 0.1%		30		ns
Output Rise Time(2)	10% to 90%		2		ns
Output Fall Time(2)	10% to 90%		2		ns
Glitch Impulse			2		pV-s
DC ACCURACY					
Full-Scale Output Range(3)(FSR)	All Bits HIGH, I_{OUT}	2		20	mA
Output Compliance Range		–1.0		+1.25	V
Gain Error—Full-Scale	With Internal Reference	–5	±1	+5	%FSR
Gain Error	With External Reference	–2.5	±1	+2.5	%FSR
Gain Matching	With Internal Reference	–2.0	0.5	+2.0	%FSR
Gain Drift	With Internal Reference		±50		ppmFSR/°C
Offset Error	With Internal Reference	–0.02		+0.02	%FSR
Offset Drift	With Internal Reference		±0.2		ppmFSR/°C
Power-Supply Rejection, $+V_A$	+5V, ±10%	–0.2		+0.2	%FSR/V
Power-Supply Rejection, $+V_D$	+3.3V, ±10%	–0.025		+0.025	%FSR/V
Output Noise	I_{OUT} = 20mA, R_{LOAD} = 50Ω		50		pA/√Hz
	I_{OUT} = 2mA		30		pA/√Hz
Output Resistance			200		kΩ
Output Capacitance	I_{OUT}, $I_{\overline{OUT}}$ to Ground		6		pF
REFERENCE/CONTROL AMP					
Reference Voltage		+1.18	+1.25	+1.31	V
Reference Voltage Drift			±50		ppmFSR/°C
Reference Output Current			100		nA
Reference Multiplying Bandwidth			0.3		MHz
Input Compliance Range		+0.5		+1.25	V
DIGITAL INPUTS					
Logic Coding			Straight Binary		
Logic High Voltage, V_{IH}	$+V_D$ = +5V	3.5	5		V
Logic Low Voltage, V_{IL}	$+V_D$ = +5V		0	1.2	V
Logic High Voltage, V_{IH}	$+V_D$ = 3.3V	2	3		V
Logic Low Voltage, V_{IL}	$+V_D$ = 3.3V		0	0.8	V
Logic High Current, I_{IH}(4)	$+V_D$ = 3.3V		±10		µA
Logic Low Current	$+V_D$ = 3.3V		±10		µA
Input Capacitance			5		pF
POWER SUPPLY					
Supply Voltages					
$+V_A$		+3.0	+5	+5.5	V
$+V_D$		+3.0	+3.3	+5.5	V
Supply Current					
I_{VA}(5)	V_A = +5V, I_{OUT} = 20mA		58	65	mA
I_{VA}(5)	Power-Down Mode		1.7	3	mA
I_{VD}(5)			4.2	7	mA
I_{VD}(6)			17	19.5	mA
Power Dissipation(5)	V_A = +5V, V_D = 3.3V, I_{OUT} = 20mA		310	350	mW
Power Dissipation(6)	V_A = +5V, V_D = 3.3V, I_{OUT} = 20mA		348	390	mW
Power Dissipation(5)	V_A = +5V, V_D = 3.3V, I_{OUT} = 2mA		130		mW
Power Dissipation	Power-Down Mode		23	38	mW
Thermal Resistance, TQFP-48					
θ_{JA}			60		°C/W
θ_{JC}			13		°C/W
TEMPERATURE RANGE					
Specified	Ambient	–40		+85	°C
Operating	Ambient	–40		+85	°C

NOTES: (1) At output I_{OUT}, while driving a virtual ground. (2) Measured single-ended into 50Ω load. (3) Nominal full-scale output current is $32 \times I_{REF}$; see Application section for details. (4) Typically 45µA for the PD pin, which has an internal pull-down resistor. (5) Measured at f_{CLOCK} = 25MSPS and f_{OUT} = 1MHz. (6) Measured at f_{CLOCK} = 100MSPS and f_{OUT} = 40MHz.

PIN CONFIGURATION

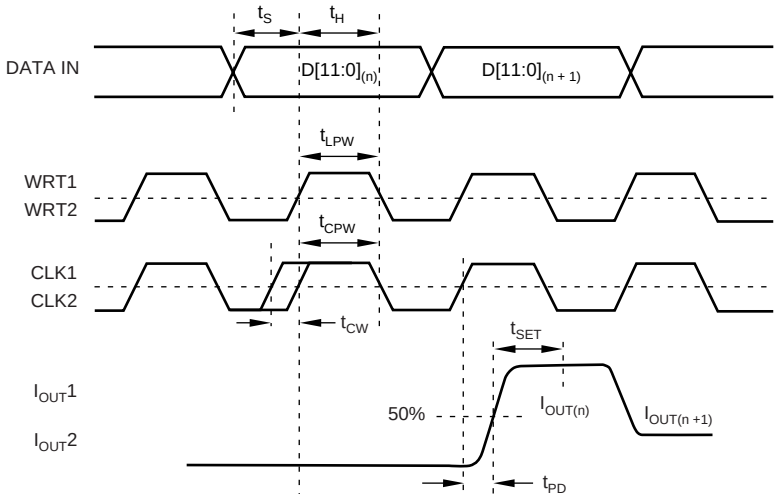
Top View **TQFP-48**



PIN DESCRIPTIONS

PIN	DESIGNATOR	DESCRIPTION
1-12	D[11:0]_1	Data Port DAC1, Data Bit 11 (MSB) to Bit 0 (LSB).
13, 14	NC	No Connection
15	DGND	Digital Ground
16	$+V_D$	Digital Supply, +3.0V to +5.5V
17	WRT1	DAC1 Input Latches Write Signal
18	CLK1	Clock Input DAC1
19	CLK2	Clock Input DAC2
20	WRT2	DAC2 Input Latches Write Signal
21	DGND	Digital Ground
22	$+V_D$	Digital Supply, +3.0V to +5.5V
23-34	D[11:0]_2	Data Port DAC2, Data Bit 11 (MSB) to Bit 0 (LSB).
35, 36	NC	No Connection
37	PD	Power-Down Function Control Input; *H* = DAC in power-down mode; *L* = DAC in normal operation (Internal pull-down for default "L").
38	AGND	Analog Ground
39	$I_{OUT}2$	Current Output DAC2. Full-scale with all bits of data port 2 HIGH.
40	$I_{\overline{OUT}}2$	Complementary Current Output DAC2. Full-scale with all bits of data port 2 LOW.
41	FSA2	Full-Scale Adjust, DAC2. Connect External R_{SET} Resistor.
42	GSET	Gain-Setting Mode (H = 1 Resistor, L = 2 Resistor)
43	REF_{IN}	Internal Reference Voltage output; External Reference Voltage input. Bypass with 0.1µF to AGND for internal reference operation.
44	FSA1	Full-Scale Adjust, DAC1. Connect External R_{SET} Resistor
45	$I_{\overline{OUT}}1$	Complementary Current Output DAC1. Full-scale with all bits of data port 1 LOW.
46	$I_{OUT}1$	Current Output DAC1. Full-scale with all bits of data port 1 HIGH.
47	$+V_A$	Analog Supply, +3.0V to +5.5V
48	NC	No Connection

TIMING DIAGRAM



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_S	Input Setup Time	2			ns
t_H	Input Hold Time	1.5			ns
t_{LPW}, t_{CPW}	Latch/Clock Pulsewidth	3.5	4		ns
t_{CW}	Delay Rising CLK Edge to Rising WRT Edge	0		t_{PW} – 2	ns
t_{PD}	Propagation Delay		1		ns
t_{SET}	Settling Time (0.1%)		30		ns

DIGITAL INPUTS AND TIMING

The data input ports of the DAC2902 accept a standard positive coding with data bit D11 being the most significant bit (MSB). The converter outputs support a clock rate of up to 125MSPS. The best performance will typically be achieved with a symmetrical duty cycle for write and clock; however, the duty cycle may vary as long as the timing specifications are met. Also, the setup and hold times may be chosen within their specified limits.

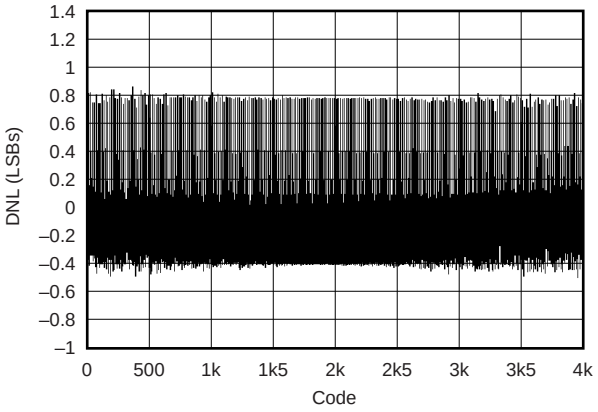
All digital inputs of the DAC2902 are CMOS-compatible. The logic thresholds depend on the applied digital supply voltages, such that they are set to approximately half the supply voltage: $V_{th} = +V_D/2$ (±20% tolerance). The DAC2902 is designed to operate with a digital supply ($+V_D$) of +3.0V to +5.5V.

The two converter channels within the DAC2902 consist of two independent, 12-bit, parallel data ports. Each DAC channel is controlled by its own set of write (WRT1, WRT2) and clock (CLK1, CLK2) inputs. Here, the WRT lines control the channel input latches and the CLK lines control the DAC latches. The data is first loaded into the input latch by a rising edge of the WRT line. This data is presented to the DAC latch on the following falling edge of the WRT signal. On the next rising edge of the CLK line, the DAC is updated with the new data and the analog output signal will change accordingly. The double latch architecture of the DAC2902 results in a defined sequence for the WRT and CLK signals, expressed by parameter t_{CW}. A correct timing is observed when the rising edge of CLK occurs at the same time, or before, the rising edge of the WRT signal. This condition can simply be met by connecting the WRT and CLK lines together. Note that all specifications were measured with the WRT and CLK lines connected together.

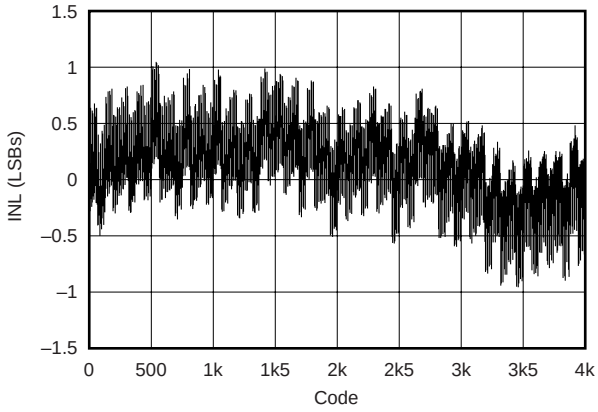
TYPICAL CHARACTERISTICS

T_A = +25°C, $+V_D$ = +3.3V, $+V_A$ = +5V, differential transformer coupled, I_{OUT} = 20mA, 50Ω double-terminated load, and SFDR up to Nyquist, unless otherwise noted.

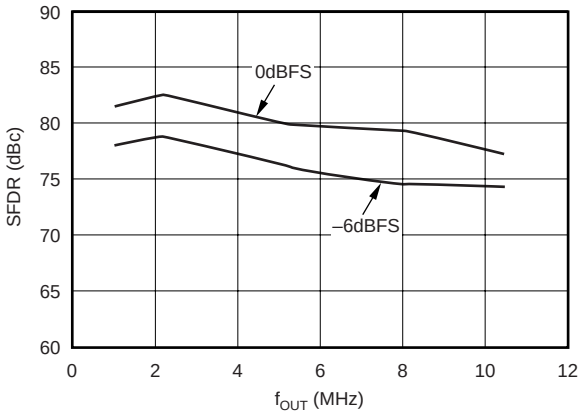
TYPICAL DNL



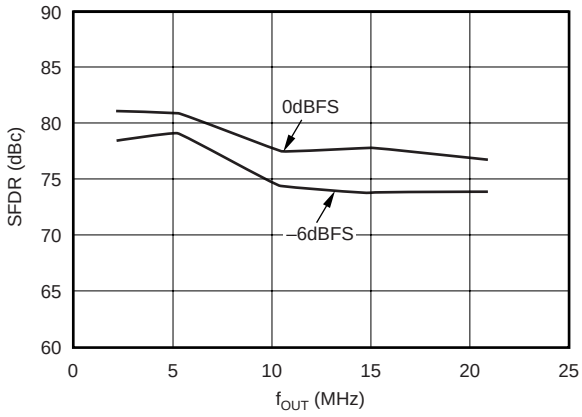
TYPICAL INL



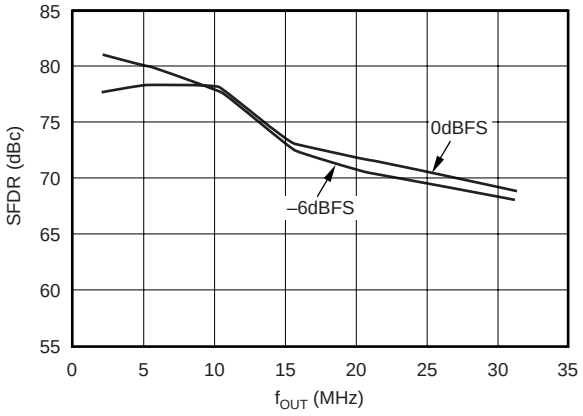
SFDR vs f_{OUT} AT 26MSPS



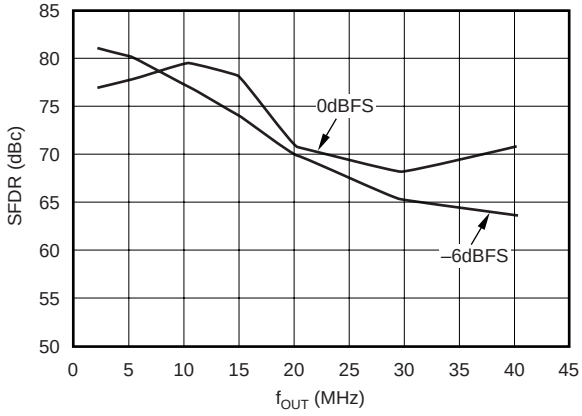
SFDR vs f_{OUT} AT 52MSPS



SFDR vs f_{OUT} AT 78MSPS



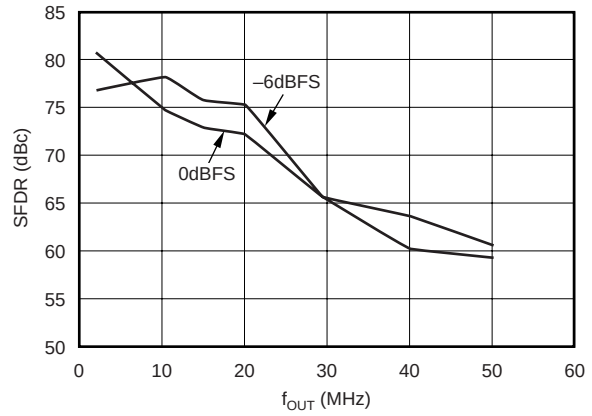
SFDR vs f_{OUT} AT 100MSPS



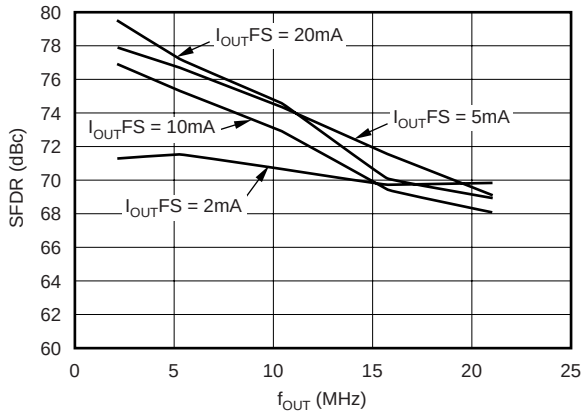
TYPICAL CHARACTERISTICS (continued)

T_A = +25°C, $+V_D$ = +3.3V, $+V_A$ = +5V, differential transformer coupled, I_{OUT} = 20mA, 50Ω double-terminated load, and SFDR up to Nyquist, unless otherwise noted.

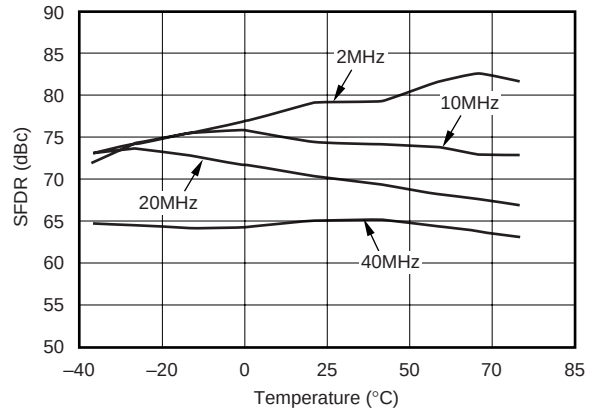
SFDR vs f_{OUT} AT 125MHz



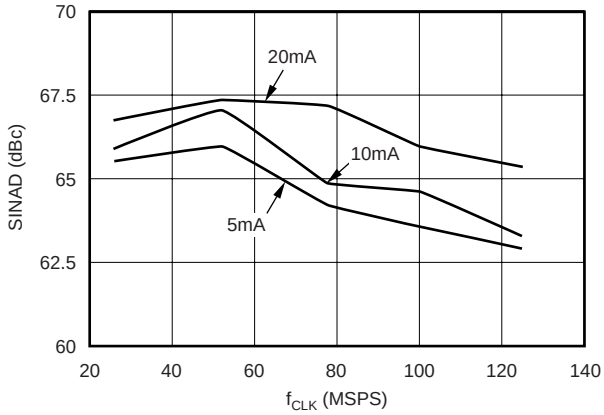
SFDR vs I_{OUT}FS AND f_{OUT} AT 78MSPS, 0dBFS



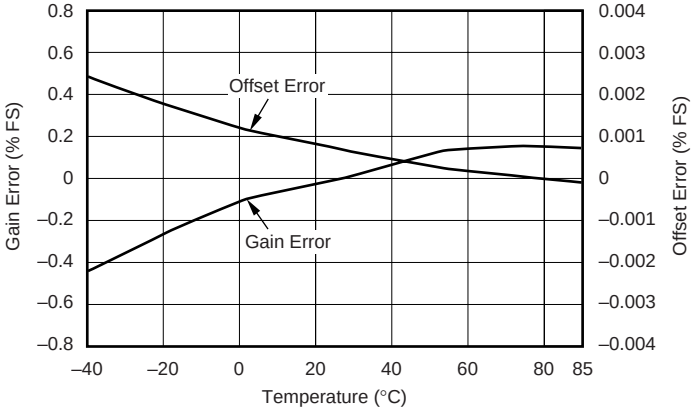
SFDR AT 125MSPS vs TEMPERATURE



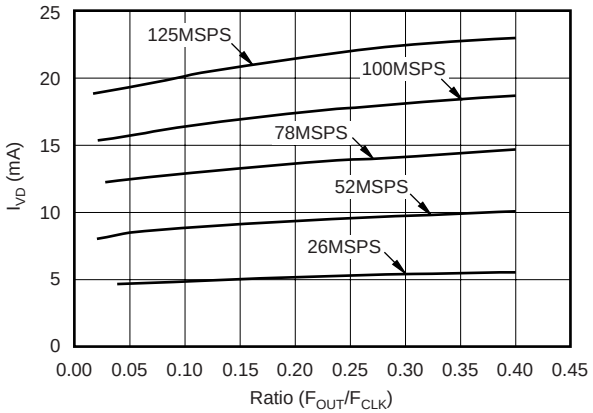
SINAD vs f_{CLK} AND I_{OUT} AT 5MHz



GAIN AND OFFSET DRIFT



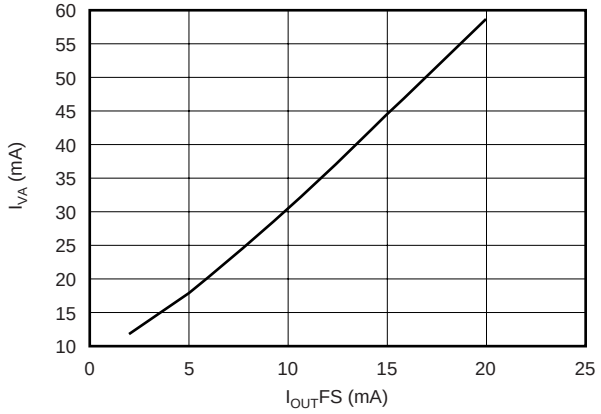
I_{VD} vs RATIO AT $+V_D$ = +3.3V



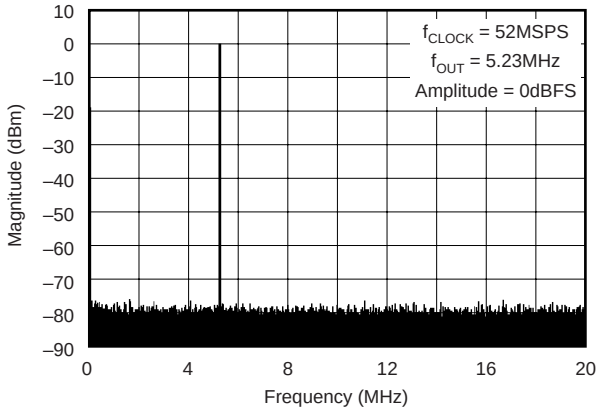
TYPICAL CHARACTERISTICS (continued)

T_A = +25°C, $+V_D$ = +3.3V, $+V_A$ = +5V, differential transformer coupled, I_{OUT} = 20mA, 50Ω double-terminated load, and SFDR up to Nyquist, unless otherwise noted.

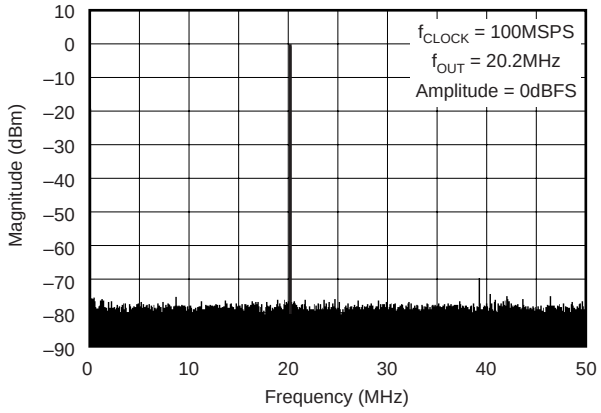
I_{VA} vs I_{OUT}FS



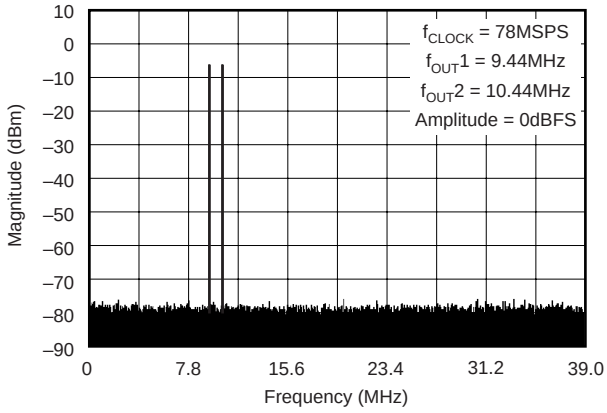
SINGLE-TONE SFDR



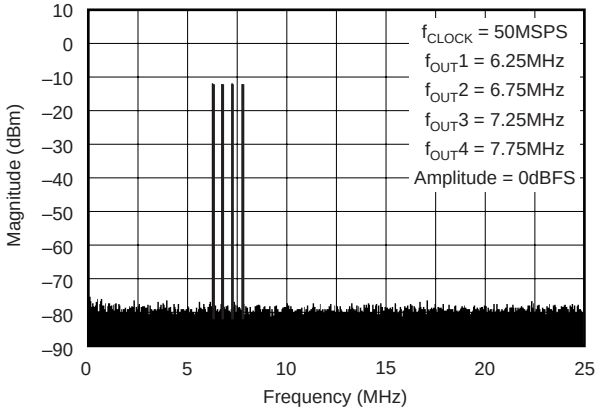
SINGLE-TONE SFDR



DUAL-TONE SFDR



FOUR-TONE SFDR



APPLICATION INFORMATION

THEORY OF OPERATION

The architecture of the DAC2902 uses the current steering technique to enable fast switching and a high update rate. The core element within the monolithic DAC is an array of segmented current sources that are designed to deliver a full-scale output current of up to 20mA, as shown in Figure 1. An internal decoder addresses the differential current switches each time the DAC is updated and a corresponding output current is formed by steering all currents to either output summing node, I_{OUT} or $I_{\overline{OUT}}$. The complementary outputs deliver a differential output signal, which improves the dynamic performance through reduction of even-order harmonics, common-mode signals (noise), and double the peak-to-peak output signal swing by a factor of two, compared to single-ended operation.

The segmented architecture results in a significant reduction of the glitch energy, improves the dynamic performance (SFDR), and DNL. The current outputs maintain a very high output impedance of greater than 200kΩ.

The full-scale output current is determined by the ratio of the internal reference voltage (approx. +1.25V) and an external resistor, R_{SET}. The resulting I_{REF} is internally multiplied by a factor of 32 to produce an effective DAC output current that can range from 2mA to 20mA, depending on the value of R_{SET}.

The DAC2902 is split into a digital and an analog portion, each of which is powered through its own supply pin. The digital section includes edge-triggered input latches and the decoder logic, while the analog section consists of the current source array with its associated switches, and the reference circuitry.

DAC TRANSFER FUNCTION

Each of the DACs in the DAC2902 has a complementary current output, $I_{OUT}1$ and $I_{OUT}2$. The full-scale output current, I_{OUTFS}, is the summation of the two complementary output currents:

$$I_{OUTFS} = I_{OUT} + I_{\overline{OUT}} \quad (1)$$

The individual output currents depend on the DAC code and can be expressed as:

$$I_{OUT} = I_{OUTFS} \times (Code/4096) \quad (2)$$

$$I_{\overline{OUT}} = I_{OUTFS} \times (4095 - Code) \quad (3)$$

where *Code* is the decimal representation of the DAC data input word. Additionally, I_{OUTFS} is a function of the reference current I_{REF}, which is determined by the reference voltage and the external setting resistor, R_{SET}.

$$I_{OUTFS} = 32 \times I_{REF} = 32 \times V_{REF}/R_{SET} \quad (4)$$

In most cases the complementary outputs will drive resistive loads or a terminated transformer. A signal voltage will develop at each output according to:

$$V_{OUT} = I_{OUT} \times R_{LOAD} \quad (5)$$

$$V_{\overline{OUT}} = I_{\overline{OUT}} \times R_{LOAD} \quad (6)$$

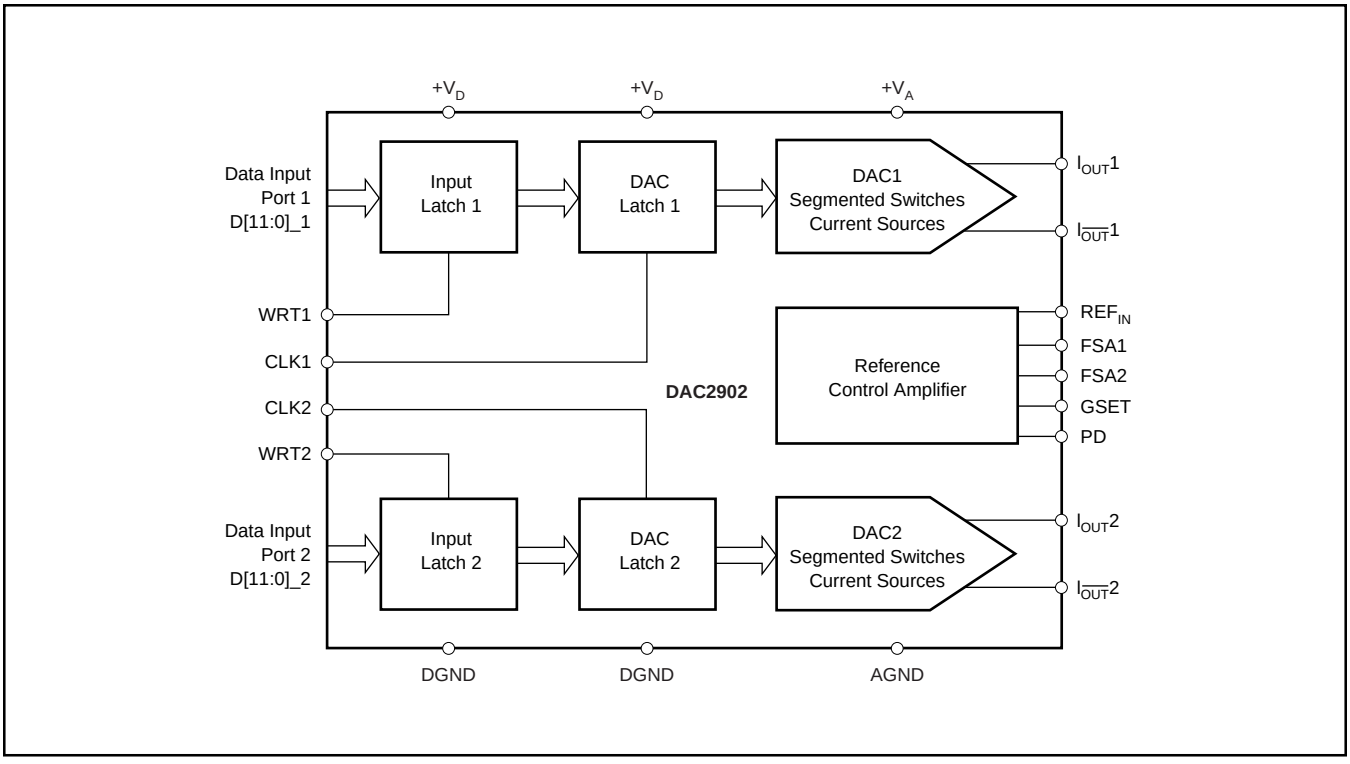


FIGURE 1. Block Diagram of the DAC2902.

The value of the load resistance is limited by the output compliance specification of the DAC2902. To maintain specified linearity performance, the voltage for I_{OUT} and $I_{\overline{OUT}}$ should not exceed the maximum allowable compliance range.

The two single-ended output voltages can be combined to find the total differential output swing:

$$V_{OUTDIFF} = V_{OUT} - V_{\overline{OUT}} = \frac{(2 \times Code - 4095)}{4096} \times I_{OUTFS} \times R_{LOAD} \quad (7)$$

ANALOG OUTPUTS

The DAC2902 provides two complementary current outputs, I_{OUT} and $I_{\overline{OUT}}$. The simplified circuit of the analog output stage representing the differential topology is shown in Figure 2. The output impedance of I_{OUT} and $I_{\overline{OUT}}$ results from the parallel combination of the differential switches, along with the current sources and associated parasitic capacitances.

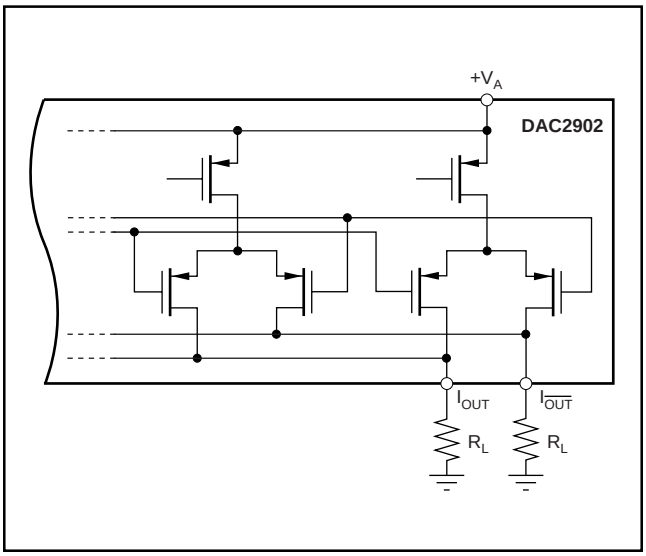


FIGURE 2. Equivalent Analog Output.

The signal voltage swing that may develop at the two outputs, I_{OUT} and $I_{\overline{OUT}}$, is limited by a negative and positive compliance. The negative limit of –1V is given by the breakdown voltage of the CMOS process, and exceeding it will compromise the reliability of the DAC2902, or even cause permanent damage. With the full-scale output set to 20mA, the positive compliance equals 1.25V, operating with an analog supply of $+V_A$ = 5V. Note that the compliance range decreases to about 1V for a selected output current of I_{OUTFS} = 2mA. Care should be taken that the configuration of the DAC2902 does not exceed the compliance range to avoid degradation of the distortion performance and integral linearity.

Best distortion performance is typically achieved with the maximum full-scale output signal limited to approximately $0.5V_{PP}$. This is the case for a 50Ω doubly-terminated load and a 20mA full-scale output current. A variety of loads can be adapted to the output of the DAC2902 by selecting a suitable transformer while maintaining optimum voltage levels at I_{OUT} and $I_{\overline{OUT}}$. Furthermore, using the differential output configuration in combination with a transformer will be instrumental for achieving excellent distortion performance. Common-mode errors, such as even-order harmonics or noise, can be substantially reduced. This is particularly the case with high output frequencies.

For those applications requiring the optimum distortion and noise performance, it is recommended to select a full-scale output of 20mA. A lower full-scale range down to 2mA may be considered for applications that require a low power consumption, but can tolerate a slightly reduced performance level.

OUTPUT CONFIGURATIONS

The current outputs of the DAC2902 allow for a variety of configurations, some of which are illustrated in Table I. As mentioned previously, utilizing the converter's differential outputs will yield the best dynamic performance. Such a differential output circuit may consist of an RF transformer or a differential amplifier configuration. The transformer configuration is ideal for most applications with ac coupling, while op amps will be suitable for a DC-coupled configuration.

INPUT CODE (D11 - D0)	I_{OUT}	$I_{\overline{OUT}}$
1111 1111 1111	20mA	0mA
1000 0000 0000	10mA	10mA
0000 0000 0000	0mA	20mA

TABLE I. Input Coding Versus Analog Output Current.

The single-ended configuration may be considered for applications requiring a unipolar output voltage. Connecting a resistor from either one of the outputs to ground will convert the output current into a ground-referenced voltage signal. To improve on the DC linearity by maintaining a virtual ground, an I-to-V or op-amp configuration may be considered.

DIFFERENTIAL WITH TRANSFORMER

Using an RF transformer provides a convenient way of converting the differential output signal into a single-ended signal while achieving excellent dynamic performance (see Figure 3). The appropriate transformer should be carefully selected based on the output frequency spectrum and impedance requirements. The differential transformer configuration has the benefit of significantly reducing common-mode signals, thus improving the dynamic performance over a wide range of frequencies. Furthermore, by selecting a suitable impedance ratio (winding ratio), the transformer can be used to provide optimum impedance matching while controlling the compliance voltage for the converter outputs. The model shown, ADTT1-1 (by Mini-Circuits), has a 1:1 ratio and may be used to interface the DAC2902 to a 50Ω load. This results in a 25Ω load for each of the outputs, I_{OUT} and $I_{\overline{OUT}}$. The output signals are ac coupled and inherently isolated because of its magnetic coupling.

As shown in Figure 3, the transformer center tap is connected to ground. This forces the voltage swing on I_{OUT} and $I_{\overline{OUT}}$ to be centered at 0V. In this case the two resistors, R_L, may be replaced with one, R_{DIFF}, or omitted altogether. This approach should only be used if all components are close to each other, and if the VSWR is not important. A complete power transfer from the DAC output to the load can be realized, but the output compliance range should be observed. Alternatively, if the center tap is not connected, the signal swing will be centered at $R_L \times I_{OUTFS}/2$. However, in this case, the two resistors (R_L) must be used to enable the necessary DC-current flow for both outputs.

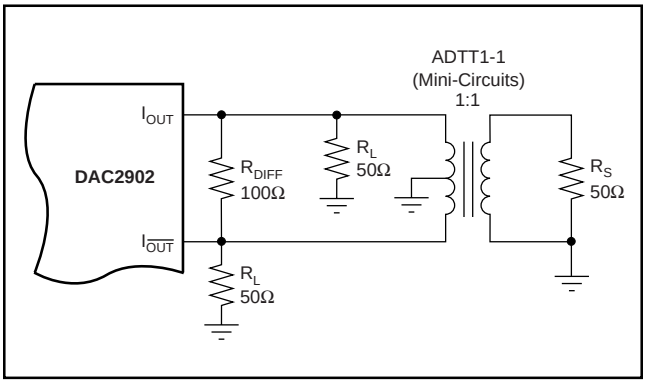


FIGURE 3. Differential Output Configuration Using an RF Transformer.

DIFFERENTIAL CONFIGURATION USING AN OP AMP

If the application requires a DC-coupled output, a difference amplifier may be considered, as shown in Figure 4. Four external resistors are needed to configure the voltage-feedback op amp OPA680 as a difference amplifier performing the differential to single-ended conversion. Under the shown configuration, the DAC2902 generates a differential output signal of $0.5V_{PP}$ at the load resistors, R_L. The resistor values shown were selected to result in a symmetric 25Ω loading for each of the current outputs since the input impedance of the difference amplifier is in parallel to resistors R_L, and should be considered.

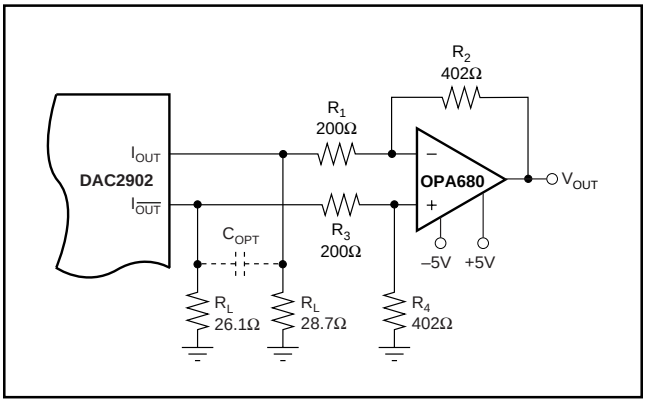


FIGURE 4. Difference Amplifier Provides Differential to Single-Ended Conversion and DC-Coupling.

The OPA680 is configured for a gain of two. Therefore, operating the DAC2902 with a 20mA full-scale output will produce a voltage output of ±1V. This requires the amplifier to operate from a dual power supply (±5V). The tolerance of the resistors typically sets the limit for the achievable common-mode rejection. An improvement can be obtained by fine tuning resistor R_4.

This configuration typically delivers a lower level of ac performance than the previously discussed transformer solution because the amplifier introduces another source of distortion. Suitable amplifiers should be selected based on their slew-rate, harmonic distortion, and output swing capabilities. High-speed amplifiers like the OPA680 or OPA687 may be considered. The ac performance of this circuit may be improved by adding a small capacitor (C_{DIFF}) between the outputs I_{OUT} and $I_{\overline{OUT}}$, as shown in Figure 4). This will introduce a real pole to create a low-pass filter in order to slew-limit the DAC fast output signal steps, that otherwise could drive the amplifier into slew-limitations or into an overload condition; both would cause excessive distortion. The difference amplifier can easily be modified to add a level shift for applications requiring the single-ended output voltage to be unipolar (that is, swing between 0V and +2V.)

DUAL TRANSIMPEDANCE OUTPUT CONFIGURATION

The circuit example of Figure 5 shows the signal output currents connected into the summing junctions of the dual voltage-feedback op amp OPA2680 that is set up as a transimpedance stage, or *I-to-V converter*. With this circuit, the DAC output will be kept at a virtual ground, minimizing the effects of output impedance variations, which results in the best DC linearity (INL). As mentioned previously, care should be taken not to drive the amplifier into slew-rate limitations, and produce unwanted distortion.

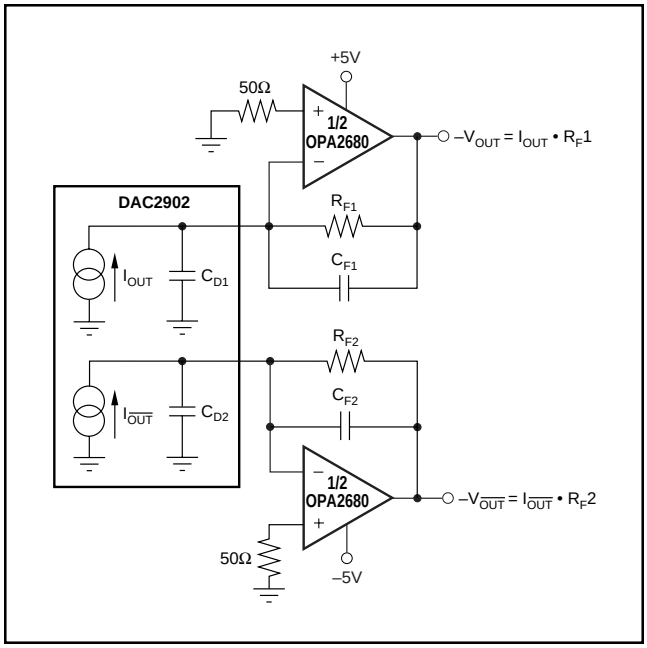


FIGURE 5. Dual, Voltage-Feedback Amplifier OPA2680 Forms Differential Transimpedance Amplifier.

The DC gain for this circuit is equal to feedback resistor R_F. At high frequencies, the DAC output impedance (C_{D1}, C_{D2}) will produce a 0 in the noise gain for the OPA2680 that may cause peaking in the closed-loop frequency response. C_F is added across R_F to compensate for this noise gain peaking. To achieve a flat transimpedance frequency response, the pole in each feedback network should be set to:

$$\frac{1}{2\pi R_F C_F} = \frac{\sqrt{GBP}}{4\pi R_F C_D} \quad (8)$$

with GBP = Gain Bandwidth Product of OPA,

which will give a corner frequency f_{-3dB} of approximately:

$$f_{-3dB} = \frac{\sqrt{GBP}}{2\pi R_F C_D} \quad (9)$$

The full-scale output voltage is simply defined by the product of $I_{OUTFS} \times R_F$, and has a negative unipolar excursion. To improve on the ac performance of this circuit, adjustment of R_F and/or I_{OUTFS} should be considered. Further extensions of this application example may include adding a differential filter at the OPA2680 output followed by a transformer, in order to convert to a single-ended signal.

SINGLE-ENDED CONFIGURATION

Using a single-load resistor connected to the one of the DAC outputs, a simple current-to-voltage conversion can be accomplished. The circuit in Figure 6 shows a 50Ω resistor connected to I_{OUT}, providing the termination of the further connected 50Ω cable. Therefore, with a nominal output current of 20mA, the DAC produces a total signal swing of 0V to 0.5V into the 25Ω load.

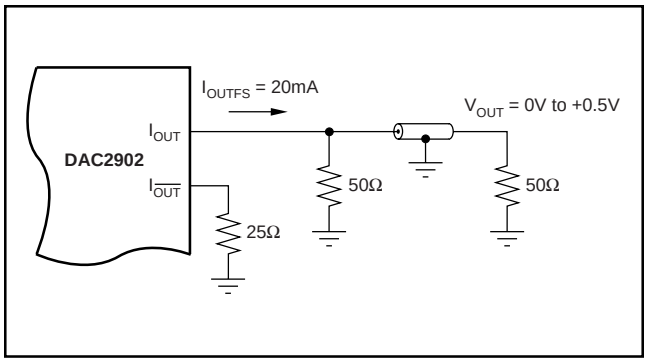


FIGURE 6. Driving a Doubly Terminated 50Ω Cable Directly.

Different load resistor values may be selected as long as the output compliance range is not exceeded. Additionally, the output current, I_{OUTFS}, and the load resistor, may be mutually adjusted to provide the desired output signal swing and performance.

INTERFACING ANALOG QUADRATURE MODULATORS

One of the main applications for the dual-channel DAC is baseband I- and Q-channel transmission for digital communications. In this application, the DAC is followed by an analog quadrature modulator, modulating an IF carrier with the baseband data, as shown in Figure 7. Often, the input stages of these quadrate modulators consist of npn-type transistors that require a DC bias (base) voltage of > 0.8V. The wide output compliance range (–10V to +1.25V) allows for a direct DC–coupling between the DAC2902 and the quadrature modulator.

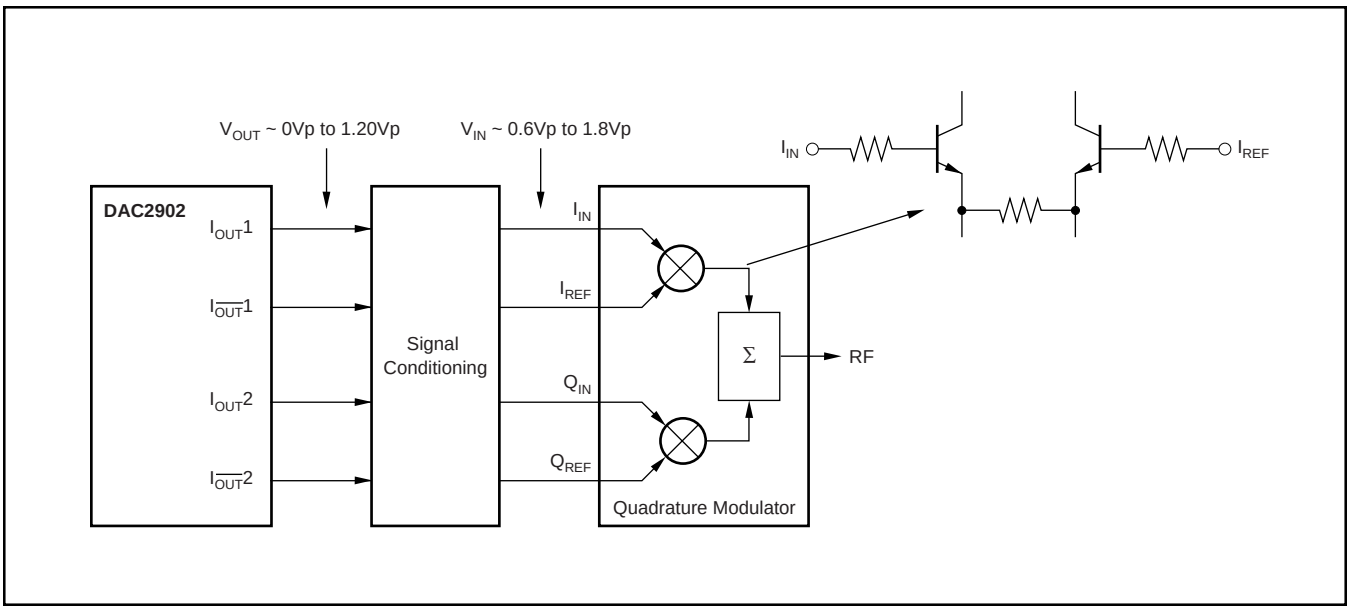


FIGURE 7. Generic Interface to a Quadrature Modulator. Signal Conditioning (Level-Shifting) May Be Required to Ensure Correct DC Common-Mode Levels At the Input of the Quadrature Modulator.

Figure 8 shows an example of a DC-coupled interface with DC level-shifting, using a precision resistor network. An ac-coupled interface, as shown in Figure 9, has the advantage that the common-mode levels at the input of the modulator can be set independently of those at the output of the DAC. Furthermore, no voltage loss is obtained in this setup.

INTERNAL REFERENCE OPERATION

The DAC2902 has an on-chip reference circuit that consists of a 1.25V bandgap reference and two control amplifiers, one for each DAC. The full-scale output current, I_{OUTFS}, of the DAC2902 is determined by the reference voltage, V_{REF}, and the value of resistor R_{SET}. I_{OUTFS} can be calculated by:

$$I_{OUTFS} = 32 \times I_{REF} = 32 \times V_{REF} / R_{SET} \qquad (10)$$

The external resistor R_{SET} connects to the FSA pin (Full-Scale Adjust), see Figure 10. The reference control amplifier operates as a V-to-I converter producing a reference current, I_{REF}, which is determined by the ratio of V_{REF} and R_{SET} (as shown in Equation 10). The full-scale output current, I_{OUTFS}, results from multiplying I_{REF} by a fixed factor of 32.

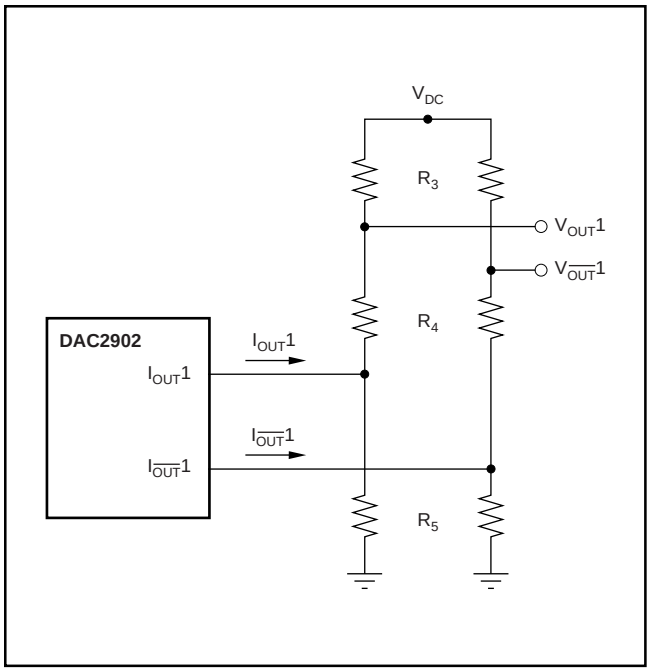


FIGURE 8. DC-Coupled Interface to Quadrature Modulator Applying Level Shifting.

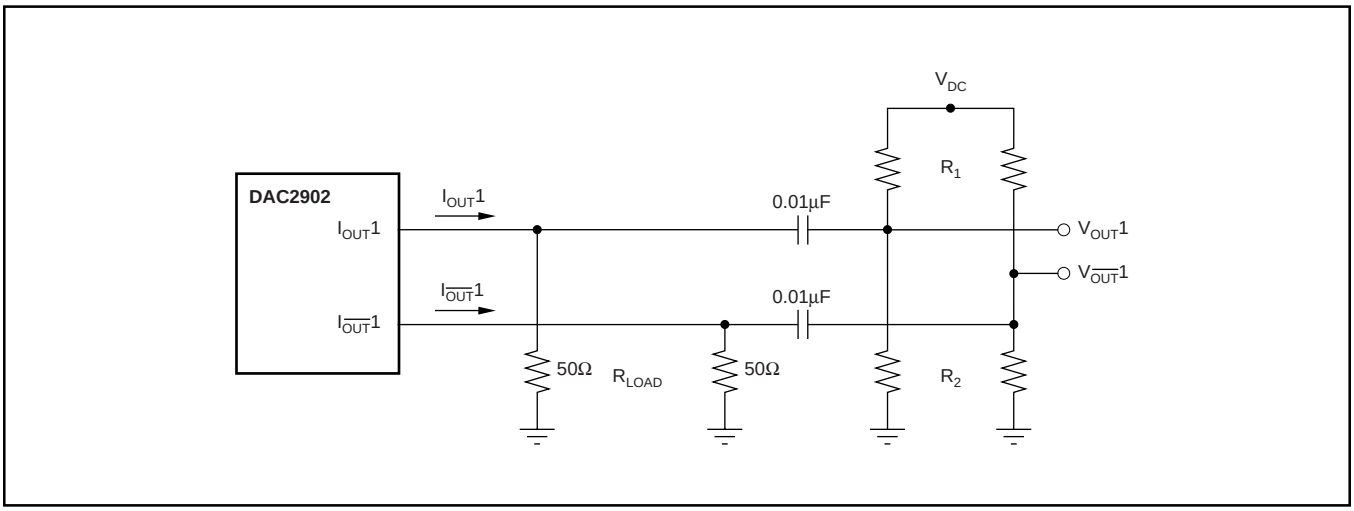


FIGURE 9. AC-Coupled Interface to Quadrature Modulator Applying Level Shifting.

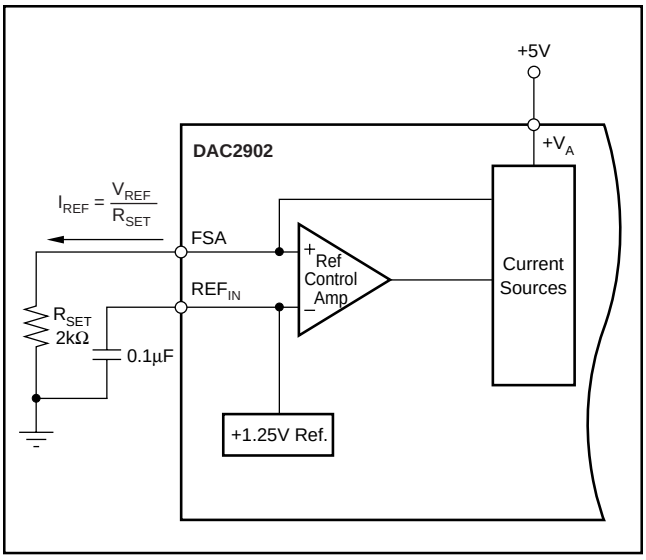


FIGURE 10. Internal Reference Configuration.

Using the internal reference, a 2kΩ resistor value results in a full-scale output of approximately 20mA. Resistors with a tolerance of 1% or better should be considered. Selecting higher values, the output current can be adjusted from 20mA down to 2mA. Operating the DAC2902 at lower than 20mA output currents may be desirable for reasons of reducing the total power consumption, optimizing the distortion performance, or observing the output compliance voltage limitations for a given load condition.

It is recommended to bypass the REF_{IN} pin with a ceramic chip capacitor of 0.1µF or more. The control amplifier is internally compensated, and its small signal bandwidth is approximately 0.3MHz.

GAIN SETTING OPTIONS

The full-scale output current on the DAC2902 can be set two ways: either for each of the two DAC channels independently or for both channels simultaneously. For the independent gain set mode, the GSET pin (pin 42) must be LOW (that is, connected to AGND). In this mode, two external resistors are required—one R_{SET} connected to the FSA1 pin (pin 44) and the other to the FSA2 pin (pin 41). In this configuration, the user has the flexibility to set and adjust the full-scale output current for each DAC independently, allowing for the compensation of possible gain mismatches elsewhere within the transmit signal path.

Alternatively, bringing the GSET pin HIGH (that is, connected to $+V_A$), the DAC2902 will switch into the simultaneous gain set mode. Now the full-scale output current of both DAC channels is determined by only one external R_{SET} resistor connected to the FSA1 pin. The resistor at the FSA2 pin may be removed, however this is not required since this pin is not functional in this mode and the resistor has no effect to the gain equation. The formula for deriving the correct R_{SET} remains unchanged (for example, R_{SET} = 2kΩ will result in a 20mA output for both DACs).

EXTERNAL REFERENCE OPERATION

The internal reference can be disabled by simply applying an external reference voltage into the REF_{IN} pin, which in this case functions as an input, as shown in Figure 11. The use of an external reference may be considered for applications that require higher accuracy and drift performance, or to add the ability of dynamic gain control.

While a 0.1µF capacitor is recommended to be used with the internal reference, it is optional for the external reference operation. The reference input, REF_{IN}, has a high input impedance (1MΩ) and can easily be driven by various sources. Note that the voltage range of the external reference should stay within the compliance range of the reference input (0.5V to 1.25V).

POWER-DOWN MODE

The DAC2902 features a power-down function that can be used to reduce the total supply current to less than 6mA. Applying a logic HIGH to the PD pin will initiate the power-down mode, while a logic LOW enables normal operation. When left unconnected, an internal active pull-down circuit will enable the normal operation of the converter.

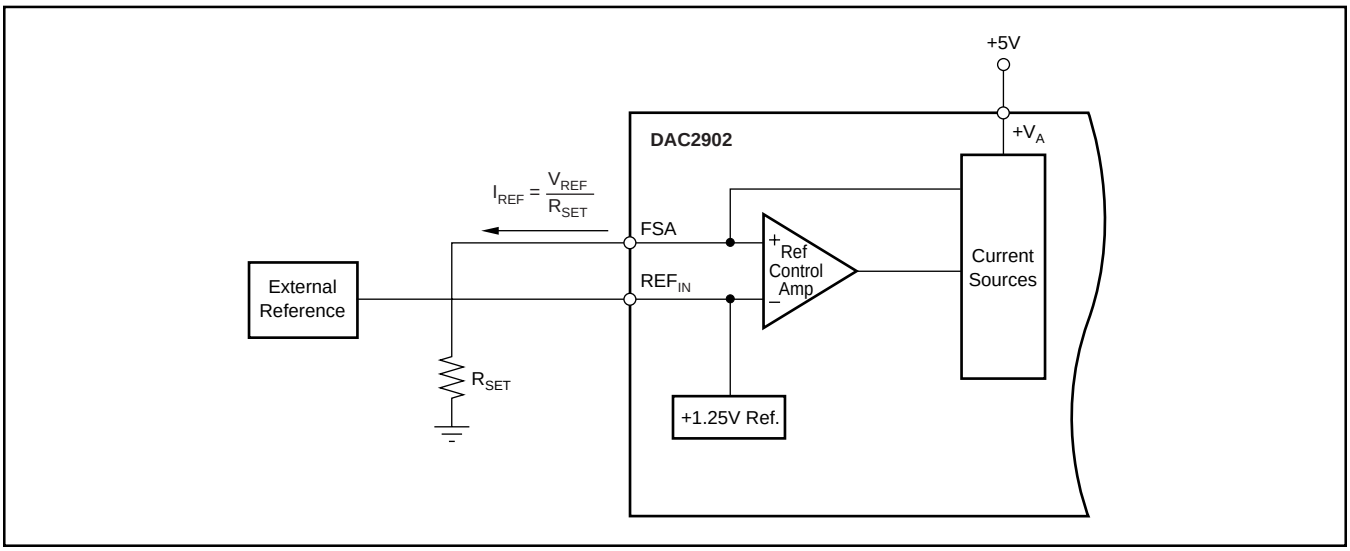


FIGURE 11. External Reference Configuration.

GROUNDING, DECOUPLING, AND LAYOUT INFORMATION

Proper grounding and bypassing, short lead length, and the use of ground planes are particularly important for high-frequency designs. Multilayer PCBs are recommended for best performance since they offer distinct advantages such as minimization of ground impedance, separation of signal layers by ground layers, etc.

The DAC2902 uses separate pins for its analog and digital supply and ground connections. The placement of the decoupling capacitor should be such that the analog supply ($+V_A$) is bypassed to the analog ground (AGND), and the digital supply bypassed to the digital ground (DGND). In most cases 0.1µF ceramic chip capacitors at each supply pin are adequate to provide a low impedance decoupling path. Keep in mind that their effectiveness largely depends on the proximity to the individual supply and ground pins. Therefore, they should be located as close as physically possible to those device leads. Whenever possible, the capacitors should be located immediately under each pair of supply/ground pins on the reverse side of the pc board. This layout approach will minimize the parasitic inductance of component leads and PCB runs.

Further supply decoupling with surface-mount tantalum capacitors (1µF to 4.7µF) may be added as needed in proximity of the converter.

Low noise is required for all supply and ground connections to the DAC2902. It is recommended to use a multilayer PCB utilizing separate power and ground planes. Mixed signal designs require particular attention to the routing of the different supply currents and signal traces. Generally, analog supply and ground planes should only extend into analog signal areas, such as the DAC output signal and the reference signal. Digital supply and ground planes must be confined to areas covering digital circuitry, including the digital input lines connecting to the converter, as well as the clock signal. The analog and digital ground planes should be joined together at one point underneath the DAC. This can be realized with a short track of approximately 1/8" (3mm).

The power to the DAC2902 should be provided through the use of wide PCB runs or planes. Wide runs will present a lower trace impedance, further optimizing the supply decoupling. The analog and digital supplies for the converter should only be connected together at the supply connector of the pc board. In the case of only one supply voltage being available to power the DAC, ferrite beads along with bypass capacitors may be used to create an LC filter. This will generate a low-noise analog supply voltage that can then be connected to the $+V_A$ supply pin of the DAC2902.

While designing the layout, it is important to keep the analog signal traces separated from any digital line, in order to prevent noise coupling onto the analog signal path.

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
9/08	C	1	–	Updated front page to standard format.
		2	Pkg/Ordering Info Table	Updated Package/Ordering Information table.
		3	Electrical Characteristics	Changed values for Supply Current and Power Dissipation.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
DAC2902Y/1K	ACTIVE	TQFP	PFB	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC2902Y/1KG4	ACTIVE	TQFP	PFB	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC2902Y/250	ACTIVE	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC2902Y/250G4	ACTIVE	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

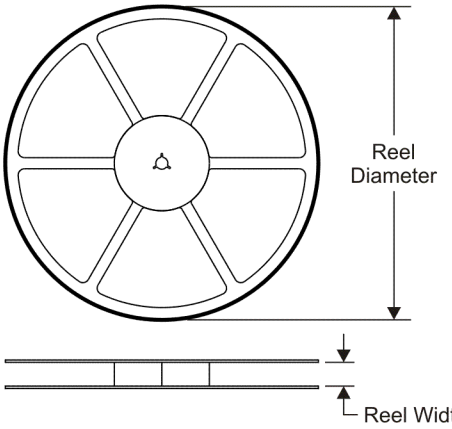
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

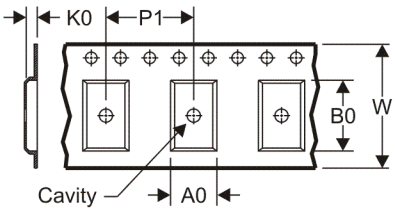
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

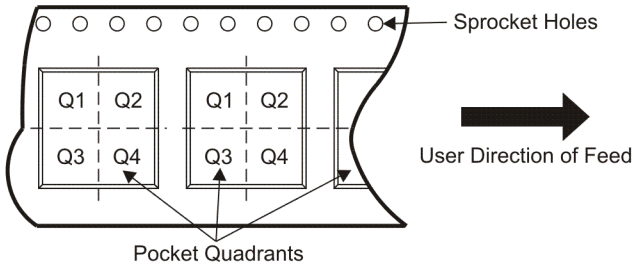


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

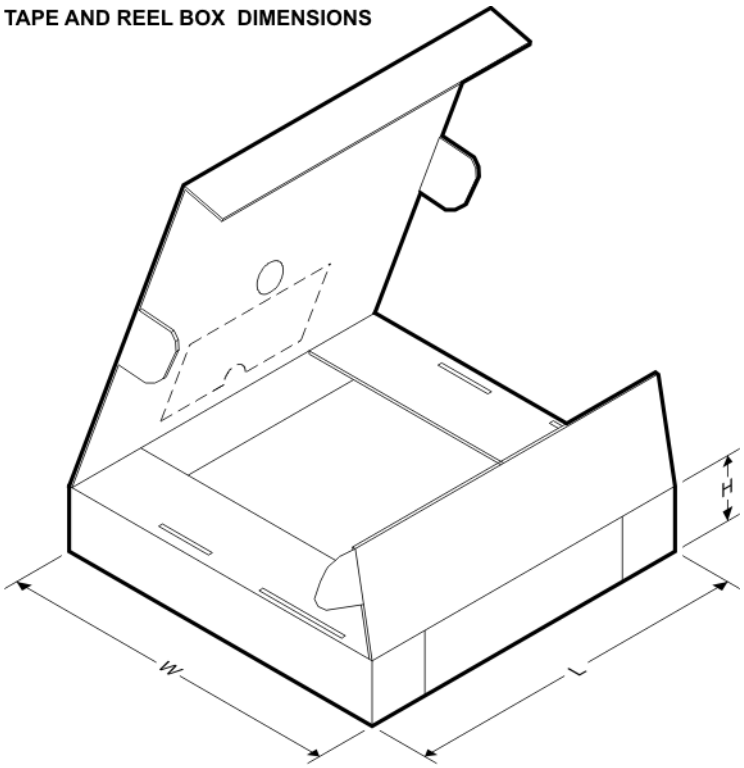
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC2902Y/1K	TQFP	PFB	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
DAC2902Y/250	TQFP	PFB	48	250	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS

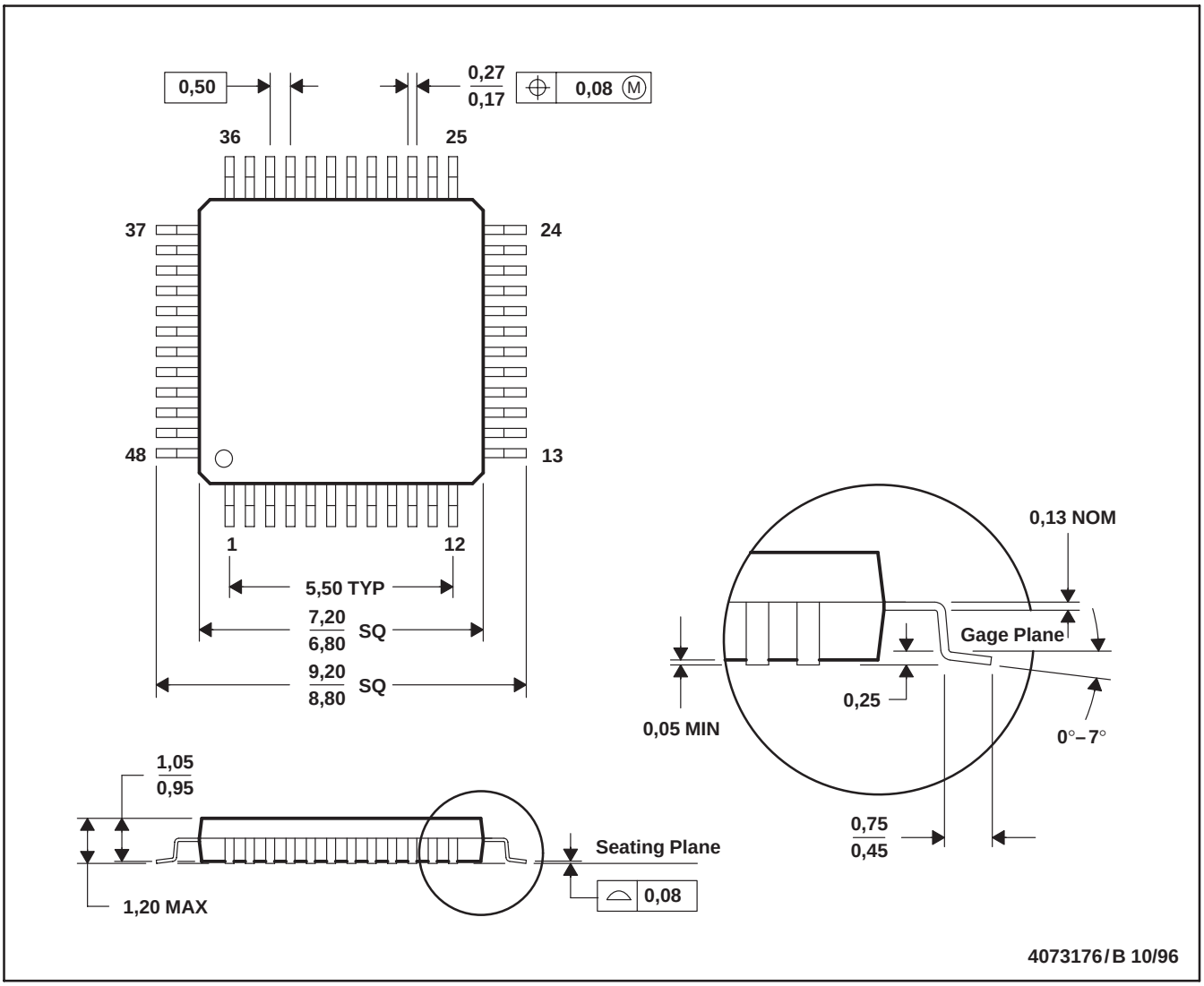


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC2902Y/1K	TQFP	PFB	48	1000	346.0	346.0	33.0
DAC2902Y/250	TQFP	PFB	48	250	346.0	346.0	33.0

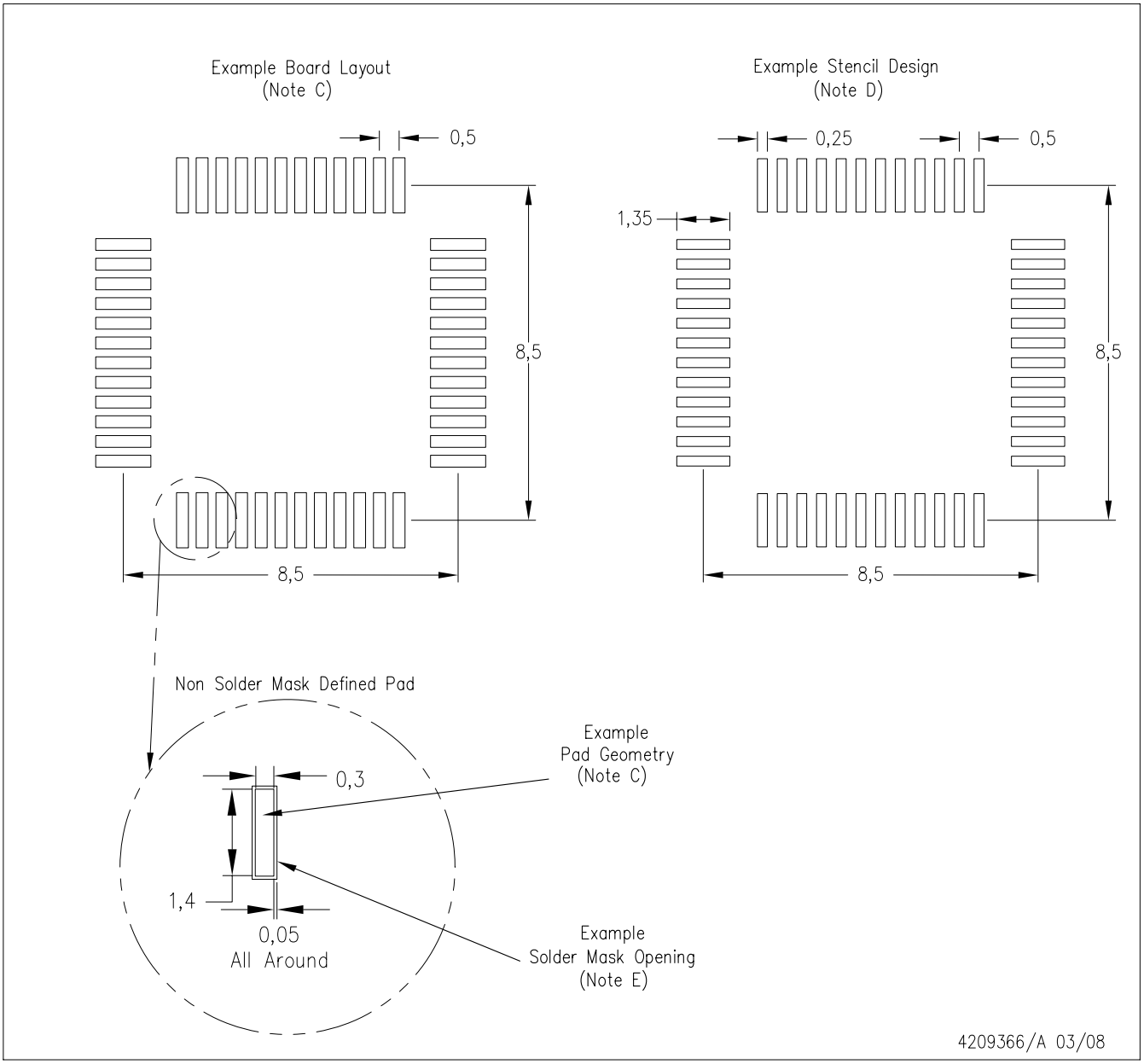
MTQF019A – JANUARY 1995 – REVISED JANUARY 1998

PFB (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PFB (S–PQFP–G48)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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