DUAL, 10-BIT 275 MSPS DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **10-Bit Dual Transmit Digital-to-Analog Converter (DAC)**
- **275 MSPS Update Rate**
- **Single Supply: 3.0 V to 3.6 V**
- **High Spurious-Free Dynamic Range (SFDR): 80 dBc at 5 MHz**
- **High Third-Order Two-Tone Intermodulation (IMD3): 78 dBc at 15.1 MHz and 16.1 MHz**
- **Independent or Single Resistor Gain Control**
- **Dual or Interleaved Data**
- **On-Chip 1.2-V Reference**
- **Low Power: 290 mW**
- **Power-Down Mode: 9 mW**
- **Package: 48-Pin Thin-Quad Flat Pack (TQFP)**

APPLICATIONS

- **Cellular Base Transceiver Station Transmit Channel**
  - **CDMA: W-CDMA, CDMA2000, IS-95**
  - **TDMA: GSM, IS-136, EDGE/UWC-136**
- **Medical/Test Instrumentation**
- **Arbitrary Waveform Generators (ARB)**
- **Direct Digital Synthesis (DDS)**
- **Cable Modem Termination System (CMTS)**

DESCRIPTION

The DAC5652 is a monolithic, dual-channel, 10-bit, high-speed DAC with on-chip voltage reference.

Operating with update rates of up to 275 MSPS, the DAC5652 offers exceptional dynamic performance, tight-gain, and offset matching characteristics that make it suitable in either I/Q baseband or direct IF communication applications.

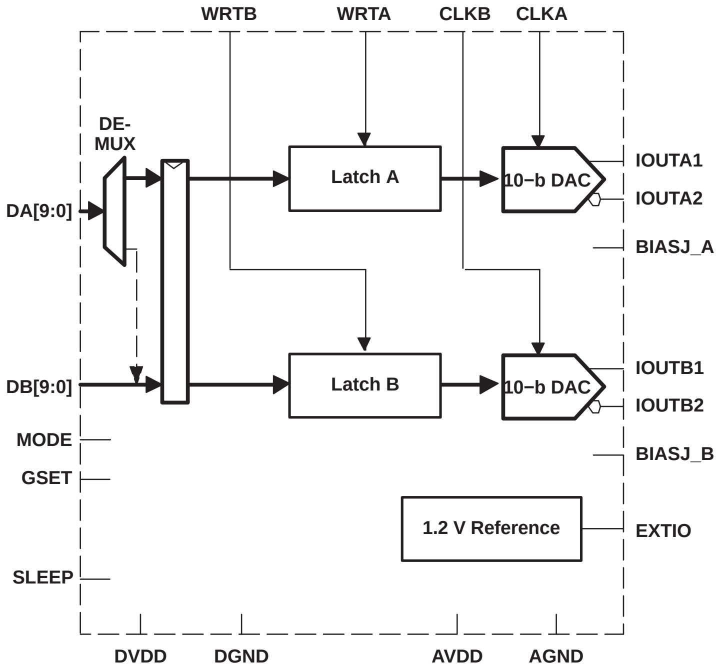
Each DAC has a high-impedance, differential-current output, suitable for single-ended or differential analog-output configurations. External resistors allow scaling of the full-scale output current for each DAC separately or together, typically between 2 mA and 20 mA. An accurate on-chip voltage reference is temperature-compensated and delivers a stable 1.2-V reference voltage. Optionally, an external reference may be used.

The DAC5652 has two, 10-bit, parallel input ports with separate clocks and data latches. For flexibility, the DAC5652 also supports multiplexed data for each DAC on one port when operating in the interleaved mode.

The DAC5652 has been specifically designed for a differential transformer-coupled output with a 50-Ω doubly-terminated load. For a 20-mA full-scale output current, both a 4:1 impedance ratio (resulting in an output power of 4 dBm) and 1:1 impedance ratio transformer (–2 dBm output power) are supported.

The DAC5652 is available in a 48-pin TQFP package. Pin compatibility between family members provides 10-bit (DAC5652), 12-bit (DAC5662), and 14-bit (DAC5672) resolution. Furthermore, the DAC5652 is pin compatible to the DAC2900 and AD9763 dual DACs. The device is characterized for operation over the industrial temperature range of –40°C to 85°C.

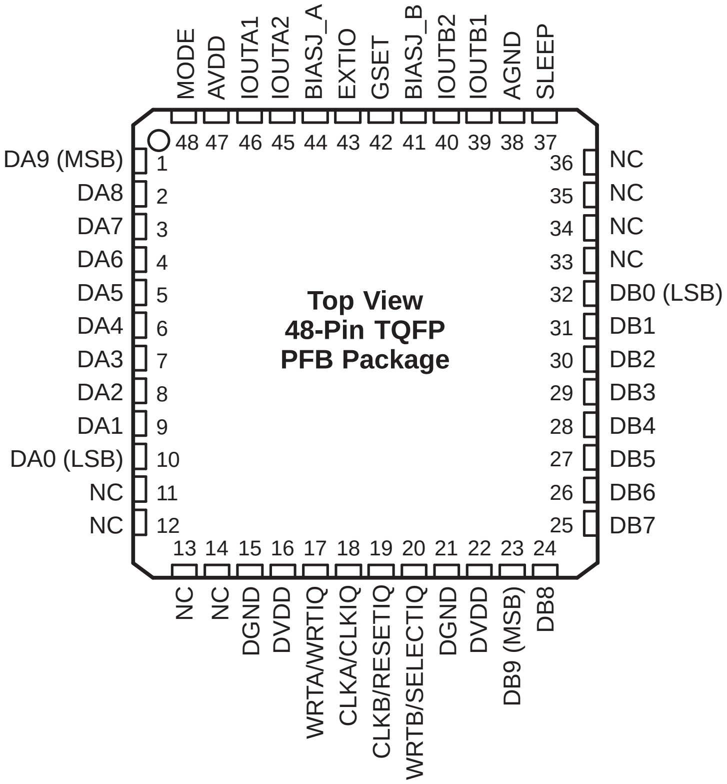
FUNCTIONAL BLOCK DIAGRAM



AVAILABLE OPTIONS

T_A	PACKAGED DEVICES 48-Pin TQFP
–40°C to 85°C	DAC5652IPFB
	DAC5652IPFBR

DEVICE INFORMATION



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGND	38	I	Analog ground
AVDD	47	I	Analog supply voltage
BIASJ_A	44	O	Full-scale output current bias for DACA
BIASJ_B	41	O	Full-scale output current bias for DACB
CLKA/CLKIQ	18	I	Clock input for DACA, CLKIQ in interleaved mode
CLKB/RESETIQ	19	I	Clock input for DACB, RESETIQ in interleaved mode
DA[9:0]	1-10	I	Data port A. DA9 is MSB and DA0 is LSB. Internal pulldown.
DB[9:0]	23-32	I	Data port B. DB9 is MSB and DB0 is LSB. Internal pulldown.
DGND	15, 21	I	Digital ground
DVDD	16, 22	I	Digital supply voltage
EXTIO	43	I/O	Internal reference output (bypass with 0.1 μF to AGND) or external reference input
GSET	42	I	Gain-setting mode: H – 1 resistor, L – 2 resistors. Internal pullup.
IOUTA1	46	O	DACA current output. Full-scale with all bits of DA high.
IOUTA2	45	O	DACA complementary current output. Full-scale with all bits of DA low.
IOUTB1	39	O	DACB current output. Full-scale with all bits of DB high.
IOUTB2	40	O	DACB complementary current output. Full-scale with all bits of DB low.
MODE	48	I	Mode Select: H – Dual Bus, L – Interleaved. Internal pullup.
NC	11-14, 33-36	-	Factory use only. Pins must be connected to DGND or left unconnected.
SLEEP	37	I	Sleep function control input: H – DAC in power-down mode, L – DAC in operating mode. Internal pulldown.
WRTA/WRTIQ	17	I	Input write signal for PORT A (WRTIQ in interleaving mode)
WRTB/SELECTIQ	20	I	Input write signal for PORT B (SELECTIQ in interleaving mode)

ABSOLUTE MAXIMUM RATINGS

over T_A (unless otherwise noted)(1)

		UNIT
Supply voltage range	AVDD(2)	–0.5 V to 4 V
	DVDD(3)	–0.5 V to 4 V
Voltage between AGND and DGND		–0.5 V to 0.5 V
Voltage between AVDD and DVDD		–0.5 V to 0.5 V
Supply voltage range	DA[9:0] and DB[9:0](3)	–0.5 V to DVDD + 0.5 V
	MODE, SLEEP, CLKA, CLKB, WRTA, WRTB(3)	–0.5 V to DVDD + 0.5 V
	IOUTA1, IOUTA2, IOUTB1, IOUTB2(2)	–1 V to AVDD + 0.5 V
	EXTIO, BIASJ_A, BIASJ_B, GSET(2)	–0.5 V to AVDD + 0.5 V
Peak input current (any input)		+20 mA
Peak total input current (all inputs)		–30 mA
Operating free-air temperature range		–40°C to 85°C
Storage temperature range		–65°C to 150°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Measured with respect to AGND.
(3) Measured with respect to DGND.

ELECTRICAL CHARACTERISTICS

over T_A, AVDD = DVDD = 3.3 V, I_{OUTFS} = 20 mA, independent gain set mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Specifications						
	Resolution		10			Bits
DC Accuracy(1)						
INL	Integral nonlinearity	1 LSB = $I_{OUTFS}/2^{10}$, T_{MIN} to T_{MAX}	–1	±0.25	1	LSB
DNL	Differential nonlinearity		–0.5	±0.16	0.5	LSB
Analog Output						
	Offset error	Midscale value (internal reference)		±0.05		%FSR
	Offset mismatch	Midscale value (internal reference)		±0.03		%FSR
	Gain error	With internal reference		±0.75		%FSR
	Minimum full-scale output current(2)			2		mA
	Maximum full-scale output current(2)			20		mA
	Gain mismatch	With internal reference	–2	0.2	2	%FSR
	Output voltage compliance range(3)		–1		1.25	V
R_O	Output resistance			300		kΩ
C_O	Output capacitance			5		pF
Reference Output						
	Reference voltage		1.14	1.2	1.26	V
	Reference output current(4)			100		nA
Reference Input						
V_{EXTIO}	Input voltage		0.1		1.25	V
R_I	Input resistance			1		MΩ
	Small signal bandwidth			300		kHz

(1) Measured differentially through 50 Ω to AGND.
(2) Nominal full-scale current, I_{OUTFS}, equals 32x the I_{BIAS} current.
(3) The lower limit of the output compliance is determined by the CMOS process. Exceeding this limit may result in transistor breakdown, resulting in reduced reliability of the DAC5652 device. The upper limit of the output compliance is determined by the load resistors and full-scale output current. Exceeding the upper limit adversely affects distortion performance and integral nonlinearity.
(4) Use an external buffer amplifier with high-impedance input to drive any external load.

ELECTRICAL CHARACTERISTICS (continued)

over T_A, AVDD = DVDD = 3.3 V, I_{OUTFS} = 20 mA, independent gain set mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_I	Input capacitance			100		pF
Temperature Coefficients						
	Offset drift			2		ppm of FSR/°C
	Gain drift	With external reference		±20		ppm of FSR/°C
		With internal reference		±40		ppm of FSR/°C
	Reference voltage drift			±20		ppm/°C

ELECTRICAL CHARACTERISTICS

over T_A, AVDD = DVDD = 3.3 V, I_{OUTFS} = 20 mA, f_{DATA} = 200 MSPS, f_{OUT} = 1 MHz, independent gain set mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply						
AVDD	Analog supply voltage		3	3.3	3.6	V
DVDD	Digital supply voltage		3	3.3	3.6	V
I_{AVDD}	Supply current, analog	Including output current through load resistor		75	90	mA
		Sleep mode with clock		2.5		
		Sleep mode without clock		2.5		
I_{DVDD}	Supply current, digital			12	20	mA
		Sleep mode with clock		11.3	18	
		Sleep mode without clock		0.6		
	Power dissipation			290	360	mW
		Sleep mode with clock		45.5		
		Sleep mode without clock		9.2		
		f_{DATA} = 275 MSPS, f_{OUT} = 20 MHz		310		
APSRR	Analog power supply rejection ratio		–0.2	–0.01	0.2	%FSR/V
DPSRR	Digital power supply rejection ratio		–0.2	0	0.2	%FSR/V
T_A	Operating free-air temperature		–40		85	°C

ELECTRICAL CHARACTERISTICS

AC specifications over T_A, AVDD = DVDD = 3.3 V, I_{OUTFS} = 20 mA, independent gain set mode, differential 1:1 impedance ratio transformer coupled output, 50-Ω doubly terminated load (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog Output						
f_{clk}	Maximum output update rate(1)		275			MSPS
t_s	Output settling time to 0.1% (DAC)	Mid-scale transition		20		ns
t_r	Output rise time 10% to 90% (OUT)			1.4		ns
t_f	Output fall time 90% to 10% (OUT)			1.5		ns
	Output noise	I_{OUTFS} = 20 mA		55		pA/√Hz
		I_{OUTFS} = 2 mA		30		
AC Linearity						
SFDR	Spurious-free dynamic range	1st Nyquist zone, T_A = 25°C, f_{DATA} = 50 MSPS, f_{OUT} = 1 MHz, I_{OUTFS} = 0 dB		79		dBc
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 50 MSPS, f_{OUT} = 1 MHz, I_{OUTFS} = –6 dB		78		
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 50 MSPS, f_{OUT} = 1 MHz, I_{OUTFS} = –12 dB		73		
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 100 MSPS, f_{OUT} = 5 MHz, I_{OUTFS} = 0 dB		80		
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 100 MSPS, f_{OUT} = 20 MHz, I_{OUTFS} = 0 dB		76		
		1st Nyquist zone, T_{MIN} to T_{MAX}, f_{DATA} = 200 MSPS, f_{OUT} = 20 MHz, I_{OUTFS} = 0 dB	61	70		
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 200 MSPS, f_{OUT} = 41 MHz, I_{OUTFS} = 0 dB		67		
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 275 MSPS, f_{OUT} = 20 MHz		70		
SNR	Signal-to-noise ratio	1st Nyquist zone, T_A = 25°C, f_{DATA} = 100 MSPS, f_{OUT} = 5 MHz, I_{OUTFS} = 0 dB		63		dB
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 160 MSPS, f_{OUT} = 20 MHz, I_{OUTFS} = 0 dB		62		dB
IMD3	Third-order two-tone intermodulation	Each tone at –6 dBFS, T_A = 25°C, f_{DATA} = 200 MSPS, f_{OUT} = 45.4 MHz and 46.4 MHz		61		dBc
		Each tone at –6 dBFS, T_A = 25°C, f_{DATA} = 100 MSPS, f_{OUT} = 15.1 MHz and 16.1 MHz		78		
IMD	Four-tone intermodulation	Each tone at –12 dBFS, T_A = 25°C f_{DATA} = 100 MSPS, f_{OUT} = 15.6, 15.8, 16.2, and 16.4 MHz		76		dBc
		Each tone at –12 dBFS, T_A = 25°C f_{DATA} = 165 MSPS, f_{OUT} = 19.0, 19.1, 19.3, and 19.4 MHz		55		
		Each tone at –12 dBFS, T_A = 25°C f_{DATA} = 165 MSPS, f_{OUT} = 68.8, 69.6, 71.2, and 72.0 MHz		70		
	Channel isolation	T_A = 25°C, f_{DATA} = 165 MSPS f_{OUT} (CH1) = 20 MHz, f_{OUT} (CH2) = 21 MHz		90		dBc

(1) Specified by design and bench characterization. Not production tested.

ELECTRICAL CHARACTERISTICS

Digital specifications over T_A, AVDD = DVDD = 3.3 V, I_{OUTFS} = 20 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Input						
V_{IH}	High-level input voltage		2		3.3	V
V_{IL}	Low-level input voltage		0		0.8	V
I_{IH}	High-level input current			±50		A
I_{IL}	Low-level input current			±10		A
$I_{IH(GSET)}$	High-level input current, GSET pin			7		A
$I_{IL(GSET)}$	Low-level input current, GSET pin			–80		A
$I_{IH(MODE)}$	High-level input current, MODE pin			–30		A
$I_{IL(MODE)}$	Low-level input current, MODE pin			–80		A
C_I	Input capacitance			5		pF

SWITCHING CHARACTERISTICS

Digital specifications over T_A, AVDD = DVDD = 3.3 V, I_{OUTFS} = 20 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Timing - Dual Bus Mode						
t_{su}	Input setup time		1			ns
t_h	Input hold time		1			ns
t_{LPH}	Input clock pulse high time			1		ns
t_{LAT}	Clock latency (WRTA/B to outputs)		4		4	clk
t_{PD}	Propagation delay time			1.5		ns
Timing - Single Bus Interleaved Mode						
t_{su}	Input setup time			0.5		ns
t_h	Input hold time			0.5		ns
t_{LAT}	Clock latency (WRTA/B to outputs)		4		4	clk
t_{PD}	Propagation delay time			1.5		ns

TYPICAL CHARACTERISTICS

INTEGRAL NONLINEARITY
vs
INPUT CODE

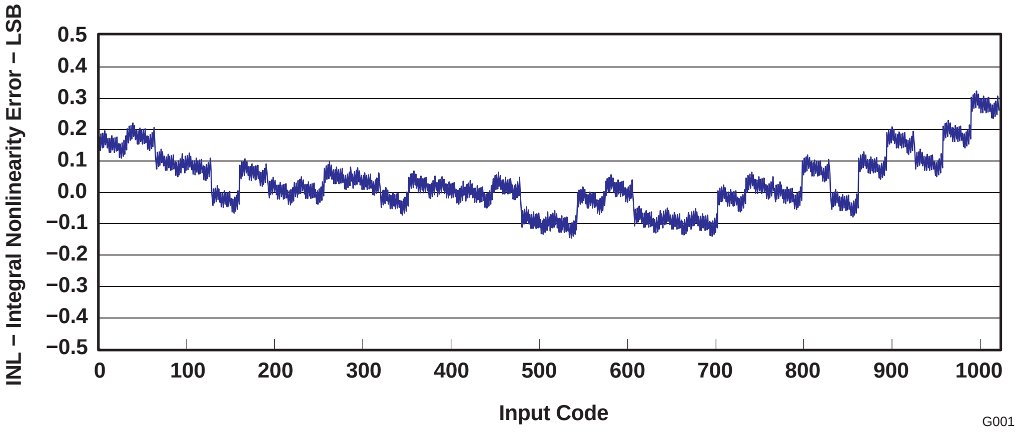


Figure 1.

DIFFERENTIAL NONLINEARITY
vs
INPUT CODE

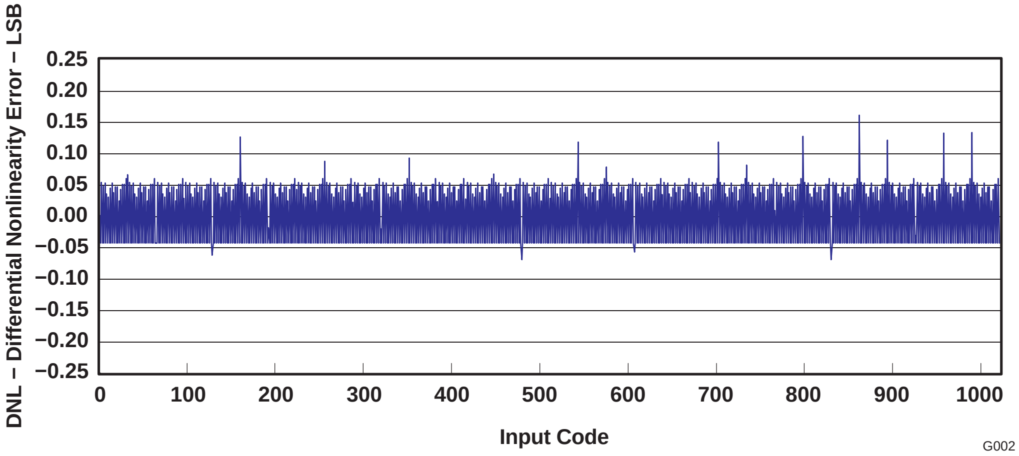


Figure 2.

TYPICAL CHARACTERISTICS (continued)

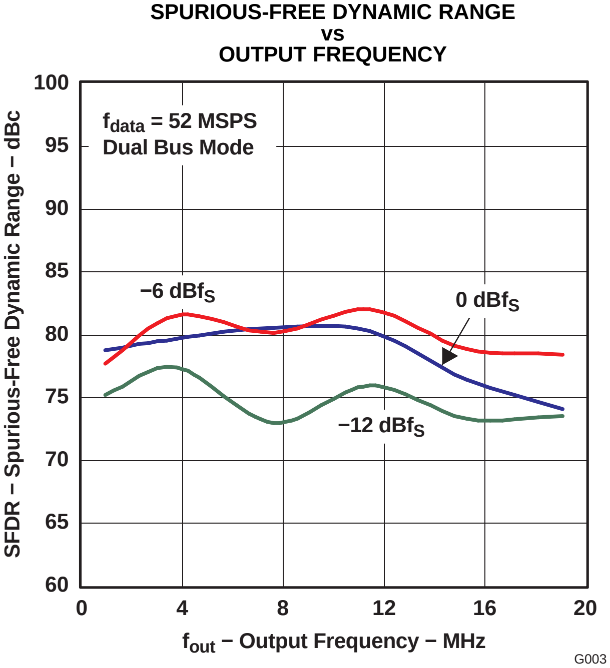


Figure 3.

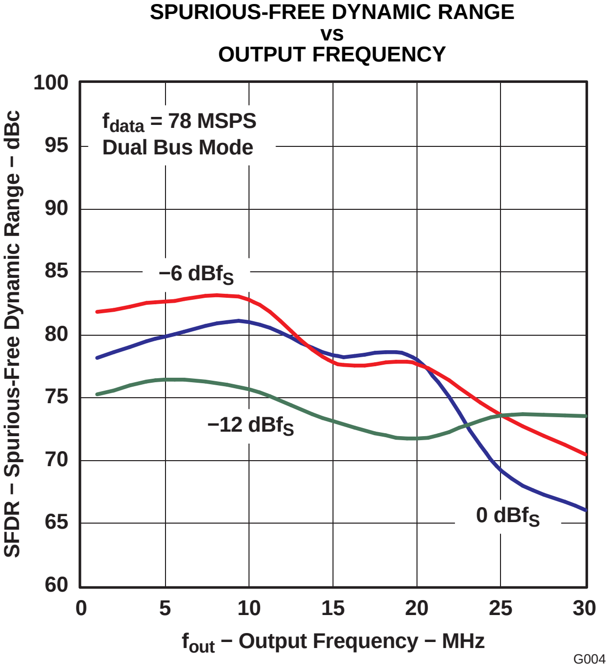


Figure 4.

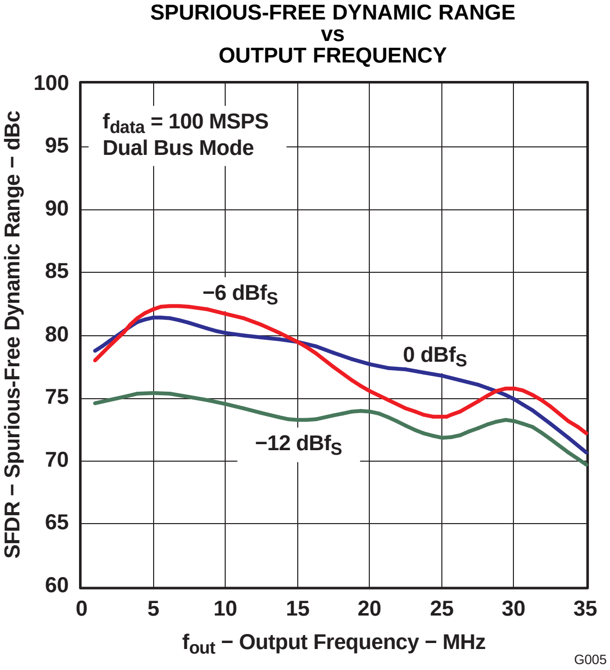


Figure 5.

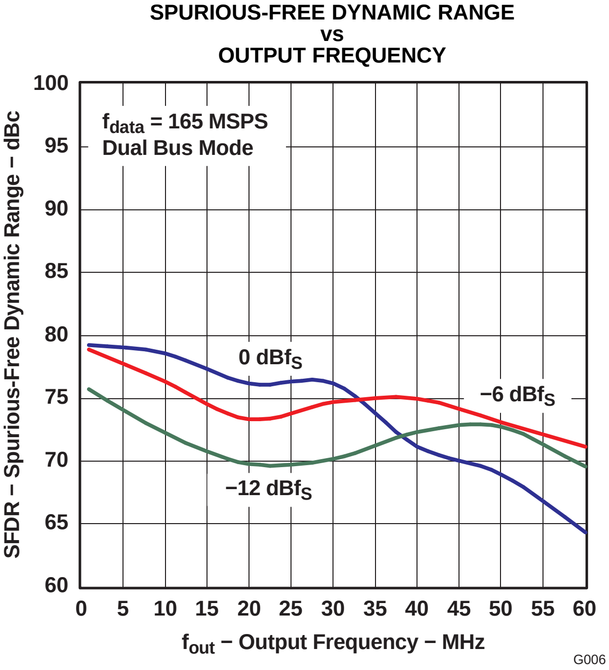


Figure 6.

TYPICAL CHARACTERISTICS (continued)

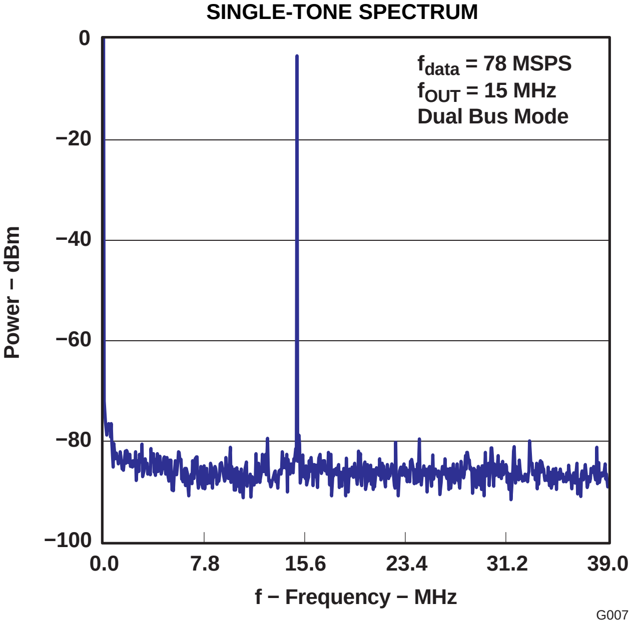
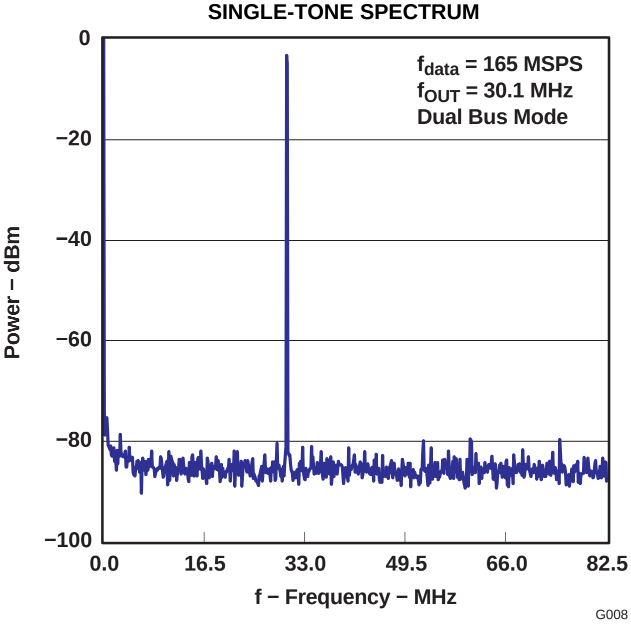


Figure 7.



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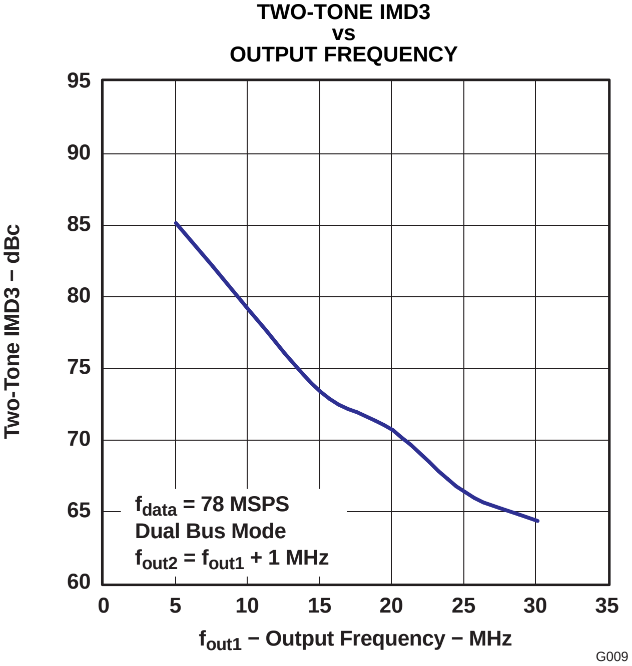

Figure 9.

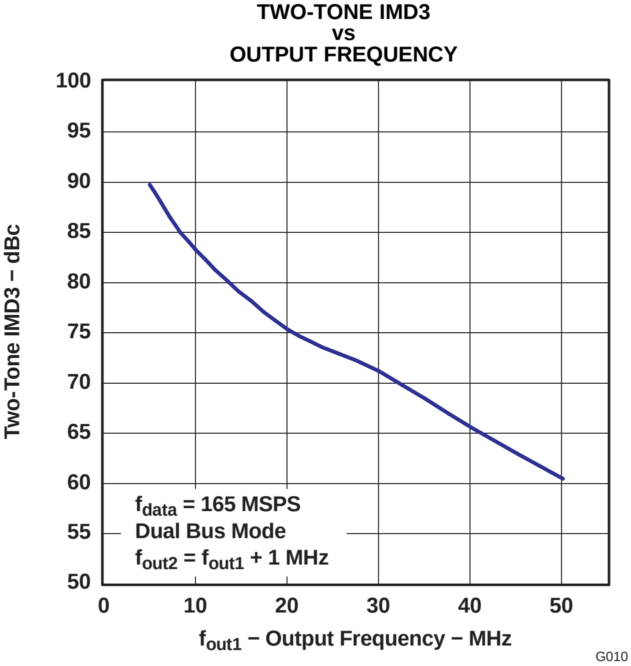

Figure 10.

TYPICAL CHARACTERISTICS (continued)

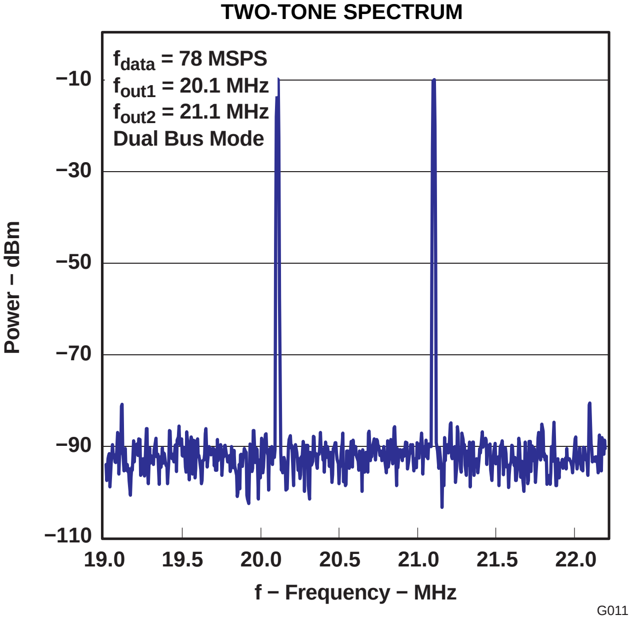

Figure 11.

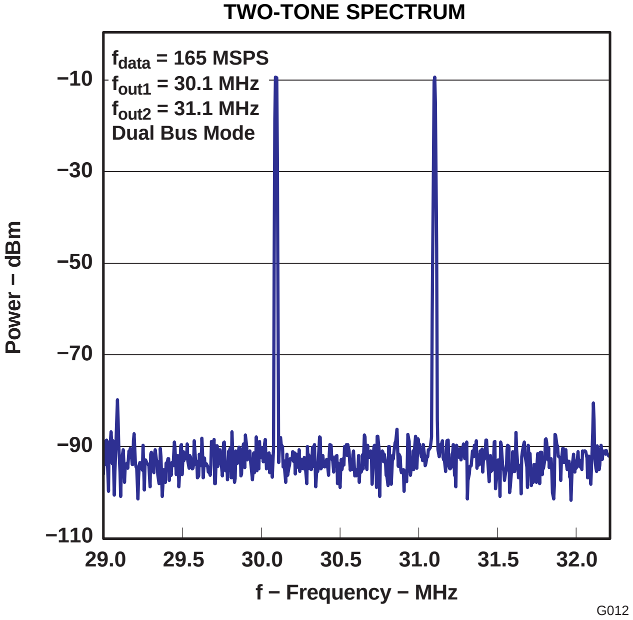

Figure 12.

Digital Inputs and Timing

Digital Inputs

The data input ports of the DAC5652 accept a standard positive coding with data bits DA9 and DB9 being the most significant bits (MSB). The converter outputs support a clock rate of up to 275 MSPS. The best performance is typically achieved with a symmetric duty cycle for write and clock; however, the duty cycle may vary as long as the timing specifications are met. Similarly, the setup and hold times may be chosen within their specified limits.

All digital inputs of the DAC5652 are CMOS compatible. Figure 13 and Figure 14 show schematics of the equivalent CMOS digital inputs of the DAC5652. The pullup and pulldown circuitry is approximately equivalent to 100kΩ.The 10-bit digital data input follows the offset positive binary coding scheme. The DAC5652 is designed to operate with a digital supply (DVDD) of 3 V to 3.6 V.

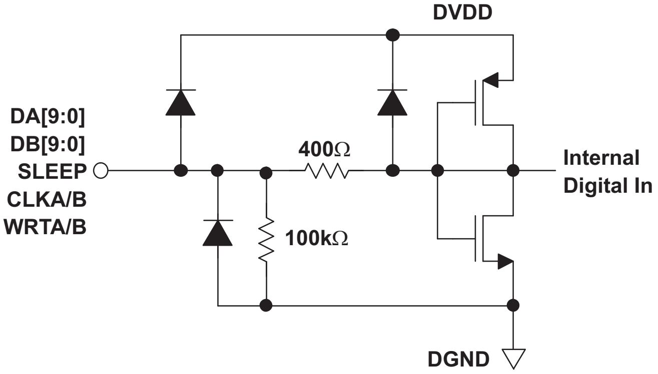

Figure 13. CMOS/TTL Digital Equivalent Input With Internal Pulldown Resistor

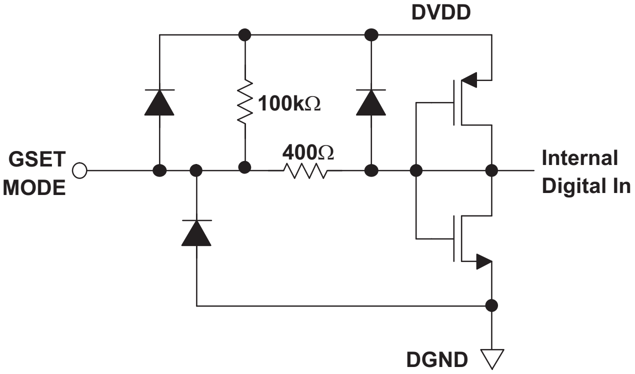

Figure 14. CMOS/TTL Digital Equivalent Input With Internal Pullup Resistor

Input Interfaces

The DAC5652 features two operating modes selected by the MODE pin, as shown in Table 1.

- For dual-bus input mode, the device essentially consists of two separate DACs. Each DAC has its own separate data input bus, clock input, and data write signal (data latch-in).
- In single-bus interleaved mode, the data must be presented interleaved at the A-channel input bus. The B-channel input bus is not used in this mode. The clock and write input are now shared by both DACs.

Table 1. Operating Modes

MODE Pin	MODE pin connected to DGND	MODE pin connected to DVDD
Bus input	Single-bus interleaved mode, clock and write input equal for both DACs	Dual-bus mode, DACs operate independently

Dual-Bus Data Interface and Timing

In dual-bus mode, the MODE pin is connected to DVDD. The two converter channels within the DAC5652 consist of two independent, 10-bit, parallel data ports. Each DAC channel is controlled by its own set of write (WRTA, WRTB) and clock (CLKA, CLKB) lines. The WRTA/B lines control the channel input latches and the CLKA/B lines control the DAC latches. The data is first loaded into the input latch by a rising edge of the WRTA/B line.

The internal data transfer requires a correct sequence of write and clock inputs, since essentially two clock domains having equal periods (but possibly different phases) are input to the DAC5652. This is defined by a minimum requirement of the time between the rising edge of the clock and the rising edge of the write inputs. This essentially implies that the rising edge of CLKA/B must occur at the same time or before the rising edge of the WRTA/B signal. A minimum delay of 2 ns must be maintained if the rising edge of the clock occurs after the rising edge of the write. Note that these conditions are satisfied when the clock and write inputs are connected externally. Note that all specifications were measured with the WRTA/B and CLKA/B lines connected together.

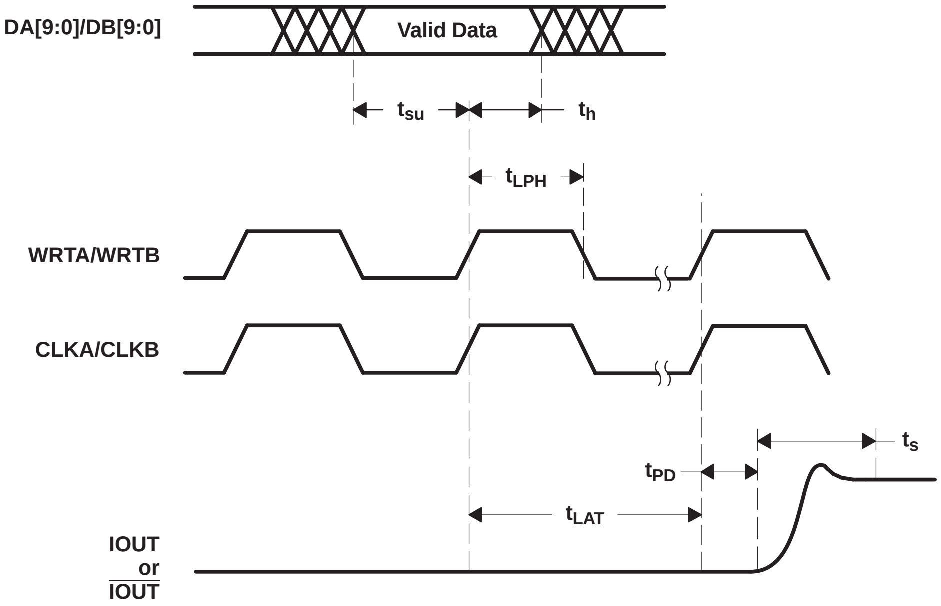

Figure 15. Dual-Bus Mode Operation

Single-Bus Interleaved Data Interface and Timing

In single-bus interleaved mode, the MODE pin is connected to DGND. Figure 16 shows the timing diagram. In interleaved mode, the A- and B-channels share the write input (WRTIQ) and update clock (CLKIQ and internal CLKDACIQ). Multiplexing logic directs the input word at the A-channel input bus to either the A-channel input latch (SELECTIQ is high) or to the B-channel input latch (SELECTIQ is low). When SELECTIQ is high, the data value in the B-channel latch is retained by presenting the latch output data to its input again. When SELECTIQ is low, the data value in the A-channel latch is retained by presenting the latch output data to its input.

In interleaved mode, the A-channel input data rate is twice the update rate of the DAC core. As in dual-bus mode, it is important to maintain a correct sequence of write and clock inputs. The edge-triggered flip-flops latch the A- and B-channel input words on the rising edge of the write input (WRTIQ). This data is presented to the A- and B-DAC latches on the following falling edge of the write inputs. The DAC5652 clock input is divided by a factor of two before it is presented to the DAC latches.

Correct pairing of the A- and B-channel data is done by RESETIQ. In interleaved mode, the clock input CLKIQ is divided by two, which would translate to a non-deterministic relation between the rising edges of the CLKIQ and CLKDACIQ. RESETIQ ensures, however, that the correct position of the rising edge of CLKDACIQ with respect to the data at the input of the DAC latch is determined. CLKDACIQ is disabled (low) when RESETIQ is high.

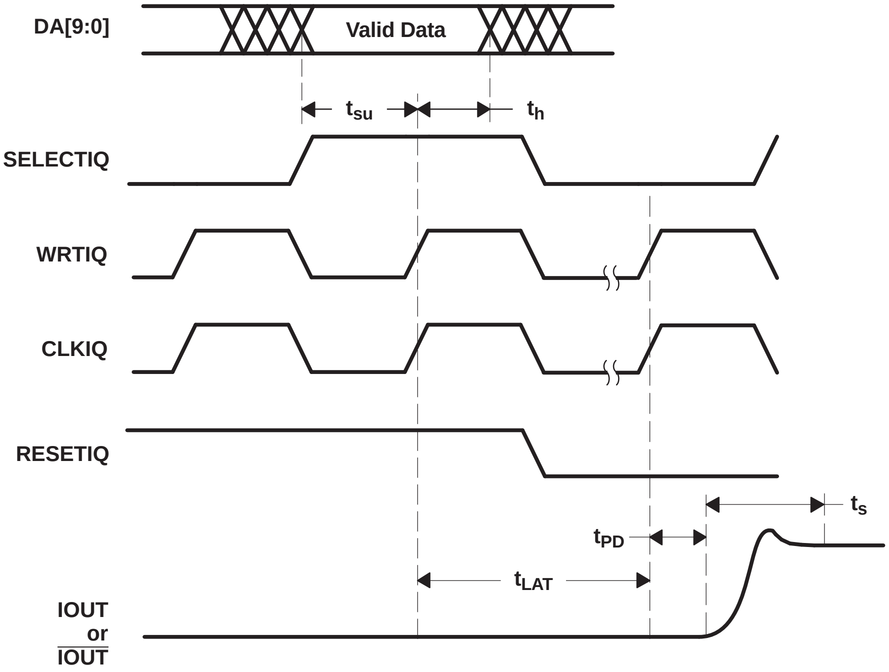

Figure 16. Single-Bus Interleaved Mode Operation

APPLICATION INFORMATION

Theory of Operation

The architecture of the DAC5652 uses a current steering technique to enable fast switching and high update rate. The core element within the monolithic DAC is an array of segmented current sources that are designed to deliver a full-scale output current of up to 20 mA. An internal decoder addresses the differential current switches each time the DAC is updated and a corresponding output current is formed by steering all currents to either output summing node, IOUT1 or IOUT2. The complementary outputs deliver a differential output signal, which improves the dynamic performance through reduction of even-order harmonics, common-mode signals (noise), and double the peak-to-peak output signal swing by a factor of two, as compared to single-ended operation.

The segmented architecture results in a significant reduction of the glitch energy and improves the dynamic performance (SFDR) and DNL. The current outputs maintain a very high output impedance of greater than 300 kΩ.

When pin 42 (GSET) is high (simultaneous gain set mode), the full-scale output current for both DACs is determined by the ratio of the internal reference voltage (1.2 V) and an external resistor (R_{SET}) connected to BIASJ_A. When GSET is low (independent gain set mode), the full-scale output current for each DAC is determined by the ratio of the internal reference voltage (1.2 V) and separate external resistors (R_{SET}) connected to BIASJ_A and BIASJ_B. The resulting I_{REF} is internally multiplied by a factor of 32 to produce an effective DAC output current that can range from 2 mA to 20 mA, depending on the value of R_{SET}.

The DAC5652 is split into a digital and an analog portion, each of which is powered through its own supply pin. The digital section includes edge-triggered input latches and the decoder logic, while the analog section comprises both the current source array with its associated switches, and the reference circuitry.

DAC Transfer Function

Each of the DACs in the DAC5652 has a set of complementary current outputs, IOUT1 and IOUT2. The full-scale output current, I_{OUTFS}, is the summation of the two complementary output currents:

$$I_{OUTFS} = I_{OUT1} + I_{OUT2} \tag{1}$$

The individual output currents depend on the DAC code and can be expressed as:

$$I_{OUT1} = I_{OUTFS} \times \left(\frac{Code}{1024}\right) \tag{2}$$

$$I_{OUT2} = I_{OUTFS} \times \left(\frac{1023 - Code}{1024}\right) \tag{3}$$

where Code is the decimal representation of the DAC data input word. Additionally, I_{OUTFS} is a function of the reference current I_{REF}, which is determined by the reference voltage and the external setting resistor (R_{SET}).

$$I_{OUTFS} = 32 \times I_{REF} = 32 \times \frac{V_{REF}}{R_{SET}} \tag{4}$$

In most cases, the complementary outputs drive resistive loads or a terminated transformer. A signal voltage develops at each output according to:

$$V_{OUT1} = I_{OUT1} \times R_{LOAD} \tag{5}$$

$$V_{OUT2} = I_{OUT2} \times R_{LOAD} \tag{6}$$

The value of the load resistance is limited by the output compliance specification of the DAC5652. To maintain specified linearity performance, the voltage for IOUT1 and IOUT2 must not exceed the maximum allowable compliance range.

The total differential output voltage is:

$$V_{OUTDIFF} = V_{OUT1} - V_{OUT2} \tag{7}$$

$$V_{OUTDIFF} = \frac{(2 \times \text{Code} - 1023)}{1024} \times I_{OUTFS} \times R_{LOAD} \tag{8}$$

Analog Outputs

The DAC5652 provides two complementary current outputs, IOUT1 and IOUT2. The simplified circuit of the analog output stage representing the differential topology is shown in Figure 17. The output impedance of IOUT1 and IOUT2 results from the parallel combination of the differential switches, along with the current sources and associated parasitic capacitances.

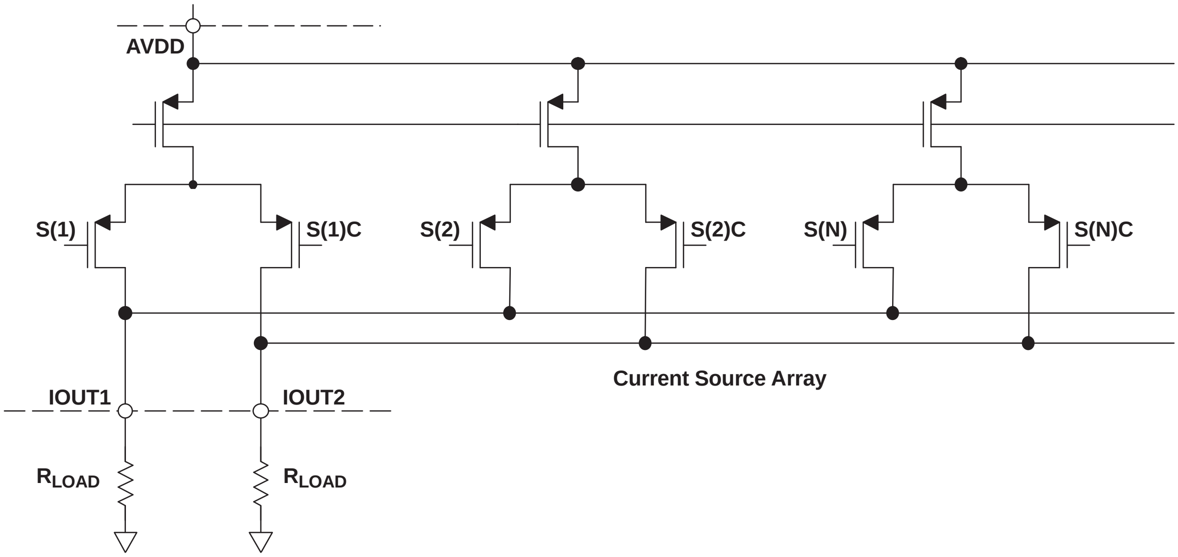

Figure 17. Analog Outputs

The signal voltage swing that may develop at the two outputs, IOUT1 and IOUT2, is limited by a negative and positive compliance. The negative limit of –1 V is given by the breakdown voltage of the CMOS process and exceeding it compromises the reliability of the DAC5652 (or even causes permanent damage). With the full-scale output set to 20 mA, the positive compliance equals 1.2 V. Note that the compliance range decreases to about 1 V for a selected output current of I_{OUTFS} = 2 mA. Care must be taken that the configuration of DAC5652 does not exceed the compliance range to avoid degradation of the distortion performance and integral linearity.

Best distortion performance is typically achieved with the maximum full-scale output signal limited to approximately 0.5 V_{PP}. This is the case for a 50-Ω doubly-terminated load and a 20-mA full-scale output current. A variety of loads can be adapted to the output of the DAC5652 by selecting a suitable transformer while maintaining optimum voltage levels at IOUT1 and IOUT2. Furthermore, using the differential output configuration in combination with a transformer is instrumental for achieving excellent distortion performance. Common-mode errors, such as even-order harmonics or noise, can be substantially reduced. This is particularly the case with high output frequencies.

For those applications requiring the optimum distortion and noise performance, it is recommended to select a full-scale output of 20 mA. A lower full-scale range of 2 mA may be considered for applications that require low power consumption, but can tolerate a slight reduction in performance level.

Output Configurations

The current outputs of the DAC5652 allow for a variety of configurations. As mentioned previously, utilizing the converter's differential outputs yield the best dynamic performance. Such a differential output circuit may consist of an RF transformer or a differential amplifier configuration. The transformer configuration is ideal for most applications with ac coupling, while op amps are suitable for a dc-coupled configuration.

The single-ended configuration may be considered for applications requiring a unipolar output voltage. Connecting a resistor from either one of the outputs to ground converts the output current into a ground-referenced voltage signal. To improve on the dc linearity by maintaining a virtual ground, an I-to-V or op-amp configuration may be considered.

Differential With Transformer

Using an RF transformer provides a convenient way of converting the differential output signal into a single-ended signal while achieving excellent dynamic performance. The appropriate transformer must be carefully selected based on the output frequency spectrum and impedance requirements.

The differential transformer configuration has the benefit of significantly reducing common-mode signals, thus improving the dynamic performance over a wide range of frequencies. Furthermore, by selecting a suitable impedance ratio (winding ratio) the transformer can provide optimum impedance matching while controlling the compliance voltage for the converter outputs.

Figure 18 and Figure 19 show 50-Ω doubly-terminated transformer configurations with 1:1 and 4:1 impedance ratios, respectively. Note that the center tap of the primary input of the transformer has to be grounded to enable a dc-current flow. Applying a 20-mA full-scale output current would lead to a 0.5-V_{PP} output for a 1:1 transformer and a 1-V_{PP} output for a 4:1 transformer. In general, the 1:1 transformer configuration will have slightly better output distortion, but the 4:1 transformer will have 6 dB higher output power.

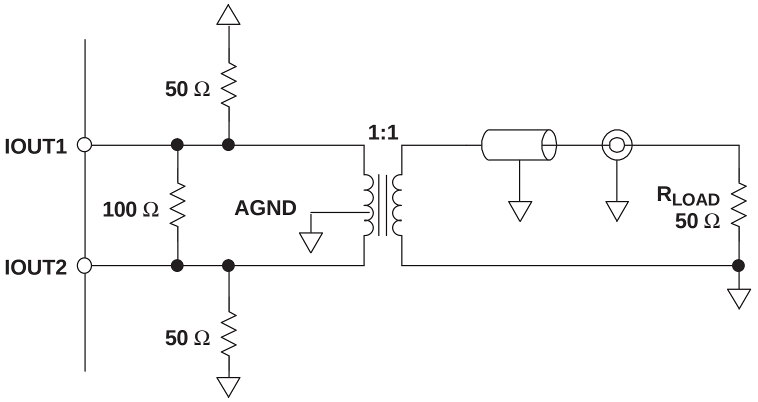

Figure 18. Driving a Doubly-Terminated 50-Ω Cable Using a 1:1 Impedance Ratio Transformer

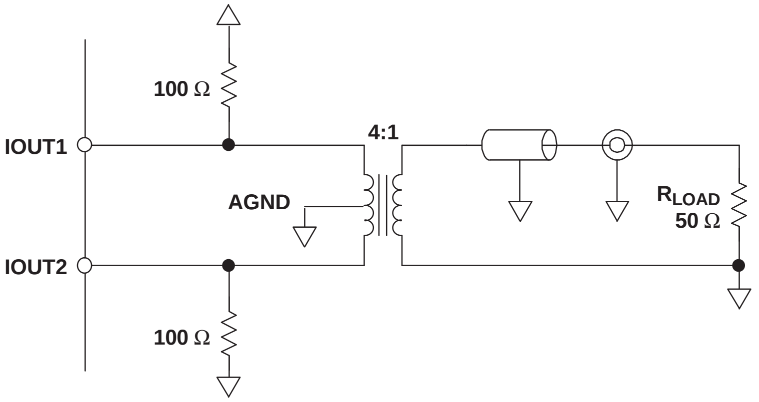

Figure 19. Driving a Doubly-Terminated 50-Ω Cable Using a 4:1 Impedance Ratio Transformer

Single-Ended Configuration

Figure 20 shows the single-ended output configuration, where the output current I_{OUT1} flows into an equivalent load resistance of 25 Ω. Node IOUT2 must be connected to AGND or terminated with a resistor of 25 Ω to AGND. The nominal resistor load of 25 Ω gives a differential output swing of 1 V_{PP} when applying a 20-mA full-scale output current.

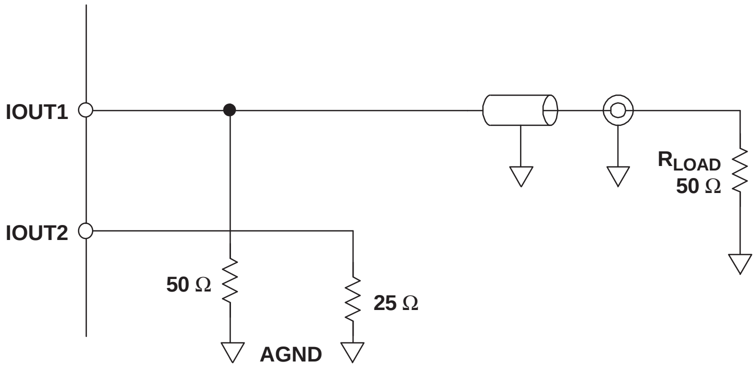

Figure 20. Driving a Doubly-Terminated 50-Ω Cable Using a Single-Ended Output

Reference Operation

Internal Reference

The DAC5652 has an on-chip reference circuit which comprises a 1.2-V bandgap reference and two control amplifiers, one for each DAC. The full-scale output current, I_{OUTFS}, of the DAC5652 is determined by the reference voltage, V_{REF}, and the value of resistor R_{SET}. I_{OUTFS} can be calculated by:

$$I_{OUTFS} = 32 \times I_{REF} = 32 \times \frac{V_{REF}}{R_{SET}} \tag{9}$$

The reference control amplifier operates as a V-to-I converter producing a reference current, I_{REF}, which is determined by the ratio of V_{REF} and R_{SET} (see Equation 9). The full-scale output current, I_{OUTFS}, results from multiplying I_{REF} by a fixed factor of 32.

Using the internal reference, a 2-kΩ resistor value results in a full-scale output of approximately 20 mA. Resistors with a tolerance of 1% or better should be considered. Selecting higher values, the output current can be adjusted from 20 mA down to 2 mA. Operating the DAC5652 at lower than 20-mA output currents may be desirable for reasons of reducing the total power consumption, improving the distortion performance, or observing the output compliance voltage limitations for a given load condition.

It is recommended to bypass the EXTIO pin with a ceramic chip capacitor of 0.1 F or more. The control amplifier is internally compensated and its small signal bandwidth is approximately 300 kHz.

External Reference

The internal reference can be disabled by simply applying an external reference voltage into the EXTIO pin, which in this case functions as an input. The use of an external reference may be considered for applications that require higher accuracy and drift performance or to add the ability of dynamic gain control.

While a 0.1-µF capacitor is recommended to be used with the internal reference, it is optional for the external reference operation. The reference input, EXTIO, has a high input impedance (1 MΩ) and can easily be driven by various sources. Note that the voltage range of the external reference must stay within the compliance range of the reference input.

Gain Setting Option

The full-scale output current on the DAC5652 can be set two ways: either for each of the two DAC channels independently or for both channels simultaneously. For the independent gain set mode, the GSET pin (pin 42) must be low (that is, connected to AGND). In this mode, two external resistors are required — one R_{SET} connected to the BIASJ_A pin (pin 44) and the other to the BIASJ_B pin (pin 41). In this configuration, the user has the flexibility to set and adjust the full-scale output current for each DAC independently, allowing for the compensation of possible gain mismatches elsewhere within the transmit signal path.

Alternatively, bringing the GSET pin high (that is, connected to AVDD), the DAC5652 switches into the simultaneous gain set mode. Now the full-scale output current of both DAC channels is determined by only one external R_{SET} resistor connected to the BIASJ_A pin. The resistor at the BIASJ_B pin may be removed; however, this is not required since this pin is not functional in this mode and the resistor has no effect on the gain equation.

Sleep Mode

The DAC5652 features a power-down function which can reduce the total supply current to approximately 3.1 mA over the specified supply range if no clock is present. Applying a logic high to the SLEEP pin initiates the power-down mode, while a logic low enables normal operation. When left unconnected, an internal active pulldown circuit enables the normal operation of the converter.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
DAC5652IPFB	ACTIVE	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC5652IPFBG4	ACTIVE	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC5652IPFBR	ACTIVE	TQFP	PFB	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC5652IPFBRG4	ACTIVE	TQFP	PFB	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF DAC5652 :

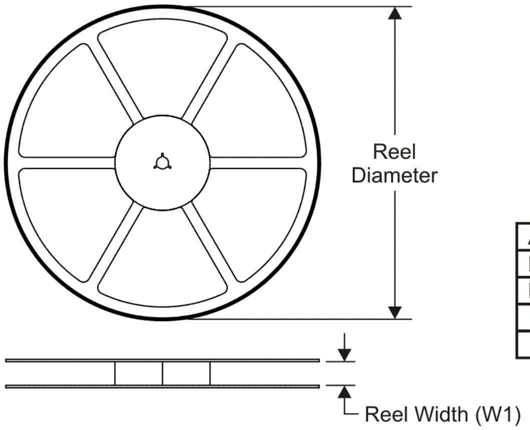
- Enhanced Product: DAC5652-EP

NOTE: Qualified Version Definitions:

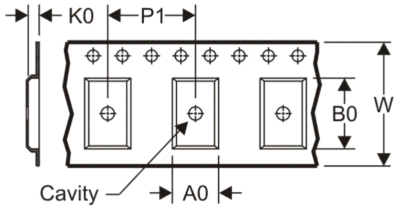
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

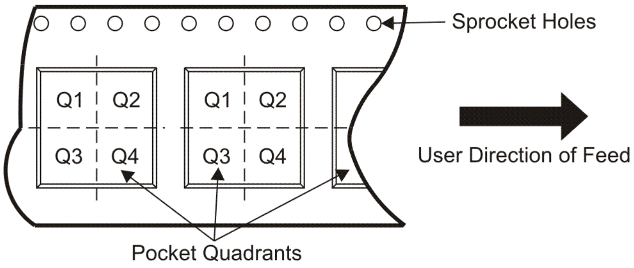


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

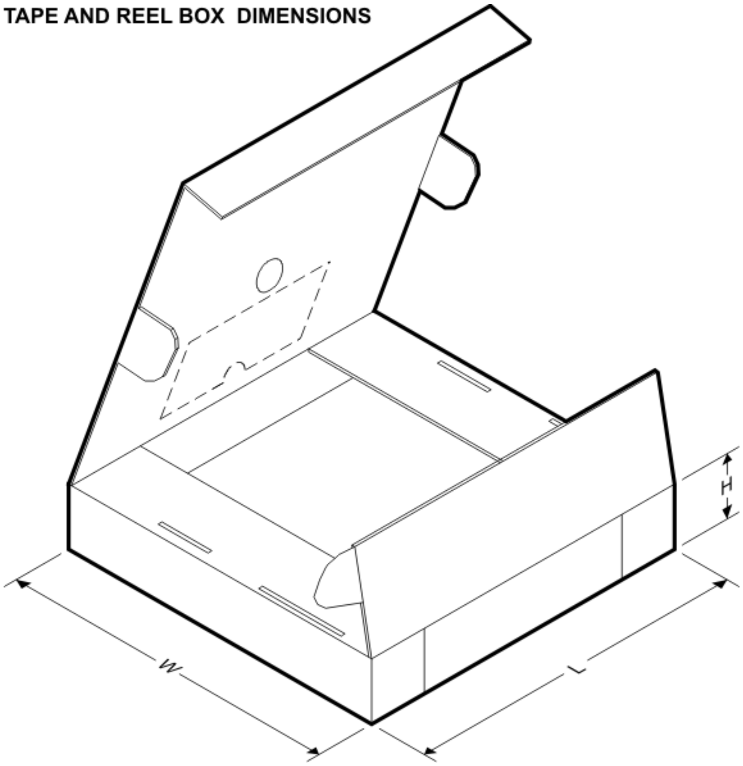
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC5652IPFBR	TQFP	PFB	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

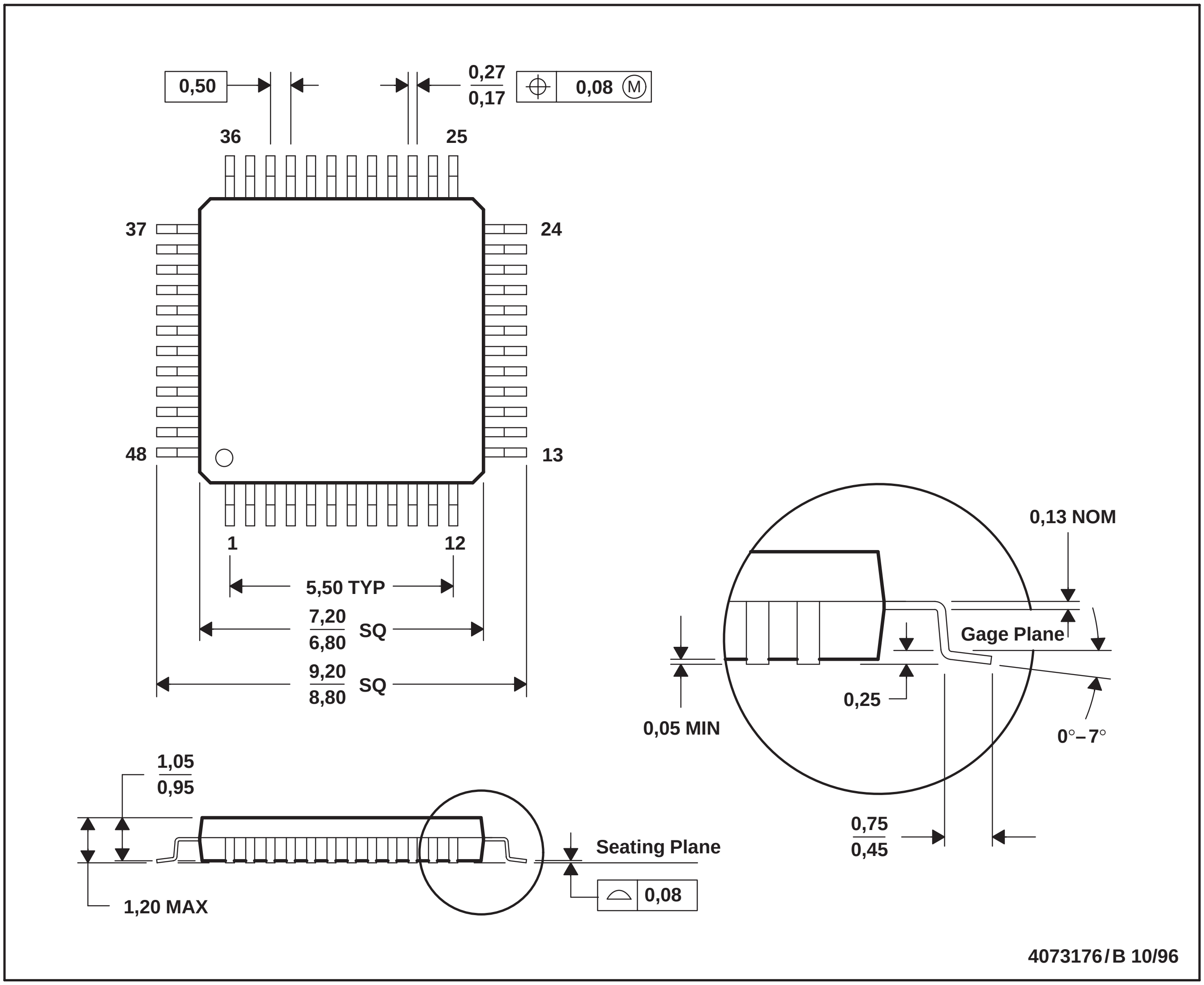
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

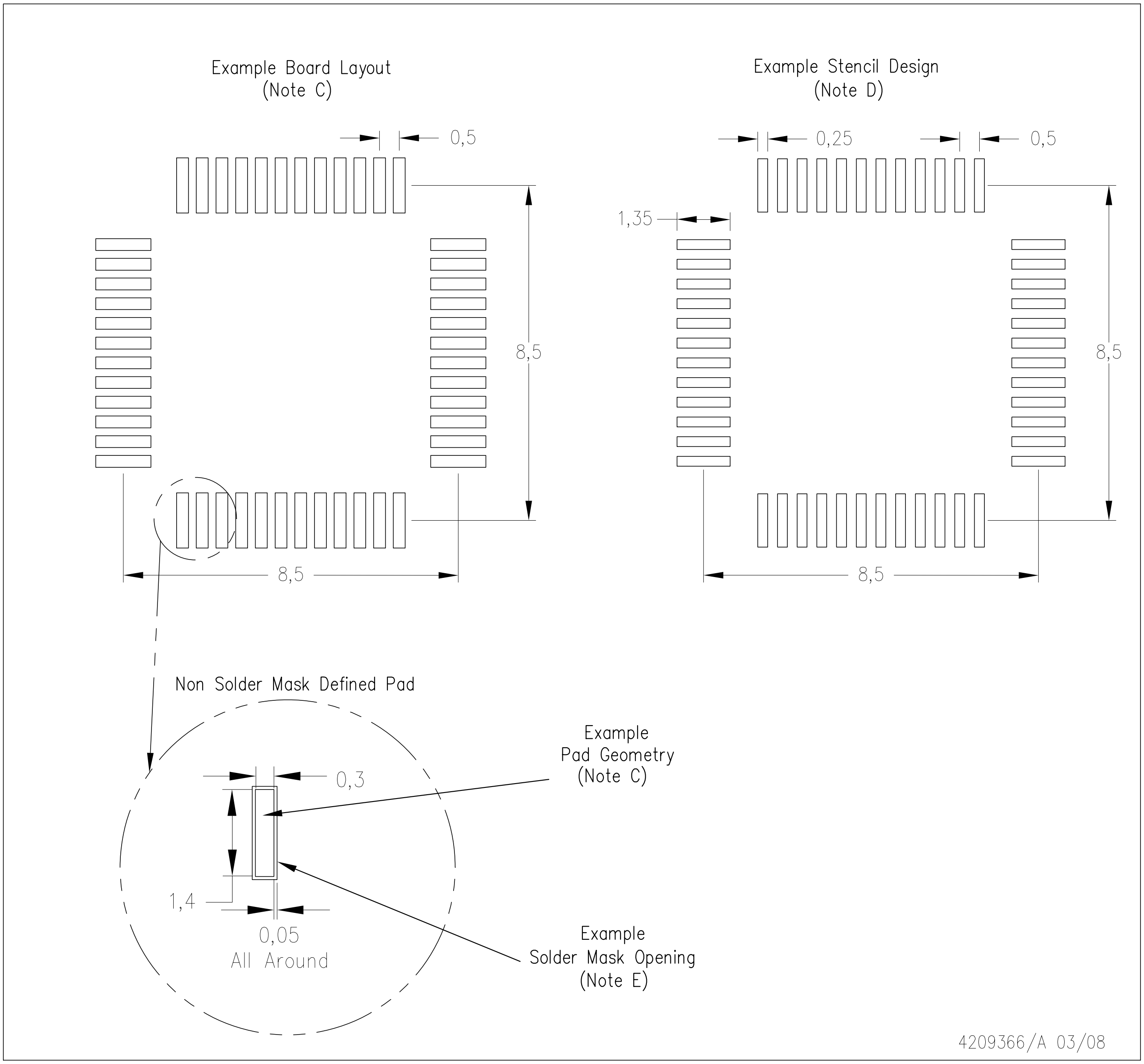
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC5652IPFBR	TQFP	PFB	48	1000	346.0	346.0	33.0

PFB (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PFB (S-PQFP-G48)



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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