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Octal, 12-Bit, Low-Power, ±15-V Output, Serial Input DIGITAL-TO-ANALOG CONVERTER

FEATURES

• Bipolar Output: ±15 V, Up to ±16.5 V

Unipolar Output: 0 V to +18 V

12-Bit Resolution

• Low Power: 20.6 mW/Ch

Relative Accuracy: 1 LSB Max

Low Zero-Code/Gain Error: ±1 LSB Max

Flexible System Calibration

Low Glitch

Settling Time: 10 μs

• Channel Monitor Output

Programmable Offset

SPI™: Up to 50-MHz, 1.8-V/3-V/5-V Logic

Schmitt Trigger Inputs

Daisy-Chain Mode

 Packages: QFN-48 (7x7mm), TQFP-64 (10x10mm)

APPLICATIONS

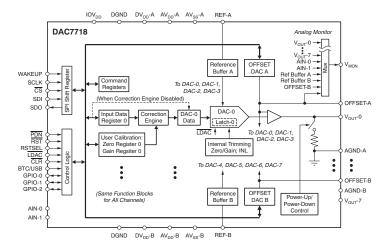
- Automatic Test Equipment
- PLC and Industrial Process Control
- Communications

DESCRIPTION

The DAC7718 is a low-power, octal, 12-bit digital-to-analog converter (DAC). The output can be a bipolar ±15-V voltage when operating from a dual ±16.5V power supply, or a unipolar 0-V to +18-V voltage when operating from a +20-V power supply. This DAC provides low-power operation, good linearity, and low glitch over the specified temperature range of -40°C to +105°C. This device is trimmed in manufacturing and has very low zero-code and gain error. In addition, system level calibration can be performed to achieve ±1 LSB zero-code and gain error over entire signal chain. The output range can be offset by properly setting the DAC offset register.

The DAC7718 features a standard, high-speed serial peripheral interface (SPI) at up to 50 MHz and 1.8-V, 3-V, and 5-V logic compatible, to communicate with a DSP or microprocessor. The input data of the device are double-buffered. An asynchronous load input ($\overline{\text{LDAC}}$) transfers data from the DAC data register to the DAC latch. The asynchronous CLR input sets the output of all eight DACs to AGND. The V_{MON} pin is a monitor output that connects to the individual analog outputs and two external inputs through a multiplexer (mux).

The DAC7718 is pin-to-pin compatible with the DAC8718 (16-bit) and the DAC8218 (14-bit).

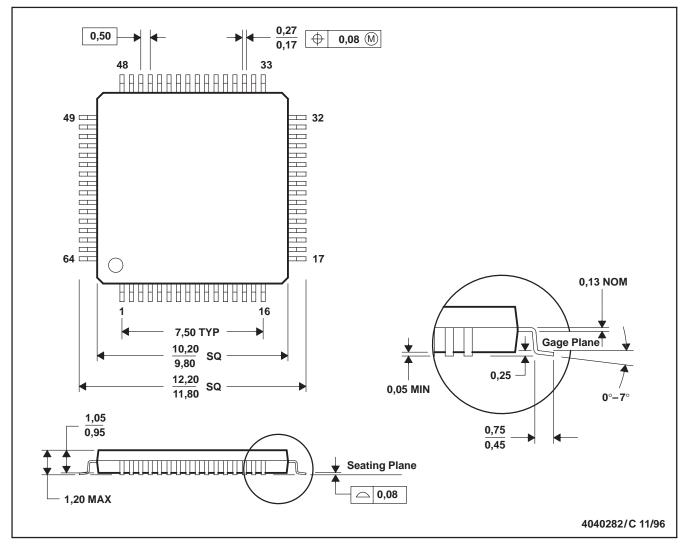


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PAG (S-PQFP-G64)

PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-026

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RGZ (S-PQFP-N48) PLASTIC QUAD FLATPACK 7,15 6,85 PIN 1 INDEX AREA TOP AND BOTTOM 1,00 0,80 → 0,20 REF. SEATING PLANE 0,08 0,05 0,00 48X $\frac{0,50}{0,30}$ 0,50 EXPOSED THERMAL PAD 37 $\frac{25}{0,18}$ $\frac{0,30}{0,18}$ $\frac{0,10}{0}$

- NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-leads (QFN) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.

 See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - E. Falls within JEDEC MO-220.



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