DS1249W
3.3V 2048kb Nonvolatile SRAM

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FEATURES

- 10 years minimum data retention in the absence of external power
- Data is automatically protected during power loss
- Unlimited write cycles
- Low-power CMOS operation
- Read and write access times as fast as 100ns
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Optional industrial (IND) temperature range of -40°C to +85°C
- JEDEC standard 32-pin DIP package

PIN ASSIGNMENT

NC	1	32	V_{CC}
A16	2	31	A15
A14	3	30	A17
A12	4	29	$\overline{WE}$
A7	5	28	A13
A6	6	27	A8
A5	7	26	A9
A4	8	25	A11
A3	9	24	$\overline{OE}$
A2	10	23	A10
A1	11	22	$\overline{CE}$
A0	12	21	DQ7
DQ0	13	20	DQ6
DQ1	14	19	DQ5
DQ2	15	18	DQ4
GND	16	17	DQ3

32-Pin Encapsulated Package
740mil Extended

PIN DESCRIPTION

A0–A17	- Address Inputs
DQ0–DQ7	- Data In/Data Out
$\overline{CE}$	- Chip Enable
$\overline{WE}$	- Write Enable
$\overline{OE}$	- Output Enable
V_{CC}	- Power (+3.3V)
GND	- Ground
NC	- No Connect

DESCRIPTION

The DS1249W 2048kb nonvolatile (NV) SRAMs are 2,097,152-bit, fully static, NV SRAMs organized as 262,144 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry that constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. There is no limit on the number of write cycles that can be executed, and no additional support circuitry is required for microprocessor interfacing.

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READ MODE

The DS1249 devices execute a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) are active (low). The unique address specified by the 18 address inputs (A_0 – A_{17}) defines which of the 262,144 bytes of data is accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later-occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than t_{ACC}.

WRITE MODE

The DS1249 executes a write cycle whenever the $\overline{WE}$ and $\overline{CE}$ signals are active (low) after address inputs are stable. The later-occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers are enabled ($\overline{CE}$ and $\overline{OE}$ active), then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA-RETENTION MODE

The DS1249W provides full functional capability for V_{CC} greater than 3.0 volts and write protects by 2.8V. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAMs constantly monitor V_{CC}. Should the supply voltage decay, the NV SRAMs automatically write protects themselves, all inputs become “don’t care,” and all outputs become high impedance. As V_{CC} falls below approximately 2.5V, a power-switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 2.5V, the power-switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 3.0V.

FRESHNESS SEAL

Each DS1249 device is shipped from Dallas Semiconductor with its lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at a level greater than V_{TP}, the lithium energy source is enabled for battery backup operation.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +4.6V
Operating Temperature Range	0°C to 70°C (-40°C to +85°C for IND parts)
Storage Temperature Range	-40°C to +70°C (-40°C to +85°C for IND parts)
Soldering Temperature	+260°C for 10 seconds
Caution: Do Not Reflow	(Wave or Hand Solder Only)

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T$_A$: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power-Supply Voltage	V_{CC}	3.0	3.3	3.6	V	
Logic 1	V_{IH}	2.2		V_{CC}	V	
Logic 0	V_{IL}	0.0		+0.4	V	

DC ELECTRICAL CHARACTERISTICS (T_A: See Note 10; V_{CC} = 3.3V ± 0.3V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-2.0		+2.0	µA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-2.0		+2.0	µA	
Output Current at 2.2V	I_{OH}	-1.0			mA	
Output Current at 0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		150	250	µA	
Standby Current $\overline{CE} = V_{CC}$ - 0.2V	I_{CCS2}		100	150	µA	
Operating Current	I_{CCO1}			50	mA	
Write Protection Voltage	V_{TP}	2.8	2.9	3.0	V	

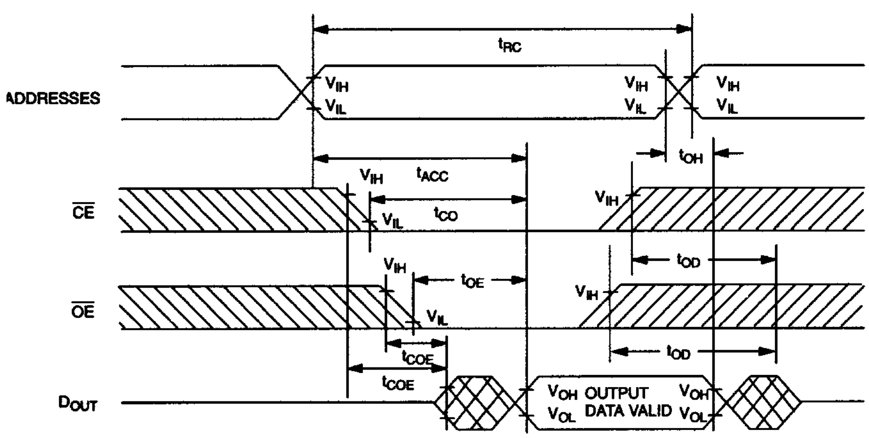
CAPACITANCE (T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		10	20	pF	
Input/Output Capacitance	$C_{I/O}$		10	20	pF	

AC ELECTRICAL CHARACTERISTICS (T_A: See Note 10; V_{CC} = 3.3V ± 0.3V)

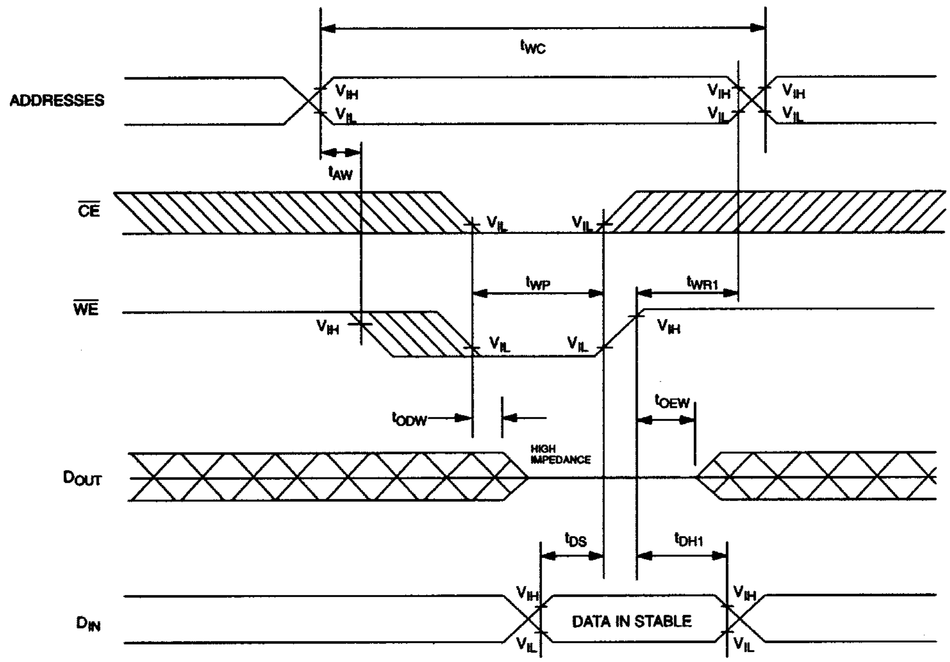
PARAMETER	SYMBOL	DS1249W-100		DS1249W-150		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	100		150		ns	
Access Time	t_{ACC}		100		150	ns	
$\overline{OE}$ to Output Valid	t_{OE}		50		70	ns	
$\overline{CE}$ to Output Valid	t_{CO}		100		150	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		ns	5
Output High-Z from Deselection	t_{OD}		35		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	100		150		ns	
Write Pulse Width	t_{WP}	75		100		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR1}	5		5		ns	12
	t_{WR2}	20		20		ns	13
Output High-Z from $\overline{WE}$	t_{ODW}		35		35	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		ns	5
Data Setup Time	t_{DS}	40		60		ns	4
Data Hold Time	t_{DH1}	0		0		ns	12
	t_{DH2}	20		20		ns	13

READ CYCLE



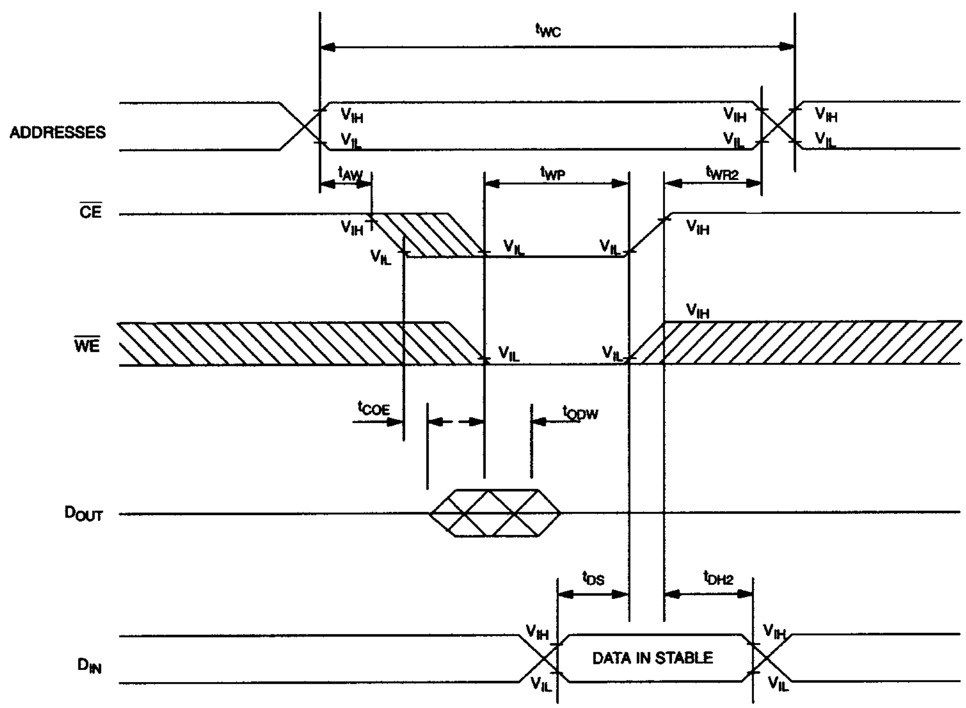
SEE NOTE 1

WRITE CYCLE 1



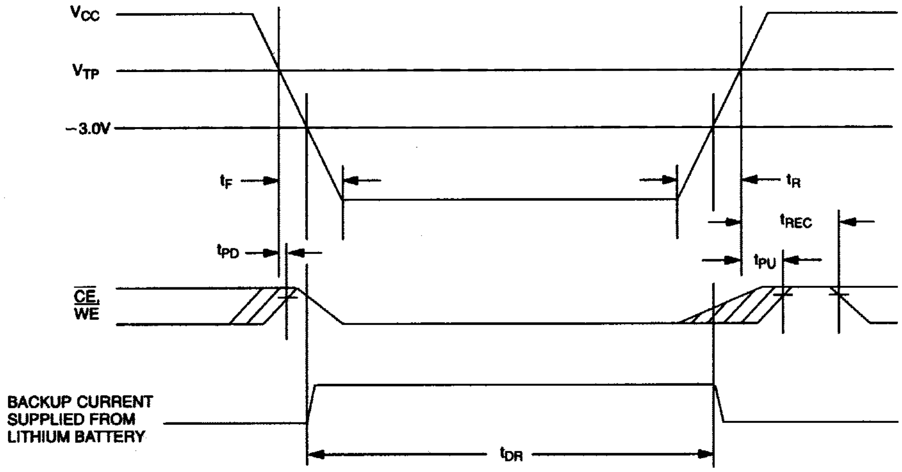
SEE NOTES 2, 3, 4, 6, 7, 8, and 12

WRITE CYCLE 2



SEE NOTES 2, 3, 4, 6, 7, 8, and 13

POWER-DOWN/POWER-UP CONDITION



SEE NOTE 11

POWER-DOWN/POWER-UP TIMING

(T_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} Fail Detect to $\overline{CE}$ and $\overline{WE}$ Inactive	t_{PD}			1.5	µs	11
V_{CC} Slew from V_{TP} to 0V	t_F	150			µs	
V_{CC} Slew from 0V to V_{TP}	t_R	150			µs	
V_{CC} Valid to $\overline{CE}$ and $\overline{WE}$ Inactive	t_{PU}			2	ms	
V_{CC} Valid to End of Write Protection	t_{REC}			125	ms	

(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data-Retention Time	t_{DR}	10			years	9

WARNING:

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DS} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter than the $\overline{WE}$ low transition in Write Cycle 1, the output buffers remain in a high-impedance state during this period.

7. If the $\overline{CE}$ high transition occurs prior to, or simultaneously with, the $\overline{WE}$ high transition, the output buffers remain in a high-impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to, or simultaneously with, the $\overline{CE}$ low transition, the output buffers remain in a high-impedance state during this period.
9. Each DS1249W has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
10. All AC and DC electrical characteristics are valid over the full operating temperature range. For commercial products, this range is 0°C to +70°C. For industrial products (IND), this range is -40°C to +85°C.
11. In a power-down condition, the voltage on any pin may not exceed the voltage on V_{CC}.
12. t_{WR1} and t_{DH1} are measured from $\overline{WE}$ going high.
13. t_{WR2} and t_{DH2} are measured from $\overline{CE}$ going high.
14. DS1249 modules are recognized by Underwriters Laboratory (U.L.®) under file E99151.

DC TEST CONDITIONS

Outputs open
Cycle = 200ns for operating current
All voltages are referenced to ground

AC TEST CONDITIONS

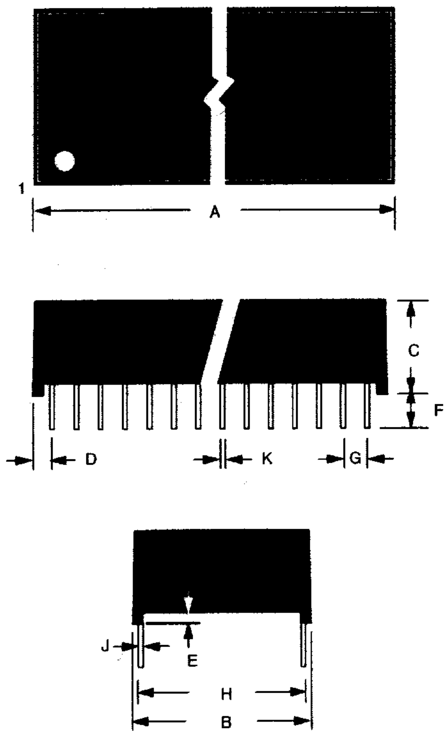
Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0 to 2.7V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

ORDERING INFORMATION

Part Number	Temperature Range	Supply Tolerance	Pin/Package	Speed Grade
DS1249W-100	0°C to +70°C	3.3V ± 0.3V	32 / 740 EMOD	100ns
DS1249W-100#	0°C to +70°C	3.3V ± 0.3V	32 / 740 EMOD	100ns
DS1249W-100IND	-40°C to +85°C	3.3V ± 0.3V	32 / 740 EMOD	100ns
DS1249W-100IND#	-40°C to +85°C	3.3V ± 0.3V	32 / 740 EMOD	100ns
DS1249W-150	0°C to +70°C	3.3V ± 0.3V	32 / 740 EMOD	150ns
DS1249W-150#	0°C to +70°C	3.3V ± 0.3V	32 / 740 EMOD	150ns

 # Denotes RoHS-compliant product.
** DS9034PC or DS9034PCI (PowerCap) required. Must be ordered separately.*

DS1249W NONVOLATILE SRAM, 32-PIN, 740MIL EXTENDED MODULE



PKG	32-PIN	
DIM	MIN	MAX
A IN. MM	2.080 52.83	2.100 53.34
B IN. MM	0.715 18.16	0.740 18.80
C IN. MM	0.395 10.03	0.405 10.29
D IN. MM	0.280 7.11	0.310 7.49
E IN. MM	0.015 0.38	0.030 0.76
F IN. MM	0.120 3.05	0.160 4.06
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.590 14.99	0.630 16.00
J IN. MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.43	0.025 0.58