2Gb NAND FLASH
HY27UG162G5A

Document Title
2Gbit (128Mx16bit) NAND Flash Memory

Revision History

Revision No.	History	Draft Date	Remark
0.1	Initial Draft.	Sep. 15. 2006	Preliminary

FEATURES SUMMARY

HIGH DENSITY NAND FLASH MEMORIES

- Cost effective solutions for mass storage applications

NAND INTERFACE

- x16 bus width.
- Multiplexed Address/ Data
- Pinout compatibility for all densities

SUPPLY VOLTAGE

- VCC = 2.7 to 3.6V : HY27UG162G5A

Memory Cell Array

= (1K+32) Bytes x 64 Pages x 2,048 Blocks

PAGE SIZE

- x16 device : (1K+32 spare) Bytes
  : HY27UF161G5A

BLOCK SIZE

- x16 device: (64K + 2K spare) Words

PAGE READ / PROGRAM

- Random access: 25us (max.)
- Sequential access: 30ns (min.)
- Page program time: 200us (typ.)

COPY BACK PROGRAM MODE

- Fast page copy without external buffering

CACHE PROGRAM

- Internal (2048+64) Byte buffer to improve the program throughput

FAST BLOCK ERASE

- Block erase time: 2ms (Typ.)

STATUS REGISTER

ELECTRONIC SIGNATURE

- 1st cycle: Manufacturer Code
- 2nd cycle: Device Code
- 3rd cycle: Internal chip number, Cell Type, Number of Simultaneously Programmed Pages.
- 4th cycle: Page size, Block size, Organization, Spare size

SERIAL NUMBER OPTION

CHIP ENABLE DON'T CARE

- Simple interface sith microcontroller

DATA RETENTION

- 100,000 Program/Erase cycles (with 1bit/528byte ECC)
- 10 years Data Retention

PACKAGE

- HY27UG162G5A-F(P)
  : 63-ball FBGA (9 x 11 x 0.86 mm)
  - HY27UG162G5A-F (Lead)
  - HY27UG162G5A-FP (Lead Free)

1. SUMMARY DESCRIPTION

The Hynix HY27UG162G5A series is a 128Mx16bit with spare 4Mx8 bit capacity. The device is offered in 3.3V Vcc Power Supply.
Its NAND cell provides the most cost-effective solution for the solid state mass storage market. The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased.
The device contains 2048 blocks, composed by 64 pages consisting in two NAND structures of 32 series connected Flash cells.
A program operation allows to write the 2112-byte page in typical 200us and an erase operation can be performed in typical 2ms on a 128K-byte block.
Data in the page can be read out at 30ns cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command input. This interface allows a reduced pin count and easy migration towards different densities, without any rearrangement of footprint.
Commands, Data and Addresses are synchronously introduced using $\overline{CE}$, $\overline{WE}$, ALE and CLE input pin. The on-chip Program/Erase Controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data.
The modify operations can be locked using the $\overline{WP}$ input pin or using the extended lock block feature described later.
The output pin R/$\overline{B}$ (open drain buffer) signals the status of the device during each operation. In a system with multiple memories the R/B pins can be connected all together to provide a global status signal.
Even the write-intensive systems can take advantage of the HY27UG162G2A extended reliability of 100K program/erase cycles by providing ECC (Error Correcting Code) with real time mapping-out algorithm.

The chip could be offered with the $\overline{CE}$ don't care function. This function allows the direct download of the code from the NAND Flash memory device by a microcontroller, since the $\overline{CE}$ transitions do not stop the read operation.

The copy back function allows the optimization of defective blocks management: when a page program operation fails the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase.
The cache program feature allows the data insertion in the cache register while the data register is copied into the flash array. This pipelined program operation improves the program throughput when long files are written inside the memory. A cache read feature is also implemented. This feature allows to dramatically improve the read throughput when consecutive pages have to be streamed out.

The HYNIX HY27UG162G5A series is available in FBGA 9 x 11 mm.

1.1 Product List

PART NUMBER	ORIZATION	VCC RANGE	PACKAGE
HY27UG162G5A	x16	2.7V - 3.6 Volt	63FBGA

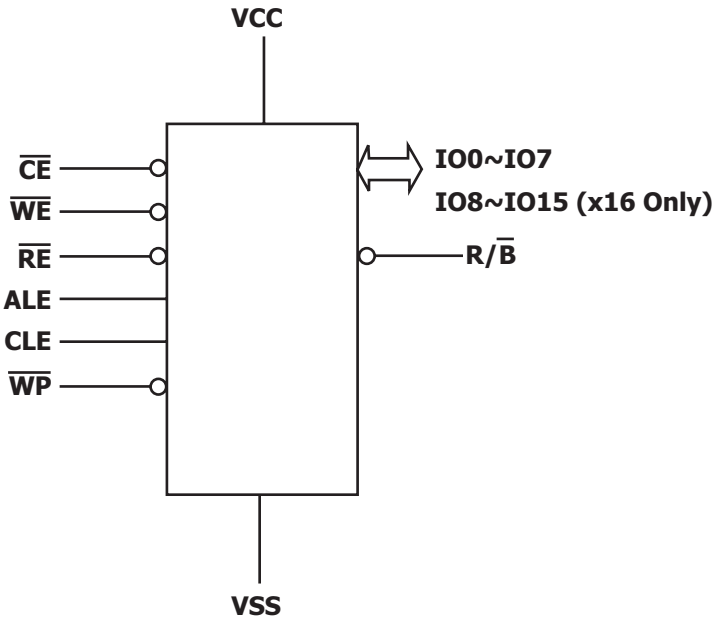


Figure1: Logic Diagram

IO15 - IO8	Data Input / Outputs (x16 only)
IO7 - IO0	Data Inputs / Outputs
CLE	Command latch enable
ALE	Address latch enable
$\overline{CE}$	Chip Enable
$\overline{RE}$	Read Enable
$\overline{WE}$	Write Enable
$\overline{WP}$	Write Protect
R/$\overline{B}$	Ready / Busy
Vcc	Power Supply
Vss	Ground
NC	No Connection

Table 1: Signal Names

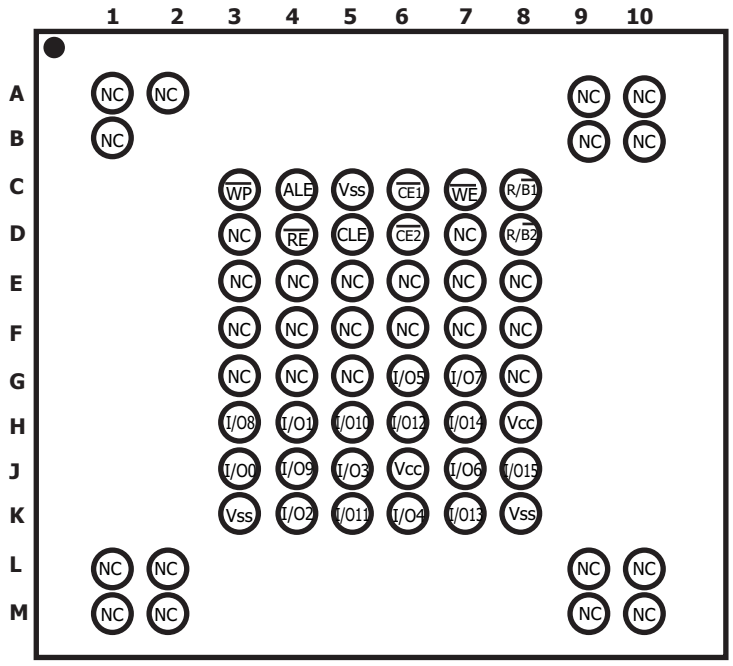


Figure 2. 63FBGA Contactions, x16 Device (Top view through package)

1.2 PIN DESCRIPTION

Pin Name	Description
IO0-IO7 IO8-IO15(1)	**DATA INPUTS/OUTPUTS** The IO pins allow to input command, address and data and to output data during read / program operations. The inputs are latched on the rising edge of Write Enable ($\overline{WE}$). The I/O buffer float to High-Z when the device is deselected or the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** This input activates the latching of the IO inputs inside the Command Register on the Rising edge of Write Enable ($\overline{WE}$).
ALE	**ADDRESS LATCH ENABLE** This input activates the latching of the IO inputs inside the Address Register on the Rising edge of Write Enable ($\overline{WE}$).
$\overline{CE}$1, $\overline{CE}$2	**CHIP ENABLE** This input controls the selection of the device. When the device is busy $\overline{CE}$1, $\overline{CE}$2 low does not deselect the memory.
$\overline{WE}$	**WRITE ENABLE** This input acts as clock to latch Command, Address and Data. The IO inputs are latched on the rise edge of $\overline{WE}$.
$\overline{RE}$	**READ ENABLE** The $\overline{RE}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of $\overline{RE}$ which also increments the internal column address counter by one.
$\overline{WP}$	**WRITE PROTECT** The $\overline{WP}$ pin, when Low, provides an Hardware protection against undesired modify (program / erase) operations.
R/$\overline{B}$1, R/$\overline{B}$2	**READY BUSY** The Ready/Busy output is an Open Drain pin that signals the state of the memory.
VCC	**SUPPLY VOLTAGE** The VCC supplies the power for all the operations (Read, Write, Erase).
VSS	GROUND
NC	NO CONNECTION

Table 2: Pin Description

NOTE:

1. A 0.1uF capacitor should be connected between the Vcc Supply Voltage pin and the Vss Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.

	IO0	IO1	IO2	IO3	IO4	IO5	IO6	IO7	IO8-IO15
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7	L(1)
2nd Cycle	A8	A9	A10	L(1)	L(1)	L(1)	L(1)	L(1)	L(1)
3rd Cycle	A11	A12	A13	A14	A15	A16	A17	A18	L(1)
4th Cycle	A19	A20	A21	A22	A23	A24	A25	A26	L(1)

Table 3: Address Cycle Map(x16)

NOTE:
1. L must be set to Low.

FUNCTION	1st CYCLE	2nd CYCLE	3rd CYCLE	4th CYCLE	Acceptable command during busy
READ 1	00h	30h	-	-	
READ FOR COPY-BACK	00h	35h	-	-	
READ ID	90h	-	-	-	
RESET	FFh	-	-	-	Yes
PAGE PROGRAM	80h	10h	-	-	
COPY BACK PGM	85h	10h	-	-	
BLOCK ERASE	60h	D0h	-	-	
READ STATUS REGISTER	70h	-	-	-	Yes
CACHE PROGRAM	80h	15h	-	-	
RANDOM DATA INPUT	85h	-	-	-	
RAMDOM DATA OUTPUT	05h	E0h	-	-	
CACHE READ START	00h	31h	-	-	
CACHE READ EXIT	34h	-	-	-	

Table 4: Command Set

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	MODE	
H	L	L	Rising	H	X	Read Mode	Command Input
L	H	L	Rising	H	X		Address Input(4 cycles)
H	L	L	Rising	H	H	Write Mode	Command Input
L	H	L	Rising	H	H		Address Input(4 cycles)
L	L	L	Rising	H	H	Data Input	
L	L	L(1)	H	Falling	X	Sequential Read and Data Output	
L	L	L	H	H	X	During Read (Busy)	
X	X	X	X	X	H	During Program (Busy)	
X	X	X	X	X	H	During Erase (Busy)	
X	X	X	X	X	L	Write Protect	
X	X	H	X	X	0V/Vcc	Stand By	

Table 5: Mode Selection

NOTE:

1. With the $\overline{CE}$ high during latency time does not stop the read operation

2. BUS OPERATION

There are six standard bus operations that control the device. These are Command Input, Address Input, Data Input, Data Output, Write Protect, and Standby.
Typically glitches less than 5 ns on Chip Enable, Write Enable and Read Enable are ignored by the memory and do not affect bus operations.

2.1 Command Input.

Command Input bus operation is used to give a command to the memory device. Command are accepted with Chip Enable low, Command Latch Enable High, Address Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/erase) the Write Protect pin must be high. See figure 4 and table 12 for details of the timings requirements. Command codes are always applied on IO7:0, disregarding the bus configuration (X16).

2.2 Address Input.

Address Input bus operation allows the insertion of the memory address. To insert the 27 addresses needed to access the 2Gbit 4 clock cycles (x8 version) are needed. Addresses are accepted with Chip Enable low, Address Latch Enable High, Command Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/erase) the Write Protect pin must be high. See figure 5 and table 12 for details of the timings requirements. Addresses are always applied on IO7:0, disregarding the bus configuration (X8/X16).

2.3 Data Input.

Data Input bus operation allows to feed to the device the data to be programmed. The data insertion is serially and timed by the Write Enable cycles. Data are accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low, Read Enable High, and Write Protect High and latched on the rising edge of Write Enable. See figure 6 and table 12 for details of the timings requirements.

2.4 Data Output.

Data Output bus operation allows to read data from the memory array and to check the status register content, the lock status and the ID data. Data can be serially shifted out toggling the Read Enable pin with Chip Enable low, Write Enable High, Address Latch Enable low, and Command Latch Enable low. See figures 7 - 11 and table 12 for details of the timings requirements.

2.5 Write Protect.

Hardware Write Protection is activated when the Write Protect pin is low. In this condition modify operation do not start and the content of the memory is not altered. Write Protect pin is not latched by Write Enable to ensure the protection even during the power up.

2.6 Standby.

In Standby mode the device is deselected, outputs are disabled and Power Consumption is reduced.

3. DEVICE OPERATION

3.1 Page Read.

Upon initial device power up, the device defaults to Read mode. This operation is also initiated by writing 00h and 30h to the command register along with four address cycles. In two consecutive read operations, the second one does need 00h command, which four address cycles and 30h command initiates that operation. Second read operation always requires setup command if first read operation was executed using also random data out command.

Two types of operations are available: random read. The random read mode is enabled when the page address is changed. The 1056 words (X16 device) of data within the selected page are transferred to the data registers in less than 25us(tR). The system controller may detect the completion of this data transfer (tR) by analyzing the output of R/$\overline{B}$ pin. Once the data in a page is loaded into the data registers, they may be read out in 30ns cycle time (3.3V device) by sequentially pulsing $\overline{RE}$. The repetitive high to low transitions of the $\overline{RE}$ clock make the device output the data starting from the selected column address up to the last column address.

The device may output random data in a page instead of the consecutive sequential data by writing random data output command. The column address of next data, which is going to be out, may be changed to the address which follows random data output command.

Random data output can be operated multiple times regardless of how many times it is done in a page.

Random data output is not available in cache read.

3.2 Page Program.

The device is programmed basically by page, but it does allow multiple partial page programming of a word or consecutive words up to 1056 (X16 device), in a single page program cycle.

The number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed 8; for example, 4 times for main array (X16 device:1time 256word) and 4 times for spare array (X16 device:1time/8word).

The addressing should be done in sequential order in a block. A page program cycle consists of a serial data loading period in which up to 1056 words (X16 device) of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell.

The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the four cycle address inputs and then serial data. The words other than those to be programmed do not need to be loaded. The device supports random data input in a page. The column address of next data, which will be entered, may be changed to the address which follows random data input command (85h). Random data input may be operated multiple times regardless of how many times it is done in a page.

The Page Program confirm command (10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The P/E/R controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit (I/O 0) may be checked. The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register. Figure 12 details the sequence.

3.3 Block Erase.

The Erase operation is done on a block basis. Block address loading is accomplished in two cycles initiated by an Erase Setup command (60h). Only address A17 to A26 (X16) is valid while A11 to A16 (X16) are ignored. The Erase Confirm command (D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions. At the rising edge of $\overline{WE}$ after the erase confirm command input, the P/E/R controller handles erase and erase-verify.

Once the erase process starts, the Read Status Register command may be entered to read the status register.

The system controller can detect the completion of an erase by monitoring the R/$\overline{B}$ output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while erasing is in progress. When the erase operation is completed, the Write Status Bit (I/O 0) may be checked.

Figure 16 details the sequence.

3.4 Copy-Back Program.

The copy-back program is configured to quickly and efficiently rewrite data stored in one page without utilizing an external memory. Since the time-consuming cycles of serial access and re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block also need to be copied to the newly assigned free block. The operation for performing a copy-back program is a sequential execution of page-read without serial access and copyingprogram with the address of destination page. A read operation with "35h" command and the address of the source page moves the whole 2112byte (X8 device) or 1056word (X16 device) data into the internal data buffer.

As soon as the device returns to Ready state, Copy Back command (85h) with the address cycles of destination page may be written. The Program Confirm command (10h) is required to actually begin the programming operation. Data input cycle for modifying a portion or multiple distant portions of the source page is allowed as shown in Figure 15.

"When there is a program-failure at Copy-Back operation, error is reported by pass/fail status. But, if Copy-Back operations are accumulated over time, bit error due to charge loss is not checked by external error detection/correction scheme. For this reason, two bit error correction is recommended for the use of Copy-Back operation."

Figure 14 shows the command sequence for the copy-back operation.

The Copy Back Program operation requires three steps:

1. The source page must be read using the Read A command (one bus write cycle to setup the command and then 4 bus write cycles to input the source page address). This operation copies all 2KBytes from the page into the Page Buffer.
2. When the device returns to the ready state (Ready/Busy High), the second bus write cycle of the command is given with the 4bus cycles to input the target page address. The value for A26 from second to the last page address must be same as the value given to A26 in first address.
3. Then the confirm command is issued to start the P/E/R Controller.

3.5 Read Status Register.

The device contains a Status Register which may be read to find out whether read, program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/$\overline{B}$ pins are common-wired. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status. Refer to Table 13 for specific Status Register definitions, and Figure 9 for specific timings requirements . The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command (00h) should be given before starting read cycles.

3.6 Read ID.

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Four read cycles sequentially output the 1st cycle (ADh), and 2nd cycle (the device code) and 3rd cycle ID, 4th cycle ID, respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 17 shows the operation sequence, while Tables 14, 15 explain the byte meaning.

3.7 Reset.

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased.

The command register is cleared to wait for the next command, and the Status Register is cleared to value E0h when $\overline{WP}$ is high. Refer to table 14 for device status after reset operation. If the device is already in reset state a new reset command will not be accepted by the command register. The R/$\overline{B}$ pin transitions to low for tRST after the Reset command is written.

3.8 Cache program

Cache Program is an extension of Page Program, which is executed with 1056word (X16 device) data registers, and is available only within a block. Since the device has 1 page of cache memory, serial data input may be executed while data stored in data register are programmed into memory cell. After writing the first set of data up to 1056word (X16 device) into the selected cache registers, Cache Program command (15h) instead of actual Page Program (10h) is input to make cache registers free and to start internal program operation. To transfer data from cache registers to data registers, the device remains in Busy state for a short period of time (tCBSY) and has its cache registers ready for the next data-input while the internal programming gets started with the data loaded into data registers. Read Status command (70h) may be issued to find out when cache registers become ready by polling the Cache- Busy status bit (I/O 6). Pass/fail status of only the previous page is available upon the return to Ready state.

When the next set of data is input with the Cache Program command, tCBSY is affected by the progress of pending internal programming. The programming of the cache registers is initiated only when the pending program cycle is finished and the data registers are available for the transfer of data from cache registers. The status bit (I/O5) for internal Ready/Busy may be polled to identify the completion of internal programming.

If the system monitors the progress of programming only with R/$\overline{B}$, the last page of the target programming sequence must be programmed with actual Page Program command (10h). If the Cache Program command (15h) is used instead, status bit (I/O5) must be polled to find out when the last programming is actually finished before starting other operations such as read. Pass/fail status is available in two steps. I/O 1 returns with the status of the previous page upon Ready or I/O6 status bit changing to "1", and later I/O 0 with the status of current page upon true Ready (returning from internal programming) or I/O 5 status bit changing to "1". I/O 1 may be read together when I/O 0 is checked. See Fig. 15 for more details.

NOTE : Since programming the last page does not employ caching, the program time has to be that of Page Program. However, if the previous program cycle with the cache data has not finished, the actual program cycle of the last page is initiated only after completion of the previous cycle, which can be expressed as the following formula.

tPROG=Program time for the last page + Program time for the (last-1)page
- (Program command cycle time + Last page data loading time)

3.9 Cache Read

Cache read operation allows automatic download of consecutive pages, up to the whole device. Immediately after 1st latency end, while user can start reading out data, device internally starts reading following page.
Start address of 1st page must be at page start (A<10:0>=00h) : in this way after 1st latency time (tr) , automatic data download will be uninterrupted. In fact latency time is 25us, while download of a page require at least 50us for x16 device.
Cache read operation command is like standard read, except for confirm code (30h for standard read, 31h for cache read) user can check operation status using :

- R/$\overline{B}$ ('0' means latency ongoing, download not possible, '1' means download of n page possible, even if device in ternally is active on n+1 page
- Status register (SR<6> behave like R/$\overline{B}$, SR<5> is '0' when device is internally reading and '1' when device is idle)

To exit cache read operation, a cache read exit command (34h) must be issued. This command can be given any time (both device idle and reading).

If device is active (SR<5>=0) it will go idle within 5us, while if it is not active, device itself will go busy for a time shorter then tCBSY before becoming again idle and ready to accept any further commands. Figure 16 describes how to handle Cache Read through Status register .
If user reads last byte/word of the memory array, then he has to stop by giving a cache read exit command. In general, if user wants to terminate a cache read, then he must give a cache read exit command (or reset command) before starting any new operation.
Random data output is not available in cache read.

Cache read operation must be done only block by block if system needs to avoid reading also from invalid blocks.

4. OTHER FEATURES

4.1 Data Protection for Power on/off Sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 2.0V (3.3V version). $\overline{WP}$ pin provides hardware protection and is recommended to be kept at VIL during power-up and power-down. A recovery time of minimum 10us is required before internal circuit gets ready for any command sequences as shown in Figure 22. The two-step command sequence for program/erase provides additional software protection.
If the power is dropped during the ready read/write/erase operation, Power protection function may not guaranteed the data. Power protection function is only available during the power on/off sequence.

4.2 Ready/Busy.

The device has a Ready/Busy output that provides method of indicating the completion of a page program, erase, copy-back, cache program and random read completion. The R/$\overline{B}$ pin is normally high and goes to low when the device is busy (after a reset, read, program, erase operation). It returns to high when the P/E/R controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{B}$ outputs to be Or-tied. Because pull-up resistor value is related to tr(R/$\overline{B}$) and current drain during busy (Ibusy), an appropriate value can be obtained with the following reference chart (Figure 23). Its value can be determined by the following guidance.

Parameter	Symbol	Min	Typ	Max	Unit
Valid Block Number	N_{VB}	2008		2048	Blocks

Table 6: Valid Blocks Number

NOTE:

1. The 1st block is guaranteed to be a valid block up to 1K cycles with ECC. (1bit/528bytes)

Symbol	Parameter	Value	Unit
		3.3V	
T_A	Ambient Operating Temperature (Temperature Range Option 1)	0 to 70	℃
	Ambient Operating Temperature (Industrial Temperature Range)	-40 to 85	℃
T_{BIAS}	Temperature Under Bias	-50 to 125	℃
T_{STG}	Storage Temperature	-65 to 150	℃
V_{IO}(2)	Input or Output Voltage	-0.6 to 4.6	V
Vcc	Supply Voltage	-0.6 to 4.6	V

Table 7: Absolute maximum ratings

NOTE:

1. Except for the rating “Operating Temperature Range”, stresses above those listed in the Table “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

2. Minimum Voltage may undershoot to -2V during transition and for less than 20ns during transitions.

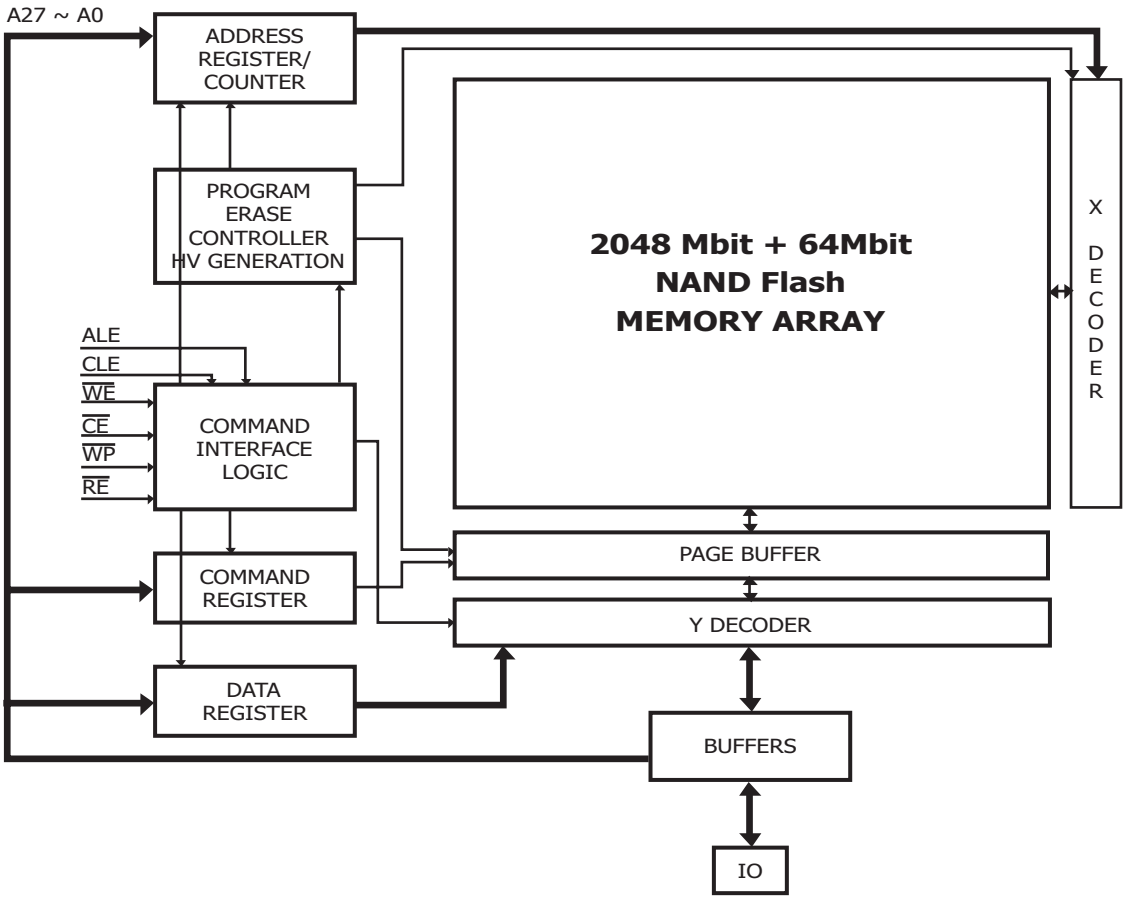


Figure 3: Block Diagram

Parameter		Symbol	Test Conditions	3.3Volt			Unit
				Min	Typ	Max	
Operating Current	Sequential Read	I_{CC1}	t_{RC}=30ns, $\overline{CE}$=V_{IL}, I_{OUT}=0mA	-	15	30	mA
	Program	I_{CC2}	-	-	15	30	mA
	Erase	I_{CC3}	-	-	15	30	mA
Stand-by Current (TTL)		I_{CC4}	$\overline{CE}$=V_{IH}, $\overline{WP}$=0V/Vcc	-		1	mA
Stand-by Current (CMOS)		I_{CC5}	$\overline{CE}$=Vcc-0.2, $\overline{WP}$=0V/Vcc	-	20	100	uA
Input Leakage Current		I_{LI}	V_{IN}=0 to Vcc (max)	-	-	± 20	uA
Output Leakage Current		I_{LO}	V_{OUT} =0 to Vcc (max)	-	-	± 20	uA
Input High Voltage		V_{IH}	-	Vccx0.8	-	Vcc+0.3	V
Input Low Voltage		V_{IL}	-	-0.3	-	Vccx0.2	V
Output High Voltage Level		V_{OH}	I_{OH}=-400uA	2.4	-	-	V
Output Low Voltage Leve		V_{OL}	I_{OL}=2.1mA	-	-	0.4	V
Output Low Current (R/$\overline{B}$)		I_{OL} (R/$\overline{B}$)	V_{OL}=0.4V	8	10	-	mA

Table 8: DC and Operating Characteristics

Parameter	Value
	3.3Volt
Input Pulse Levels	0V to Vcc
Input Rise and Fall Times	5ns
Input and Output Timing Levels	Vcc / 2
Output Load (2.7V - 3.6V)	1 TTL GATE and CL=50pF

Table 9: AC Conditions

Item	Symbol	Test Condition	Min	Max	Unit
Input / Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	20	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	20	pF

Table 10: Pin Capacitance (TA=25C, F=1.0MHz)

Parameter		Symbol	Min	Typ	Max	Unit
Program Time		t_{PROG}	-	200	700	us
Dummy Busy Time for Cache Program		t_{CBSY}	-	3	700	us
Number of partial Program Cycles in the same page	Main Array	NOP	-	-	4	Cycles
	Spare Array	NOP	-	-	4	Cycles
Block Erase Time		t_{BERS}	-	2	3	ms

Table 11: Program / Erase Characteristics

Parameter	Symbol	3.3Volt		Unit
		Min	Max	
CLE Setup time	tCLS	15		ns
CLE Hold time	tCLH	5		ns
$\overline{CE}$ setup time	tCS	20		ns
$\overline{CE}$ hold time	tCH	5		ns
$\overline{WE}$ pulse width	tWP	15		ns
ALE setup time	tALS	15		ns
ALE hold time	tALH	5		ns
Address to Data Loading	tADL(4)	100		ns
Data setup time	tDS	5		ns
Data hold time	tDH	5		ns
Write Cycle time	tWC	30		ns
$\overline{WE}$ High hold time	tWH	10		ns
Data Transfer from Cell to register	tR		25	us
ALE to $\overline{RE}$ Delay	tAR	15		ns
CLE to $\overline{RE}$ Delay	tCLR	15		ns
Ready to $\overline{RE}$ Low	tRR	20		ns
$\overline{RE}$ Pulse Width	tRP	15		ns
$\overline{WE}$ High to Busy	tWB		100	ns
Read Cycle Time	tRC	30		ns
$\overline{RE}$ Access Time	tREA		20	ns
$\overline{RE}$ High to Output High Z	tRHZ		50	ns
$\overline{CE}$ High to Output High Z	tCHZ		50	ns
$\overline{RE}$ High Hold Time	tREH	10		ns
Output High Z to $\overline{RE}$ low	tIR	0		ns
$\overline{CE}$ Access Time	tCEA		25	ns
$\overline{WE}$ High to $\overline{RE}$ low	tWHR	60		ns
$\overline{RE}$ or $\overline{CE}$ High to Output Hold	tOH	10		ns
Device Resetting Time (Read / Program / Erase)	tRST		5/10/500(1)	us
Write Protection time	tWW(3)	100		ns

Table 12: AC Timing Characteristics

NOTE:

1. If Reset Command (FFh) is written at Ready state, the device goes into Busy for maximum 5us
2. The time to Ready depends on the value of the pull-up resistor tied R/$\overline{B}$ pin.ting time.
3. Program / Erase Enable Operation : $\overline{WP}$ high to $\overline{WE}$ High.
   Program / Erase Disable Operation : $\overline{WP}$ Low to $\overline{WE}$ High.
4. tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising of first data cycle.

IO	Pagae Program	Block Erase	Cache Program	Read	Cache Read	CODING
0	Pass / Fail	Pass / Fail	Pass / Fail (N)	NA		Pass: '0' Fail: '1'
1	NA	NA	Pass / Fail (N-1)	NA		Don't care
2	NA	NA	NA	NA		-
3	NA	NA	NA	NA		-
4	NA	NA	NA	NA		-
5	Ready/Busy	Ready/Busy	P/E/R Controller Bit	Ready/Busy	P/E/R Controller Bit	Active: '0' Idle: '1'
6	Ready/Busy	Ready/Busy	Cache Register Free	Ready/Busy	Ready/Busy	Busy: '0' Ready': '1'
7	Write Protect	Write Protect	Write Protect	Write Protect		Protected: '0' Not Protected: '1'

Table 13: Status Register Coding

DEVIIDENTIFIER CYCLE	DESCRIPTION
1st	Manufacturer Code
2nd	Device Identifier
3rd	Internal chip number, cell Type, Number of Simultaneously Programmed pages.
4th	Page size, spare size, Block size, Organization

Table 14: Device Identifier Coding

Part Number	Voltage	Bus Width	1st cycle (Manufacture Code)	2nd cycle (Device Code)	3rd Code	4th Code
HY27UG162G5A	3.3V	x16	ADh	C1h	80h	5Dh

Table 15: Read ID Data Table

	Description	IO7	IO6	IO5 IO4	IO3 IO2	IO1 IO0
Die / Package	1 2 4 Reserved					0 0 0 1 1 0 1 1
String Type	Single Level 2x Multi-level Reserved Reservedl				0 0 0 1 1 0 1 1	
Number of Simultaneously Programmed Pages	1 2 3 4			0 0 0 1 1 0 1 1		
Interleave Program Between different dice	Not Support Support		0 1			
Write Cache	Not Support Support	0 1				

Table 16: 3rd Byte of Device Idendifier Description

	Description	IO7	IO6	IO5-4	IO3	IO2	IO1-0
Page Size (Without Spare Area)	1KB 2KB 4KB Reserved						0 0 0 1 1 0 1 1
Spare Area Size (Byte / 512 Byte)	8 16					0 1	
Serial Access Time	50ns 30ns 25ns Reserved	0 0 1 1			0 1 0 1		
Block Size (Without Spare Area)	64KB 128KB 256KB 512KB			0 0 0 1 1 0 1 1			
Organization	X8 X16		0 1				

Table 17: 4th Byte of Device Identifier Description

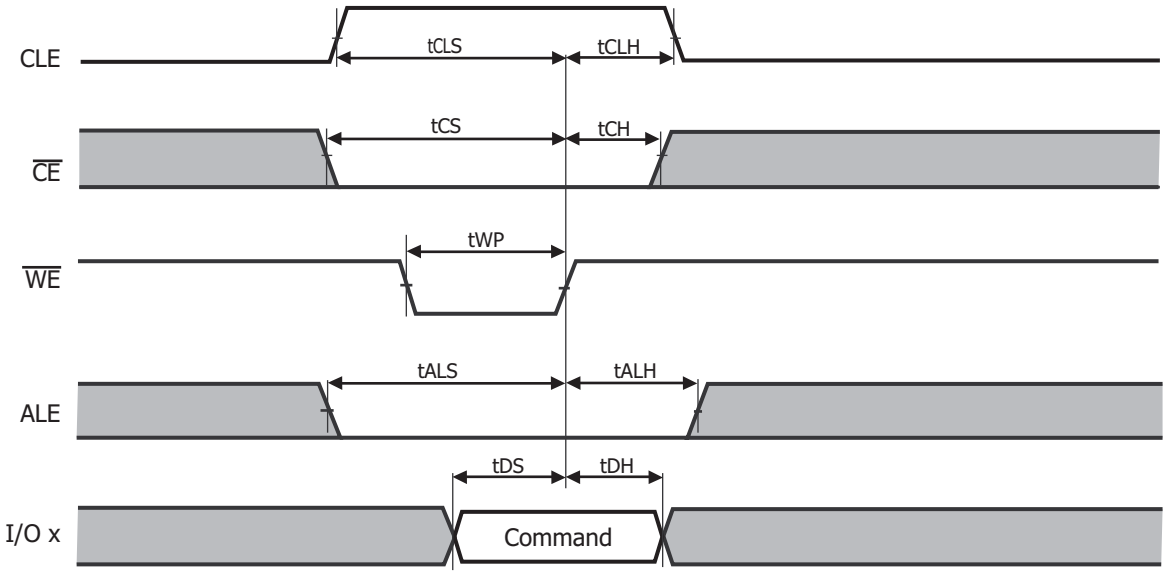


Figure 4: Command Latch Cycle

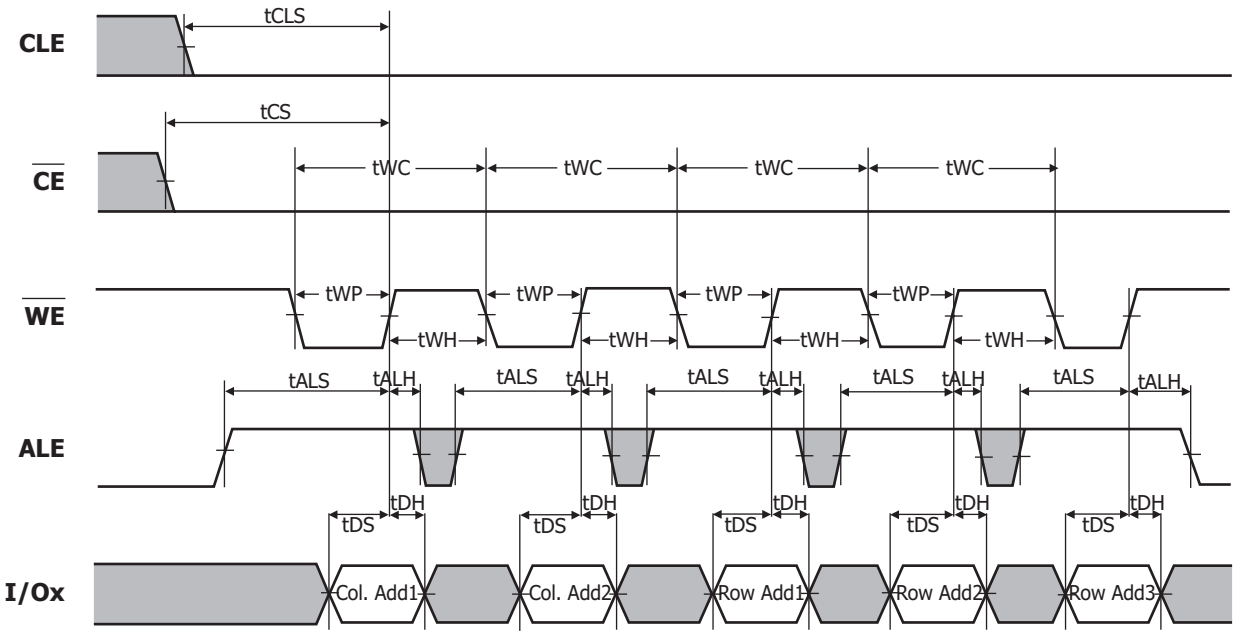
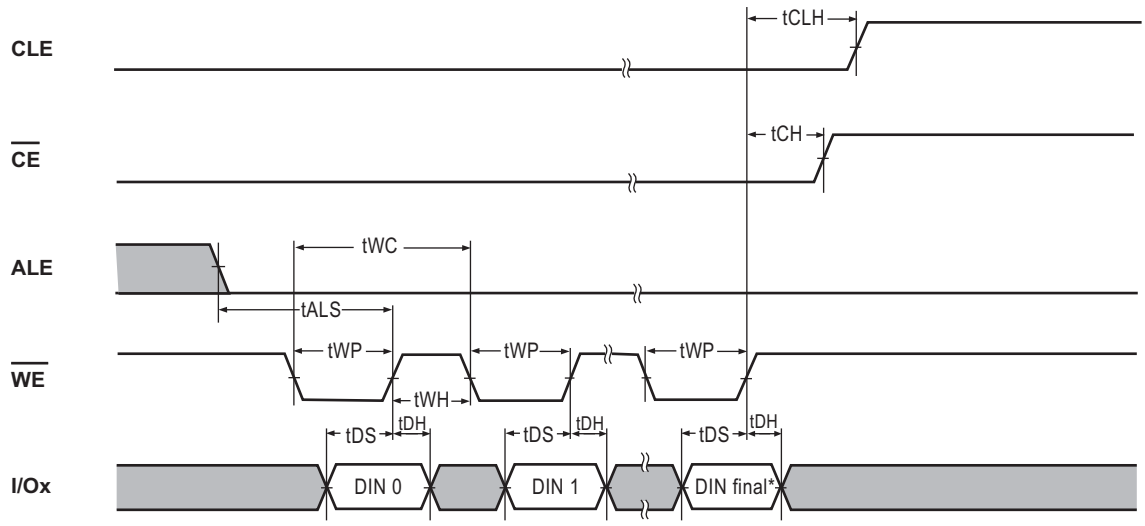
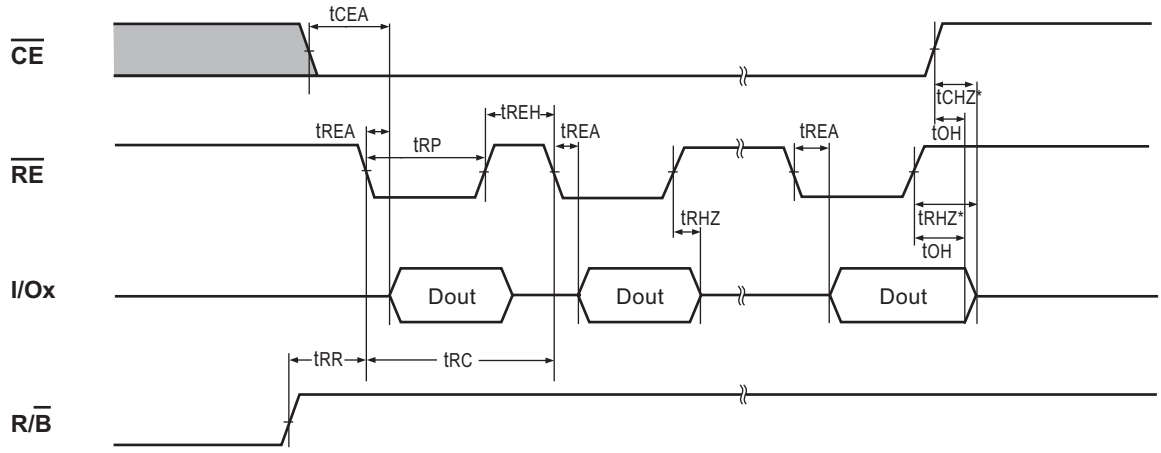


Figure 5: Address Latch Cycle



Notes: DIN final means 2,112

Figure 6. Input Data Latch Cycle



Notes : Transition is measured ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.

Figure 7: Sequential Out Cycle after Read (CLE=L, $\overline{WE}$=H, ALE=L)

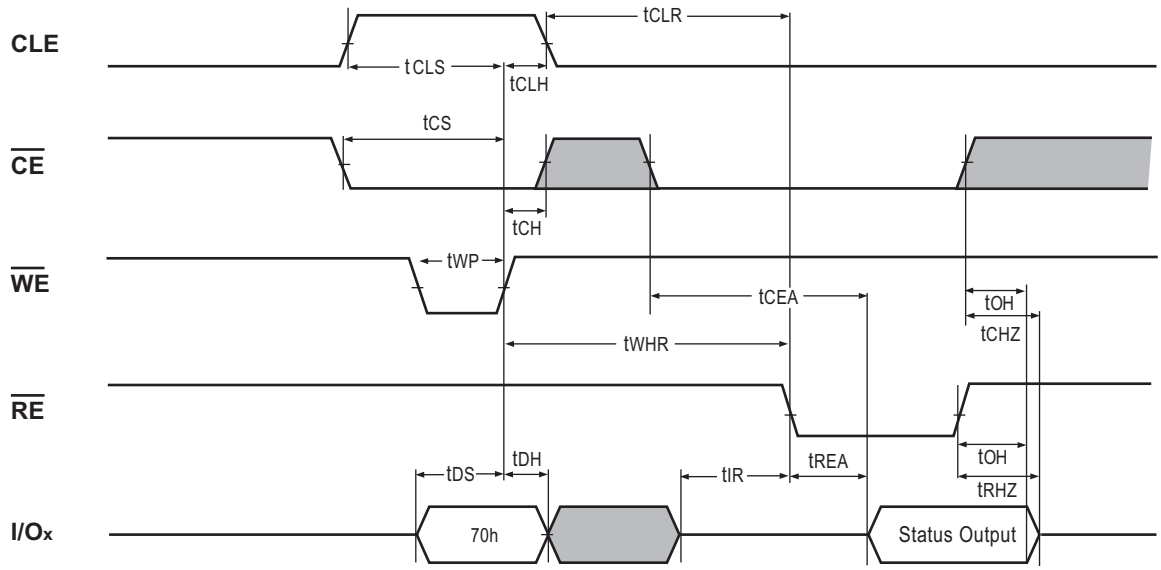


Figure 8: Status Read Cycle

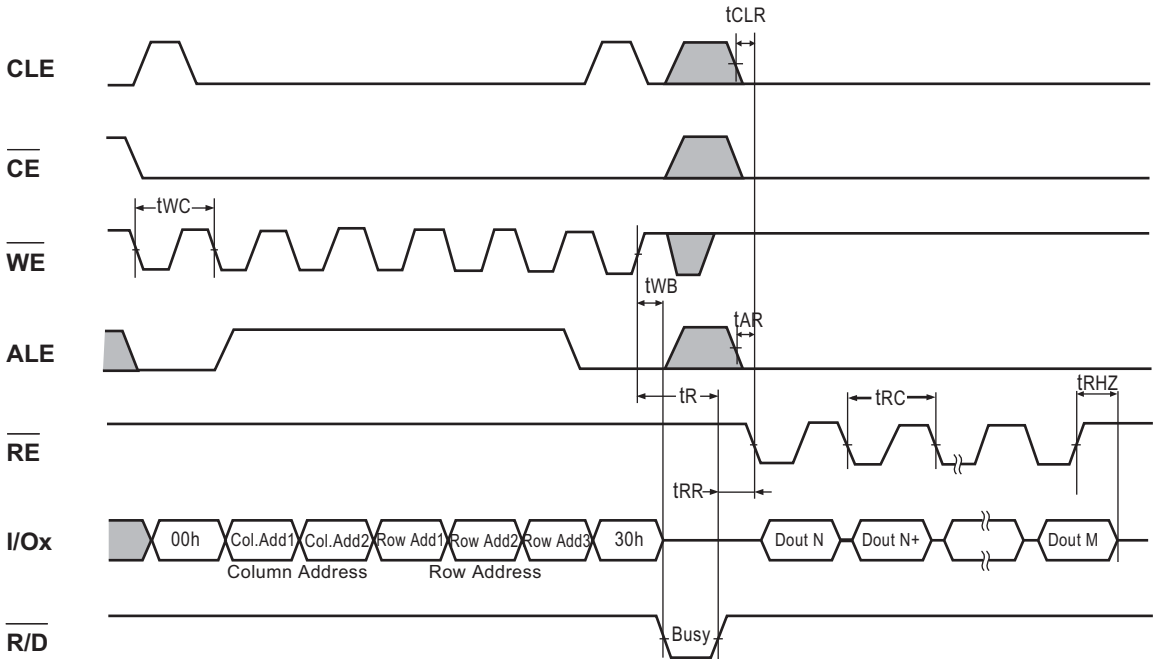


Figure 9: Read1 Operation (Read One Page)

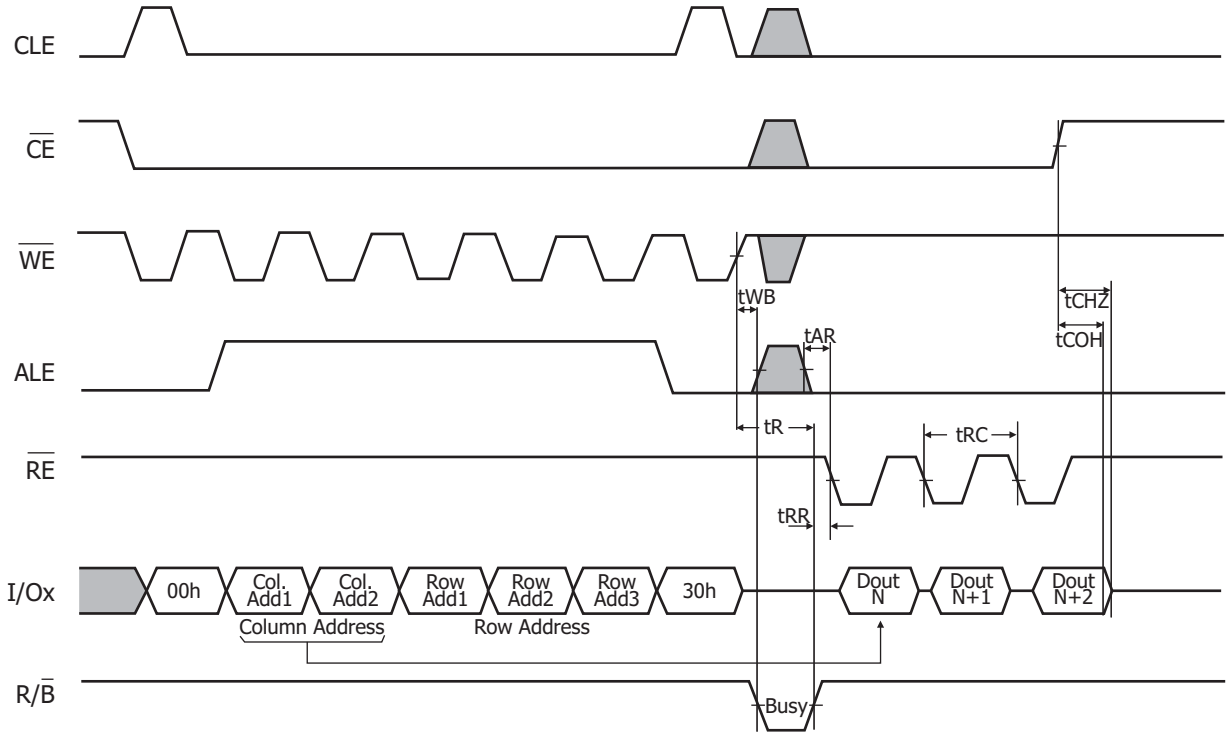


Figure 10: Read1 Operation intercepted by $\overline{CE}$

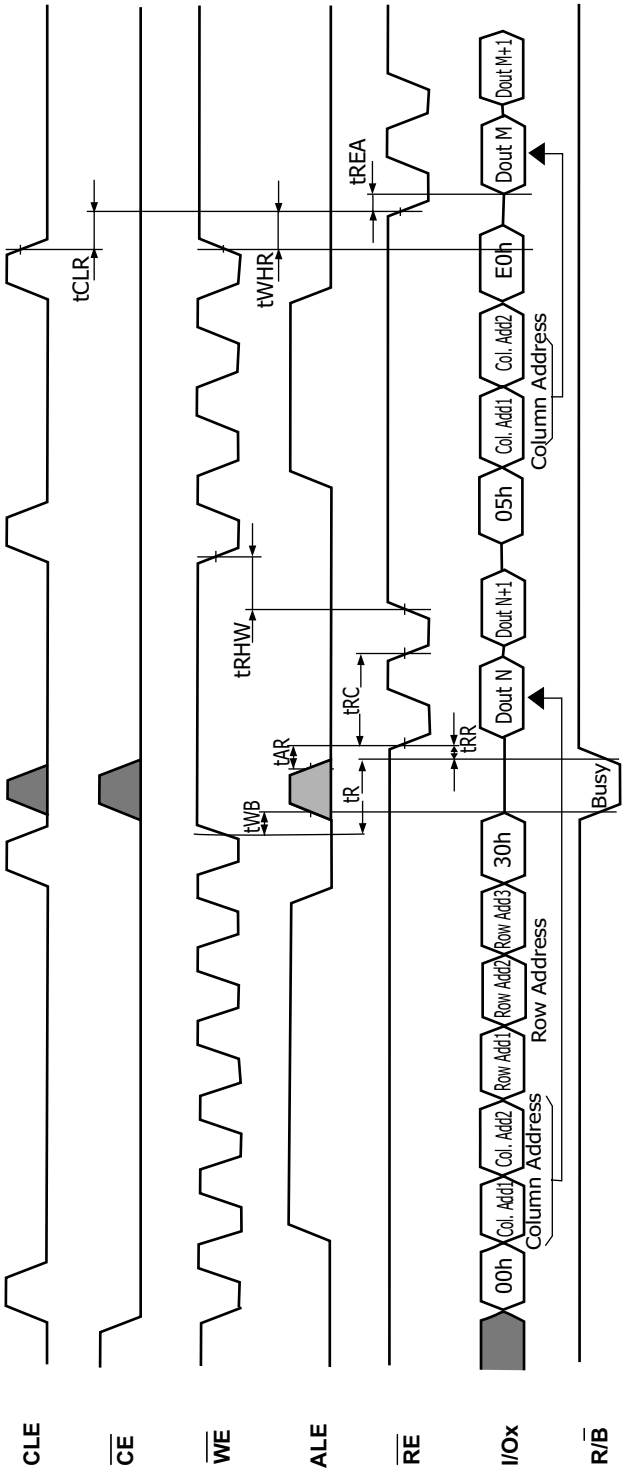


Figure 11 : Random Data output

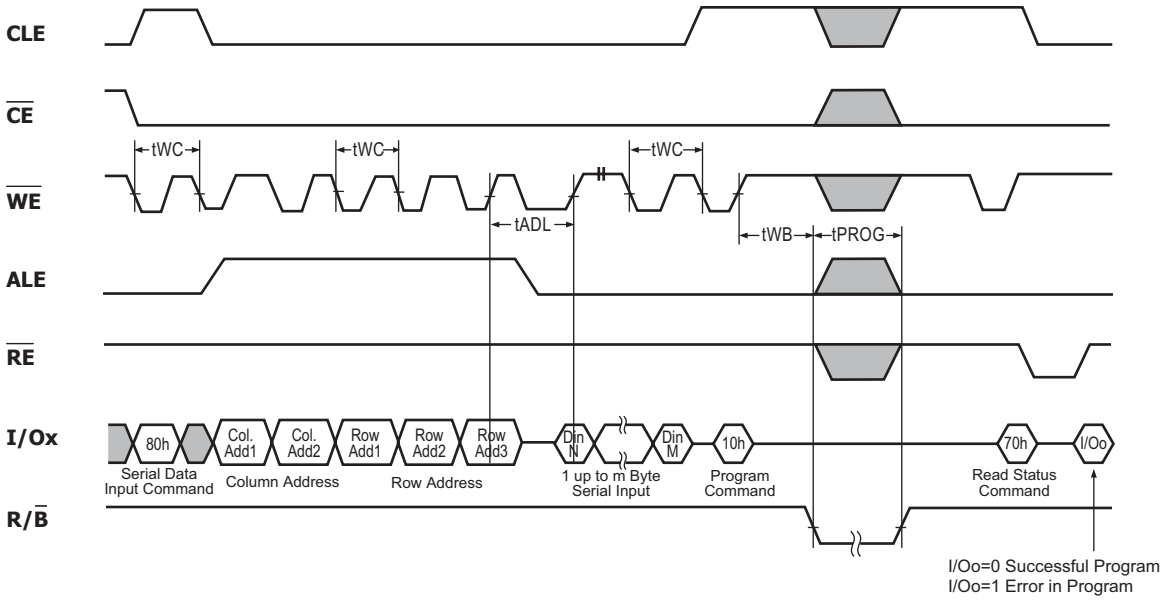


Figure 12: Page Program Operation

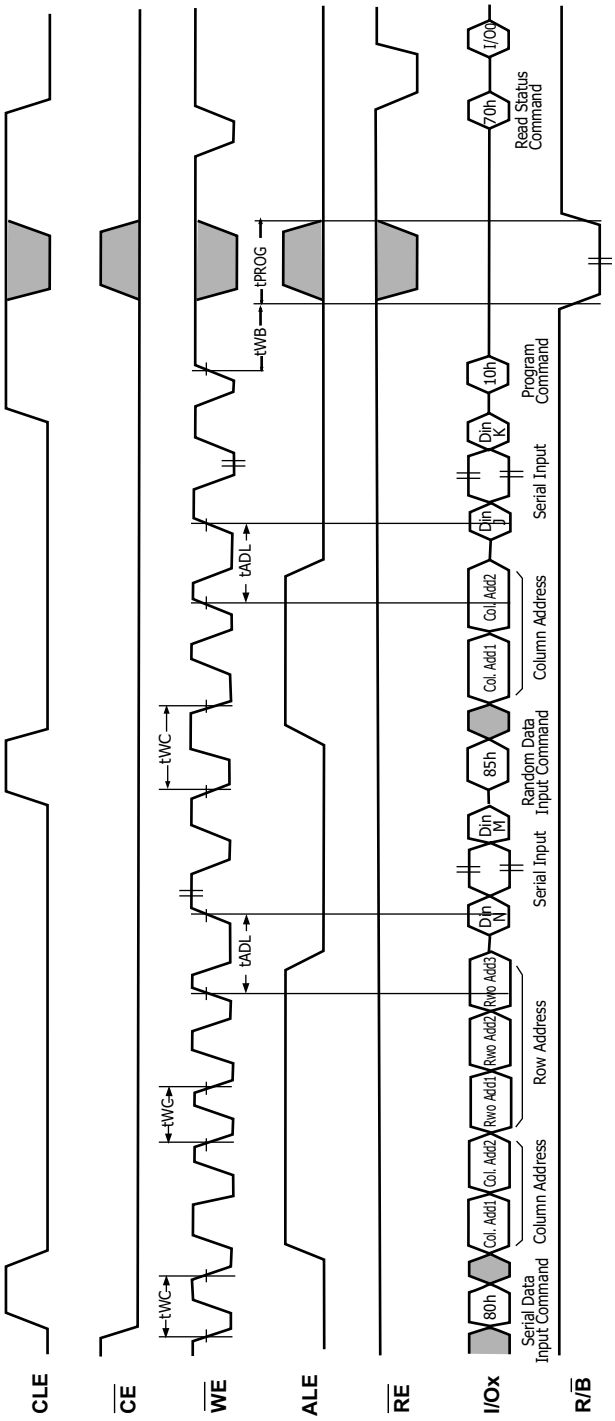


Figure 13 : Random Data In

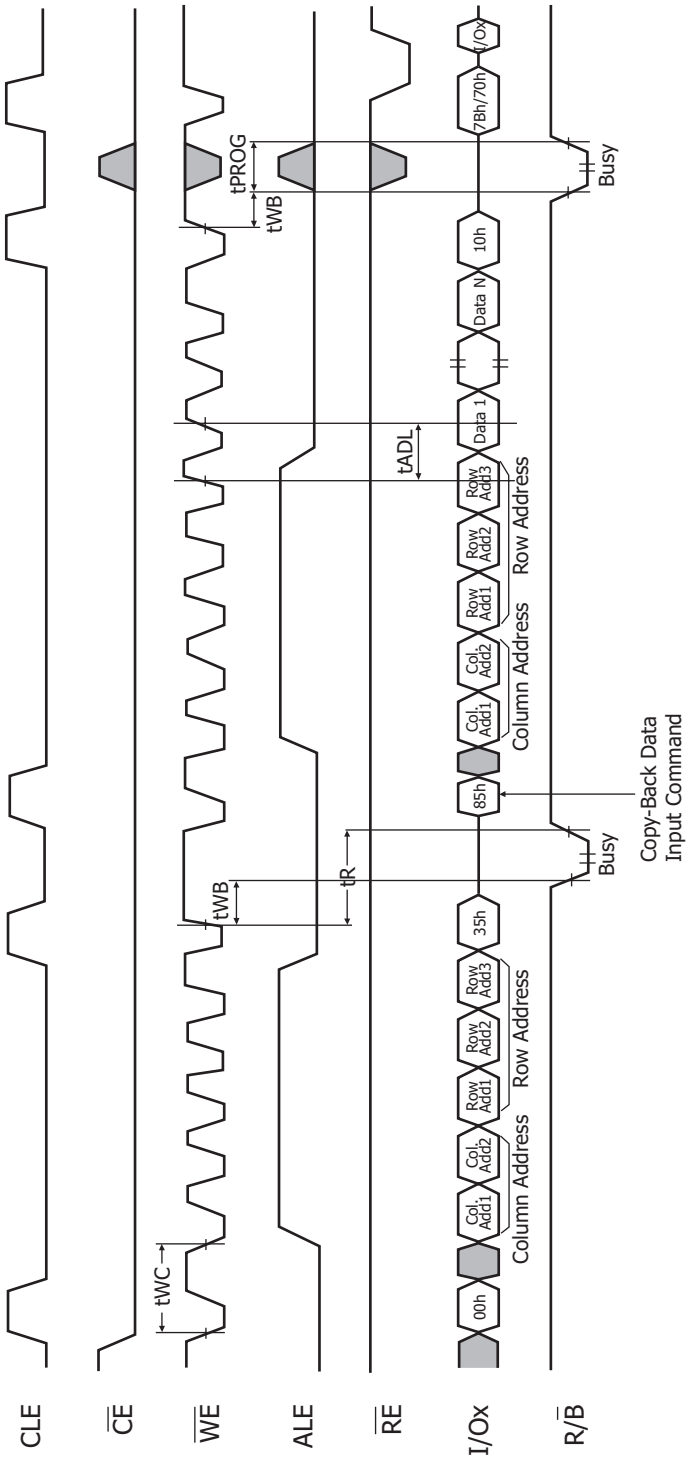


Figure 14 : Copy Back Program

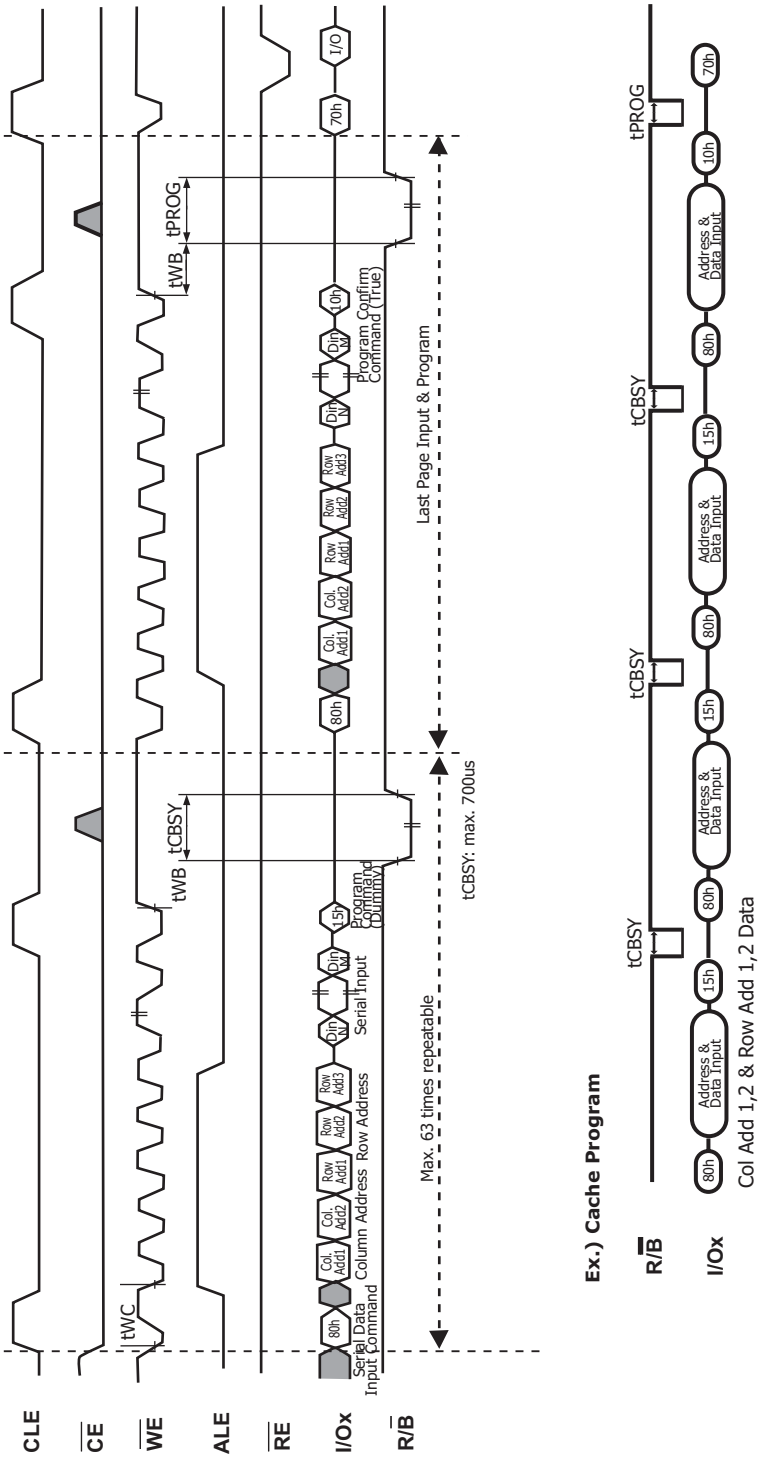


Figure 15 : Cache Program

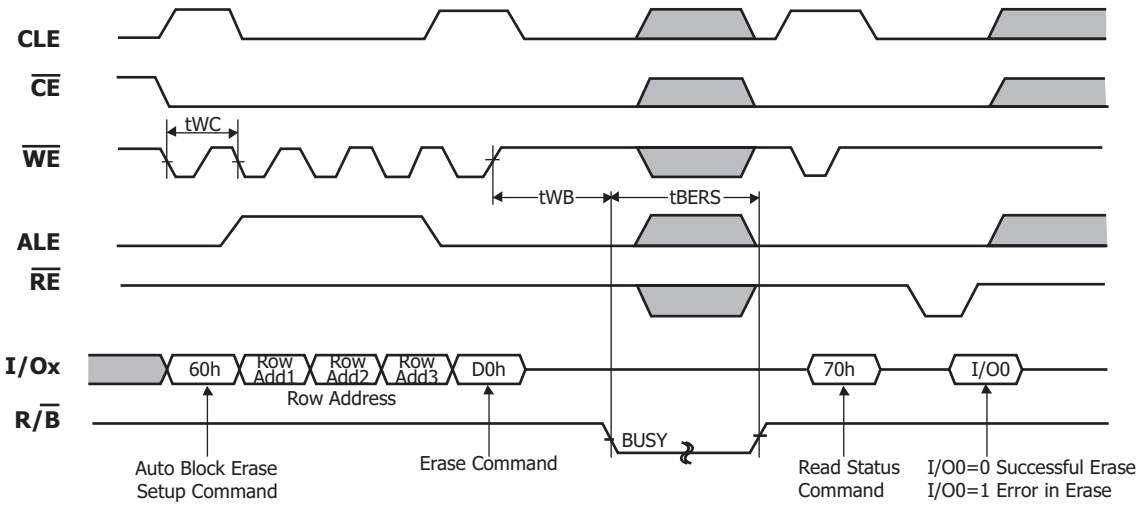


Figure 16: Block Erase Operation (Erase One Block)

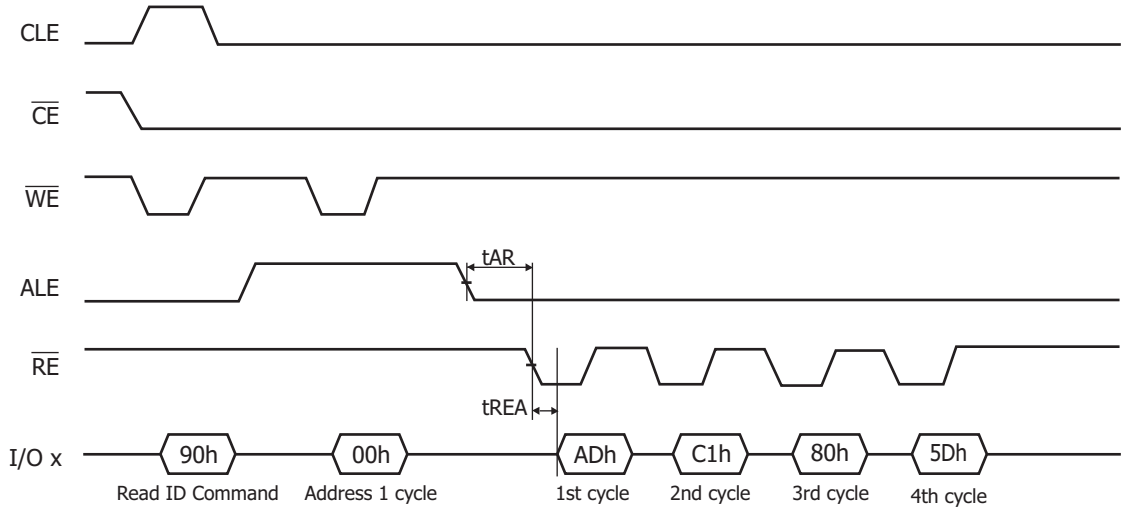


Figure 17: Read ID Operation

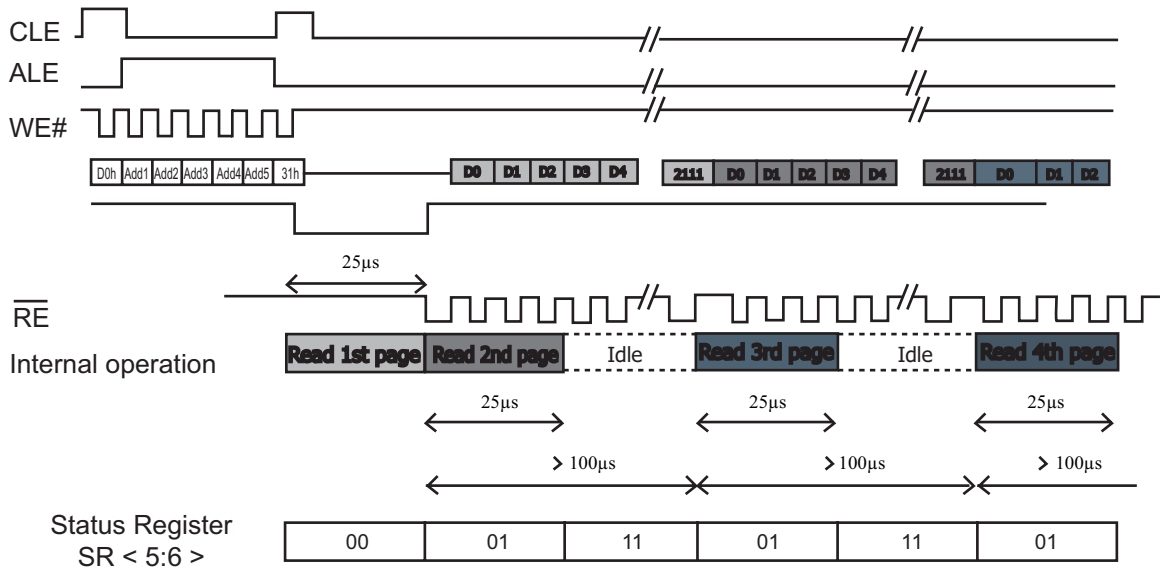


Figure 18: start address at page start :after 1st latency uninterrupted data flow

System Interface Using $\overline{CE}$ don't care

To simplify system interface, $\overline{CE}$ may be deasserted during data loading or sequential data-reading as shown below. So, it is possible to connect NAND Flash to a microporcessor. The only function that was removed from standard NAND Flash to make $\overline{CE}$ don't care read operation was disabling of the automatic sequential read function.

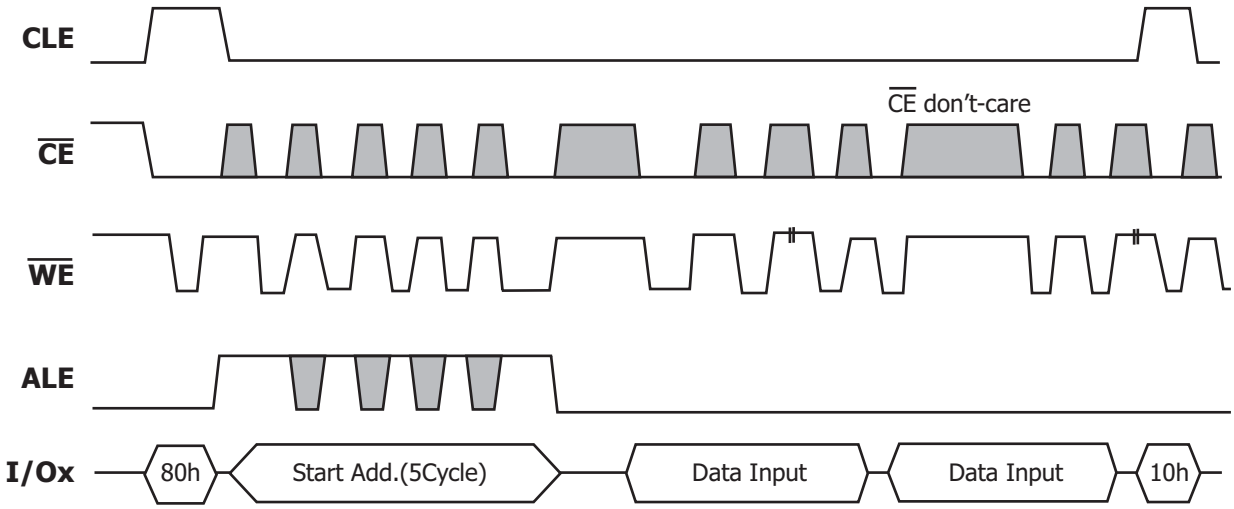


Figure 19: Program Operation with $\overline{CE}$ don't-care.

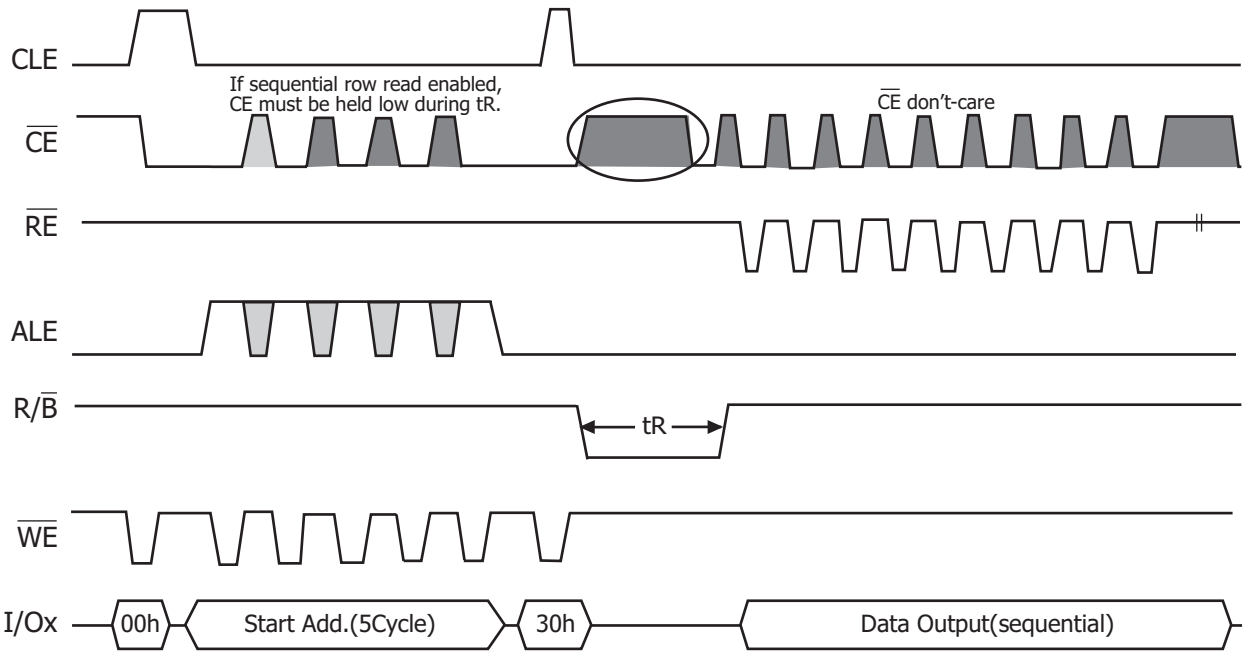


Figure 20: Read Operation with $\overline{CE}$ don't-care.

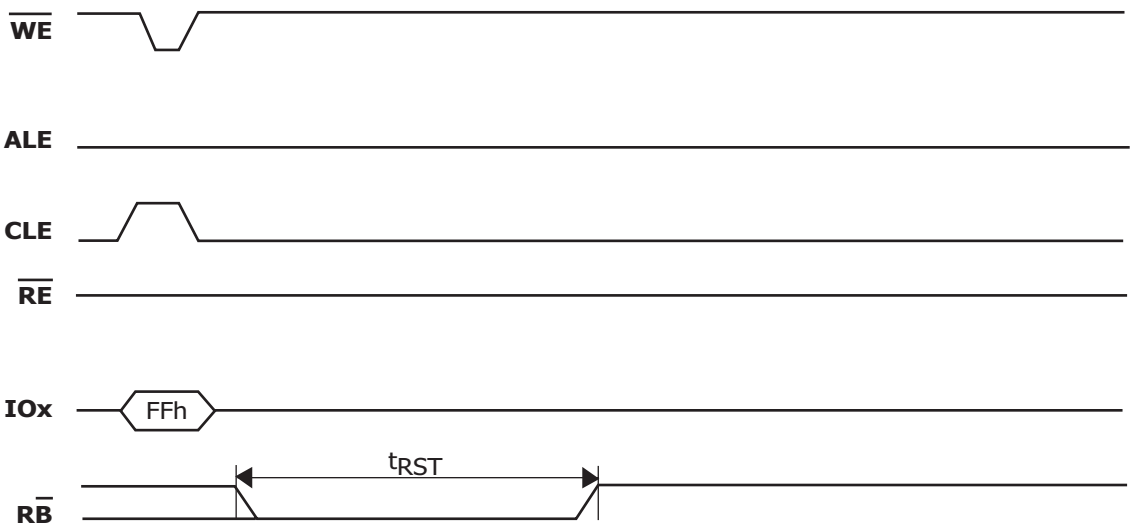


Figure 21: Reset Operation

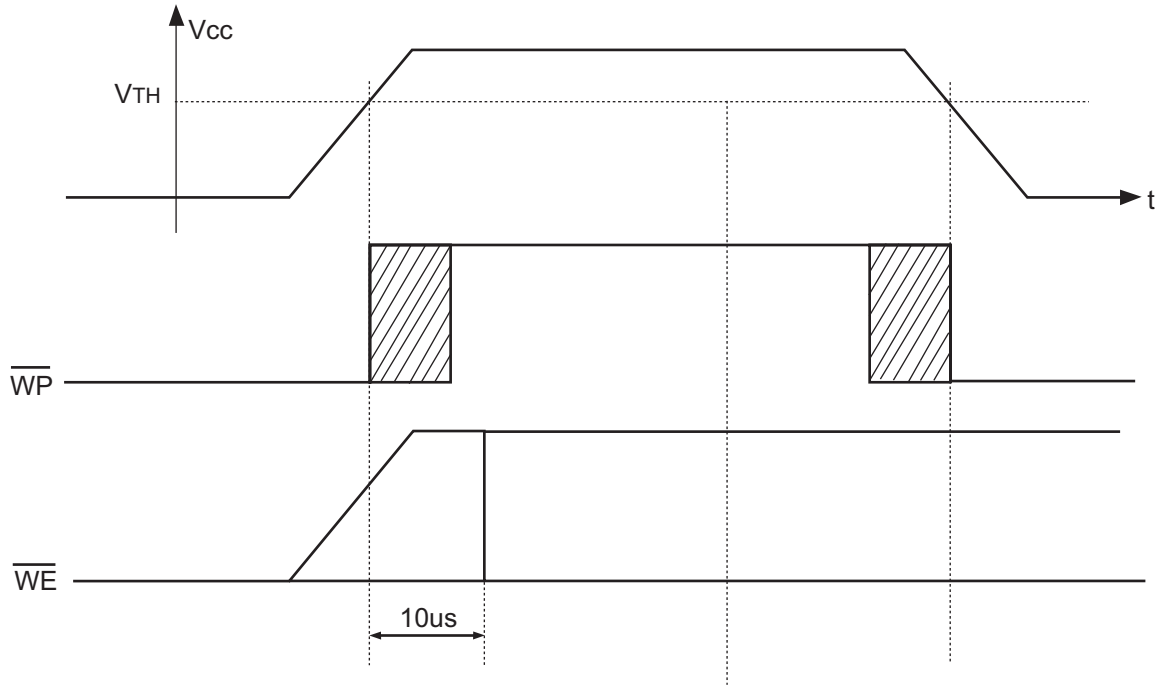
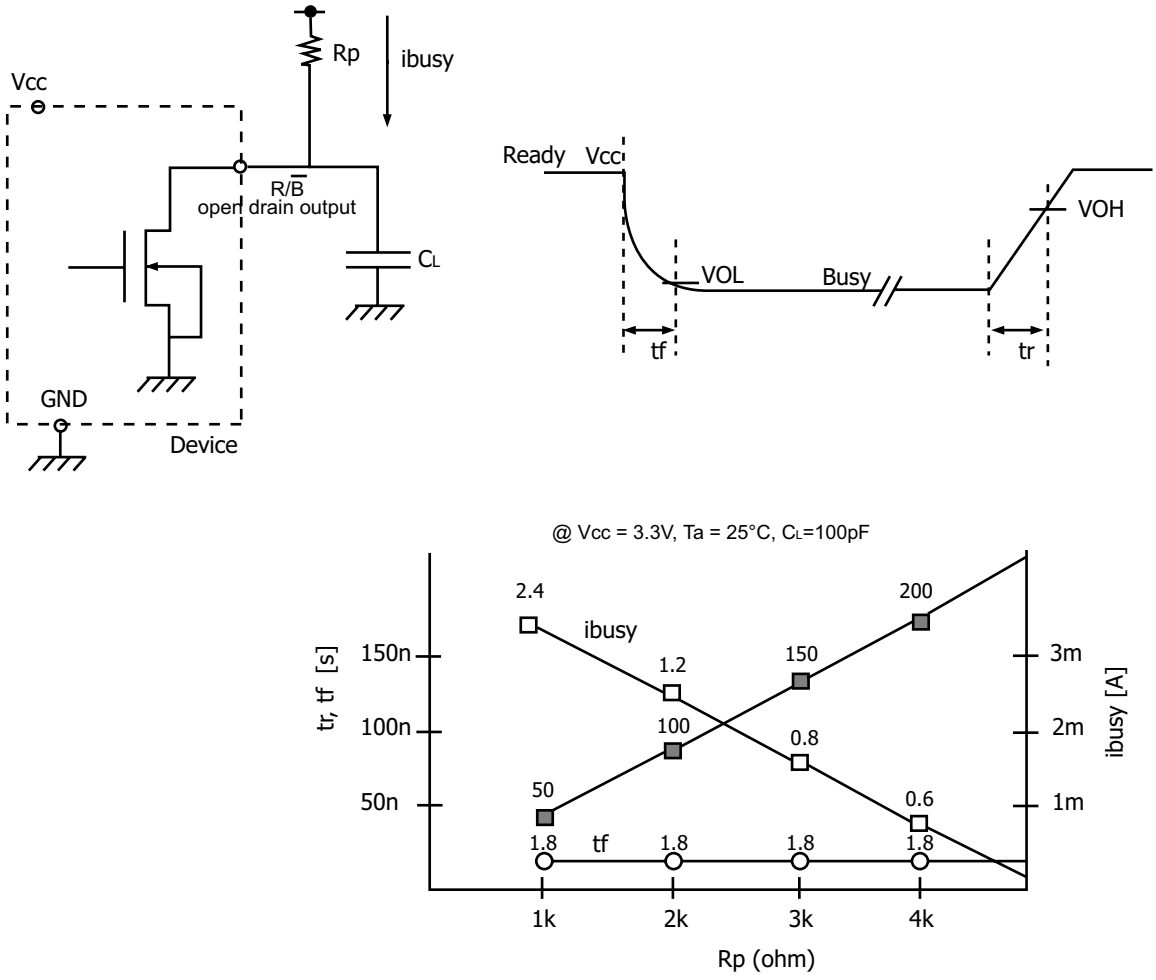


Figure 22: Power On and Data Protection Timing

VTH = 2.5 Volt for 3.3 Volt Supply devices



Rp value guidence

$$Rp(\text{min, 3.3V part}) = \frac{Vcc\ (Max.) - V_{OL}\ (Max.)}{I_{OL} + \sum I_L} = \frac{3.2V}{8mA + \sum I_L}$$

where IL is the sum of the input currnts of all devices tied to the R/$\overline{B}$ pin.

Rp(max) is determined by maximum permissible limit of tr

Figure 23: Ready/Busy Pin electrical specifications

Bad Block Management

Devices with Bad Blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A Bad Block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor. The devices are supplied with all the locations inside valid blocks erased(FFh).

The Bad Block Information is written prior to shipping. Any block where the 1st Byte/ 1st Word in the spare area of the 1st or 2nd page (if the 1st page is Bad) does not contain FFh is a Bad Block. The Bad Block Information must be read before any erase is attempted as the Bad Block Information may be erased. For the system to be able to recognize the Bad Blocks based on the original information it is recommended to create a Bad Block table following the flowchart shown in Figure 24. The 1st block, which is placed on 00h block address is guaranteed to be a valid block.

Block Replacement

Over the lifetime of the device additional Bad Blocks may develop. In this case the block has to be replaced by copying the data to a valid block. These additional Bad Blocks can be identified as attempts to program or erase them will give errors in the Status Register.

As the failure of a page program operation does not affect the data in other pages in the same block, the block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block. The Copy Back Program command can be used to copy the data to a valid block.

See the "Copy Back Program" section for more details.

Refer to Table 18 for the recommended procedure to follow if an error occurs during an operation.

Operation	Recommended Procedure
Erase	Block Replacement
Program	Block Replacement or ECC (with 1bit/528byte)
Read	ECC (with 1bit/528byte)

Table 18: Block Failure

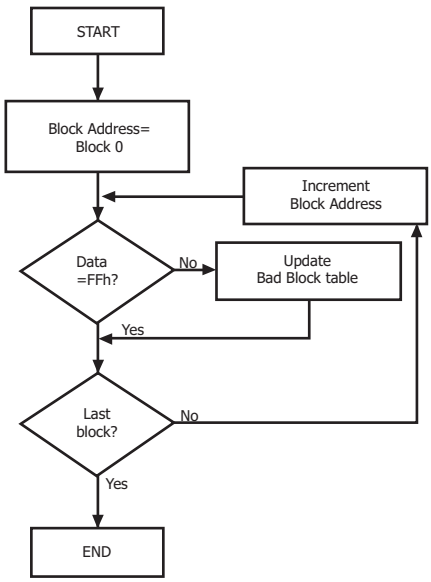


Figure 24: Bad Block Management Flowchart

Write Protect Operation

The Erase and Program Operations are automatically reset when $\overline{WP}$ goes Low (tWW = 100ns, min). The operations are enabled and disabled as follows (Figure 26~29)

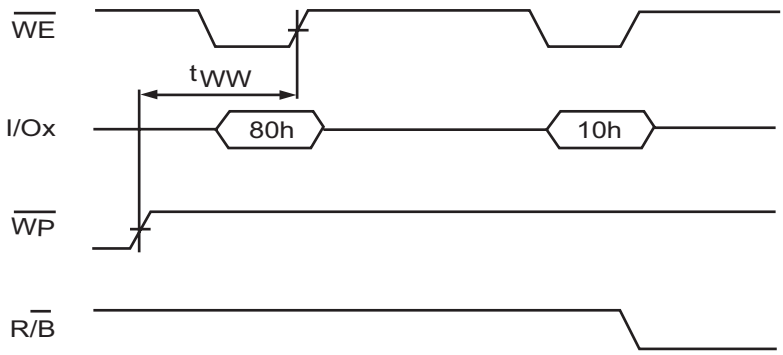


Figure 25: Enable Programming

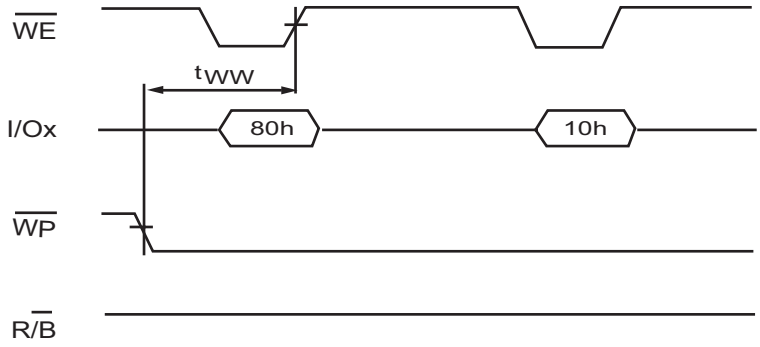


Figure 26: Disable Programming

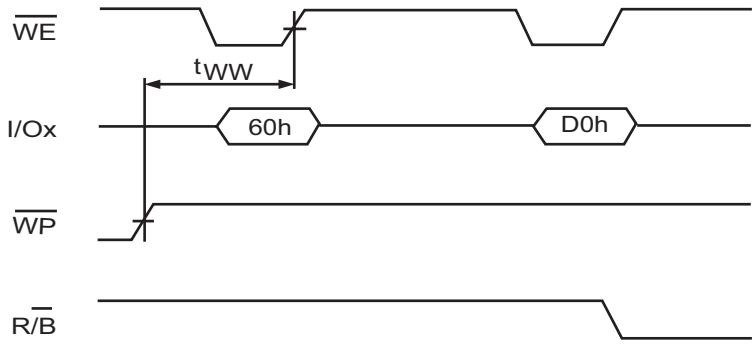


Figure 27: Enable Erasing

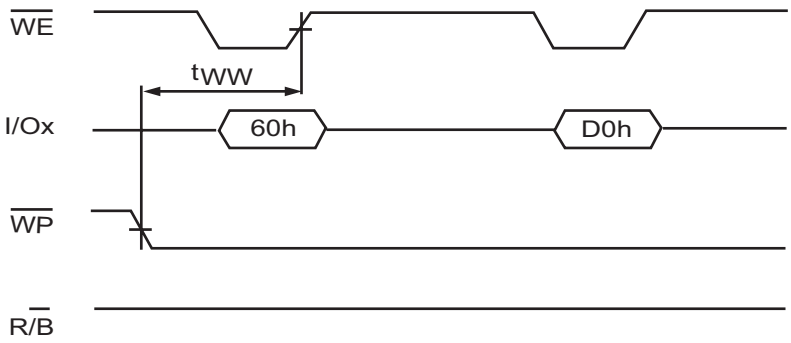


Figure 28: Disable Erasing

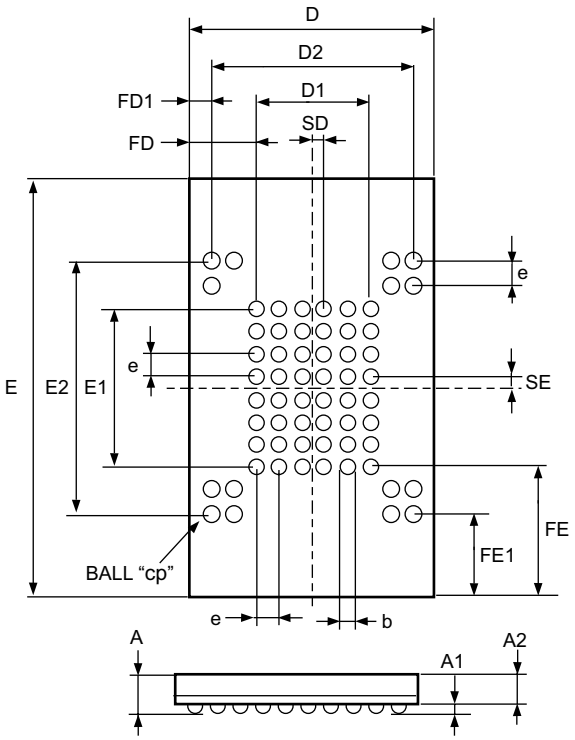
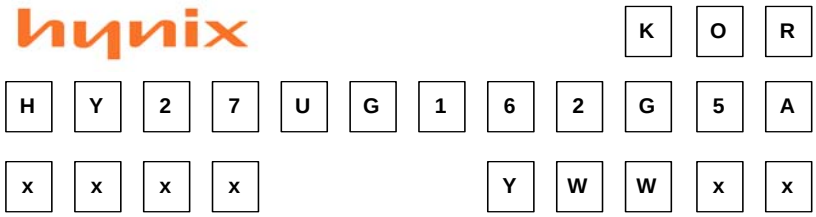


Figure 29. 63-ball FBGA, 9 x 11 ball array 0.8 mm pitch, Package Outline

Symbol	Millimeters		
	Min	Typ	Max
A		0.80	0.86
A1		0.20	
A2		0.60	
b	0.25	0.30	0.35
D	8.90	9.00	9.10
D1		4.00	
D2		7.20	
E	10.90	11.00	11.10
E1		5.60	
E2		8.80	
e		0.80	
FD		2.50	
FD1		0.90	
FE		2.70	
FE1		1.10	
SD		0.40	
SE		0.40	

Table 19: 63-ball FBGA - 9 x 11 ball array 0.8mm pitch, Pakage Mechanical Data

MARKING INFORMATION - FBGA

Packag	Marking Example
FBGA	

- **hynix** : Hynix Symbol
- **KOR** : Origin Country

- **HY27UG162G5A xxxx** : Part Number
  - **HY:** Hynix
  - **27:** NAND Flash
  - **U:** Power Supply : U(2.7V~3.6V)
  - **G:** Classification : Single Level Cell+Double Die+Large Block
  - **16:** Bit Organization : 16(x16)
  - **2G:** Density : 2Gbit
  - **5:** Mode : 2nCE & 2R/nB; Sequential Row Read Disable
  - **A:** Version : 2nd Generation

- **x:** Package Type : F(63-FBGA)
- **x:** Package Material : Blank(Normal), P(Lead Free)
- **x:** Operating Temperature : C(0℃~70℃), I(-40℃~85℃)
- **x:** Bad Block : B(Included Bad Block), S(1~5 Bad Block), P(All Good Block)

- **Y:** Year (ex: 5=year 2005, 06= year 2006)
- **ww:** Work Week (ex: 12= work week 12)
- **xx:** Process Code

Note

- **Capital Letter** : Fixed Item
- **Small Letter** : Non-fixed Item