

IS61WV25632ALL/ALS IS61WV25632BLL/BLS IS64WV25632BLL/BLS



256K x 32 HIGH-SPEED ASYNCHRONOUS CMOS STATIC RAM WITH 3.3V SUPPLY

PRELIMINARY INFORMATION
APRIL 2008

FEATURES

- High-speed access times:
8, 10, 20 ns
- High-performance, low-power CMOS process
- Multiple center power and ground pins for greater noise immunity
- Easy memory expansion with \overline{CE} and \overline{OE} options
- \overline{CE} power-down
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Single power supply
V_{DD} 1.65V to 2.2V (IS61WV25632Axx)
speed = 20ns for V_{DD} 1.65V to 2.2V
V_{DD} 2.4V to 3.6V (IS61/64WV25632Bxx)
speed = 10ns for V_{DD} 2.4V to 3.6V
speed = 8ns for V_{DD} 3.3V ± 5%
- Packages available:
 - 90-ball miniBGA (8mm x 13mm)
- Industrial and Automotive Temperature Support
- Lead-free available

DESCRIPTION

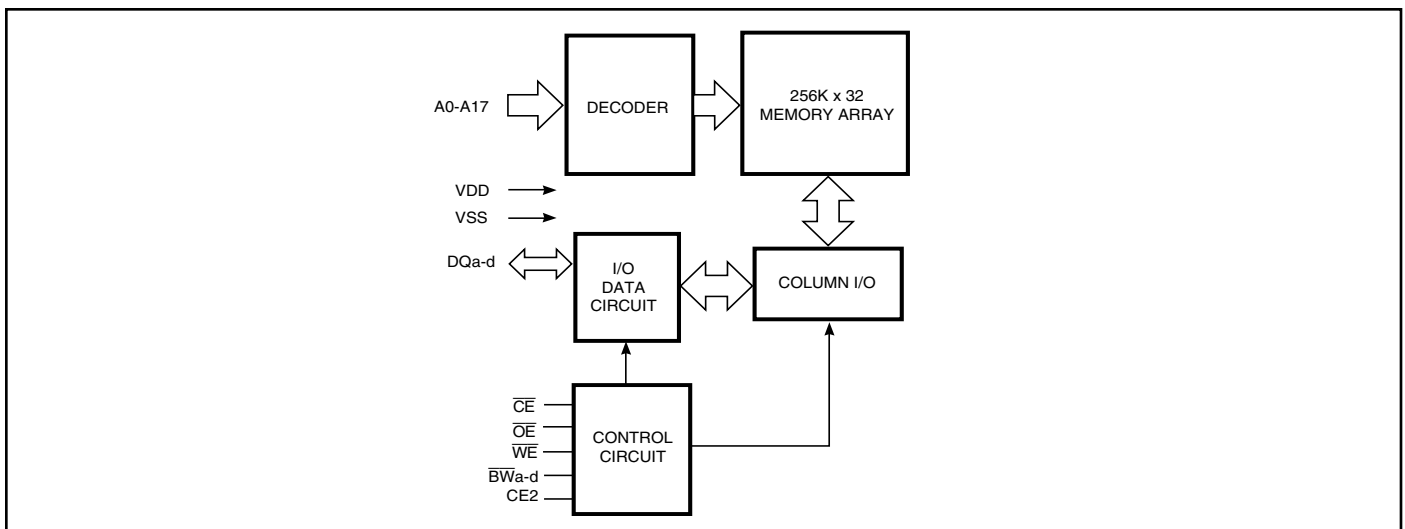
The *ISSI* IS61WV25632Axx/Bxx and IS64WV25632Bxx are high-speed, 8M-bit static RAMs organized as 256K words by 32 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When \overline{CE} is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs, \overline{CE} and \overline{OE} . The active LOW Write Enable (\overline{WE}) controls both writing and reading of the memory.

The device is packaged in the JEDEC standard 90-ball BGA (8mm x 13mm).

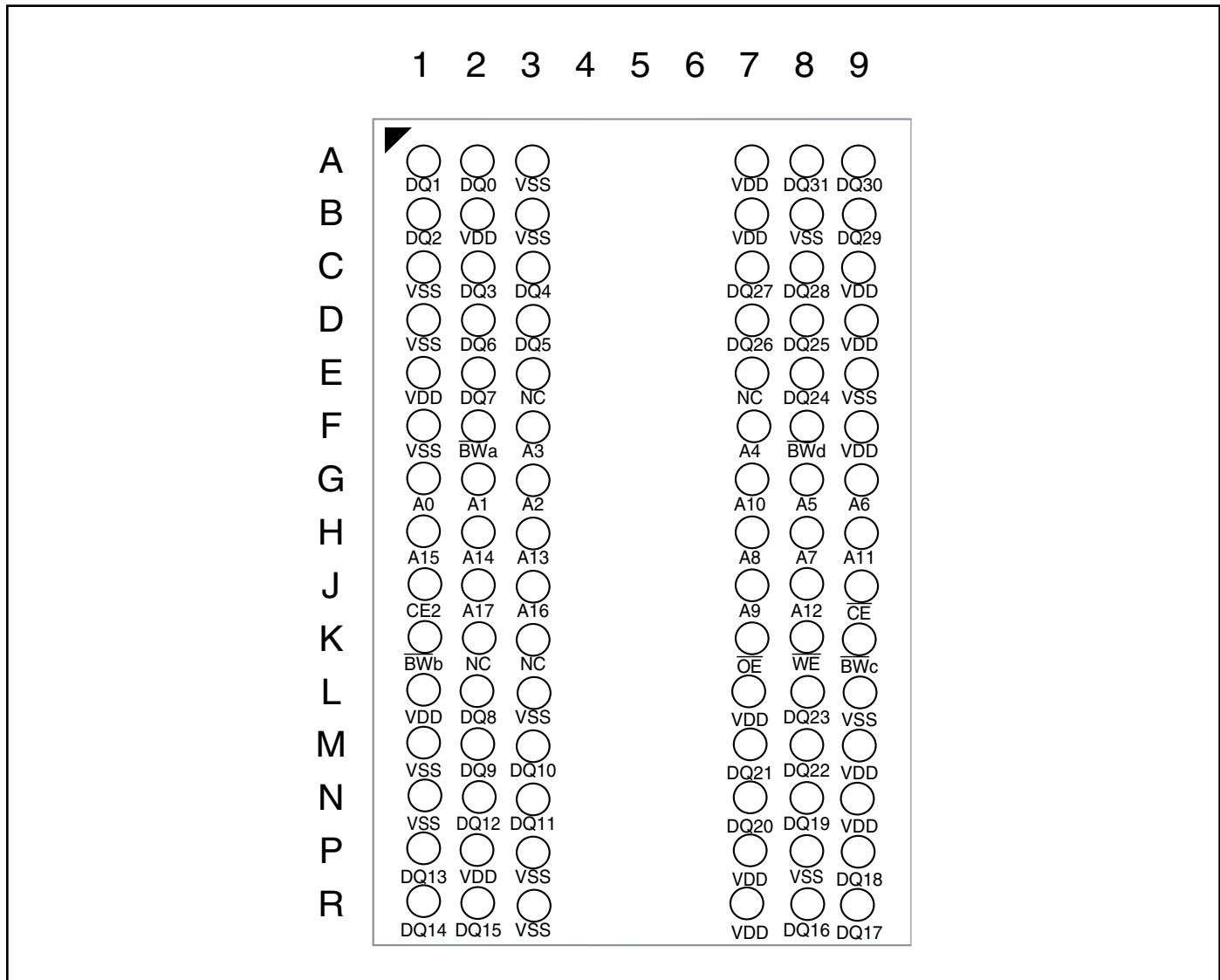
FUNCTIONAL BLOCK DIAGRAM



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PIN CONFIGURATION

PACKAGE CODE: B 90 BALL FBGA (Top View) (8.00 mm x 13.00 mm Body, 0.8 mm Ball Pitch)



PIN DESCRIPTIONS

A0-A17	Address Inputs
DQx	Data I/O
CE, CE2	Chip Enable Input
OE	Output Enable Input
WE	Write Enable Input
BW _x (x=a-d)	Byte Write Control
V _{DD}	Power
V _{SS}	Ground
NC	No Connection

TRUTH TABLE

CE	CE2	OE	WE	BW _a	BW _b	BW _c	BW _d	DQ ₀₋₇	DQ ₈₋₁₅	DQ ₁₆₋₂₃	DQ ₂₄₋₃₁	Mode	Power
H	X	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Power Down	(I _{SB})
X	L	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Power Down	(I _{SB})
L	H	L	H	L	L	L	L	Data Out	Data Out	Data Out	Data Out	Read All Bits	(I _{CC})
L	H	L	H	L	H	H	H	Data Out	High-Z	High-Z	High-Z	Read Byte a Bits Only	(I _{CC})
L	H	L	H	H	L	H	H	High-Z	Data Out	High-Z	High-Z	Read Byte b Bits Only	(I _{CC})
L	H	L	H	H	H	L	H	High-Z	High-Z	Data Out	High-Z	Read Byte c Bits Only	(I _{CC})
L	H	L	H	H	H	H	L	High-Z	High-Z	High-Z	Data Out	Read Byte d Bits Only	(I _{CC})
L	H	X	L	L	L	L	L	Data In	Data In	Data In	Data In	Write All Bits	(I _{CC})
L	H	X	L	L	H	H	H	Data In	High-Z	High-Z	High-Z	Write Byte a Bits Only	(I _{CC})
L	H	X	L	H	L	H	H	High-Z	Data In	High-Z	High-Z	Write Byte b Bits Only	(I _{CC})
L	H	X	L	H	H	L	H	High-Z	High-Z	Data In	High-Z	Write Byte c Bits Only	(I _{CC})
L	H	X	L	H	H	H	L	High-Z	High-Z	High-Z	Data In	Write Byte d Bits Only	(I _{CC})
L	H	H	H	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Selected, Outputs Disabled	(I _{CC})

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
V _{TERM}	Terminal Voltage with Respect to GND	-0.5 to V _{DD} + 0.5	V
V _{DD}	V _{DD} Relates to GND	-0.3 to 4.0	V
T _{STG}	Storage Temperature	-65 to +150	°C
P _T	Power Dissipation	1.0	W

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE^(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	pF
C _{I/O}	Input/Output Capacitance	V _{OUT} = 0V	8	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V.

HIGH SPEED

OPERATING RANGE (V_{DD}) (IS61WV25632ALL)

Range	Ambient Temperature	V _{DD}	Speed
Commercial	0°C to +70°C	1.65V-2.2V	20ns
Industrial	-40°C to +85°C	1.65V-2.2V	20ns
Automotive	-40°C to +125°C	1.65V-2.2V	20ns

OPERATING RANGE (V_{DD}) (IS61WV25632BLL)⁽¹⁾

Range	Ambient Temperature	V _{DD} (8 ns) ¹	V _{DD} (10 ns) ¹
Commercial	0°C to +70°C	3.3V ± 5%	2.4V-3.6V
Industrial	-40°C to +85°C	3.3V ± 5%	2.4V-3.6V

Note:

- When operated in the range of 2.4V-3.6V, the device meets 10ns. When operated in the range of 3.3V ± 5%, the device meets 8ns.

OPERATING RANGE (V_{DD}) (IS64WV25632BLL)

Range	Ambient Temperature	V _{DD} (10 ns)
Automotive	-40°C to +125°C	2.4V-3.6V

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions		-8		-10		-20		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
I _{CC}	V _{DD} Dynamic Operating Supply Current	V _{DD} = Max., I _{OUT} = 0 mA, f = f _{MAX}	Com.	—	110	—	90	—	50	mA
			Ind.	—	115	—	95	—	60	
			Auto. typ. ⁽²⁾	—	—	—	140	—	100	
I _{CC1}	Operating Supply Current	V _{DD} = Max., I _{OUT} = 0 mA, f = 0	Com.	—	85	—	85	—	45	mA
			Ind.	—	90	—	90	—	55	
			Auto.	—	—	—	110	—	90	
I _{SB1}	TTL Standby Current (TTL Inputs)	V _{DD} = Max., V _{IN} = V _{IH} or V _{IL} CE ≥ V _{IH} , f = 0	Com.	—	30	—	30	—	30	mA
			Ind.	—	35	—	35	—	35	
			Auto.	—	—	—	70	—	70	
I _{SB2}	CMOS Standby Current (CMOS Inputs)	V _{DD} = Max., CE ≥ V _{DD} - 0.2V, V _{IN} ≥ V _{DD} - 0.2V, or V _{IN} ≤ 0.2V, f = 0	Com.	—	20	—	20	—	20	mA
			Ind.	—	25	—	25	—	25	
			Auto. typ. ⁽²⁾	—	—	—	60	—	60	

Note:

- At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
- Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

LOW POWER

OPERATING RANGE (V_{DD}) (IS61WV25632ALS)

Range	Ambient Temperature	V _{DD}	Speed
Commercial	0°C to +70°C	1.65V-2.2V	35ns
Industrial	-40°C to +85°C	1.65V-2.2V	35ns
Automotive	-40°C to +125°C	1.65V-2.2V	35ns

OPERATING RANGE (V_{DD}) (IS61WV25632BLS)⁽¹⁾

Range	Ambient Temperature	V _{DD} (25 ns) ¹
Commercial	0°C to +70°C	2.4V-3.6V
Industrial	-40°C to +85°C	2.4V-3.6V

Note:

1. When operated in the range of 2.4V-3.6V, the device meets 25ns. When operated in the range of 3.3V ± 5%, the device meets 20ns.

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions		-25		-35		Unit
				Min.	Max.	Min.	Max.	
I _{CC}	V _{DD} Dynamic Operating Supply Current	V _{DD} = Max., I _{OUT} = 0 mA, f = f _{MAX}	Com.	—	30	—	25	mA
			Ind.	—	35	—	30	
			Auto.	—	60	—	60	
			typ. ⁽²⁾	25				
I _{CC1}	Operating Supply Current	V _{DD} = Max., I _{OUT} = 0 mA, f = 0	Com.	—	20	—	20	mA
			Ind.	—	30	—	30	
			Auto.	—	50	—	50	
I _{SB1}	TTL Standby Current (TTL Inputs)	V _{DD} = Max., V _{IN} = V _{IH} or V _{IL} CE ≥ V _{IH} , f = 0	Com.	—	15	—	15	mA
			Ind.	—	20	—	20	
			Auto.	—	40	—	40	
I _{SB2}	CMOS Standby Current (CMOS Inputs)	V _{DD} = Max., CE ≥ V _{DD} - 0.2V, V _{IN} ≥ V _{DD} - 0.2V, or V _{IN} ≤ 0.2V, f = 0	Com.	—	0.8	—	0.8	mA
			Ind.	—	1.2	—	1.2	
			Auto.	—	2	—	2	
			typ. ⁽²⁾	0.1		0.1		

Note:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
 2. Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

AC TEST CONDITIONS (HIGH SPEED)

Parameter	Unit (2.4V-3.6V)	Unit (3.3V ± 5%)	Unit (1.65V-2.2V)
Input Pulse Level	0.4V to V _{DD} -0.3V	0.4V to V _{DD} -0.3V	0.4V to V _{DD} -0.2V
Input Rise and Fall Times	1.5ns	1.5ns	1.5ns
Input and Output Timing and Reference Level (V _{Ref})	V _{DD} /2	V _{DD} /2 + 0.05	V _{DD} /2
Output Load	See Figures 1 and 2	See Figures 1 and 2	See Figures 1 and 2

AC TEST LOADS

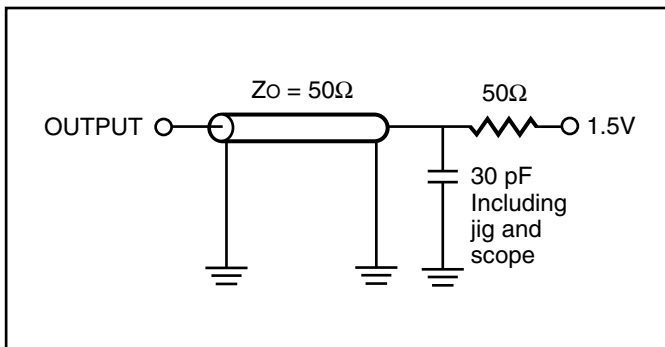


Figure 1.

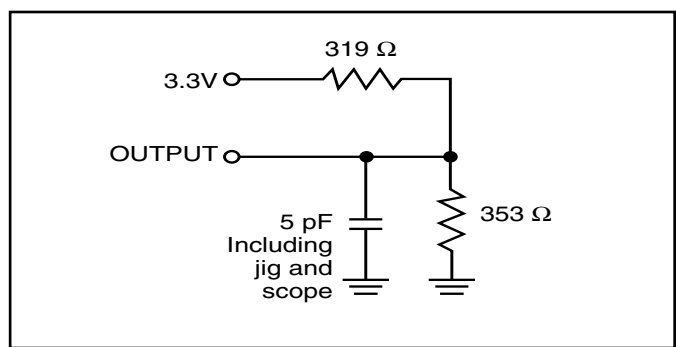


Figure 2.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	-8		-10		Unit
		Min.	Max.	Min.	Max.	
t _{RC}	Read Cycle Time	8	—	10	—	ns
t _{AA}	Address Access Time	—	8	—	10	ns
t _{OHA}	Output Hold Time	2.5	—	2.5	—	ns
t _{ACE}	$\overline{\text{CE}}$ Access Time	—	8	—	10	ns
t _{DOE}	$\overline{\text{OE}}$ Access Time	—	5.5	—	6.5	ns
t _{HZOE⁽²⁾}	$\overline{\text{OE}}$ to High-Z Output	—	3	—	4	ns
t _{LZOE⁽²⁾}	$\overline{\text{OE}}$ to Low-Z Output	0	—	0	—	ns
t _{HZCE⁽²⁾}	$\overline{\text{CE}}$ to High-Z Output	0	3	0	4	ns
t _{LZCE⁽²⁾}	$\overline{\text{CE}}$ to Low-Z Output	3	—	3	—	ns
t _{BA}	Byte Enable to Data Valid	3	—	3	—	ns
t _{LZB}	Byte Enable to Low-Z	0	—	0	—	ns
t _{HZB}	Byte Enable to High-Z	0	3	0	3	ns

Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

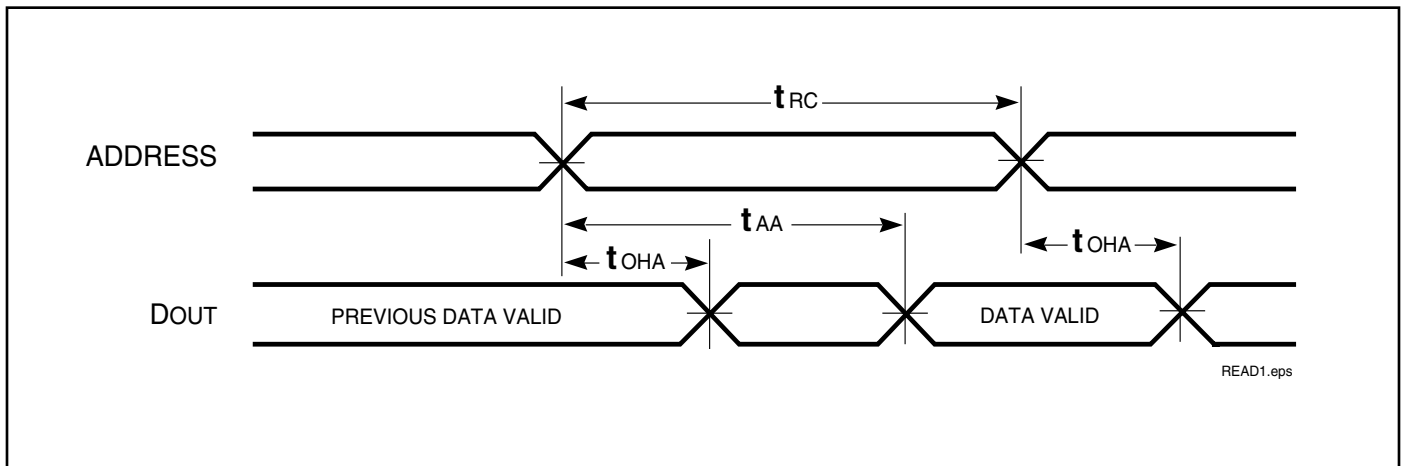
Symbol	Parameter	-20 ns		Unit
		Min.	Max.	
t _{RC}	Read Cycle Time	20	—	ns
t _{AA}	Address Access Time	—	20	ns
t _{OHA}	Output Hold Time	2.5	—	ns
t _{ACE}	CE Access Time	—	20	ns
t _{DOE}	OE Access Time	—	8	ns
t _{HZOE⁽²⁾}	OE to High-Z Output	0	8	ns
t _{LZOE⁽²⁾}	OE to Low-Z Output	0	—	ns
t _{HZCE⁽²⁾}	CE to High-Z Output	0	8	ns
t _{LZCE⁽²⁾}	CE to Low-Z Output	3	—	ns
t _{BA}	Byte Enable to Data Valid	3	—	ns
t _{LZB}	Byte Enable to Low-Z	0	—	ns
t _{HZB}	Byte Enable to High-Z	0	3	ns

Notes:

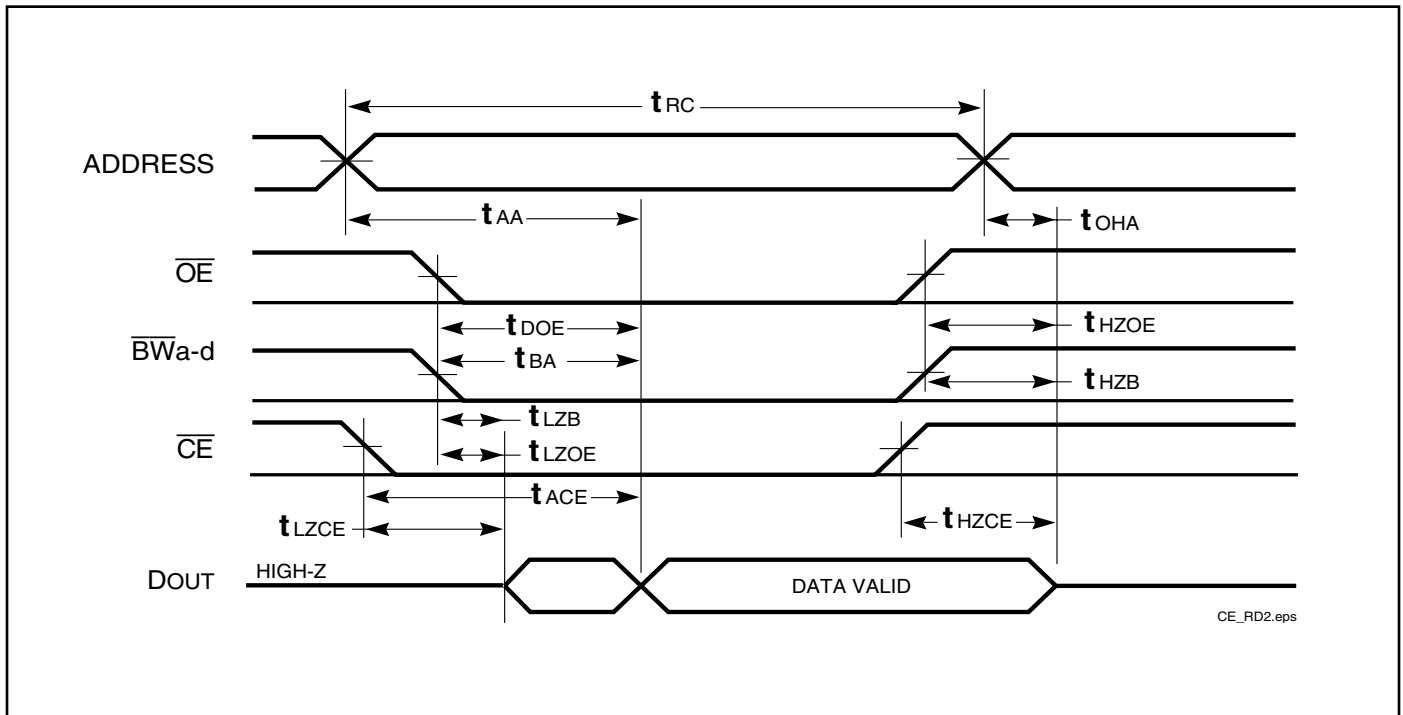
1. Test conditions assume signal transition times of 1.5 ns or less, timing reference levels of 1.25V, input pulse levels of 0.4V to V_{DD}-0.3V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC WAVEFORMS

READ CYCLE NO. 1^(1,2) (Address Controlled) ($\overline{CE} = \overline{OE} = V_{IL}$)



READ CYCLE NO. 2^(1,3) (\overline{CE} and \overline{OE} Controlled)



Notes:

1. \overline{WE} is HIGH for a Read Cycle.
2. The device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$.
3. Address is valid prior to or coincident with \overline{CE} LOW transitions.

WRITE CYCLE SWITCHING CHARACTERISTICS^(1,3) (Over Operating Range)

Symbol	Parameter	-8		-10		Unit
		Min.	Max.	Min.	Max.	
t _{WC}	Write Cycle Time	8	—	10	—	ns
t _{SCE}	\overline{CE} to Write End	6.5	—	8	—	ns
t _{AW}	Address Setup Time to Write End	6.5	—	8	—	ns
t _{HA}	Address Hold from Write End	0	—	0	—	ns
t _{SA}	Address Setup Time	0	—	0	—	ns
t _{PWB}	\overline{BWA} -d Valid to End of Write	6.5	—	8	—	ns
t _{PWE1}	\overline{WE} Pulse Width	6.5	—	8	—	ns
t _{PWE2}	\overline{WE} Pulse Width ($\overline{OE} = \text{LOW}$)	8.0	—	10	—	ns
t _{SD}	Data Setup to Write End	5	—	6	—	ns
t _{HD}	Data Hold from Write End	0	—	0	—	ns
t _{HZWE⁽²⁾}	\overline{WE} LOW to High-Z Output	—	3.5	—	5	ns
t _{LZWE⁽²⁾}	\overline{WE} HIGH to Low-Z Output	2	—	2	—	ns

Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of \overline{CE} LOW, and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write. Shaded area product in development

WRITE CYCLE SWITCHING CHARACTERISTICS^(1,2) (Over Operating Range)

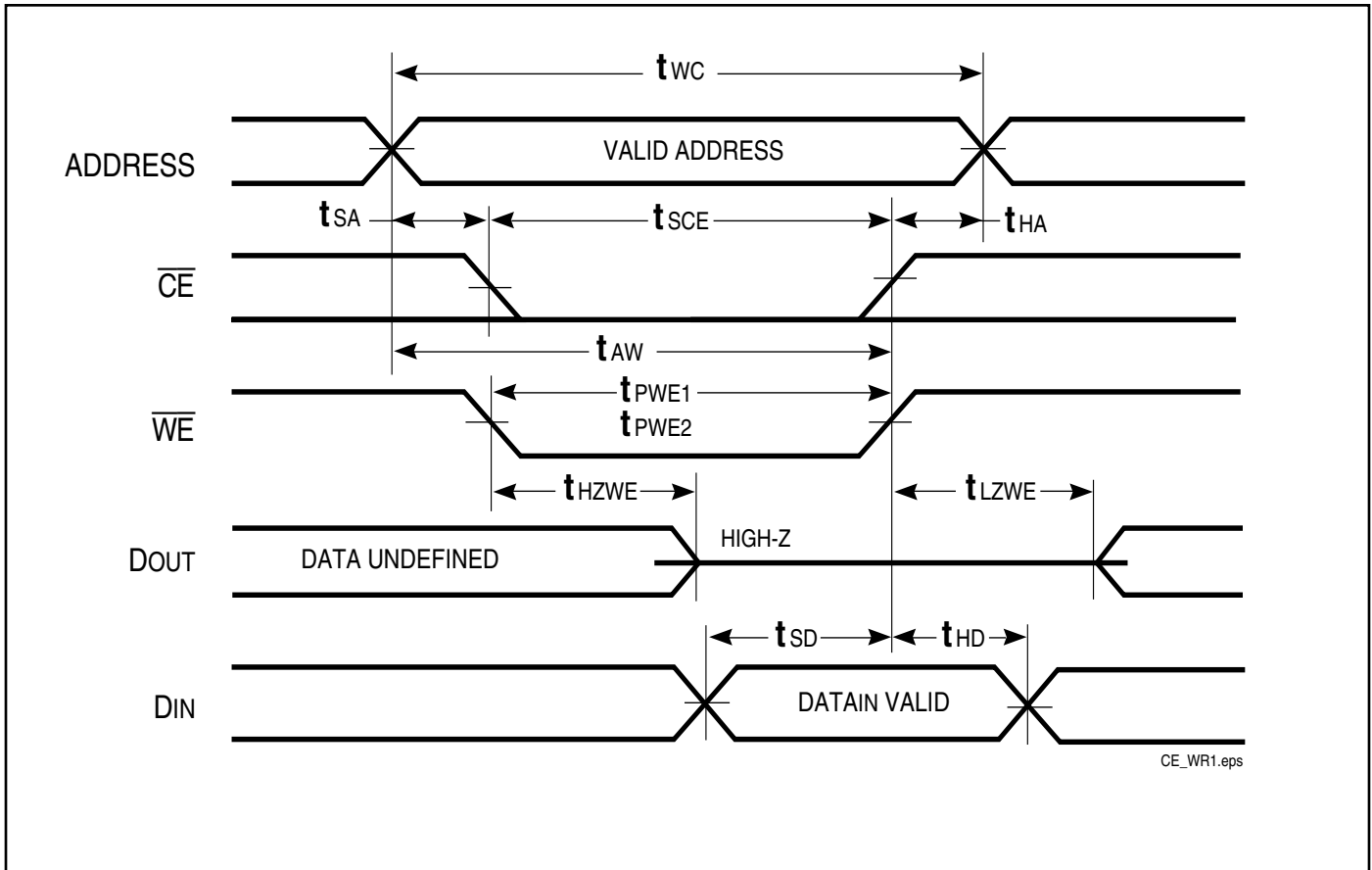
Symbol	Parameter	-20 ns		Unit
		Min.	Max.	
t _{WC}	Write Cycle Time	20	—	ns
t _{SCE}	\overline{CE} to Write End	12	—	ns
t _{AW}	Address Setup Time to Write End	12	—	ns
t _{HA}	Address Hold from Write End	0	—	ns
t _{SA}	Address Setup Time	0	—	ns
t _{PWB}	\overline{BWA} -d Valid to End of Write	12	—	ns
t _{PWE1}	\overline{WE} Pulse Width (\overline{OE} = HIGH)	12	—	ns
t _{PWE2}	\overline{WE} Pulse Width (\overline{OE} = LOW)	17	—	ns
t _{SD}	Data Setup to Write End	9	—	ns
t _{HD}	Data Hold from Write End	0	—	ns
t _{HZWE⁽³⁾}	\overline{WE} LOW to High-Z Output	—	9	ns
t _{LZWE⁽³⁾}	\overline{WE} HIGH to Low-Z Output	3	—	ns

Notes:

1. Test conditions assume signal transition times of 3ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 0.3V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

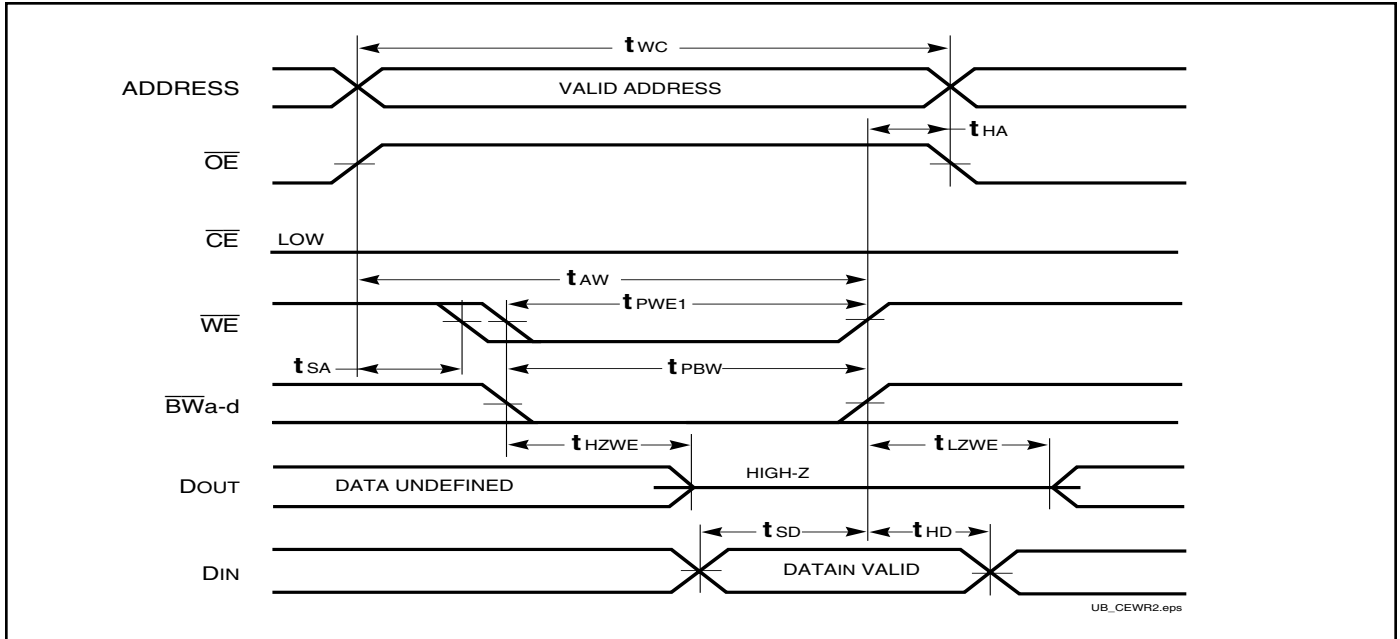
AC WAVEFORMS

WRITE CYCLE NO. 1^(1,2) (\overline{CE} Controlled, \overline{OE} = HIGH or LOW)

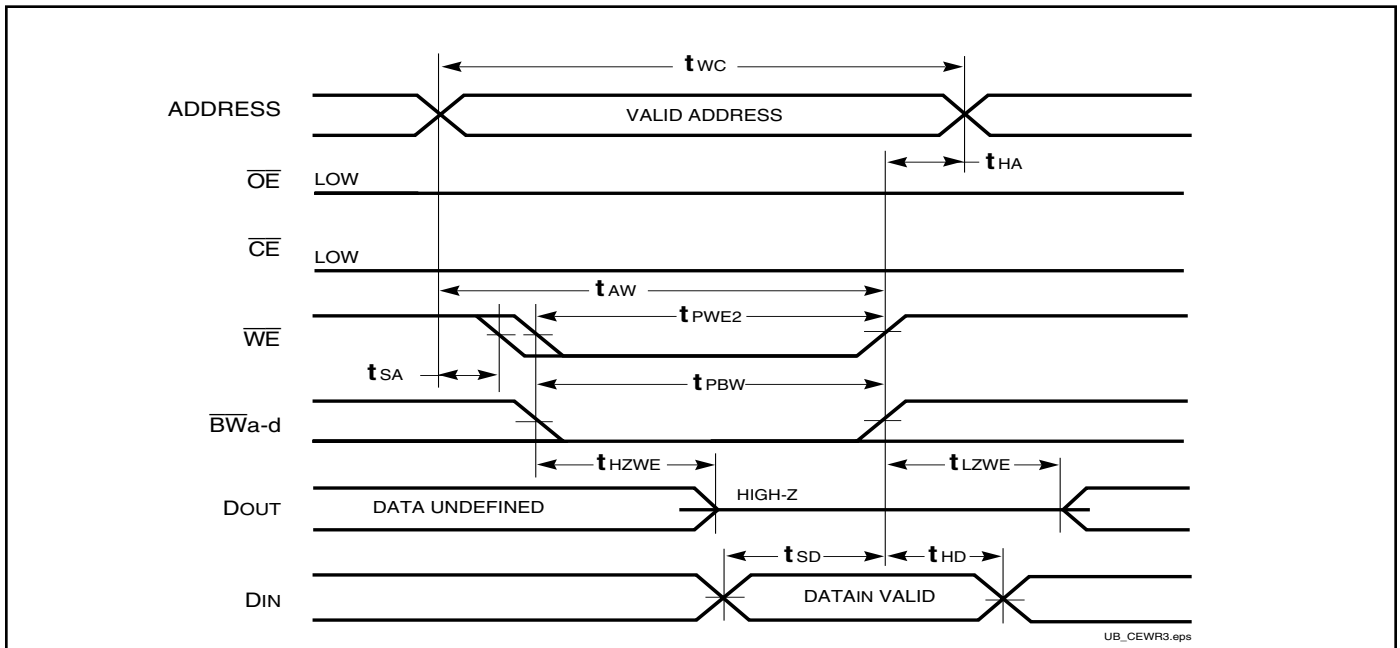


AC WAVEFORMS

WRITE CYCLE NO. 2 (\overline{WE} Controlled. \overline{OE} is HIGH During Write Cycle) ^(1,2)

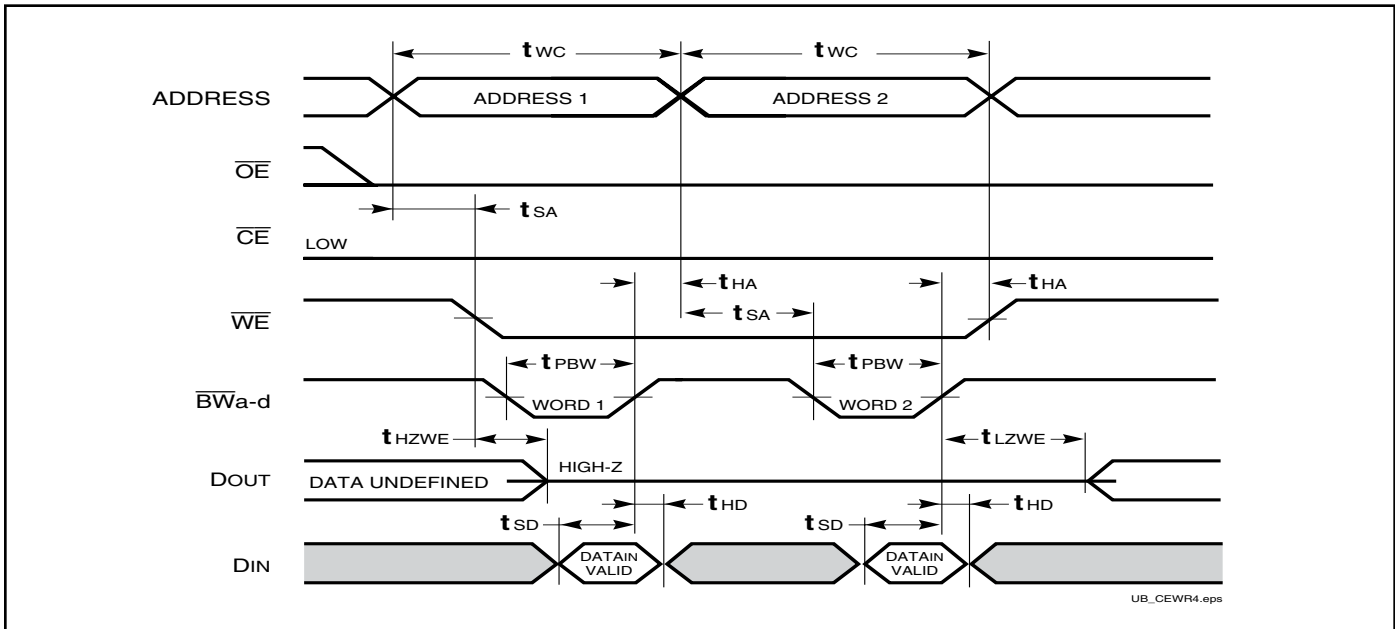


WRITE CYCLE NO. 3 (\overline{WE} Controlled. \overline{OE} is LOW During Write Cycle) ⁽¹⁾



AC WAVEFORMS

WRITE CYCLE NO. 4 (Byte Controlled, Back-to-Back Write) ^(1,3)



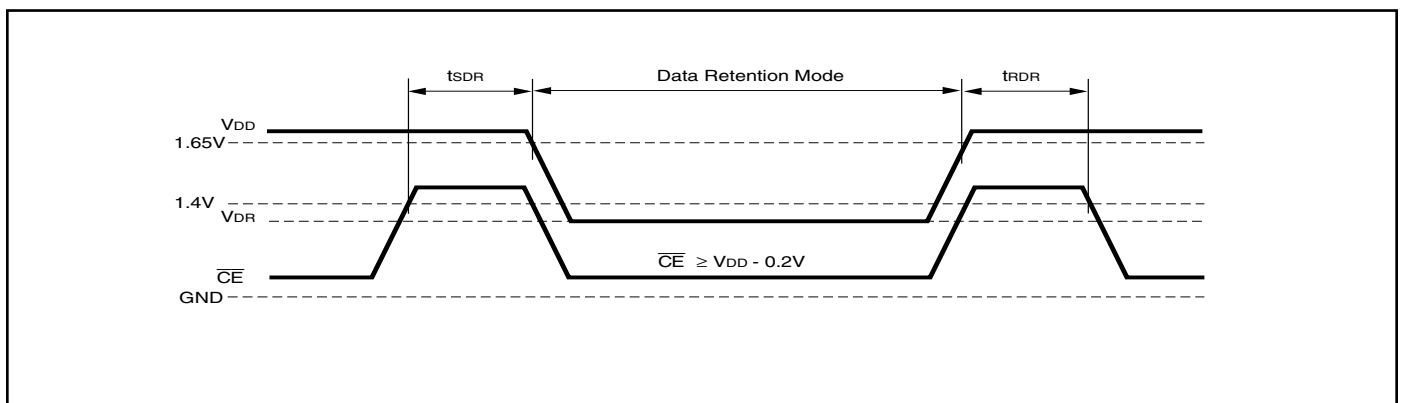
Notes:

1. The internal Write time is defined by the overlap of $\overline{WE} = \text{LOW}$. All signals must be in valid states to initiate a Write, but any can be deasserted to terminate the Write. The t_{SA} , t_{HA} , t_{SD} , and t_{HD} timing is referenced to the rising or falling edge of the signal that terminates the Write.
2. Tested with \overline{OE} HIGH for a minimum of 4 ns before $\overline{WE} = \text{LOW}$ to place the I/O in a HIGH-Z state.

DATA RETENTION SWITCHING CHARACTERISTICS (HIGH SPEED) (IS61WV25632ALL/BLL)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform	1.2	3.6	V
I_{DR}	Data Retention Current	$V_{DD} = 1.2V, \overline{CE} \geq V_{DD} - 0.2V$	Ind. Auto.	25 60	mA
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform	0	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform	t_{RC}	—	ns

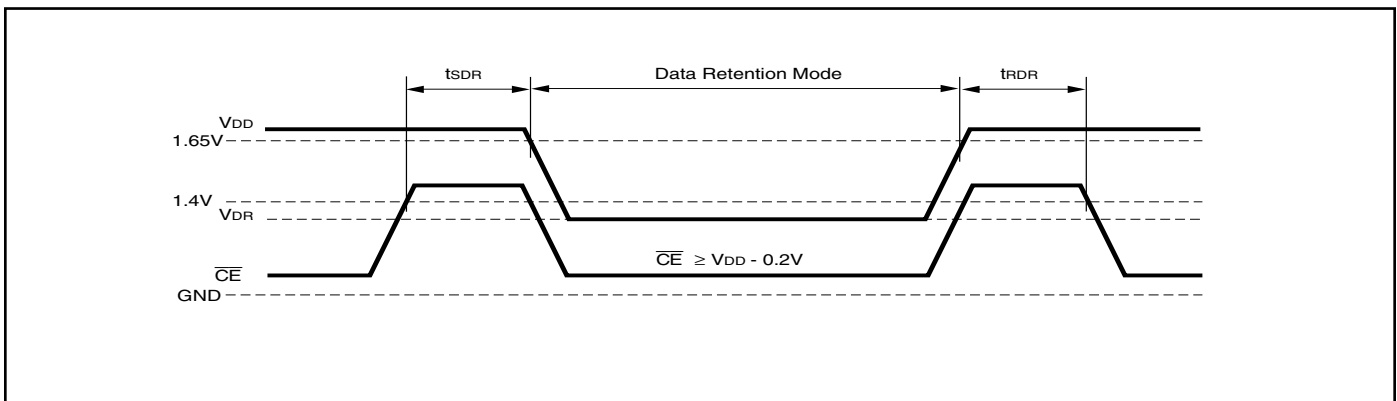
DATA RETENTION WAVEFORM (\overline{CE} Controlled)



DATA RETENTION SWITCHING CHARACTERISTICS (LOW POWER) (IS61WV25632ALS/BLS)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform	1.2	3.6	V
I_{DR}	Data Retention Current	$V_{DD} = 1.2V, \overline{CE} \geq V_{DD} - 0.2V$	Ind. Auto.	1.2 2	mA
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform	0	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform	t_{RC}	—	ns

DATA RETENTION WAVEFORM (\overline{CE} Controlled)



ORDERING INFORMATION

Industrial Range: -40°C to +85°C

Voltage Range: 2.4V to 3.6V

Speed (ns)	Order Part No.	Package
10 (8 ¹)	IS61WV25632BLL-10BI	90-ball BGA (8mm x 13mm)
	IS61WV25632BLL-10BLI	90-ball BGA (8mm x 13mm), Lead-free

Note:

1. Speed = 8ns for $V_{DD} = 3.3V \pm 5\%$. Speed = 10ns for $V_{DD} = 2.4V - 3.6V$

Industrial Range: -40°C to +85°C

Voltage Range: 1.65V to 2.2V

Speed (ns)	Order Part No.	Package
20	IS61WV25632ALL-20BI	90-ball BGA (8mm x 13mm)

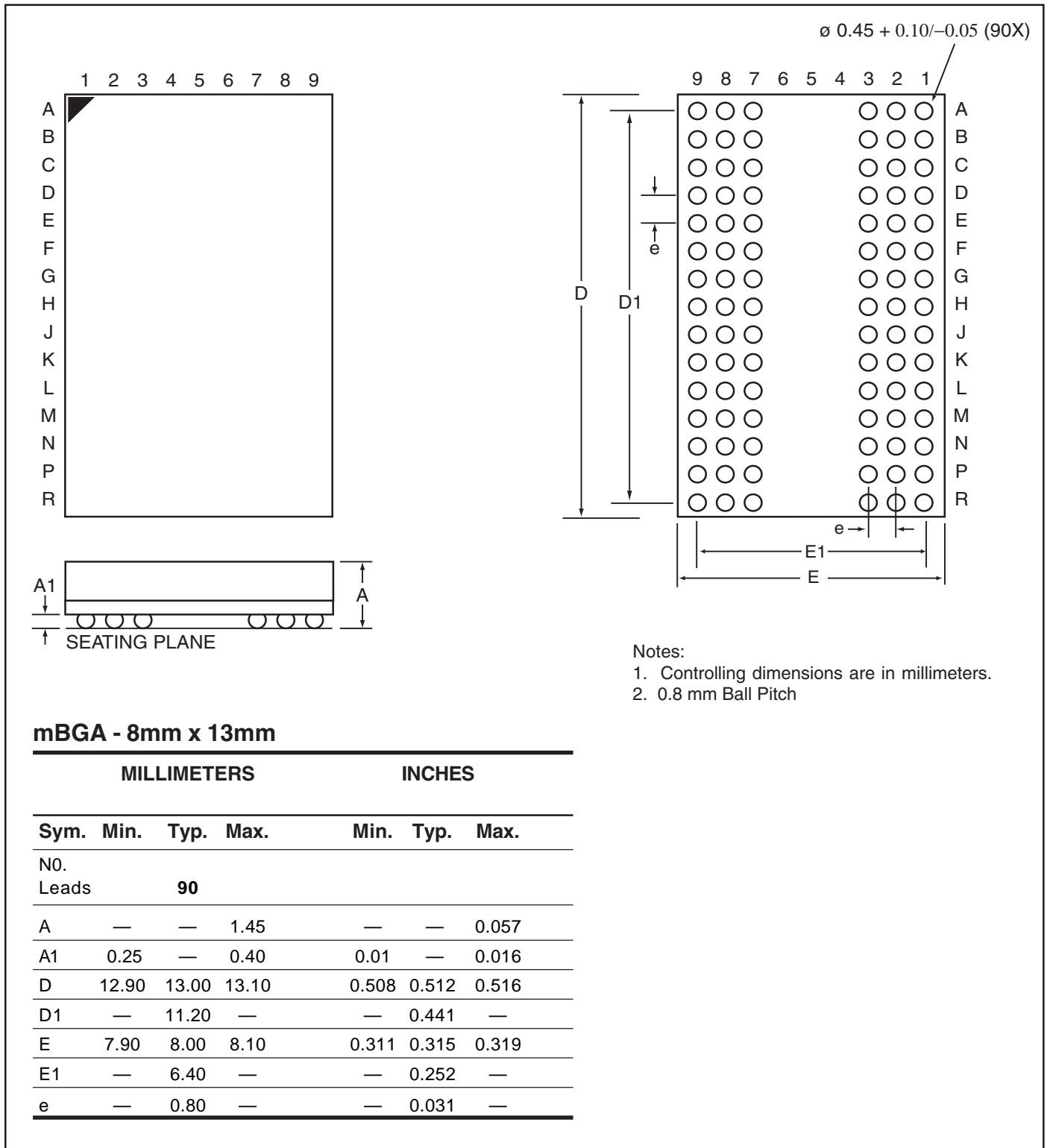
Automotive Range: -40°C to +125°C

Voltage Range: 2.4V to 3.6V

Speed (ns)	Order Part No.	Package
10	IS64WV25632BLL-10BA3	90-ball BGA (8mm x 13mm)

PACKAGING INFORMATION

Mini Ball Grid Array Package Code: B (90-Ball)



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