IS66WV25632ALL
IS66WV25632BLL

8Mb LOW VOLTAGE, ULTRA LOW POWER PSEUDO CMOS STATIC RAM

ADVANCED INFORMATION
SEPTEMBER 2007

FEATURES

- High-speed access time: 55ns
- CMOS low power operation
  - – mW (typical) operating
  - – µW (typical) CMOS standby
- Single power supply
  - – 1.7V--1.95V V_{DD} (66WV25632ALL) (70ns)
  - – 2.5V--3.6V V_{DD} (66WV25632BLL) (55ns)
- Three state outputs
- Data control for upper and lower bytes
- Industrial temperature available
- Lead-free available

DESCRIPTION

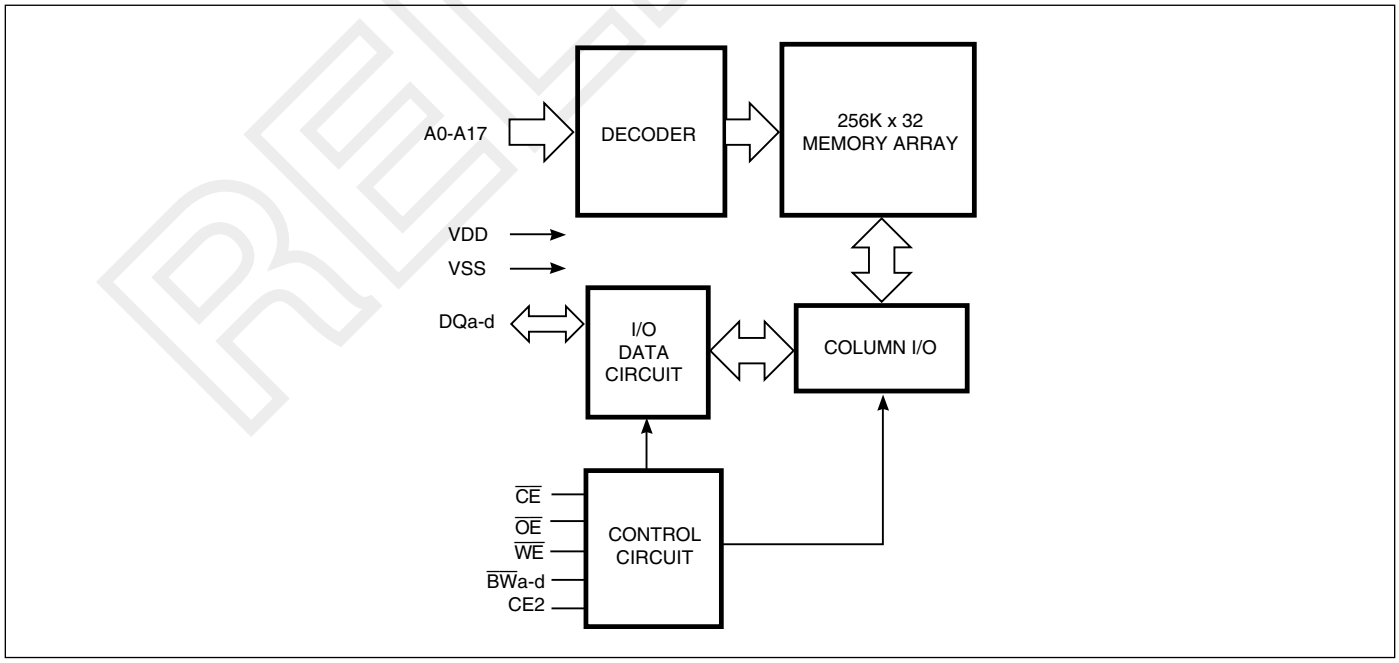
The *ISSI* IS66WV25632ALL/BLL is a high-speed, 8M bit static RAMs organized as 256K words by 32 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When $\overline{CS1}$ is HIGH (deselected) or when CS2 is LOW (deselected) or when $\overline{CS1}$ is LOW, CS2 is HIGH and both $\overline{LB}$ and $\overline{UB}$ are HIGH, the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory. A data byte allows Upper Byte ($\overline{UB}$) and Lower Byte ($\overline{LB}$) access.

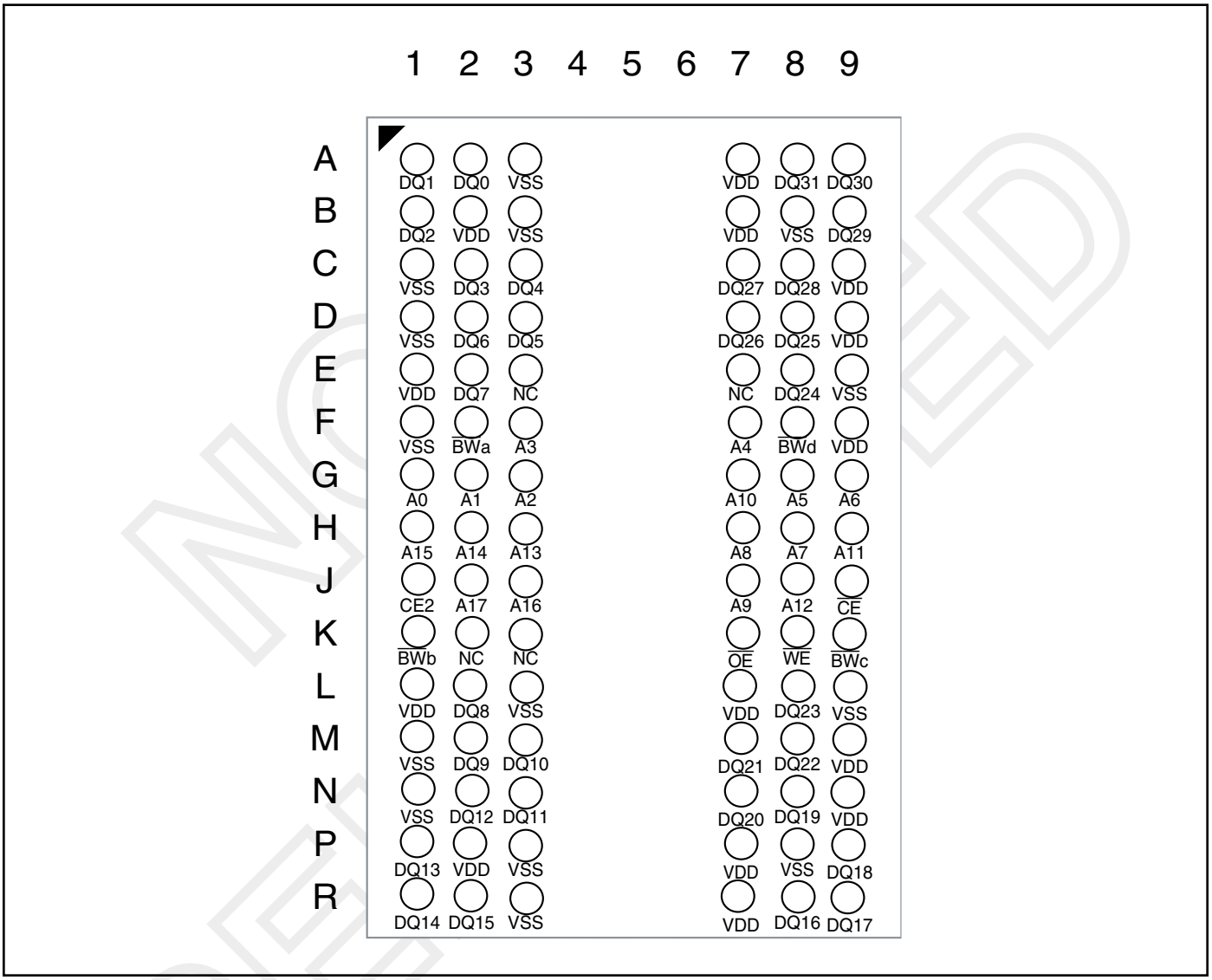
The IS66WV25632ALL/BLL is packaged in 90-ball mini BGA (8mm x 13mm). The device is also available for die sales.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

PACKAGE CODE: B 90 BALL FBGA (Top View) (8.00 mm x 13.00 mm Body, 0.8 mm Ball Pitch)



PIN DESCRIPTIONS

A0-A18	Address Inputs
DQx	Data I/O
$\overline{CE}$, CE2	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$\overline{BW}$x (x=a-d)	Byte Write Control
V_{DD}	Power
Vss	Ground
NC	No Connection

TRUTH TABLE

$\overline{CE}$	CE2	$\overline{OE}$	$\overline{WE}$	$\overline{BWa}$	$\overline{BWb}$	$\overline{BWc}$	$\overline{BWd}$	DQ_{0-7}	DQ_{8-15}	DQ_{16-23}	DQ_{24-31}	Mode	Power
H	X	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Power Down	(I_{SB})
X	L	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Power Down	(I_{SB})
L	H	L	H	L	L	L	L	Data Out	Data Out	Data Out	Data Out	Read All Bits	(I_{CC})
L	H	L	H	L	H	H	H	Data Out	High-Z	High-Z	High-Z	Read Byte a Bits Only	(I_{CC})
L	H	L	H	H	L	H	H	High-Z	Data Out	High-Z	High-Z	Read Byte b Bits Only	(I_{CC})
L	H	L	H	H	H	L	H	High-Z	High-Z	Data Out	High-Z	Read Byte c Bits Only	(I_{CC})
L	H	L	H	H	H	H	L	High-Z	High-Z	High-Z	Data Out	Read Byte d Bits Only	(I_{CC})
L	H	X	L	L	L	L	L	Data In	Data In	Data In	Data In	Write All Bits	(I_{CC})
L	H	X	L	L	H	H	H	Data In	High-Z	High-Z	High-Z	Write Byte a Bits Only	(I_{CC})
L	H	X	L	H	L	H	H	High-Z	Data In	High-Z	High-Z	Write Byte b Bits Only	(I_{CC})
L	H	X	L	H	H	L	H	High-Z	High-Z	Data In	High-Z	Write Byte c Bits Only	(I_{CC})
L	H	X	L	H	H	H	L	High-Z	High-Z	High-Z	Data In	Write Byte d Bits Only	(I_{CC})
L	H	H	H	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Selected, Outputs Disabled	(I_{CC})

OPERATING RANGE (V_{DD})

Range	Ambient Temperature	(70ns)	(55ns)	(70ns)
Commercial	0°C to +70°C	1.7V - 1.95V	2.5V - 3.6V	
Industrial	–40°C to +85°C	1.7V - 1.95V	2.5V - 3.6V	
Automotive	–40°C to +105°C			2.5V-3.6V

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.2 to V_{DD}+0.3	V
T_{BIAS}	Temperature Under Bias	–40 to +85	°C
V_{DD}	V_{DD} Related to GND	–0.2 to +3.8	V
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	V_{DD}	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -0.1 mA	1.7-1.95V	1.4	—	V
		I_{OH} = -1 mA	2.5-3.6V	2.2	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	1.7-1.95V	—	0.2	V
		I_{OL} = 2.1 mA	2.5-3.6V	—	0.4	V
V_{IH}	Input HIGH Voltage		1.7-1.95V	1.4	V_{DD} + 0.2	V
			2.5-3.6V	2.2	V_{DD} + 0.3	V
V_{IL}[1]	Input LOW Voltage		1.7-1.95V	–0.2	0.4	V
			2.5-3.6V	–0.2	0.6	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}		–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled		–1	1	µA

Notes:
1. V_{IL} (min.) = –1.0V for pulse width less than 10 ns.

CAPACITANCE[1]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	10	pF

Note:
1. Tested initially and after any design or process changes that may affect these parameters.

AC TEST CONDITIONS

Parameter	1.7V-1.95V (Unit)	2.5V-3.6V (Unit)
Input Pulse Level	0.4V to V_{DD}-0.2	0.4V to V_{DD}-0.3V
Input Rise and Fall Times	5 ns	5ns
Input and Output Timing and Reference Level	V_{REF}	V_{REF}
Output Load	See Figures 1 and 2	See Figures 1 and 2

	1.7V - 1.95V	2.5V - 3.6V
R1(Ω)	3070	1029
R2(Ω)	3150	1728
V_{REF}	0.9V	1.4V
V_{TM}	1.8V	2.8V

AC TEST LOADS

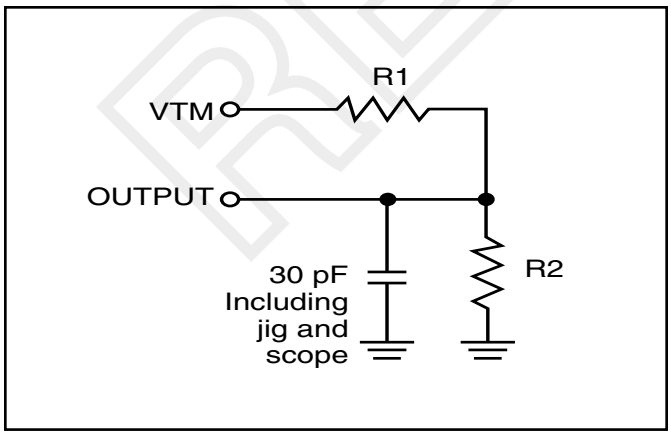


Figure 1

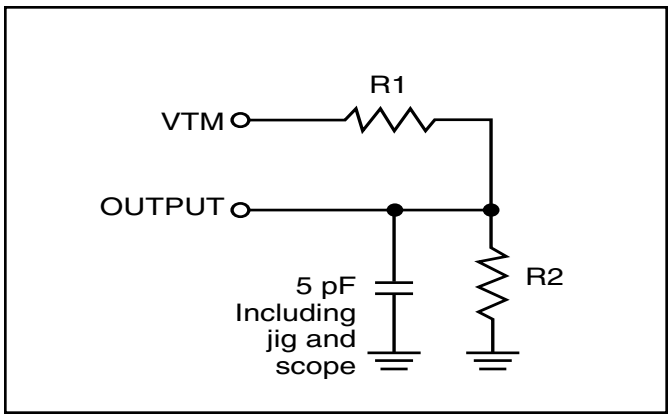


Figure 2

1.7V-1.95V POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		Max. 70ns	Unit
I_{CC}	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} All Inputs 0.4V or V_{DD} – 0.2V	Com.	20	mA
			Ind.	25	
			Auto.	30	
			typ.[1]		
I_{CC1}	Operating Supply Current	V_{DD} = Max., $\overline{CS1}$ = 0.2V $\overline{WE}$ = V_{DD} – 0.2V	Com.	4	mA
			Ind.	4	
		CS2 = V_{DD} – 0.2V, f = 1MHz	Auto.	10	
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{DD} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CS1}$ = V_{IH} , CS2 = V_{IL}, f = 1 MHz	Com.	0.6	mA
			Ind.	0.6	
			Auto.	1	
	OR				
	ULB Control	V_{DD} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CS1}$ = V_{IL}, f = 0, $\overline{UB}$ = V_{IH}, $\overline{LB}$ = V_{IH}			
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max., $\overline{CS1}$ ≥ V_{DD} – 0.2V, CS2 ≤ 0.2V, V_{IN} ≥ V_{DD} – 0.2V, or V_{IN} ≤ 0.2V, f = 0	Com.	150	µA
			Ind.	180	
			Auto.	200	
			typ.[1]		
	OR				
	ULB Control	V_{DD} = Max., $\overline{CS1}$ = V_{IL}, CS2=V_{IH} V_{IN} ≥ V_{DD} – 0.2V, or V_{IN} ≤ 0.2V, f = 0; $\overline{UB}$ / $\overline{LB}$ = V_{DD} – 0.2V			

Note:.
1. Typical values are measured at V_{DD} = 1.8V, T_A = 25°C and not 100% tested.

2.5V-3.6V POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		Max. 55ns	Unit
I_{CC}	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} All Inputs 0.4V or V_{DD} – 0.3V	Com.	25	mA
			Ind.	28	
			Auto.	35	
			typ.[2]	15	
I_{CC1}	Operating Supply Current	V_{DD} = Max., $\overline{CS1}$ = 0.2V $\overline{WE}$ = V_{DD} – 0.2V CS2 = V_{DD} – 0.2V, f = 1MHz	Com.	5	mA
			Ind.	5	
			Auto.	10	
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{DD} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CS1}$ = V_{IH} , CS2 = V_{IL}, f = 1 MHz	Com.	0.6	mA
			Ind.	0.6	
			Auto.	1	
	OR				
	ULB Control	V_{DD} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CS1}$ = V_{IL}, f = 0, $\overline{UB}$ = V_{IH}, $\overline{LB}$ = V_{IH}			
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max., $\overline{CS1}$ ≥ V_{DD} – 0.2V, CS2 ≤ 0.2V, V_{IN} ≥ V_{DD} – 0.2V, or V_{IN} ≤ 0.2V, f = 0	Com.	150	µA
			Ind.	180	
			Auto.	200	
			typ.[2]	75	
	OR				
	ULB Control	V_{DD} = Max., $\overline{CS1}$ = V_{IL}, CS2=V_{IH} V_{IN} ≥ V_{DD} – 0.2V, or V_{IN} ≤ 0.2V, f = 0; $\overline{UB}$ / $\overline{LB}$ = V_{DD} – 0.2V			

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

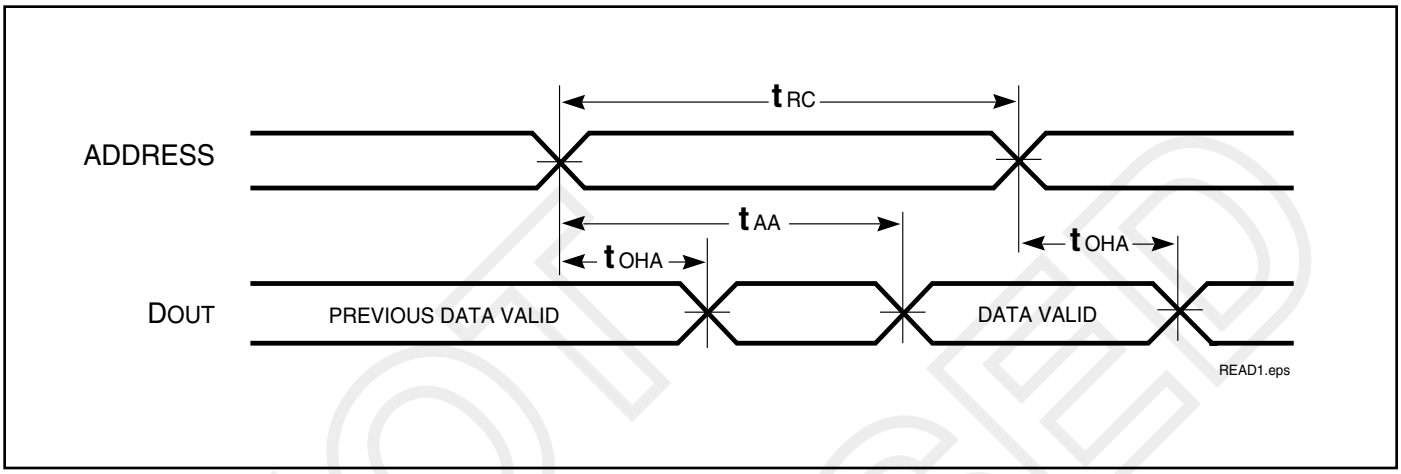
READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	55 ns Min.	55 ns Max.	70 ns Min.	70 ns Max.	Unit
t_{RC}	Read Cycle Time	55	—	70	—	ns
t_{AA}	Address Access Time	—	55	—	70	ns
t_{OHA}	Output Hold Time	10	—	10	—	ns
t_{ACS1}/t_{ACS2}	$\overline{CS1}$/CS2 Access Time	—	55	—	70	ns
t_{DOE}	$\overline{OE}$ Access Time	—	25	—	35	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	—	20	—	25	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	5	—	5	—	ns
t_{HZCS1}/t_{HZCS2}[2]	$\overline{CS1}$/CS2 to High-Z Output	0	20	0	25	ns
t_{LZCS1}/t_{LZCS2}[2]	$\overline{CS1}$/CS2 to Low-Z Output	10	—	10	—	ns
t_{BA}	$\overline{LB}$, $\overline{UB}$ Access Time	—	55	—	70	ns
t_{HZB}	$\overline{LB}$, $\overline{UB}$ to High-Z Output	0	20	0	25	ns
t_{LZB}	$\overline{LB}$, $\overline{UB}$ to Low-Z Output	0	—	0	—	ns

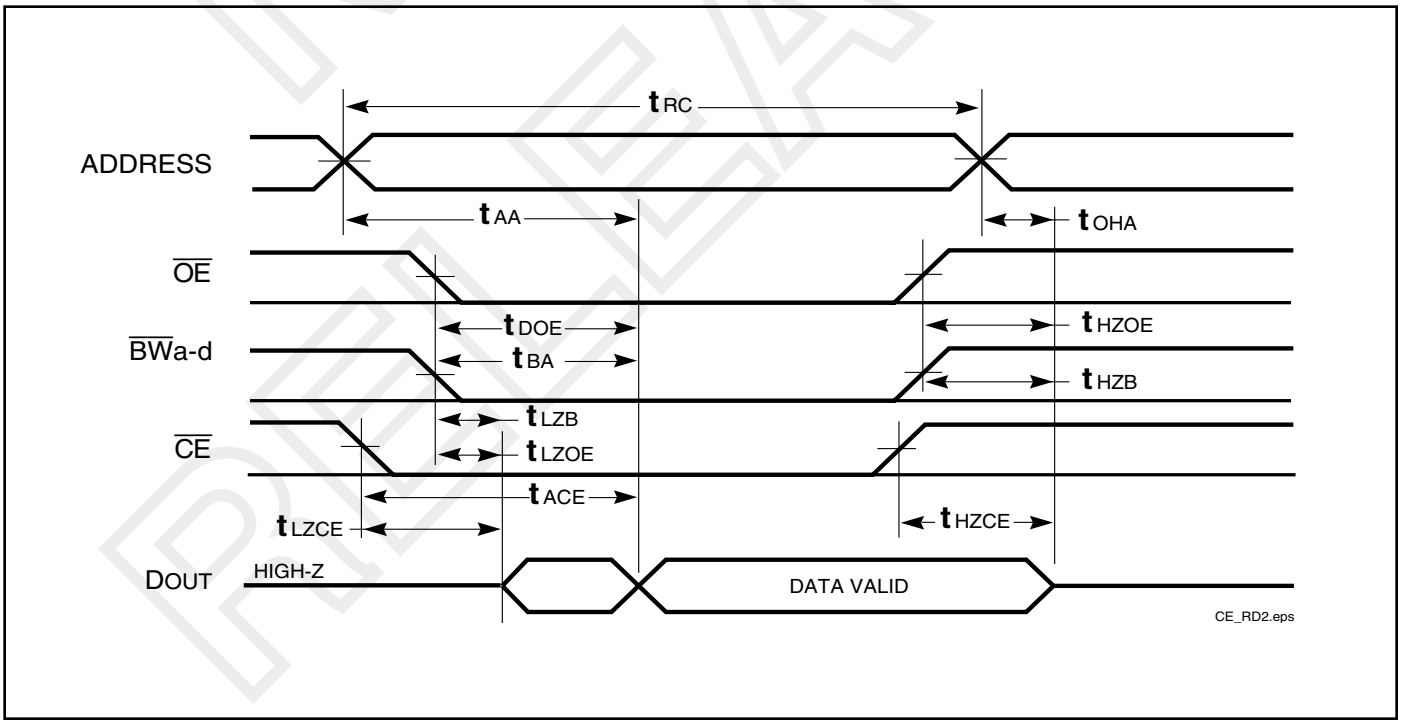
Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0.4 to V_{DD}-0.2V/0.4V to V_{DD}-0.3V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±100 mV from steady-state voltage. Not 100% tested.

AC WAVEFORMS

READ CYCLE NO. 1[1,2] (Address Controlled) ($\overline{CE}$ = $\overline{OE}$ = V_{IL})



READ CYCLE NO. 2[1,3] ($\overline{CE}$ and $\overline{OE}$ Controlled)



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.

WRITE CYCLE SWITCHING CHARACTERISTICS[1,2] (Over Operating Range)

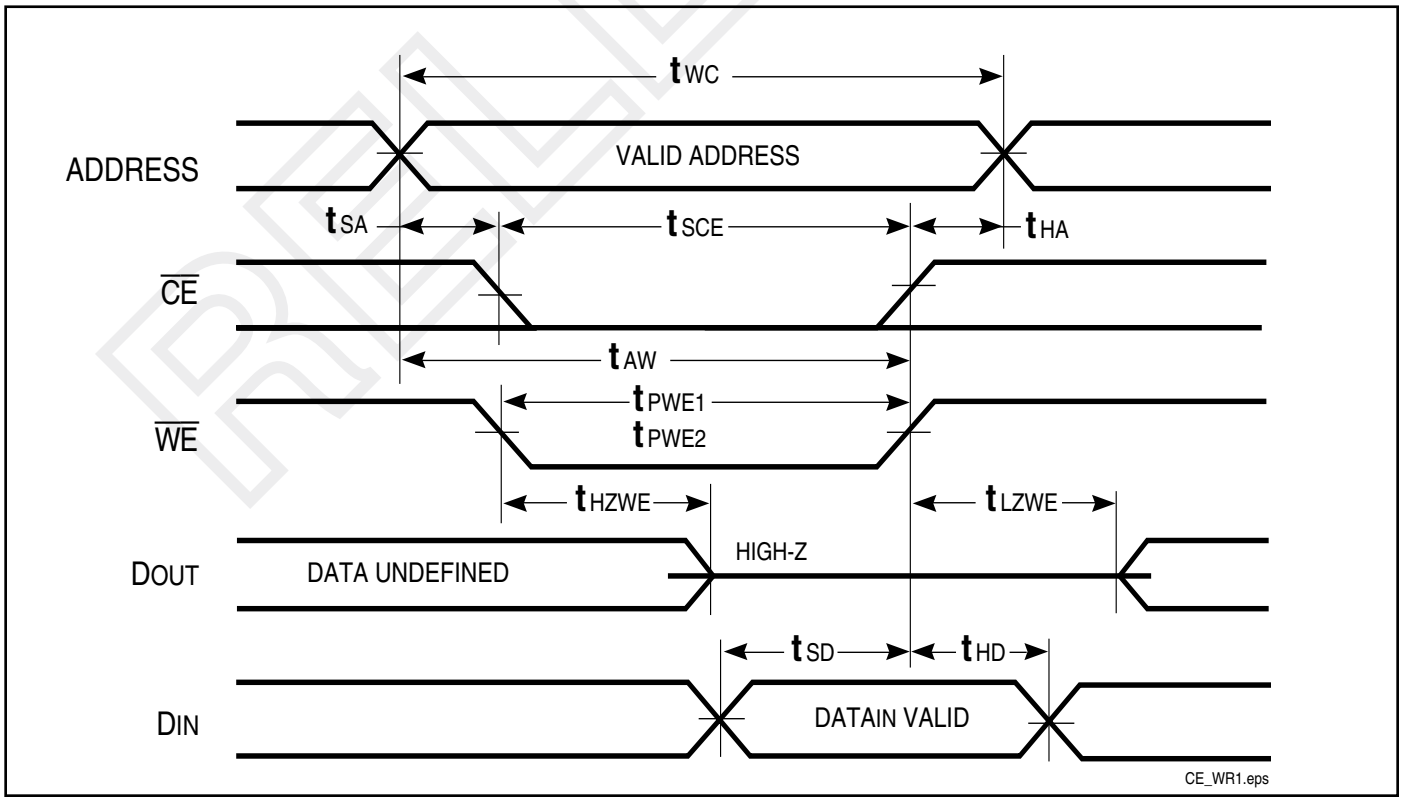
Symbol	Parameter	55 ns Min.	55 ns Max.	70 ns Min.	70 ns Max.	Unit
t_{WC}	Write Cycle Time	55	—	70	—	ns
t_{SCS1}/t_{SCS2}	$\overline{CS1}$/CS2 to Write End	45	—	60	—	ns
t_{AW}	Address Setup Time to Write End	45	—	60	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	ns
t_{PWB}	$\overline{LB}$, $\overline{UB}$ Valid to End of Write	45	—	60	—	ns
t_{PWE}[4]	$\overline{WE}$ Pulse Width	45	—	60	—	ns
t_{SD}	Data Setup to Write End	25	—	30	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	ns
t_{HZWE}[3]	$\overline{WE}$ LOW to High-Z Output	—	20	—	30	ns
t_{LZWE}[3]	$\overline{WE}$ HIGH to Low-Z Output	5	—	5	—	ns

Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0.4 to V_{DD}-0.2V/0.4V to V_{DD}-0.3V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of $\overline{CS1}$ LOW, CS2 HIGH and $\overline{UB}$ or $\overline{LB}$, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured ±100 mV from steady-state voltage. Not 100% tested.
4. $t_{PWE} > t_{HZWE} + t_{SD}$ when $\overline{OE}$ is LOW.

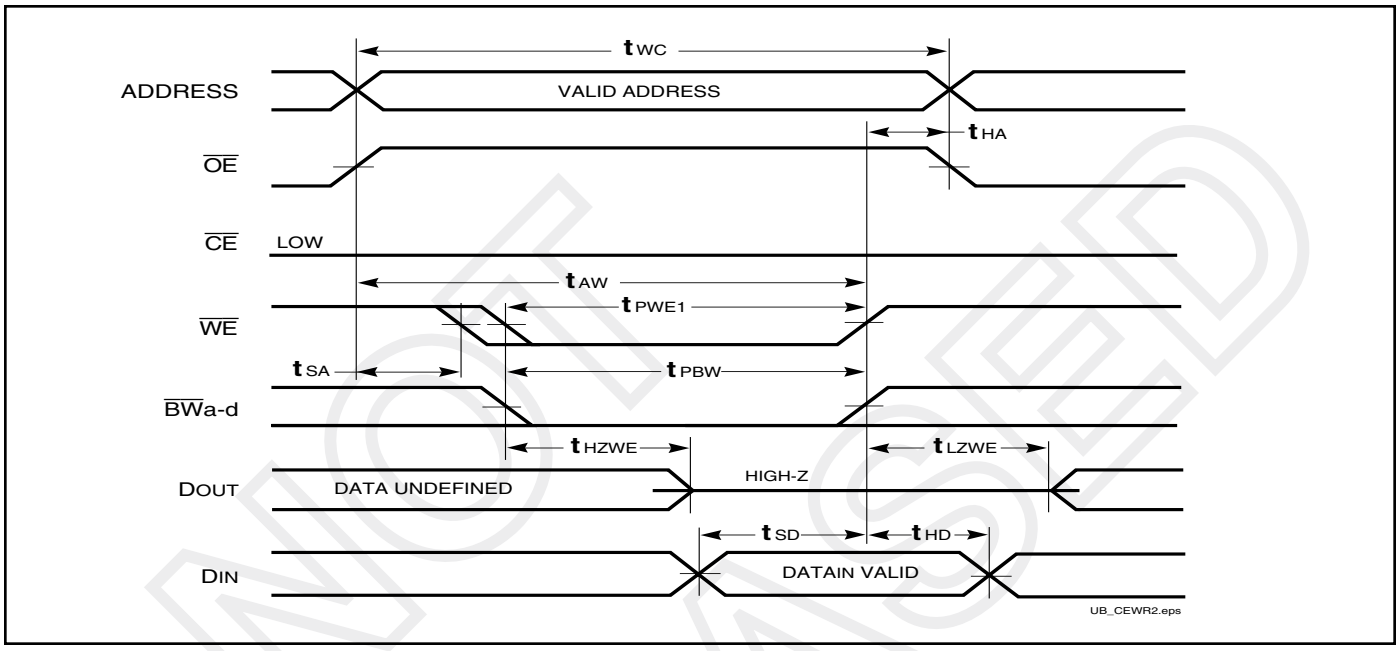
AC WAVEFORMS

WRITE CYCLE NO. 1[1,2] ($\overline{CE}$ Controlled, $\overline{OE}$ = HIGH or LOW)

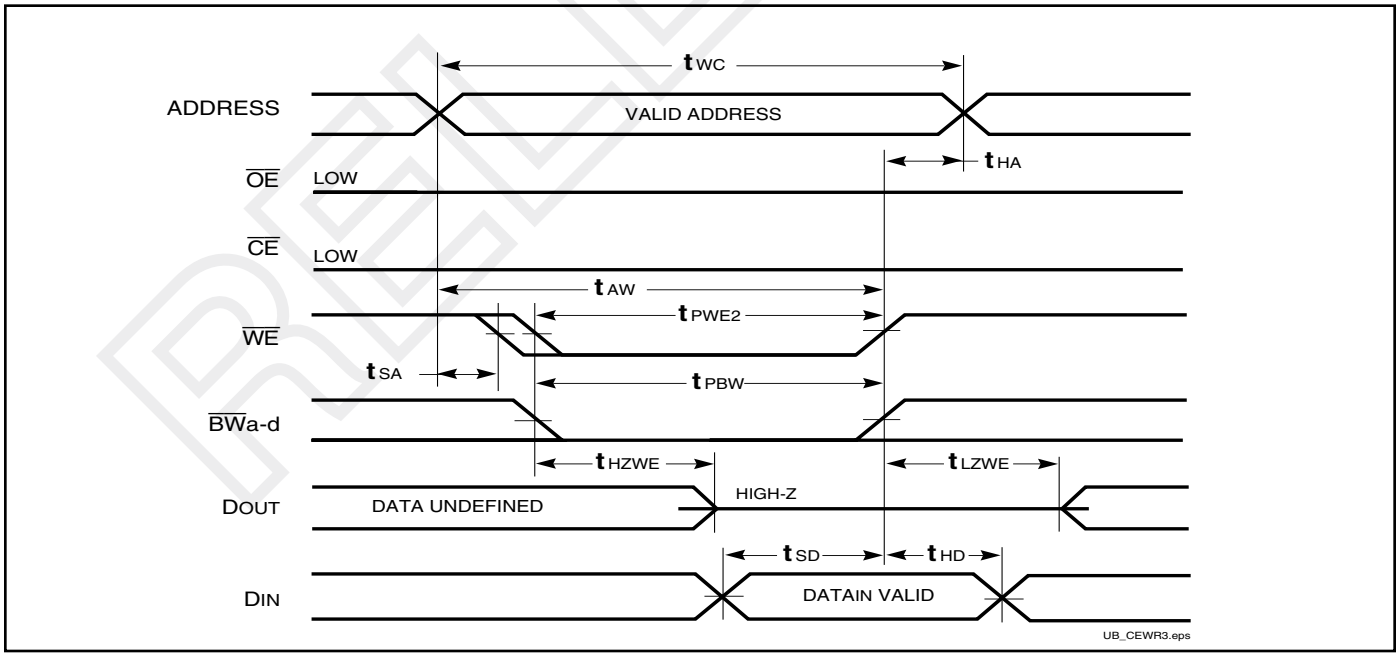


AC WAVEFORMS

WRITE CYCLE NO. 2 ($\overline{WE}$ Controlled. $\overline{OE}$ is HIGH During Write Cycle) [1,2]

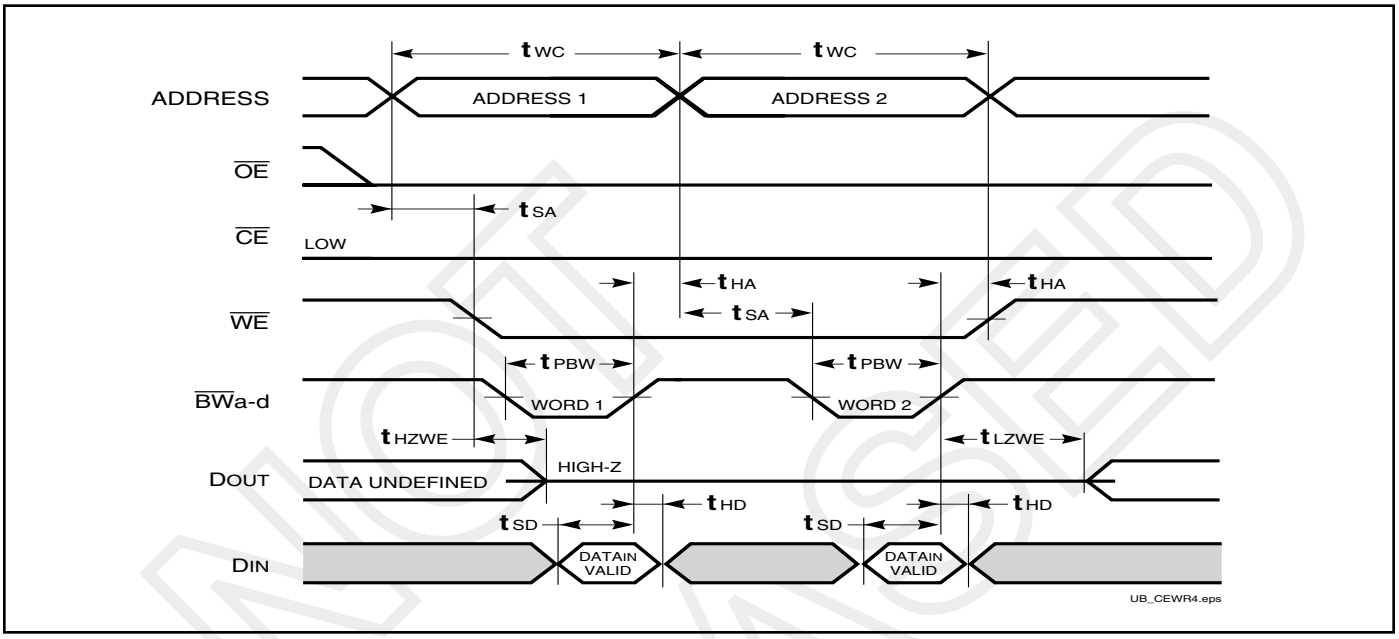


WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled. $\overline{OE}$ is LOW During Write Cycle) [1]



AC WAVEFORMS

WRITE CYCLE NO. 4 (Byte Controlled, Back-to-Back Write) [1,3]



Notes:

1. The internal Write time is defined by the overlap of and $\overline{WE}$ = LOW. All signals must be in valid states to initiate a Write, but any can be deasserted to terminate the Write. The t_{SA}, t_{HA}, t_{SD}, and t_{HD} timing is referenced to the rising or falling edge of the signal that terminates the Write.
2. Tested with $\overline{OE}$ HIGH for a minimum of 4 ns before $\overline{WE}$ = LOW to place the I/O in a HIGH-Z state.
3. $\overline{WE}$ may be held LOW across many address cycles and the $\overline{BW}$a-d pins can be used to control the Write function.

Figure 1: **Avoidable Timing**

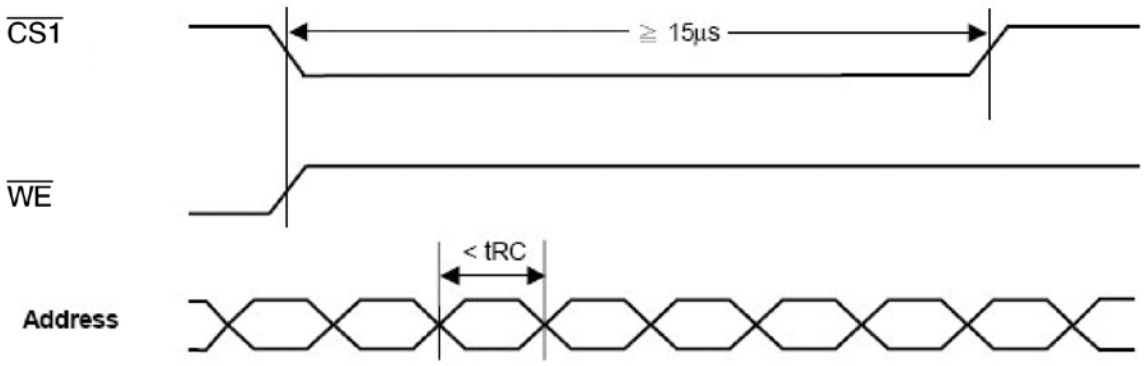


Figure 2:

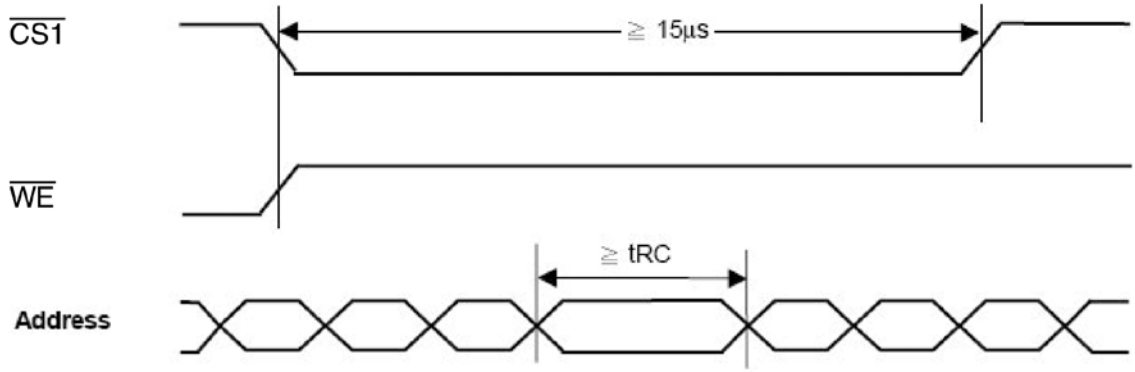
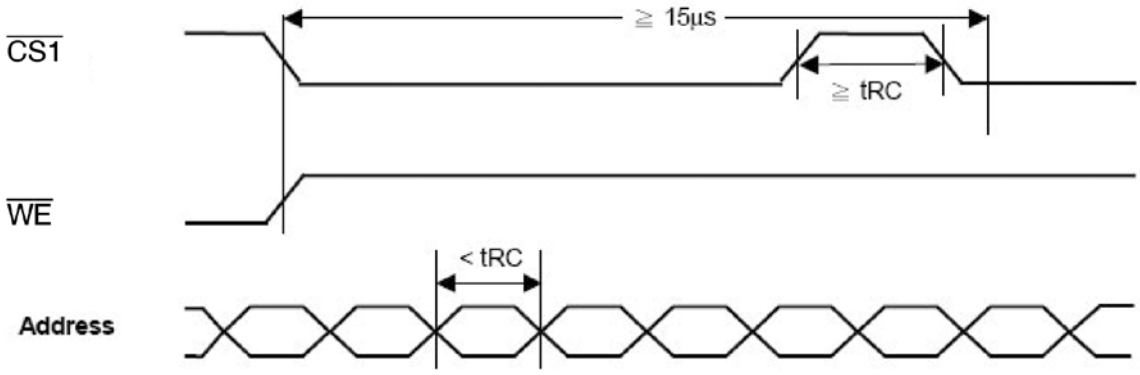


Figure 3:



Please avoid address change for less than t_{RC} during the cycle time longer than 15 µs (Figure 1). Figure 2 & 3 provide work around solution for this issue.

IS66WV25632ALL

Industrial Range: -40°C to +85°C
Voltage Range: 1.7V to 1.95V

Speed (ns)	Order Part No.	Package
70	IS66WV25632ALL-70BLI	mini BGA (8mm x 13mm), Lead-free

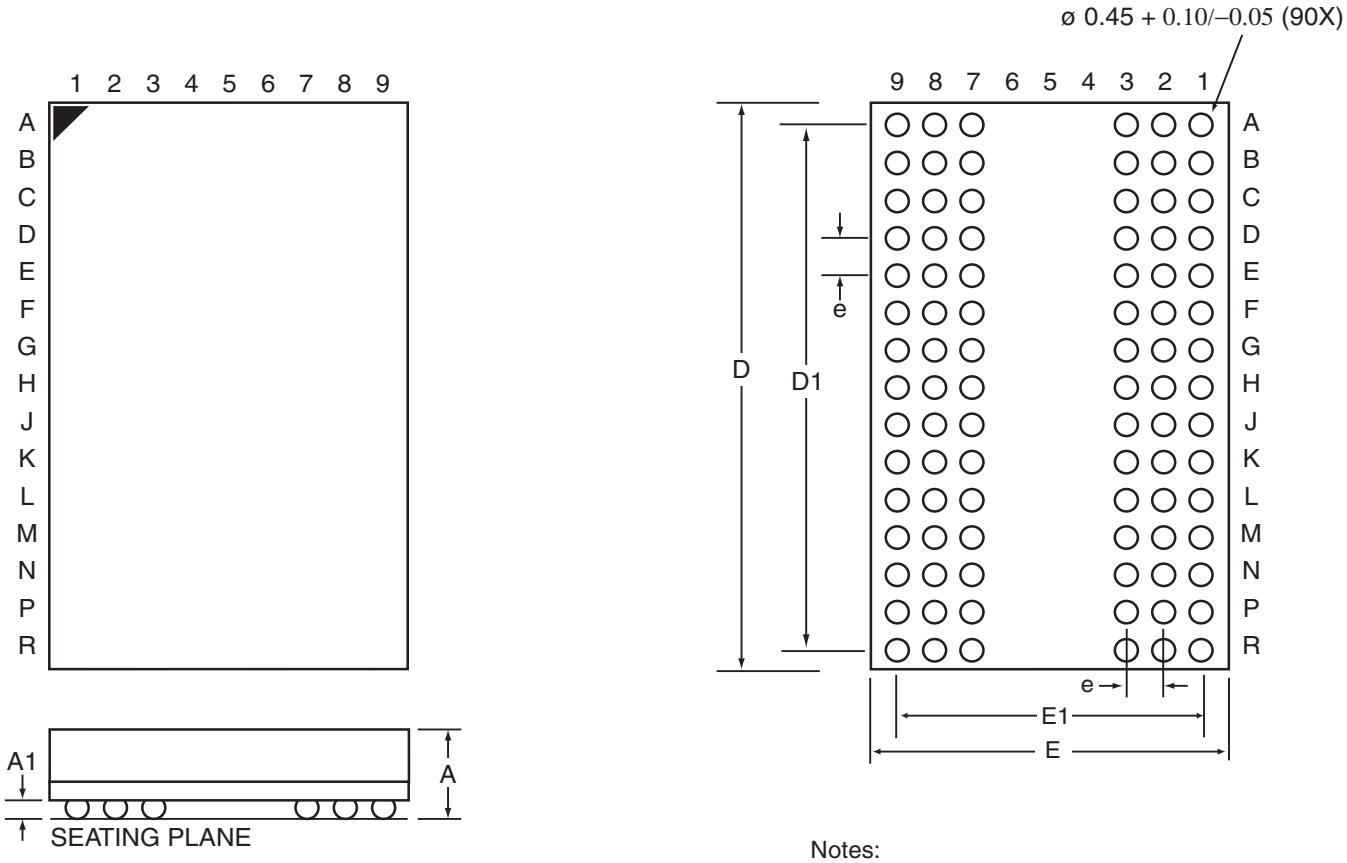
IS66WV25632BLL

Commercial Range: 0°C to +70°C
Voltage Range: 2.5V to 3.6V

Speed (ns)	Order Part No.	Package
55	IS66WV25632BLL-55BLI	mini BGA (8mm x 13mm), Lead-free

PACKAGING INFORMATION

Mini Ball Grid Array
Package Code: B (90-Ball)



Notes:
1. Controlling dimensions are in millimeters.
2. 0.8 mm Ball Pitch

mBGA - 8mm x 13mm

	MILLIMETERS			INCHES		
Sym.	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
N0. Leads		**90**				
A	—	—	1.45	—	—	0.057
A1	0.25	—	0.40	0.01	—	0.016
D	12.90	13.00	13.10	0.508	0.512	0.516
D1	—	11.20	—	—	0.441	—
E	7.90	8.00	8.10	0.311	0.315	0.319
E1	—	6.40	—	—	0.252	—
e	—	0.80	—	—	0.031	—