



# ISD1200 Series

## Single-Chip Voice Record/Playback Devices

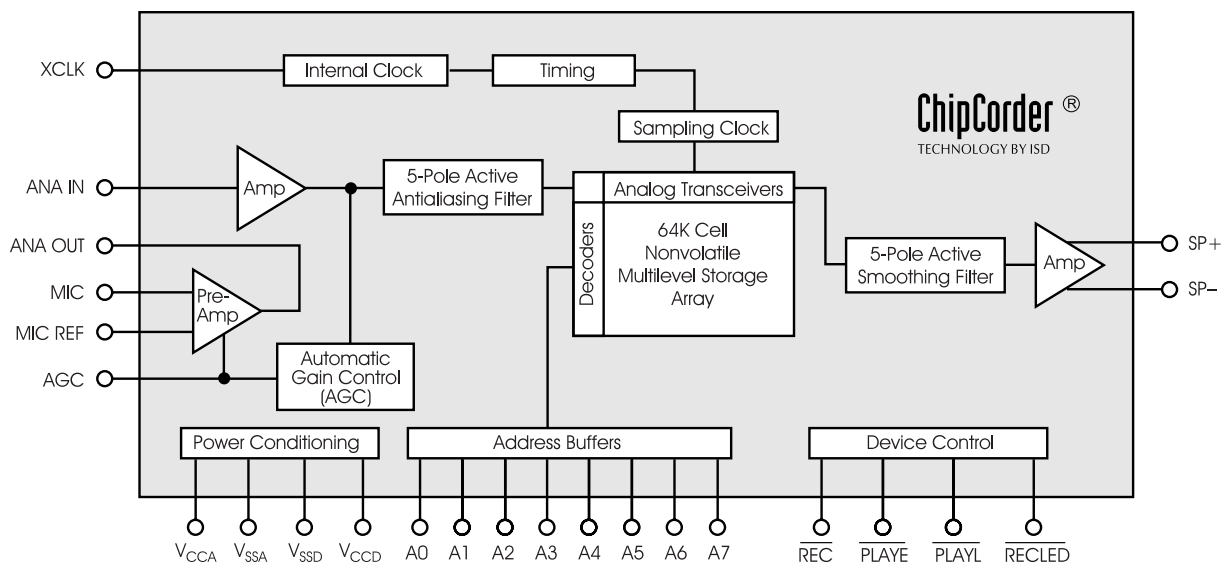
### 10- and 12-Second Durations

#### GENERAL DESCRIPTION

Information Storage Devices' ISD1200 ChipCorder® series provides high-quality, single-chip record/playback solutions to 10- and 12-second messaging applications. The CMOS devices include an on-chip oscillator, microphone preamplifier, automatic gain control, antialiasing filter, smoothing filter, and speaker amplifier. A minimum Record/Playback subsystem can be configured with a microphone, a speaker, several passives, two push-buttons, and a power source.

Recordings are stored in on-chip nonvolatile memory cells, providing zero-power message storage. This unique, single-chip solution is made possible through ISD's patented multilevel storage technology. Voice and audio signals are stored directly into memory in their natural form, providing high-quality, solid-state voice reproduction.

Figure: ISD1200 Series Block Diagram



**FEATURES**

- Easy-to-use single-chip voice record/playback solution
- High-quality, natural voice/audio reproduction
- Push-button interface
  - Playback can be edge- or level-activated
- Single-chip durations of 10 and 12 seconds
- Automatic power-down mode
  - Enters standby mode immediately following a record or playback cycle
  - Standby current 0.5  $\mu$ A (typical)
- Zero-power message storage
  - Eliminates battery backup circuits
- Fully addressable to handle multiple messages
- 100-year message retention (typical)
- 100,000 record cycles (typical)
- On-chip clock source
- No programmer or development system needed
- Single +5 volt power supply
- Available in die form, DIP, and SOIC packaging

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**Table: ISD1200 Series Summary**

<b>Part Number</b>	<b>Minimum Duration (Seconds)</b>	<b>Input Sample Rate (KHz)</b>	<b>Typical Filter Pass Band (KHz)</b>
ISD1210	10	6.4	2.6
ISD1212	12	5.3	2.2

# Table of Contents

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## ISD1200 Series

Single-Chip Voice Record/Playback Devices  
10- and 12-Second Durations

DETAILED DESCRIPTION	1
Speech/Sound Quality	1
Duration	1
EEPROM Storage	1
Basic Operation	1
Automatic Power-Down Mode	1
Addressing (optional)	1
PIN DESCRIPTIONS	2
Voltage Inputs ( $V_{CCA}$ , $V_{CCD}$ )	2
Ground Inputs ( $V_{SSA}$ , $V_{SSD}$ )	2
Record ( $\overline{REC}$ )	2
Playback, Edge-Activated ( $\overline{PLAYE}$ )	2
Playback, Level-Activated ( $\overline{PLAYL}$ )	2
Record LED Output ( $\overline{RECLD}$ )	3
Microphone Input (MIC)	3
Microphone Reference (MIC REF)	3
Automatic Gain Control (AGC)	3
Analog Output (ANA OUT)	3
Analog Input (ANA IN)	3
External Clock Input (XCLK)	3
Speaker Outputs (SP+, SP-)	4
Address Inputs (A0–A7)	4
OPERATIONAL MODES	4
OPERATIONAL MODES DESCRIPTION	5
A0 — Message Cueing	5
A1 — Delete EOM Markers	5
A2 — Unused	5
A3 — Message Looping	5
A4 — Consecutive Addressing	5
A5 — Unused	5
TIMING DIAGRAMS	6
TYPICAL PARAMETER VARIATION WITH VOLTAGE AND TEMPERATURE (PACKAGED PARTS)	10
TYPICAL PARAMETER VARIATION WITH VOLTAGE AND TEMPERATURE (DIE)	14
FUNCTIONAL DESCRIPTION EXAMPLE	15
APPLICATIONS NOTE	16
ISD1200 SERIES PHYSICAL DIMENSIONS	17
ORDERING INFORMATION	21

## FIGURES, CHARTS, AND TABLES IN THE ISD1200 SERIES DATASHEET

Figure 1:	ISD1200 Series Pinouts	2
Figure 2:	Record	6
Figure 3:	Playback	6
Figure 4:	Application Example	15
Figure 5:	28-Lead 0.600-Inch Plastic Dual Inline Package (PDIP) (P)	17
Figure 6:	28-Lead 0.300-Inch Plastic Small OutLine Integrated Circuit (SOIC) (S)	18
Figure 7:	ISD1200 Series Bonding Physical Layout	19
Chart 1:	Record Mode Operating Current ( $I_{CC}$ )	10
Chart 2:	Total Harmonic Distortion	10
Chart 3:	Standby Current ( $I_{SB}$ )	10
Chart 4:	Oscillator Stability	10
Chart 5:	Record Mode Operating Current ( $I_{CC}$ )	14
Chart 6:	Total Harmonic Distortion	14
Chart 7:	Standby Current ( $I_{SB}$ )	14
Chart 8:	Oscillator Stability	14
Table 1:	Device Playback/Record Durations	1
Table 2:	External Clock Sample Rates	3
Table 3:	Operational Modes Table	5
Table 4:	Absolute Maximum Ratings (Packaged Parts)	7
Table 5:	Operating Conditions (Packaged Parts)	7
Table 6:	DC Parameters (Packaged Parts)	7
Table 7:	AC Parameters (Packaged Parts)	8
Table 8:	Absolute Maximum Ratings (Die)	11
Table 9:	Operating Conditions (Die)	11
Table 10:	DC Parameters (Die)	11
Table 11:	AC Parameters (Die)	12
Table 12:	Plastic Dual Inline Package (PDIP) (P) Dimensions	17
Table 13:	Plastic Small OutLine Integrated Circuit (SOIC) (S) Dimensions	18
Table 14:	ISD1200 Series PIN/PAD Designations, with Respect to Die Center ( $\mu\text{m}$ )	20

## DETAILED DESCRIPTION

### SPEECH/SOUND QUALITY

ISD's patented ChipCorder technology provides natural record and playback. The ISD1200 series includes devices offered at 5.3 and 6.4 KHz sampling frequencies allowing the user a choice of speech quality options. The input voice signals are stored directly in nonvolatile EEPROM cells, and reproduced without the synthetic effect often heard with digital solid-state speech solutions. A complete sample is stored in a single cell, minimizing the memory necessary to store a recording of a given duration.

### DURATION

To meet end system requirements, the ISD1200 series offers single-chip solutions at 10 and 12 seconds.

### EEPROM STORAGE

One of the benefits of ISD's ChipCorder technology is the use of on-chip nonvolatile memory, providing zero-power message storage. The message is retained for up to 100 years typically without power. In addition, the device can be re-recorded typically over 100,000 times.

### BASIC OPERATION

The ISD1200 ChipCorder series devices are controlled by a single record signal,  $\overline{REC}$ , and either of two push-button control playback signals,  $\overline{PLAYE}$  (edge-activated playback), and  $\overline{PLAYL}$  (level-activated playback). The ISD1200 parts are configured for simplicity of design in a single-message application. Using the address lines will allow multiple message applications. Device operation is explained on page 4.

### AUTOMATIC POWER-DOWN MODE

At the end of a playback or record cycle, the ISD1200 series devices automatically return to a low-power standby mode, consuming typically  $0.5 \mu\text{A}$ . During a playback cycle, the device powers down automatically at the end of the message. During a record cycle, the device powers down immediately after  $\overline{REC}$  is released HIGH.

### ADDRESSING (OPTIONAL)

In addition to providing simple message playback, the ISD1200 series provides a full addressing capability.

The ISD1200 series storage array has 80 distinct addressable segments, providing the following resolutions. See Application Information in this book for ISD1200 address tables.

**Table 1: Device Playback/Record Durations**

Part Number	Minimum Duration (Seconds)
ISD1210	125 ms
ISD1212	150 ms

## PIN DESCRIPTIONS

**NOTE** The  $\overline{\text{REC}}$  signal is denounced for 50 ms on the rising edge to prevent a false retriggering from a push-button switch.

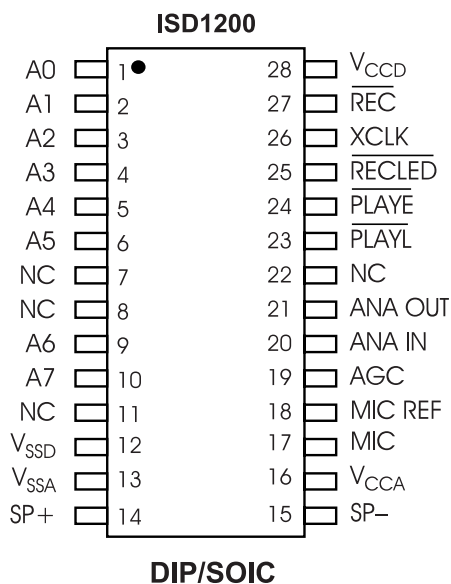
### VOLTAGE INPUTS ( $V_{\text{CCA}}$ , $V_{\text{CCD}}$ )

Analog and digital circuits internal to the ISD1200 series use separate power buses to minimize noise on the chip. These power buses are brought out to separate pins on the package and should be tied together as close to the supply as possible. It is important that the power supply be decoupled as close as possible to the package.

### GROUND INPUTS ( $V_{\text{SSA}}$ , $V_{\text{SSD}}$ )

Similar to  $V_{\text{CCA}}$  and  $V_{\text{CCD}}$ , the analog and digital circuits internal to the ISD1200 series use separate ground buses to minimize noise. These pins should be tied together as close as possible to the device.

Figure 1: ISD1200 Series Pinouts



**NOTE:** NC means must Not Connect.

### RECORD ( $\overline{\text{REC}}$ )

The  $\overline{\text{REC}}$  input is an active-LOW record signal. The device records whenever  $\overline{\text{REC}}$  is LOW. This signal must remain LOW for the duration of the recording.  $\overline{\text{REC}}$  takes precedence over either playback ( $\overline{\text{PLAYE}}$  or  $\overline{\text{PLAYL}}$ ) signal. If  $\overline{\text{REC}}$  is pulled LOW during a playback cycle, the playback immediately ceases and recording begins. A record cycle is completed when  $\overline{\text{REC}}$  is pulled HIGH or the memory space is filled.

An end-of-message marker (EOM) is internally recorded, enabling a subsequent playback cycle to terminate appropriately. The device automatically powers down to standby mode when  $\overline{\text{REC}}$  goes HIGH.

### PLAYBACK, EDGE-ACTIVATED ( $\overline{\text{PLAYE}}$ )

When a LOW-going transition is detected on this input signal, a playback cycle begins. Playback continues until an EOM marker is encountered or the end of the memory space is reached. Upon completion of the playback cycle, the device automatically powers down into standby mode. Taking  $\overline{\text{PLAYE}}$  HIGH during a playback cycle will not terminate the current cycle.

### PLAYBACK, LEVEL-ACTIVATED ( $\overline{\text{PLAYL}}$ )

When this input signal transitions from HIGH to LOW, a playback cycle is initiated. Playback continues until  $\overline{\text{PLAYL}}$  is pulled HIGH, an EOM marker is detected, or the end of the memory space is reached. The device automatically powers down to standby mode upon completion of the playback cycle.

**NOTE** In playback, if either  $\overline{\text{PLAYE}}$  or  $\overline{\text{PLAYL}}$  is held LOW during EOM or OVF, the device will still enter standby and the internal oscillator and timing generator will stop. However, the rising edge of  $\overline{\text{PLAYE}}$  and  $\overline{\text{PLAYL}}$  are not denounced and any subsequent falling edge (particularly switch bounce) present on the input pins will initiate another playback.

### RECORD LED OUTPUT ( $\overline{\text{RECLED}}$ )

The output  $\overline{\text{RECLED}}$  is LOW during a record cycle. It can be used to drive an LED to provide feedback that a record cycle is in progress. In addition,  $\overline{\text{RECLED}}$  pulses LOW momentarily when an EOM marker is encountered in a playback cycle.

### MICROPHONE INPUT (MIC)

The microphone input transfers its signal to the on-chip preamplifier. An on-chip Automatic Gain Control (AGC) circuit controls the gain of this preamplifier from  $-15$  to  $24$  dB. An external microphone should be AC coupled to this pin via a series capacitor. The capacitor value, together with the internal  $10\text{ K}\Omega$  resistance on this pin, determine the low-frequency cutoff for the ISD1200 series passband. See the ISD Application Information in this book for additional information on low-frequency cutoff calculations.

### MICROPHONE REFERENCE (MIC REF)

The MIC REF input is the inverting input to the microphone preamplifier. This provides a noise-canceling or common-mode rejection input to the device when connected differentially to a microphone.

### AUTOMATIC GAIN CONTROL (AGC)

The AGC dynamically adjusts the gain of the preamplifier to compensate for the wide range of microphone input levels. The AGC allows the full range of sound, from whispers to loud sounds, to be recorded with minimal distortion. The "attack" time is determined by the time constant of a  $5\text{ K}\Omega$  internal resistance and an external capacitor (C6 on the schematic in Figure 4) connected from the AGC pin to  $V_{SSA}$  analog ground. The "release" time is determined by the time constant of an external resistor (R5) and an external capacitor (C6) connected in parallel between the AGC Pin and  $V_{SSA}$  analog ground. Nominal values of  $470\text{ K}\Omega$  and  $4.7\text{ }\mu\text{F}$  give satisfactory results in most cases.

### ANALOG OUTPUT (ANA OUT)

This pin provides the preamplifier output to the user. The voltage gain of the preamplifier is determined by the voltage level at the AGC pin.

### ANALOG INPUT (ANA IN)

The ANA IN pin transfers the input signal to the chip for recording. For microphone inputs, the ANA OUT pin should be connected via an external capacitor to the ANA IN pin. This capacitor value, together with the  $3.0\text{ K}\Omega$  input impedance of ANA IN, is selected to give additional cutoff at the low-frequency end of the voice passband. If the desired input is derived from a source other than a microphone, the signal can be fed, capacitively coupled, into the ANA IN pin directly.

### EXTERNAL CLOCK INPUT (XCLK)

The external clock input for the ISD1200 devices has an internal pull-down device. The ISD1200 is configured at the factory with an internal sampling clock frequency that guarantees its minimum nominal record/playback time. For instance, an ISD1210 operating within specification will be observed to always have a minimum of 10 seconds of recording time. The sampling frequency is then maintained to a variation of  $\pm 2.25$  percent over the commercial temperature and operating voltage ranges while still maintaining the minimum specified recording duration. This will result in some devices having a few percent more than nominal recording time. If greater precision is required, the device can be clocked through the XCLK pin as follows:

**Table 2: External Clock Sample Rates**

Part Number	Sample Rate	Required Clock
ISD1210	6.4 KHz	819.2 KHz
ISD1212	5.3 KHz	682.7 KHz

These recommended clock rates should not be varied because the antialiasing and smoothing filters are fixed, and aliasing problems can occur if the sample rate differs from the one recommended. The duty cycle on the input clock is not critical, as the clock is immediately divided by two internally.

**If the XCLK is not used, this input should be connected to ground.**

### **SPEAKER OUTPUTS (SP+, SP-)**

The SP+ and SP- pins provide direct drive for loudspeakers with impedances as low as 16  $\Omega$ . A single output may be used, but, for direct-drive loudspeakers, the two opposite-polarity outputs provide an improvement in output power of up to four times over a single-ended connection. Furthermore, when SP+ and SP- are used, a speaker-coupling capacitor is not required. A single-ended connection will require an AC-coupling capacitor between the SP pin and the speaker. The speaker outputs are in a high-impedance state during a record cycle, and held at  $V_{SSA}$  during power-down.

### **ADDRESS INPUTS (A0–A7)**

The Address Inputs have two functions, depending upon the level of the two Most Significant Bits (MSB) of the address.

If either of the two MSBs is LOW, the inputs are all interpreted as address bits and are used as the start address for the current record or playback cycle. The address pins are inputs only and do not output internal address information as the operation progresses. Address inputs are latched by the falling edge of  $\overline{\text{PLAYE}}$ ,  $\overline{\text{PLAYL}}$ , or  $\overline{\text{REC}}$ .

### **OPERATIONAL MODES**

The ISD1200 series is designed with several built-in operational modes provided to allow maximum functionality with a minimum of additional components, described in detail below. The operational modes use the address pins on the ISD1200 devices, but are mapped outside the valid address range. When the two Most Significant Bits (MSBs) are HIGH (A6 and A7), the remaining address signals are interpreted as mode bits and not as address bits. Therefore, operational modes and direct addressing are not compatible and cannot be used simultaneously.

There are two important considerations for using operational modes. First, all operations begin initially at address 0, which is the beginning of the ISD1200 address space. Later operations can begin at other address locations, depending on the operational mode(s) chosen. In addition, the address pointer is reset to 0 when the device is changed from record to playback but not from playback to record when A4 is HIGH in Operational Mode.

Second, an Operational Mode is executed when any of the control inputs,  $\overline{\text{PLAYE}}$ ,  $\overline{\text{PLAYL}}$ , or  $\overline{\text{REC}}$ , go LOW and the two MSBs are HIGH. This Operational Mode remains in effect until the next LOW-going control input signal, at which point the current address/mode levels are sampled and executed.

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**NOTE** *The two MSBs are on pins 9 and 10 for each ISD1200 series device.*

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## OPERATIONAL MODES DESCRIPTION

The Operational Modes can be used in conjunction with a microcontroller, or they can be hard-wired to provide the desired system operation.

### A0 — MESSAGE CUEING

Message Cueing allows the user to skip through messages, without knowing the actual physical addresses of each message. Each control input LOW pulse causes the internal address pointer to skip to the next message. This mode should be used for playback only, and is typically used with the A4 Operational Mode.

### A1 — DELETE EOM MARKERS

The A1 Operational Mode allows sequentially recorded messages to be combined into a single message with only one EOM marker set at the end of the final message. When this operational mode is configured, messages recorded sequentially are played back as one continuous message.

### A2 — UNUSED

### A3 — MESSAGE LOOPING

The A3 Operational Mode allows for the automatic, continuously repeated playback of the message located at the beginning of the address space.

A message can completely fill the ISD1200 device and will loop from beginning to end. Pulsing  $\overline{\text{PLAYE}}$  will start the playback and pulsing  $\overline{\text{PLAYL}}$  will end the playback.

### A4 — CONSECUTIVE ADDRESSING

During normal operations, the address pointer will reset when a message is played through to an EOM marker. The A4 Operational Mode inhibits the address pointer reset, allowing messages to be recorded or played back consecutively. When the device is in a static state; i.e., not recording or playing back, momentarily taking this pin LOW will reset the address counter to zero.

### A5 — UNUSED

**Table 3: Operational Modes Table**

Address Ctrl. (HIGH)	Function	Typical Use	Jointly Compatible*
A0	Message cueing	Fast-forward through messages	A4
A1	Delete EOM markers	Position EOM marker at the end of the last message	A3, A4
A2	Unused		
A3	Looping	Continuous playback from Address 0	A1
A4	Consecutive addressing	Record/play multiple consecutive messages	A0, A1
A5	Unused		

**NOTE:** An asterisk (\*) indicates additional operational modes that can be used simultaneously with the given mode.

TIMING DIAGRAMS

Figure 2: Record

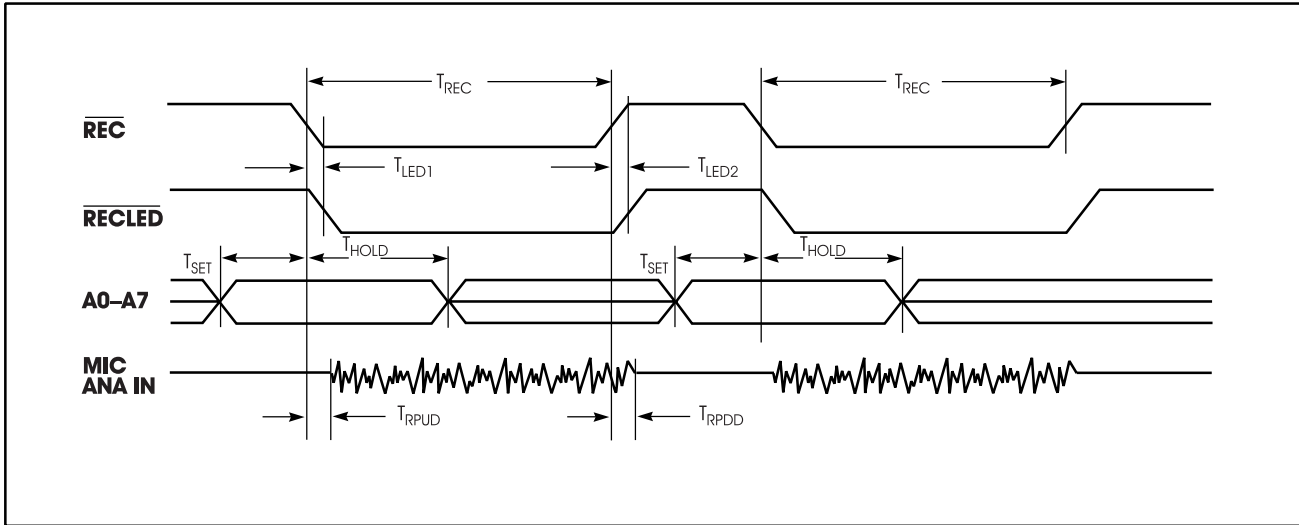
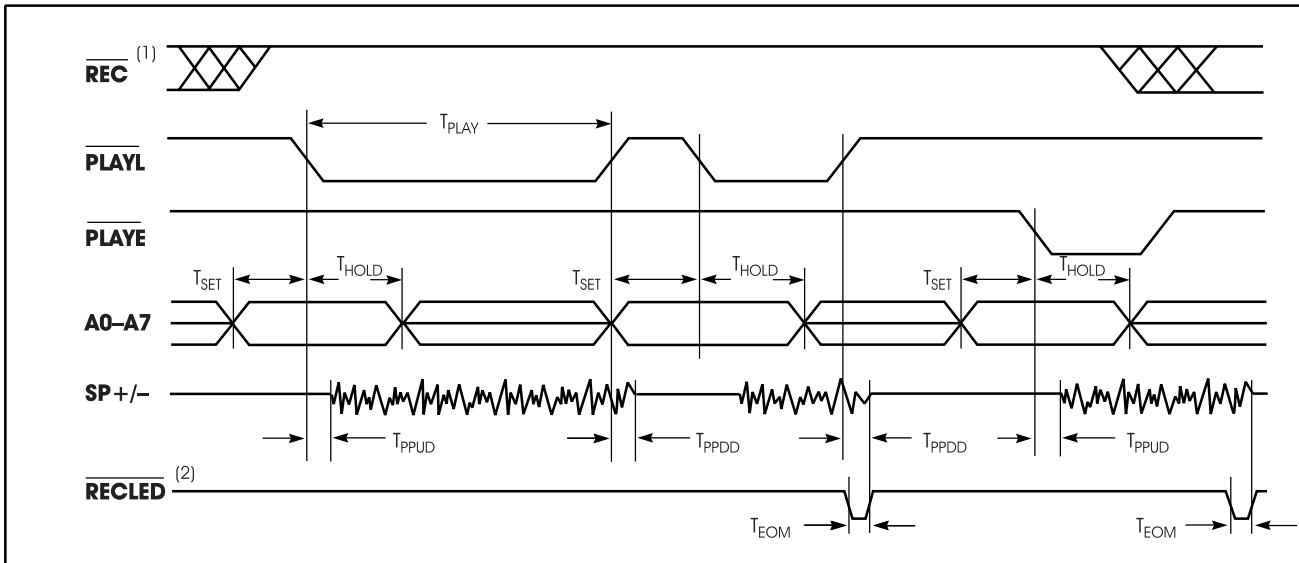


Figure 3: Playback



1.  $\overline{REC}$  must be HIGH for the entire duration of a playback cycle.
2.  $\overline{RECLEd}$  functions as an EOM during playback.

**Table 4: Absolute Maximum Ratings (Packaged Parts)<sup>(1)</sup>**

Condition	Value
Junction temperature	150°C
Storage temperature range	-65°C to +150°C
Voltage applied to any pin	(V <sub>SS</sub> - 0.3 V) to (V <sub>CC</sub> + 0.3 V)
Voltage applied to any pin (Input current limited to ±20 mA)	(V <sub>SS</sub> - 1.0 V) to (V <sub>CC</sub> + 1.0 V)
Lead temperature (soldering - 10 seconds)	300°C
V <sub>CC</sub> - V <sub>SS</sub>	-0.3 V to +7.0 V

**1.** Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.

**Table 5: Operating Conditions (Packaged Parts)**

Condition	Value
Commercial operating temperature range <sup>(1)</sup>	0°C to +70°C
Supply voltage (V <sub>CC</sub> ) <sup>(2)</sup>	+4.5 V to +5.5 V
Ground voltage (V <sub>SS</sub> ) <sup>(3)</sup>	0 V

**1.** Case temperature.

**2.** V<sub>CC</sub> = V<sub>CCA</sub> = V<sub>CCD</sub>.

**3.** V<sub>SS</sub> = V<sub>SSA</sub> = V<sub>SSD</sub>.

**Table 6: DC Parameters (Packaged Parts)**

Symbol	Parameters	Min <sup>(2)</sup>	Typ <sup>(1)</sup>	Max <sup>(2)</sup>	Units	Conditions
V <sub>IL</sub>	Input Low Voltage			0.8	V	
V <sub>IH</sub>	Input High Voltage	2.4			V	
V <sub>OL</sub>	Output Low Voltage			0.4	V	I <sub>OL</sub> = 4.0 mA
V <sub>OH</sub>	Output High Voltage	2.4			V	I <sub>OH</sub> = -1.6 mA
I <sub>CC</sub>	V <sub>CC</sub> Current (Operating)		15	30	mA	V <sub>CC</sub> = 5.5 V <sup>(3)</sup> , R <sub>EXT</sub> = ∞
I <sub>SB</sub>	V <sub>CC</sub> Current (Standby)		0.5	10	μA	(3) (4)
I <sub>IL</sub>	Input Leakage Current			±1	μA	
I <sub>ILPD</sub>	Input Current HIGH w/Pull Down			130	μA	Force V <sub>CC</sub> <sup>(5)</sup>
R <sub>EXT</sub>	Output Load Impedance	16			Ω	Speaker Load
R <sub>MIC</sub>	Preamp In Input Resistance		10		KΩ	Pins 17, 18
R <sub>ANA IN</sub>	ANA IN Input Resistance		3		KΩ	
A <sub>PRE1</sub>	Preamp Gain 1		24		dB	AGC = 0.0 V
A <sub>PRE2</sub>	Preamp Gain 2		-45	-15	dB	AGC = 2.5 V

Table 6: DC Parameters (Packaged Parts)

Symbol	Parameters	Min <sup>(2)</sup>	Typ <sup>(1)</sup>	Max <sup>(2)</sup>	Units	Conditions
A <sub>ARP</sub>	ANA IN to SP +/- Gain		22		dB	
R <sub>AGC</sub>	AGC Output Resistance		5		K $\Omega$	
I <sub>PREH</sub>	Preamplifier Output Source		-2		mA	@ V <sub>OUT</sub> = 1.0 V
I <sub>PREL</sub>	Preamplifier Input Sink		0.5		mA	@ V <sub>OUT</sub> = 2.0 V

1. Typical values @ T<sub>A</sub> = 25°C and 5.0 V.
2. All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.
3. V<sub>CCA</sub> and V<sub>CCD</sub> connected together.
4. REC, PLAYL, and PLAYE must be at V<sub>CCD</sub>.
5. Pin 26.

Table 7: AC Parameters (Packaged Parts)

Symbol	Characteristic	Min <sup>(2)</sup>	Typ <sup>(1)</sup>	Max <sup>(2)</sup>	Units	Conditions
F <sub>S</sub>	Sampling Frequency			6.4	KHz	<sup>(5)</sup>
				5.3	KHz	<sup>(5)</sup>
F <sub>CF</sub>	Filter Pass Band		2.6		KHz	3 dB Roll-Off Point <sup>(3)(6)</sup>
			2.2		KHz	3 dB Roll-Off Point <sup>(3)(6)</sup>
T <sub>REC</sub>	Record Duration	10			sec	
		12			sec	
T <sub>PLAY</sub>	Playback Duration	10			sec	<sup>(5)</sup>
		12			sec	<sup>(5)</sup>
T <sub>LED1</sub>	RECLED ON Delay		5		msec	
T <sub>LED2</sub>	RECLED OFF Delay	40	48.6	100	msec	
		50	58.3	105	msec	
T <sub>SET</sub>	Address Setup Time	300			nsec	
T <sub>HOLD</sub>	Address Hold Time	0			nsec	
T <sub>RPUD</sub>	Record Power-Up		32		msec	
	Delay		39		msec	
T <sub>RPDD</sub>	Record Power-Down		32		msec	
	Delay		39		msec	
T <sub>PPUD</sub>	Play Power-Up		32		msec	
	Delay		39		msec	

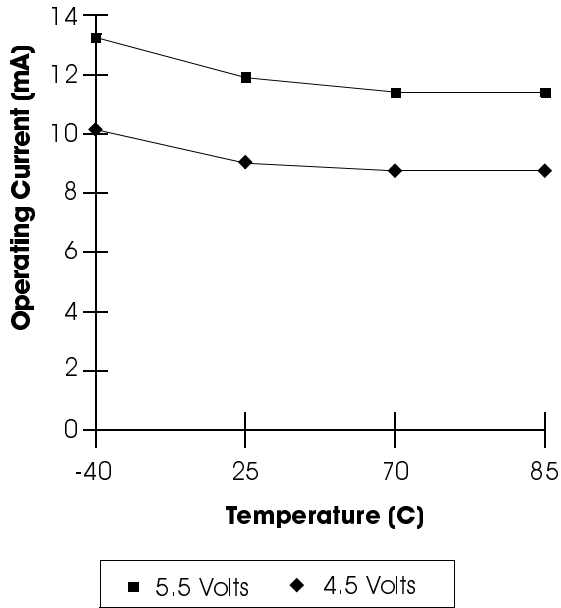
**Table 7: AC Parameters (Packaged Parts)**

Symbol	Characteristic	Min <sup>(2)</sup>	Typ <sup>(1)</sup>	Max <sup>(2)</sup>	Units	Conditions
T <sub>PPDD</sub>	Play Power-Down		8.1		msec	
	Delay		9.7		msec	
T <sub>EOM</sub>	EOM Pulse Width		15.625		msec	
			18.75		msec	
THD	Total Harmonic Distortion		1		%	@ 1 KHz
P <sub>OUT</sub>	Speaker Output Power		12.2		mW	R <sub>EXT</sub> = 16 Ω
V <sub>OUT</sub>	Voltage Across Speaker Pins		1.25	2.5	V p-p	R <sub>EXT</sub> = 600 Ω
V <sub>IN1</sub>	MIC Input Voltage			20	mV	Peak-to-Peak <sup>(4)</sup>
V <sub>IN2</sub>	ANA IN Input Voltage			50	mV	Peak-to-Peak

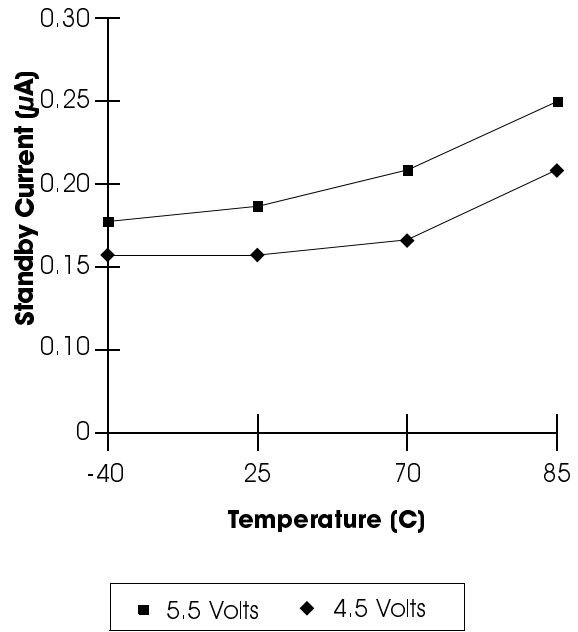
1. Typical values @ T<sub>A</sub> = 25°C, 5.0 V, and 6.4 KHz sample rate.
2. All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.
3. Low-frequency cutoff depends upon value of external capacitors (see Pin Descriptions).
4. With 5.1 KΩ series resistor at ANA IN.
5. Sampling frequency and playback duration will vary as much as ±2.25 percent over the commercial temperature and voltage ranges. All devices will meet the maximum sampling frequency and minimum playback duration parameters. For greater stability, an external clock can be utilized (see Pin Descriptions).
6. Filter specification applies to the antialiasing filter and to the smoothing filter.

**TYPICAL PARAMETER VARIATION WITH VOLTAGE AND TEMPERATURE (PACKAGED PARTS)**

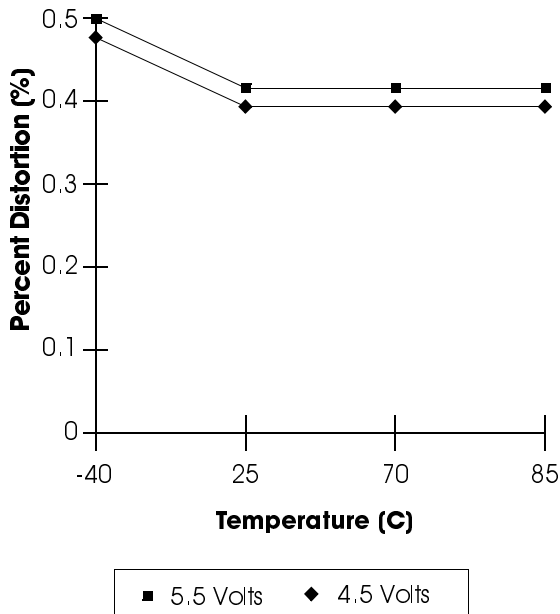
**Chart 1: Record Mode Operating Current ( $I_{CC}$ )**



**Chart 3: Standby Current ( $I_{SB}$ )**



**Chart 2: Total Harmonic Distortion**



**Chart 4: Oscillator Stability**

