19-3709; Rev 2; 11/06

MAXIM

1.5V to 3.6V, 357ksps, 1-Channel True-Differential/ 2-Channel Single-Ended, 10-Bit, SAR ADCs

General Description

The MAX1392/MAX1395 micropower, serial-output, 10-bit, analog-to-digital converters (ADCs) operate with a single power supply from +1.5V to +3.6V. These ADCs feature automatic shutdown, fast wake-up, and a high-speed 3-wire interface. Power consumption is only 0.740mW (V_{DD} = +1.5V) at the maximum conversion rate of 357ksps. AutoShutdown™ between conversions reduces power consumption at slower throughput rates.

The MAX1392/MAX1395 require an external reference V_{REF} that has a wide range from 0.6V to V_{DD}. The MAX1392 provides one true-differential analog input that accepts signals ranging from 0 to V_{REF} (unipolar mode) or $\pm V_{REF}/2$ (bipolar mode). The MAX1395 provides two single-ended inputs that accept signals ranging from 0 to V_{REF}. Analog conversion results are available through a 5MHz, 3-wire SPI™-/QSPI™-/MICROWIRE™-/digital signal processor (DSP)-compatible serial interface. Excellent dynamic performance, low voltage, low power, ease of use, and small package sizes make these converters ideal for portable battery-powered data-acquisition applications, and for other applications that demand low power consumption and minimal space.

The MAX1392/MAX1395 are available in a space-saving (3mm x 3mm) 10-pin TDFN package. The parts operate over the extended (-40°C to +85°C) and military (-55°C to +125°C) temperature ranges.

Applications

Portable Datalogging

Data Acquisition

Medical Instruments

Battery-Powered Instruments

Process Control

Features

- **357ksps 10-Bit Successive-Approximation Register (SAR) ADCs**
- **Single True-Differential Analog Input Channel with Unipolar-/Bipolar-Selected Input (MAX1392)**
- **Dual Single-Ended Input Channel with Channel-Selected Input (MAX1395)**
- **±0.5 LSB INL, ±0.5 LSB DNL, No Missing Codes**
- **±1 LSB Total Unadjusted Error**
- **61dB SINAD at 85kHz Input Frequency**
- **Single-Supply Voltage (+1.5V to +3.6V)**
- **0.945mW at 350ksps, 1.8V**
- **0.27mW at 100ksps, 1.8V**
- **3.1µW at 1ksps, 1.8V**
- **< 1µA Shutdown Current**
- **External Reference (0.6V to V_{DD})**
- **AutoShutdown Between Conversions**
- **SPI-/QSPI-/MICROWIRE-/DSP-Compatible, 3- or 4-Wire Serial Interface**
- **Small (3mm x 3mm), 10-Pin TDFN**

Typical Operating Circuit and Pin Configurations appear at end of data sheet.

AutoShutdown is a trademark of Maxim Integrated Products, Inc.
SPI/QSPI are trademarks of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corp.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	ANALOG INPUTS	TOP MARK	PKG CODE
MAX1392ETB	-40°C to +85°C	10 TDFN-EP*	1-CH DIFF	AOY	T1033-1
MAX1392MTB**	-55°C to +125°C	10 TDFN-EP*	1-CH DIFF	—	T1033-1
MAX1395ETB	-40°C to +85°C	10 TDFN-EP*	2-CH S/E	APB	T1033-1
MAX1395MTB**	-55°C to +125°C	10 TDFN-EP*	2-CH S/E	—	T1033-1

*EP = Exposed pad.
**Future product—contact factory for availability.

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ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +4V
SCLK, $\overline{CS}$, $\overline{OE}$, $\overline{CH1}$/CH2, UNI/$\overline{BIP}$,
DOUT to GND.....-0.3V to (V_{DD} + 0.3V)
AIN+, AIN-, AIN1, AIN2, REF to GND .....-0.3V to (V_{DD} + 0.3V)
Maximum Current into Any Pin .....±50mA
Continuous Power Dissipation (T_A = +70°C)
10-Pin TDFN (derate 18.5mW/°C above +70°C) 1481.5mW

Operating Temperature Ranges
MAX139_E_ _.....-40°C to +85°C
MAX139_M_ _.....-55°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +1.5V to +3.6V, V_{REF} = V_{DD}, C_{REF} = 0.1µF, f_{SCLK} = 5MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ACCURACY (Note 2)							
Resolution				10			Bits
Integral Nonlinearity	INL					±0.5	LSB
Differential Nonlinearity	DNL	No missing code overtemperature				±0.5	LSB
Offset Error					0.25	±0.5	LSB
Gain Error		Offset nulled			0.25	±0.5	LSB
Total Unadjusted Error	TUE					±1	LSB
Offset-Error Temperature Coefficient					±0.001		LSB/°C
Gain-Error Temperature Coefficient					±0.00025		LSB/°C
Channel-to-Channel Offset Matching		MAX1395 only			±0.1		LSB
Channel-to-Channel Gain Matching		MAX1395 only			±0.1		LSB
Input Common-Mode Rejection	CMR	V_{CM} = 0 to V_{DD}, MAX1392 only			±0.1		mV/V
DYNAMIC SPECIFICATIONS (Note 3)							
Signal-to-Noise Plus Distortion	SINAD	V_{REF} = V_{DD} = 1.6 to 3.6V		61			dB
Signal-to-Noise Ratio	SNR	V_{REF} = V_{DD} = 1.6 to 3.6V		61			dB
Total Harmonic Distortion	THD				-83	-73	dBc
Spurious-Free Dynamic Range	SFDR				-84	-74	dBc
Intermodulation Distortion	IMD	f_{IN1} = 83kHz at -6.5dBFS, f_{IN2} = 87kHz at -6.5dBFS			-75		dB
Channel-to-Channel Crosstalk		MAX1395 only			-70		dB
Full-Power Bandwidth		-3dB point			4		MHz
Full-Linear Bandwidth		SINAD > 59dB	MAX1392		200		kHz
			MAX1395		150		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +1.5V to +3.6V, V_{REF} = V_{DD}, C_{REF} = 0.1µF, f_{SCLK} = 5MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CONVERSION RATE						
Conversion Time	t_{CONV}	11 clock cycles	2.2			µs
Throughput Rate		14 clocks per conversion; includes power-up, acquisition, and conversion time			357	ksps
Power-Up and Acquisition Time	t_{ACQ}	Three SCLK cycles	600			ns
Aperture Delay	t_{AD}			8		ns
Aperture Jitter	t_{AJ}			30		ps
Serial Clock Frequency	f_{CLK}		0.1		5.0	MHz
ANALOG INPUTS (AIN+, AIN-, AIN1, AIN2)						
Input Voltage Range	V_{IN}	Unipolar	0		V_{REF}	V
		Bipolar, MAX1392 only (AIN+ - AIN-)	$-V_{REF}/2$		$+V_{REF}/2$	
Common-Mode Input Voltage Range	V_{CM}	Bipolar, MAX1392 only [(AIN+) + (AIN-)] / 2	0		V_{DD}	V
Input Leakage Current		Channel not selected, or conversion stopped, or in shutdown mode			±1.5	µA
Input Capacitance				16		pF
REFERENCE INPUT (REF)						
REF Input Voltage Range	V_{REF}		0.6		V_{DD} + 0.05	V
REF Input Capacitance				24		pF
REF DC Leakage Current				0.025	±2.5	µA
REF Input Dynamic Current		357ksps		20	60	µA
DIGITAL INPUTS (SCLK, $\overline{CS}$, $\overline{OE}$, $\overline{CH1}$/CH2, UNI/$\overline{BIP}$)						
Input-Voltage Low	V_{IL}				0.3 x V_{DD}	V
Input-Voltage High	V_{IH}		0.7 x V_{DD}			V
Input Hysteresis				0.06 x V_{DD}		V
Input Leakage Current	I_{IL}	Inputs at GND or V_{DD}			±1	µA
Input Capacitance	C_{IN}	$\overline{CS}$, $\overline{OE}$		1		pF
		$\overline{CH1}$/CH2, UNI/$\overline{BIP}$		12.5		
DIGITAL OUTPUT (DOUT)						
Output-Voltage Low	V_{OL}	I_{SINK} = 2mA			0.1 x V_{DD}	V
Output-Voltage High	V_{OH}	I_{SOURCE} = 2mA	0.9 x V_{DD}			V

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ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +1.5V to +3.6V, V_{REF} = V_{DD}, C_{REF} = 0.1µF, f_{SCLK} = 5MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Tri-State Leakage Current	I_{LT}	$\overline{OE}$ = V_{DD}				±1	µA
Tri-State Output Capacitance	C_{OUT}	$\overline{OE}$ = V_{DD}			10		pF
POWER SUPPLY							
Positive Supply Voltage	V_{DD}			1.5		3.6	V
Positive Supply Current (Note 4)	I_{DD}	f_{SAMPLE} = 100ksps	V_{DD} = 1.6V		150	170	µA
			V_{DD} = 3V		200	225	
		f_{SAMPLE} = 357ksps	V_{DD} = 1.6V		520	600	
			V_{DD} = 3V		710	800	
		Power-down mode (Note 5)			5	10	
		Power-down mode (Note 6)			0.2	±2.5	
Power-Supply Rejection (Note 7)	PSR	V_{DD} = 1.5V to 3.6V, full-scale input			±150	±1000	µV/V

TIMING CHARACTERISTICS

(V_{DD} = +1.5V to +3.6V, V_{REF} = V_{DD}, C_{REF} = 0.1µF, f_{SCLK} = 5MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Figure 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Clock Period	t_{CP}		200		10000	ns
SCLK Pulse-Width High	t_{CH}		90			ns
SCLK Pulse-Width Low	t_{CL}		90			ns
$\overline{CS}$ Fall to SCLK Rise Setup	t_{CSS}		80			ns
SCLK Rise to $\overline{CS}$ Fall Ignore	t_{CSO}		0			ns
SCLK Fall to DOUT Valid	t_{DOV}	C_{LOAD} = 0 to 30pF	10		80	ns
$\overline{OE}$ Rise to DOUT Disable	t_{DOD}			6	20	ns
$\overline{OE}$ Fall to DOUT Enable	t_{DOE}			9	20	ns
$\overline{CS}$ Pulse-Width High or Low	t_{CSW}		80			ns
$\overline{OE}$ Pulse-Width High or Low	t_{OEW}		80			ns
$\overline{CH1}$/CH2 Setup Time (to the First SCLK)	t_{CHS}	MAX1395 only	10			ns
$\overline{CH1}$/CH2 Hold Time (to the First SCLK)	t_{CHH}	MAX1395 only	0			ns
UNI/$\overline{BIP}$ Setup Time (to the First SCLK)	t_{UBS}	MAX1392 only	10			ns
UNI/$\overline{BIP}$ Hold Time (to the First SCLK)	t_{UBH}	MAX1392 only	0			ns

Note 1: Devices are production tested at T_A = +25°C and T_A = +85°C. Specifications to -40°C are guaranteed by design.
Note 2: V_{DD} = 1.5V, V_{REF} = 1.5V, and V_{AIN} = 1.5V.
Note 3: V_{DD} = 1.5V, V_{REF} = 1.5V, V_{AIN} = 1.5V_{P-P}, f_{SCLK} = 5MHz, f_{SAMPLE} = 357ksps, and f_{IN} (sine-wave) = 85kHz.
Note 4: All digital inputs swing between V_{DD} and GND. V_{REF} = V_{DD}, f_{IN} = 85kHz sine-wave, V_{AIN} = V_{REFP-P}, C_{LOAD} = 30pF on DOUT.
Note 5: $\overline{CS}$ = V_{DD}, $\overline{OE}$ = UNI/$\overline{BIP}$ = $\overline{CH1}$/CH2 = V_{DD} or GND, SCLK is active.
Note 6: $\overline{CS}$ = V_{DD}, $\overline{OE}$ = UNI/$\overline{BIP}$ = $\overline{CH1}$/CH2 = V_{DD} or GND, SCLK is inactive.
Note 7: Change in V_{AIN} at code boundary 1022.5.

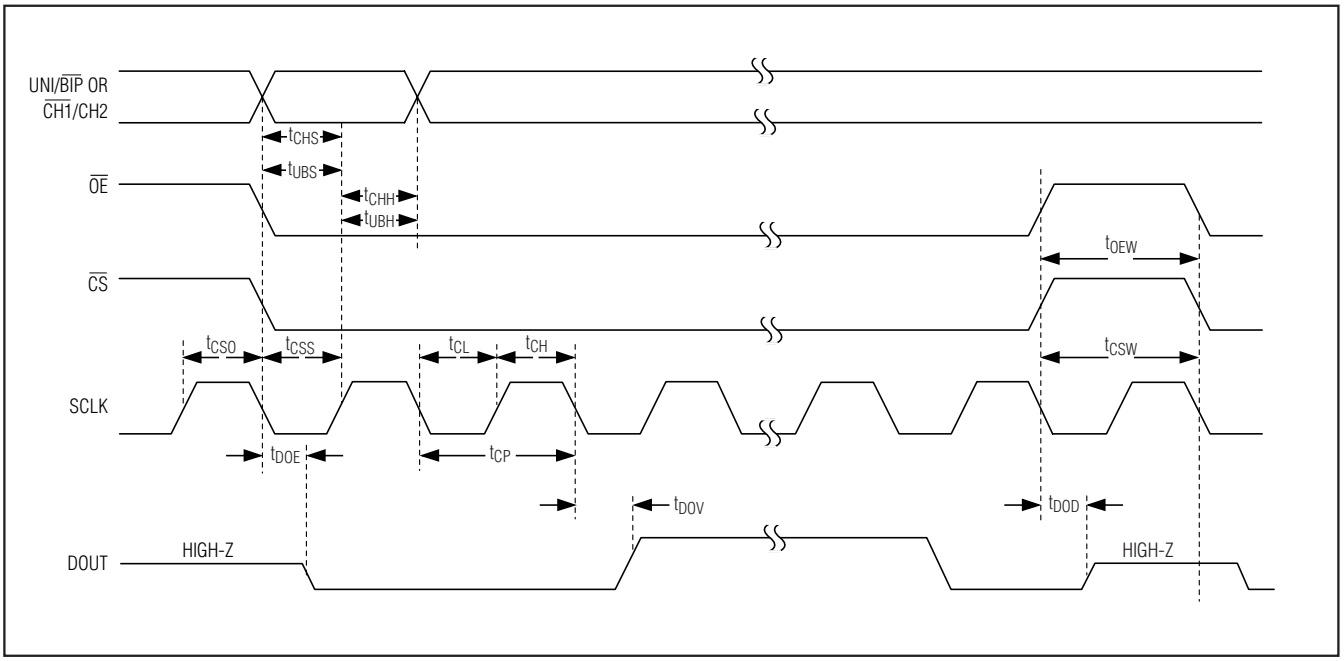


Figure 1. Detailed Serial-Interface Timing Diagram

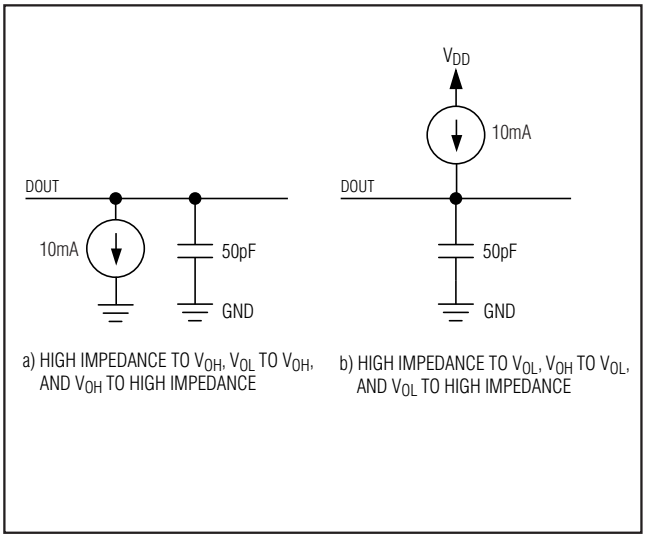


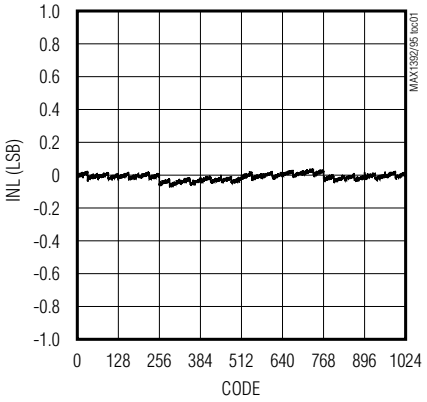
Figure 2. Load Circuits for Enable/Disable Times

1.5V to 3.6V, 357ksps, 1-Channel True-Differential/ 2-Channel Single-Ended, 10-Bit, SAR ADCs

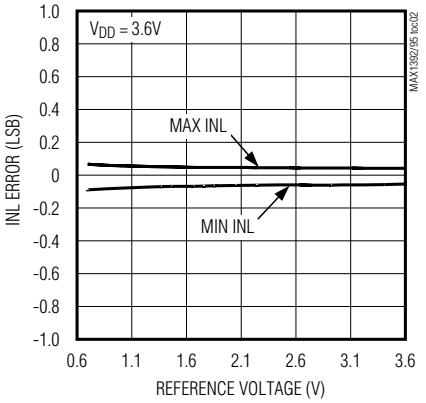
Typical Operating Characteristics

(V_{DD} = +1.5V, V_{REF} = +1.5V, C_{REF} = 0.1µF, C_L = 30pF, f_{SCLK} = 5MHz. T_A = +25°C, unless otherwise noted.)

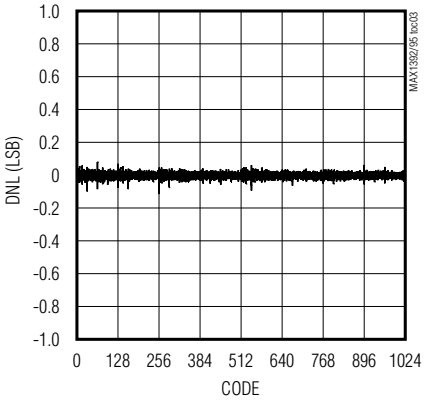
INL vs. CODE



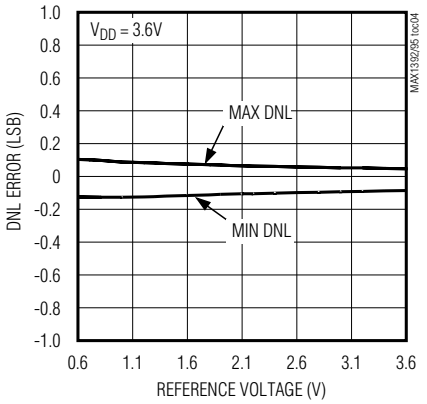
INL ERROR vs. REFERENCE VOLTAGE



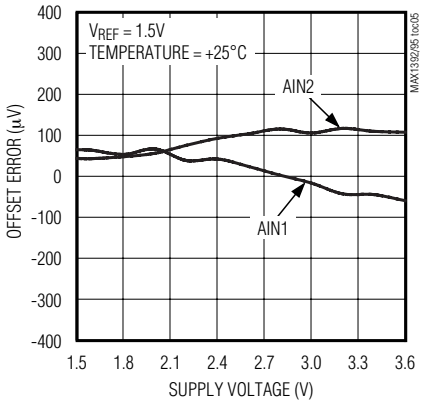
DNL vs. CODE



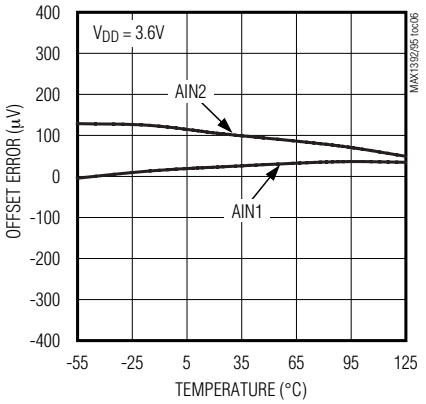
DNL ERROR vs. REFERENCE VOLTAGE



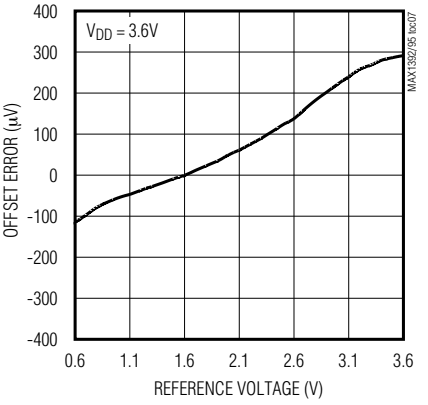
OFFSET ERROR vs. SUPPLY VOLTAGE



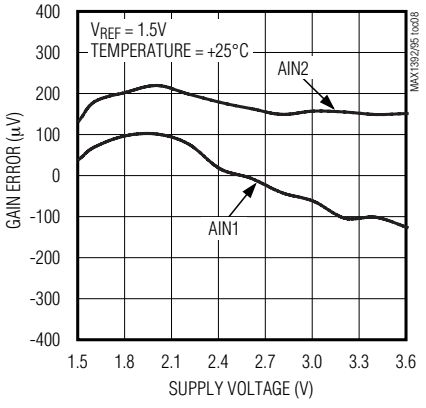
OFFSET ERROR vs. TEMPERATURE



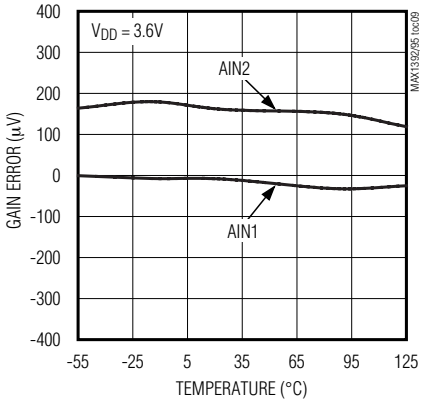
OFFSET ERROR vs. REFERENCE VOLTAGE



GAIN ERROR vs. SUPPLY VOLTAGE



GAIN ERROR vs. TEMPERATURE

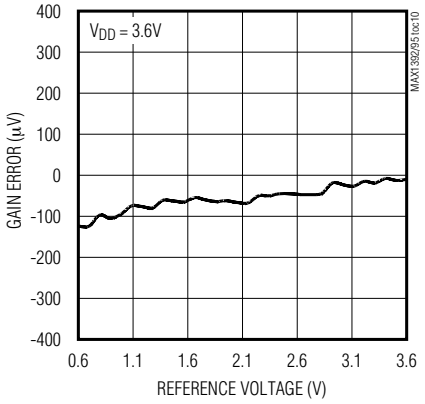


1.5V to 3.6V, 357ksps, 1-Channel True-Differential/ 2-Channel Single-Ended, 10-Bit, SAR ADCs

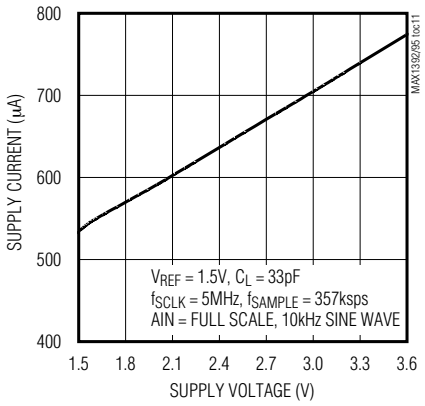
Typical Operating Characteristics (continued)

(V_{DD} = +1.5V, V_{REF} = +1.5V, C_{REF} = 0.1µF, C_L = 30pF, f_{SCLK} = 5MHz. T_A = +25°C, unless otherwise noted.)

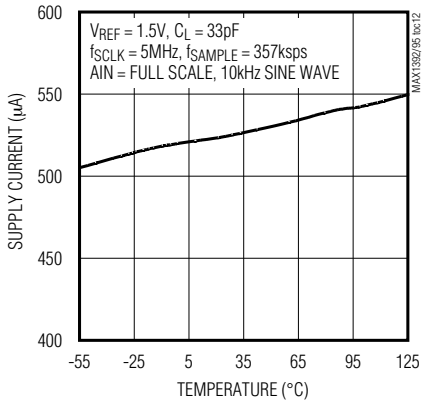
GAIN ERROR vs. REFERENCE VOLTAGE



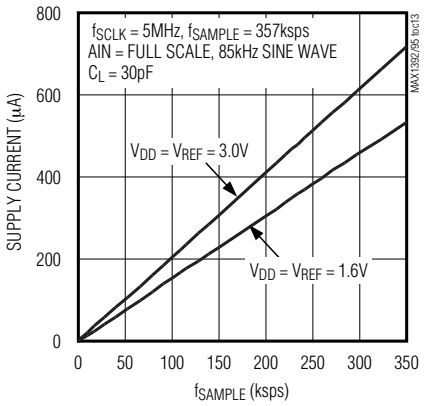
SUPPLY CURRENT vs. SUPPLY VOLTAGE



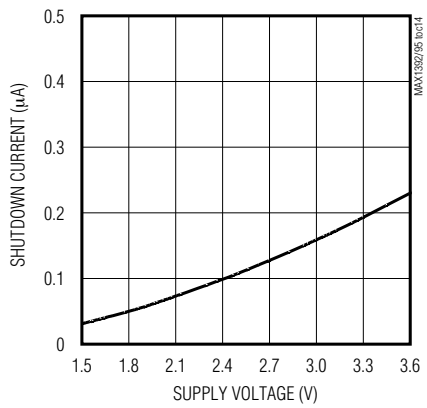
SUPPLY CURRENT vs. TEMPERATURE



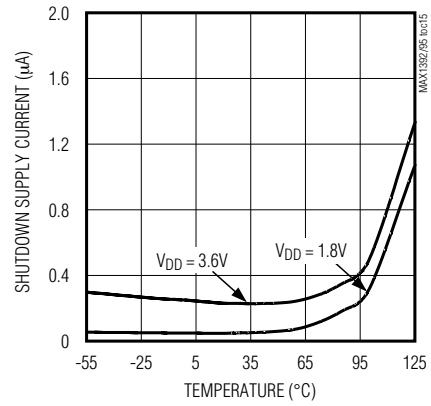
SUPPLY CURRENT vs. CONVERSION RATE



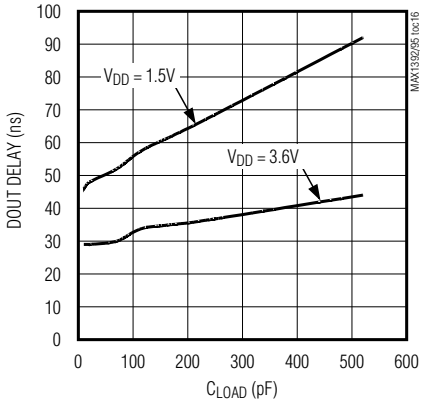
SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



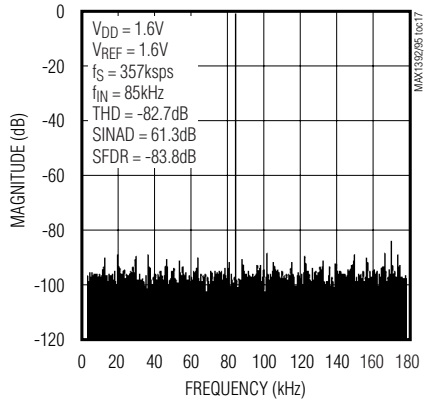
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



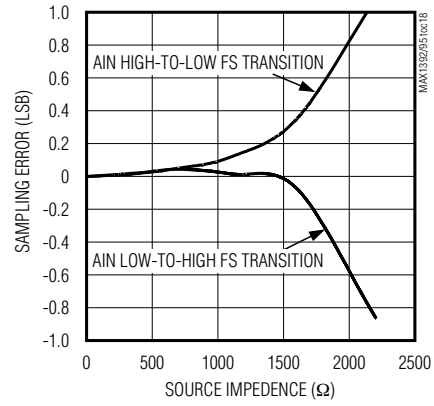
SCLK-TO-DOUT TIMING



FFT



SAMPLING ERROR vs. SOURCE IMPEDANCE



1.5V to 3.6V, 357ksps, 1-Channel True-Differential/ 2-Channel Single-Ended, 10-Bit, SAR ADCs

Pin Description

PIN		NAME	FUNCTION
MAX1392	MAX1395		
1	1	V_{DD}	Positive Supply Voltage. Connect V_{DD} to a 1.5V to 3.6V power supply. Bypass V_{DD} to GND with a 0.1µF capacitor as close to the device as possible.
2	—	AIN-	Negative Analog Input
—	2	AIN2	Analog Input Channel 2
3	—	AIN+	Positive Analog Input
—	3	AIN1	Analog Input Channel 1
4	4	GND	Ground
5	5	REF	External Reference Voltage Input. V_{REF} = 0.6V to (V_{DD} + 0.05V). Bypass REF to GND with a 0.1µF capacitor as close to the device as possible.
6	—	UNI/$\overline{BIP}$	Input-Mode Select. Drive UNI/$\overline{BIP}$ high to select unipolar input mode. Pull UNI/$\overline{BIP}$ low to select bipolar input mode. In unipolar mode, the output data is in straight binary format. In bipolar mode, the output data is in two's-complement format.
—	6	$\overline{CH1}$/CH2	Channel-Select Input. Pull $\overline{CH1}$/CH2 low to select channel 1. Drive $\overline{CH1}$/CH2 high to select channel 2.
7	7	$\overline{OE}$	Active-Low Output Enable. Pull $\overline{OE}$ low to enable DOUT. Drive $\overline{OE}$ high to disable DOUT. Connect to $\overline{CS}$ to interface with SPI, QSPI, and MICROWIRE devices or set low to interface with DSP devices.
8	8	$\overline{CS}$	Active-Low Chip-Select Input. A falling edge on $\overline{CS}$ initiates power-up and acquisition.
9	9	DOUT	Serial-Data Output. DOUT changes state on the falling edge of SCLK. DOUT is high impedance when $\overline{OE}$ is high.
10	10	SCLK	Serial-Clock Input. SCLK drives the conversion process and clocks data out. Acquisition ends on the 3rd falling edge after the $\overline{CS}$ falling edge. The LSB is clocked out on the SCLK 13th falling edge and the device enters AutoShutdown mode (see Figures 8, 9, and 10).
—	—	EP	Exposed Pad. Not internally connected. Connect the exposed pad to GND or leave unconnected.

Detailed Description

The MAX1392/MAX1395 use an input track and hold (T/H) circuit along with a SAR to convert an analog input signal to a serial 10-bit digital output data stream. The serial interface provides easy interfacing to microprocessors and DSPs. Figure 3 shows the simplified functional diagram for the MAX1392 (1 channel, true differential) and the MAX1395 (2 channels, single ended).

True-Differential Analog Input T/H

The equivalent input circuit of Figure 4 shows the MAX1392/MAX1395 input architecture, which is composed of a T/H, a comparator, and a switched-capacitor DAC. The T/H enters its tracking mode on the falling edge of $\overline{CS}$ (while $\overline{OE}$ is held low). The positive input capacitor is connected to AIN+ (MAX1392), or to AIN1 or AIN2 (MAX1395). The negative input capacitor is connected to AIN- (MAX1392) or GND (MAX1395). The T/H enters its hold mode on the 3rd falling edge of SCLK

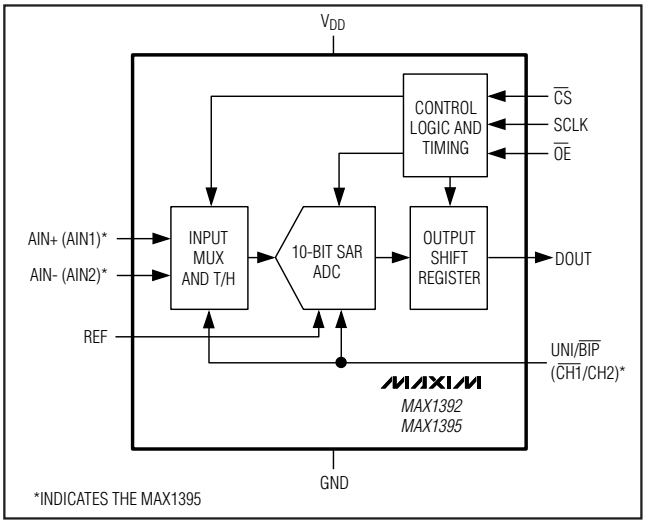


Figure 3. Simplified Functional Diagram

and the difference between the sampled positive and negative input voltages is converted. The time required for the T/H to acquire an input signal is determined by how quickly its input capacitance is charged. The required acquisition time lengthens as the input signal's source impedance increases. The acquisition time, t_{ACQ}, is the minimum time needed for the signal to be acquired. It is calculated by the following equation:

$$t_{ACQ} \geq 7.4 \times (R_{SOURCE} + R_{IN}) \times C_{IN} + t_{PU}$$

where:

R_{SOURCE} is the source impedance of the input signal.

R_{IN} = 500Ω, which is the equivalent differential analog input resistance.

C_{IN} = 16pF, which is the equivalent differential analog input capacitance.

t_{PU} = 400ns.

Note: t_{ACQ} is never less than 600ns and any source impedance below 400Ω does not significantly affect the ADC's AC performance.

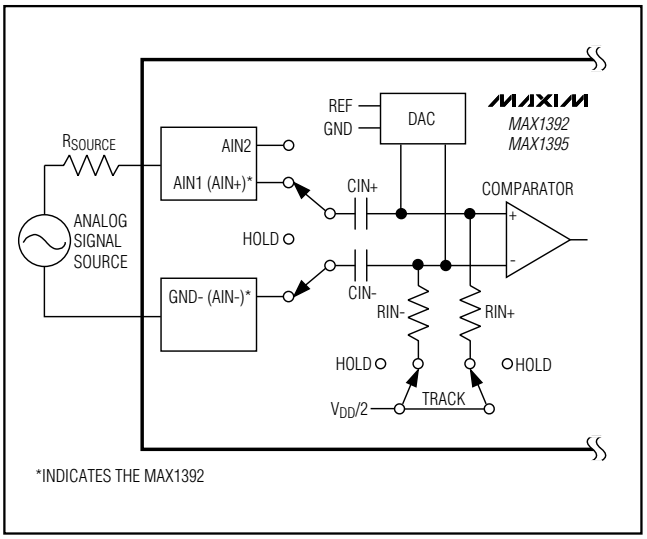


Figure 4. Equivalent Input Circuit

Analog Input Bandwidth

The ADC's input-tracking circuitry has a 4MHz full-power bandwidth, making it possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques.

Use anti-alias filtering to avoid high-frequency signals being aliased into the frequency band of interest.

Analog Input Range and Protection

The MAX1392/MAX1395 produce a digital output that corresponds to the analog input voltage as long as the analog inputs are within their specified range. When operating the MAX1392 in unipolar mode (UNI/$\overline{BIP}$ = 1), the specified differential analog input range is from 0 to V_{REF}. When operating in bipolar mode (UNI/$\overline{BIP}$ = 0), the differential analog input range is from -V_{REF}/2 to +V_{REF}/2 with a common mode range of 0 to V_{DD}. The MAX1395 has an input range from 0 to V_{REF}.

Internal protection diodes confine the analog input voltage within the region of the analog power input rails (V_{DD}, GND) and allow the analog input voltage to swing from GND - 0.3V to V_{DD} + 0.3V without damage. Input voltages beyond GND - 0.3V and V_{DD} + 0.3V forward bias the internal protection diodes. In this situation, limit the forward diode current to less than 50mA to avoid damage to the MAX1392/MAX1395.

Output Data Format

Figures 8, 9, and 10 illustrate the conversion timing for the MAX1392/MAX1395. Fourteen SCLK cycles are required to read the conversion result and data on DOUT transitions on the falling edge of SCLK. The conversion result contains 4 zeros, followed by 10 data bits with the data in MSB-first format. For the MAX1392, data is straight binary for unipolar mode and two's complement for bipolar mode. For the MAX1395, data is always straight binary.

Transfer Function

Figure 5 shows the unipolar transfer function for the MAX1392/MAX1395. Figure 6 shows the bipolar transfer function for the MAX1392. Code transitions occur halfway between successive-integer LSB values.

1.5V to 3.6V, 357ksps, 1-Channel True-Differential/ 2-Channel Single-Ended, 10-Bit, SAR ADCs

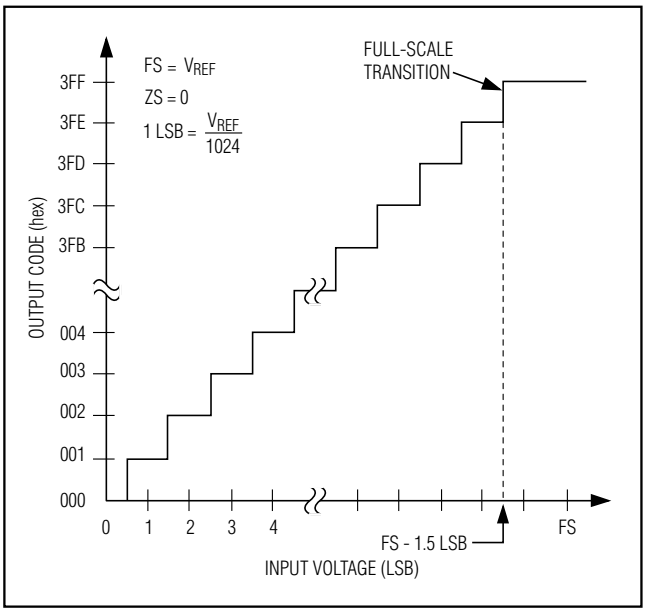


Figure 5. Unipolar Transfer Function

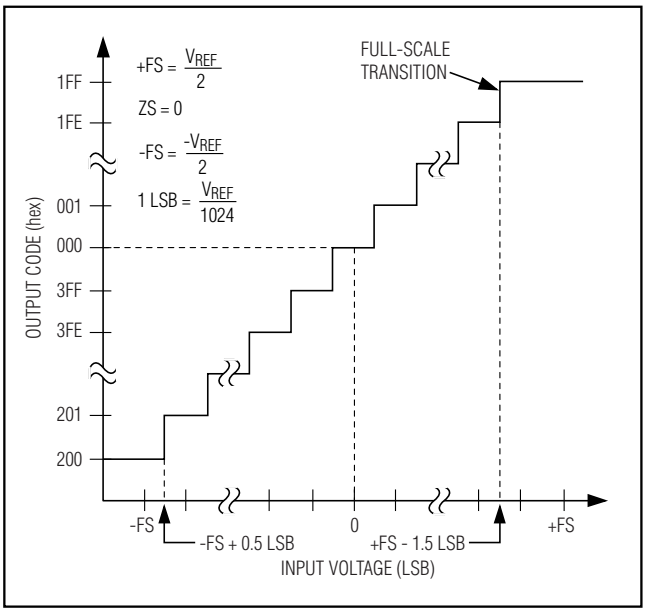


Figure 6. Bipolar Transfer Function

Applications Information

Starting a Conversion

A falling edge on $\overline{CS}$ initiates the power-up sequence and begins acquiring the analog input as long as $\overline{OE}$ is also asserted low. On the 3rd SCLK falling edge, the analog input is held for conversion. The most significant bit (MSB) decision is made and clocked onto DOUT on the 4th SCLK falling edge. Valid DOUT data is available to be clocked into the master (microcontroller (µC)) on the following SCLK rising edge. The rest of the bits are decided and clocked out to DOUT on each successive SCLK falling edge. See Figures 8 and 9 for conversion timing diagrams.

Once a conversion has been initiated, $\overline{CS}$ can go high at any time. Further falling edges of $\overline{CS}$ do not reinitiate an acquisition cycle until the current conversion completes. Once a conversion completes, the first falling edge of $\overline{CS}$ begins another acquisition/conversion cycle.

Selecting Unipolar or Bipolar Mode (MAX1392 Only)

Drive UNI/$\overline{BIP}$ high to select unipolar mode or pull UNI/$\overline{BIP}$ low to select bipolar mode. UNI/$\overline{BIP}$ can be connected to V_{DD} for logic high, to GND for logic low, or actively driven. UNI/$\overline{BIP}$ needs to be stable for t_{UBS} prior to the first rising edge of SCLK after the $\overline{CS}$ falling edge (see Figure 1) for a valid conversion result when being actively driven.

Selecting Analog Input AIN1 or AIN2 (MAX1395 Only)

Pull $\overline{CH1}$/CH2 low to select AIN1 or drive $\overline{CH1}$/CH2 high to select AIN2 for conversion. $\overline{CH1}$/CH2 can be connected to V_{DD} for logic high, to GND for logic low, or actively driven. $\overline{CH1}$/CH2 needs to be stable for t_{CHS} prior to the first rising edge of SCLK after the $\overline{CS}$ falling edge (see Figure 1) for a valid conversion result when being actively driven.

AutoShutdown Mode

The ADC automatically powers down on the SCLK falling edge that clocks out the LSB. This is the falling edge after the 13th SCLK. DOUT goes low when the LSB has been clocked into the master (µC) on the 16th rising SCLK edge.

Alternatively, drive $\overline{OE}$ high to force the MAX1392/MAX1395 into power-down. Whenever $\overline{OE}$ goes high, the ADC powers down and disables DOUT regardless of $\overline{CS}$, SCLK, or the state of the ADC. DOUT enters a high-impedance state after t_{DOD}.

External Reference

The MAX1392/MAX1395 use an external reference between 0.6V and (V_{DD} + 50mV). Bypass REF with a 0.1µF capacitor to GND for best performance (see the *Typical Operating Circuit*).

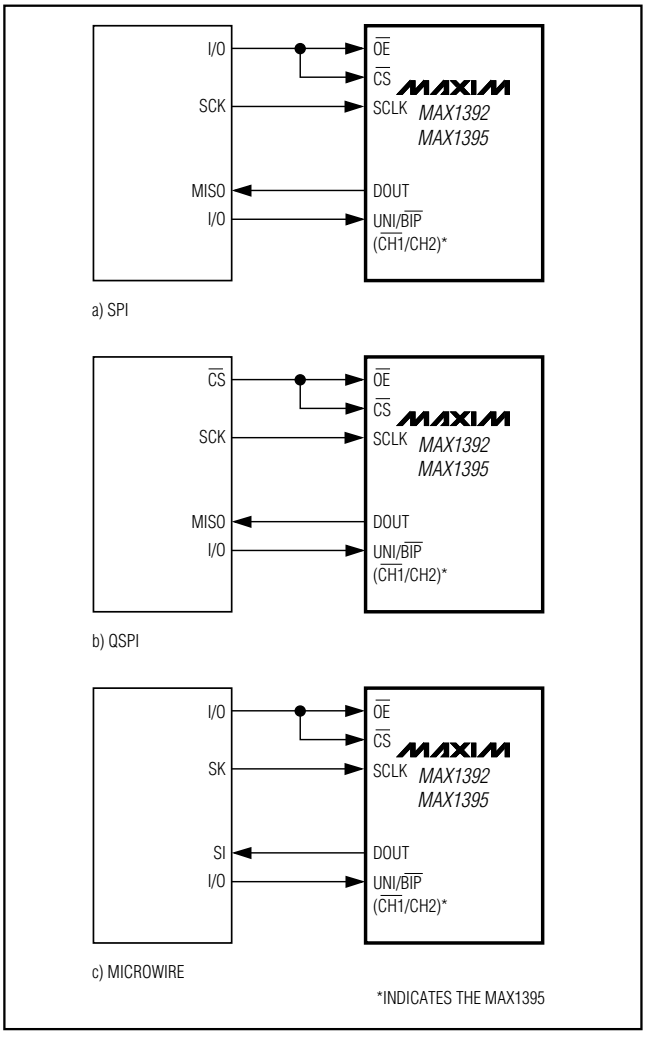


Figure 7. Common Serial-Interface Connections to the MAX1392/MAX1395

Serial Interface

The MAX1392/MAX1395 serial interface is fully compatible with SPI, QSPI, and MICROWIRE (see Figure 7). If a serial interface is available, set the µC's serial interface in master mode so the µC generates the serial clock. Choose a clock frequency between 100kHz and 5MHz. $\overline{CS}$ and $\overline{OE}$ can be connected together and driven simultaneously. $\overline{OE}$ can also be connected to GND if the DOUT bus is not shared and driven independently.

SPI and MICROWIRE

When using SPI or MICROWIRE, make the µC the bus master and set CPOL = 0 and CPHA = 0 or CPOL = 1 and CPHA = 1. (These are the bits in the SPI or MICROWIRE control register.) Two consecutive 1-byte reads are required to get the entire 10-bit result from the ADC. The MAX1392/MAX1395 shut down after clocking the LSB and DOUT becomes high impedance. DOUT transitions on SCLK's falling edge and is clocked into the µC on the SCLK's rising edge. See Figure 7 for connections and Figures 8 and 9 for timing diagrams. The conversion result contains 4 zeros, followed by the 10 data bits with the data in MSB-first format. When using CPOL = 0 and CPHA = 0 or CPOL = 1 and CPHA = 1, the MSB of the data is clocked into the µC on the SCLK's fifth rising edge. To be compatible with SPI and MICROWIRE, connect $\overline{CS}$ and $\overline{OE}$ together and drive simultaneously.

QSPI

Unlike SPI, which requires two 1-byte reads to acquire the 10 bits of data from the ADC, QSPI allows the minimum number of clock cycles necessary to clock in the data. The MAX1392/MAX1395 require a minimum of 14 clock cycles from the µC to clock out the 10 bits of data. See Figure 7 for connections and Figures 8 and 9 for timing diagrams. The conversion result contains 4 zeros, followed by the 10 data bits with the data in MSB-first format. The MAX1392/MAX1395 shut down after clocking out the LSB. DOUT then becomes high impedance. When using CPOL = 0 and CPHA = 0 or CPOL = 1 and CPHA = 1, the MSB of the data is clocked into the µC on the SCLK's fifth rising edge. To be compatible with QSPI, connect $\overline{CS}$ and $\overline{OE}$ together and drive simultaneously.

DSP Interface

Figure 10 shows the timing for DSP operation. Figure 11 shows the connections between the MAX1392/MAX1395 and several common DSPs.

1.5V to 3.6V, 357ksps, 1-Channel True-Differential/ 2-Channel Single-Ended, 10-Bit, SAR ADCs

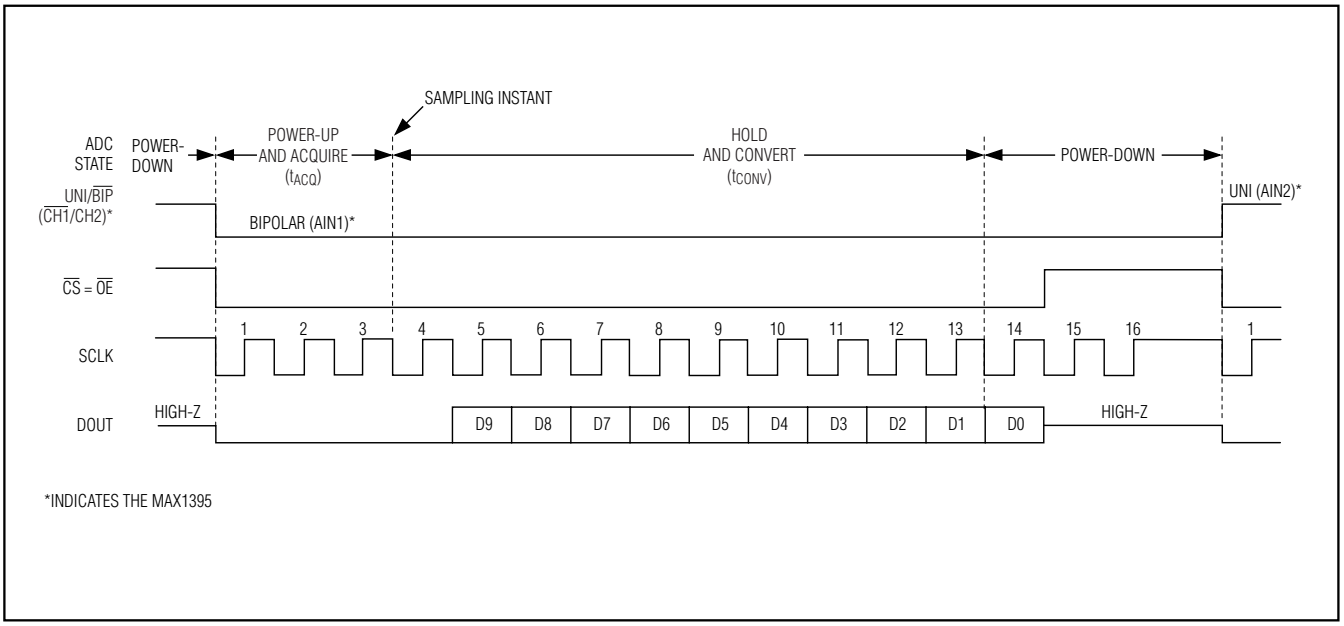


Figure 8. Serial-Interface Timing for SPI/QSPI (CPOL = CPHA = 1) and MICROWIRE (G6 = 0, G5 = 1)

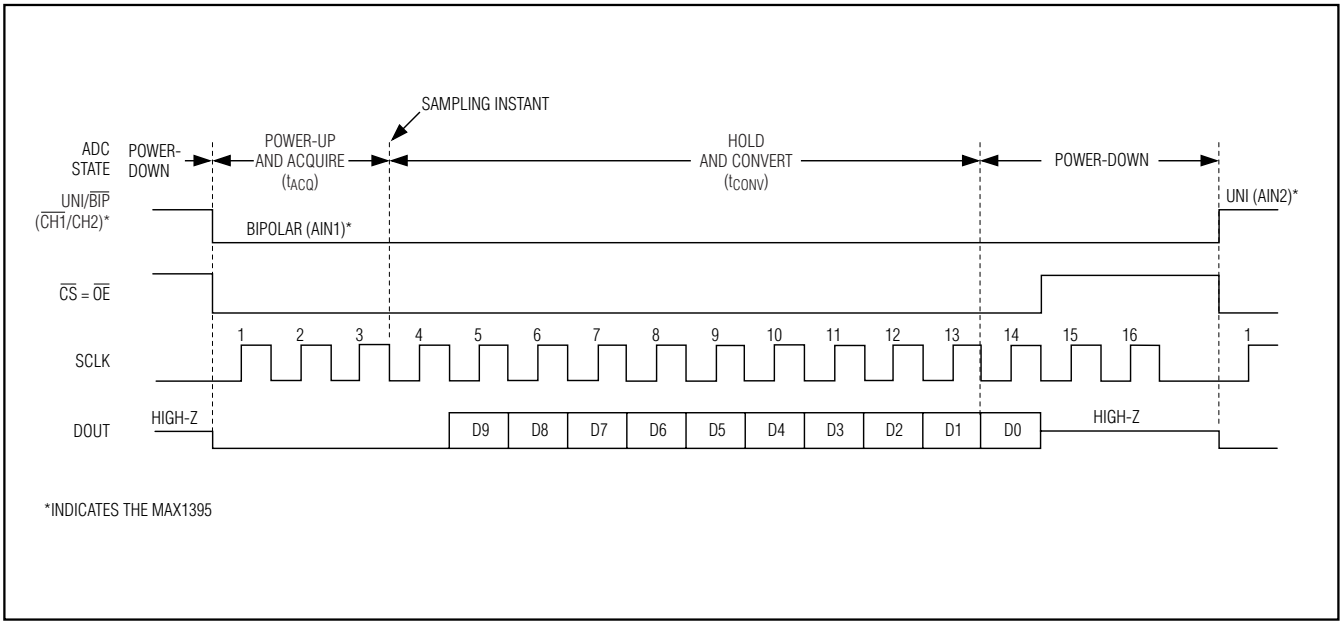


Figure 9. Serial-Interface Timing for SPI/QSPI (CPOL = CPHA = 0) and MICROWIRE (G6 = 0, G5 = 0)

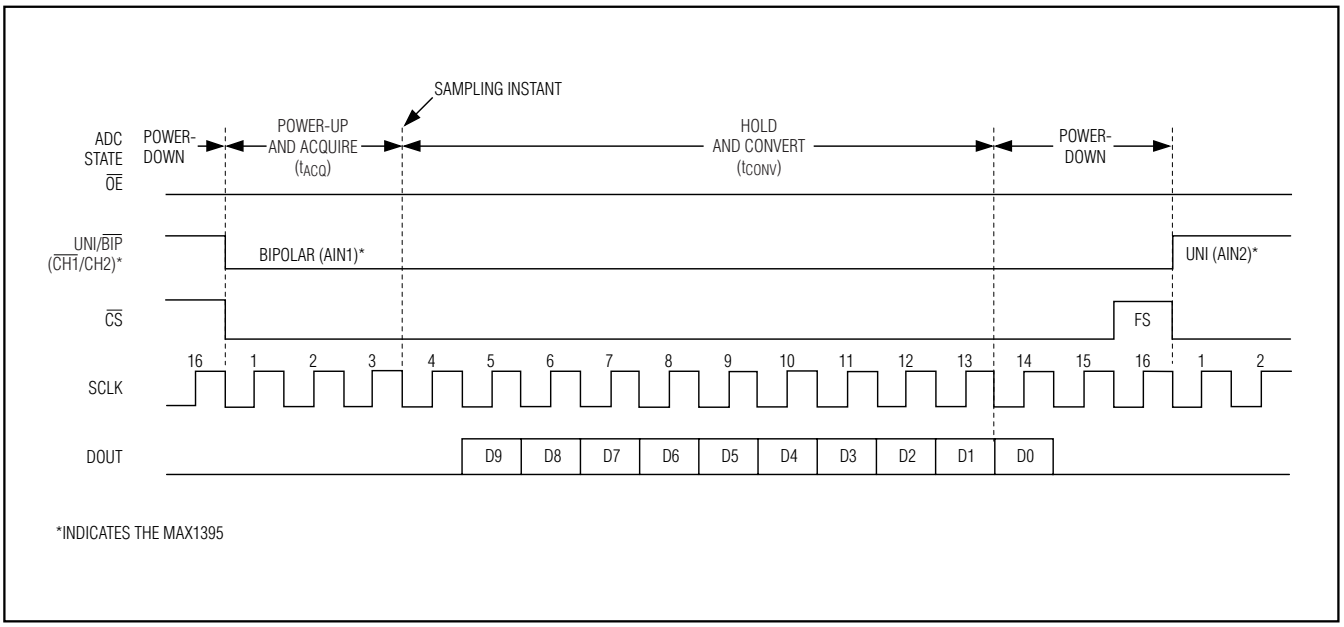


Figure 10. DSP Serial-Timing Diagram

As shown in Figure 11, drive the MAX1392/MAX1395 chip-select input ($\overline{CS}$) with the DSP's frame-sync signal. $\overline{OE}$ may be connected to GND or driven independently. For continuous conversion operation, keep $\overline{OE}$ low and make the $\overline{CS}$ falling edge coincident with the 14th falling edge of the SCLK. Fourteen-bit data transfers can also be performed with compatible DSPs.

Unregulated Two-Cell or Single Lithium $LiMnO_2$ Cell Operation

Low operating voltage (1.5V to 3.6V) and ultra-low-power consumption make the MAX1392/MAX1395 ideal for low cost, unregulated, battery-powered applications without the need for a DC-DC converter. Power the MAX1392/MAX1395 directly from two alkaline/NiMH/NiCd cells in series or a single lithium coin cell as shown in the *Typical Operating Circuit*.

Fresh alkaline cells have a voltage of approximately 1.5V per cell (3V with 2 cells in series) and approach end of life at 0.8V (1.6V with 2 cells in series). A typical 2xAA alkaline discharge curve is shown in Figure 12a. A typical CR2032 lithium ($LiMnO_2$) coin cell discharge curve is shown in Figure 12b.

Layout, Grounding, and Bypassing

For best performance, use PC boards. Board layout must ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

Figure 13 shows the recommended system ground connections. Establish a single-point analog ground (star ground point) at the MAX1392/MAX1395s' GND pin or use the ground plane.

High-frequency noise in the power supply (V_{DD}) degrades the ADC's performance. Bypass V_{DD} to GND with a 0.1µF capacitor as close to the device as possible. Minimize capacitor lead lengths for best supply noise rejection. To reduce the effects of supply noise, a 10Ω resistor can be connected as a lowpass filter to attenuate supply noise.

Exposed Pad

The MAX1392/MAX1395 TDFN package has an exposed pad on the bottom of the package. This pad is not internally connected. Connect the exposed pad to the GND pin on the MAX1392/MAX1395 or leave unconnected for proper electrical performance.

Definitions

Integral Nonlinearity (INL)

INL is the deviation of the values on an actual transfer function from a straight line. For the MAX1392/MAX1395, this straight line is between the end points of the transfer function once offset and gain errors have been nullified. INL deviations are measured at every step and the worst-case deviation is reported in the *Electrical Characteristics* section.

1.5V to 3.6V, 357ksps, 1-Channel True-Differential/ 2-Channel Single-Ended, 10-Bit, SAR ADCs

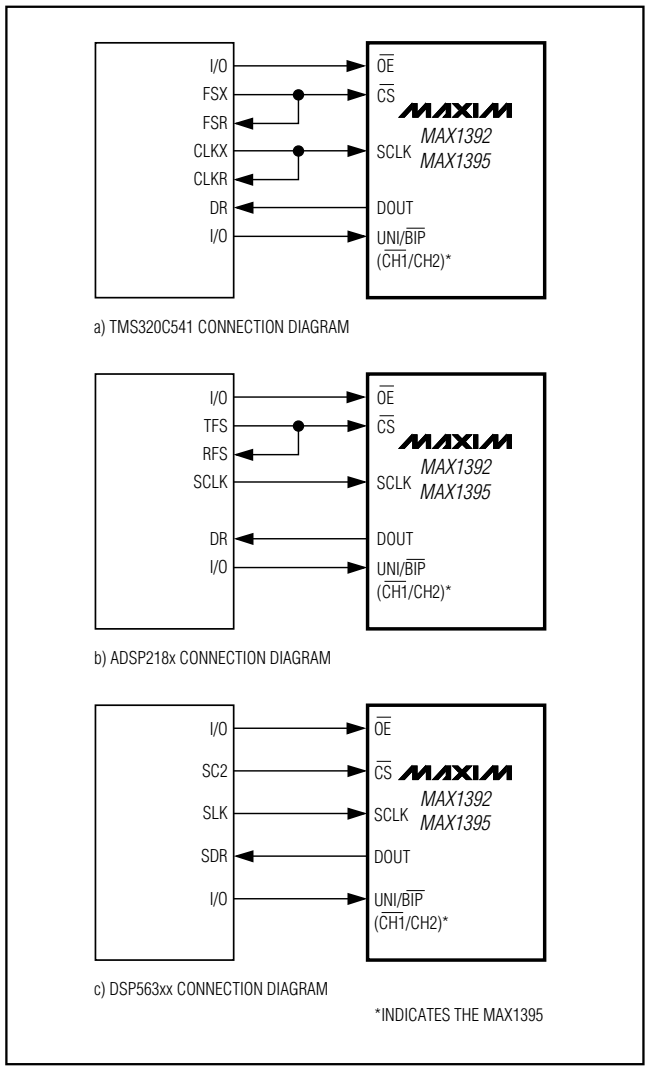


Figure 11. Common DSP Connections to the MAX1392/MAX1395

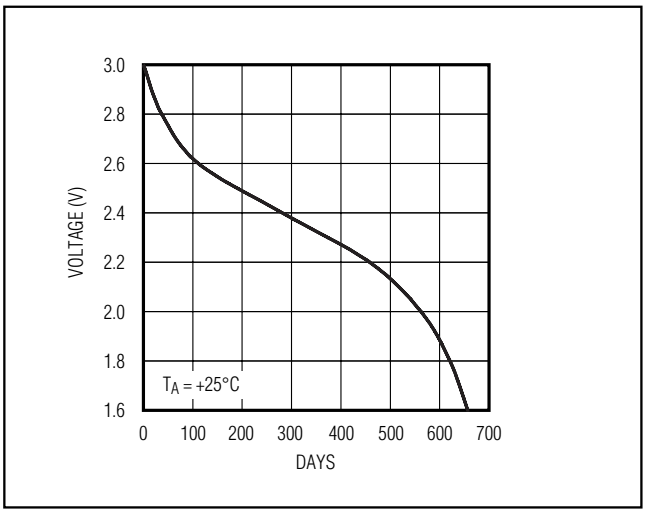


Figure 12a. Typical 2xAA Discharge Curve at 100ksps

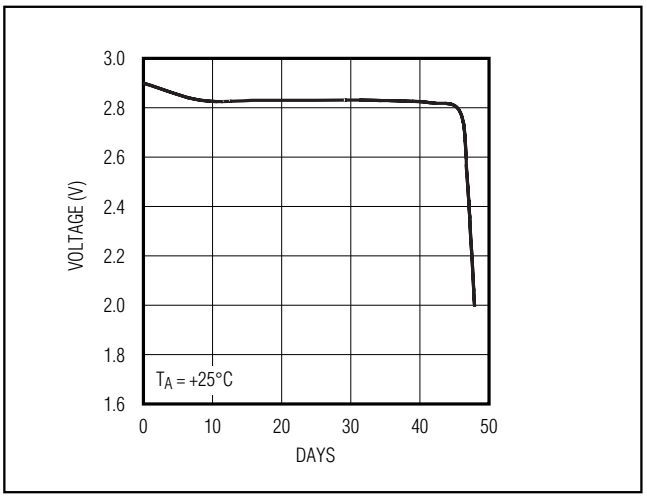


Figure 12b. Typical CR2032 Discharge Curve at 100ksps

Differential Nonlinearity (DNL)

DNL is the difference between an actual step width and the ideal value of 1 LSB. A DNL error specification of less than ±1 LSB guarantees no missing codes and a monotonic transfer function. For the MAX1392/MAX1395, DNL deviations are measured at every step and the worst-case deviation is reported in the *Electrical Characteristics* section.

Signal-to-Noise Plus Distortion (SINAD)

SINAD is computed by taking the ratio of the RMS signal to the RMS noise plus the RMS distortion. RMS noise includes all spectral components to the Nyquist frequency excluding the fundamental, the first five harmonics (HD2–HD6), and the DC offset. RMS distortion includes the first five harmonics (HD2–HD6).

$$SINAD = 20 \times \log\left(\frac{SIGNAL_{RMS}}{\sqrt{NOISE_{RMS}^{2} + DISTORTION_{RMS}^{2}}}\right)$$

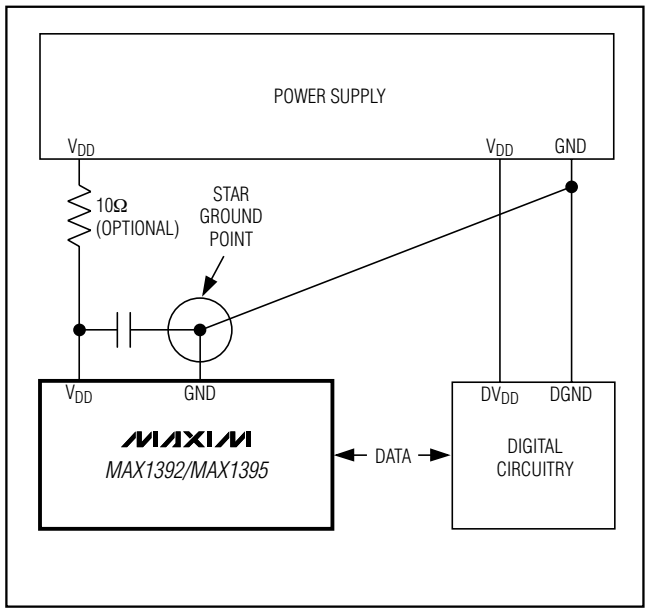


Figure 13. Power-Supply Grounding Connections

Signal-to-Noise Ratio (SNR)

SNR is a dynamic figure of merit that indicates the converter's noise performance. For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR_{dB[max]} = 6.02_{dB} \times N + 1.76_{dB}$$

In reality, there are other noise sources such as thermal noise, reference noise, and clock jitter that also degrade SNR. SNR is computed by taking the ratio of the RMS signal to the RMS noise. RMS noise includes all spectral components to the Nyquist frequency excluding the fundamental, the first five harmonics, and the DC offset.

Total Harmonic Distortion (THD)

THD is a dynamic figure of merit that indicates how much harmonic distortion the converter adds to the signal.

THD is the ratio of the RMS sum of the first five harmonics of the fundamental signal to the fundamental itself. This is expressed as:

$$THD = 20 \times \log\left(\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}\right)$$

where V_1 is the fundamental amplitude, and V_2 through V_6 are the amplitudes of the 2nd- through 6th-order harmonics.

Spurious-Free Dynamic Range (SFDR)

SFDR is a dynamic figure of merit that indicates the lowest usable input signal amplitude. SFDR is the ratio of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next-largest spurious component, excluding DC offset. SFDR is specified in decibels relative to the carrier (dBc).

Intermodulation Distortion (IMD)

IMD is the ratio of the RMS sum of the intermodulation products to the RMS sum of the two fundamental input tones. This is expressed as:

$$IMD = 20 \times \log\left(\frac{\sqrt{V_{IM1}^2 + V_{IM2}^2 + ... + V_{IM3}^2 + V_{IMN}^2}}{\sqrt{V_1^2 + V_2^2}}\right)$$

The fundamental input tone amplitudes (V_1 and V_2) are at -6.5dBFS. Fourteen intermodulation products ($V_{IM\_}$) are used in the MAX1392/MAX1395 IMD calculation. The intermodulation products are the amplitudes of the output spectrum at the following frequencies, where f_{IN1} and f_{IN2} are the fundamental input tone frequencies:

- 2nd-order intermodulation products:
  $f_{IN1} + f_{IN2}$, $f_{IN2} - f_{IN1}$
- 3rd-order intermodulation products:
  $2 \times f_{IN1} - f_{IN2}$, $2 \times f_{IN2} - f_{IN1}$, $2 \times f_{IN1} + f_{IN2}$, $2 \times f_{IN2} + f_{IN1}$
- 4th-order intermodulation products:
  $3 \times f_{IN1} - f_{IN2}$, $3 \times f_{IN2} - f_{IN1}$, $3 \times f_{IN1} + f_{IN2}$, $3 \times f_{IN2} + f_{IN1}$
- 5th-order intermodulation products:
  $3 \times f_{IN1} - 2 \times f_{IN2}$, $3 \times f_{IN2} - 2 \times f_{IN1}$, $3 \times f_{IN1} + 2 \times f_{IN2}$, $3 \times f_{IN2} + 2 \times f_{IN1}$

Channel-to-Channel Crosstalk

Channel-to-channel crosstalk indicates how well each analog input is isolated from the others. The channel-to-channel crosstalk for the MAX1395 is measured by applying DC to channel 2 while an AC sine wave is applied to channel 1. An FFT is taken for channel 1 and channel 2 and the difference (in dB) is reported as the channel-to-channel crosstalk.

1.5V to 3.6V, 357ksps, 1-Channel True-Differential/ 2-Channel Single-Ended, 10-Bit, SAR ADCs

Aperture Delay

The MAX1392/MAX1395 sample data on the falling edge of its third SCLK cycle (Figure 14). In actuality, there is a small delay between the falling edge of the sampling clock and the actual sampling instant. Aperture delay (t_{AD}) is the time defined between the falling edge of the sampling clock and the instant when an actual sample is taken.

Aperture Jitter

Aperture jitter (t_{AJ}) is the sample-to-sample variation in the aperture delay (Figure 14).

DC Power-Supply Rejection Ratio (PSRR)

DC PSRR is defined as the change in the positive full-scale transfer function point caused by a full range variation in the analog power-supply voltage (V_{DD}).

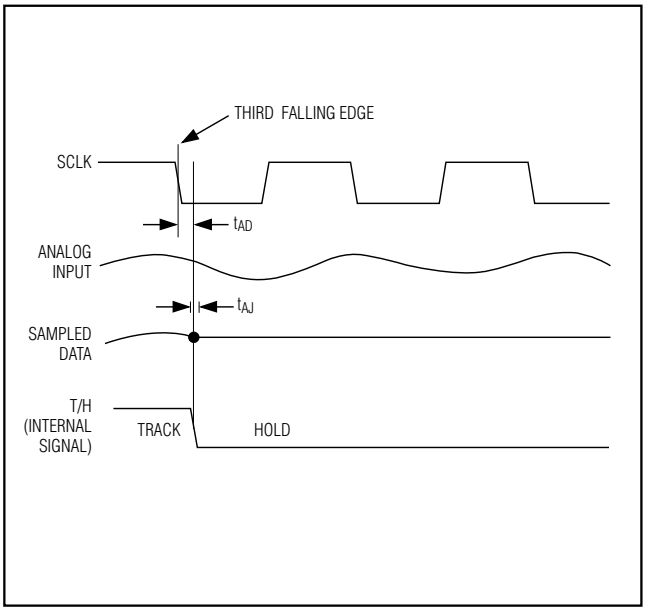


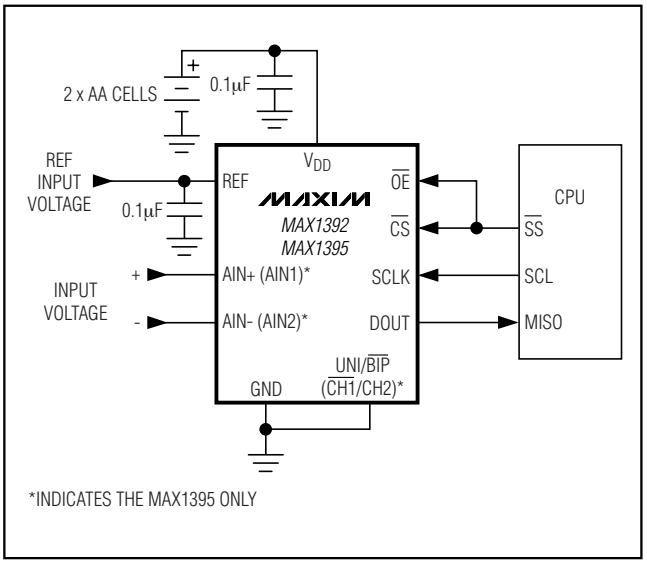
Figure 14. T/H Aperture Timing

Chip Information

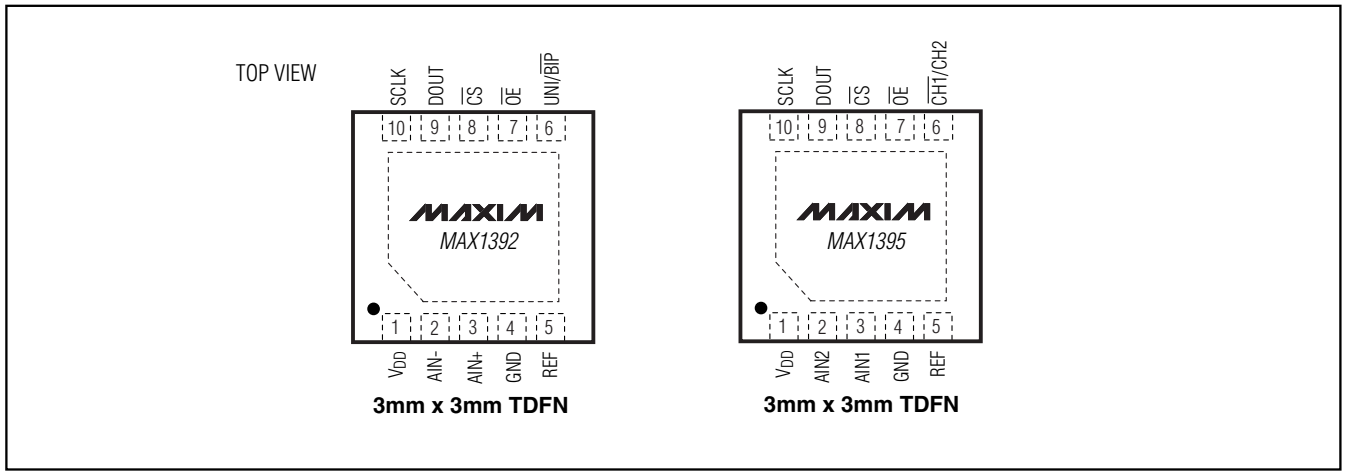
TRANSISTOR COUNT: 9106

PROCESS: BiCMOS

Typical Operating Circuit



Pin Configurations



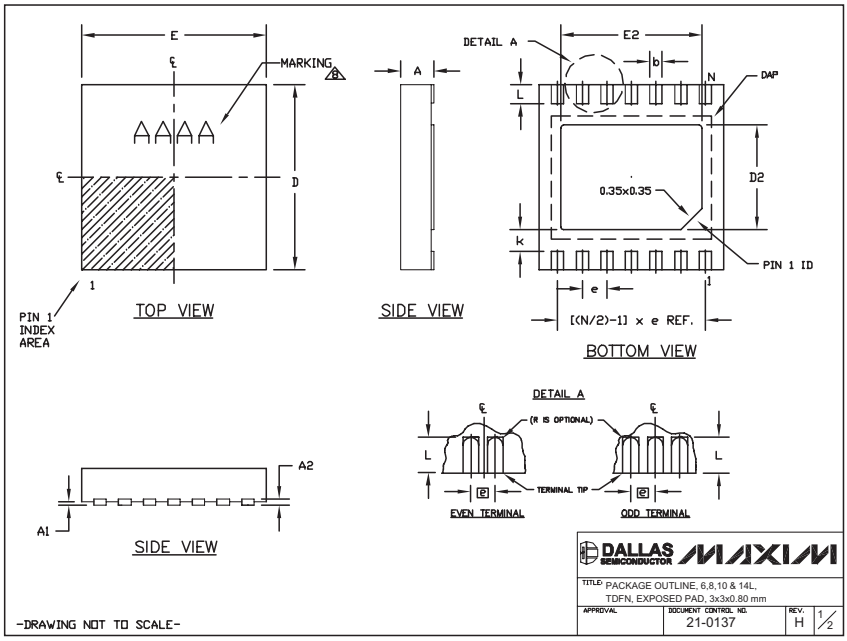
Revision History

Pages changed at Rev 2: 1, 3, 8, 13, 14, 18

1.5V to 3.6V, 357ksps, 1-Channel True-Differential/ 2-Channel Single-Ended, 10-Bit, SAR ADCs

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-1	6	1.50–0.10	2.30–0.10	0.95 BSC	MO229 / WEEA	0.40–0.05	1.90 REF
T633-2	6	1.50–0.10	2.30–0.10	0.95 BSC	MO229 / WEEA	0.40–0.05	1.90 REF
T833-1	8	1.50–0.10	2.30–0.10	0.65 BSC	MO229 / WEEC	0.30–0.05	1.95 REF
T833-2	8	1.50–0.10	2.30–0.10	0.65 BSC	MO229 / WEEC	0.30–0.05	1.95 REF
T833-3	8	1.50–0.10	2.30–0.10	0.65 BSC	MO229 / WEEC	0.30–0.05	1.95 REF
T1033-1	10	1.50–0.10	2.30–0.10	0.50 BSC	MO229 / WEED-3	0.25–0.05	2.00 REF
T1033-2	10	1.50–0.10	2.30–0.10	0.50 BSC	MO229 / WEED-3	0.25–0.05	2.00 REF
T1433-1	14	1.70–0.10	2.30–0.10	0.40 BSC	----	0.20–0.05	2.40 REF
T1433-2	14	1.70–0.10	2.30–0.10	0.40 BSC	----	0.20–0.05	2.40 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

DALLAS SEMICONDUCTOR MAXIM
TITLE: PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm
APPROVAL
DOCUMENT CONTROL NO. 21-0137
REV. H
2/2
-DRAWING NOT TO SCALE-