

IW4502B

Strobed Hex Inverter/Buffer
High-Voltage Silicon-Gate CMOS

The IW4502B consists of six inverter/buffers with 3-state outputs. A logic "1" on the OUTPUT ENABLE input produces a high impedance state in all six outputs. This feature permits common busing of the outputs, thus simplifying system design. A logic "1" on the DIRECTION input switches all six outputs to logic "0" if the OUTPUT ENABLE input is a logic "0".

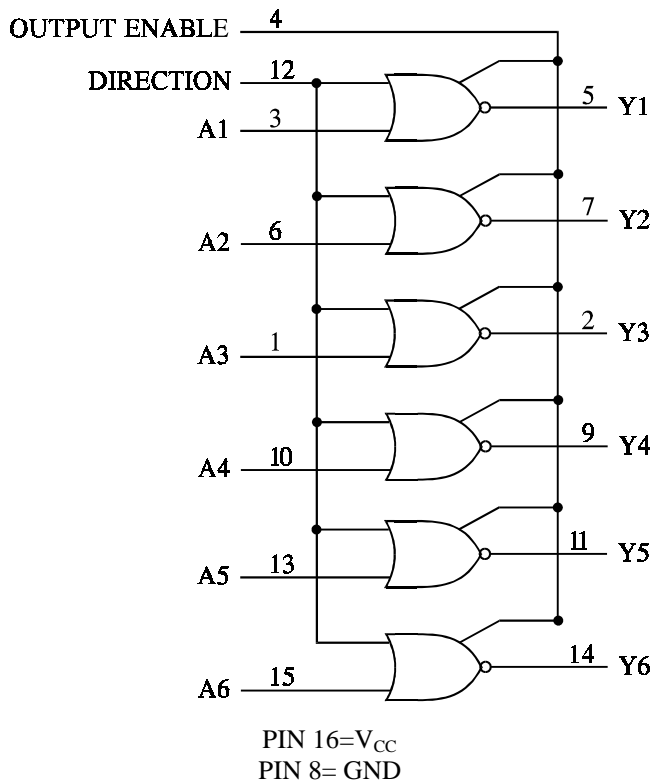
- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
 - 1.0 V min @ 5.0 V supply
 - 2.0 V min @ 10.0 V supply
 - 2.5 V min @ 15.0 V supply

N SUFFIX PLASTIC

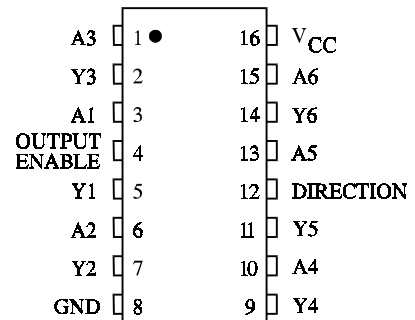
D SUFFIX SOIC

ORDERING INFORMATION
 IW4502BN Plastic
 IW4502BD SOIC
 $T_A = -55^\circ$ to 125° C for all packages

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Output
Output Enable	Direction	A	Y
L	L	L	H
L	L	H	L
L	H	X	L
H	X	X	Z

Z = high impedance
 X = don't care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V _{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
V _{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{IN}	DC Input Current, per Pin	±10	mA
P _D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
P _D	Power Dissipation per Output Transistor	100	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	3.0	18	V
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).
Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				≥-55°C	25°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} =0.5 V V _{OUT} =1 V V _{OUT} =1.5	5.0	3.5	3.5	3.5	V
			10	7	7	7	
			15	11	11	11	
V _{IL}	Maximum Low-Level Input Voltage	V _{OUT} = V _{CC} - 0.5V V _{OUT} = V _{CC} - 1.0 V V _{OUT} = V _{CC} - 1.5V	5.0	1.5	1.5	1.5	V
			10	3	3	3	
			15	4	4	4	
V _{OH}	Minimum High-Level Output Voltage	V _{IN} =GND	5.0	4.95	4.95	4.95	V
			10	9.95	9.95	9.95	
			15	14.95	14.95	14.95	
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} = V _{CC}	5.0	0.05	0.05	0.05	V
			10	0.05	0.05	0.05	
			15	0.05	0.05	0.05	
I _{IN}	Maximum Input Leakage Current	V _{IN} = GND or V _{CC}	18	±0.1	±0.1	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} = GND or V _{CC}	5.0	1	1	30	μA
			10	2	2	60	
			15	4	4	120	
			20	20	20	600	
I _{OL}	Minimum Output Low (Sink) Current	V _{IN} = GND or V _{CC} U _{OL} =0.4 V U _{OL} =0.5 V U _{OL} =1.5 V	5.0	3.84	3.06	2.16	mA
			10	9.6	7.8	5.4	
			15	25.2	20.4	14.4	
I _{OH}	Minimum Output High (Source) Current	V _{IN} = GND or V _{CC} U _{OH} =2.5 V U _{OH} =4.6 V U _{OH} =9.5 V U _{OH} =13.5 V	5.0	-2	-1.6	-1.15	mA
			5.0	-0.64	-0.51	-0.36	
			10	-1.6	-1.3	-0.9	
			15	-4.2	-3.4	-2.4	
I _{OZ}	Maximum Tree-State Leakage Current	Output in High-Impedance State V _{IN} = GND or V _{CC} V _{OUT} = GND or V _{CC}	18	±0.4	±0.4	±12	μA

AC ELECTRICAL CHARACTERISTICS($C_L=50\text{pF}$, $R_L=200\text{k}\Omega$ unless otherwise specified, Input $t_r=t_f=20\text{ ns}$)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			$\geq -55^\circ\text{C}$	25°C	$\leq 125^\circ\text{C}$	
t_{PHL}	Maximum Propagation Delay, Input A or Direction to Output Y (Figure 1)	5.0	270	270	540	ns
		10	120	120	240	
		15	80	80	160	
t_{PLH}	Maximum Propagation Delay, Input A or Direction to Output Y (Figure 1)	5.0	380	380	760	ns
		10	180	180	360	
		15	130	130	260	
t_{PHZ}	Maximum Propagation Delay, Output Enable to Output Y (Figure 2) $R_L = 1\text{ k}\Omega$	5.0	120	120	240	ns
		10	80	80	160	
		15	60	60	120	
t_{PZH}	Maximum Propagation Delay, Output Enable to Output Y (Figure 2) $R_L = 1\text{ k}\Omega$	5.0	220	220	440	ns
		10	100	100	200	
		15	80	80	160	
t_{PLZ}	Maximum Propagation Delay, Output Enable to Output Y (Figure 2) $R_L = 1\text{ k}\Omega$	5.0	250	250	500	ns
		10	130	130	260	
		15	110	110	220	
t_{PZL}	Maximum Propagation Delay, Output Enable to Output Y (Figure 2) $R_L = 1\text{ k}\Omega$	5.0	250	250	500	ns
		10	110	110	220	
		15	80	80	160	
t_{TLH}	Maximum Output Transition Time, Any Output (Figure 1)	5.0	200	200	400	ns
		10	100	100	200	
		15	80	80	160	
t_{THL}	Maximum Output Transition Time, Any Output (Figure 1)	5.0	120	120	240	ns
		10	60	60	120	
		15	40	40	80	
C_{IN}	Maximum Input Capacitance	-		7.5		pF
C_{OUT}	Maximum Tree-State Output Capacitance (Output in High-Impedance State)	-		15		pF

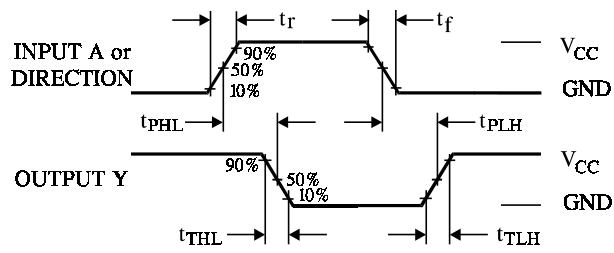


Figure 1. Switching Waveforms

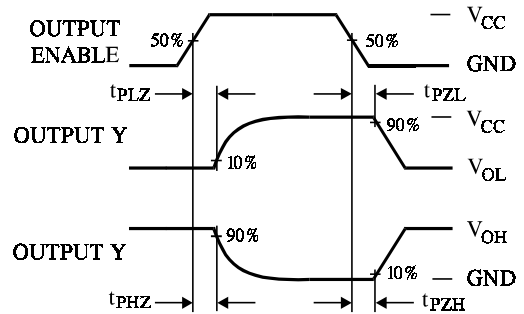


Figure 2. Switching Waveforms

**EXPANDED LOGIC DIAGRAM
(1/6 of the Device)**

